# Digitally-scalable Transformer-combining Power Amplifier Techniques

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**Abstract**

## Digitally-scalable Transformer-combining Power Amplifier Techniques

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The need for seamless connectivity in handheld and tablet devices is driving the integration of high data-rate radios on to SoCs implemented on deeply scaled CMOS processes. Current and emerging wireless standards such as WiFi and 4G (WiMAX and LTE) are based on complex modulations such as OFDM for spectral efficiency reasons. The watt-level peak powers and large peak-to-average power ratios required by these standards present significant efficiency and linearity challenges to the design of CMOS PAs. As a result, power amplifiers remain the dominant power consumption and integration bottleneck today. This dissertation proposes novel techniques for efficiently combining the outputs of power amplifiers to achieve high output power with good efficiency at back-off. By dynamically reconfiguring the power combining network, we minimize the passive losses at back-off. This technique only uses CMOS thin-gate digital transistors as switches and the single nominal digital supply making it compatible with SoC integration. Additionally, the

performance is expected to improve with process scaling. The integrated matching network is based on transformer combining and is inherently broadband.

A 2.5 GHz digitally-scalable transformer combining power amplifier (DST-PA) is implemented in a 32 nm CMOS process as a proof of concept. An inverter-based class-D PA topology is utilized to obtain low output impedance and good linearity. The fabricated stand alone DST-PA in simulation delivers 26 dBm peak CW power with 39% total system Power Added Efficiency (includes all drivers). Average OFDM power is 21 dBm with efficiency 37% when transmitting WiFi signals with PA pre-distortion. The integrated PA with the digital phase modulator is packaged in a flip-chip BGA package. Good linearity performance (ACPR and EVM) demonstrates the applicability of the proposed power combined configurations.

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# Dedication

To my parents

# 1 Introduction

The standards with high Peak to Average ratio like WiFi, 4G (Wimax and LTE) requires high output power while maintaining high efficiency at backoff. CMOS processes are well-suited for large-scale integration and low-cost and form-factor communication devices. They are well-suited for digital design, however presents challenges for RF integration. Specifically, power amplifiers have yet to achieve a high power and efficiency on CMOS implementations, due to low device breakdown voltage and lossy passive components in CMOS process. Recently, transformer combining has been proposed [1], [2], [3] to obtain higher Watt-level output powers with CMOS power amplifiers. However, achieving both high efficiency and power combining is yet to be solved with transformer combining, especially at deep back off power level. This dissertation proposes a novel and efficient technique of a digitally reconfigurable transformer combiner called digitally-scalable switched transformer combining power amplifier (DST-PA), for efficiently combining of the power amplifiers to achieve watt level output power with the best known until this date back-off efficiency for a Wifi/Wimax/LTE standards and fully integrated (including the output matching network) on CMOS process. As a result, not only a high power would have achieved but also it is an efficient way of combining at average power leading to highly efficient (battery life) design across wide power range.

Two prototypes of this proposed technique have been taped-out and will be tested in the lab to prove the concept. This technique uses only thin-gate digital switches and a single

nominal 1-V supply making it compatible with current state-of-the-art digital CMOS processes. Further, the performance is expected to improve with scaling.

This dissertation is organized as follows. Chapters 2 and 3 provide a brief survey of the current techniques in use for CMOS power amplifiers and transformer combiners. From this survey, it will be apparent that switching power amplifiers have the potential to achieve high efficiency with good linearity. However, the switching nature of the PAs results in significant harmonic energy which requires external filters contributing to cost and loss. Chapter 4 introduces the concept of a harmonic rejection power amplifier which can address the issue of the harmonics. The concept of harmonic rejection [4] for mixers is extended to power amplifiers. The theoretical analysis and system level simulation of this approach is presented. It will focus on the effect of harmonic rejection on the LO harmonics as well as the PA non-linearity. These calculations and simulations will demonstrate that this technique is very effective at reducing the harmonics of the LO signal at the output of the PA, thereby relaxing the off-chip filtering requirements. However it cannot cancel out the intermodulation components from the PA non-linearity itself. Chapter 5 will introduce the proposed reconfiguration technique for transformer combining in such an efficient way to reduce the passive losses during the back off. The theory of operation and the predicted efficiency and linearity are presented along with the details of how the desired resolution and dynamic switching are implemented at the transistor and layout level. One prototype include the stand alone PA which benefits the freedom of the looking into different switching schemes through an on chip Look Up Table (LUT) and will be tested with the custom probes and the other prototype is being integrated with the whole polar phase-modulator to constitute a fully integrated up to the antenna digital transmitter for wifi standard. Both prototypes have been

taped-out in 32nm CMOS process and fully post extracted verified with OFDM modulated signal. Measurement results are summarized. Finally, Chapter 6 concludes this dissertation.

# 2 Power Amplifier

The Power Amplifier (PA) is a critical block in the transmit chain of an RFIC. This chapter reviews some background in the field of power amplifiers. PAs amplify the desired RF transmit signal to a high enough power level at the antenna port that a remote receiver can demodulate the signal with adequate SNR. For example in WiFi, a PA is required to deliver an average power of about 100mW into a 50ohm load. The efficiency of the power amplifier is the key determining factor in the battery life on account of the high power it delivers. At the same time the PA is required to be very linear in order to process complex modulations such as OFDM with good modulation quality (EVM). As a result, recent literature has focused on designing highly linear, highly efficient PAs in CMOS processes for SoC integration.

PAs can be classified into two categories based on their mode of operation. The first groups of the PAs are the linear or transconductanse-based PAs which ideally act as a voltage controlled current source. The second categories are the switching based PAs which ideally act as a voltage source in the on and off state with the source resistance equal to the transistor's linear resistance. The two types of PAs will be reviewed briefly in section 2.1 and 2.2 respectively. Switching PAs are more power efficient but they are also more non-linear since they essentially produce only two output states. There are several techniques to improve the linearity of a PA. Digital predistortion takes advantage of digital processing power to linearize the characteristic of a conventional, mildly non-linear power amplifier and improve efficiency by allowing operation at a smaller back-off. Envelope tracking (ET) techniques can be used to adjust the power supply of a linear

PA to maintain optimum efficiency at all power levels [6]. In an Envelope Elimination and Restoration (EER) transmitter [7], an efficient switching PA is used to process the phase information, while the amplitude is introduced via supply modulation. Finally, the outphasing architecture [5][8][9] decomposes the PA input signal into two constant amplitude components that are efficiently processed through switching power amplifiers whose outputs are then combined together. Sections 2.3 and 2.4 briefly cover the two later methods. Sections 2.5 and 2.6 review two recent implementations of polar modulations. More detailed information on Power amplifiers can be found on these references [10] [11] [12].

## 2.1 Linear PA

The linear PAs as their names indicate have output power which scales fairly linearly with input power. In this group of PAs, the active device is used as a current source and so they are also often referred to as transconductance PAs. Class-A, AB, B and C are four classical types of linear PAs. From class-A to C, the bias of the transistor is progressively adjusted from always conducting (in linear gain mode) all the way to conducting for a very short duration near the peaks of the input signal. The concept of conduction angle proposed for a way to improve the efficiency with minimum linearity degradation. The conduction angle of 360 degree means PA is on during the whole period (drawing current constantly). The conduction angle is 360 degree in class-A to 180 degree in class B and in between of 180 to 360 for class AB and less than 180 degree in class C. The theoretical max drain efficiency

(which is defined as output power divided by the dc supply power) of class-A is 50% and the efficiency linearly degrades with output power since the PA is biased to draw a fixed current irrespective of the output power. Due to losses in the matching network and accounting for the I-V characteristics of real transistors, a practical peak efficiency of the class A is about 20% to 30%. The maximum efficiency of class-B is $\pi/4$ ~ 78.5%. Ideal class-B is perfectly linear but in practice since the PA transistor does not remain an ideal transconductor at moderate and weak inversion and can also end up going into triode region with large swings, class-B operation ends up being more non-linear than class-A. Class-AB is more nonlinear but has better efficiency than class-A, and so makes is more attractive than other classes in the linear PA group. Class-C has close to 100% efficiency at very low (~zero) output power which makes it unsuitable for high output power applications but can be useful in bio-medical or low-power applications.

## 2.2 Switching PA

In the linear PAs in section 2.1, the output power is modulated by changing the swing at the input to the PA transconductor device. However, in switching PAs, the transistor acts as a switch which is either on or off. As a result they generally deliver a fixed output power. An example of a switching PAs is shown in Figure 2-1. A class-D PA is one of the types of switching PAs and it can be think of a voltage-controlled switch and a filtering tank. As the name implies, the output switches between the vdd and ground and so has a square wave shape which contains energy at the fundamental tone as well as its harmonics. The LC tank presents the proper impedance at the fundamental frequency and high impedance at the

harmonics. Like other switching PAs the ideal drain efficiency of the class-D PAs at peak is 100% with ideal matching network. Due to the nature of the switch this amplifier does not track the envelope of the input signal and so additional techniques are required to add the amplitude information for a non-constant envelope modulated signal. In practical class-D PAs, the crowbar current limits the peak efficiency below 100%. Due to finite rise and fall time of the output signal there is always a window of the time for both pmos and nmos device to draw current at the same time, also referred to as short circuit current. Using non-overlapping input signals mitigates this problem at the expense of a linearity hit. Losses in the output matching network also contribute to a lower peak efficiency.

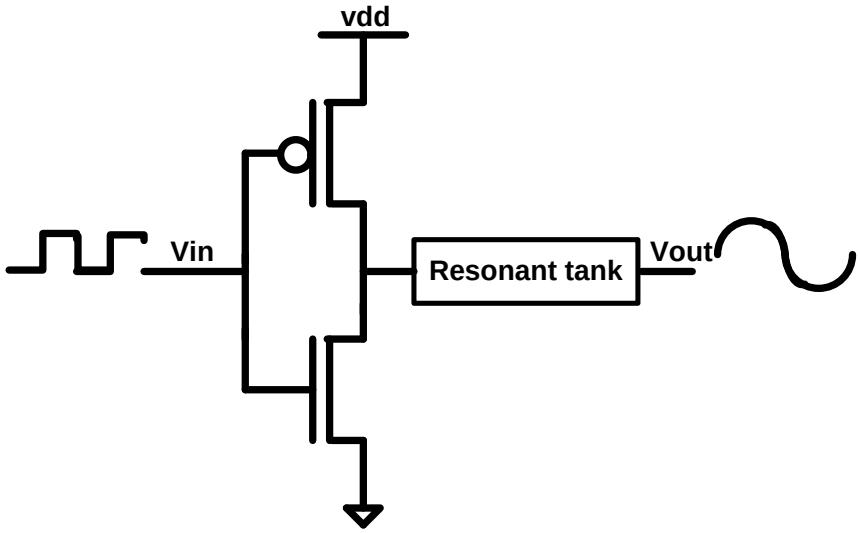



**Fig. 2-1: Class-D PA.**

## 2.3 Polar Modulation

Polar modulation [11] has become popular in the past ten years, was originally called "envelope elimination and restoration" (EER) [13]. The RF input signal is divided into two paths, envelope and phase path which are operating at different frequencies. The envelope signal modulates the supply voltage of a switching PA and so provides a linear amplitude technique and phase signal is applied to the input of the power amplifier switch as shown in

fig. 2-2. Since the RF phase modulation is applied to a switching PA therefore this technique offers good efficiency. The distortion in this technique is due to mismatch between the signal paths after they combine together.

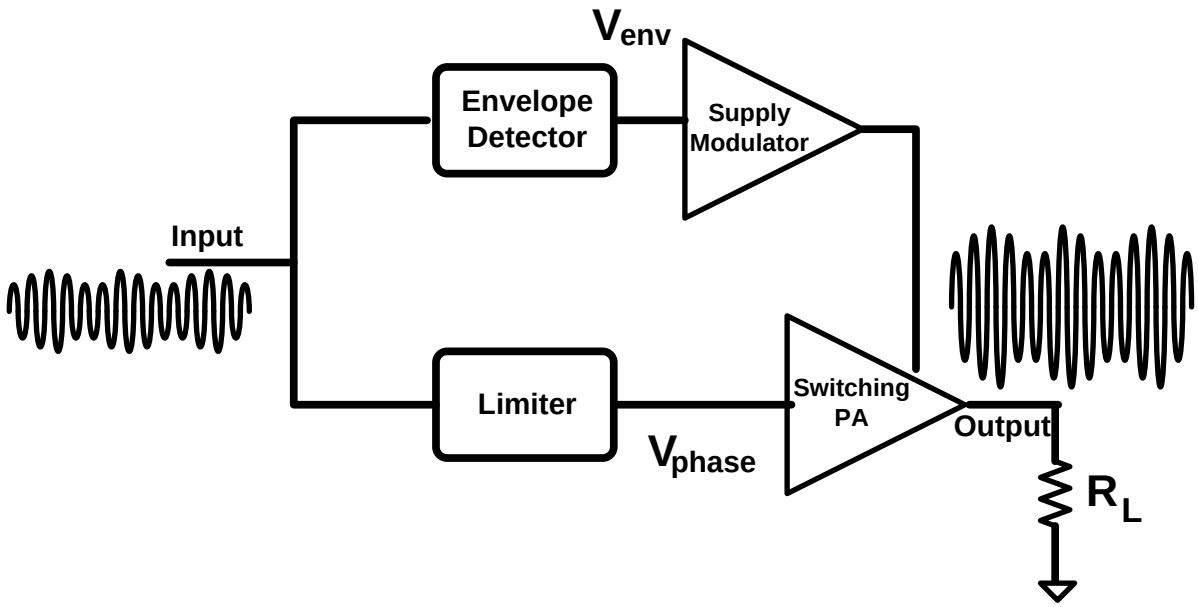



**Fig. 2-2: Envelope Elimination and Restoration (EER), original Kahn.**

The improved version of the polar modulation is shown in fig. 2-3, which instead of decomposing the RF signal into envelope and phase, extracts the amplitude/phase information digitally in the baseband (BB). A DSP operation directly converts the desired transmit baseband signal to its polar representation. A CORDIC (Coordinate Rotation Digital Computer) algorithm in the BB implements this co-ordinate conversion. The digital envelope signal is applied to the PA supply through a DAC and the phase path is up-converted through a mixer before going into the PA.

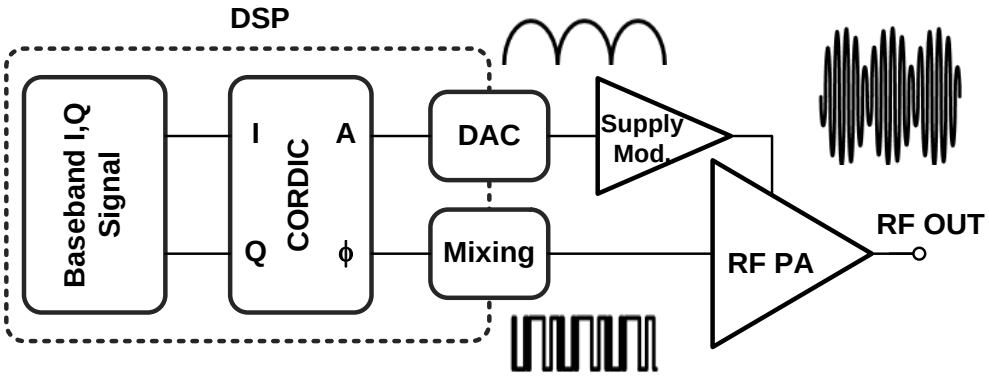



**Fig. 2-3: Modern Kahn.**

## 2.4 Outphasing Modulation

One limitation of polar modulation is that the two signal components go through different circuitry and it has been difficult historically to match them in timing to the level required for good EVM and spectral mask performance. Also supply modulators have been difficult to design for low spurs and high current delivery and efficiency. However, another architecture called “Outphasing” [8] and “linear amplification with nonlinear components” (LINC) [14] decomposes a variable-envelope signal into two constant-envelope waveforms Fig. 2-4. Outphasing can operate with completely nonlinear PA stages and it does not require supply modulation, making it easier to implement in monolithic ICs. However, summation of the outputs in the outphasing technique causes power loss.

The other issue is the signal traveling in one PA may affect the other one causing the spectral re-growth and corruption of the modulation information. Also, the combining of the two paths has to be done efficiently so to minimize the loss of the combiner. Some of these

problems have been solved or improved by employing class-D switches with non-isolating transformer combining which are well suited to scaled technology [15].

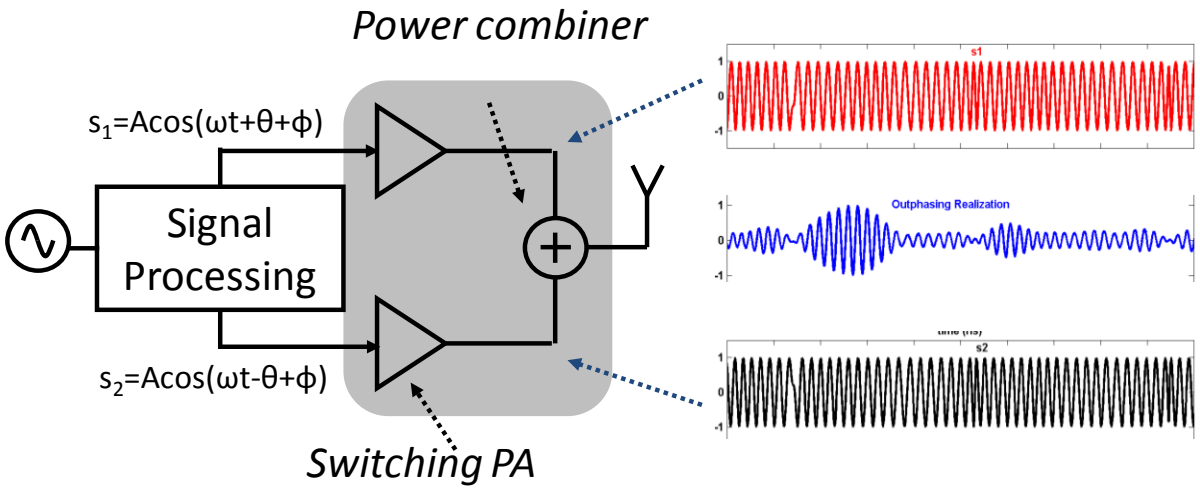



**Fig. 2-4: Outphasing Architecture.**

## 2.5 Digitally-Modulated PA

Digitally-Modulated PA, mitigates some of the issues with the polar modulation by removing the supply modulator. The supply modulator not only takes extra area and power but also it is narrow band which limits the performance of the polar PAs. Also, with the trends of moving into the more digitally friendly designs, makes this technique more attractive than other techniques. In section 2.3, fig. 2-3 briefly reviewed a trend of this technique which is also called modern Kahn.

Wider bandwidths can be achieved with another type of DPA. [16] proposes a digitally modulated PA, which can be understood as implementing the same function as a

current steering DAC. As the individual PA units turn on, based on the amplitude signal, their currents add up at the output to achieve the amplitude modulation (fig. 2-5). Aside from the wider bandwidth, this also mitigates the signal distortion in polar transmitters since the envelope and phase of the signal are combined together at the same cell and can be better matched by construction. Since, in this technique, the cells are turned on and off based on the digital amplitude code, the current drawn is proportional to the output voltage. Since voltage is square root of power, then the efficiency of this technique has a square root relation to the output power, makes it superior to the prior linear PA techniques. However, its linearity is compromised by low output impedance in the current cells (just as with any current steering DAC). So the cells have to be designed with a high output impedance. On the other hand, the PA has to support a high output voltage to achieve high output power levels. A large swing can drive the transistor stack into triode or can at least modulate the operating point (Vds and therefore *rout*) of the active device causing non-linearity at high power level. Therefore, usually additional linearization techniques are need like pre-distortion. Other issues in these PAs include quantization noise and sampling images. This further is addressed in later chapters. Sampling and the finite quantization levels of the PA produce images and quantization noise which corrupt the output spectrum. Eventually, the resolution and amplitude sampling rate required of the digital PA is determined by the EVM and spectral mask requirements.

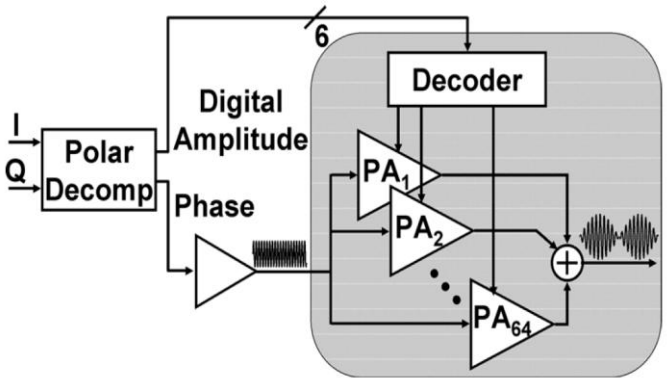



**Fig. 2-5: DPA with 6-bit power DAC ($PA_1$, $PA_2$, … $PA_{64}$) [17]**

## 2.6 Switched-Capacitor PA

Recently, a new DPA has been proposed in [18]. The difference of this technique with the previous DPA methods is, it does the amplitude control through the charge transfer in a capacitor array. It is so called Switched Capacitor Power Amplifier (SCPA) and it consists of a capacitor bank in which one of their plates is shared at the output and the other plate is connected to the output of a switching PA which charges these caps to vdd/gnd or stays at ground depending on the digital code applied to the PA. This technique also takes advantage of the CMOS scaling. Fig. 5-6, shows the SCPA implementation.

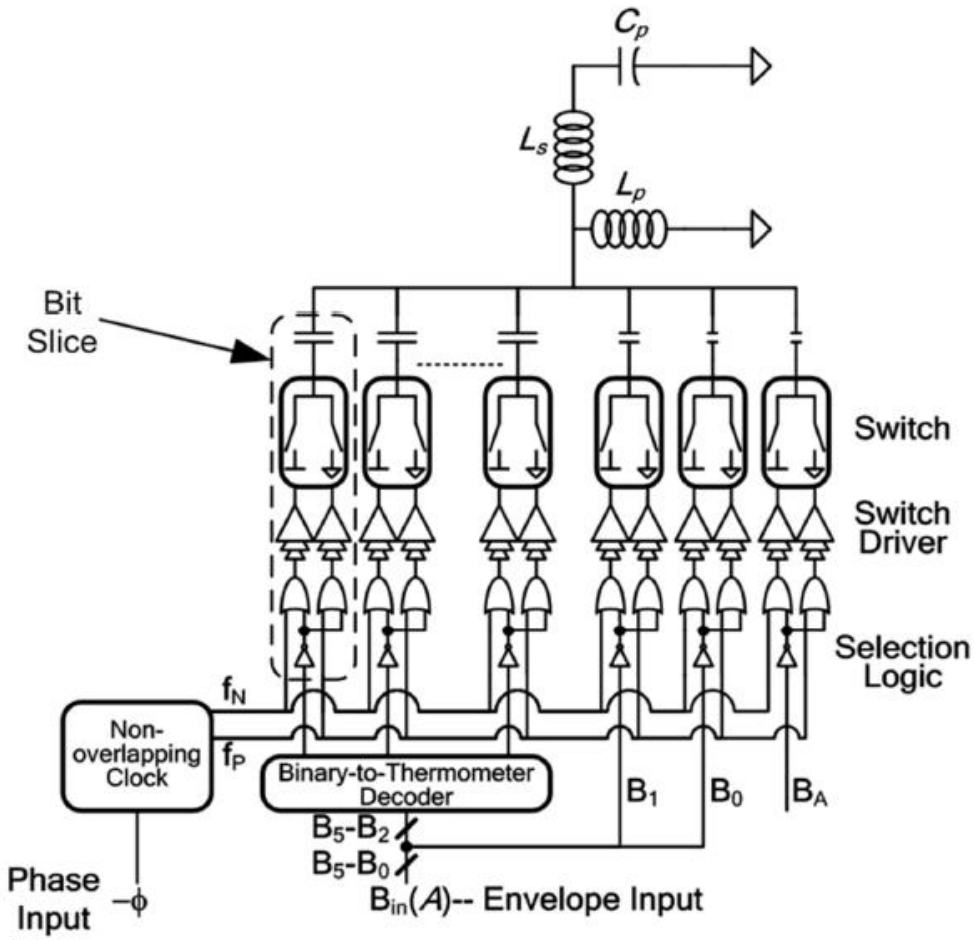



**Fig. 2-6: SCPA.**

This technique shows good efficiency and better AM-AM than previous DPA techniques. Further, discussion requires addressing the poor AM-PM and the WiFi mask violation in this technique. The efficiency characteristic of this technique is compared in later chapters.

# 3 CMOS Power Amplifier Transformer-Combiner

PAs have remained as the main integration bottleneck for wireless transceiver products today. This is mainly due to the challenges achieving high power level (around 1 watt or more) in CMOS PA and lossy passive components. However, the current solution of GaAs PAs as well as the requirement for off-chip components associated with the PA drives up system cost. Furthermore, the increased interest in small form factor devices with long battery life makes it imperative to come up with low cost, integrated, efficient single-chip CMOS transceivers. In CMOS process the low break down voltage of the devices and the fact that CMOS scaling further reduces the supply makes it quite challenging to achieve the desired power levels. To alleviate the low voltage break down of the CMOS process, a higher impedance ratio is required. This implies using more aggressive matching network to transfer the load impedance (typically 50ohm) to the optimum impedance that device can drive with an output voltage without being concerned about reliability issues. Also, the conductive substrate in CMOS process makes the passive elements quite lossy. This chapter looks into the recent techniques developed in order to achieve higher output power and more efficient on chip CMOS PA solution with on chip power combining.

## 3.1 DAT combiner

The distributed active-transformer (DAT) [1] provides a watt-level CMOS PA solution. It combines four differential push-pull amplifiers in series to provide a large output power at the 50ohm load. It offers both the advantage of the LC network and coupled inductor matching simultaneously. This becomes feasible by further using the ac virtual ground and magnetic coupling to avoid the use of off-chip components. The architecture results in a 1:n impedance transformation and n transistor power combining. The cross coupled drain caps tunes the inductor to the frequency of the operation as well as acts as the parallel cap for the load. This is necessary to compensate for the leakage inductance produced by the relatively low coupling coefficient of the transformer (k~0.6). Fig. 3-1, shows the primary side's circuit diagram of this architecture. Fig. 3-2, shows a circular geometry implementation of the DAT. The circular geometry with differential implementation create low loss virtual ac grounds to avoid using long metal leads which is a layout limitation in slab inductors as they compromise the PA performance due to high loss. Fig. 3-3, illustrates complete DAT system.

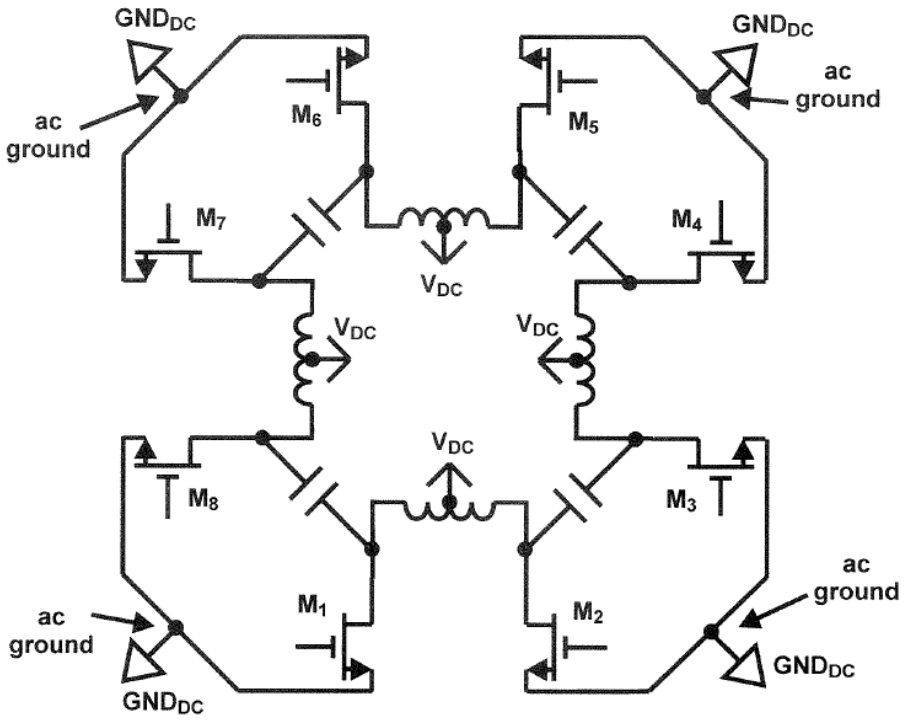



**Fig. 3-1: schematic of a primary side of DAT.**

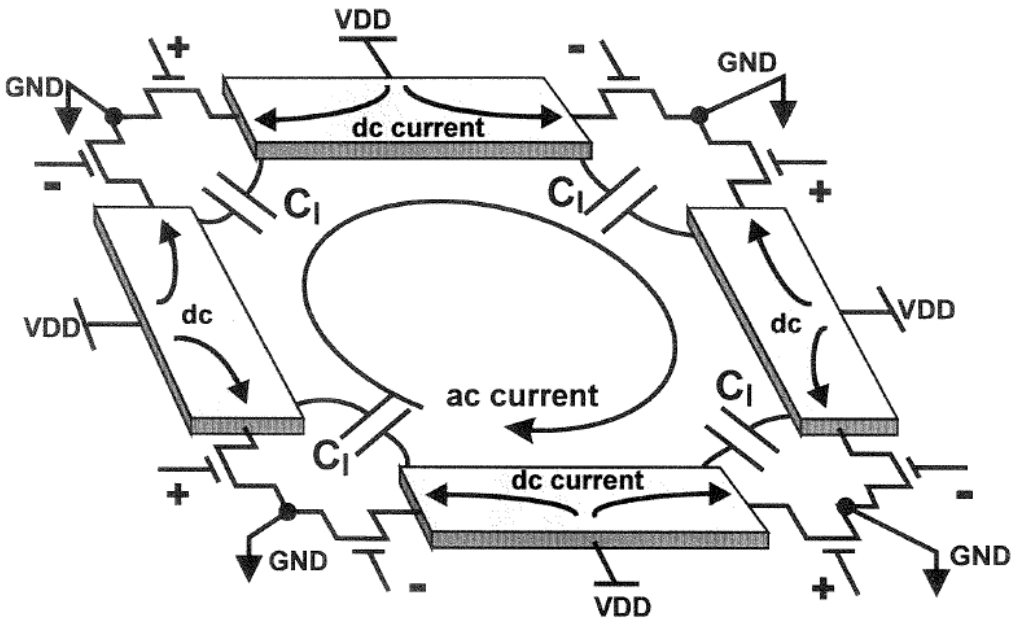



**Fig. 3-2: primary of a DAT with slab inductor.**

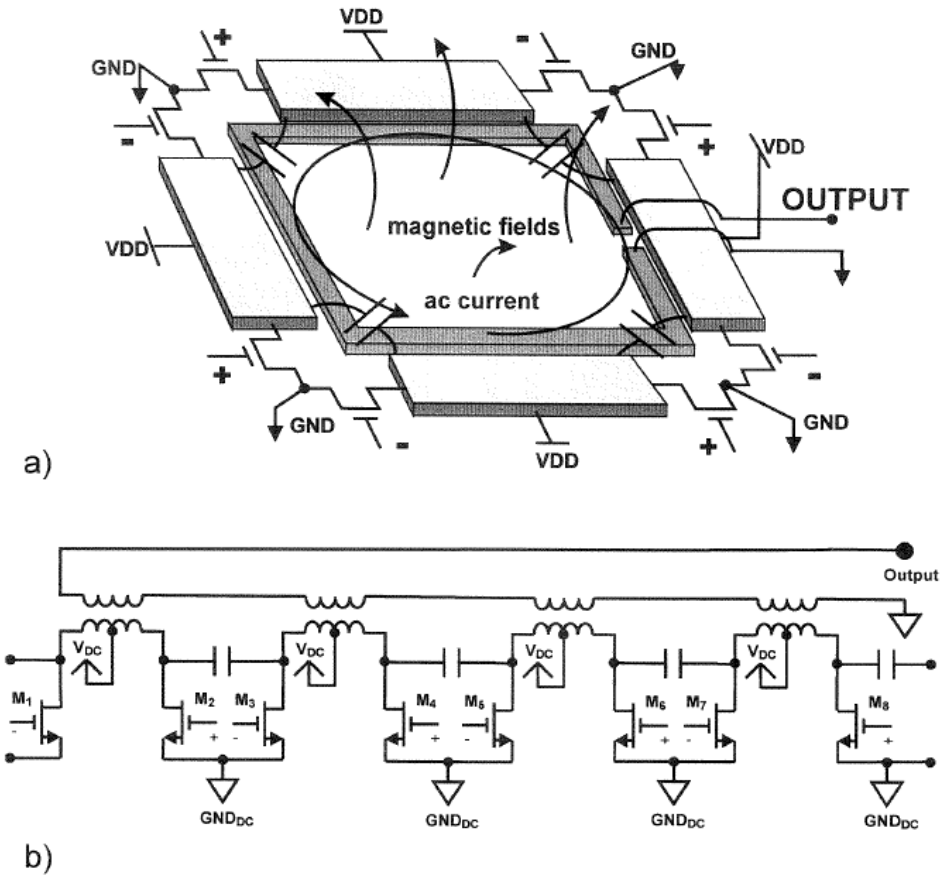



**Fig. 3-3: a) A combined four push-pull DAT. b) its corresponding schematic diagram.**

Even though the DAT achieves high output power with good efficiency but it suffers from the lower efficiency at back-off as well as it suffers from inherent coupling between input and output.

## 3.2 Figure-8 combiner

With wireless standards moving towards higher peak to Average Power Ratio (PAPR) modulations to accommodate more users with higher data rates (spectral efficiency), it is essential for PAs to maintain good efficiency over a wider range of power levels. With the DAT technique, the PA can achieve good efficiency at peak power but has yet to achieve

good efficiency at back-off comparable to off-chip bipolar PAs. In standards involving OFDM the PA may be operating 6-10dB backed off from the peak power on average. Figure-8 power combiner [2] proposes an efficient solution for the above problems. The main attraction of this technique is its proposed efficiency enhancement at back-off.

The transformer in this design works not only as impedance transformation but also as differential to single ended output so that the PA can be connected to the antenna directly. Further [2] proposes a new transformer shape which enhances the Q and magnetic coupling which both factors are essential for a low loss transformer design. The main attraction of this technique is, it takes advantage of the full parallel structures of the PAs. It provides the flexibility to enable and access control of each unit PA cell.

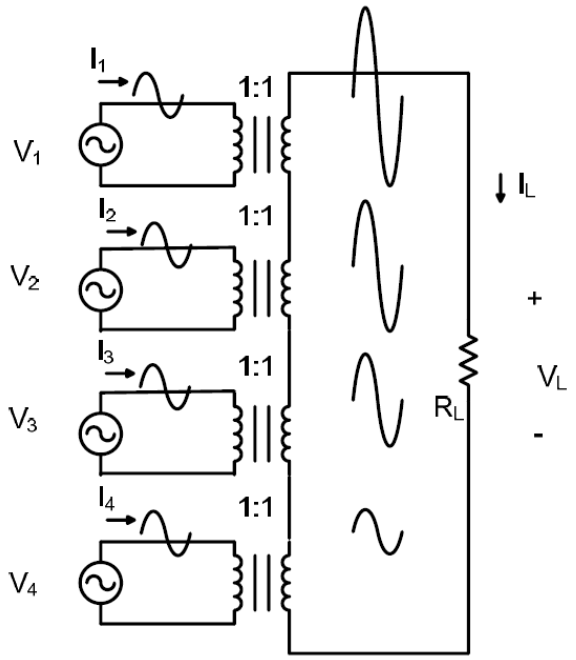



**Fig. 3-4: a 4 to 1 combiner [2].**

Figure 3-4, shows a four to 1 combiner. Assume, all $V_i$s' are equal and so the will add up in secondary side since on the secondary side they are all connected in series and so they

would lift the "ac ground" of the secondary side resulting in $NV_i$ at the load. Further the series connection on the secondary side forces all the currents to be equal to each other and to ther secondary side: $I_i = I_L$

So the impedance seen from the primary side of each transformer can be calculated as

$Z_i = \frac{V_i}{I_i} = \frac{V_L}{NI_L} = \frac{R_L}{N}$

Consequently the power delivers to the load is:

$$P_L = \frac{V_L^2}{2R_L} = \frac{(NV_i)^2}{2R_L} = \frac{N^2}{2}\frac{V_i^2}{R_L}$$

$$=> P_i = \frac{V_i^2}{2Z_i} = \frac{V_i^2}{\frac{2R_L}{N}} = N\frac{V_i^2}{2R_L}$$

$$=> P_L = \sum P_i$$

The above can be summarized as follow:

- The power on the secondary side is an N combined power of the primary side through magnetic coupling.
- Due to electric isolation characteristic of the transformer, the total added ac voltage swings on the secondary will not affect the primary low swing, below the transistor voltage break down. The ratio of the swing is N.
- The current on both sides of the transformer are equal but the total current on the primary to the secondary is 1/N ratio.
- The impedance seen the each primary side is N times smaller than the load, leading to an impedance transformation of 1/N.

- This combiner uses the dynamic load modulation to benefit in efficiency at back-off. Therefore, the at each section of the power back-off the efficiency moves up to peak efficiency as shown in fig. 3-5.

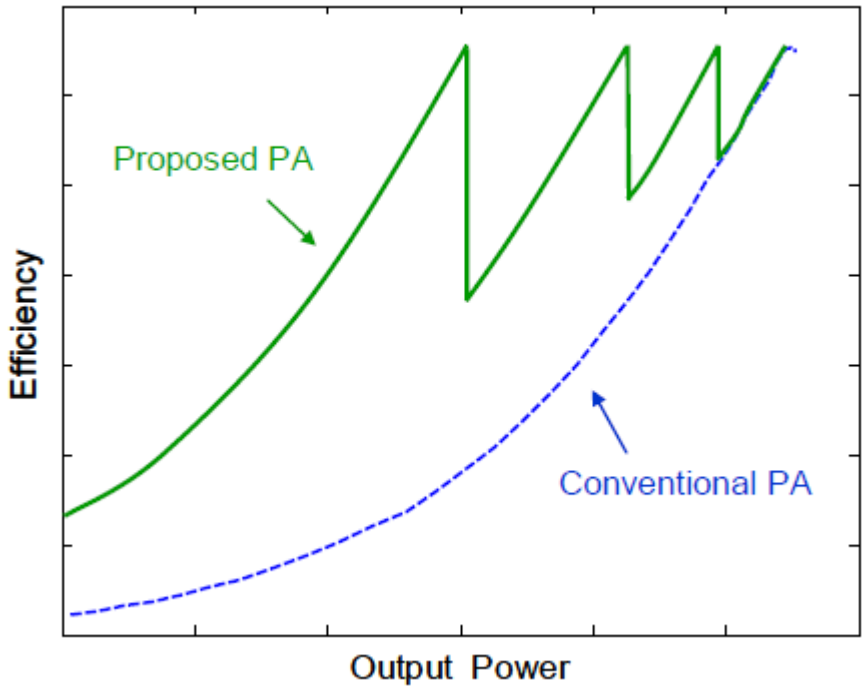



**Fig. 3-5: Efficiency comparison of [2] PA with the conventional PA.**

Therefore, the proposed architecture in this section [2] shows ideally this transformer combining should have an efficiency curve as it is shown in Fig. 3-5.

A new figure-8 layout of the transformer is proposed in [19] which address some of the issue of on chip transformer combiner. It reduces the insertion loss of the transformers from 2-3dB down to 1.4dB a when simulated in 90nm CMOS process at 5GHz. This transformer is shown in fig. 3-6. The two important features of this transformer are: (1) the sandwich of two

primaries to increase the coupling factor and (2) alternating the direction on the secondary which makes it immune to the distance source because the magnetic flux induces currents in opposite direction across each "figure 8" section. Therefore, an even number of sections is preferred in this proposed design.

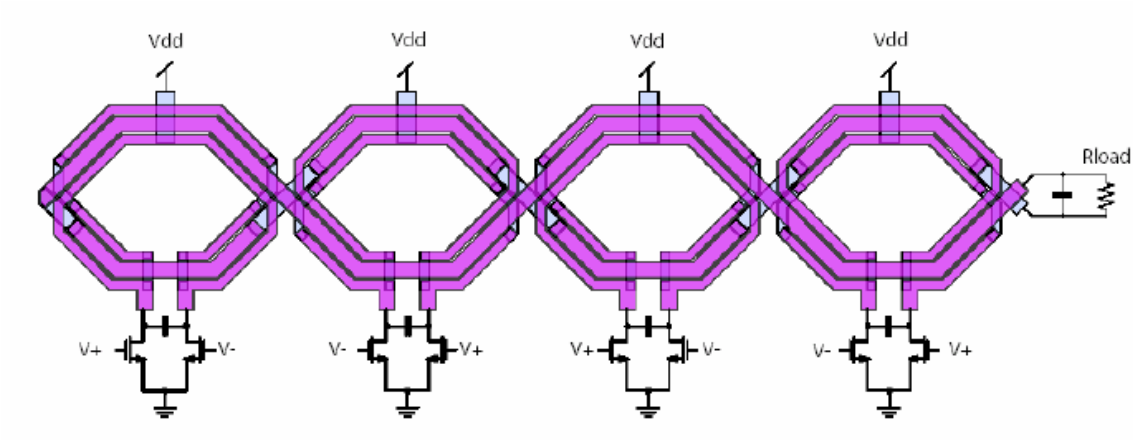



**Fig. 3-6: A power amplifier with "figure 8" transformer power combiner [19].**

## 3.3 Dynamic-Reconfigurable Combiner

Section 3.1 and 3.2 presented two efficient combiners. [2] tries to achieve an efficiency boost at back-off by static deactivation of the off PAs (turning off the transformer sections). Both above were implemented with linear PAs. In this section a Dynamic Power Control PA (DPC-PA) proposed which uses a class-D PA in outphasing modulation scheme and it shows improvement under OFDM modulated tests. Fig. 3-7, shows an implementation of this architecture. Fig. 3-8, shows dynamic power control concept. The PAs turn on or off based on the OFDM signal and therefore improve the average OFDM power added efficiency. Fig. 3-9, shows the operation of the proposed PA at various power levels.

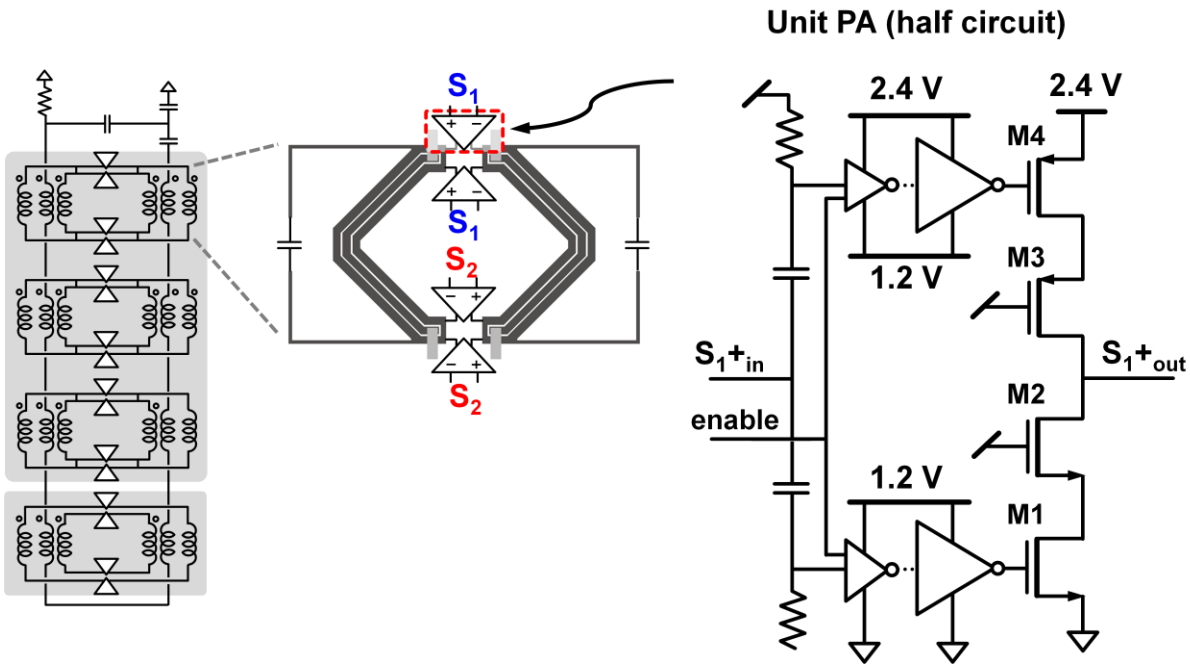



**Fig. 3-7: DPC-PA circuit and transformer layout implementation of a unit section.**

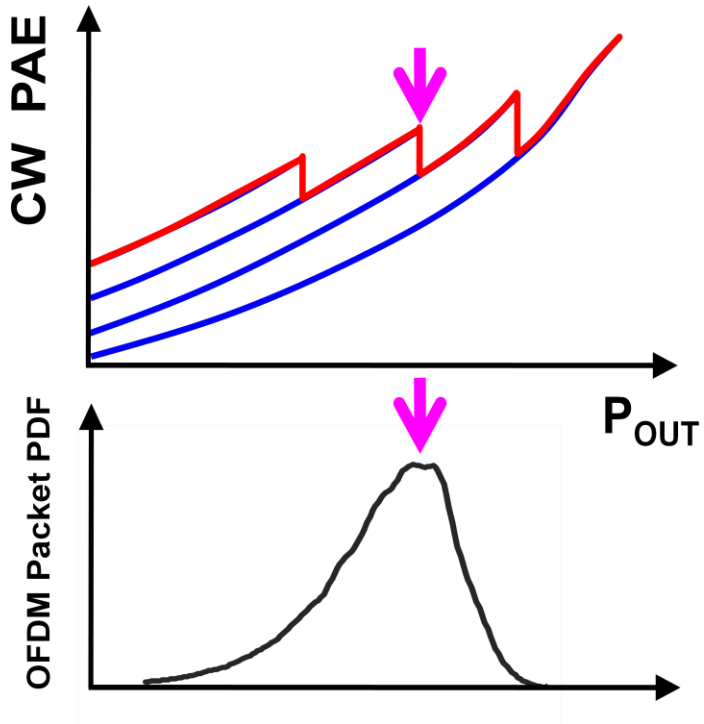


**Fig. 3-8: Dynamic power control concept.**

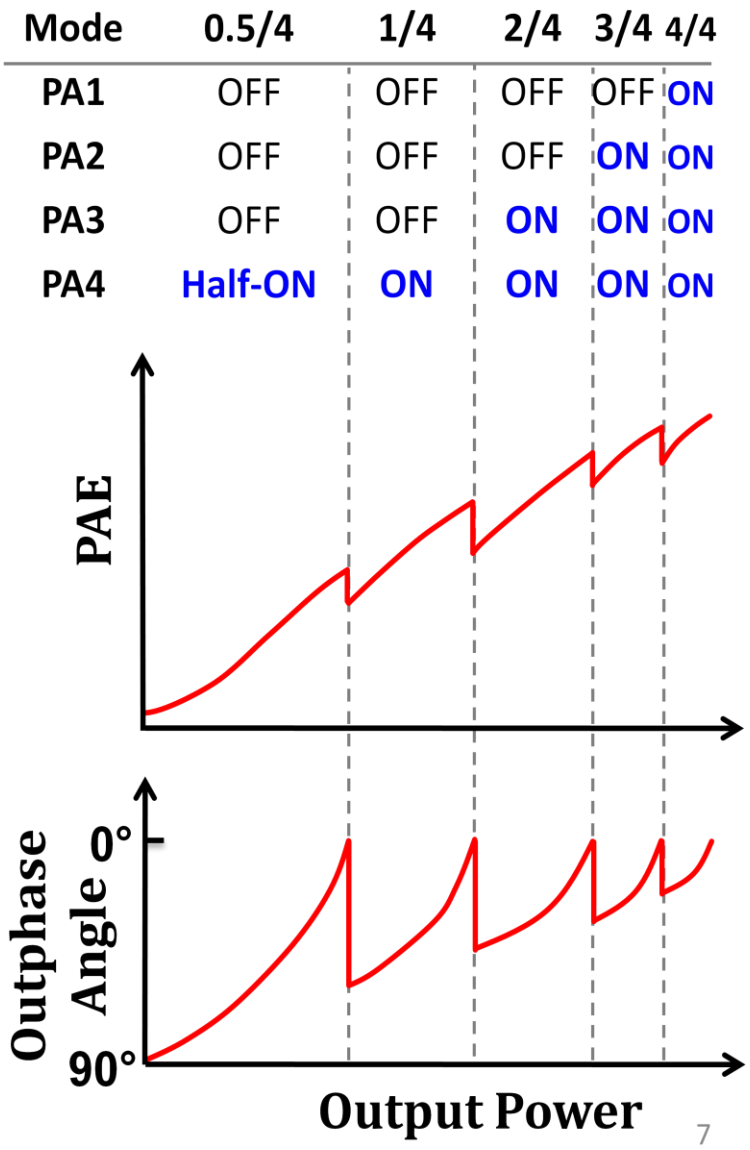



**Fig. 3-9: Operation of DPC-PA at various power levels.**

# 4 Harmonic Rejection Power Amplifier Technique (HRPA)

In this section, the idea of harmonic rejection is explored to investigate if it is possible to take advantage of this technique to compensate for the impact of the nonlinearities of the PA. It will focus on the PA since it is typically the most power hungry block in the transceiver and breaking the trade-off between efficiency and linearity is a crucial breakthrough required for integrating it into multi-standard transceivers. Modern high data rate communication standards, such as WiFi, WiMax, 3G and LTE, typically encode the information to be transmitted in complex modulations with both amplitude and phase information for spectral efficiency reasons. These signals are therefore characterized by large peak-average power ratios, i.e. the instantaneous power of the signal can be significantly higher than the average transmit power. When these modulated signals are passed through a power amplifier, the nonlinearity (distortion) of the PA degrades the Error Vector Magnitude (EVM) and results in spectral emissions in adjacent channels and out-of-band. It is also a source of the harmonics of the RF signal present in the output of the transmitter. So for this reason, typically in linear PA architectures, it is preferred to operate the PAs in their linear region which usually is backed off from the saturation point by several dB (6 – 10dB back-off is commonly used). Effectively, backing off the average power from the saturated power of the PA ensures that the instantaneous power peaks of the modulation are not clipped. Linear PAs are sized and biased for the peak power. So while the output power can be varied over a wide dynamic range the current drawn from the supply remains constant. Therefore, operating the PA at large back-offs results in a poor average efficiency and translates to

reduced battery life. Therefore, some architectural or circuit techniques are desirable to make PAs to operate at smaller back-off.

## 4.1 Proposed HRPA

The Harmonic Rejection Mixer (HRM) was introduced in [4] as a technique to reduce the LO harmonics from a switching mixer (fig. 4-1). While this is a very interesting idea to remove the RF filter after the mixer, the RF filter after the PA is still required to remove the effects of the PAs nonlinearity, i.e. harmonics. A related approach in [21] extended the concept of harmonic rejection to also reduce the BB harmonics at the output of mixer but it still did not address the issue of the power amplifier non-linearity.

To study the feasibility of harmonic rejection in the PA, consider the system in Fig. 4-2. If the harmonic rejection technique can be used to cancel out the PA nonlinearity, it can operate the PA closer to saturation and therefore at a higher efficiency without incurring a penalty in the spectral emissions. Since source of EVM degradation is due to in band nonlinearities than harmonics, the following show the effect of harmonic rejection in the intermodulation products. For this purpose a two subcarriers of the OFDM (orthogonal frequency modulation) are put through a simplified model of the PA nonlinearities.

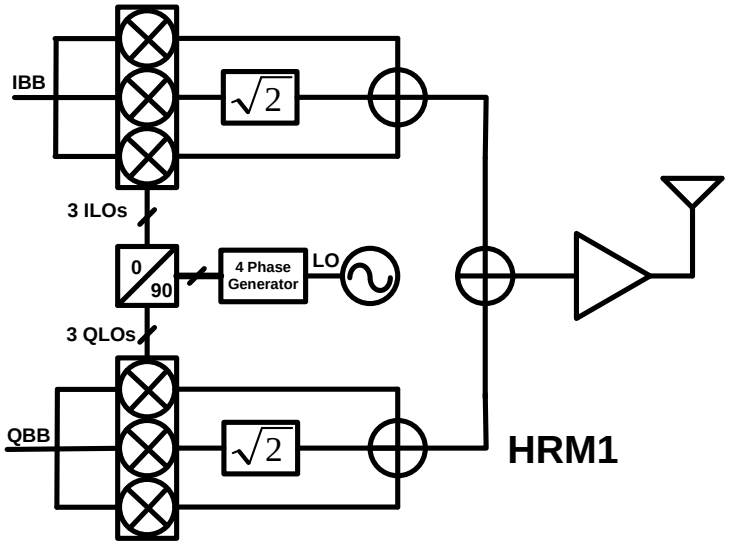



**Fig. 4-1: HRM Tx.**

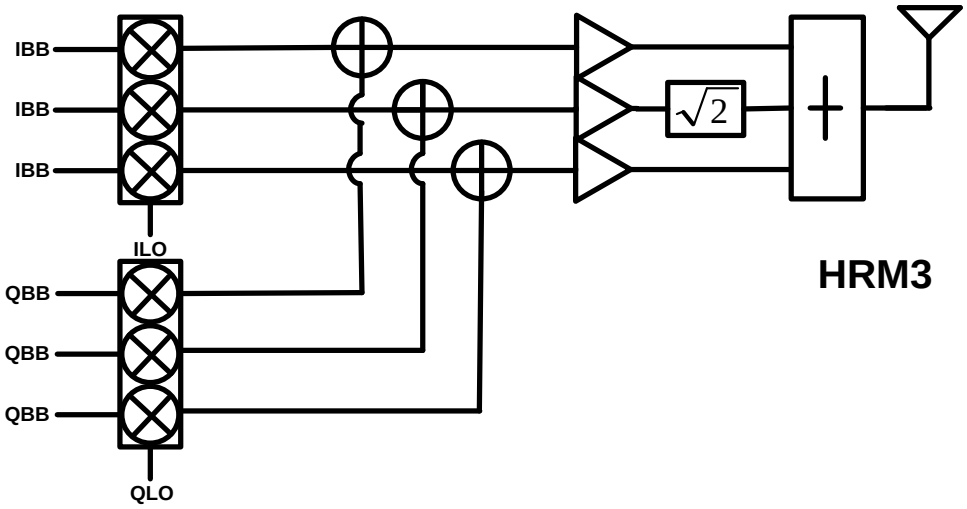



**Fig. 4-2: HRPA Tx.**

Assume the architecture in Fig. 4-2 with the following input signals:

$$IBB = Cos(\Delta\omega_1 t) + Cos(\Delta\omega_2 t)$$

$$QBB = Sin(\Delta\omega_1 t) + Sin(\Delta\omega_2 t)$$

$$ILO = Cos(\omega_{LO}t + \theta)$$

$$QLO = Sin(\omega_{LO}t + \theta)$$

The spectrum is shown in fig. 4-3.

If one of the path input of the PA is called XRF and simplify the math then:

$$XRF = IBB \times ILO - QBB \times QLO$$

$$XRF = Cos[(\omega_{LO} + \Delta\omega_1)t + \theta] + Cos[(\omega_{LO} + \Delta\omega_2)t + \theta]$$

If we call $\omega_1 = \omega_{LO} + \Delta\omega_1$ and $\omega_2 = \omega_{LO} + \Delta\omega_2$ and rewriting the above equation:

$$XRF = Cos(\omega_1 t + \theta) + Cos(\omega_2 t + \theta)$$

If assuming a 3rd order distortion differential PA (no even harmonics) with a simplified math model as follow:

$$y = \alpha_1 x + \alpha_3 x^3$$

Now, applying $XRF$ into this model and simplifying the math, then the output of the PA is as follow and the spectrum and phasor diganram are shown in fig. 4-4:

$$y = \left[\alpha_1 + \frac{9}{4}\alpha_3\right] Cos(\omega_1 t + \theta) + \left[\alpha_1 + \frac{9}{4}\alpha_3\right] Cos(\omega_2 t + \theta) + \frac{1}{4}\alpha_3 Cos(3\omega_1 t + 3\theta) +$$

$$\frac{1}{4}\alpha_3 Cos(3\omega_2 t + 3\theta) +$$

$$\frac{3}{4}\alpha_3 Cos[(2\omega_1 - \omega_2)t + \theta] - \frac{3}{4}\alpha_3 Cos[(2\omega_1 + \omega_2)t + 3\theta] + \frac{3}{4}\alpha_3 Cos[(2\omega_2 - \omega_1)t + \theta]$$

$$- \frac{3}{4}\alpha_3 Cos[(2\omega_2 + \omega_1)t + 3\theta]$$

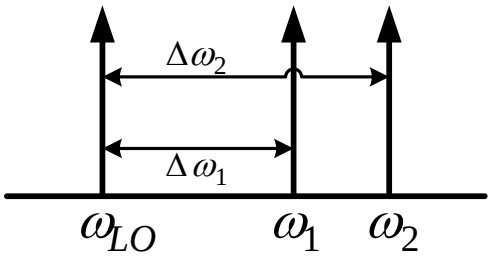



**Fig. 4-3: two tone spectrum.**

If the coefficient renamed for more readability as follow:

$$\alpha_1 + \frac{9}{4}\alpha_3 = \beta$$

$$\frac{1}{4}\alpha_3 = \gamma$$

$$\frac{3}{4}\alpha_3 = 3\gamma$$

And applying the three path with the angle of 45, 0, -45 degrees then the output of the HRPA is shown in fig. 4-5 and phasor diagram in fig. 4-6.

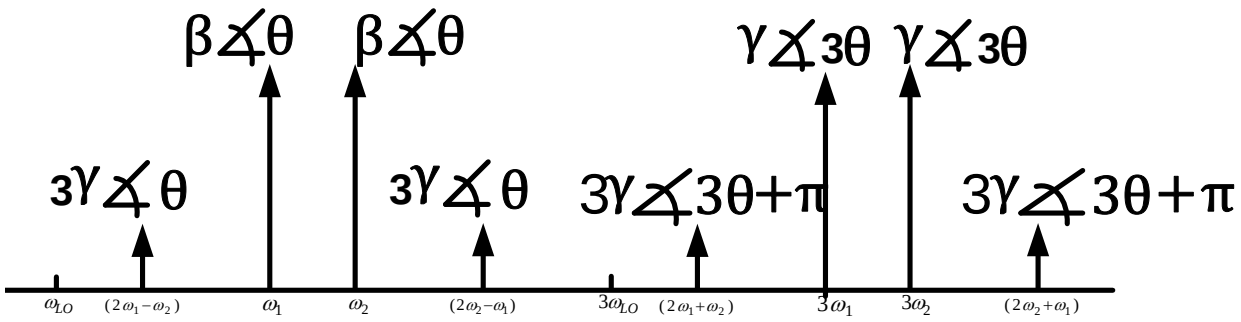



**Fig. 4-4: output spectrum of just one of the path of the HRPA.**

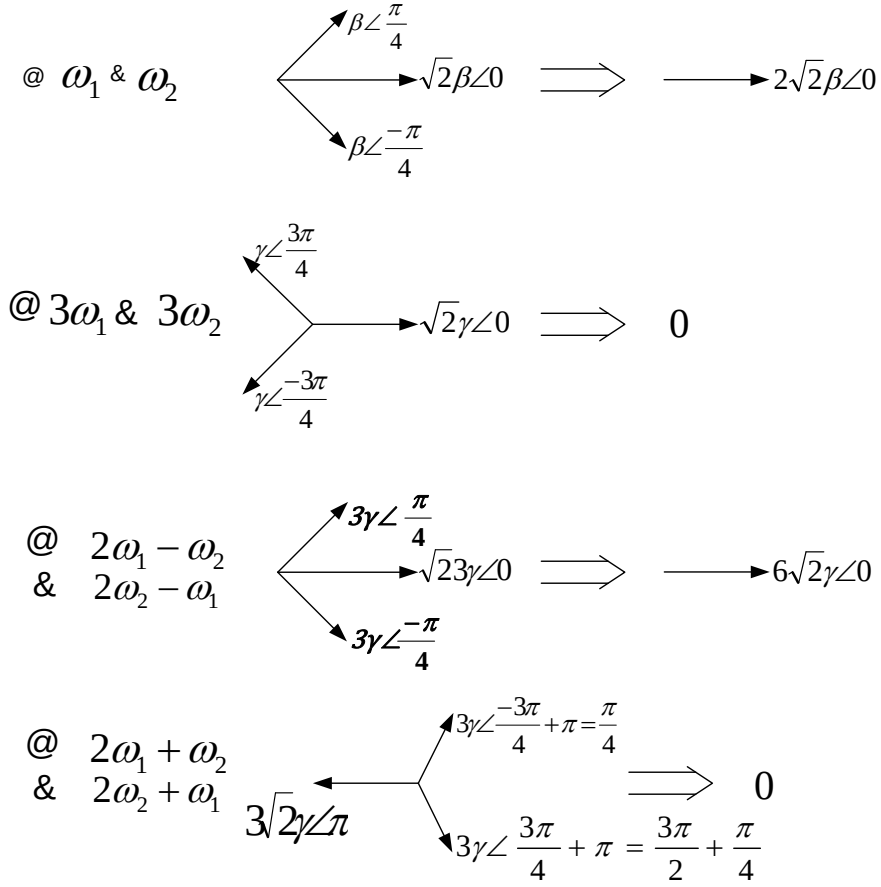



**Fig. 4-5: the Phasor diagram of the output of HRPA**

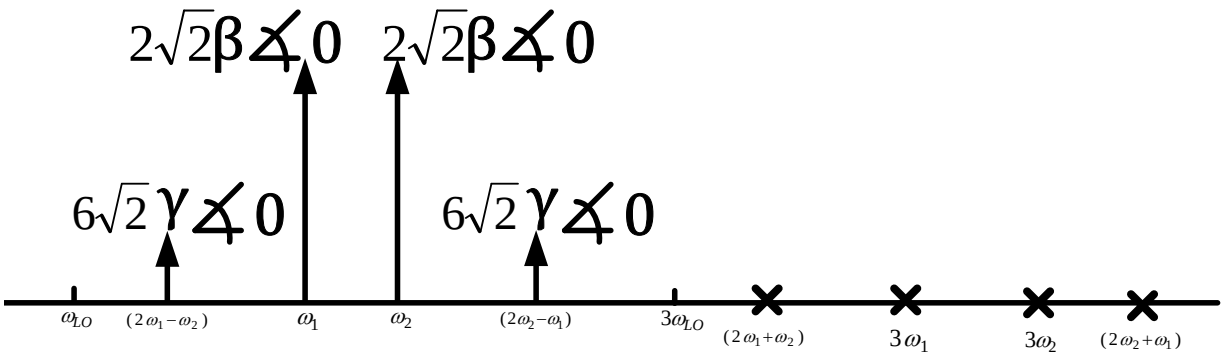



**Fig. 4-6: output spectrum of HRPA after the three path angles are as follow respectively [45 0 -45] degrees.**

So as it can be seen from above the intermod around fundamental frequency has the same angle as the fundamental frequency and so if we are trying to cancel these intermods the fundamental gets cancelled as well and so this is not possible.

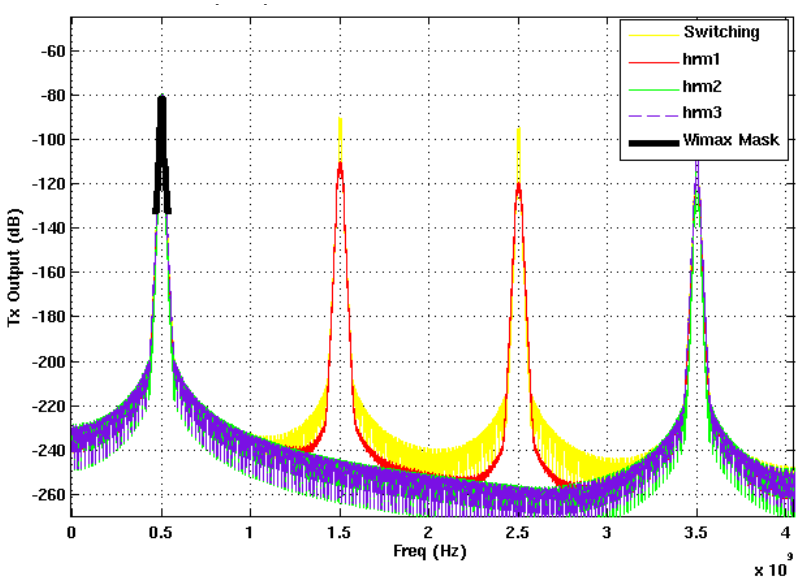
It is shown both mathematically and through MATLAB™ simulations, that this technique can be used for harmonic suppression (figs. 4-7 and 4-8(a)) but not improving the linearity of the power amplifier (fig. 4-8(b)). This is because the distortion is due to intermodulation of the two subcarriers (for example in OFDM modulation) and they are in phase with the carrier signal and no suppression is achieved by this. In order to achieve low backoff it is required to suppress these intermod components. Since the harmonic rejection technique does not cancel out the intermod components, by itself, it cannot be used to compensate for the spectral emissions from reducing the back-off in the PA. Therefore, even with the use of harmonic reject approaches in the PA, we are forced to operate at a low efficiency.

In the specific case of a two tone modulation, it can be shown mathematically (not included in this document), that by specifically constructing the signal and applying the phase shift to the baseband signal than LO, the intermods around the fundamental tones can be cancelled out without affecting the desired modulation signal. The baseband phase shifting approach requires a total of 6 DACs for the three paths (one pair of I/Q DACs per phase shifted path). With this baseband phase shifting technique however, intermods around the $3^{rd}$ harmonics are still not cancelled. However, since the intermods around the $3^{rd}$ harmonics are much lower than the $3^{rd}$ harmonics and it still relaxes the filtering requirements. However, this does not for a modulation scheme with more than two sub-carriers such as the many subcarriers of OFDM. This is because the intermods of different carriers could sit on top of each other and the cancellation may not be possible.

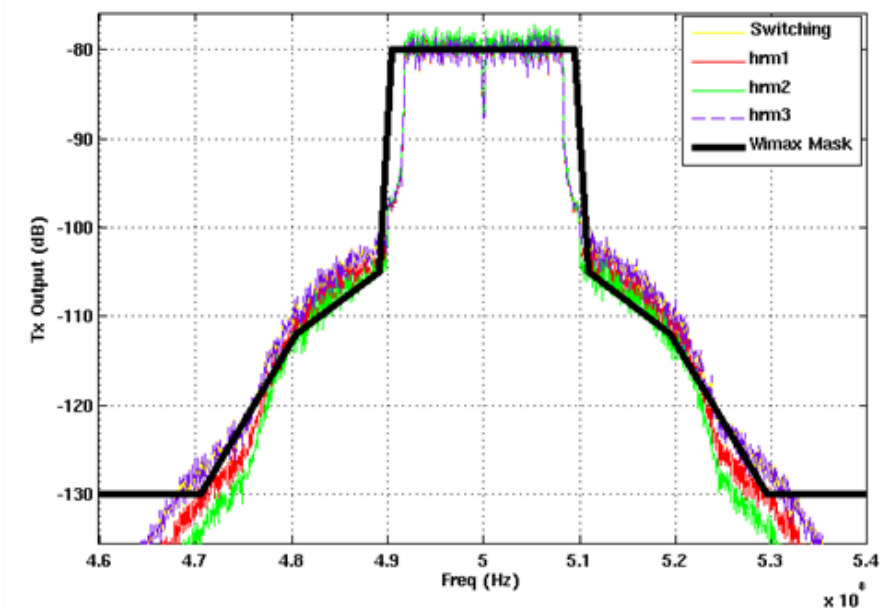
So to summarize this section, it is shown that HRPA cannot improve the PA linearity but it can improve the $3^{rd}$ and $5^{th}$ harmonic suppressions if assuming a three path system. Since there is no linearity improvement, there cannot be any reduction in the back-off and hence efficiency. This is still very useful as it ideally removes the filter after the PA which typically has 2-3db of loss. This means the PA can be design for the saturation power of 2-3dB less and so less current from the supply and consequently higher efficiency. Eliminating or simplifying the filter after the PA also reduces the system cost.

In chapter 2, polar/EER and outphasing are covered briefly. These approaches both rely on PAs that operate in saturation in order to obtain higher efficiencies. The linearity is achieved through the combination of two different signal paths: amplitude and phase in polar and two different phase modulation paths in outphasing. The linearity of the reconstruction is critically dependent on matching the different paths. Imperfect reconstruction in the

combination of the two paths results in undesired spectral emissions. The sampling and quantization, inherent to the polar and outphasing approaches, results in additional out-of-band components in the spectrum. Finally, the switching nature of the PAs in these approaches result in substantial harmonic energy at the outputs of these PAs. In the next section, techniques for low out of band emissions addressed and the specific out-of-band components of these approaches including sampling images, quantization noise and harmonics.




**(a)**




**(b)**

**Fig. 4-7: (a) Yellow curve is the original transmitter with no HRM technique. Red is the [4] with no filtering. Purple and green are both HRPA. (b) zoomed spectrum of the mask.**

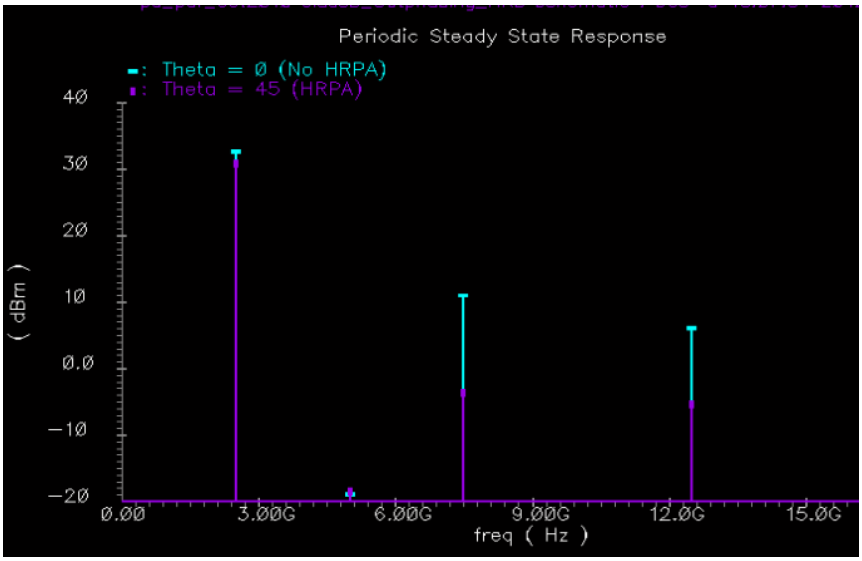


**Fig. 4-8: shows the schematic simulation of HRPA when the three path angles are zero (no HR) and when they are 45deg apart (HR) it shows about 15 to 18 dB reduction in the 3rd Harmonics and 10 dB reduction in the 5th harmonic.**

## 4.2 Low out of band image Emission

Digitally-modulated PAs have recently been proposed to improve these tradeoffs by using a discrete number of sub-PAs that are switched into and out of the circuit in order to provide amplitude modulation [16] [22]. Since amplitude modulation is achieved through this "digital" scheme, at least in principle, each sub-PA can be implemented using an efficient but otherwise non-linear design. Section 2.5 and 2.6 of this document briefly reviewed two examples of this architecture.

Sampling and the finite quantization levels of the PA produce images and quantization noise which corrupt the output spectrum. The resolution required of the digital PA is determined by the EVM and spectral mask requirements. In addition, switching PAs have harmonics by nature due to the square wave output at the drain of the PA. The harmonics of the Switching PA s would further spoil the spectrum and need to be filtered out as well. Therefore, a combination of both circuit and DSP techniques is required for lowering these harmonics and images in each individual Tx making the co-exiting of the radios feasible.

One immediate solution that comes into mind is to use sharp filters in order to suppress the harmonics and images of the PA. Since, some of these images are close to the carrier frequency, using conventional filters to remove them is not feasible. Also, for incorporating more standards into a single die solution, the number of these filters grow and create more expensive, less efficient (due to insertion loss of the filters) design. Therefore,

recently, new circuit and DSP techniques require for lowering these harmonics and images in each individual Tx making the co-exiting of the radios feasible.

An alternate solution in [23], for a polar architecture, uses oversampling on the amplitude path to suppress the images of the power amplifier. A finite-impulse response (FIR) interpolating filter is implemented on chip to attenuate the spectral images not only below the FCC mask limits, but also to lowers the noise floor in order to enable coexistence. Since the filter is on, even when the output amplitude is small, it must be implemented with very low power consumption. A bigger issue with this approach is that the FIR filter increases the number of bits in the amplitude path thereby requiring the PA to support finer quantization levels. This can quickly become impractical due to the overhead of more complex layout and routing, additional parasitic caps, higher supply and ground inductances, and the limitations of matching. A limited resolution results in the re-growth of the spectral images and noise and so in this proposal, a combination of circuit [17] and DSP techniques are explored to suppress the out of band emission of the high efficiency switching PAs.

As an implementation example, [18] presents a 6-bit digital PA which achieves a good efficiency at back-off by switching on and off the sub PA s. However, as it is shown in fig. 4-10, a simplified matlab model (without showing the PA distortions) that both PAs in [16] and [18] have spectral images that violates the FCC requirement as well as prohibits the radios co-existence if no filtering were applied to them. By applying a simple FIR filter to approximate a first-order hold (FOH) (fig. 4-9 is an example of FOH) for this architecture. In this specific case, the spectral images were reduced below FCC and co-existence levels (fig. 4-11) but the number of required bits in the amplitude path of the PA increased to 8. This would translate to 256 sub-PAs which is clearly impractical for the above-mentioned cost

and implementation reasons. The proposed techniques suppress the spectral images well below the spectral mask by increasing the resolution of the PA without increasing the number of sub-PAs as it is shown in fig. 4-12.

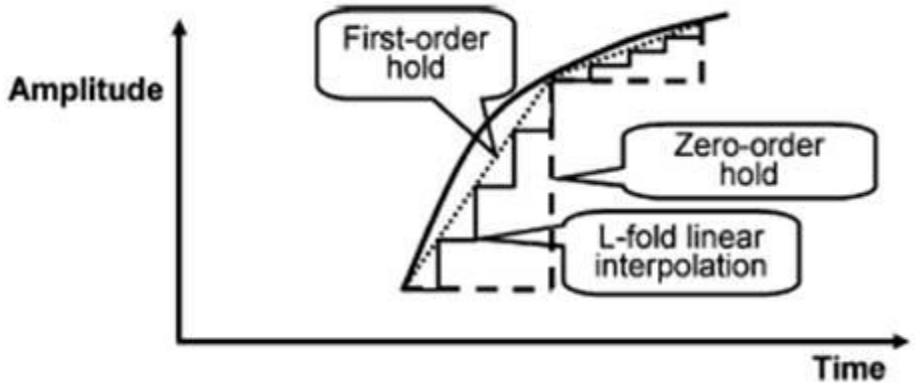



**Fig. 4-9: from [16] FOH implementation by 4-fold interpolation**

However, these techniques still do not address harmonic suppressions which should be at very low energy levels in multi-standard radios. Based on the harmonic rejection mixers presented in [4] proposed, these techniques might be used to help with harmonic suppression of the switching PA. It should be noted that the harmonic currents need to see proper terminations in a switching PA to prevent the efficiency from degrading. These techniques help to achieve the harmonic suppression at the output without disrupting the switching operation of the PA. It combines with image suppression to get a clean out-of-band spectrum.

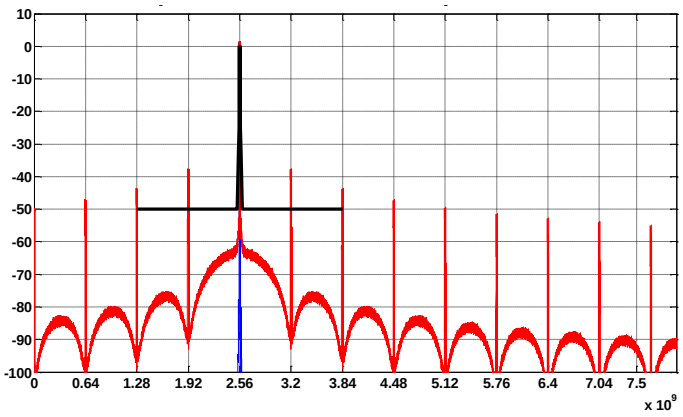



**Fig. 4-10. Spectral Mask of a 6-bit amplitude path**

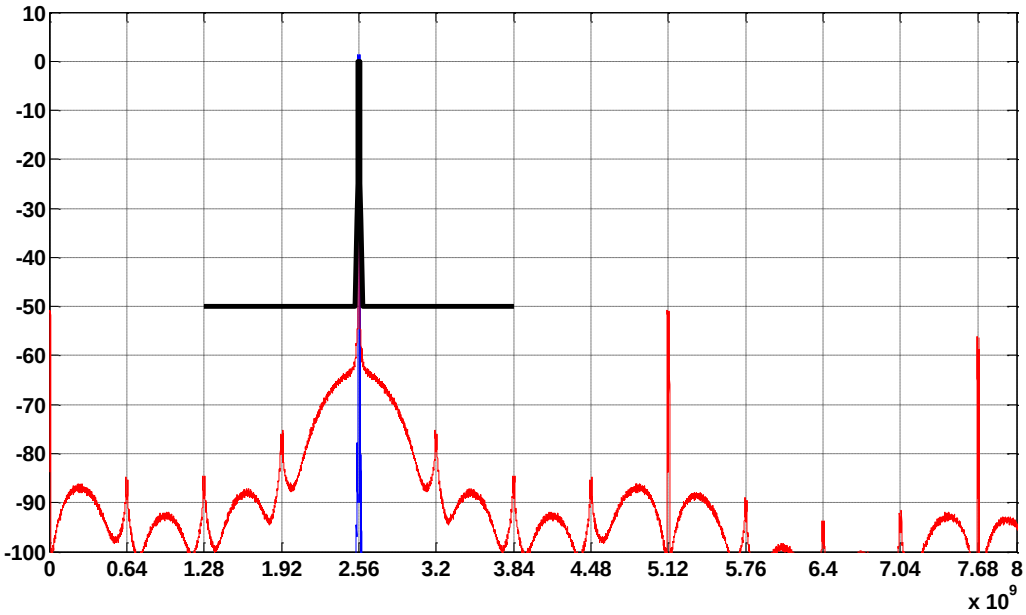



**Fig. 4-11: Spectral Mask of an 8-bit amplitude path**

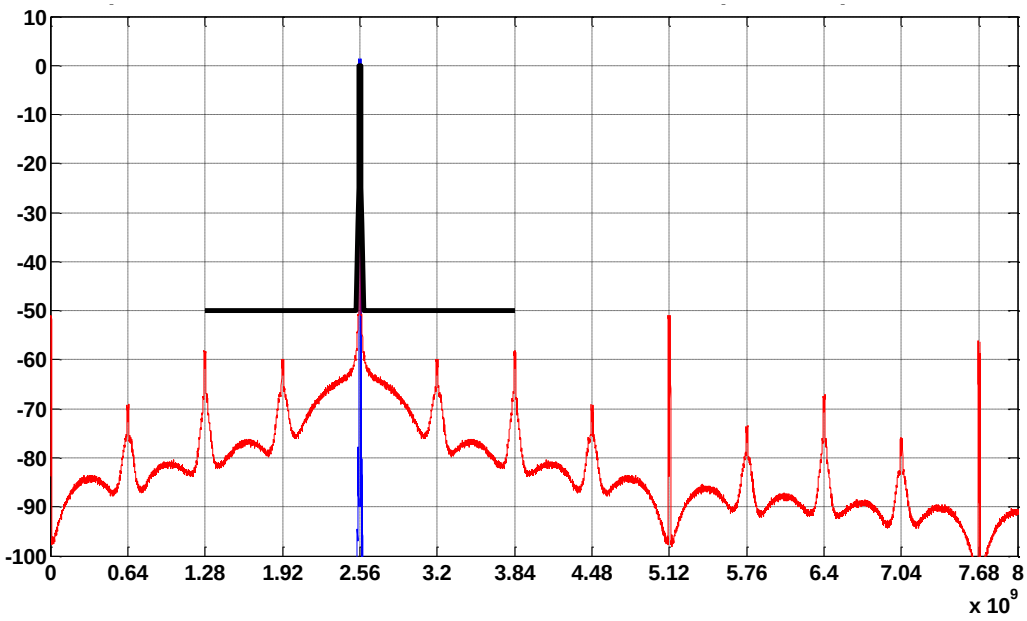



**Fig. 4-12. 6-bit Spectral Mask with the proposed techniques.**

This chapter presented with harmonic rejection technique and an analog and DSP techniques it is possible to reduce the images of the RF transmitters to well below the mask and reduce the 3$^{rd}$ and 5$^{th}$ harmonic of the PAs so that relax or remove the RF filtering requirements results in more efficient transmitter design.

# 5 Digitally-Scalable Transformer-Combining

Due to increase of hand held devices and more than ever concerns over global warming, the attention towards more energy efficient solutions and longer battery life can be seen in all aspects of today's life. The switching PAs are more efficient PAs than the linear PAs. However, linear PAs are well known for achieving higher output power. In order to achieve a fully integrated solution into the product, it is important to have a CMOS PAs that achieves similar or higher efficiency and output power than GaAs linear PAs which are currently the dominant wireless devices' power amplification.

The standards with high peak-to-average power ratio, such as WiFi, WiMAX, and LTE, require high output power while maintaining high efficiency at back-off. CMOS (complementary metal-oxide semiconductor) processes are well known for their large-scale integration and low cost. They are well suited for digital design, but do not yet achieve a high power and efficient implementation of a radio frequency (RF) power amplifier, due to low device breakdown voltage and passive components in the CMOS process.

Recently, transformer combining has been proposed for producing a higher output power amplifier (chapter 3). While improvements at peak power have been realized with power amplifiers that use transformer combining, efficient power output at back-off power levels remains elusive.

CMOS (digital) process for its high integration, scaling and low cost is known to be a good candidate for fully integrated high frequency radio transceivers. However, due to poor performance of RF circuits in digital processes, a combination of both circuit and digital

signal processing (DSP) techniques are crucial to compensate for this flaw and transfer the design into a full digital realization on chip, e.g. all digital transmitter (Tx) [24] [25]. This particularly true in the case of power amplifiers, which are a key component of the transceiver, that have yet to be integrated in high volumes. Traditional linear PA designs generally suffer from poor trade-offs between peak efficiency, linearity, and output power, and hence a great deal of research has focused on breaking this trade-off.

The standards for mobile communication require High Peak to Average Power Ratio (PAPR) modulations. This challenges the PA design to have high efficiency at average power as well as high amplitude and phase linearity. The other main challenges of CMOS PAs are to have high output power in the era of reverse scaling in power supply as well as passive losses in conductive substrate.

An optimum solution points toward more digital friendlier PA design. In recent years some architectural as well as design improvement of power amplifier design has been develop [15] [16] [18] [22]. In [15] the PA design achieves linearity without pre-distortion while maintaining good efficiency. In [18] has a digital friendly design with good efficiency while yet to maintain the well spectrum and high output power. [26] tried to achieve the high output power by transformer combining while efficiency degraded.

In digital design, the active power consumption is proportion to $CV^2f$ while this is not the case for a power amplifier design as PA output power is dictated by the wireless standard. Furthermore, the CMOS scaling results in smaller transistors with lower voltage breakdown to increase the reliability of the design. Even though the scaling helps with linearity of the PAs by having more efficient digital baseband circuitry by pre-distortion but

PAs generally suffers from performance degradation with process scaling. Therefore, a PA design with capability to generate required output power with reduced voltage supply is becoming an important form factor into having an integrated low cost and process scalable design. Transformer combining is used to mitigate the low output power problem of CMOS PAs while maintaining ok efficiency [1] [2]. The latter problem rises from the low transistor breakdown voltage as well as lossy on-chip impedance transformation to achieve watt level output power. While these would achieve a high output power with better efficiency than others PAs had before at that time but to satisfy today's WiFi, 4G, LTE standards with high peak to average ratios, PAs should maintain good efficiency at their average power output level. This is though as usually PAs are known to have better efficiency at peak power. This is because all efficiency metrics are defined as output power over dc power and/or driver power. So by having the output decrease to its average output level while the denominator stays constant hurts overall efficiency of the PAs even more. [2] proposed a new way of transformer combining to not only achieves close to the watt level output power but also mains good efficiency at power back-off. This is done through turning off the PAs that are not contributing to the output power at back-off. As a result in efficiency metric not only the numerator decreases but also the driver and dc power decrease which are the denominators of the metric. [26] used the latter combiner to improve the SCPA low output power, however its back-off efficiency decreases. [20] Further used the [2] combiner but configured it dynamically.

This research proposed a novel power combining technique which not only well suited for digital process as it benefits from CMOS scaling but also improves the PAE at back off powers.

## 5.1 Theory of Operation

Transformers combining are commonly used to enable CMOS PAs to efficiently operate at higher power. Previous methods suggest turning off sections of transformers to maintain good efficiency at lower power level. Assume a general 4 to 1 transformer combiner as it is shown in Fig. 5-1. To lower the even harmonics, we drive them differentially. At back off, in previous methods, they would turn off one of the transformer branches by grounding or tri-stating the PAs connected to them depending on the PA architecture Fig. 5-2. In these cases, the primaries which were connected to off PAs were still dissipating power. This is due to the induced field from the current flow in the secondary not only drives the load it also induces a magnetic field that results in current flow back to the primary winding. This back flow of current into the primary winding causes dissipation of power in primary inductors. This is known to give sub-optimum efficiency at back-off. Thus, the nature of this electromagnetic behavior in the transformer demands that each section of the transformer contribute evenly. In other words, for efficient combining, the transformer does not leave any primary inductors of the transformer off-load. It can also be stated as, an open circuit in the primary results in self-inductance seen in the secondary, which disturbs the matching network, reducing the efficiency of the active power amplifiers.

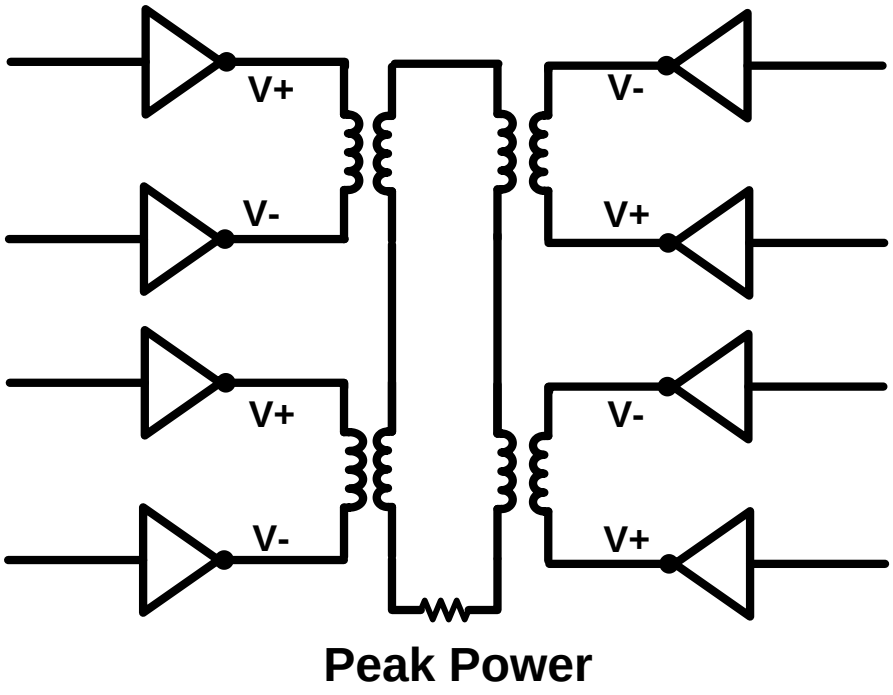



**Fig. 5-1: Peak power configuration in conventional transformer combining.**

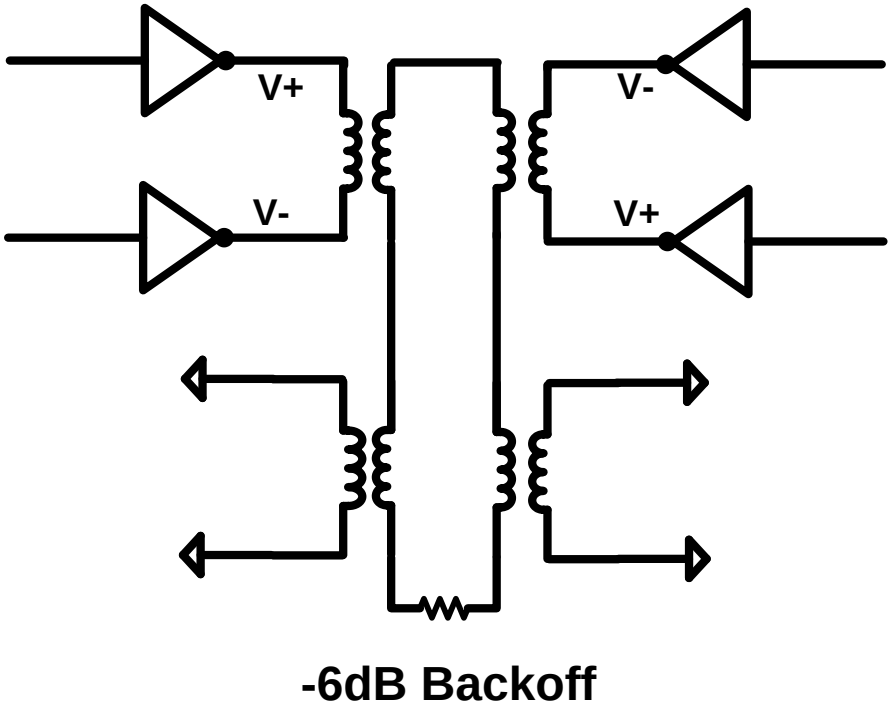



**Fig. 5-2: -6dB back off in conventional transformer combining.**

Now, with the proper switching and at the same time grounding or tri-stating the PAs (depending on the various power level as it is explained further down), all the primary transformers will be engaged in delivering power to the secondary and so higher efficiency at back-off would be achieved. The proposed system is shown in Fig. 5-3.

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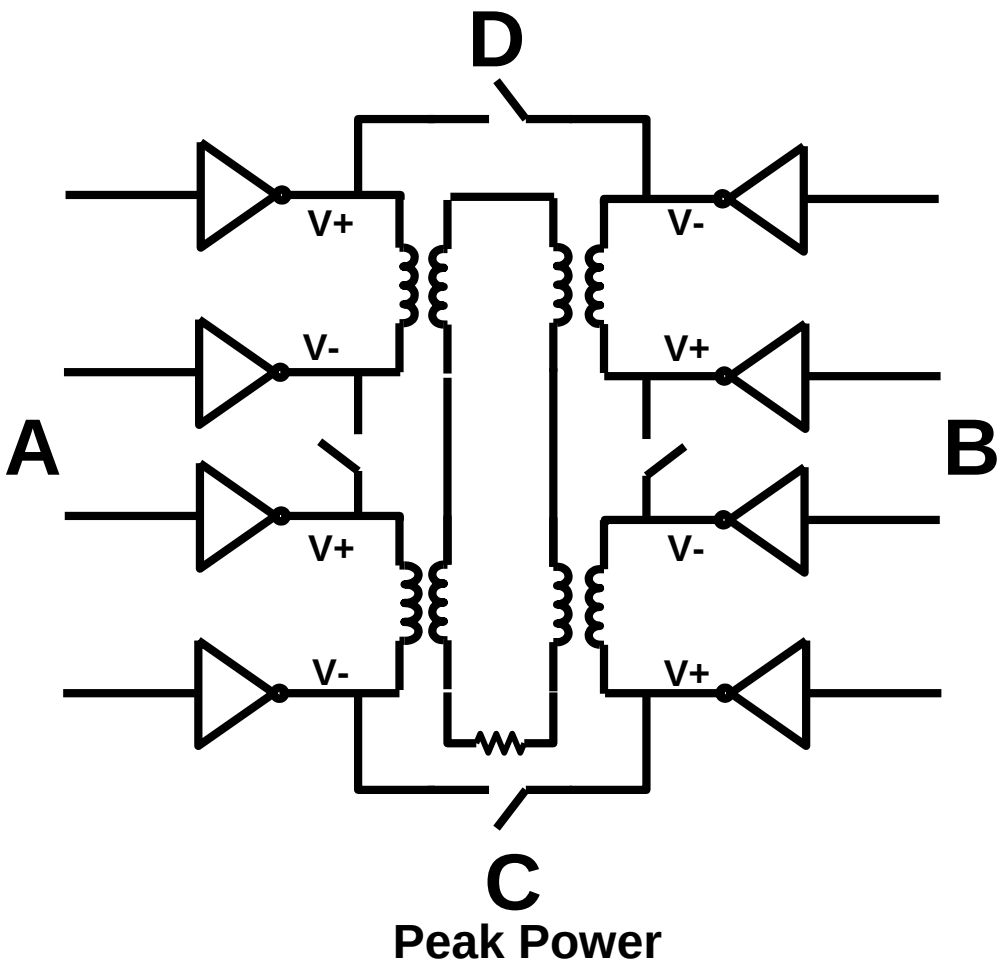



**Fig. 5-3: Proposed transformer combining, digitally-scalable transformer-combining PA (DST-PA).**

### 5.1.1 6dB back-off operation

In this proposed method shown in Fig. 5-3, the addition of switches A, B, C and D maintains the matching network of the power amplifier, resulting in efficient operation of the remaining active sections of the power amplifier and good back-off efficiency. Switches are used to connect primary coils when turning the corresponding PA sections off to achieve power back off. For example, to achieve 6dB back off, the middle PA sections (section A, B) are turned off and use SW1 and SW2 to connect the corresponding primary coils. In this case, inactive sections of the PA can be tristated as in Fig. 5-4, or grounded as in Fig. 5-5. The addition of switches (SW1 & SW2) helps as follows:

***Inactive PA sections tristated*:** In the conventional approach, tristated PA sections do not dissipate power (at least in theory). However, open circuit in the primary results self inductance is seen in the secondary and it disturbs the matching network, reducing the efficiency of the active PA sections. In the proposed solution, the addition of SW1 and SW2 maintains the matching network of the PA intact, resulting in efficient operation of the remaining active sections of the PA and good back off efficiency.

***Inactive PA sections grounded*:** The power amplifiers are considered to be turned off by grounding when they are at virtual ground points (e.g., the midpoint of differential signals). In this case, the Ron of the grounded power amplifiers dissipates power without delivering any useful power to the load. The addition of large SW1 and SW2 reduces overall power amplifiers' Ron by making a parallel combination of switch resistances and power amplifiers' Ron, which, in turn, reduces the power loss. For this case, in some cases, dc blocking capacitors are used to prevent dc current from flowing from active power amplifiers

to ground. If this DC blocking cap is absorbed into the transformer design as part of the matching network, then the switch is placed directly at the power amplifier outputs. Figure 5-7 shows an example of this configuration.

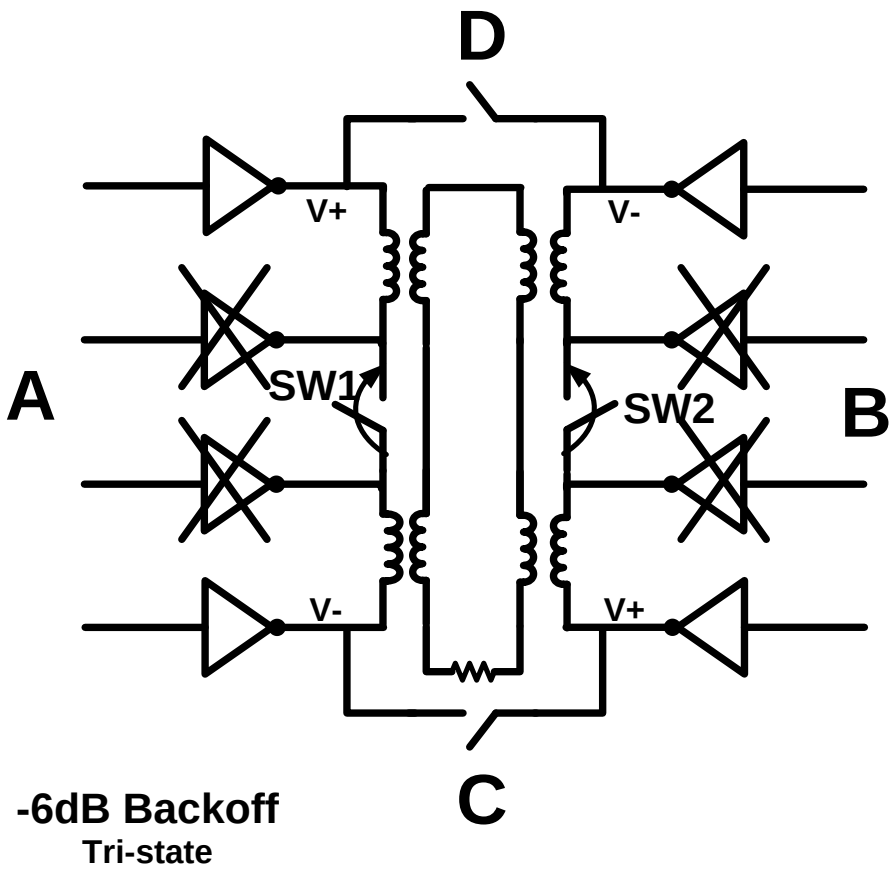



**Fig. 5-4: Proposed transformer combining at 6dB back-off by Tri-stating.**

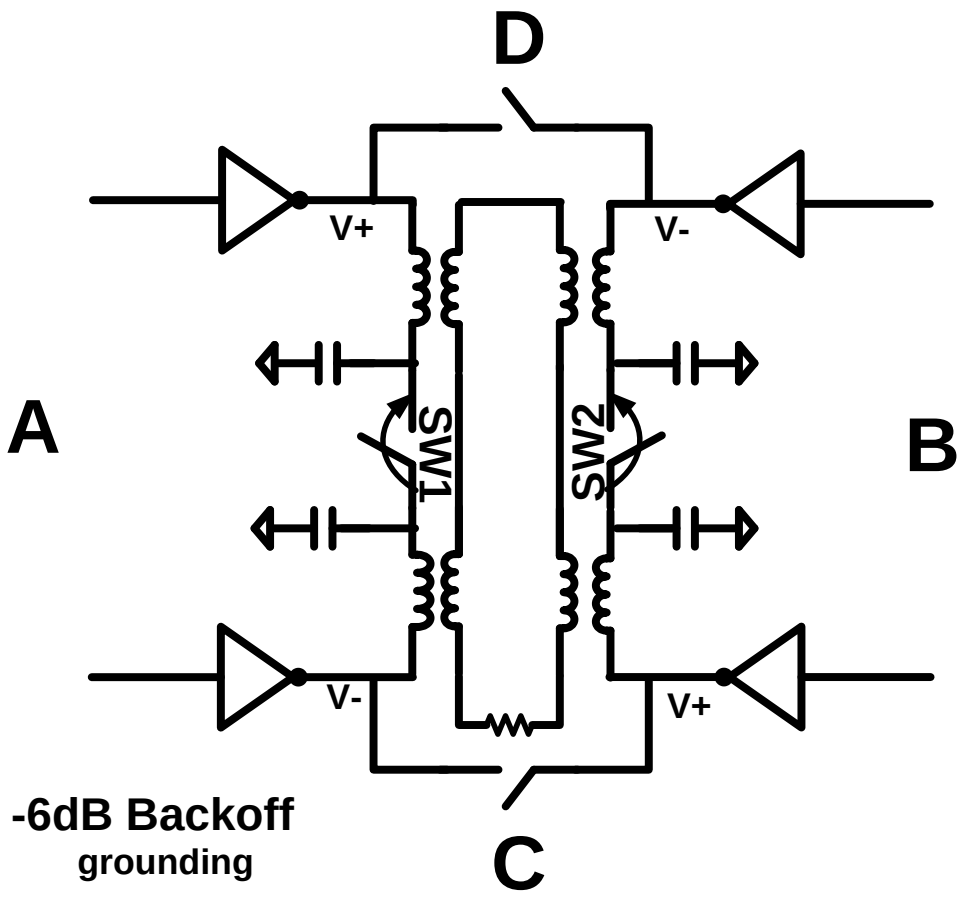



**Fig. 5-5: Proposed transformer combining at 6dB back-off by grounding.**

### 5.1.2 12dB back-off operation

Fig. 5-6 shows the transformer arrangement at 12dB back off. Here PA sections A-B-C are turned off. At this power level, the middle PA sections A and B-need to be tri-stated, otherwise similar as figure 5-2, the RF power induced by the secondary is dissipated in bottom 2 sections, which are terminated by grounds on both side. However, the bottom PA section C can be grounded or tri-stated as analyzed above, since it is at a virtual ground point.

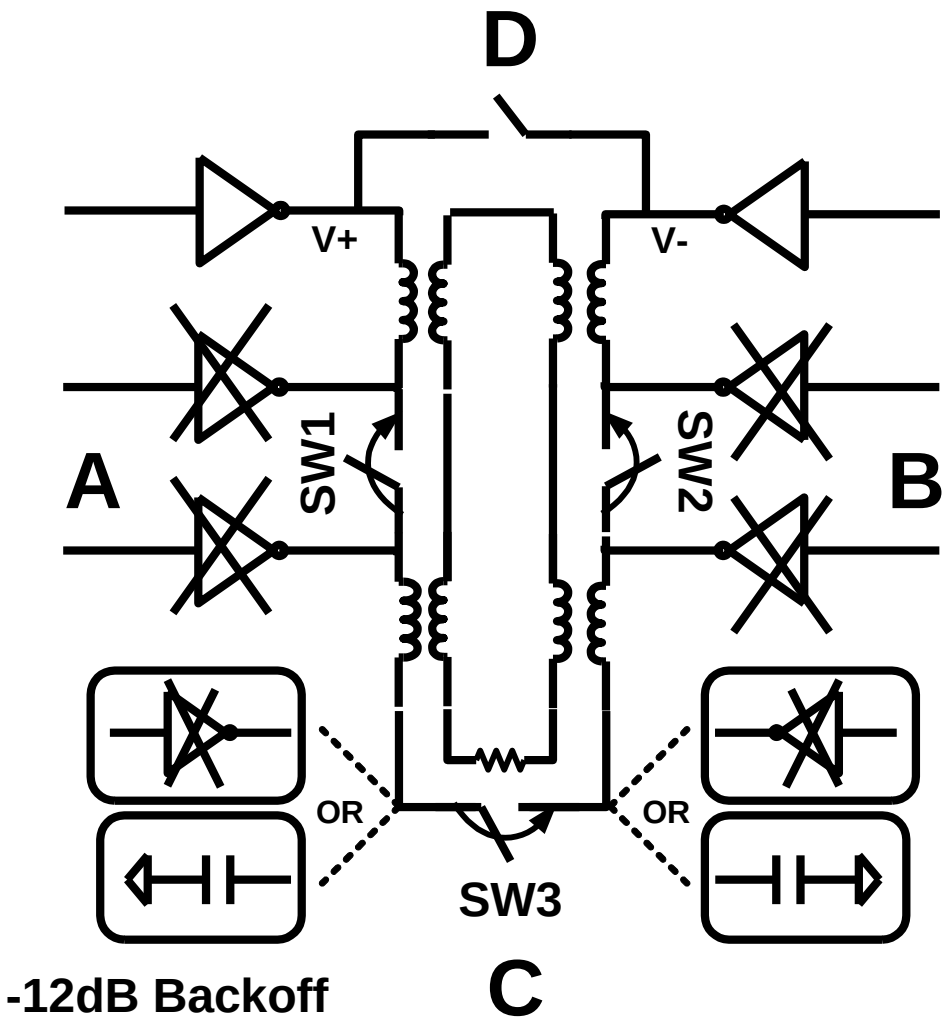



**Fig. 5-6: Proposed transformer combining at >12dB back-off.**

## 5.2 Amplitude resolution

The above techniques have been tested with both outphasing power amplifiers and switching polar power amplifiers (Figure 5-7). Both of these power amplifier architectures have similar efficiency numbers at peak, -6 dB, and – 12 dB back-offs. However, their efficiency differs significantly at intermediate power levels (between – 12 dB and – 6 dB and

between – 6 dB and 0 dB). Polar switching power amplifiers have been found to give very good efficiency across power levels, as shown in Figure 5-8. This technique may also be applicable to other power amplifier classes (e.g., class-AB) to achieve discrete steps of 6 dB, 12 dB, etc.

Figure 5-7, shows a comparison plot of the proposed combiner with two different modulation methods (polar and outphasing) as well as a comparison to the class A and recently proposed SCPA [18].

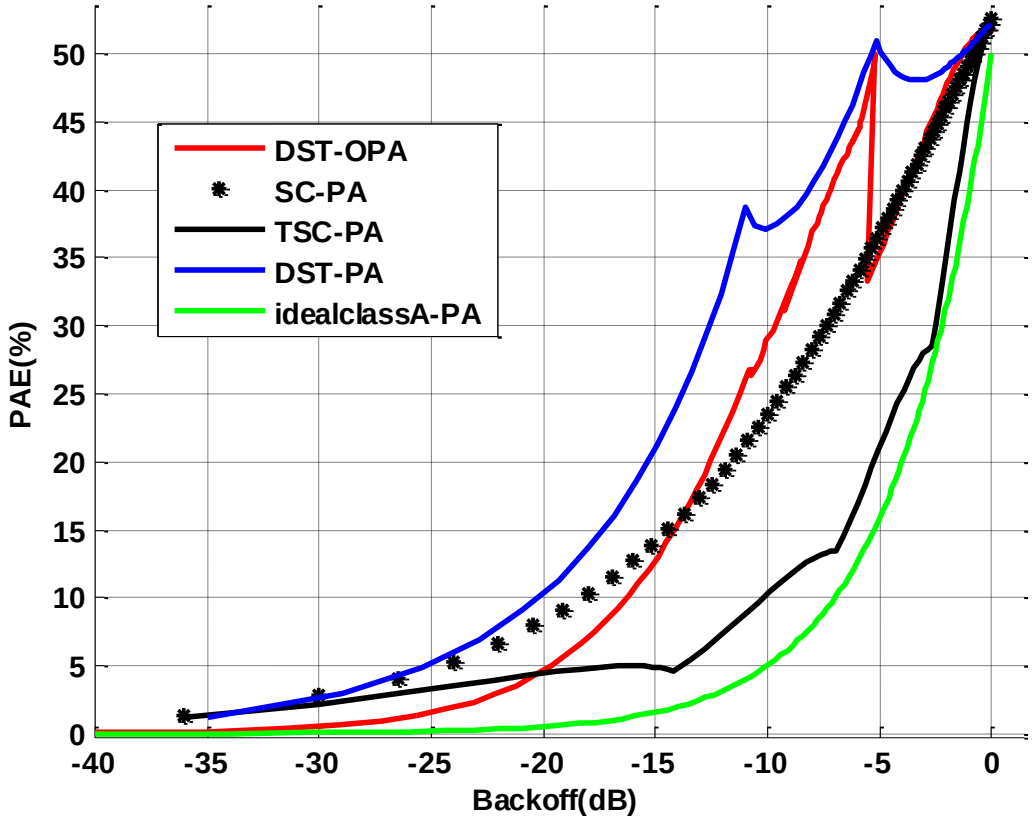



**Fig. 5-7: Comparison of different PAs with the proposed transformer combiner.**

Even though, 4 transformers are used here to explain the concept, it can be extended to more steps as more transformers are included. The proposed technique can be used with any transformer-based PA to achieve discrete steps of 6, 12, etc dB while maintaining efficiency. It can also be combined with turning on-off smaller sections of the PA to achieve very efficient switching polar operation. An example polar PA that employs the proposed efficiency enhancement technique is shown in Fig. 5-8.

The specific amplitude mapping used has a significant impact on achieved efficiency characteristic over power. The graph in Figure 5-8 plots power out (Pout) versus power added efficiency (PAE). From peak power, marked as region I, (where all power amplifiers are turned on) and all the switches are open, power is reduced by alternatively turning off sections of power amplifiers A and B and then C and D (and closing the corresponding switches). Region II shows the power back-off from the peak power to - 6 dB back-off. In this region, the power amplifiers A and B are turned off alternatively, one from each section, until all N power amplifiers are turned off by either tri-stating or grounding them and closing their corresponding switches simultaneously. At the end of this region, the A and B power amplifiers are off and their switches are closed while the C and D power amplifiers are on and their switches are open. Region III shows the power back off from - 6 dB to - 12 dB. In this region, all power amplifiers in sections A and B are tri-stated and the corresponding switches closed, while section C power amplifiers are turned off, one by one, and their corresponding switches closes simultaneously, until all N power amplifiers in section C are off. Region IV shows power back-off below - 12 dB. In this region, all the A and B power amplifiers are the same as in region III and all the section C power amplifiers are either tristated or grounded and their corresponding switches are closed. The power amplifiers in

section D are turned off, one by one, either by grounding or tristating until all the N power amplifiers are off and their corresponding switches are closed.

**Table 1. Amplitude mapping**

| | I | II | III | IV |
|---|---|---|---|---|
| **A** | PA: N on<br>SW: N open | PA: 1→ N tri/gnd<br>SW: 1 → N closes | PA: N tristated<br>SW: N closed | PA: N tristated<br>SW: N closed |
| **B** | PA: N on<br>SW: N open | PA: 1→ N tri/gnd<br>SW: 1 → N closes | PA: N tristated<br>SW: N closed | PA: N tristated<br>SW: N closed |
| **C** | PA: N on<br>SW: N open | PA: N on<br>SW: N open | PA: 1→ N tri/gnd<br>SW: 1 → N closes | PA: N tri/gnd<br>SW: N closed |
| **D** | PA: N on<br>SW: N open | PA: N on<br>SW: N open | PA: N on<br>SW: N open | PA: 1 → N tri/gnd<br>SW: 1 → N closes |

**Table 5-1: Example of an amplitude mapping.**

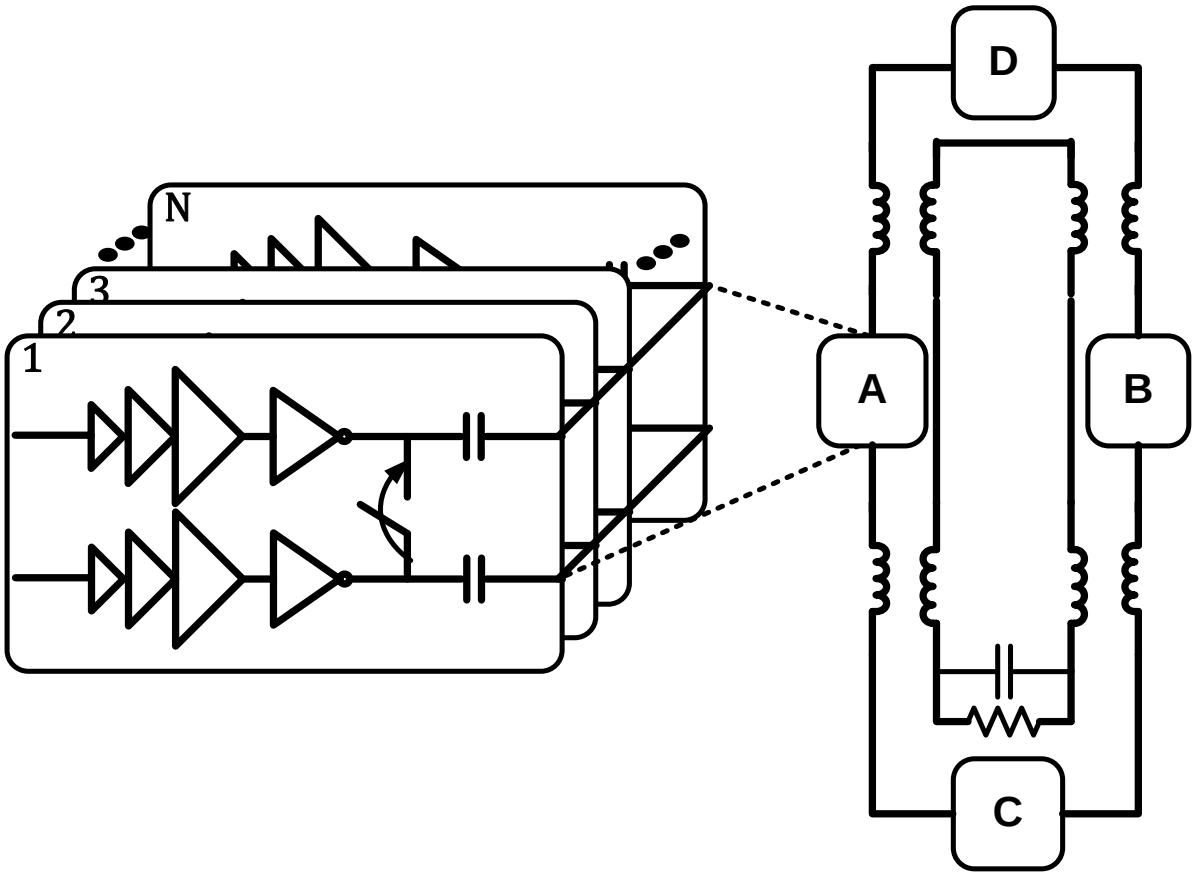



**Fig. 5-8: Proposed transformer combining embedded in a polar PA architecture.**

## 5.3 Different Switching Scheme Comparison

Another important fact is to maintain the symmetric configuration of the transformer as turning off PA sections. For example in Fig. 5-3 or 5-8, instead of turning off section A and C to reduce power level by 6dB, turning off section A and B give better efficiency. This is required to enforce good differential PA pair operation, which could be impaired due to non-ideal transformers and parasitic otherwise. So how to switch off PAs at steps of lower power is important factor as planed in Fig 5-8 and Table 5-1. In the next section,

different switching modes have been compared with each other all having the consideration of have a symmetric switching scheme for power control.

Different switching methods and their evaluations, (note: by turning off it means tri-stating unless it is stated otherwise):

Moda - Start turning off PAs one from each side at the same time until half out of total PA sections are off (-6dB). For the rest of the power control, start turning them off the entire bottom PAs and then all the top PAs.

Modb - Start turning off PAs one from left and one from right side until the half out of total PA sections are off (-6dB). For the rest of the power control, start turning them off the entire bottom PAs and then all the top PAs.

Modc - Start turning off PAs one from left and one from right side until the half out of total PA sections are off (-6dB). For the rest of the power control, start turning them off one from the top and bottom alternatively until the end.

Modd - Start turning off PAs one from left and one from right side until half out of total PA sections are off (-6dB). For the rest of the power control, start turning them off the entire bottom PAs and then all the top PAs.

Mode - Start turning off PAs one from left and one from right side until half out of total PA sections are off (-6dB). Then ground both top and bottom while their switches are also open.

Modf - Start turning off PAs one from left and one from right side until half out of total PA sections are off (-6dB). Then from -6dB to -12dB ground PAs and close the switches and then from -12 to 0 ground the PAs but leave the switch open as well.

Figures 5-9 to Figure 5-14 show the above case with ideal schematic simulations for a 6-bit polar pa. Figure 5-9 shows output power versus input codes while figure 5-10 shows the zoomed in version of figure 5-9 to show the more detailed amplitude steps. Figure 5-11, shows both logarithmic axis of the output power vs. input code which shows pretty linear PAs in all cases. Figure 5-12 shows the PAE vs. the input codes. In this figure even though all the switching methods, show same -6dB back off but their differences manifest at -12dB back off and it is the same as expected in Figure 5-13 which shows PAE vs. output power. Figure 5-14 shows the AM-PM distortion.

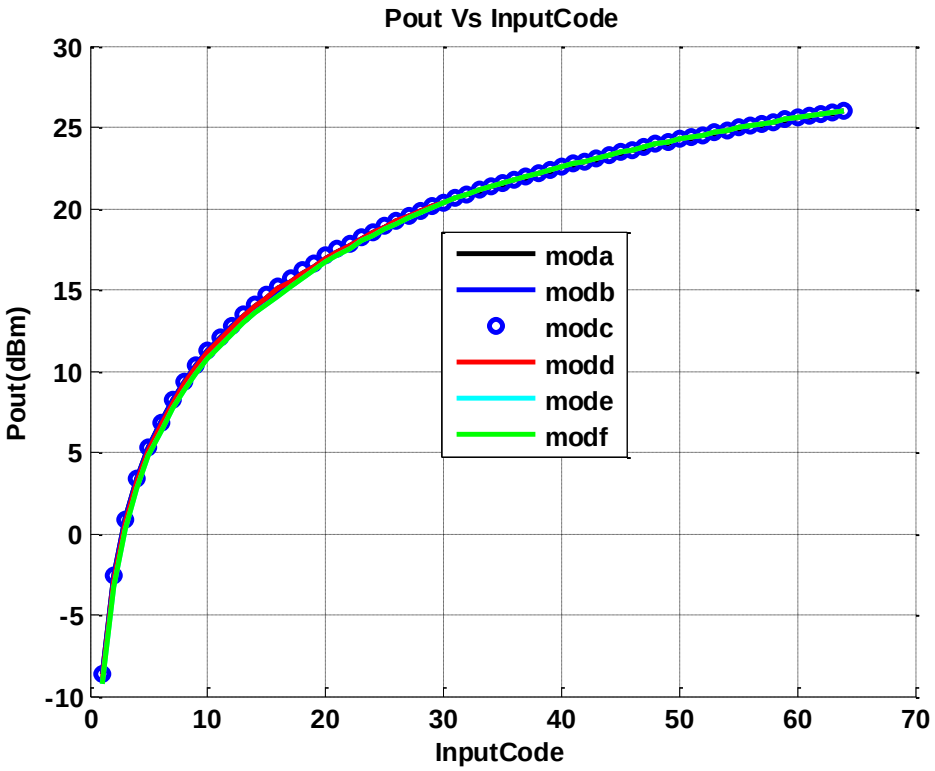



**Fig. 5-9: Output power vs. input code for different switching schemes.**

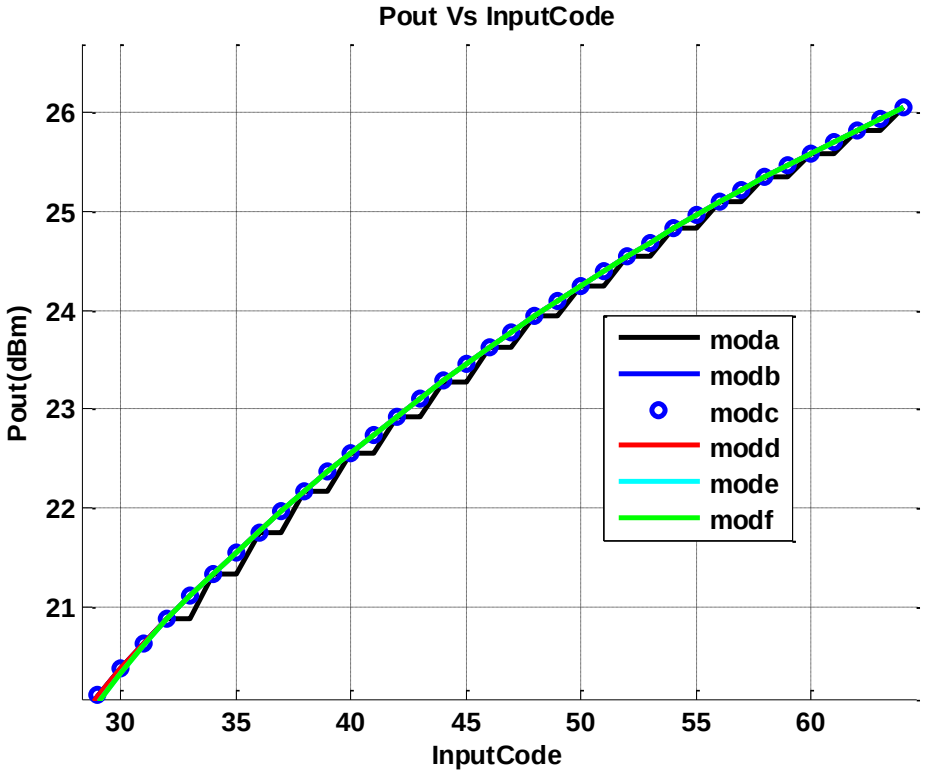


**Fig. 5-10: zoomed in to the last power steps of Output power vs. input code for different switching schemes.**

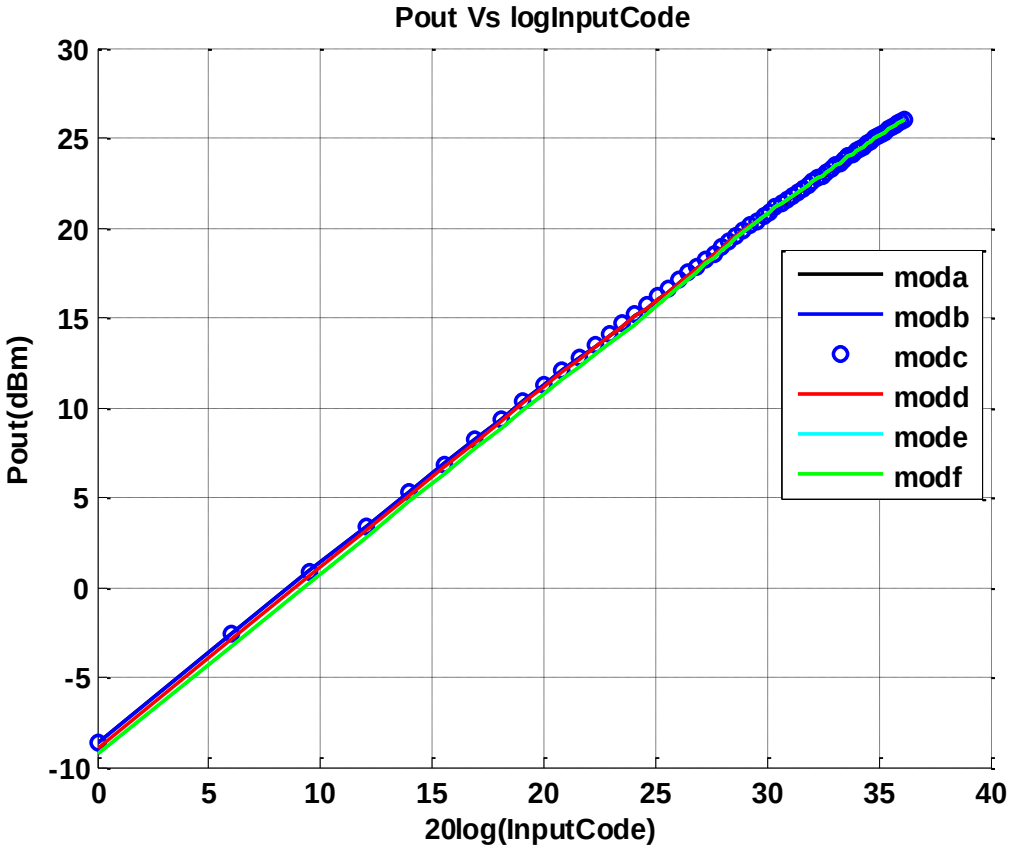



**Fig. 5-11: Output power vs. log of input code for different switching schemes to see the linearity better. (AM-AM)**

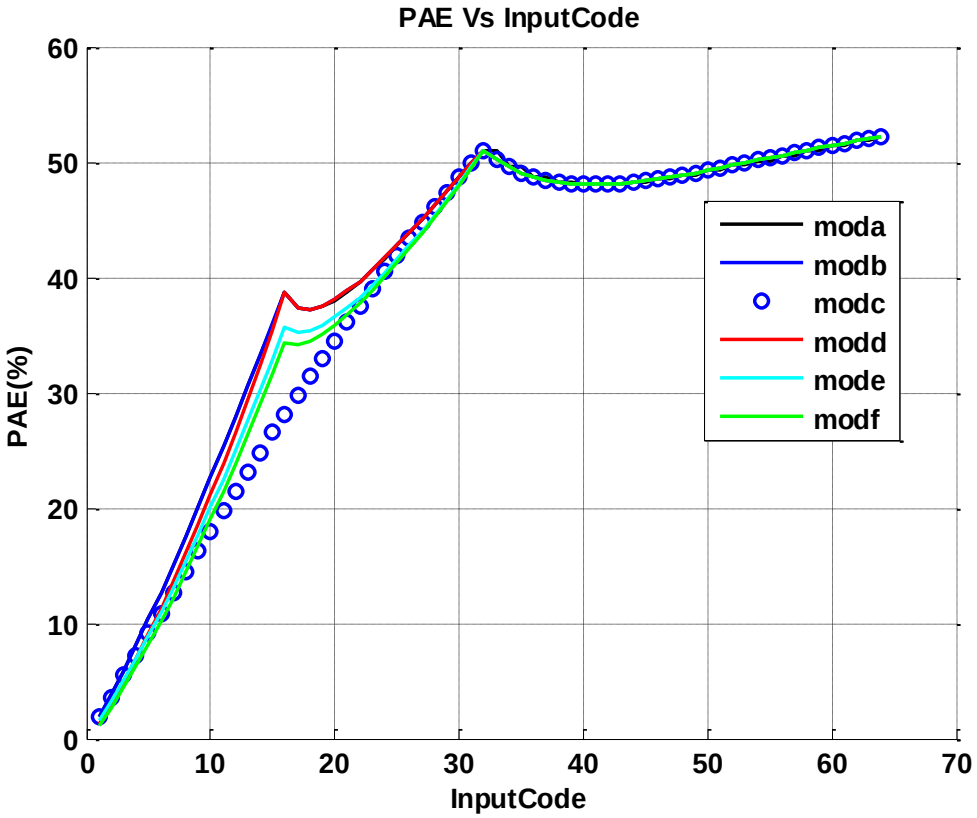



**Fig. 5-12: PAE vs. input code for different switching schemes.**

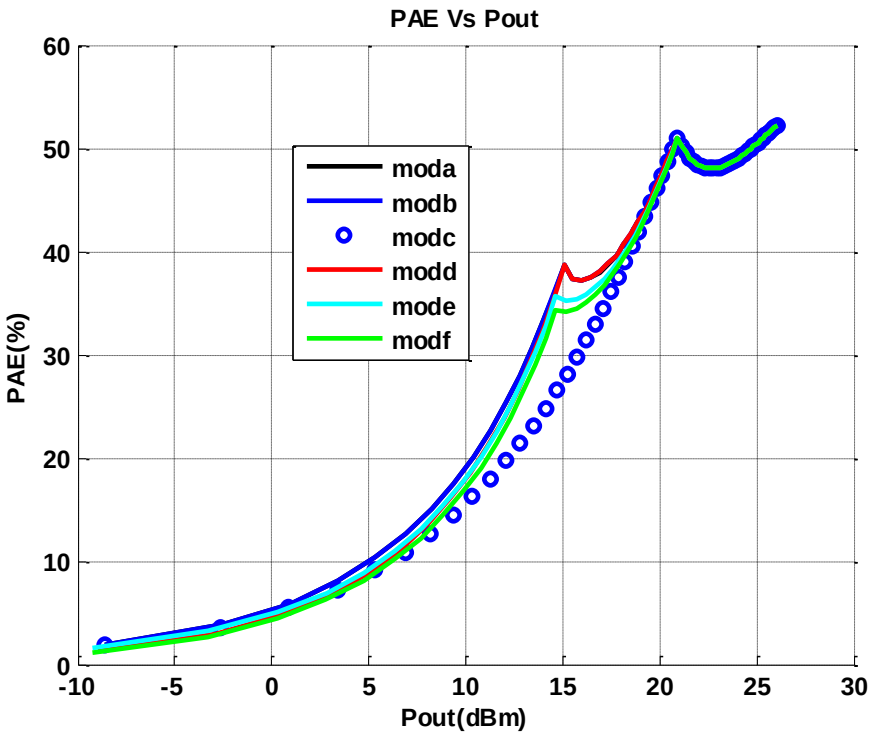



**Fig. 5-13: PAE vs. Output power for different switching schemes.**

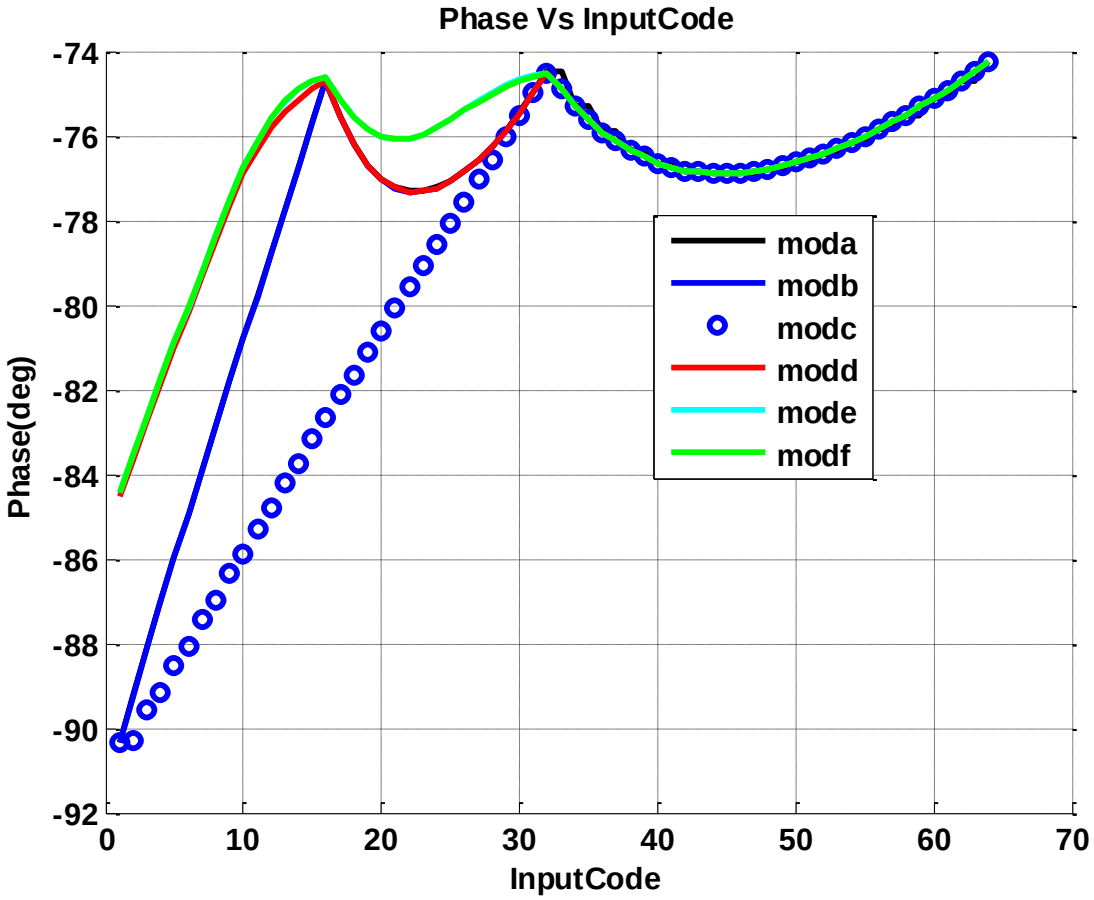



**Fig. 5-14: Phase vs. Output power for different switching schemes. (AM-PM)**

From the above comparison – it seems MODD has overall better efficiency as well as AM-AM and AM-PM. Even though symmetry was considered in all these cases (otherwise, efficiencies would have been much lower) but the key contribution for the differences, is if the transformer been in the full use mostly or not. For example, MODC performs as conventional combiner but since the transformer gets out of the main loop for power steps after 12dB back off, the second peak in efficiency is gone.

## 5.4 Theoretical Analysis

In this section, some design consideration as well as the linearity and efficiency analysis for this PA is being presented.

### 5.4.1 Efficiency

Consider an ideal transformer for the proposed combiner (Fig. 5-3). It is shown in Fig. 5-15. At the peak power when all the switches are open, the combiner looks like a conventional combiner. The load seen by each primary side of the combiner is $R_L/N$ which N stands for the N combiner. In our case, N is always 4, since it is a 4 to 1 combiner. A switching PA can be modeled as a Thevenin equivalent, which Vthevenin=Vin and Rthevenin=$r_{on}$ of the PA as it is shown in Fig. 5-16.

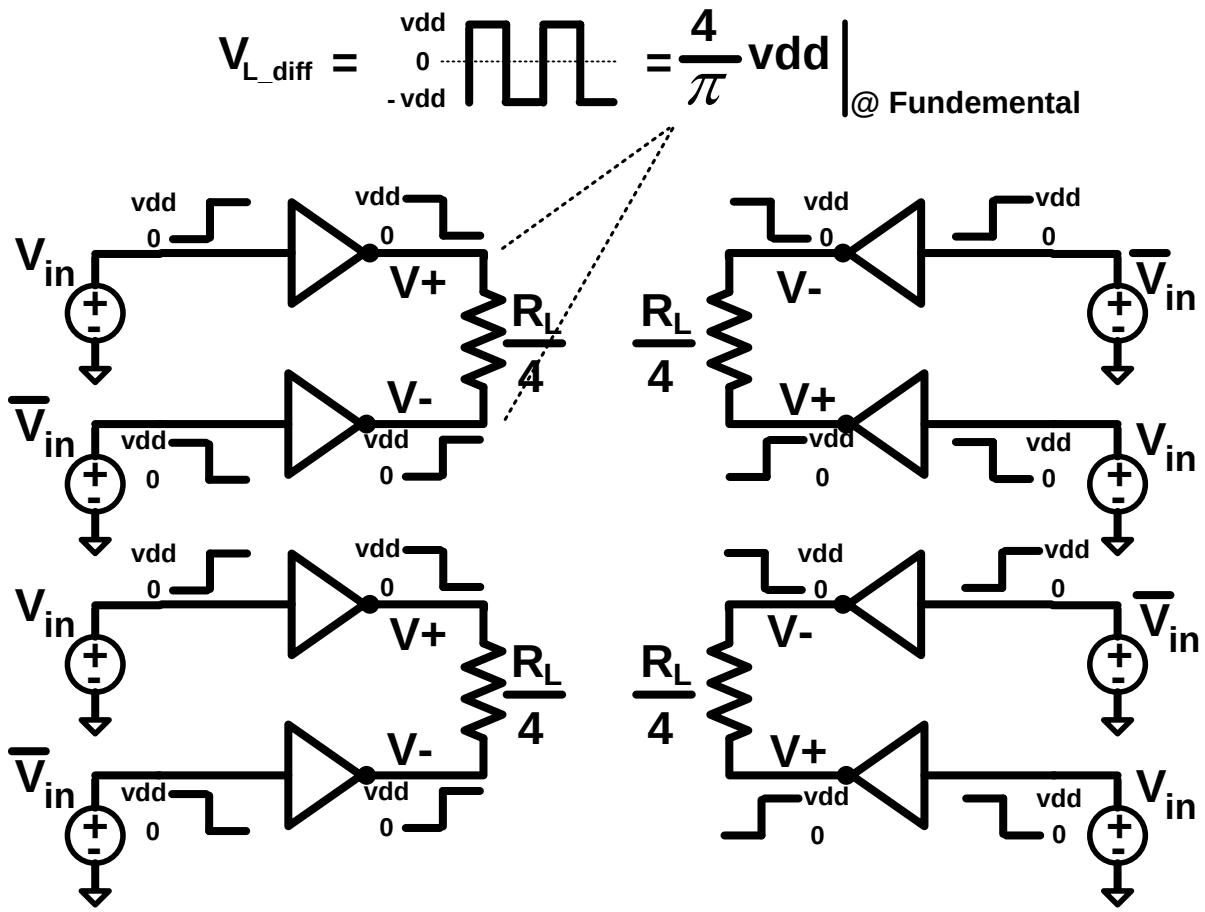



**Fig. 5-15: Ideal 4 x 1 power combiner.**

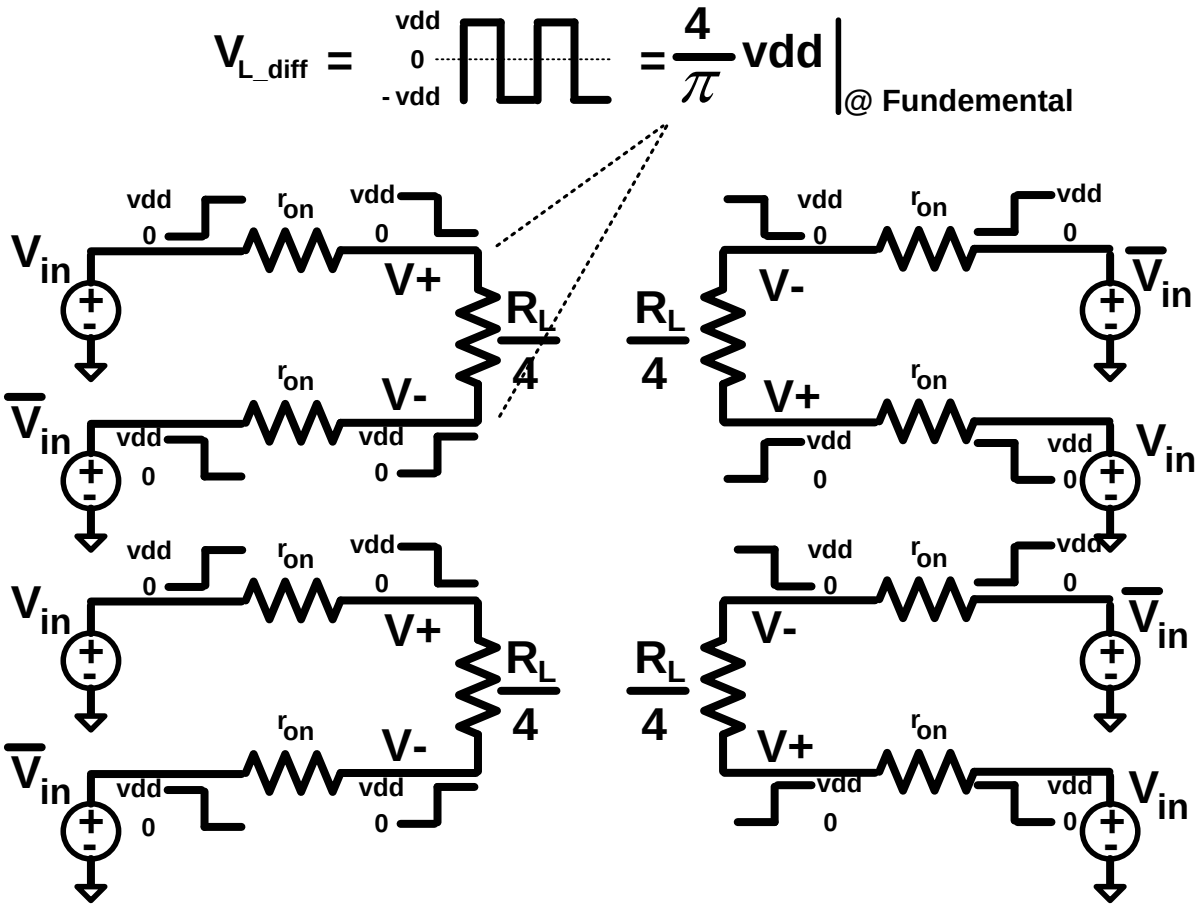



**Fig. 5-16: Ideal 4 x 1 power combiner with PA thevenin Equivalent.**

The total output power delivers to the load:

$$P_{out\_total} = 4 \times \frac{(V_{L\_diff})^2}{2R} \tag{5.1}$$

This assumes the fundamental component of the PA output at the load:

$$V_{L_{diff}} = \left(\frac{4}{\pi}\right) vdd \frac{R}{R+2r_{on}} \tag{5.2}$$

$$R = \frac{R_L}{4} \tag{5.3}$$

$$P_{out\_total\_@pk} = 4 \times \frac{\left(\left(\frac{4}{\pi}\right) vdd \frac{R}{R+2r_{on}}\right)^2}{2R} \tag{5.4}$$

The total DC power:

$$P_{dc_{total_{@pk}}} = 4 \times i_{dc} \times vdd$$

$$= 4 \times \frac{vdd}{R+2r_{on}} \times vdd = 4 \times \frac{1}{R+2r_{on}} \tag{5.5}$$

Now, assuming PAE with no driver power consumption or in other words the drain efficiency (DE) of the PA:

$$DE_{@pk} = \frac{P_{out\_total}}{P_{dc\_total}} = \left(\frac{8}{\pi^2}\right)\left(\frac{\frac{R_L}{4}}{\frac{R_L}{4}+2r_{on}}\right) \times 100\% \tag{5.6}$$

If we assume ideal PA $r_{on} = 0$, then DE becomes approximately to 81%. This is the fundamental efficiency. The reason that this is not 100% despite all ideal assumption is due to wasted power in the harmonics of the square wave. If using some methods like harmonic filter or harmonic trap or harmonic rejection, then this would approach to 100% ideally.

Now, consider the -6dB back off of the proposed transformer combiner with PA thevenin equivalent in Fig. 5-17.

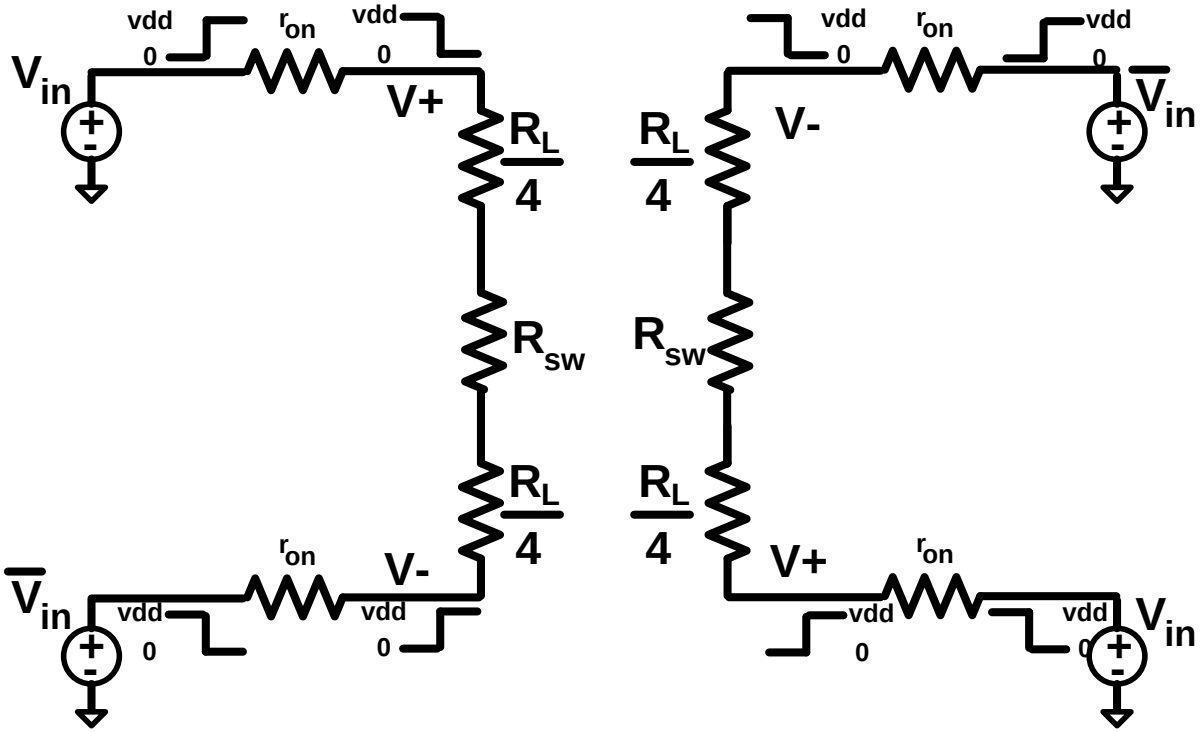



**Fig. 5-17: proposed 4 x 1 power combiner (ideally) with PA thevenin Equivalent @ -6dB back-off.**

$$V_{L_{diff}|@6dB} = \left(\frac{4}{\pi}\right) vdd \frac{2R}{2R+2r_{on}+r_{sw}} \tag{5.7}$$

The total output power delivers to the load at -6dB back-off using equation (5.3):

$$P_{out\_total\_@6dB} = 2 \times \frac{\left(\left(\frac{4}{\pi}\right) vdd \frac{2R}{2R+2r_{on}+r_{sw}}\right)^2}{2 \times 2R} \tag{5.8}$$

The total DC power:

$$P_{dc_{total_{@6dB}}} = 2 \times i_{dc} \times vdd = 2 \times \frac{vdd}{2R + 2r_{on} + r_{sw}} \times vdd$$

$$= 2 \times \frac{1}{2R+2r_{on}+r_{sw}} \quad (5.9)$$

$$DE_{@-6dB} = \frac{P_{out\_total}}{P_{dc\_total}} = \left(\frac{8}{\pi^2}\right)\left(\frac{\frac{R_L}{2}}{\frac{R_L}{2}+2r_{on}+r_{sw}}\right) \times 100\% \quad (5.10)$$

If diving the numerator and denominator by a factor of 2, it can be seen that if $r_{sw} = 2r_{on}$, then the same efficiency as the peak power would be achieved.

Same as peak power, if we assume ideal PA $r_{on} = 0$ & $r_{sw} = 0$, then DE becomes approximately to 81% which is the same as peak DE of the fundamental.

The behavior of efficiency curve can be explained as follow:

Assume a case where there are only 4 total PAs unit cells, where each of them is called A, B, C, D. Let's consider only two case: the peak power and -6dB. Assume PAs C and D are always on and PAs A and B are turned off for -6dB. Since there is no driver power consumption is being considered, let's look at the drain efficiency:

$$DE = \frac{P_{out}}{I \times V} \quad (5.11)$$

Assume V is a constant and in this case, it is 1v supply. From the above equation efficiency is proportional to the output power and in reverse relation with supply current. On the other hand, ideally, the loaded Q at the peak power and -6dB back-off are equal since the on PAs see the same scaled load resistance and inductance (both doubles than the situation at the peak power). Therefore:

$$Q_{loaded-peak} = Q_{loaded-6dB} = \frac{\omega L}{R_L} \quad (5\text{-}12)$$

$$\Rightarrow DE_{peak} = DE_{-6dB} \quad (5\text{-}13)$$

At the peak power, the Pout of each unit PA, contributes ¼ of the power to the output, therefore, the current of each unit PA is ¼ of the total current:

$$Pu_{pk} = \frac{P_{pk}}{4}, V = 1v \Rightarrow Iu_{pk} = \frac{Pu_{pk}}{DE_{pk}} \Rightarrow Iu_{pk} = \frac{P_{pk}}{4 \times DE_{pk}} \quad (5\text{-}14)$$

At -6dB back-off, units A and B are off and only C and D are on. Therefore, the total power which is the ¼ of the peak power, the current divides by two for each "on" PA unit:

$$Pu_{-6dB} = \frac{1}{2} \times \frac{P_{pk}}{4} \xrightarrow{DE_{peak} = DE_{-6dB}} Iu_{-6dB} = \frac{1}{2} \times Iu_{pk} \quad (5\text{-}15)$$

Therefore, writing a general formula for the DE for these 4 unit PAs:

$$DE_{total} = \frac{2P_{CD} + 2P_{AB}}{\frac{2P_{CD}}{DE_{CD}} + \frac{2P_{AB}}{DE_{AB}}} \quad (5\text{-}16)$$

Where $P_{CD}$and $P_{AB}$ stands for unit output power for each C, D and A and B. Sicne AB have the same characteristics they are grouped together and so as C and D.

Fig. 5.a shows DE vs. Pout. At the peak power, each unit PAs are at their peak efficiency so all starts at the same point. Units C and D stays the same throughout back-off because are always on but unit A,B scale down as their sub-units turns off until all are off at -6dB back

off, so they follow a curve like blue one. Therefore, the overall efficiency curve is a combination of the blue and black curve results in red curve.

$from\ DE_{total}\ equation$:

$$at\ peak: P_{CD} = P_{AB}\ \ \&\ \ \ DE_{CD} = DE_{AB} \Rightarrow\ \ DE_{total} =\ DE_{unit} \quad (5\text{-}17)$$

$$at - 6dB: P_{AB} \to 0\ \ \Rightarrow$$

$$DE_{total} = \frac{2P_{CD}+0}{\frac{2P_{CD}}{DE_{CD}}+\frac{0}{DE_{AB}}} = DE_{CD} = DE_{unit} \quad (5\text{-}18)$$

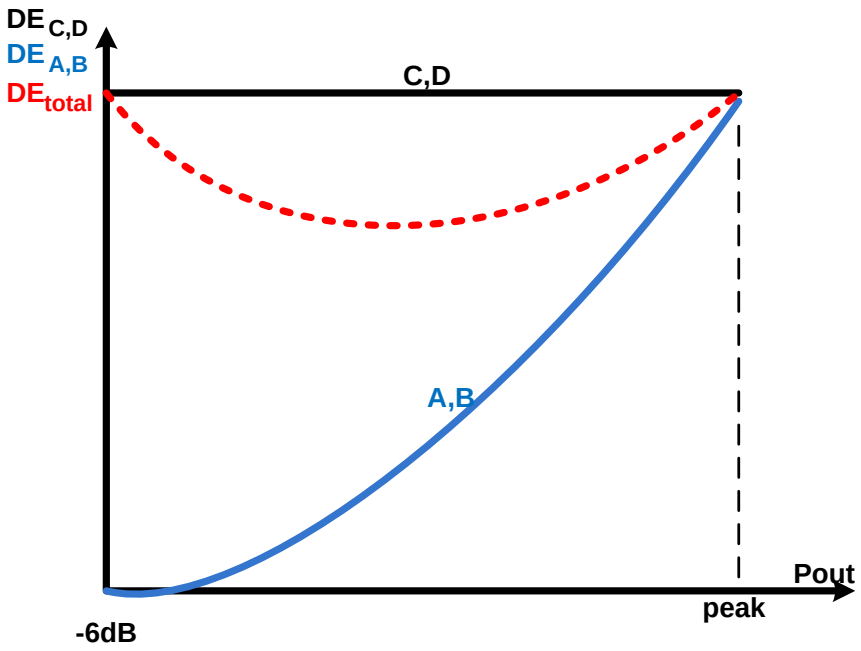



**Fig. 5-17a: drain efficiency vs. output power.**

Figure 5-b, shows the circuit model for the in between steps of the power control.

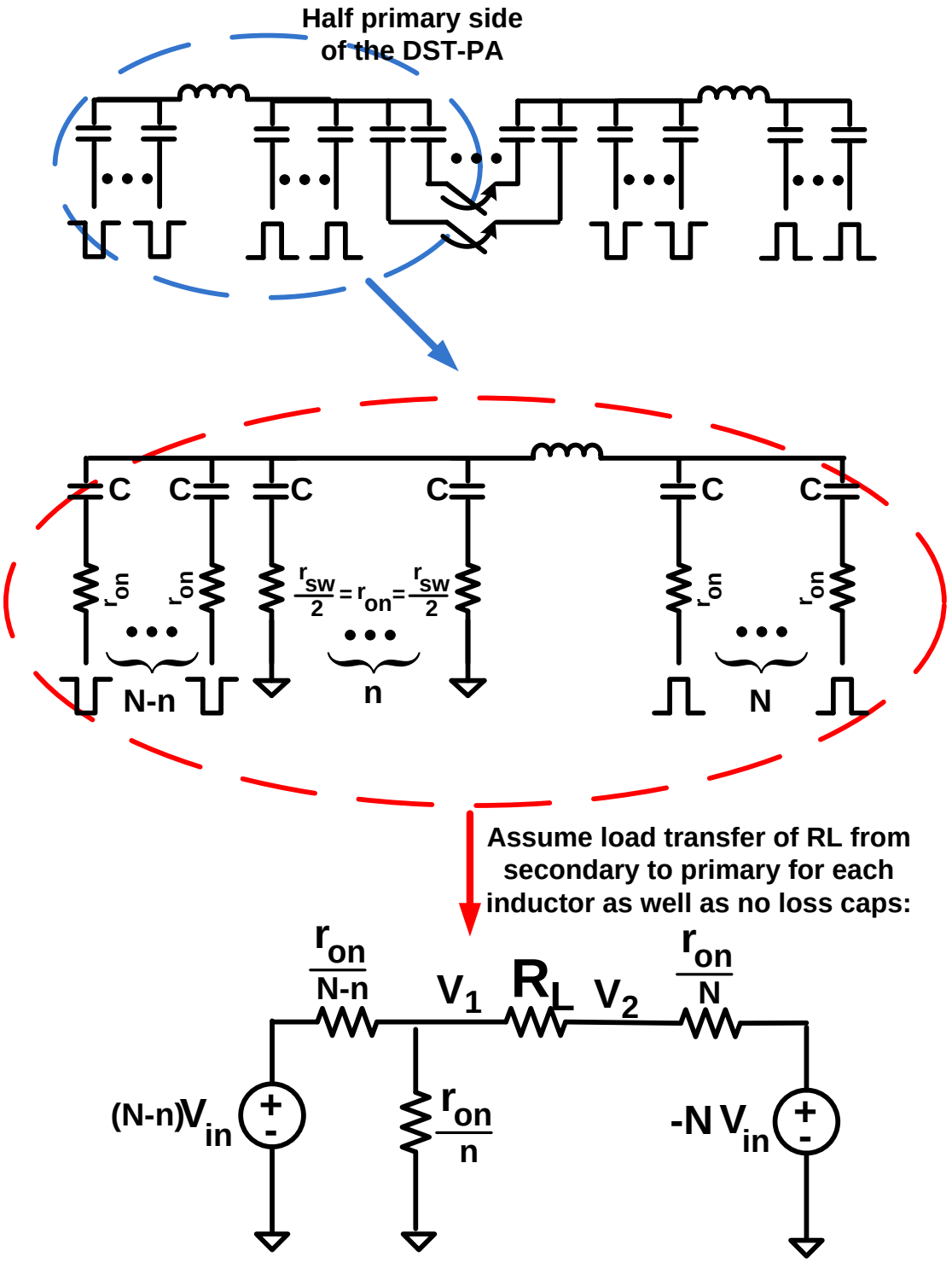



**Fig. 5-17b: circuit model for in between power steps.**

$$V_L = V_1 - V_2 \qquad (5\text{-}19)$$

***Using Superposition***:

$\boldsymbol{when\ vin\ source = 0 \Rightarrow}$

$$\boldsymbol{V_L' = V_1 \frac{R_L}{R_L + \frac{r_{on}}{N}}} \qquad (5\text{-}20)$$

$$\boldsymbol{V_1 = (N-n)V_{in} \frac{\frac{r_{on}}{n} || \left(R_L + \frac{r_{on}}{N}\right)}{\frac{r_{on}}{N-n} + \frac{r_{on}}{n} || \left(R_L + \frac{r_{on}}{N}\right)}} \qquad (5\text{-}21)$$

$$\boldsymbol{if \qquad Req = \frac{\frac{r_{on}}{n}\left(R_L + \frac{r_{on}}{N}\right)}{\frac{r_{on}}{n} + R_L + \frac{r_{on}}{N}}}$$

$$\boldsymbol{\Longrightarrow \quad V_1 = (N-n)V_{in} \frac{Req}{\frac{r_{on}}{N-n} + Req}}$$

$$\boldsymbol{V_L' = (N-n)V_{in} \frac{Req}{\frac{r_{on}}{N-n} + Req} \times \frac{R_L}{R_L + \frac{r_{on}}{N}}}$$

$\boldsymbol{when - vin\ source = 0 \Rightarrow}$

$$\boldsymbol{V_L'' = -IR_L = \frac{-(-NV_{in})}{\frac{r_{on}}{N} + R_L + \frac{r_{on}}{n} || \frac{r_{on}}{N-n}} R_L = NV_{in} \frac{R_L}{\frac{r_{on}}{N} + R_L + \frac{r_{on}}{N}}}$$

$$\boldsymbol{\Rightarrow V_L'' = NV_{in} \frac{R_L}{\frac{2r_{on}}{N} + R_L}} \qquad (5\text{-}22)$$

$$\boldsymbol{V_L = V_L' + V_L'' = (N-n)V_{in}\frac{Req}{\frac{r_{on}}{N-n}+Req} \times \frac{R_L}{R_L+\frac{r_{on}}{N}} + NV_{in}\frac{R_L}{R_L+\frac{2r_{on}}{N}}}$$

(5-23)

$\boldsymbol{if\ n = 0\ (at\ peak\ power)}$:

$$\boldsymbol{V_1 = R_L + \frac{r_{on}}{N}}$$

$$\boldsymbol{=> V_L' = NV_{in}\frac{R_L}{\frac{2r_{on}}{N}+R_L} = V_L''}$$

$$\boldsymbol{=> V_L = V_L' + V_L'' = 2NV_{in}\frac{R_L}{\frac{2r_{on}}{N}+R_L}}$$

$$\boldsymbol{=> V_L = NV_{in}\frac{2R_L}{\frac{2r_{on}}{N}+R_L} = NV_{in}\frac{R_L}{\frac{r_{on}}{N}+\frac{R_L}{2}}}$$

Equation 5.21 and 5.23, demonstrates overall voltage output of the in between power level assuming ideal passives. The efficiency equation follows by dividing the load power using 5.21 and 5.23 voltage equations by the total current from each the source. The current, same as voltage, is calculated by superposition principle.

### 5.4.2 Linearity

Assume the same conditions as the previous section of Fig. 5-16 and Fig. 5-17. in order to compare the linearity of the system, in general it is desired the peak power to be linearly scaled which power control. Therefore, the following format is desired:

$$\frac{Pout_{pk}}{Pout_{-6dB}} = -6\ in\ dB\ scale \tag{5.11}$$

$$\frac{Pout_{pk}}{Pout_{pk/4}} = 4\ \ in\ linear\ scale \tag{5.12}$$

Therefore, from the peak and -6dB back-off equation in previous section:

$$\frac{Pout_{pk}}{Pout_{-6dB}} = \frac{4\times\frac{\left(\left(\frac{4}{\pi}\right)vdd\frac{R}{R+2r_{on}}\right)^2}{2R}}{2\times\frac{\left(\left(\frac{4}{\pi}\right)vdd\frac{2R}{2R+2r_{on}+r_{sw}}\right)^2}{2\times 2R}} = \left(\frac{2R+2r_{on}+r_{sw}}{R+2r_{on}}\right)^2 \tag{5.13}$$

$$\Rightarrow \frac{Pout_{pk}}{Pout_{-6dB}} = 4\times\left(\frac{R+r_{on}+\frac{r_{sw}}{2}}{R+2r_{on}}\right)^2 \tag{5.14}$$

$$if\ A = \left(\frac{R+r_{on}+\frac{r_{sw}}{2}}{R+2r_{on}}\right) \tag{5.15}$$

Therefore, for the peak power to be in a linear relation with -6dB back-off power, it is required term A to be 1.

$$\frac{Pout_{pk}}{Pout_{-6dB}} = 4 \quad => \quad \left(\frac{R+r_{on}+\frac{r_{sw}}{2}}{R+2r_{on}}\right)^2 = 1 \tag{5.16}$$

$$=> \quad r_{sw} = 2r_{on} \tag{5.17}$$

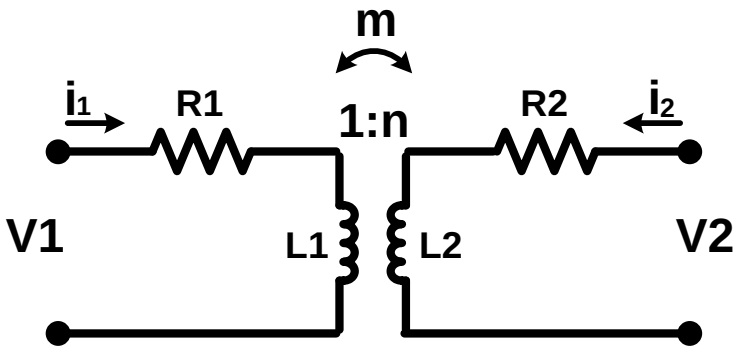
### 5.4.3 Transformer Equivalent model

For theoretical analysis, the following modeled is used for transformer in the following sections, fig. 5-18. where:

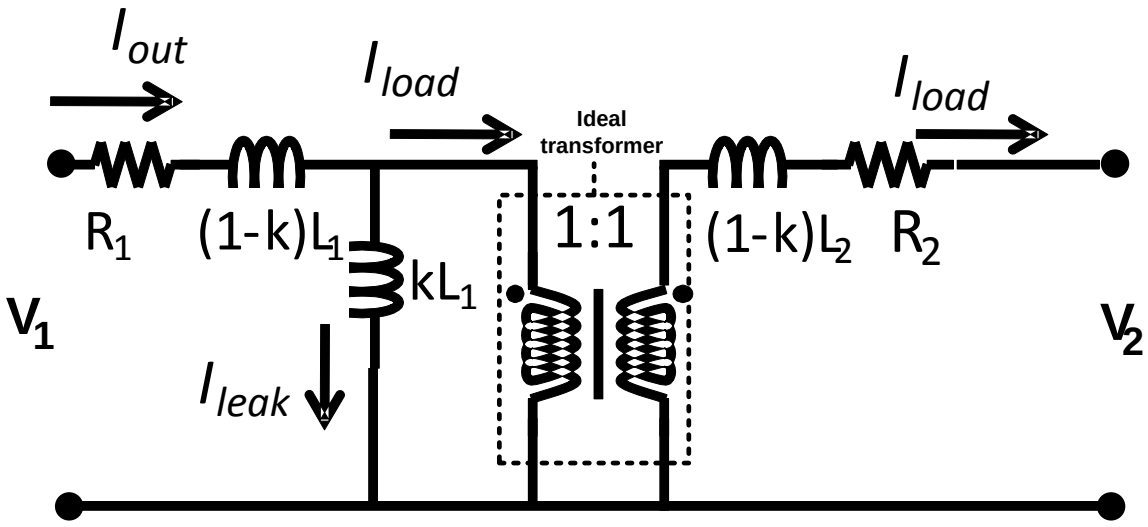
$$m(magnetic\ coupling) = k\sqrt{\frac{L2}{L1}} \tag{5.18}$$

$$n = \frac{1}{k}\sqrt{\frac{L_2}{L_1}} \tag{5.19}$$

$$L1\ and\ L2\ losses\ are\ defined\ as:\ R_1 = \frac{\omega L_1}{Q_1}\ \&\ R_2 = \frac{\omega L_2}{Q_2} \tag{5.20}$$




(a)




(b)

**Fig. 5-18: (a) a 1:n lossy transformer with magnetic coupling m. (b) its equivalent model.**

### 5.4.4 Efficiency and Linearity analysis with passives included

Fig. 5-19 and 5-20, show the whole circuit at the peak power and -6dB back-off respectively, including the passive elements. Using equation, 5-18 to 5-20, if assuming no lossy inductors and L1=L2=L and a 1 to 1 transformer, then n=K=1. Using the transformer model in Fig. 5-18 and looking at only one out of the four primaries (the others are exactly the same), results in figure 5-21.

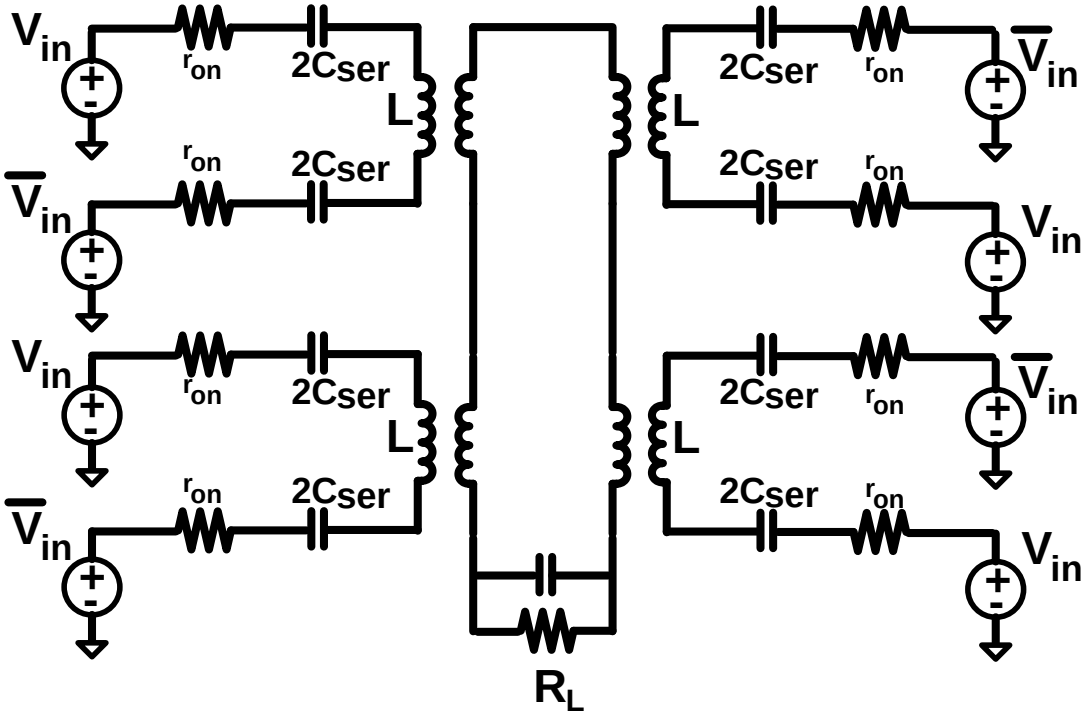



**Fig. 5-19: peak power circuit model including the passives (series caps, transformers).**

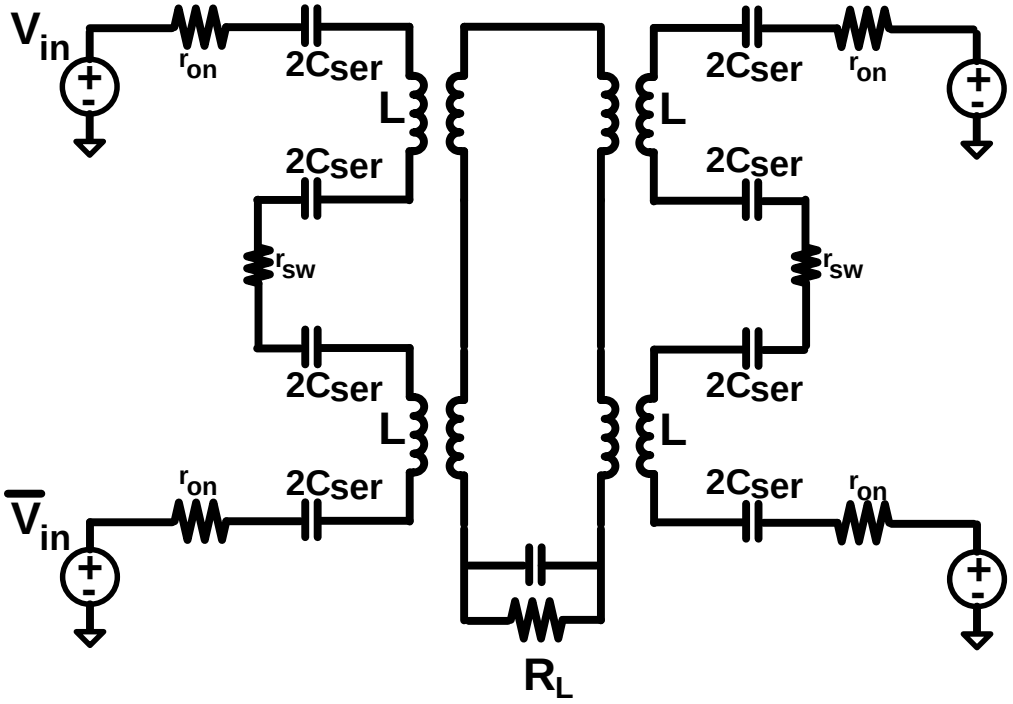
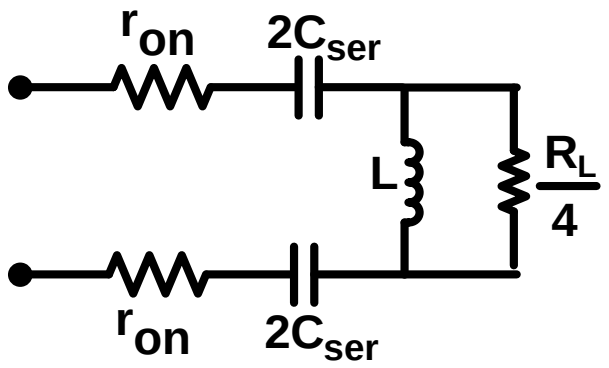
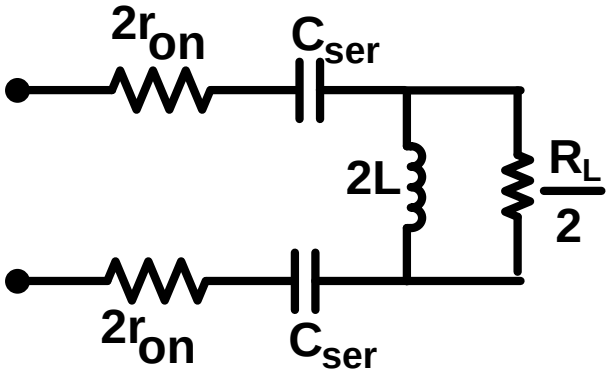



**Fig. 5-20: -6dB back-off power circuit model including the passives (series caps, transformers).**




**(a)**

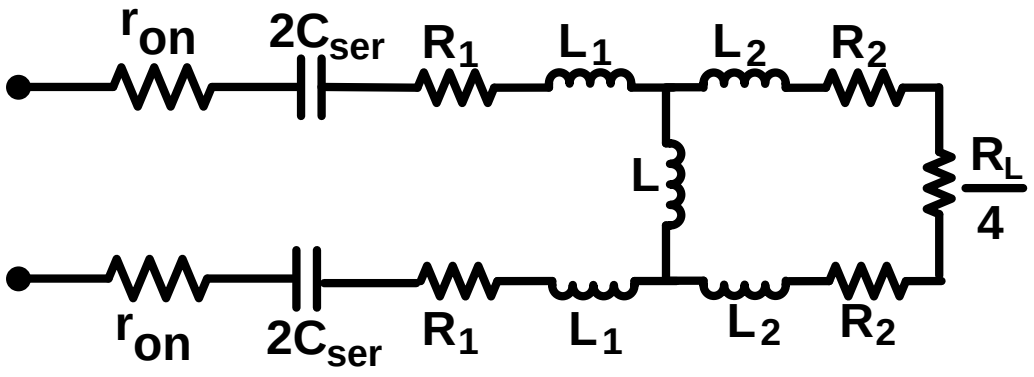



**(b)**

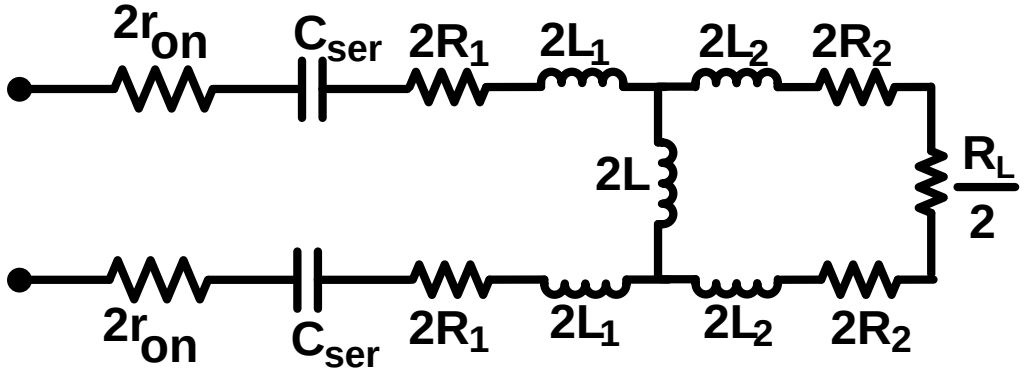
**Fig. 5-21: (a) peak power (b) -6dB back-off, equivalent circuit model.**

Based on equation (5.17), then figure 5-20, simplifies to figure 5-21(b). Figure 5-21, shows with the passives in ideal form, the linear relation mains from the peak power to -6dB power if the off PAs are tri-stated. If the PAs are off by grounding then it imposes small nonlinearity with the trade of off marginally better power. The better power is due to the fact that, the *ron*'s of the off PAs are in parallel with switch resistance and forms overall smaller resistance than PAs *ron* and so efficiency improves.

Now, if assuming a lossy and leaky transformer, then figure 5-21 looks like figure 5-22. Again, if the off PAs are tri-stated, a linear relation between the peak and -6dB back-off is maintained.




(a)

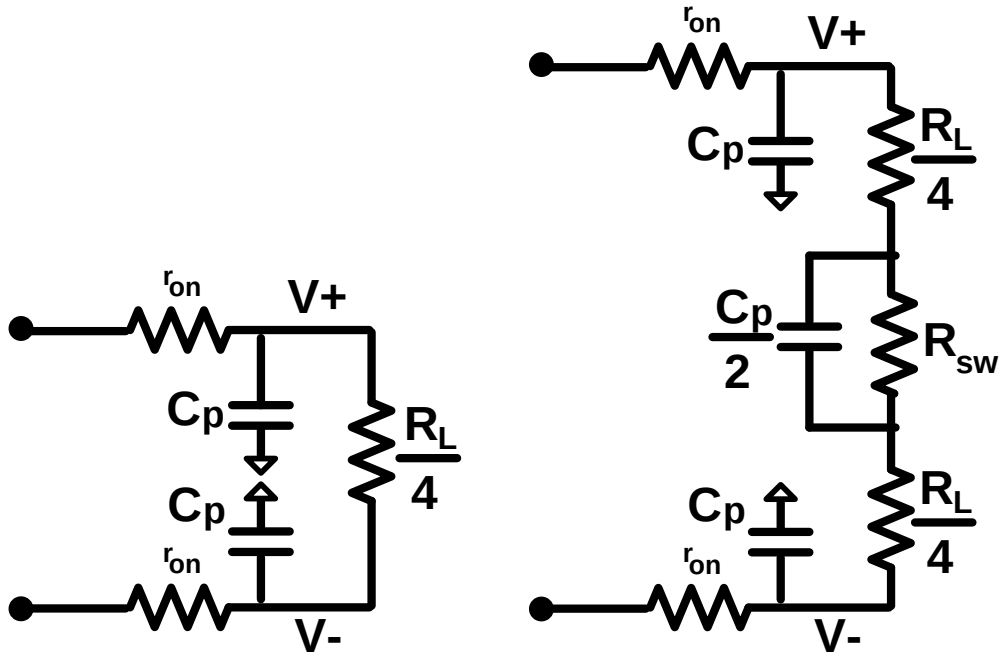



(b)

**Fig. 5-22: (a) peak power (b) -6dB back-off, equivalent circuit model with lossy and leaky transformer.**

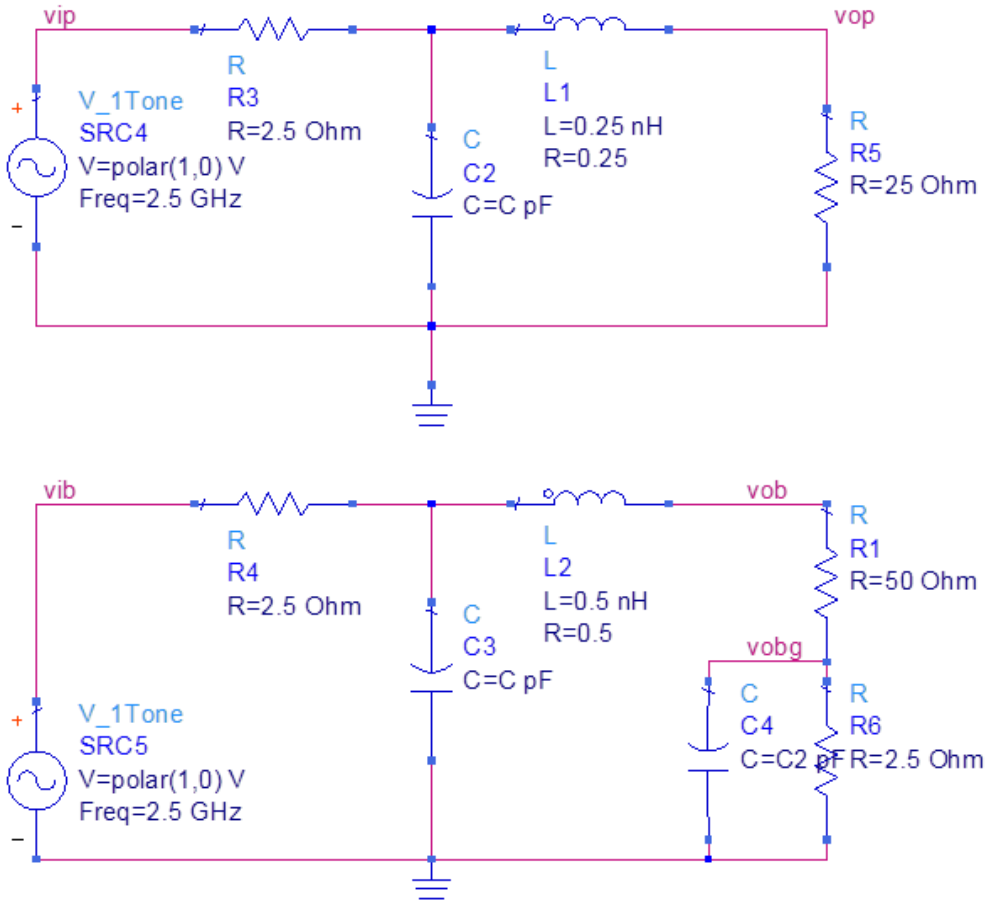
So far from the above analysis, PA shows a pretty linear relation, however; next it is shown how PA parasitic affects this linearity. Let's also assume ideal transformer with no passive

losses. Fig. 5-23, shows the equivalent circuit model of such a system at peak and -6dB back-off. The simulations results of such a model is shown in Fig. 5-24, and it shows a linear relation between the two cases if the Cp cap at the PA output and around the switch are exactly the same which is the case in DST-PA. This is a very good thing that the linearity of the system is not sensitive to the parasitic capacitances.




(a) (b)

**Fig. 5-23: (a) peak power (b) -6dB back-off, half-side equivalent circuit model with PA parasitic caps included with the ideal transformer assumption.**


vip
R
R3
R=2.5 Ohm
V_1Tone
SRC4
V=polar(1,0) V
Freq=2.5 GHz
C
C2
C=C pF
L
L1
L=0.25 nH
R=0.25
vop
R
R5
R=25 Ohm
vib
R
R4
R=2.5 Ohm
V_1Tone
SRC5
V=polar(1,0) V
Freq=2.5 GHz
C
C3
C=C pF
L
L2
L=0.5 nH
R=0.5
vob
R
R1
R=50 Ohm
vobg
C
C4
C=C2 pF
R
R6
R=2.5 Ohm

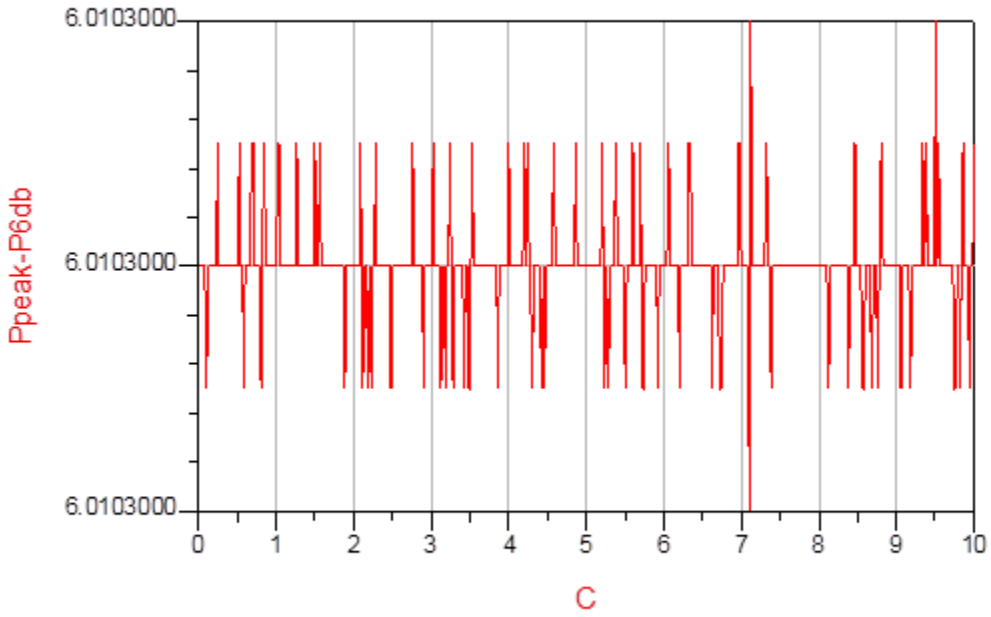



**Fig. 5-24: Simulation results of the circuit equivalent model the PA with the parasitic cap. [27]**

## 5.5 AM-AM and AM-PM Distortion

The simulation results show when the transformer is ideal, there is no non-linearity seen. Also when PA and switch is ideal, and using the transformer pi-model, there is still no nonlinearity seen. However, when PA and switch and transformer are present, the non-ideality is seen. From the previous section, it is shown that it is important to have the switch $\boldsymbol{r_{on}}$ to be twice of the PA $\boldsymbol{r_{on}}$ to have a linear relation between the peak and -6dB back-off.

However, the simulation shows that the $\boldsymbol{r_{on}}$ of the switch ($\boldsymbol{r_{sw}}$) is extremely sensitive to the DC bias at its S/D. If this DC bias at S/D is not 0.5 as would initially be thought or tried to be set by biased inverters at its source or drain, then $r_{sw}$ is actually changing with the signal swing at the terminals of the transformer. The dc voltage will in reality dynamically

change with envelope and may causes both AM-AM and memory effects. Therefore, the $r_{on}$of the switch is very sensitive and variable. As a result of the DC at its S/D, $r_{on}$ of the switch ($r_{sw}$) becomes about the same as $r_{on}$ of the PA device (which by simulation it is confirmed that it introduces close to 1dB AM-AM) which we showed also theoretically that it imposes the non-linearity if $r_{sw}$ is not equal to $2r_{on}$ of the PA.

So this is the major source of the AM-AM in this design. Also, as it is stated in [5] and shown in fig. 5-25, that non-overlapping or slow rise/fall time on the RF signal could impose some non-linearity.

As shown on figure 5-14, the DST (3 peak point) shows little AMPM distortion. The AM-PM comes from the nature of switching cap operation. DST-PA helps to reduce AM-PM effect on in the first 6dB back off region, since only half of PA is operating at this condition (switching cap). However power below -12dB back-off shows the worst AMPM, which is dominated by switching cap operation.

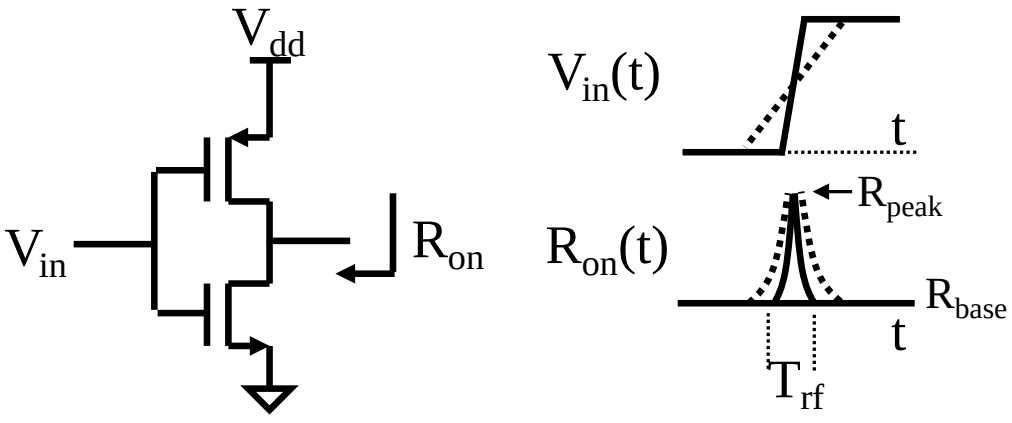
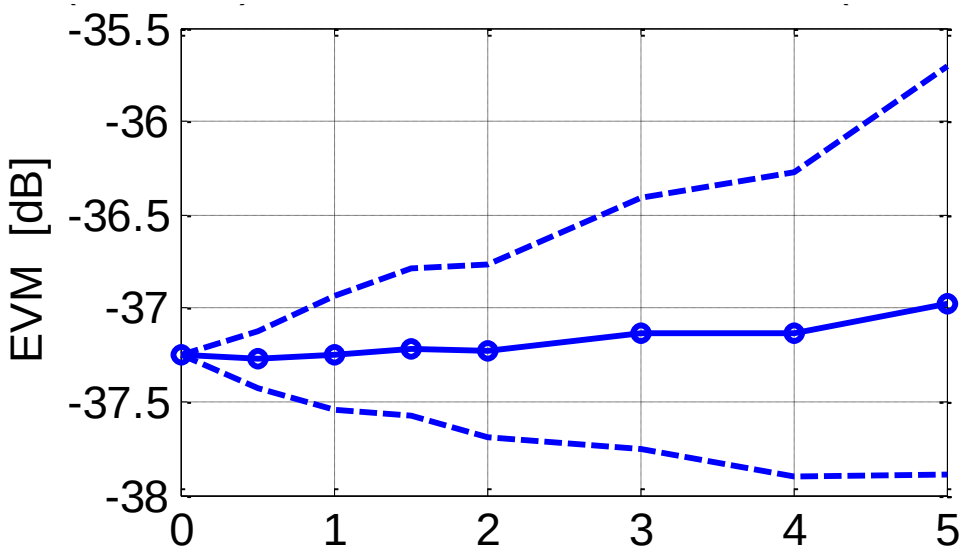



**Fig. 5-25: PA $r_{on}$ variation due to finite rise and fall time of the clock [5].**

## 5.6 Mismatch effects

The mismatch analysis is done with the assumption of 6bits in the PA but the 7bit case should have a very similar performance. The rest of the conditions are as follows: 8dB back-off packet is used. No other source of PA non-linearity is assumed. An 802.11g 64-QAM packet is been used. 0 to 5% mismatch between each amplitude step is used. 5% mismatch is already a large number even for the PA unit cell given the size of it. This mismatch will contribute to the integral non-linearity of the amplitude path of the PA. Fig. 5-26 shows the result of 100 runs of Monte-carlo simulations. The dashed lines show the boundary of the MonteCarlo results assuming a 5-95% interval; this enables to measure the PA performance under worst case of two sigma spread.

It can be seen from fig. 5-26, that EVM in the worse case still has 10dB margin (Target EVM in this case is -25dB) to the WiFi specs and ACPR shows about 12dB margin to the Wifi mask (Wifi mask is -40dBr).



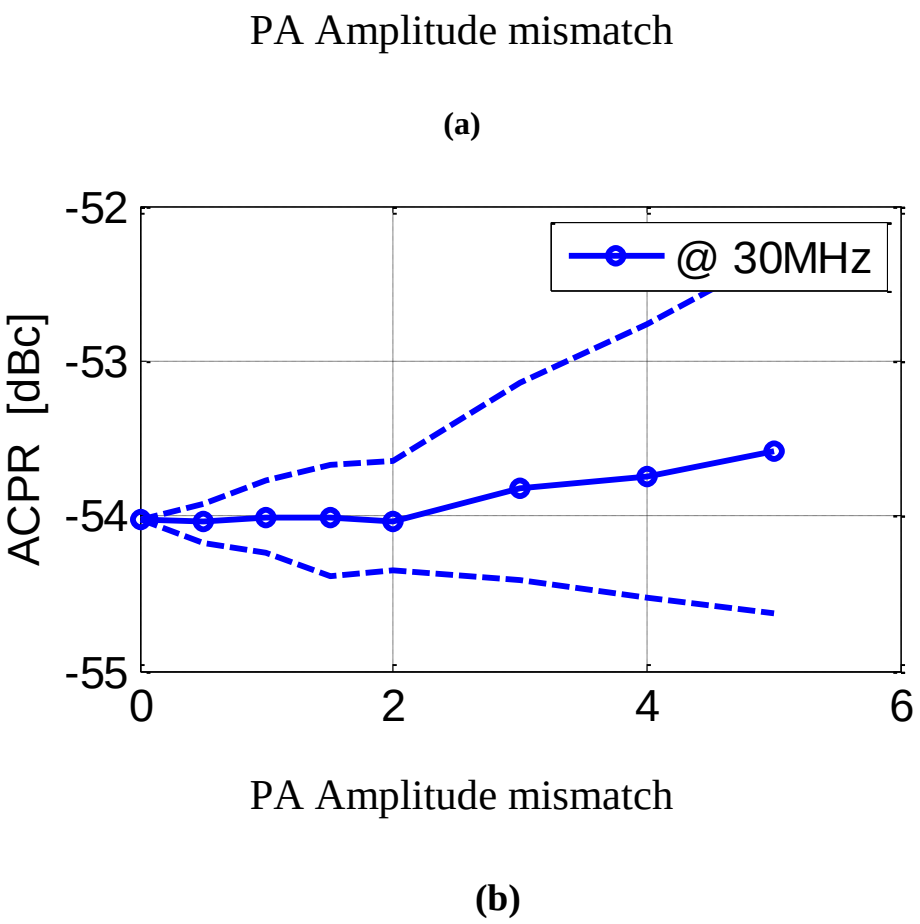


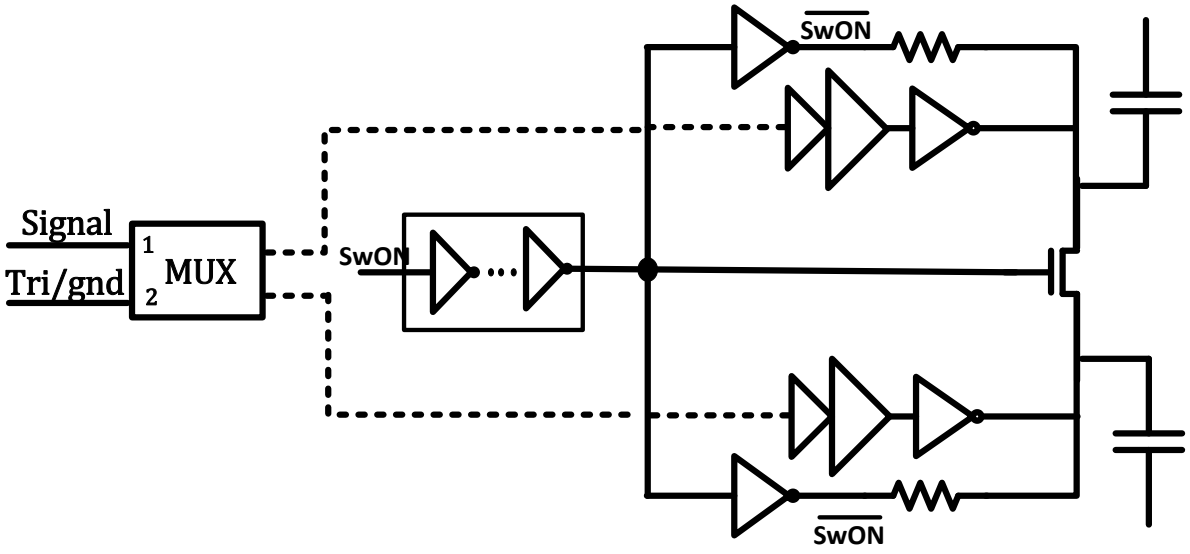

**Fig. 5-26: (a) EVM (b) ACPR, mismatch estimation of 100 runs of monte-carlo simulations. [28]**

## 5.7 Circuit Details

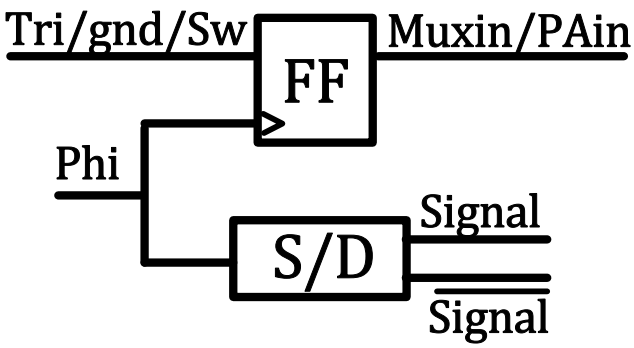
This section shows the circuit level details of DST-PA. Fig. 5-27, shows the PA unit cells and its supporting blocks. There are 32 units of the Fig. 5-27(a) in each 4 corner of the transformer, making it a total of 128 units. The biased inverters are connected through the large resistances to the source and drain of the nmos switch to ensure that the switch is biased properly for its on/off state. The caps are designed as part of the matching network to resonate out the inductive passives at the frequency of operation. The delay line block is

designed to account for the delay on the RF path so that the switch control signal arrives to the nmos gate at the same time as the PA outputs arrive at the source and drain terminals of the switch.

Fig. 5-27(b) shows the pre-PA block. The modulated phi signal is clocked at the LO rate, the generation of the complimentary phase modulated signal (inverted phi) is generated only at the end of the buffer chains that drive the PA cells. This not only saves more power but also results in more accurate differential clock edges. The single-ended to differential block (S/D) generates the differential phase modulated signals, RF and RFbar, to drive the PA. Although, the amplitude control bits are aligned once to the phase modulated signal at the top level hierarchy of the PA through the re-sampler block, for additional assurance they are re-aligned before entering the PA unit cells with flip-flops (FFs) clocked with phi signal.




**(a)**




**(b)**

**Fig. 5-27: (a) Switch and PAcell unit (b) differential clk generation and control bits alignment.**

### 5.7.1 Switch design and reliability analysis and simulations

In section, 5.5 it is shown that design of the switch is important for both linearity and efficiency of the DST-PA. Despite the proper sizing of the switch further considerations need to be taken into account for reliability since it is located at the output of the PA. At peak power there is a differential signal from 0 to vdd on the switch and so it always maintains a differential voltage on the transistor terminals is bounded to never exceed vdd. At -6dB back-off, the two middle switches are closed (transistor is in linear state) to keep the primaries in the loop. The two biased inverters make sure that the DC of the switch is well defined and it is at 0 volt when the gate of the switch sees a 1v or vdd signal, i.e. the switch is on with a low on resistance. In the ideal situation, when the switch is on, it is a virtual ground as the signals on the two sides of the switch are differential. So, from the reliability point of view, there is still no stress on the device.

At -12 dB back-off, (fig. 5-28) the lower switch sees the same situations as the closed switches would see at -6dB back-off. Let’s focus on the situation for the middle switches.

Clearly, they are not at virtual ground point anymore. In fig. 5-28, the PA can be looked at as a voltage divider, where from a V+ side to V- side there are a quarter of a voltage drop at each stage since all the switches have equal values. So for example, the voltage at node A swings between, V+ + ¼ (V+ - V-) which when V+=vdd and V-=0 attends up being a swing of A= ¾ vdd and when V+=0 and V-=vdd, then the swing at A would be -1/4vdd. As stated before, to assure a defined DC level at S/D of the switch when the switch is closed, the biased inverter defines a 0V DC at this node. Therefore, there is a 0.5V ac swing peak-peak at this node which could impose some reliability issues. However, simulation shows the DC at node A and B at -12dB back-off is more than zero than initially estimated. Further investigation into this matter, shows, even though there is a DC 0v is been set at these nodes but when the drain signal goes negative momentarily due to the leakage current from the nmos of the PA tri-stated devices, from ground to the drain node which charges up the DC level of this node to about 200mv when it settles. This DC offset, helps to alleviate the stress on the device to only 50mv to 100mv worse case above vdd. This should not be of a concern since, this behavior happens at -12dB back-off which is of very small duration in OFDM packets. Also, this is an AC stress and not DC and so its effective duration and impact on lifetime is much smaller.

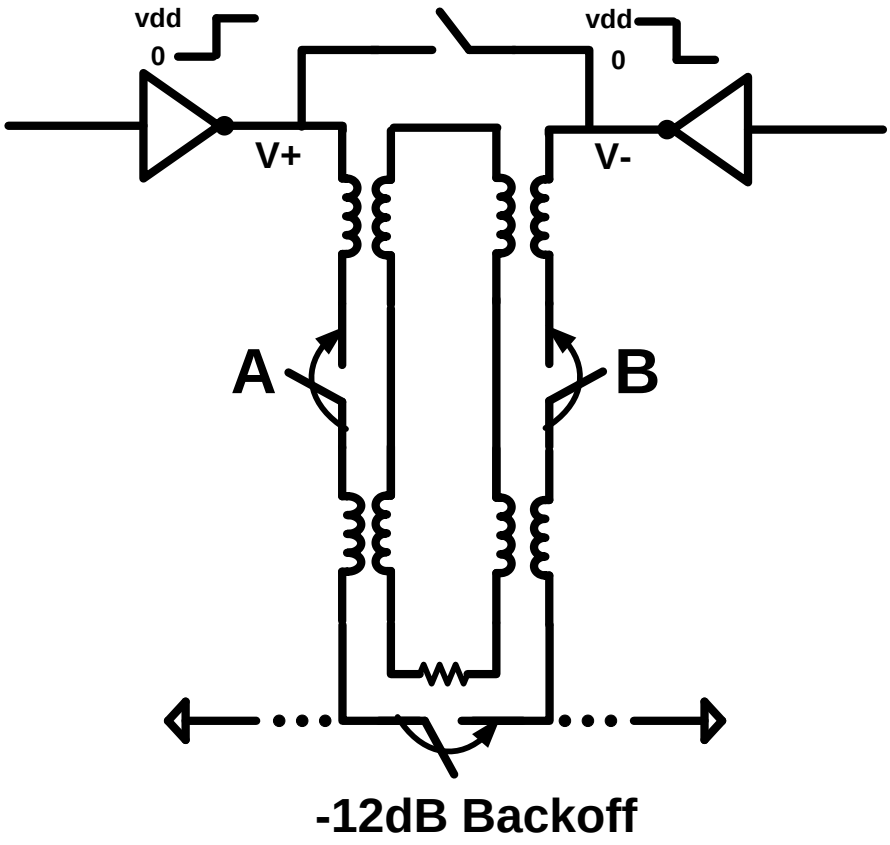



**Fig. 5-28: shows the virtual ground at -12 dB back-off.**

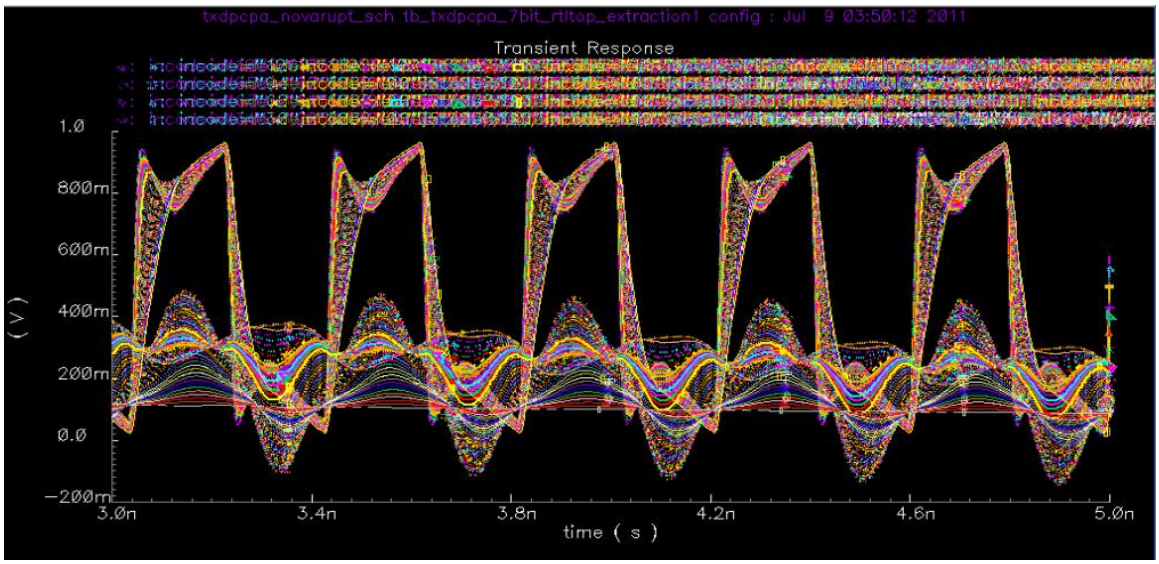



**Fig. 5-29: transient power sweep while monitoring the S/D of the switch.**

### 5.7.2 Transformer model

The transformer modeling is done with ADS momentum. A pi-model is used for approximating the substrate resistance and capacitance as well as the coupling cap. The model is shown in Fig. 5-30. The transformer sees different parasitic caps and slightly different area in the probed-PA version vs. the packaged version, there are two slightly different designs are considered for each version. The careful analysis shows that the series cap in the unit PA cells should stay at the same value while the output matching and transformer values change from one version to the other.

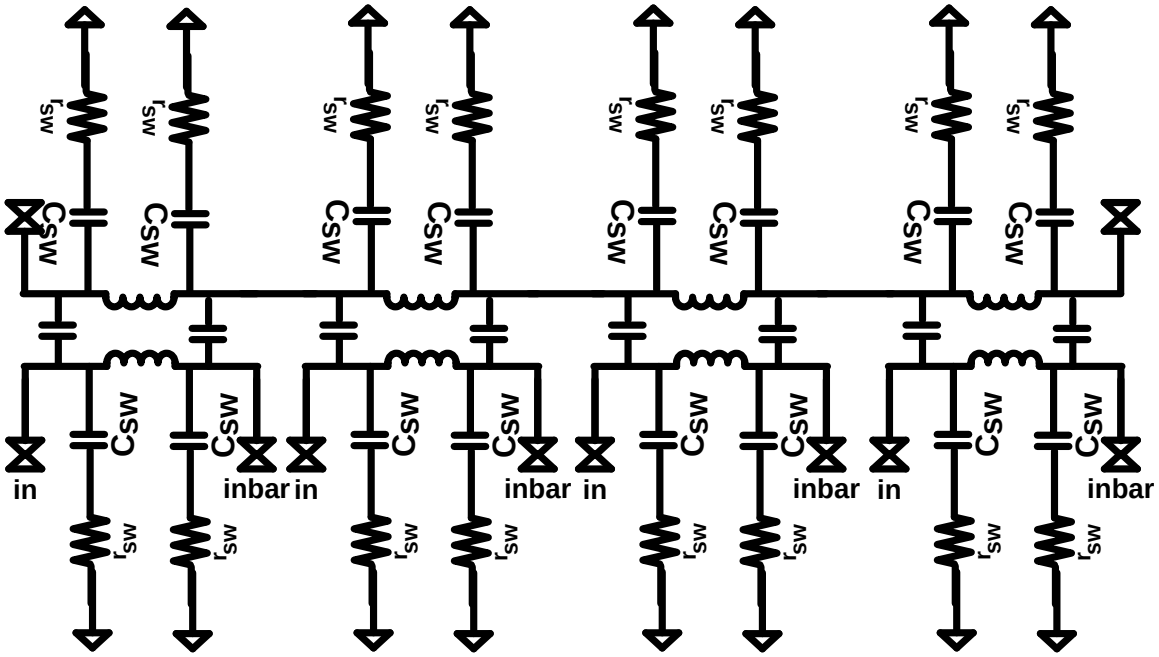



**Fig. 5-30: Transformer pi-model.**

## 5.8 Floor Plan

Fig. 5-31, shows the floor plan of the DST-PA. PA# is defined as on/off sequence. Note that unit PAs in PA1/3 and PA2/4 are alternatively turned off as power goes lower. The amplitude bits from the RTL block are first synchronized by the re-sampler block to the phi signal before entering the PA at the top-level of hierarchy. There are 218 signals that need to be routed quite symmetrically. This is important to ensure a minimal skew when they arrive at the PA unit cells. Therefore, a digital method for clock distribution, called an H-tree, is adopted for this purpose, as shown in fig. 5-32.

The total number of signals to be routed throughout the floor plan:

((2halfpa-bits+7unitpa-bits)x3ctrls/bit)x8sections =216

216 amplitude control signals + 2 RF pahse modulation signals = 218 signals

Originally the design of DST-PA was done with a 6 bit PAs. However, simulation results of OFDM inputs showed that the margin to the WiFi mask was only 5dB. This is not considered adequate margin to account for issues in the manufacturing/testing stages. Therefore, a pseudo-7bit design based on the existing 6bit thermometric was developed. This is done by having 6bit thermometric array with one PA units cells in each section further split into half-unit cells. Specifically, the 8x block in fig. 5-31 consists of 8 PAcells when it is a 6bit design. To match the 7bit design, one of the PAunits is split into two-half PA cells. Each half-PA is now driven by its own independent mux. All the other unit cells share a mux for the half cells. Effectively each 8x block of fig. 5-31 consists of 16 half PAcells.

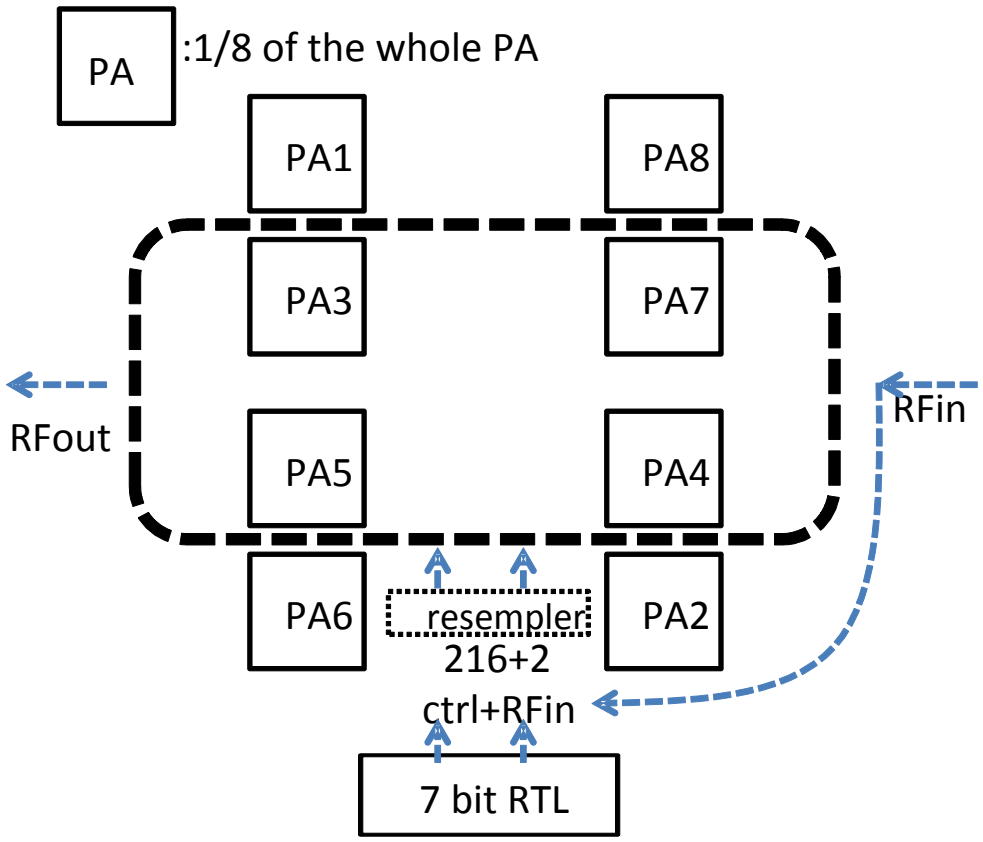



**Fig. 5-31: probed-pa floor plan.**

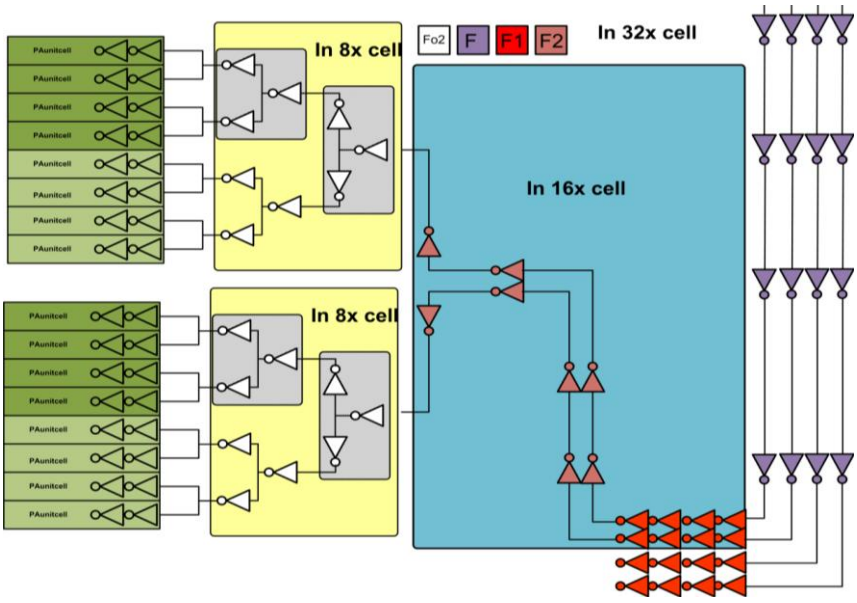
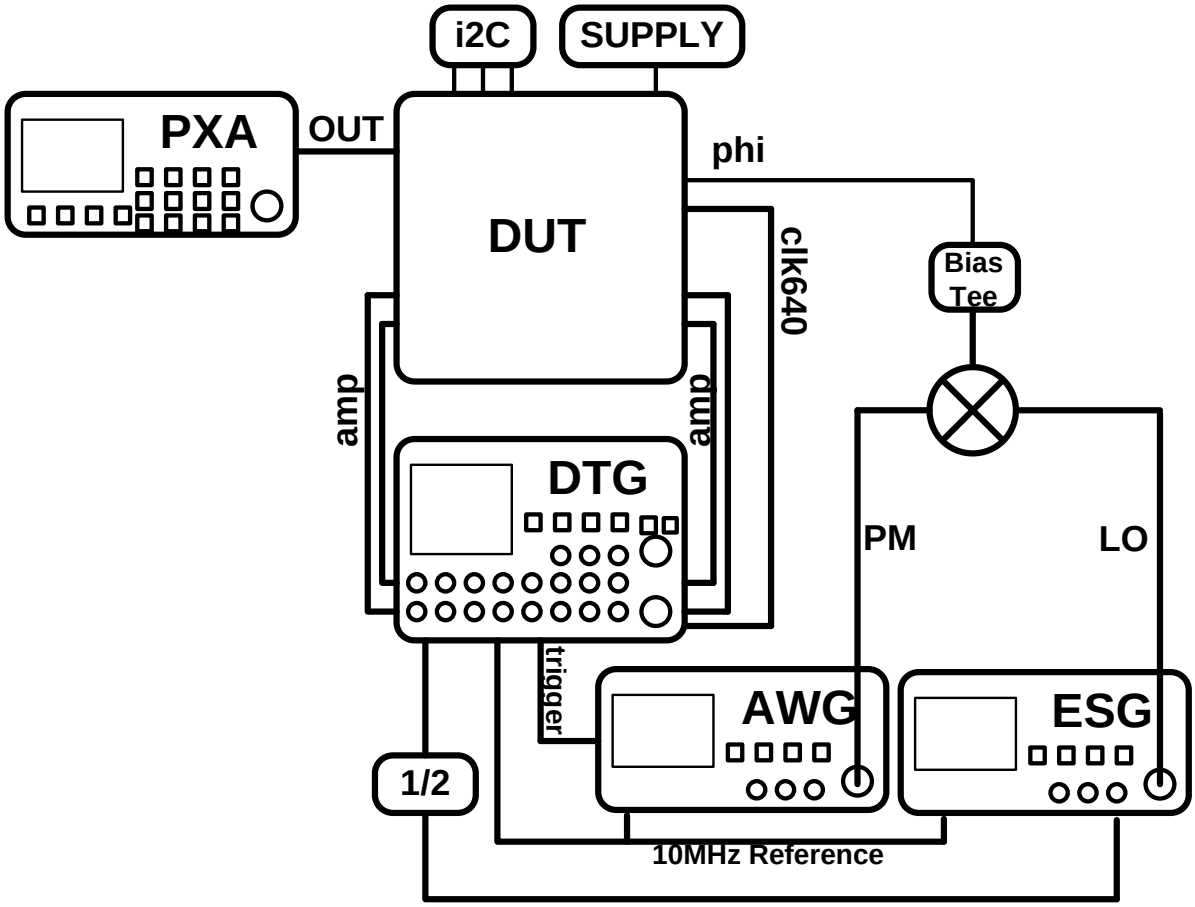


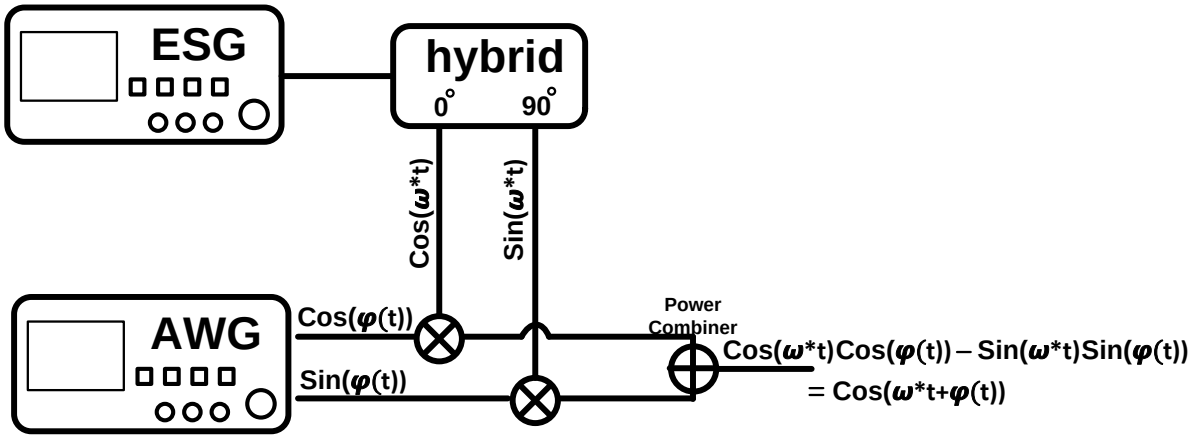

**Fig. 5-32: H-tree signal routing for equal rise or fall time arrival.**

## 5.9 Measurement Set up

Figure 5-33, shows the experiment set up for the DST-PA characterizations. The PA is tested with a wideband Arbitrary Waveform Generator (AWG) to generate the phase modulated signal. The quadrature outputs of the AWG are up-converted to RF using a direct conversion mixer implemented with discrete components. The 2.5Ghz LO signal is generated with a signal generator (VSG or ESG). In addition to a 10MHz reference to synchronize ESG, DTG and AWG, a high frequency signal (LO/2) is used from ESG to DTG to further guarantee synchronous triggering. A bias-T is used for proper biasing of on chip interface devices. The single-ended output of the PA is down-converted and analyzed by vector signal analyzer personality on the PXA. The amplitude modulation signals are oversampled to 640MHz to prevent aliasing and suppress the spectral images below the mask. Due to the limited number of high-speed probe pads that can be accommodated, the 7 amplitude bits were serialized to 4 channels at 2x the rate. The later is because a 7bit polar implementation requires a 7bit modulated amplitude signals from the Digital Timing Generator (DTG). With serialization only 4 amplitude signals and one synchronization signal from the DTG are required for the amplitude inputs. Fig. 5-34, shows the top level signals inside Device Under Test (DUT). The RTL block incorporates a synthesized SRAM Look Up Table (LUT) that gives us the freedom to implement different switching schemes on DST-PA. The re-sampler synchronizes the amplitude signals from the RTL block to the phase modulated (phi) signal.




**(a)**




**(b)**

**Fig. 5-33: (a) Measurement Set up. (b) phase modulation generation details.**

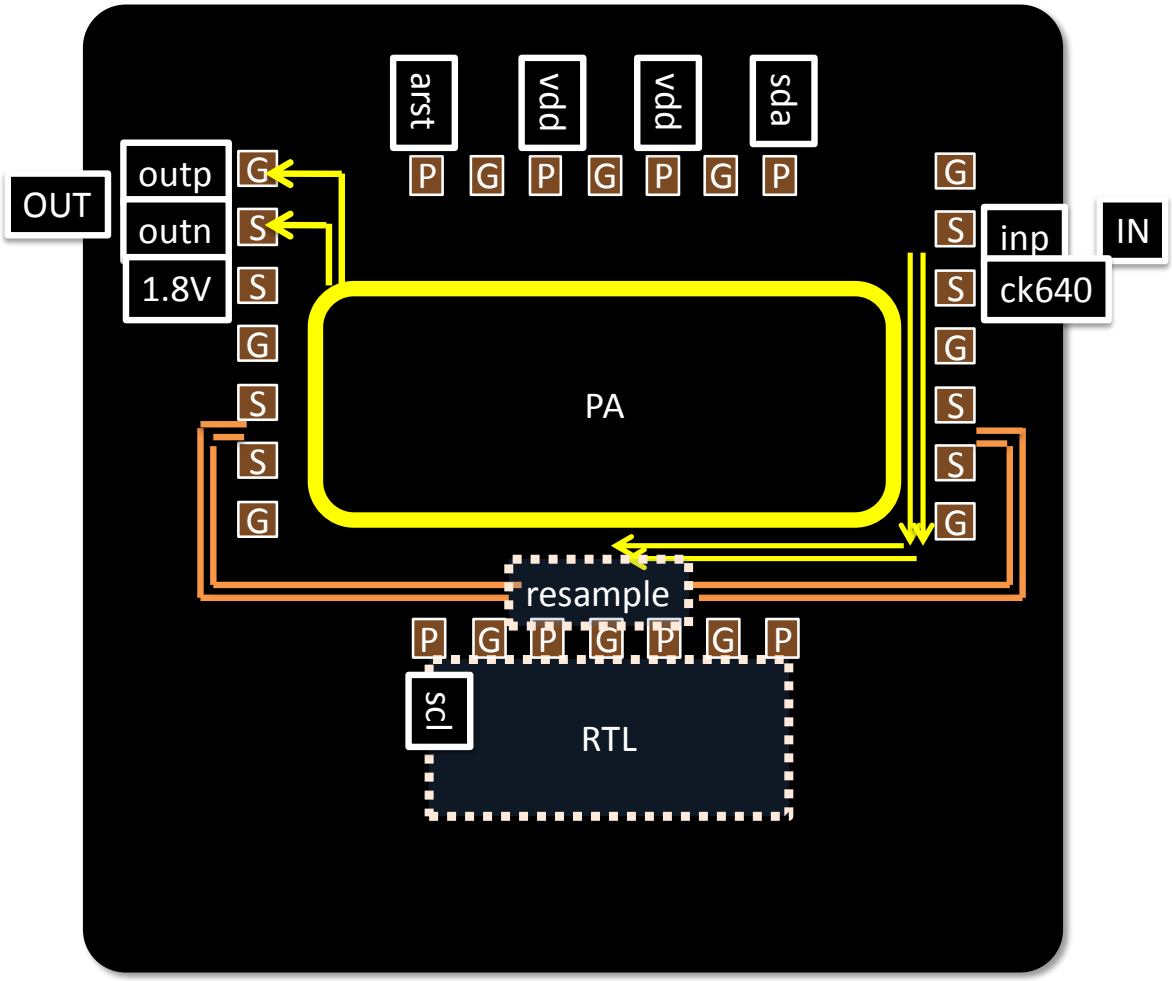



**Fig. 5-34: Stand-alone probed location and floor plan.**

The complete transmitter consisting of the integrated PA with the phase-modulator, is implemented in a SoC flip-chip package. To re-use the same package designed in [5] for this design, careful top-level routing is considered for this design and particularly for the stand-alone version. This is to avoid further re-layout and verification of the main PA core. In the integrated PA, flip-chip bumps can interfere with the transformer and degrade RF performance. To minimize the parasitic introduced by the package, the transformer is routed in the open area between bumps. 2.5-D EM simulation is done as described in [5] to estimate

transformer performance in flip-chip package environment. The transformer loss is simulated to be -1.3dB between 2.4–2.5 GHz.

Wide DC supply routing is used at the top level to handle DC current and minimize IR drop. To accommodate the package bump pattern for the supply routing, a special DC probed is designed and ordered for the probed version of DST-PA as it is shown in Fig. 5-35. Decoupling capacitors are placed underneath of the supply network to minimize high frequency supply variations. All the capacitors used in this design are metal finger structures. A 64-QAM, 20MHz bandwidth 64-pt FFT size OFDM, WiFi signal is used to measure the dynamic performance of this prototype. The OFDM signals are applied with pre-distortion. The die photograph is shown in fig. 5-36. It main PA core occupies an area of 1.2x0.8$mm^2$.

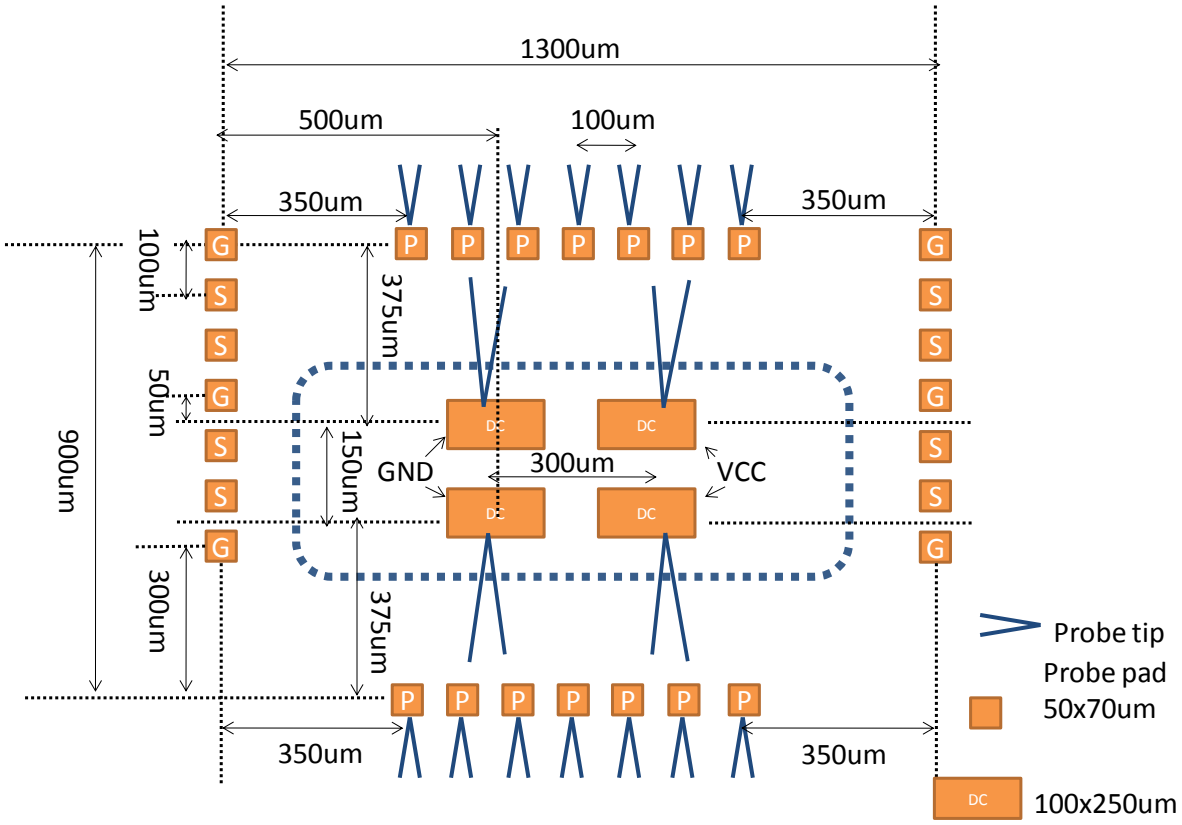



**Fig. 5-35: Stand-alone special DC probes.**

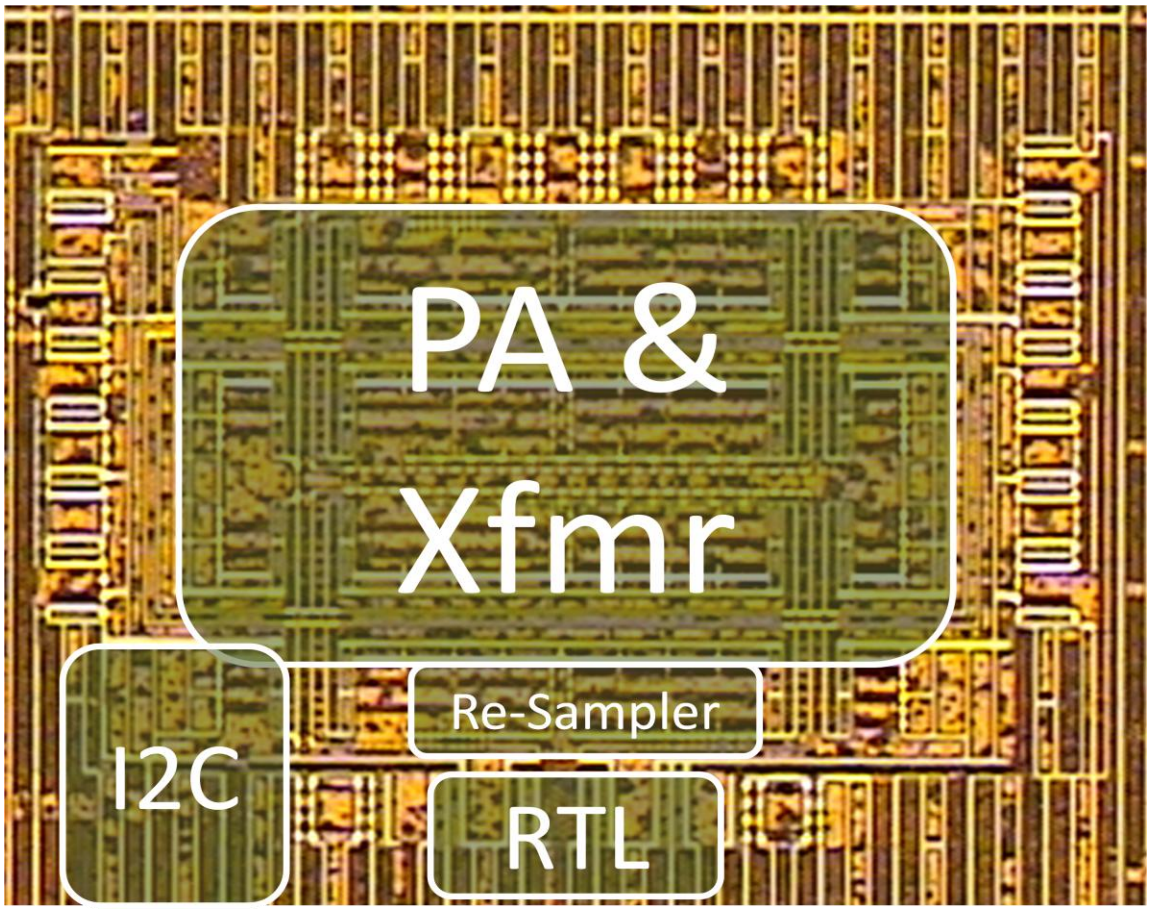



**Fig. 5-36: The die photograph.**

## 5.10 Results

This design is fully verified at various stages, from the schematic all the way to the post extraction simulations. The extracted simulations of the PA_top level are extremely slow. In order to overcome this problem and fully verify the design the following verification procedure is considered. All the top level routing up to the PA cells are extracted and simulated with the schematic view of the PA unit cells. These have been verified for proper rise and fall time of lower than 30ps and approximate equal delay with respect to the falling

edge of the phi signal. This is to account for enough set up and hold time for the FFs inside the PA unit cells. After all these been verified, a verilog view of the buffer chain replaces the schematic to speed up the verification simulations. Since the PA cells contribute to the nonlinearity but takes quite long time for the power sweep and even more for OFDM simulation, the parasitic caps have been added to the schematic view of the PA cells with their values are taken from the extraction log files. Figure 5-37 and 5-38, show the CW simulations on the extracted caps view of PA unit cells in probed PA and integrated PA, respectively. The buffers are ideal to speed up the simulation, since they do not contribute to the nonlinearity of the system as well as minor power consumption relative to the PA cells for static simulation. Table 5-2, shows the tabulated results of figures 5-37 and 5-38 for three steps of power control.

| | Pout (dBm) | PAE | Phase(deg.) |
|---|---|---|---|
| **Probed pa with extracted caps added in the PA cell. No buffers or supply drop.** | **26.2** | **47.3%** | **42.5** |
| | **21.3** | **44%** | **40.9** |
| | **15.7** | **29.9%** | **36.1** |
| | | | |
| **Integrated pa with extracted caps added in the PA cell. No buffers or supply drop.** | **26.4** | **44%** | **48.3** |
| | **21.8** | **43.4%** | **48.5** |
| | **16.4** | **32%** | **45.2** |

**Table 5-2: tabulated results of Figures 5-37 and 5-38 for three steps of power control.**

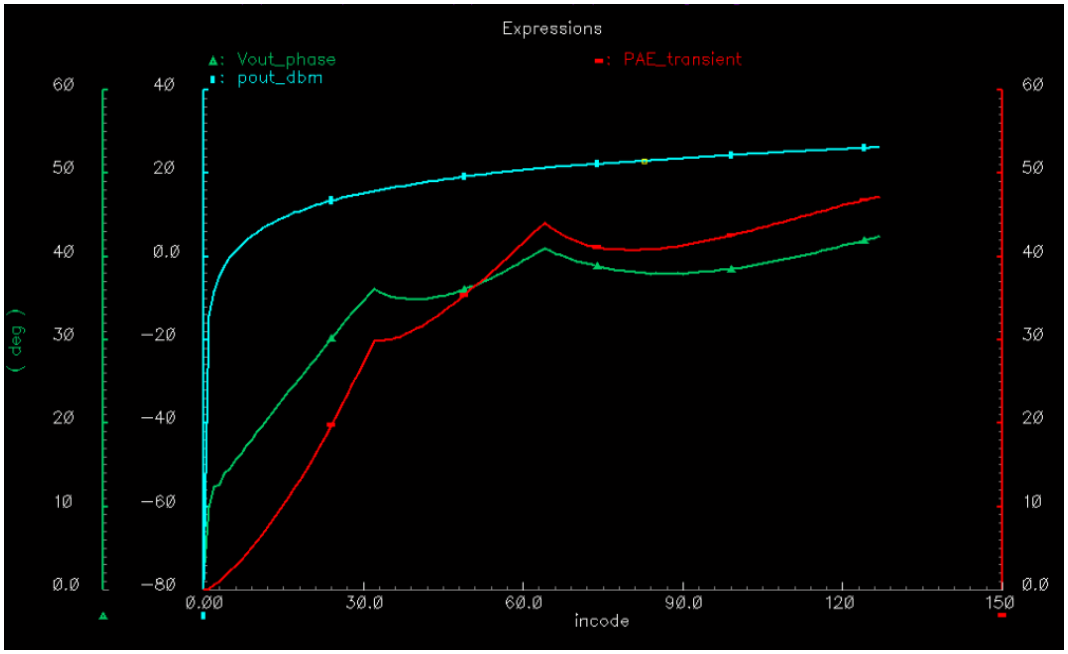



**Fig. 5-37: Constant Wave (CW) power sweep for output power, phase and PAE for the probed PA.**

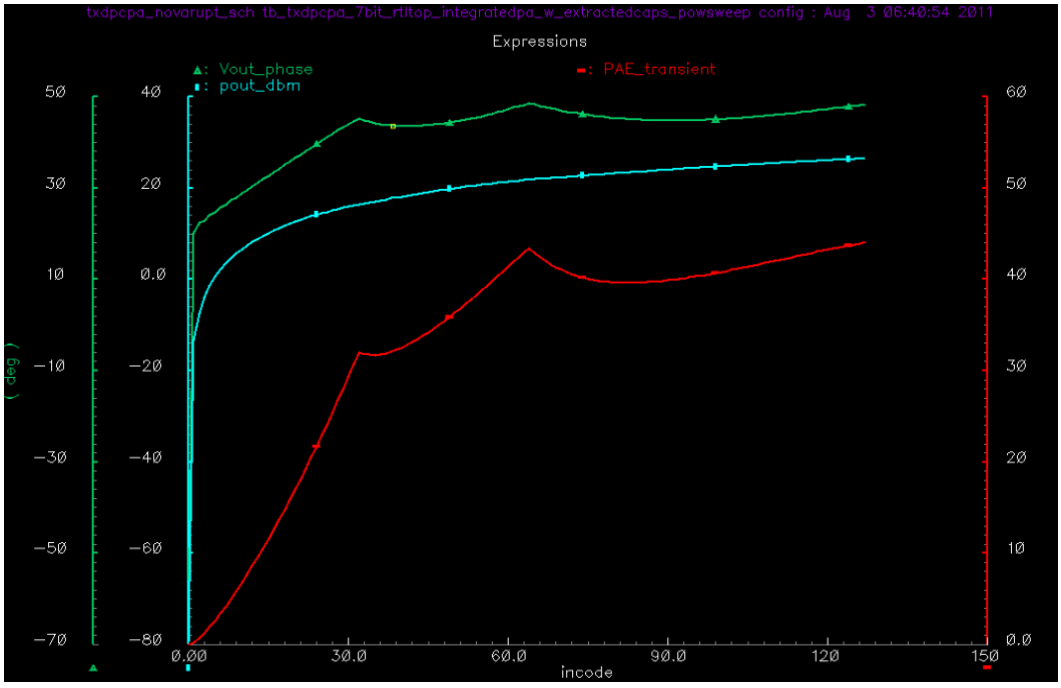



**Fig. 5-38: Constant Wave (CW) power sweep for output power, phase and PAE for the integrated PA.**

Figure 5-39, shows OFDM simulation with the pre-distortion package of the probed (red) and integrated (blue) PA, respectively. It is shown a 10dB margin to the Wifi mask with a PAE of 38% and 37% respectively. To capture the EVM, the OFDM simulation had to be run for the full 48us package length. This is a lengthy transient simulation. Therefore, for the EVM/mask simulation an all-schematic view of the PA core is simulated. The result shows a -26.5dB EVM meets the Wifi specification and it is shown in Figure 5-40.

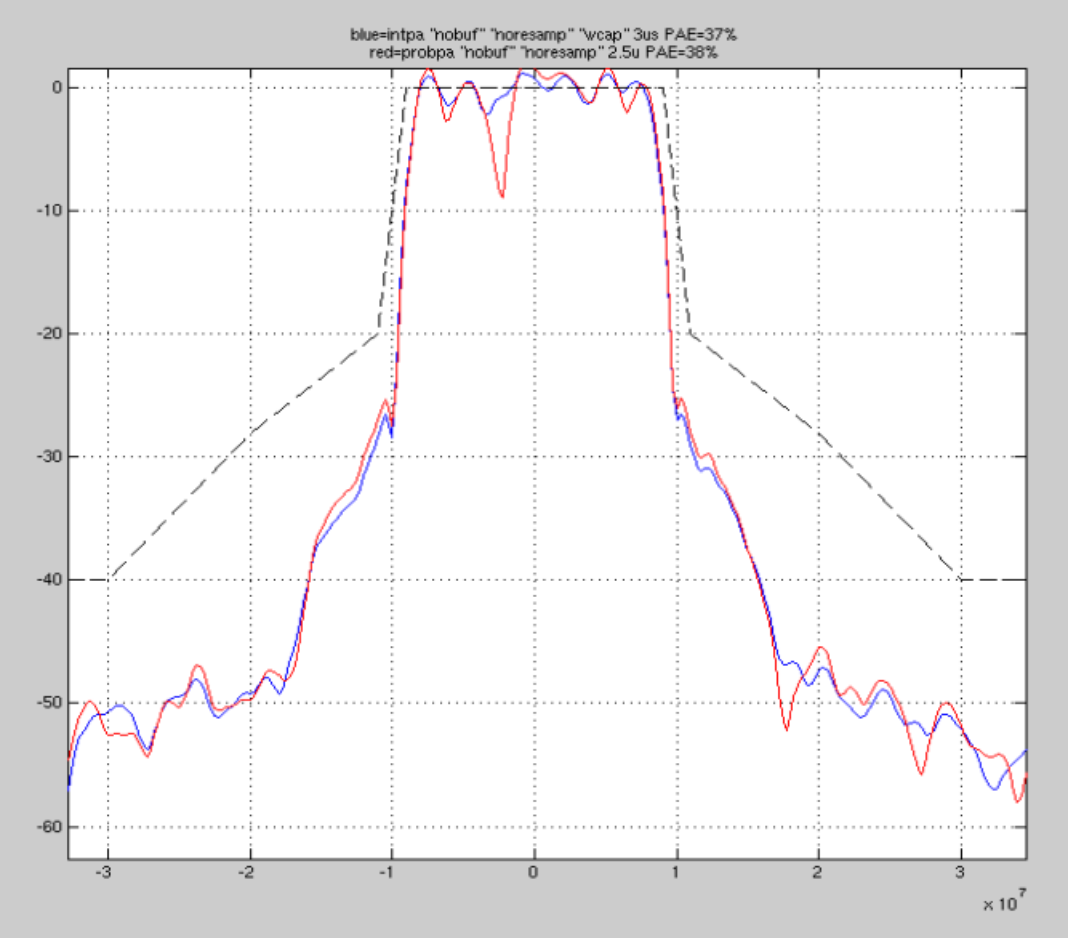



**Fig. 5-39: The OFDM post-extraction simulation (included the parasitic caps in the PA cells) Blue= integratedpa "nobuf" "noresamp" "w parasitic cap" until 3us PAE=37%**
**Red= probedpa "nobuf" "noresamp" "w parasitic cap" until 2.5us PAE=38%**

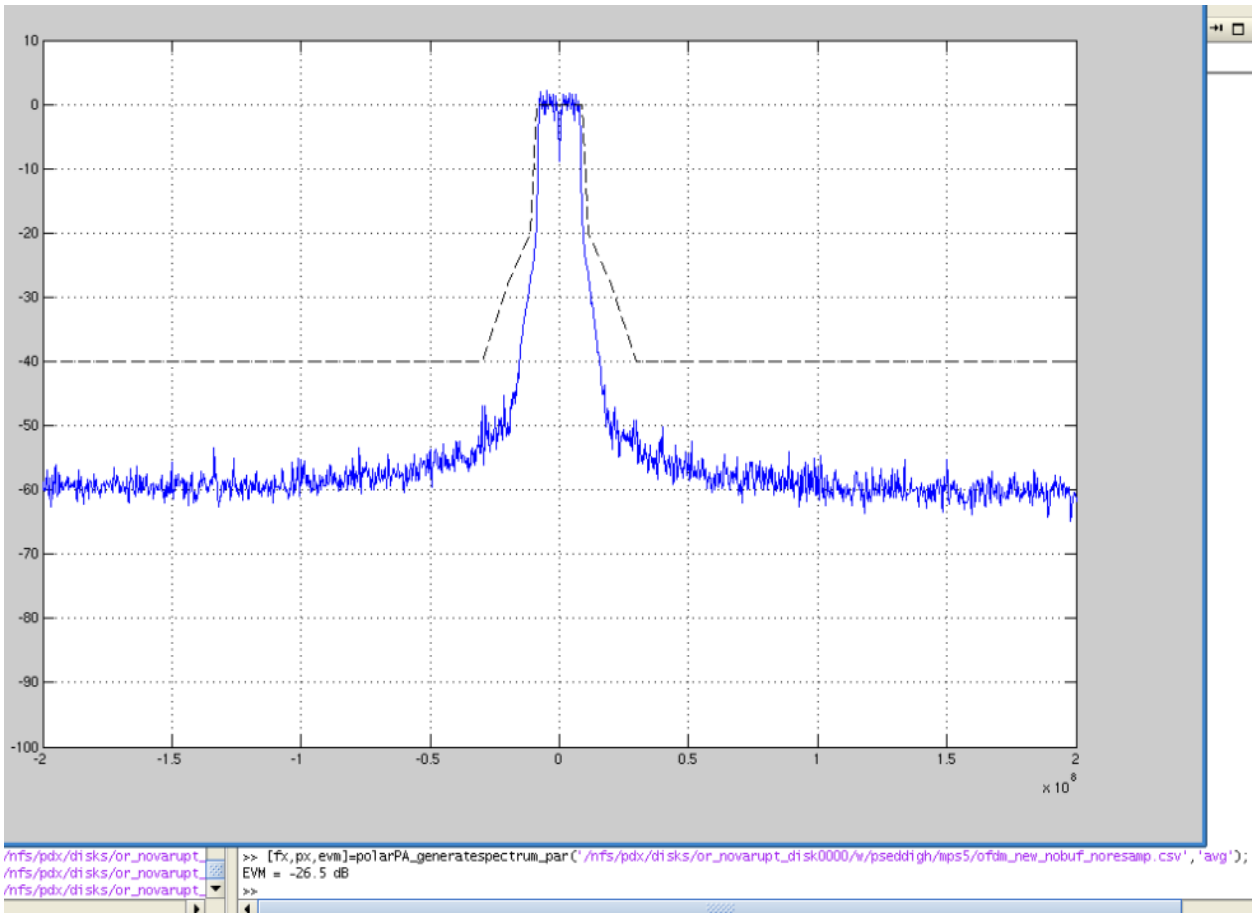



**Fig. 5-40: The OFDM simulation to capture the EVM. It is all schematic view of the PA Core with PAE of 40.8% and EVM of -26.5dB.**

# 6 Conclusions

This dissertation presented a novel transformer combining technique which is digital friendly and digitally scalable called DST-PA. This promises towards a low power integrated CMOS PA. It demonstrates a peak output power of about 26 dBm with 39% peak PAE. The average 64-QAM WiFi OFDM output is 21 dBm with Average efficiency of 37%. It has about a 10dB margin to the mask with EVM is about -26.5dB. With the trends toward a single all digital multi-radio solutions on CMOS chip, the dissertation also shows two techniques for spectral improvement in transmitters: close-in harmonics suppression (HRPA) and reductions in out of band emissions.

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