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Enhanced Optical Modulation in Integrated Silicon Waveguides for the  
Near-Infrared

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A thesis

submitted in partial fulfillment of the  
requirements for the degree of  
Master Of Science In Electrical Engineering

University of Washington

Year 2012 of graduation

Committee

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Electrical Engineering

University of Washington

**Abstract**

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Optics in the near-infrared has emerged as a key technology in the past several decades. The primary application has been the rapidly expanding demand for high-bandwidth communications. A challenge in adopting this technology has been the relative expense of optical components, which are typically fabricated in exotic material systems. The possibility of utilizing the relatively low-cost silicon material platform for integrated optics is therefore extremely attractive. However, several key challenges must first be addressed. One of the key components in optical systems are high-bandwidth optical modulators. For modulators that have been demonstrated in silicon so far, the performance is significantly inferior to the conventional material systems. Here, I present

two approaches to improve EO modulation in silicon. One of them is by introducing some highly nonlinear organic material to the silicon device. The other approach is a novel reverse-biased PN junction geometry. While reverse-biased PN junction geometries have been used for modulation previously, the new proposed design will achieve substantial improvements over the state of the art. These two approaches both address the challenge of modulation in silicon, and are important steps towards making silicon a more attractive platform for optical system.

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# **Chapter 1 . Introduction**

## **1.1 Photonics Technology**

One of the defining needs of modern society is for an increasing amount of communications bandwidth, driven by the increasing needs of rich media, high-resolution video, video games, as well as high-performance computing for defense and commercial applications. Optoelectronic technology is regarded as a promising solution to meet these needs, because compared with electrical cables, optical fibers provide dramatically improved total bandwidth and reduced loss. This is particularly true when techniques like wavelength-division multiplexing are included. With such techniques, it is possible to transmit terabits of data through a single optical fiber [1] . Today, for long distance telecom applications, the optical solution has been proven to be a major success[1] . Historically optics has been an expensive solution, and has thus dominated longer-distance links first. But it has become widely recognized that even very short data connections are limiting the performance of computer systems [2] and this will continue to become an increasingly severe problem over time. As multi-core architecture is becoming increasingly popular, the communication bandwidth needed between core and core, core and memory is hitting the bottleneck [3] . The necessity of implementing a chip scale short reach optical data communication solution is beginning to be recognized in the community [4]

## **1.2 Current Photonics Material Systems**

For a long time, III-V semiconductors such as InP, and electro-optical materials such as Lithium Niobate ( $\text{LiNbO}_3$ ) were widely considered to be the most viable material systems for optics. Even today, they form the basis for most of the photonics components in use.  $\text{LiNbO}_3$  is an outstanding material for doing electro-optical modulation. The state of the art technology for EO modulator for data communication applications is based on  $\text{LiNbO}_3$ . The  $\text{LiNbO}_3$  modulators take advantage of Pockels [5] (the linear electro-optic) effect and provide high speed and relatively efficient modulation. Commercial products operating at 40GHz, 5V  $V\pi$ , and 4dB optical insertion loss are available[6]. III-V compound semiconductors like InP benefit from a direct band structure and proper bandgap. This makes them ideal platforms to integrate light generation, modulation and detection components working in the range of 1.3-1.6 $\mu\text{m}$ , which is preferred for data communication. On this platform, commercial modulators operating at 30GHz, 3V  $V\pi$ , and 5.8dB optical insertion loss have also been achieved[7]. Moreover, practical systems have also been demonstrated. InP chip maker Infinera launched 40 channel WDM transmitter with 40 Gb/s/channel, and an aggregate bandwidth of 1.6T/s[1].

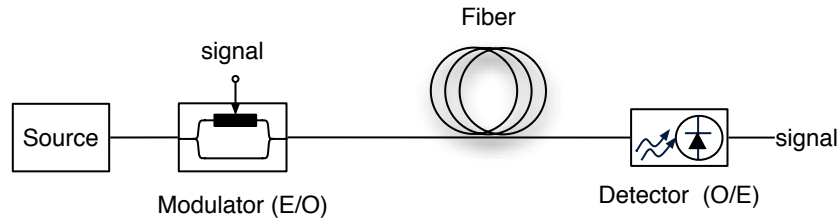
## **1.3 Benefits and challenges of Si photonics**

Although the device performance is good on conventional platforms like  $\text{LiNbO}_3$ , GaAs and InP, a big limitation is the large cost per component due to the expensive substrate and large device footprints in the case of Lithium Niobate. This has prompted a search for an alternative material platform that is suitable for low-cost high-density integration and mass production. Silicon has recently emerged as an attractive candidate. Silicon has excellent optical property at data communication regime (1.3-1.6 $\mu\text{m}$ ). The bandgap of

silicon (1.12eV) is such that it's transparent in the near IR wavelength range. The high refractive of silicon ( $n=3.48$ ) makes it possible to guide light over very tight bends, which is necessary for high density integration of photonic devices. More importantly, by utilizing Si CMOS manufacturing technology, which has been well developed in the past half century, silicon photonics is believed to have the potential of delivering low-cost, high reliable photonics systems, and the possibility of seamless integration with electronics. During the past decade, great progress has been made in this area. Low loss waveguides[8] , high speed modulators [9] and detectors [10] have been demonstrated, and performance across a wide range of devices has improved rapidly. Commercialization of this technology has also occurred. For example, Luxtera, the industry leading in silicon photonics has launched a 40Gb/s active optical cable, which comprises a 4x10Gb/s 0.13um CMOS integrated silicon transceiver chip and a co-packed commercial VCSEL.

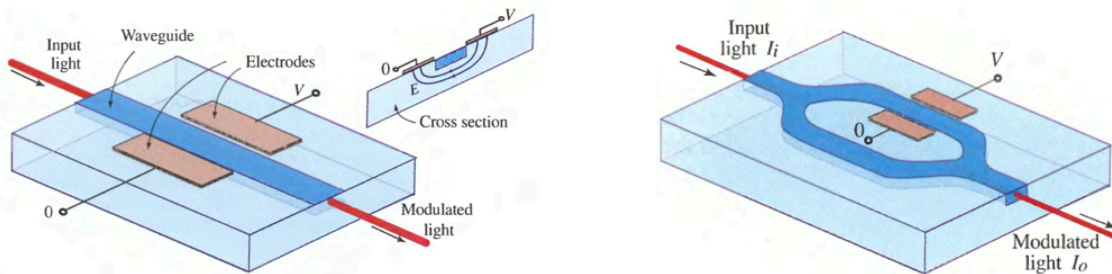
## **1.4 Modulators**

The simplest optical interconnect comprises a light source, an electro-optical (EO) modulator, a photodetector and the optical fiber or waveguide that connects them. The modulator convert the input electrical signal into optical signal by modulate the light emitted from the light source. The optical signal is then transmitted to the photodetector through the optical fiber, and turned back to electrical signal. As one can see, the EO modulator plays a key roll in the optical interconnects—it determines the data rate and signal quality of the transmitted optical signal.



**Fig 1.1: a simple optical interconnect**

EO modulators are usually built with electro-optic materials like Lithium Niobate. These materials change their refractive index when an electric field is applied. Taking advantage of this property, we can form an EO phase modulator simply by putting an optical waveguide between a pair of electrodes. When a voltage is applied on the electrode, the refractive index of the waveguide will be modulated by the electric field, thus light propagates through the waveguide will experience a phase shift modulated by the input voltage. Once phase modulation is achieved, a Mach-Zehnder interferometer with a phase modulator in one arm can be readily constructed to turn the phase modulation into intensity modulation.



**Fig 1.2: phase modulator and intensity modulator [5]**

The performance of an optical modulator is characterized by a number of metrics.

- **Bandwidth:** the maximum RF frequency which can be efficiently converted into an optical signal, which determines the ultimate bit rate the modulator can support; higher is better.

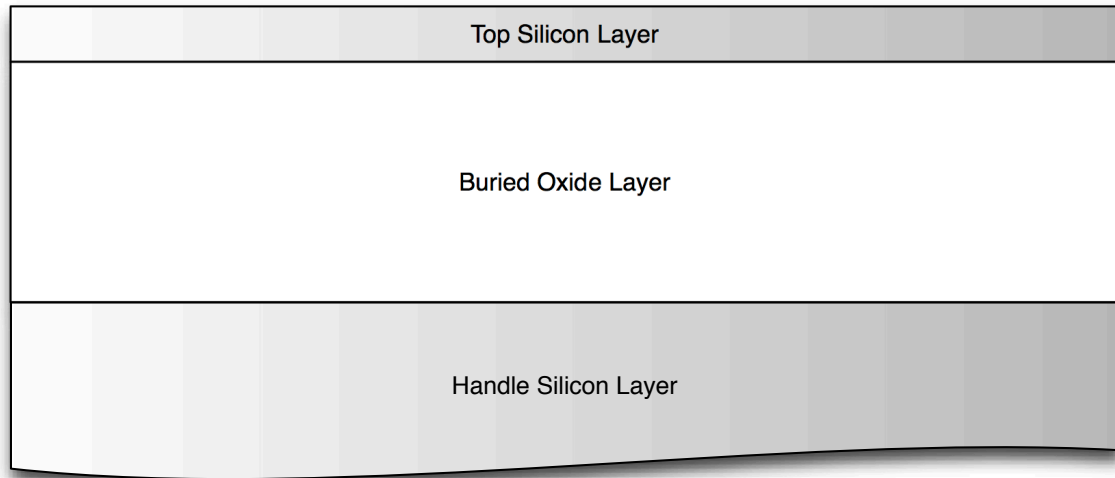
- $V\pi L$ : the product of the voltage and device length needed to obtain a full pi phase shift; smaller is better.
- Power efficiency: the energy needed to produce a bit of data; smaller is better.
- Driving voltage: The input voltage needed to obtain certain extinction ratio between the 'on' and 'off' state; smaller is better
- Footprint: the area of the device, usually smaller is better.
- Optical Insertion loss: the amount of light lost during a trip through the modulator; less light loss is preferable

In the rest of the thesis, I'm going to focus on approaches to improve optical modulators in silicon, i.e. maximizing the bandwidth while minimizing other metrics like  $V\pi L$ , driving voltage and power efficiency. This is very challenging work because in many cases, there involves trade-offs between the metrics. For instance, by shortening the length of the device, one can reduce its capacitance, thus increase its bandwidth. However, shortening the device length implies a larger driving voltage, which is undesirable. In is paper, I'm going to show some approaches that improves one or more metrics without scarifying the others.

## **Chapter 2 Integrated Silicon Optics and Design Tools**

### **2.1 Basics of the silicon platform**

Almost all integrated optics in silicon is constructed in silicon-on-insulator (SOI), as opposed to the bulk silicon that is most commonly used in transistor fabrication. The SOI wafer consists of a top silicon layer, a buried oxide layer and silicon handle layer. The top silicon layer is used to guide light; its thickness is usually a few hundred nanometers. The buried oxide layer is typically 2~3 micrometer thick. It acts as a low index cladding, preventing the light guided in the top silicon layer to leak into the silicon handle layer. The silicon handle layer is usually more than 500 $\mu$ m thick, which provides mechanical support to the upper structures. Sometimes an oxide passivation layer is introduced above the top silicon. Designing and fabricating photonics devices on the SOI platform is quite challenging and very different from the fiber based optoelectronics devices that are presently used in industry. But the explosion of interest in silicon photonics over the past decade has seen a number of significant advances. Components like low loss waveguides [8] , high efficiency grating couplers [11] , high-speed modulators [9] and detectors [10] have been successfully demonstrated on the SOI platform. In the rest of this chapter, I'll introduce the some challenges of integrated silicon photonics and the commonly used tools to help address these challenges.



**Fig 2.1 Configuration of SOI wafer**

## **2.2 Challenges of Integrated Optics**

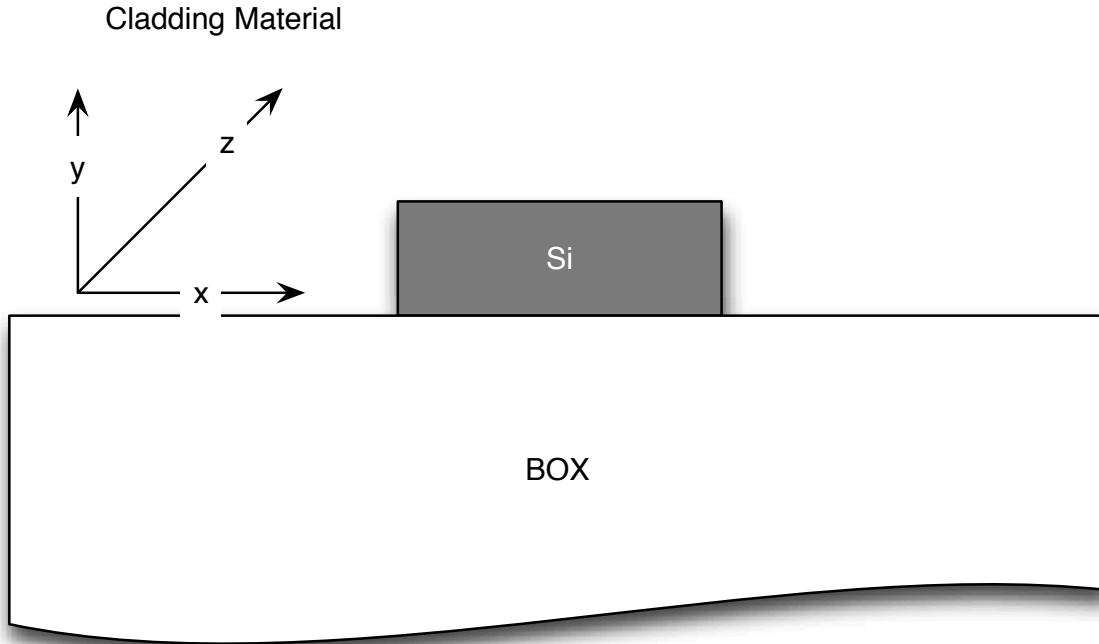
When trying to construct integrate photonics circuit on silicon, the first challenge encountered is to design and build a single mode low loss waveguide. The waveguide guides light and connect components in a photonics circuit. Unlike the small refractive index difference ( $\Delta n \approx 0.01$ ) in optical fibers, the refractive index different in SOI is very large( $\Delta n \approx 2.0$ ). As a result, the guided optical mode is highly confined, and generally doesn't have a closed form analytical solution. The same is true for almost all silicon photonics structures. To well model and understand the behavior of the guided mode, a program has to be used to discretize and numerically solve the Maxwell's equation.

Most practical silicon waveguides are formed in the SOI platform by an etch, providing either a ridge or a strip-loaded ridge geometry. The feature size of commonly used waveguide is around 500nm. With the proper choice of ridge width, only a single TE or TM mode will be supported. Waveguides that meet this condition are known as single-

mode waveguides. The high index of the silicon creates tight confinement of the mode. On one hand, this is a very attractive advantage of silicon photonics because it allow for going through ultra small bend radii on (5  $\mu\text{m}$ ) without significant optical loss, which is vital for building high density photonic integrate circuits. On the other hand, the highly confined optical mode has a high field intensity at the Si/SiO<sub>2</sub> boundary, thus the optical loss is particularly sensitive to sidewall roughness and scattering centers in the waveguide. Even a minimal amount of roughness on the waveguide can result in catastrophic loss. Roughness on the waveguide usually arises due to imperfections in the mask used to etch the waveguide as well as to anisotropies in the etching process itself. Over the last decade, great effort has been spend on both fabrication process and optical design, bringing the loss number from 30dB/cm to around 1dB/cm [12] for single-mode waveguides. For multi-mode waveguides in silicon, the value is even lower; losses on the order of 0.3 dB/cm [13] have been achieved. This is an acceptable value for building a real system-- it allows one to construct an optical path of a few centimeters length without losing too much power.

### **2.3: Mode solving**

As we have discussed above, a very basic but nontrivial question in silicon photonics is how guided mode propagates in a waveguide. The structure of a common waveguide is a high index medium surrounded by a low index medium (Fig.2.2 ). As a result, the optical field was confined, and only field of certain pattern could propagate along the waveguide.



**Fig 2.2 Optical Mode Solving**

The behavior of the guided mode is governed by the Maxwell's equation. However, the strong dielectric boundary condition at the Si/SiO<sub>2</sub> interface makes it very hard to solve the Maxwell's equations analytically; numerical method is needed in practical. To develop the algorithm for solving the modal pattern, let's start with the Maxwell's equation of a time harmonic field.

$$\begin{aligned}\nabla \times \vec{H} &= -i\omega\epsilon_r \vec{E} \\ \nabla \times \vec{E} &= i\omega\mu_r \vec{H}\end{aligned}\tag{2.1}$$

Here we've assumed no variation in magnetic permeability, which is true for many common materials. Furthermore, let's assume the structure has translational symmetry along the z axis, in other words,

$$\epsilon(x, y, z + \Delta z) = \epsilon(x, y, z)$$

is satisfied for any  $\Delta z$ .

An optical mode is a solution to the Maxwell's equation with phase dependence  $e^{i(\beta z - \omega t)}$ , where  $\beta$  is the propagation constant. In photonics, the propagation constant is more commonly expressed in terms of effective index  $n_{eff}$ . In this convention, a guided mode can be formally expressed as

$$\begin{pmatrix} \mathbf{E} \\ \mathbf{H} \end{pmatrix} = \begin{pmatrix} \mathbf{E}_m(x, y, \omega) \\ \mathbf{H}_m(x, y, \omega) \end{pmatrix} \exp\left(in_{eff}(\omega)z - i\omega t - \frac{\omega}{c}z\right) \quad (2.2)$$

The goal of mode solving is to find the effective index and associated modal pattern of a given waveguide geometry at certain frequency.

By applying the curl operator again, we can reexpress (2.1) as an eigenvalue problem in H.

$$\nabla \times \frac{1}{\epsilon} \nabla \times \mathbf{H} = \frac{\omega^2}{c^2} \mathbf{H} \quad (2.3)$$

Equation (2.3) is sometimes called the “master equation” for H field. To solve it numerically, we discretize the H field on a spatial grid (the Yee grid is commonly used), and rewrite (2.3) in the matrix form. To obtain a relative accurate solution, a 10nm grid spacing is recommended. Combined with appropriate boundary conditions (periodic in Z direction and zero on other directions), it is possible to solve for the eigenvalue and associated eigenvector of (2.3) via numerical methods like Lanczos iteration, and readily derive the modal pattern and effective index. By applying the mode solve at different frequencies, we can obtain the effective index as a function of frequency, named the dispersion relation. The dispersion relation plays a key roll in photonics engineering. From it, many important parameters associated with the mode like group index and group

velocity dispersion (GVD) [5] can be calculated. Fig2.3 shows an example of solved mode and dispersion relation of a ridge and a slot waveguide.

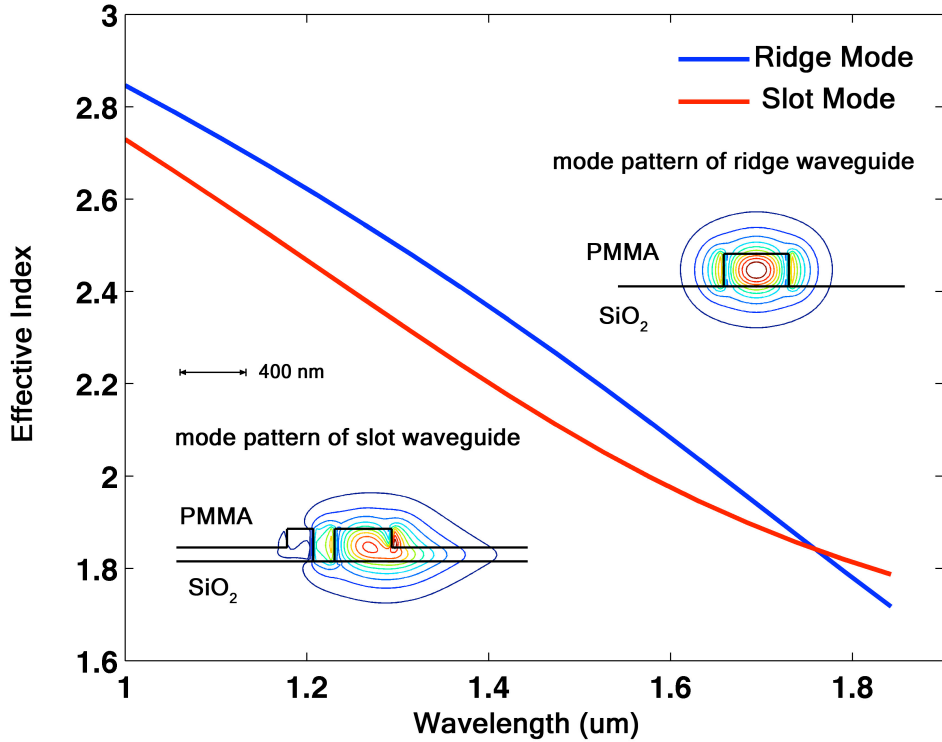


Fig 2.3 The Mode and dispersion plot of strip and strip-loaded slot waveguides. The strip waveguide has 400 nm width and 200 nm height. The strip-loaded slot waveguide has 350 nm wide large arm, 160 nm wide small arm and 130 nm wide slot. Both waveguides are clad in polymethyl methacrylate. The inserts show the TE<sub>0</sub> modes of strip and strip-loaded slot waveguides. Contours in  $|E_x|$  are shown [15].

## 2.4 Electromagnetic simulation: FDTD

When designing an integrated photonics circuit, it's often needed to analyze the optical property (i.e. transmission and reflection spectrum) of some 3D structures like a waveguide taper or y junction. Since even for a simple ridge waveguide, one cannot solve for modal pattern in closed form. It's probably not surprising that for these more complicated structures, analytical expression is in general not available. The Finite-difference time-domain (FDTD) [14] method is a robust and relative accurate algorithm

that is widely used for the simulation of light propagation in silicon photonic devices. It directly discretizes Maxwell's equations on the Yee grids, and integrates the revolution of electromagnetism field in the time domain. With use of Fourier transformation, the time domain field information can be readily translated in to frequency domain transfer functions.

Here let me present an example of FDTD simulation. In a photonics device like a modulator, the actual functioning waveguide is usually different from the routing bus waveguide. Therefore, mode converters [15] are needed to connect different types of waveguide without inducing too much optical loss. In our work toward building a slot waveguide modulator, we designed a mode converter to efficiently couple ridge waveguides to strip-loaded slot waveguides.

With the help of FDTD simulation, we proposed the following structure. It is composed first of a taper from a ridge waveguide to a strip-loaded slot waveguide. Then, a slot curves in from the side gradually. Crucially, there are no sharp points in the optically active region. We try to keep the termination point of the slot far away from the main waveguide as possible, in order to minimize the extra scattering at the termination of the slot.

The mode converter was simulated using the FDTD package from Rsoft. We launched a ridge waveguide mode and placed 2 cross-section monitors before and after the mode conversion region. The monitors project the EM wave onto the ridge and strip-loaded slot

modes, obtaining the power contained in the modes. At steady state, the simulated loss is 0.86 dB at 1550 nm. After the design was fabricated, the measured insertion loss agreed perfectly with the FDTD prediction.

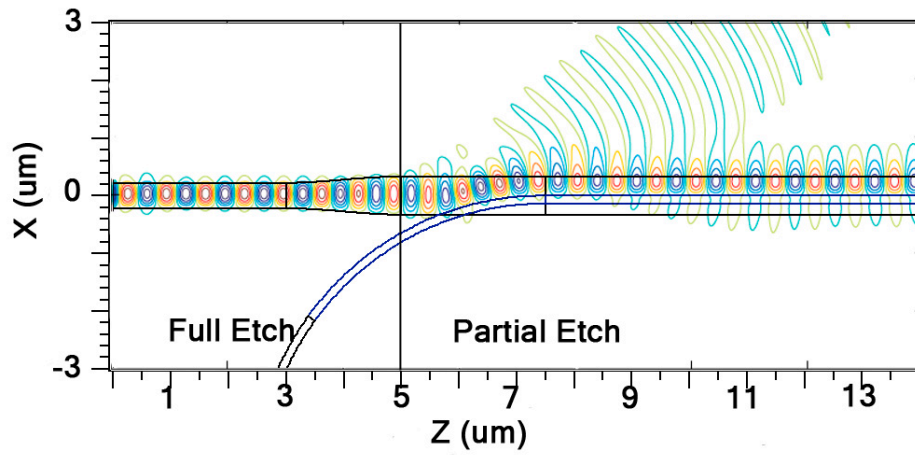


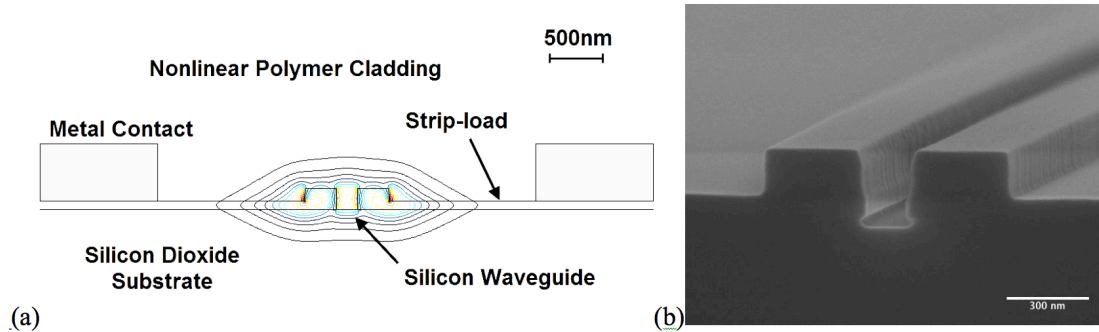
Fig 2.4 FDTD simulation of a mode converter[15]

## Chapter 3 Silicon Modulators- Polymer Approach

### 3.1 Introduction

In order to build a photonics toolbox for intra and inter chip data communication on the CMOS-compatible SOI platform, a EO modulator with high bandwidth, low power, low driving voltage is one of the key components that need to be implemented. Modulators operating at several tens of gigahertz with below 1V<sub>pp</sub> driving voltage are highly desirable, for compatibility with CMOS circuit. However, achieving efficient modulation at high speed in silicon has been a challenge for a long time [16]. Due to the inversion symmetry of its lattice structure, silicon happens to not have the Pockels' effect. Thus, alternative methods need to be explored for modulation. In the past decade, the silicon photonics community has made great progress in modulator development, and boosted the modulation speed from the MHz range to 50GHz. Generally, the approaches been demonstrated so far can be divided into two categories. One of them is using the plasma dispersion effect (also called the free carrier effect[17]), in which the concentration of free charges in silicon changes the real and imaginary parts of the refractive index. We will explore the details of this approach in the following chapters. Another approach is incorporating EO materials to the SOI platform. Taking advantage of slot waveguide and a highly nonlinear electro-optic (EO) organic material. This method can potentially achieve very high speeds and low power consumption. Base on this concept, we've demonstrated a modulator with a bandwidth of 500MHz and a  $V\pi L$  of 0.8 V.cm [18] on the silicon-polymer hybrid platform.

### 3.2 Design and fabrication



**Fig 3.1 a. Sketch of the slot waveguide as used in this work. The modal pattern near 1550nm is plotted; contours of  $|E_x|$  are shown (b) SEM micrograph of the cross-section of a strip-loaded slot waveguide**

The structure of this modulator is a Mach-Zehnder interferometer (MZI), with phase shifters in both arms. The phased shifter in this device is a strip loaded slot silicon waveguide filled with highly nonlinear EO polymer, which is able to change its refractive index when electric field is applied. The configurations and SEM image of the “strip-loaded” slot waveguide are shown in Fig. 3.1. The slot waveguide [19] consists of two strips of silicon separated by a very narrow trench. When filled with low index polymer, light will be strongly confined into the slot, providing enhanced modulation efficiency. When voltage is applied, the arms of the slot waveguide also act as electrodes, creating a strong electric field in the slot region, which also help to achieve more phase shift. A thin strip of doped silicon, so called “strip-loading”, is used to connect the metal pad to each arm of the slot waveguide. In this specific device, the waveguide dimensions are 200 nm silicon thickness, 300 nm arm width, and 200 nm slot width, the modal pattern near 1550 nm as shown in Fig. 3.1(a). To avoid extra optical loss, the metal electrodes were placed 10  $\mu\text{m}$  away from the waveguide.

The thickness and doping level of the silicon strip load need to be carefully designed. The first consideration is the tradeoff between optical loss and electrical conductivity. Heavier doping level in the strip load helps to reduce the parasitic resistance, therefore lead to a higher operation speed. However high doping level also induce extra loss. Another consideration is the thickness of the strip load. Making the strip-loading thicker will naturally decrease the resistance in accordance with Ohm's law, although the optical mode becomes less confined, which reduce the modulation efficiency. To balance, we chose a relatively thick strip-loading as 70 nm to accommodate various doping concentrations.

The fabrication of the slot waveguides was done with two self- aligned photolithography steps on a 193 nm stepper and two Si dry etching steps on Silicon- On-Insulator (SOI) wafers (having 220 nm thick silicon layer, 2  $\mu\text{m}$  thick buried oxide layer and substrate resistivity of 10  $\Omega\text{-cm}$ ). Thin thermal oxide was employed to smoothen the waveguide sidewalls. This oxide was stripped by buffered oxide etch (BOE) before metallization. The chip was uniformly  $10^{18} \text{ cm}^{-3}$  Boron doped (resistivity was anticipated as 0.04  $\Omega\text{-cm}$ ) and annealed after fabrication. The metallization process was done by contact photolithography and the pads were formed by Al evaporated and lift-off process. Before polymer coating, a 10min anneal at 460  $^{\circ}\text{C}$  was performed to enhance metal-semiconductor contact since there was no contact implant step.

The EO polymer used on this device is AJSP100 developed by Alex Jen et al, for broad spectrum of photonic applications [ref]. It exhibits relatively large electro-optic activity ( $r_{33}$  value of  $\sim 65$  pm/V at 1550 nm), low optical loss ( $\sim 1$  dB/cm), and good temporal and photochemical stability. The electro-optic polymer cladding was prepared by doping AJSP100 into PMMA host and the resultant refractive index of the polymer was 1.54 at 1550 nm. A poling field of  $100$  V/ $\mu\text{m}$  and poling temperature of  $103$  °C were used. During the poling the center pad was set to  $0$  V, left pad was set to  $+V_{\text{pole}}$  and right pad was set to  $-V_{\text{pole}}$ , where  $V_{\text{pole}} = 20$  V to achieve the poling field across a  $200$  nm slot. During modulation, the center pad was set to signal while the left and right pads were held at ground, so that the modulator was operated in a push-pull fashion.

### **3.3 Measurement results**

Grating couplers were used to couple light on and off the chip [21], which had a  $3$  dB bandwidth of around  $35$  nm. Figure 3 shows device transmission spectra for various DC drive voltages, which was applied to the center pad of the device while the side pads being held at ground. Because the MZI was intentionally unbalanced, with arm lengths of  $1$  mm and  $1.08$  mm, there is an approximately  $7$  nm periodicity in the transmission as a function of wavelength. The more gradual variation is from the grating coupler bandwidth. The half-wave voltage  $V_{\pi}$  can be roughly determined as  $8$  V, from the plots, which corresponds to a  $V_{\pi}L$  of  $0.8$  V-cm. Due to the strip-loading, the optical mode was less confined as compared to that of a slot waveguide without strip-loading, and the  $200$

nm relatively wide slot further lowered the effective index susceptibility [22] , which turned out to be only  $0.2 \mu\text{m}^{-1}$ . Thus,  $0.8 \text{ V-cm V}\pi\text{L}$  suggested that an in-device poled  $r_{33}$  of  $40 \text{ pm/V}$  was achieved.

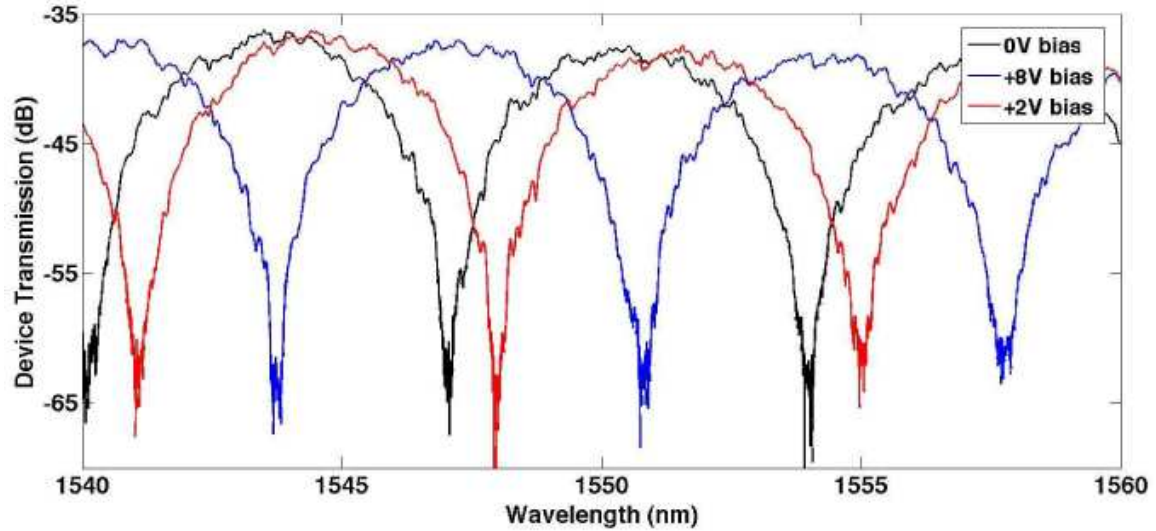


Fig 3.2 Spectrum of MZI when bias voltage is applied

Solely from the static phase shift, we can't rule out the possibility that the phase shift was due to other mechanisms. To confirm the phase shift is induced by the polymer, frequency response of the device need to be measured. In the RF measurement, the wavelength of the input laser was set to the quadrature point of the MZI to maximum response at a driving voltage. Due to the limitation of our equipment, the frequency response was characterized with different apparatuses, and catenated together.

For the 20MHz to 2GHz frequency range, a vector network analyzer (VNA) was used to drive the modulator from port 1, with a New Focus 1647 1.1 GHz bandwidth avalanche photodiode (APD) converting the optical response to RF, which was directed to port 2. Then, a New Focus 1414 25 GHz high-speed photodetector was used instead of the APD to take data from 100 MHz up to 6 GHz. It can readily be shown that the  $S_{21}$  parameter

is directly related to the  $V\pi$  value of the modulator when the modulator is biased at the  $-3$  dB point, so as to be in a linear operating regime. The typical signal to noise ratio encountered in this measurement was 30 dB. As the modulator was expected to have high impedance, we assumed that the drive voltage was doubled on the actual device.

For the frequency range from 200 Hz to 100 MHz, a function generator was used to drive the modulator with a sinusoidal signal with peak-to-peak voltage of 2 V. A DC lock-in amplifier and an RF lock-in amplifier were used to characterize the signal output by the photodetector, which was a Thorlab DET01CFC. The results are shown in Fig. 4 as normalized S21. The corresponding normalized S21 of  $8 V V\pi$  is also plotted on the same axes. The S21 measurement from each detector was renormalized as well for the detector gain and the laser power level, so as to allow direct comparisons between different measurements. Typical noise floors were at least 10 dB beneath the measurement, and often substantially lower. The noise floor during the measurement with the high-speed detector is plotted in Fig. 4. Since the high-speed photodetector only has a peak gain of 0.6 A/W, and the VNA has a lower dynamic range in low frequency band, the data taken with the high-speed photodetector is not presented for the frequency range from 100 MHz to 200 MHz due to the low signal to noise ratio.

From the spectrum of S21, we observed that the flatness of the response extended from DC to gigahertz range, and the absolute value of S21 corresponded very well to the value implied by  $8 V V\pi$ . 3 dB rolloff point occurred at around 500 MHz. The capacitance of each arm can be estimated as 80 pF/m if we assume the polymer has a RF dielectric constant of 4 [13]. When combined with the arm resistance, which is roughly 70  $\Omega$  from

each pad to the waveguide arm (assuming fully-charged surface states, thus 10nm silicon depletion region at this doping), one would expect to see a device bandwidth on the order of 15 GHz. So, our observed bandwidth was significantly lower than the predicted value. RF coupling to the substrate is another possible source of the rolloff – the pads are large and the silicon substrate beneath the buried-oxide layer is not highly resistive. Further design and experimental work is expected to increase the bandwidth of these devices greatly.

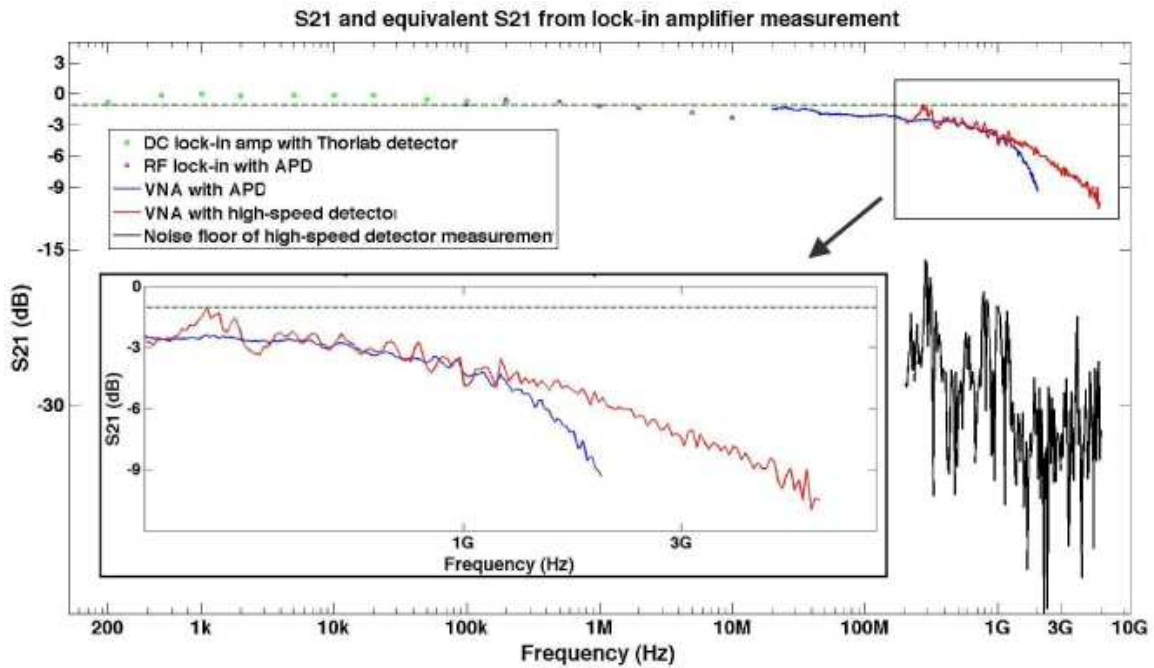


Fig 3.3 RF performance of the MZI

[#Ref the polymer modulator paper]

## **Chapter 4 Optical Semiconductor Design Tools**

### **4.1 Introduction**

Though the silicon-polymer hybrid approach is very compelling for its potential to work at very high speed, it also has some drawbacks. Firstly, the fabrication of these devices is relatively complicated since it includes some CMOS compatible steps like polling. Furthermore, the exploit of second order material in this wavelength range may be challenging since organics tend to have strong absorption at longer wavelength. On the contrary, free-carrier based modulators, due to their reliability and excellent integrability with modern CMOS process flow, have drawn more attention in the community in the past few years.

In this chapter, I'll introduce some useful simulation tools for modeling and understanding semiconductor devices. These methods will become important building blocks in the design of free carrier based silicon modulators.

### **4.2 Semiconductor Process Simulation**

Since first invented 50 years ago, the integrated circuit has changed our world. Its remarkable success is built on a highly developed silicon manufacturing technology. With this technology, billions of transistors can be integrated on a single chip. In modern silicon manufacturing technology, a set of unit steps including etching, lithography, deposition, implantation, thermal annealing, and metallization, are performed successively and turn silicon into useful devices. The goal of semiconductor process simulation is to accurately model these unit steps and predict the properties of the

fabricated device, including active dopant distribution, and device geometry. The semiconductor process simulation is usually the first step of a semiconductor device design flow. It takes the fabrication conditions as input, and output a virtual device containing detailed electrical characteristics, which can then be used as input for device simulation.

Sentaurus Process (Sprocess)[23] is the world leading process simulation package. Now let's take a look at how the fabrication of an ion doped waveguide was simulated in Sprocess.

The fabrication process starts from SOS (silicon on sapphire) wafer. The top silicon layer is 600 nm thick, with 10  $\Omega\cdot\text{cm}$  resistivity, corresponding to a  $1\times 10^{15}/\text{cm}^3$  Boron concentration.

- a): Silicon waveguide was defined by lithography, and formed by an 500nm silicon dry (anisotropic)etch. The remaining photoresist was striped.
- b): Conformal deposition of 200 nm thick silicon oxide, this oxide layer will act as a hard mask for implantation and silicidation.
- c): 300nm photoresist was deposited and patterned. Left pad region was exposed by an oxide etch. Phosphorus implantation with 30 keV energy,  $4\times 10^{14}/\text{cm}^2$  dose, and  $7^\circ$  tilt angle was performed. The remaining photoresist was striped after implantation.
- d): deposit 500nm photoresist and expose right pad region, Boron implantation with 10 keV energy,  $4\times 10^{14}/\text{cm}^2$  dose and  $7^\circ$  tilt angle was performed . The photoresist is acting as an implant screening on the left pad.

e): A rapid thermal annealing at 1050 °C for 10 seconds was used to activate the dopants. A 300nm thick Titanium layer was deposited by sputtering, and reacts at 800°C for 30 seconds to form silicide on the left and right pad. After reaction, the remaining Ti was removed.

f): Put down Al on the left and right pad, anneal at 400 °C to achieve good contact. After the thermal annealing, the doping concentration is  $3 \times 10^{19}/\text{cm}^3$  in n type region and  $2.5 \times 10^{19}/\text{cm}^3$  in p type region.

The designer can inspect each process step individually and adjust the recipe until the result meets the expectation. The final virtual device can be directly imported by Sentaurus Device for device simulation.

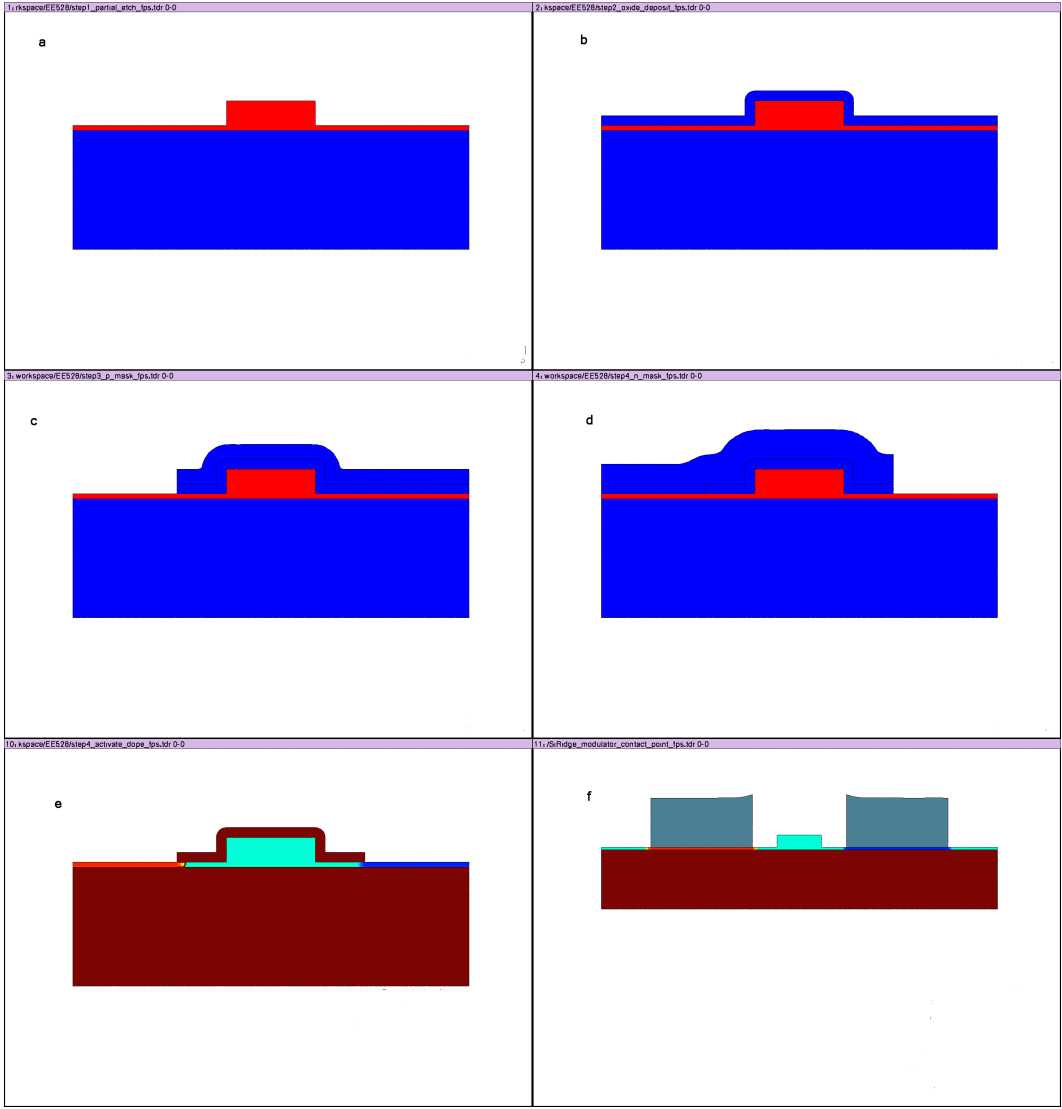


Fig 4.1 illustration of the fabrication of a doped waveguide in Process

### 4.3 Semiconductor Device Simulation

To successfully design a free carrier based modulator in silicon, it's essential to understand the electrical performance of the device. For instance, how the electrons and holes are distributed in the device when a voltage is applied, what's the current density at each spatial point, etc. This can be done by semiconductor device simulation software. In

this thesis, the industry standard package Sentaurus Device (Sdevice)[24] will be used for device simulation. To see how device simulation is done, let's first briefly review the basic equations in a semiconductor.

The carriers and currents in a semiconductor device are governed by a set of coupled partial derivative equations:

Continuity equation for electrons and holes:

$$\frac{dn}{dt} = \frac{1}{q} \nabla \cdot \vec{J}_n + G - R$$

$$\frac{dp}{dt} = -\frac{1}{q} \nabla \cdot \vec{J}_p + G - R$$

Drift diffusion equation for electron and hole current

$$\vec{J}_n = q(\mu_n n \vec{E} + D_n \nabla n)$$

$$\vec{J}_p = q(\mu_p p \vec{E} - D_p \nabla p)$$

Poisson equation

$$\nabla^2 \psi = -\frac{q(p - n + N_d^+ - N_a^-)}{\epsilon \epsilon_0}$$

$$n = n_i e^{q(\psi_i - \psi_f)/kT}$$

$$p = n_i e^{-q(\psi_i - \psi_f)/kT}$$

In Sdevice, these coupled nonlinear equations are discretized on a mesh grid and solved numerically [ref device manual]. After simulation, the carrier distribution, electric potential, and current density in the device can be obtained. Depending on the problem to be solved, other physics models, such as the high field velocity saturation, the SRH recombination, and optical generation can be incorporated into the simulation.

As an example, let's take a look at the simulation of a 1D PN junction. The left side is uniformly doped with Boron with concentration of  $1E18$ , and the right side is uniformly doped with Phosphorus with  $1E19$  concentration. We are interested in the band structure, carrier distribution and electric field in the junction at equilibrium as well as the junction capacitance when a bias voltage is applied. The simulation result can be readily checked with the well-known analytical model.

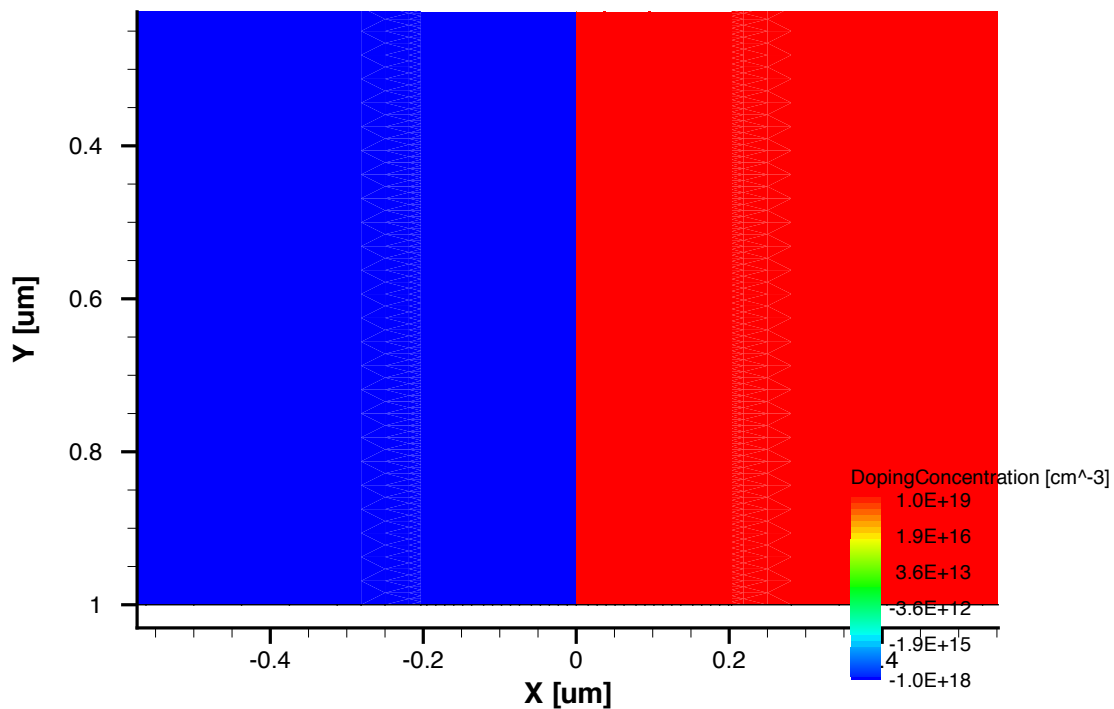


Fig 4.2 1D pn junction in Sdevice

The field dependent mobility, SRH recombination, and band gap narrowing were taken into account in the simulation. The spacing of mesh grid was 5nm near the junction, and 30nm elsewhere.

At the first simulation step, no bias voltage was applied, so the junction is at equilibrium. The band structure, space charge and electric field were plotted in Fig 4.3.

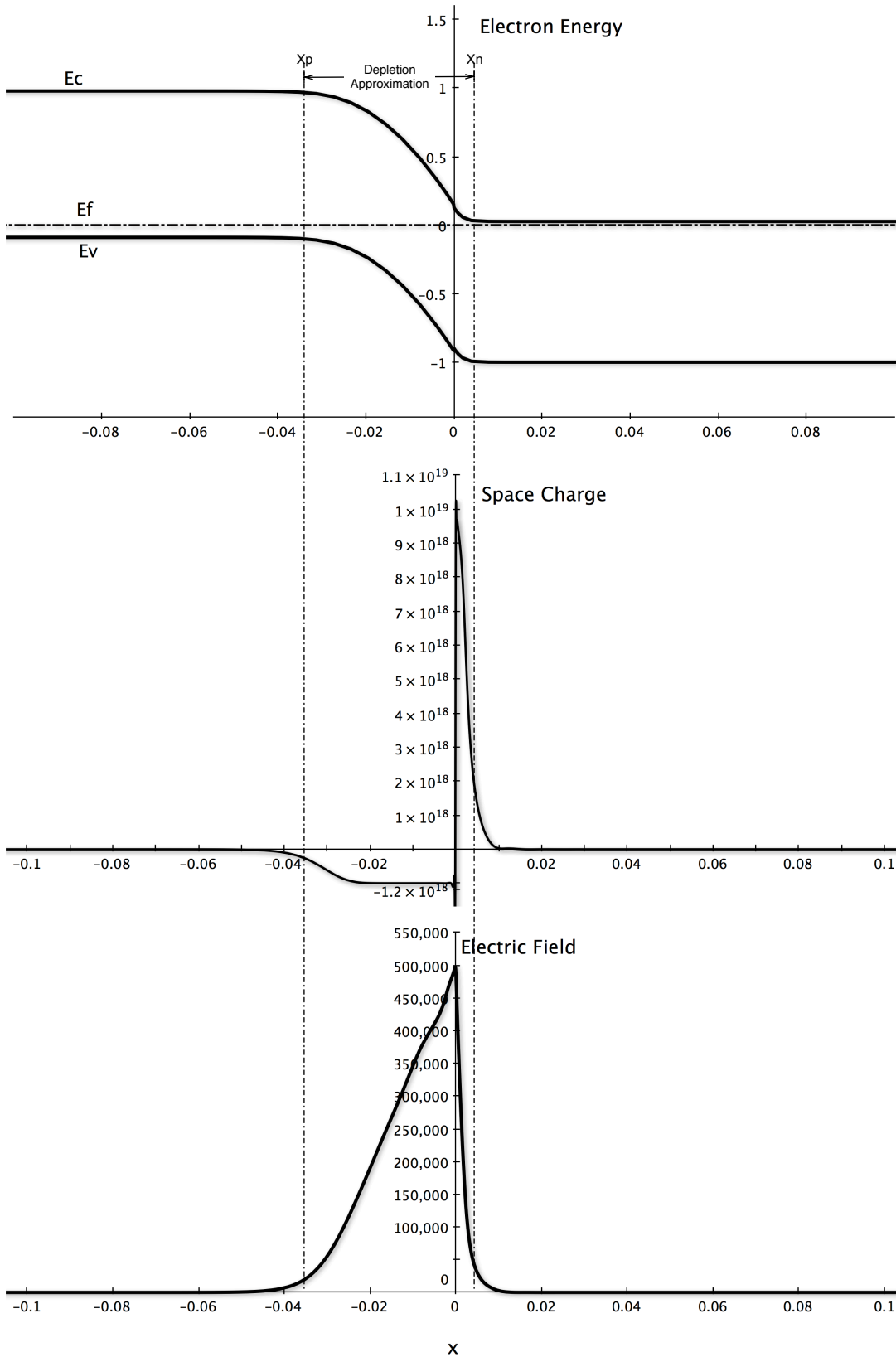


Fig 4.3 simulation of pn junction at equilibrium

Let's compare the simulation result with the analytical model. When proceeding the analytical calculation, the depletion approximation was used, which assumes the depletion charge has a box profile [25]. In this simplified condition, the width of the depletion width can be calculated as.

$$\begin{aligned}
 \phi_i &= \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right) = 1.01 eV \\
 x_p &= -\frac{N_a}{N_a + N_d} \sqrt{\frac{2\epsilon_s}{q} \phi_i \left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = -34.8 nm \\
 x_n &= \frac{N_d}{N_a + N_d} \sqrt{\frac{2\epsilon_s}{q} \phi_i \left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = 3.48 nm
 \end{aligned} \tag{4.1}$$

As we can see, the simulation and the analytical calculation are in good agreement. Almost all electric fields and band bending happens in the depletion region predicted by eq(4.1). However, the space charge near the edge of the depletion region has a gradual transition from 0 to the impurity level, rather than sudden jump as assumed by the depletion approximation. As we'll see later the depletion width given by (4.1) is overestimated due to this non-box charge profile.

In the second simulation step, a bias voltage is applied across the junction. The junction capacitance was extracted from a small signal AC analysis. The junction capacitance obtained by numerical simulation is about 7% larger than the value predicted by the depletion approximation. As the reverse bias increased, the capacitance decrease as we expected.

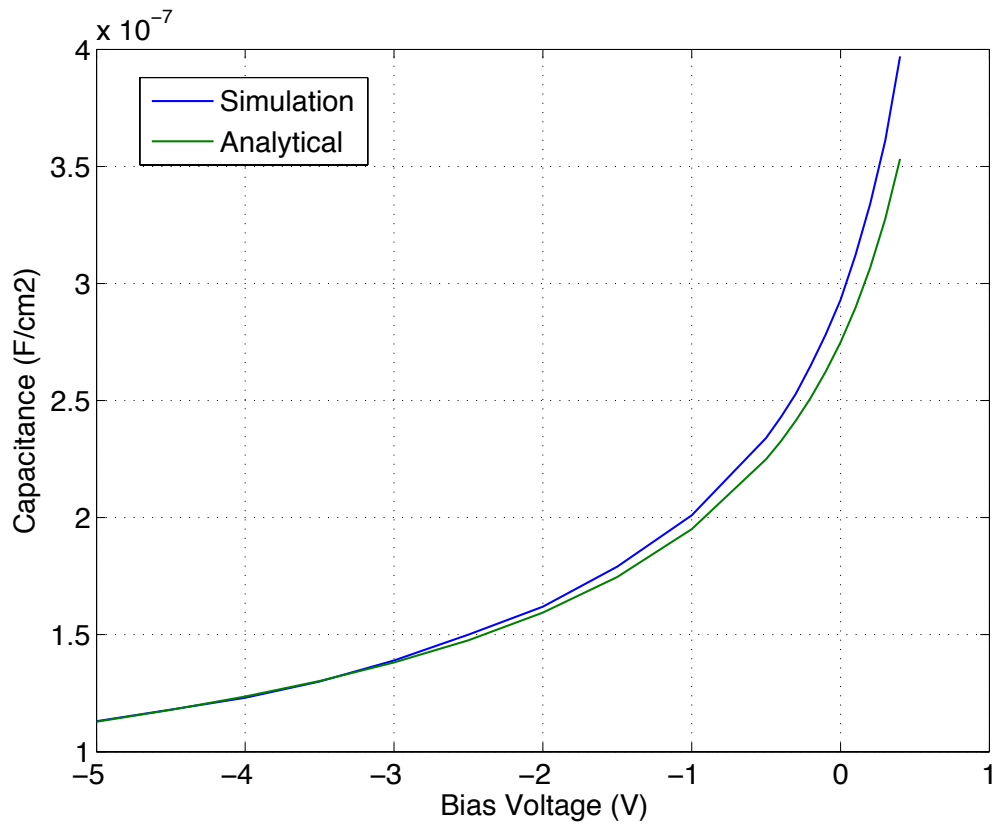


Fig 4.4 The pn junction capacitance under different bias voltage.

## Chapter 5 The PN Junction Optical Modulator

### 5.1 PN junction modulators-State of the Art

Today, the most common approach for achieving EO modulation is using a reverse biased pn junction based Mach-Zehnder interferometer[16] . In this approach, a pn junction is formed in the waveguide (Fig 5.1). When operating, the junction is reverse biased, and the width of its depletion region is modulated by the input electrical signal, causing the change of the waveguide effective index. Light propagating through the waveguide then experiences a phase shift. The unique advantage of this approach is very high operation bandwidth and CMOS compatible fabrication process. In the past half decade, great effort has been made to improve the metrics of pn junction based modulators. So far, the highest 3dB bandwidth reported in literature 30 GHz, and 50 Gb/s [26] . The lowest  $V\pi L$  shown is 1.1 V-cm [27] . Table 1 lists the important results reported in literature.

In this chapter, I'll illustrate the principle and fundamental limitation of a pn junction modulator by a simplified 1D analytical model. Then we'll establish a design flow, which is able to predict the modulator performance from the fabrication recipe. This with this design flow, we'll be able to dramatically improve the modulator performance by optimizing the fabrication recipe.

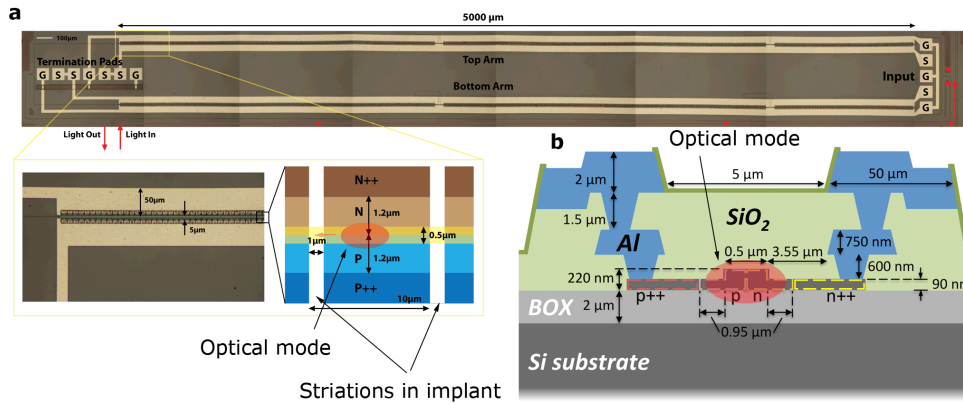


Fig 5.1 Illustration of a pn junction based modulator [9]

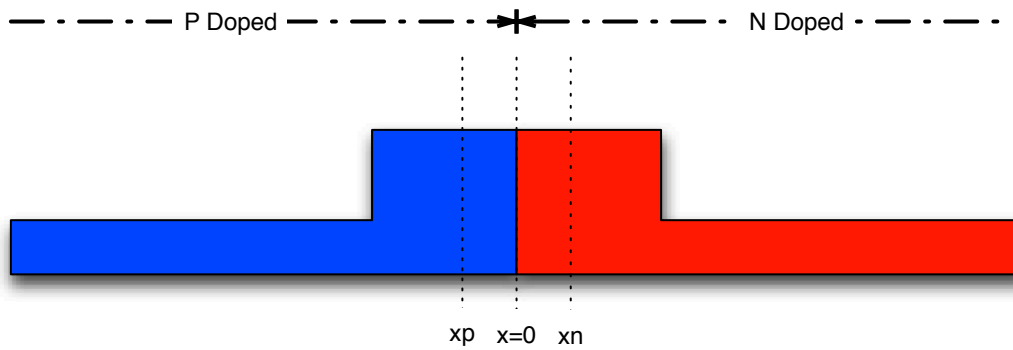
Vpp(V)	VpiL (V.cm)	length (cm)	insertion loss (dB)	Loss(dB/cm) due to dopants	ER (dB)	doping level (p/n)	Speed (Gb/s)
6 [28]	11	0.14	15	57	6.5	1.00E+18	40
4 [29]	2.7	0.35	15	40	7.5	3E17/1.5e18	40
5 [27]	1.1	0.05	N.A	30	N.A	1.00E+18	10
6 [30]	4	0.1	<4	18	1.1	1.50E+17	40
6.5 [31]	8	0.35	N.A	N.A	6	3E17/1.5e18	10
N.A [32]	4	0.05	N.A	N.A	N.A	1E18/2E17	40(26GHz)
6 [33]	1.4	0.1	N.A	19	>7	1E18~5E17	12.5
5 [34]	2.18	0.4	N.A	4.5	8	N.A	10 (17GHz)
6 [35]	2.4	0.24	<5	17	7.2	N.A	30(30GHz)

Table 5.1 pn junction based modulator in literature

## 5.2: 1D analytical model

In a conventional design of a pn junction modulator, the phase shifter is a slab waveguide with a lateral PN junction formed in the center. A typical cross section of such a phase shifter is sketched in Fig.5.1. To understand the basic idea and performance tradeoffs of the phase shifter, let's first do some rough estimation under the following simplified conditions Fig 5.2.

- Half of the waveguide is uniformly doped with P type dopants, with concentration  $N_a$ , the other half of the waveguide is uniformly doped with N type dopants, the concentration is  $N_d$ . An abrupt junction is formed right at the center of the waveguide.
- The optical mode in the waveguide is approximated by a uniform field profile. In other words, the light intensity in the waveguide is assumed to be a constant.
- The junction is considered as a 1D structure, any fringe effect is ignored



**Fig 5.2 Simplified pn junction model**

Under this set of assumptions, we can derive the performance of the phase shifter analytically. When the bias voltage  $V_a$  was applied on the electrodes, the width of the depleted N and P region can be expressed as:

$$\begin{aligned}
\phi_i &= \frac{kT}{q} \ln \left( \frac{N_a N_d}{n_i^2} \right) \\
x_p &= \frac{N_a}{N_a + N_d} \sqrt{\frac{2\epsilon_s}{q} (\phi_i - V_a) \left( \frac{1}{N_a} + \frac{1}{N_d} \right)} \\
x_n &= \frac{N_d}{N_a + N_d} \sqrt{\frac{2\epsilon_s}{q} (\phi_i - V_a) \left( \frac{1}{N_a} + \frac{1}{N_d} \right)}
\end{aligned} \tag{1}$$

The change of refractive index and absorption of silicon due to changes in the carrier densities in silicon at 1.55um is [17] :

$$\begin{aligned}
\Delta n &= \Delta n_e + \Delta n_h = - \left[ 8.8 \times 10^{-22} \Delta n_e + 8.5 \times 10^{-18} \Delta n_h^{0.8} \right] \\
\Delta \alpha &= 8.5 \times 10^{-18} \Delta n_e + 6.0 \times 10^{-18} \Delta n_h
\end{aligned} \tag{2}$$

From this expression, we could know the average change of effective index and absorption coefficient of the whole waveguide.

$$\begin{aligned}
\Delta n_{eff} &= - \left[ 8.8 \times 10^{-22} N_d \frac{x_n}{D} + 8.5 \times 10^{-18} N_a^{0.8} \frac{x_p}{D} \right] \\
\Delta \alpha_{eff} &= \frac{1}{2} \left( 8.5 \times 10^{-18} N_d + 6.0 \times 10^{-18} N_a \right)
\end{aligned}$$

The expressions above reveals the fundamental trade off of the pn junction modulator—it's very hard to achieve a low  $V\pi L$ . Increasing the doping concentration helps reducing the  $V\pi L$ , but at the same time, the extra optical loss goes up very rapidly (Fig 5.3). For instance, to achieve a 0.3V.cm  $V\pi L$ , the doping level need to be around 4E19 with about 1000dB/cm excess loss!

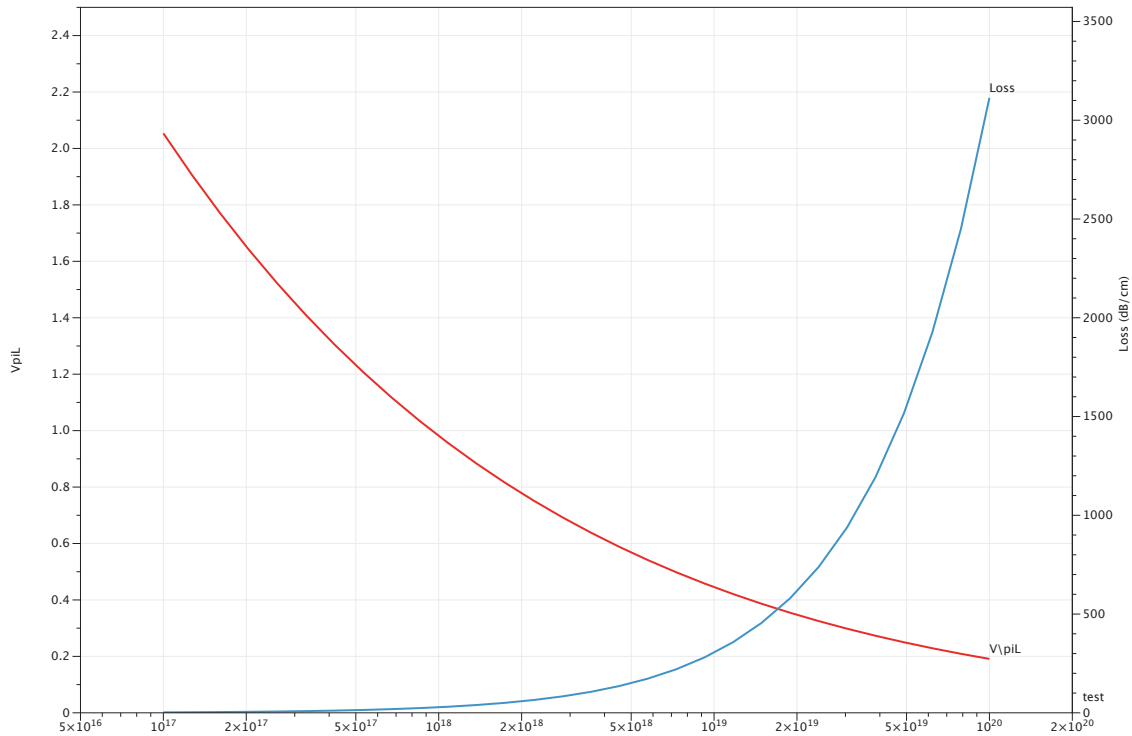


Fig 5.3 the fundamental trade off of lateral junction

### 5.3: Junction simulation, combining Sdevice and mode overlap

The above 1D model is useful for understanding the principle of a pn modulator, but it's oversimplified in several aspects. On one hand, the doping profile in the waveguide is quite complicate since dopants in the waveguide are usually induced by implantations. On the other hand, the optical mode in the waveguide is also nonuniform. Thus the modulator performance predicted by the 1D model is not accurate enough for modulator design. To model the phase shift and optical loss in the waveguide more precisely, we need to establish a more detailed model, which take into account the nonuniform distribution of both the free carrier and the optical mode.

Let's start from the optical mode in an undoped silicon waveguide. After obtaining the effective index and transverse modal pattern from the mode solver, each propagating mode is fully specified by:

$$\begin{pmatrix} \mathbf{E} \\ \mathbf{H} \end{pmatrix} = \begin{pmatrix} \mathbf{E}_m(x, y, \omega) \\ \mathbf{H}_m(x, y, \omega) \end{pmatrix} \exp\left(in_{eff}(\omega)z \frac{\omega}{c} - i\omega t\right) \quad (3)$$

plugging (3) into the Maxwell's equations for a guided mode [ref Tom].

$$\begin{pmatrix} i\omega\epsilon_0\epsilon(x, y) & 0 & 0 & 0 & 0 & \partial_y \\ 0 & i\omega\epsilon_0\epsilon(x, y) & 0 & 0 & 0 & -\partial_x \\ 0 & 0 & i\omega\epsilon_0\epsilon(x, y) & -\partial_y & \partial_x & 0 \\ 0 & 0 & -\partial_y & i\omega\mu_0 & 0 & 0 \\ 0 & 0 & \partial_x & 0 & i\omega\mu_0 & 0 \\ \partial_y & -\partial_x & 0 & 0 & 0 & i\omega\mu_0 \end{pmatrix} \begin{pmatrix} Ex \\ Ey \\ Ez \\ Hx \\ Hy \\ Hz \end{pmatrix} = i\beta \begin{pmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} Ex \\ Ey \\ Ez \\ Hx \\ Hy \\ Hz \end{pmatrix} \quad (4)$$

Equation (4) can be more compactly written as:

$$H\psi = i\beta A\psi \quad (5)$$

Here the H and A are hermitian and anti-hermitian operators identified with the left and right 6x6 matrices in (5), respectively, and the  $\psi$  is the 6-vector of E, H in a single column. Equation (5) has great importance in integrated optics because it fully characterizes a guided mode. We'll see later that the combination of equation (5) and perturbation theory gives us a convenient way to predict the phase shift and optical loss of an pn doped waveguide.

In the case of a doped waveguide, the presence of free carriers will change the local refractive index and absorption coefficient slightly. This effect can be expressed as a perturbation of permittivity  $\epsilon(x, y) = \epsilon^0(x, y) + \Delta\epsilon(x, y)$ . In our application, the change in  $\epsilon$  is usually very small ( $\sim 0.1\%$ ), so that the optical mode can be regarded as unchanged, and the effect of the free carrier can be regarded as a small perturbation.

$$H = H^0 + \Delta H = \begin{pmatrix} i\omega\epsilon_0\epsilon(x,y) & 0 & 0 & 0 & 0 & \partial_y \\ 0 & i\omega\epsilon_0\epsilon(x,y) & 0 & 0 & 0 & -\partial_x \\ 0 & 0 & i\omega\epsilon_0\epsilon(x,y) & -\partial_y & \partial_x & 0 \\ 0 & 0 & -\partial_y & i\omega\mu_0 & 0 & 0 \\ 0 & 0 & \partial_x & 0 & i\omega\mu_0 & 0 \\ \partial_y & -\partial_x & 0 & 0 & 0 & i\omega\mu_0 \end{pmatrix} + i\omega\epsilon_0\Delta\epsilon(x,y) \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}$$

Due to this permittivity change, the propagation constant of the optical mode is also changed by a small amount. Our goal is figure out the change of the effective index of the mode.

$$\begin{aligned} i(\beta + \Delta\beta) &= \frac{\langle \psi | H^0 + \Delta H | \psi \rangle}{\langle \psi | A | \psi \rangle} = \frac{\langle \psi | H^0 | \psi \rangle + \langle \psi | \Delta H | \psi \rangle}{\langle \psi | A | \psi \rangle} = i\beta + \frac{\langle \psi | \Delta H | \psi \rangle}{\langle \psi | A | \psi \rangle} \\ &= i\beta + \frac{\langle \psi | \Delta H | \psi \rangle}{\langle \psi | A | \psi \rangle} = i\beta + \frac{i\omega\epsilon_0 \iint \Delta\epsilon(x,y) |\vec{E}|^2 dx dy}{2 \iint \text{Re}(\vec{E} \times \vec{H}) dx dy} \end{aligned}$$

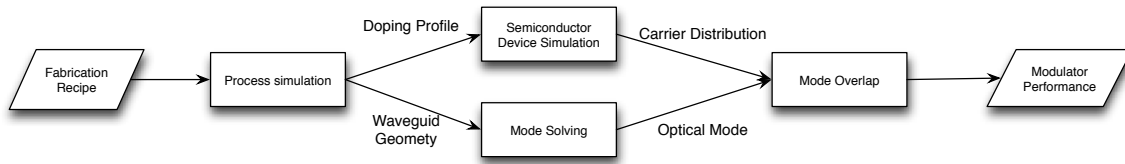
Noting at a certain frequency, the change in propagation constant is proportional to the change in effective index, we have.

$$\Delta n_{eff} = \frac{n_{si} \iint_{si} \Delta n(x,y) |\vec{E}|^2 dx dy}{Z_0 \iint \text{Re}(\vec{E} \times \vec{H}) dx dy} \quad (6)$$

$$\Delta \alpha_{eff} = \frac{n_{si} \iint_{si} \Delta \alpha(x,y) |\vec{E}|^2 dx dy}{Z_0 \iint \text{Re}(\vec{E} \times \vec{H}) dx dy}$$

## 5.5: Full Simulation of a PN modulator

Now we've introduced all the necessary tools and method and ready to fully simulate the performance of an pn modulator from scratch.



**Fig 5.4 Design flow of pn junction modulator**

The simulation starts from the fabrication recipe. Via process simulation, we obtain the waveguide geometry and doping profile in the waveguide. The unpertubated optical mode solving is done with the fabricated waveguide geometry and assuming zero free carrier. On the other hand, the carrier distribution in the waveguide was simulated under difference bias voltage in Sdevice. By overlapping the carrier concentration and the optical mode according to eq(6), we can figure out the change in effective index and optical loss induced by the free carriers, and further more the  $V\pi L$  of the modulator.

Here’s an example illustrating the design flow. Assuming the phase shifter is fabricated with the following recipe:

	<b>Step1</b>	<b>Step2</b>
<b>P implant</b>	Boron, 15keV, 4E12/cm2, 7° tilt	Boron, 50keV, 6E12/cm2, 7° tilt
<b>N implant</b>	Phosphorus, 45keV, 2.5E12/cm2, 7° tilt	Phosphorus, 130keV, 4E12/cm2, 7° tilt
<b>Anneal</b>	1030 ° C, 5s	

**Table 5.2 Implantation Recipe**

Start with the SOI wafer with 220nm top silicon and 2um BOX, the 500nm wide waveguide was patterned and formed by an anisotropic partial silicon etch, leaving 90nm silicon in the strip load region. Then the waveguide was implanted by Boron with the right half covered by photo resist. Similarly, the right half of the waveguide was implanted by phosphorus with the left half covered. The whole structure was then

annealed in an RTA step. The details of the implantation and RTA step are listed in the following table.

The above recipe was simulated in Sentaurus Process. The simulated active dopants distribution and the waveguide geometry was illustrated in Fig 5.5.

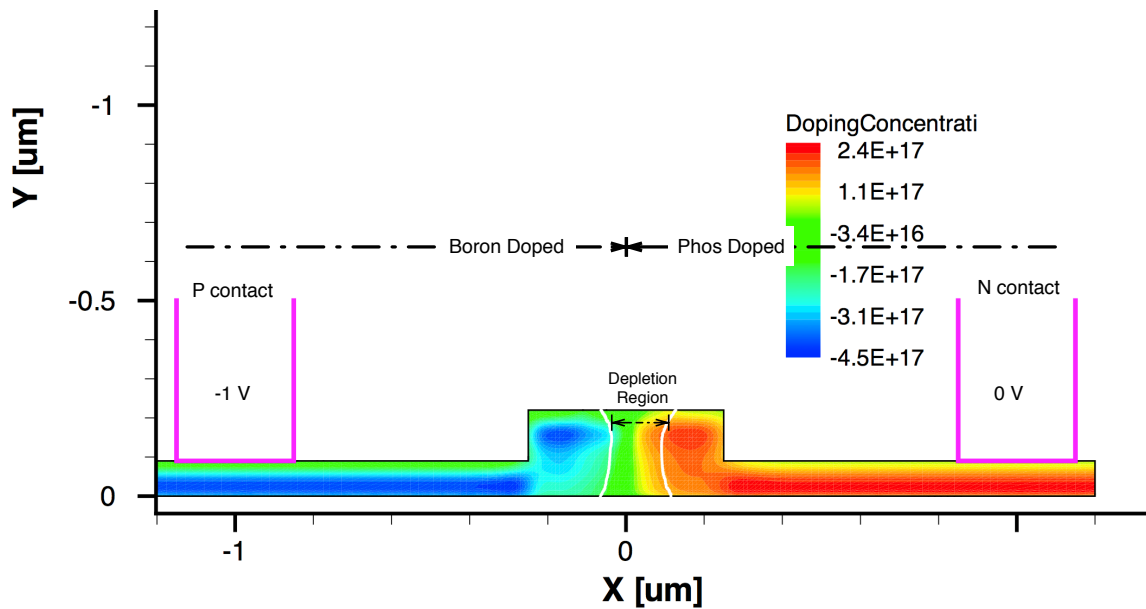


Fig 5.5 process and device simulation

The simulation of free carrier distribution and capacitance under various bias voltage was done in Sdevice, and the corresponding phase shift and optical loss was obtained by the mode overlap integral. The summary of the simulation was listed in Table 5.3.

Bias (V)	Phase Shift (rad/cm)	VpiL (V.cm)	Optical Loss (dB/cm)	Junction Capacitance(F/um)
0.5	-1.28	1.11	5.01	3.51E-16
0	0.00	1.44	4.52	2.43E-16

-0.5	0.93	1.82	4.15	2.07E-16
-1	1.71	2.21	3.85	1.86E-16
-1.5	2.38	2.53	3.59	1.72E-16
-2	2.99	2.77	3.35	1.61E-16
-2.5	3.54	2.94	3.14	1.53E-16
-3	4.04	3.12	2.95	1.45E-16
-3.5	4.51	3.47	2.77	1.39E-16
-4	4.95	4.30	2.61	1.34E-16

Table 5.3 summary of phase shifter simulation

## 5.6 Measurement of modulator parameters

To verify the above simulation technique, let's compare the predicted modulator performance with the test data. Device fabrication was done at the Institute of Microelectronics (IME)/A\*STAR [9]. The starting material was an 8" Silicon-on-Insulator (SOI) wafer from SOITEC, with a Boron-doped top silicon layer of around 10 ohm-cm resistivity and 220 nm thickness, a 2  $\mu\text{m}$  bottom oxide thickness, and a 750 ohm-cm handle silicon wafer, needed for RF performance. Slab waveguides used for modulation were formed using an anisotropic dry etch. A lateral pn junction was defined in the center of the rib with p and n implants on the exposed silicon, prior to any oxide fill. The p and n implantation recipe was IME proprietary, and not listed here. Additional p++ and n++ implants were utilized for ohmic contact formation. followed by a rapid thermal anneal at 1030  $^{\circ}\text{C}$  for 5 s for Si dopant activation, and then by the formation of contact vias and two levels of aluminum. The schematic cross-section of the final device is shown in Fig. 5.1. Additional etch steps, not shown here, were used to define grating

couplers, used to couple to a fiber mode, and channel waveguides, used for routing.

The modulation efficiency of the junction was characterized by 5mm MZI. The two arms of the MZI were intentionally unbalanced by 100um, Both arm of the MZI was pn junction loaded to balance the optical loss. Transmission spectrum as a function of wavelength for varying reverse-bias voltages was measured. By fitting the spectra to the idea transfer function  $P = P_0(1 + \cos(\frac{2\pi}{FSR}\lambda + \varphi))$ , the relative phase shift at each bias voltage is extracted and compared with the simulation.

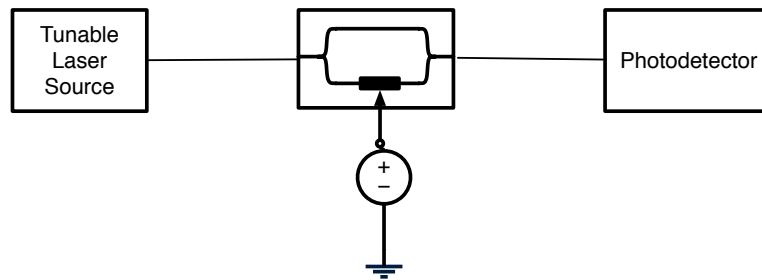
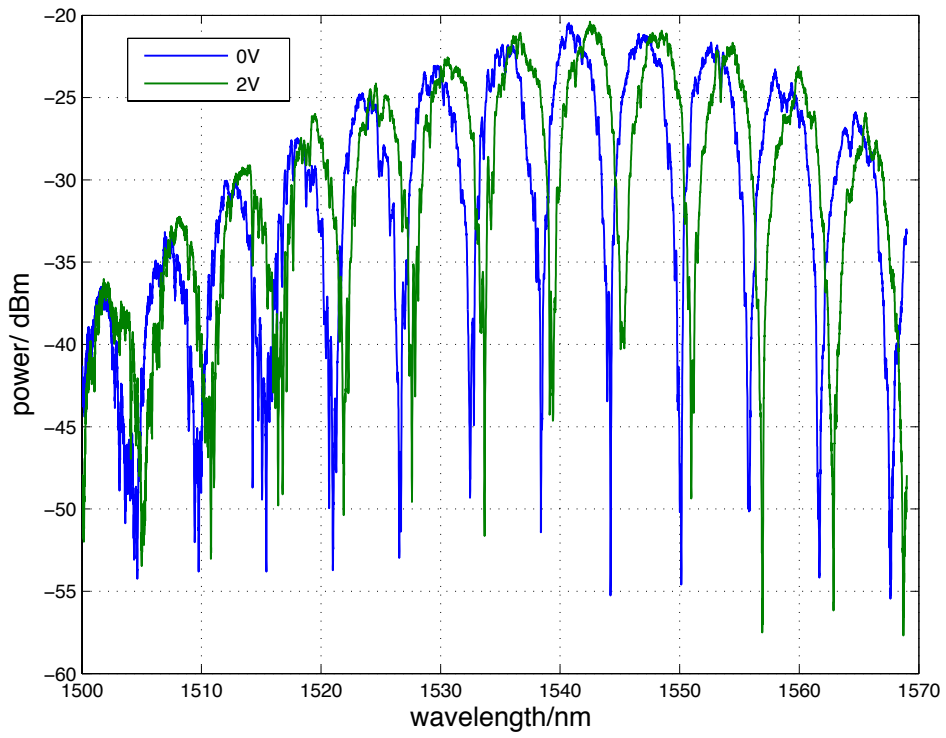
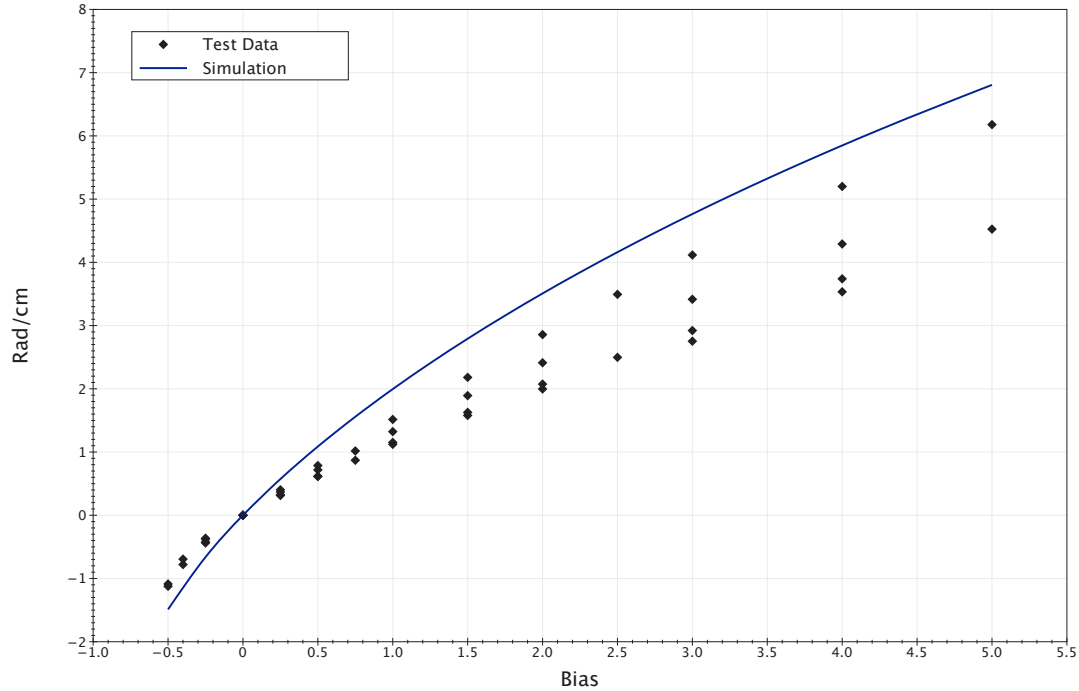


Fig 5.6 modulator static phase shift setup



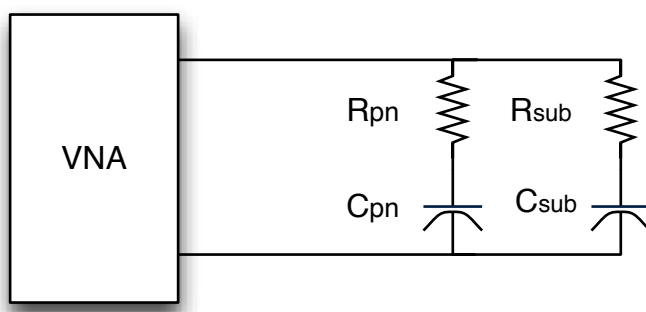
**Fig 5.7 The spectrum shift when applied bias voltage**



**Fig 5.8 Phase shift was a function of voltage.**

The simulation result is very close to the measured phase shift. The small discrepancy could be due to a number of reasons. For instance, the dopants could have diffused more than expected in the annealing step, causing the junction to be blurred. It could also be that the thickness of the silicon strip load is thicker than we expected, so that the optical mode is less confined. Further work is needed to identify the source of this discrepancy.

Finally, C-V measurements were taken by measuring the S11 of the phase shifter.



$$Z_1 = \left( \frac{1}{i\omega C_{pn}} + R_{pn} \right) \parallel \left( \frac{1}{i\omega C_{sub}} + R_{sub} \right)$$

$$S_{11} = \frac{Z_1 - Z_0}{Z_1 + Z_0}$$

It's easy to show that at low frequency, the phase of S11 is proportional to the total capacitance.

$$\varphi = 4\pi Z_0 (C_{sub} + C_{pn})$$

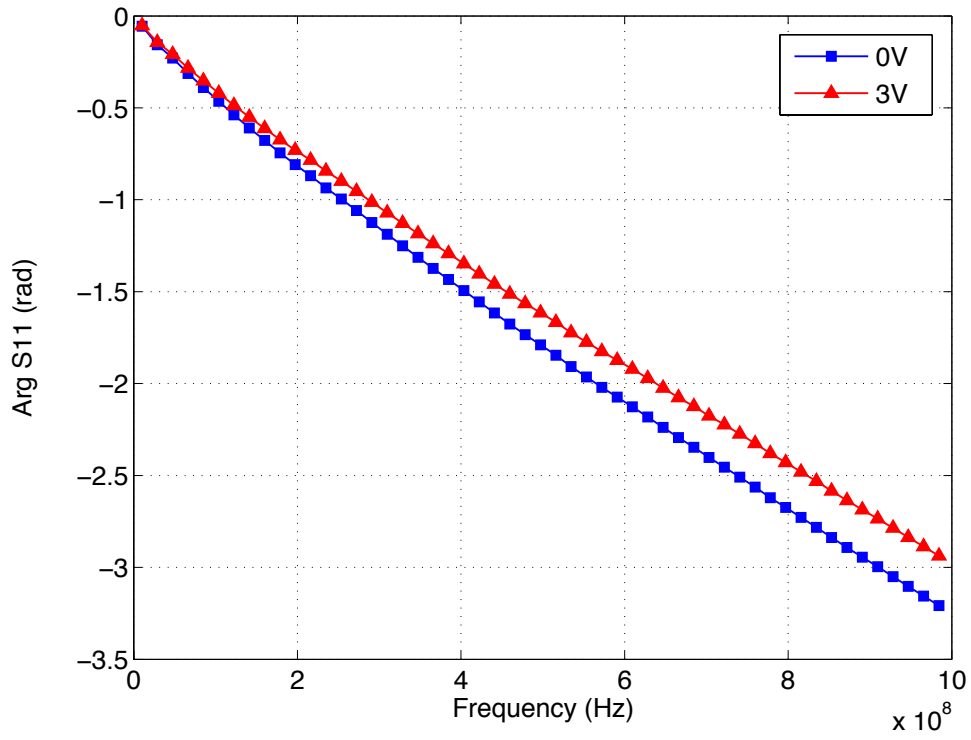


Fig 5.9 Measured Arg of S11

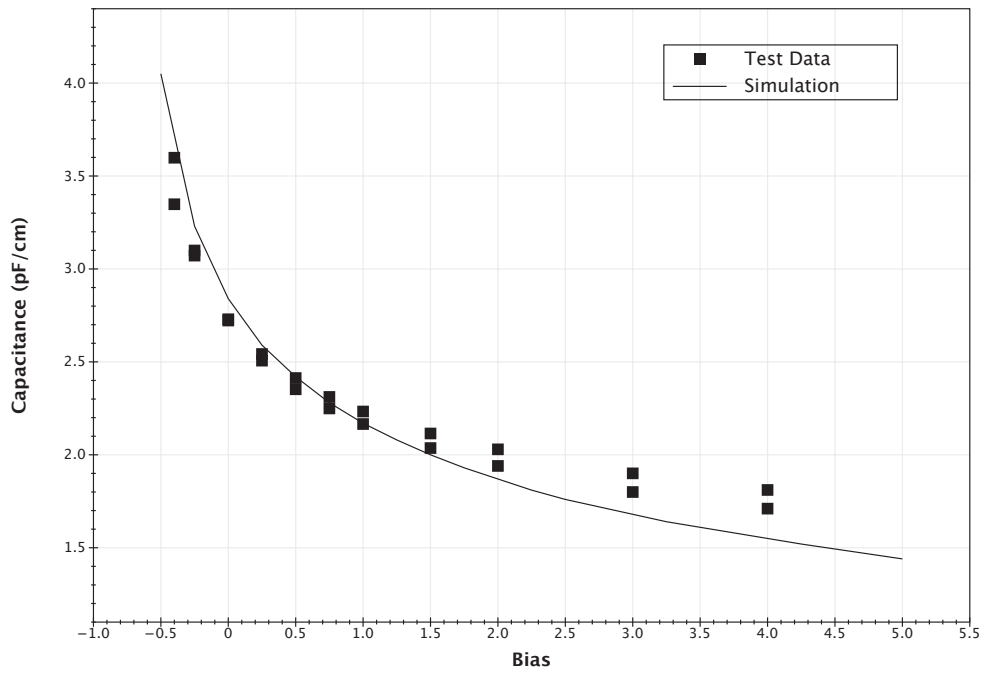


Fig 5.10 Junction capacitance as a function of bias voltage

As shown in Fig.5.10, the simulated capacitance is in well agreement with the measurement.

## Chapter 6 Enhanced PN junction Design

### 6.1 Introduction

In the past half decade, the operation speed free carrier based silicon EO modulator has been improved dramatically. The bandwidth has been boosted from the megahertz range to tens of gigahertz [26]. However, the modulation efficiency (characterized by  $V\pi L$ ) of this approach is substantially limited by optical loss. The best  $V\pi L$  reported in a MZI modulator so far is 1.1 V.cm [27], associated with 30dB/cm dopants induced optical loss. As a result, to get a desirable optical modulation, one either need a large driving voltage, or need to elongate the device length, which both raise the optical insertion loss and bring up difficulty for the RF design. In this chapter, I'm going to propose a new junction design, which provides much lower  $V\pi L$  and modest optical loss. With this design, it'll be possible to design a ultra low driving voltage, compact high speed modulator in silicon.

### 6.2 Innovation

The key of the design is to carefully design the depth profile of P and N type of dopants, so the profile for N type dopants shows two peaks, one near the top of the waveguide, and the other near the bottom of the waveguide. On the other hand, the profile for P type dopants shows one peak near the middle of the waveguide (Fig 6.1). By exposing the center of the waveguide to both N and P dopants in implantation, we can create a PN

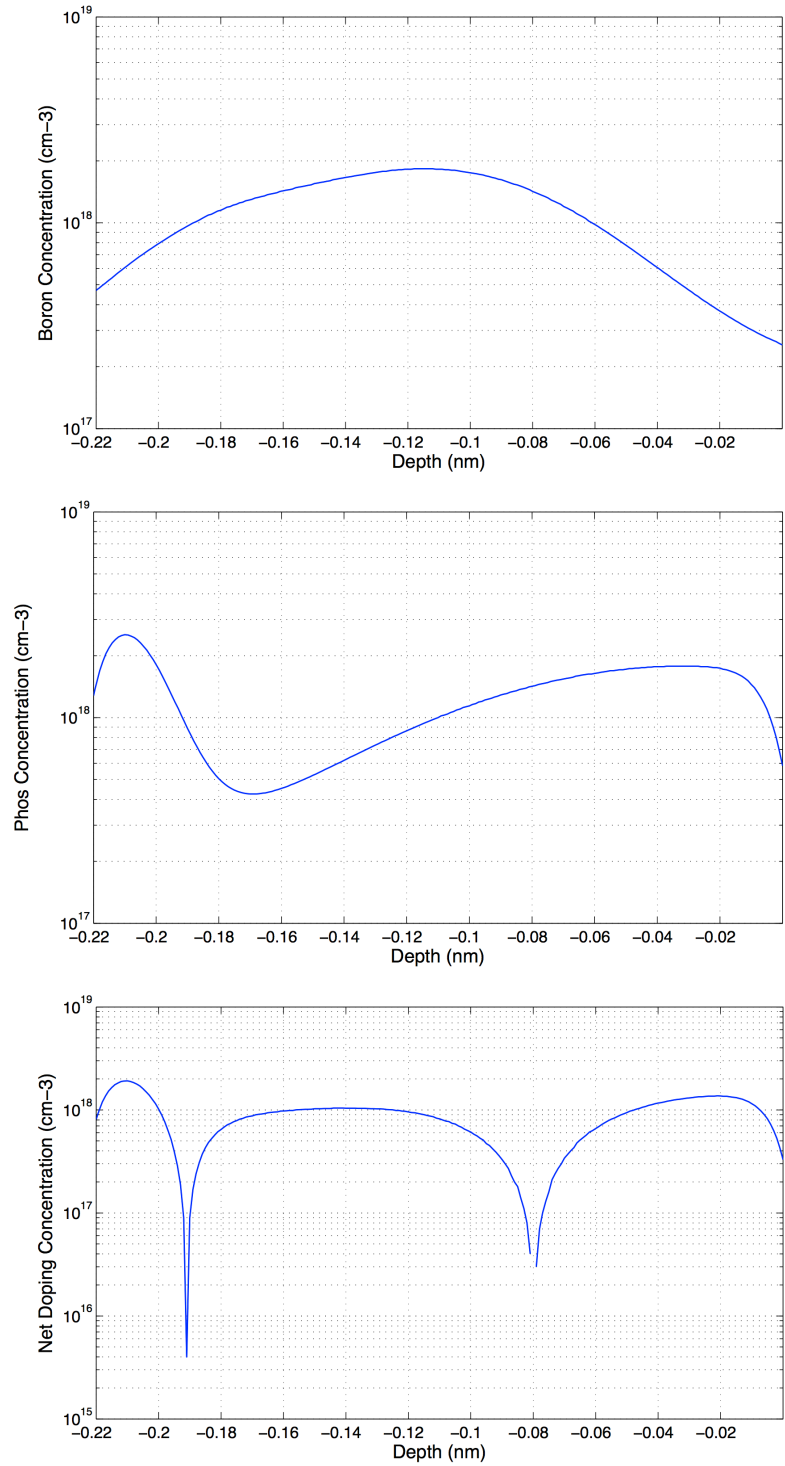
junction with an “S” shape (Fig 6.2). This type of junctions have much larger overlap with the optical mode than the lateral junction shown in, thus the  $V\pi L$  is much smaller.

Here lists the proposed fabrication steps.

- Start with SOI wafer with 220nm top silicon and 2um BOX, define the silicon slab waveguide with 130nm anisotropic etch. The resulted slab waveguide has 500nm width and 90nm slab height.
- Deposit 10nm thin silicon oxide layer on the waveguide to reduce the channeling effect in the following implantation steps.
- Ion implantation and activation with the following recipe. During the implantation, the opening of N and P mask has 300nm overlap.

	<b>Step1</b>	<b>Step2</b>
<b>P implant</b>	Boron 13.5keV, 3.65E12, 7° tilt, 4 twist splits	Boron 32.4keV, 2.26E13, 7° tilt, 4 twist splits
<b>N implant</b>	Phosphorus 9.8keV 1.08E13, 7° tilt, 4 twist splits	Phosphorus 160keV 3.50E13, 7° tilt, 4 twist splits
<b>Anneal</b>	1030° C, 5s	

**Table 6.1 Proposed implantation recipe**



**Fig 6.1 Depth Profile of Boron, Phosphorus and net doping after annealing**

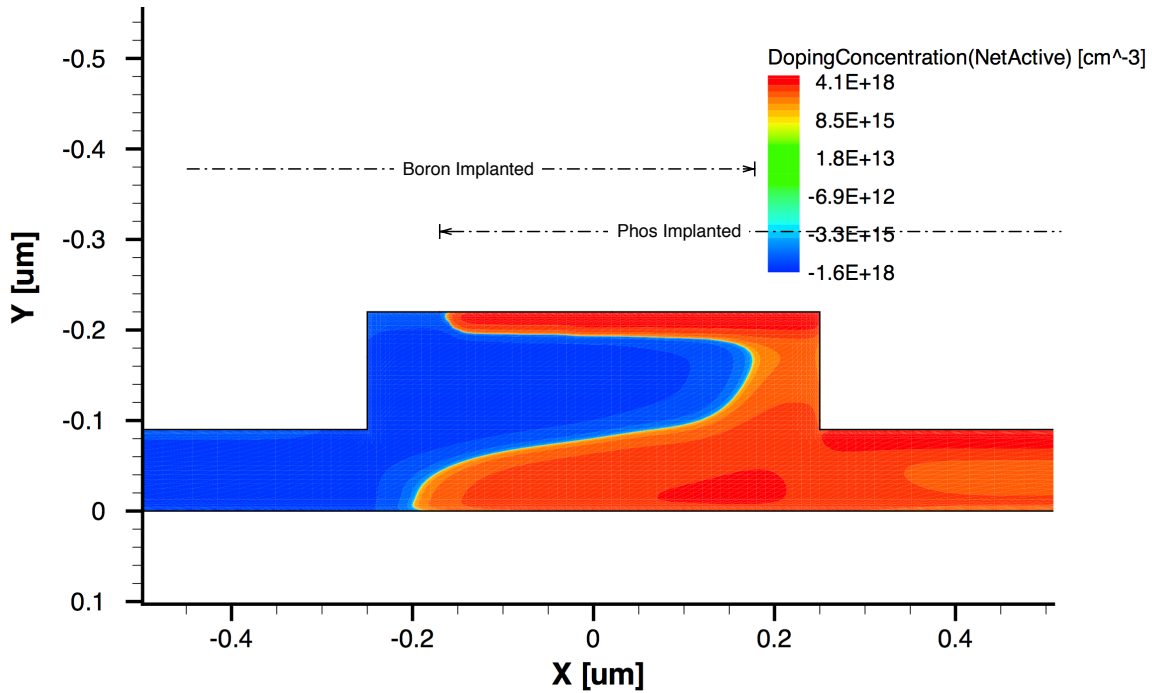


Fig 6.2 Dopants distribution on the cross section of the waveguide

### 6.3 Junction Performance

V	$V\pi L$ (V.cm)	Loss (dB/cm)	C(F/um)
-0.5	0.21	24.45	2.60E-15
0	0.27	21.38	1.61E-15
0.5	0.35	19.07	1.20E-15
1.0	0.45	17.24	9.49E-16
1.5	0.58	15.80	7.57E-16
2.0	0.74	14.69	5.94E-16
2.5	0.95	13.85	4.31E-16
3.0	1.27	13.27	3.15E-16

Table 6.2 performance of the junction

The performance of the proposed pn junction is listed above. Comparing with a typical lateral junction in Table 5.3, the  $V\pi L$  is substantially lower. For a lateral junction, in order to get the same  $V\pi L$ , the optical loss would have been on the order of 1000dB/cm. Combining the proposed junction with the proper RF design, it's possible to design a

traveling wave MZI [9] with subvolt driving voltage, ultra-compact ( $\sim 1\text{mm}$ ) and high speed (30GHz), which is close to the state of art commercial  $\text{LiNbO}_3$  modulators.

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