PCAST: A Practical Capacitor Array Synthesizer Targeted for SAR-ADC Implementation

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Abstract

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In this thesis, we introduce PCAST, a practical capacitor array synthesizer targeted for SAR-ADC implementation developed in the SKILL® language, which is natively supported by the Cadence EDA tools. We demonstrate that the proposed tool is capable of performing placement and routing of capacitor array layout under the symmetry and matching constraints.

The layout generation is performed in two steps. The first step is generating a metal-oxide-metal (MOM) unit capacitor layout and symbol. The second stage is generating the layout, netlist, and symbol of the capacitor array.

The synthesizer supports a wide range of user-specified parameters. The supported users specified parameters are chosen in consultation with experienced circuit designers to ensure the proposed tool can be effectively deployed in production. The output of PCAST is in GDSII format, ensuring the tool can be seamlessly integrated with circuit design software. The correctness of the synthesized layout can be validated by the physical verification tools. For each design, PCAST automatically outputs the capacitance parasitics and the mismatch for SAR-ADC linearity characterization. PCAST has been used in production for several SAR-ADCs that have been fabricated in 180nm, 65nm, 28nm CMOS, as well as 16nm and 14nm finFET. It significantly reduces design efforts and the chance of cockpit error in the layout of the capacitor array.

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GLOSSARY

ADC: Analog-to-digital converter

CAD: Computer aided design

CADENCE SKILL: A Lisp language used as a scripting language and PCell (parameterized cells) description language used in many EDA software suites by Cadence Design Systems.

CDAC: Capacitive digital-to-analog conversion

CMOS: Complementary metal-oxide-semiconductor

DRC: Design rules checking

EDA: Electronic design automation

ENOB: Effective number of bits

FOM: Figure of merit

GDSII FORMAT: Industry standard database for IC layout

HPP: Parallel plate capacitor

IC: Integrated circuits

LVS: Layout versus schematic

MOM CAPACITOR: Metal-Oxide-Metal capacitor

MOS CAPACITOR: Metal-oxide-semiconductor capacitor

MSB: The most significant bit

NETLIST: A description of the connectivity of an electronic circuit

PCAST: A practical capacitor array synthesizer targeted for SAR-ADC implementation

PDK: Process design kit

PEX: Practices extraction

PYHTON: A widely used high-level programming language used for general- purpose programming, created by Guido van Rossum and first released in 1991

P-N JUNCTION: A boundary or interface between two types of semiconductor material, p-type and n-type, inside a single crystal of semiconductor.

RADIX: The ratio between different bits

S12: Reverse Transmission Coefficient (leakage or isolation)

SAR: Successive approximation register

SNDR: Signal-to-(noise + distortion)

SOCS: System on chips

S-PARAMETERS: Scattering parameters

VPP: Interdigitated capacitor

Y-PARAMETERS: Admittance parameters

Z-PARAMETERS: Impedance parameters

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Finally, I would also like to thank my family, who are always supporting and encouraging me.

DEDICATION

To my parents.

Chapter 1

INTRODUCTION

Successive-approximation-register (SAR) analog-to-digital converter (ADC) is the most popular architecture for low-power design [1]. A key component of an SAR-ADC is the capacitor arrays for capacitive digital-to-analog converters (CDACs), and each capacitor serves as a bit weight, which is a multiple of the unit capacitance, for successive bit resolving. The area, speed, power, linearity [2] as well as the yield of an SAR-ADC depend critically on the design and layout of CDAC arrays. To reduce the switching power, state-of-art SAR-ADCs use metal-oxide-metal (MOM) capacitors, with unit capacitance as low as 0.3fF to 0.5fF [3].

The design and layout of MOM capacitor arrays with femtofarad and sub-femtofarad unit capacitance present several challenges. First, the exact capacitance of bit capacitors and their match under process variation are determined by the layout. Not only the design of unit capacitor itself but also the placement, interconnection and spacing of hundreds of unit capacitors are crucial. The state of art SAR-ADC design relies on experienced analog designers for manual layout, a highly laborious, repetitive, time-consuming and error-prone process. Recent works have been reported to characterize the matching property of femtofarad and sub-femtofarad capacitor design [4][5], however these characterizations are highly structure dependent and are not built into electronic design automation (EDA) tools available to circuit designers to use. Second, metal-oxide-metal capacitors are custom designed using metal layer wires and their coupling through the oxide layers to form the capacitance. Current physical verification tools like Calibre treat this as device interconnect. Circuit extraction tools simply ignore custom designed MOM capacitors or just treat as parasitics. Lack of layout-verse-schematic (LVS) and accurate characterization support for custom designed MOM capacitors causes a distraction of the standard EDA design flow, and can cause and have caused both the functional and performance failure of SAR-ADCs.

We have developed PCAST, a **P**ractical **C**apacitor **A**rray **S**ynthesizer **T**argeted for SAR-ADC implementation. Starting from a design specification, PCAST automatically generates a layout in GDSII, a device symbol and associated kits for LVS, accurate parasitic characterization, and mismatch characterization. This provides a complete EDA support for MOM capacitor synthesis and verification. Developed in SKILL®, PCAST has been seamlessly integrated to the industry standard circuit design environment. Furthermore, PCAST can be easily customized by circuit designers and supports a variety of practical design constraints such as adding dummy and redundancy [6] for manufacturability. In addition, PCAST supports the automated generation of bit weight capacitor arrays embedding bit reference capacitors [7]. PCAST has been deployed in production for several successful SAR-ADC designs in the process nodes from 180nm, 65nm down to 28nm CMOS, as well as 14nm FinFET SOI and 16nm FinFET CMOS. To the authors' best knowledge, PCAST is the first practical capacitor array synthesizer for SAR-ADCs.

This thesis is organized as follows: Chapter 2 briefly reviews the design constraints and related works. Chapter 3 provides an overview of PCAST. Chapter 4 discusses the generations of unit capacitors. Bit capacitor array generation are discussed in Chapter 5. Experiment results are provided in Chapter 6. Chapter 7 concludes this thesis.

Chapter 2

BACKGROUND

2.1 SAR-ADC

An analog-to-digital converter (ADC) with more than 10-bit accuracy operating at tens of megahertz has been the territory of CMOS successive approximation register (SAR) architectures [8]. SAR-ADC has always been an appealing architecture in ADC design due to its low power consumption and relatively simple structure.

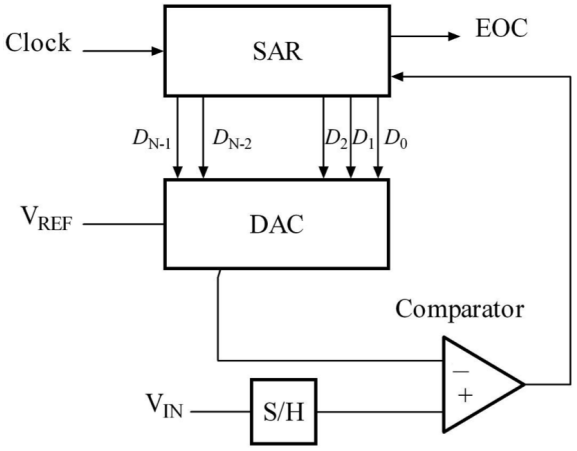


Figure 2.1: Block diagram of SAR-ADC architecture.

SAR-ADC was initially proposed by JL McCreary in 1975 [9]. Since then the overall architecture of SAR-ADC has not changed significantly. Figure 2.1 shows the structure of the SAR-ADC. It contains four sub-blocks: sample and hold (S/H), digital-to-analog conversion (DAC), comparator, and SAR logic. S/H acquires input voltage and keeps it constant during the conversion. The two inputs of the comparator are the output of the S/H circuit and the output of DAC. SAR logic generates control signals for switch/comparator and input code to DAC.

Commonly, the signal-to-(noise+ distortion) ratio (SNDR), the effective number of bits (ENOB), and the figure of merit (FOM) are the key metrics to analyze the performance of an ADC. SNDR measures the ratio of the signal power to the total noise and harmonic power at the output, given a sinusoid input signal. It is defined as (2.1).

$$SNDR_{ideal}(dB) = 10 * log_{10}(\frac{P_s}{N_q}) = 6.02 * N + 1.76(dB) \tag{2.1}$$

P_s denotes the ideal sine wave power, and N_q is the ideal quantization noise power. N denotes the resolution of the SAR-ADC.

The effective number of bits (ENOB) is defined as:

$$ENOB = \frac{SNDR_{real} - 1.76}{6.02} \tag{2.2}$$

The figure of merit (FOM) normalizes the power consumption by the sampling frequency and effective resolution [10].

$$FOM_w = \frac{P}{f_s * 2^{ENOB}}(J/converstion\_steps) \tag{2.3}$$

where P is the power consumption of each conversion. f_s denotes the sampling frequency. $ENOB$ is the effective number of bits, which is calculated in equation (2.2).

Fig. 2.2 presents the energy per Nyquist sample versus SNDR of the state-of-art ADCs [2]. Data are adopted from [11]. SAR-ADC is preferable architecture for low-power design. However, SAR-ADC suffers from limited conversion speed. Various strategies are explored to improve the conversion speed. Since this thesis concentrates on generating the capacitor array layout, we only introduce the methods that related to the capacitor array.

The redundant capacitor was first introduced in [6] to improve the conversion speed of the SAR-ADC and improve the tolerance of the settling errors. Adding redundant bits would allow the bit error correction in the early stage. Our capacitor array synthesizer supports both binary radix weighting and non-binary radix weighting [12].

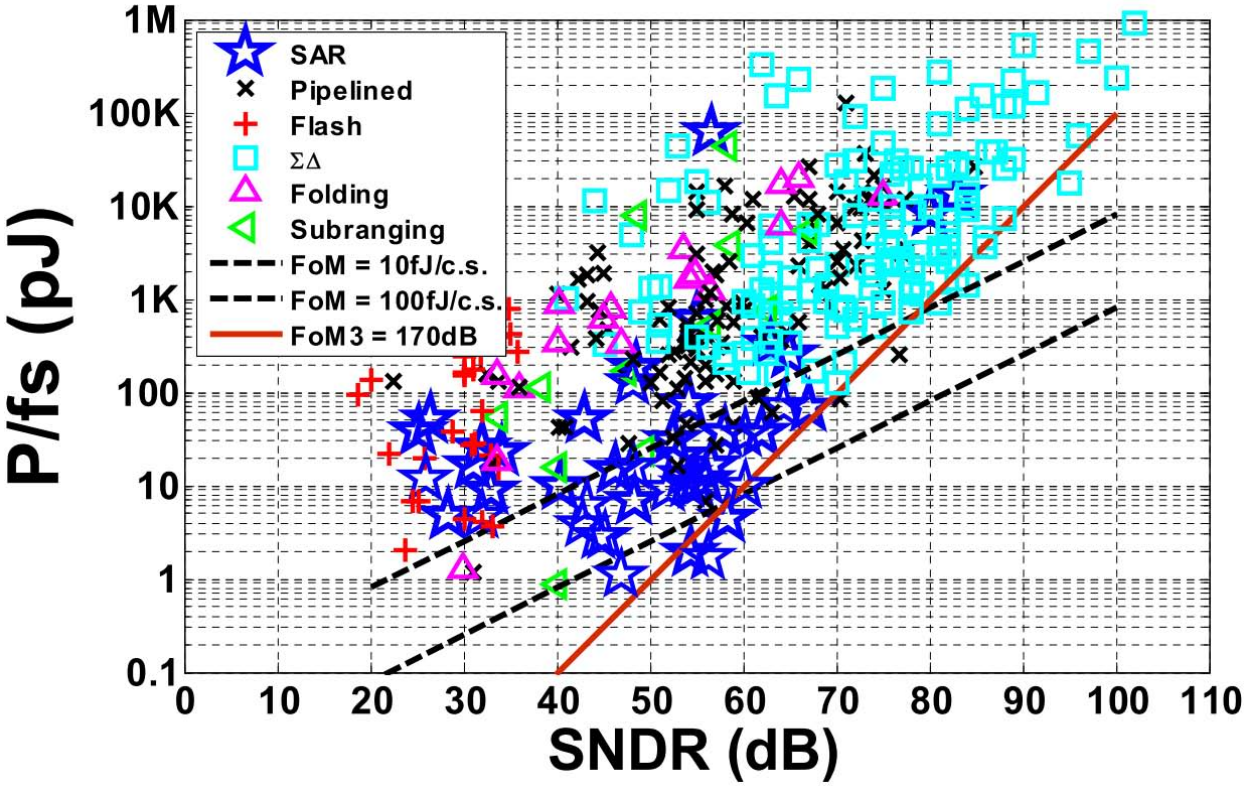


Figure 2.2: Energy per Nyquist samples versus SNDR of the state-of-art ADCs.

2.2 Capacitor Array Synthesizer

The linearity of the SAR-ADCs relies on precisely matched devices and correct capacitor ratios. In high-speed SAR-ADC design, mismatched capacitor ratio is considered to be a major contributor to loss of effective number of bits (ENOB) [13] [14] [9] [15].

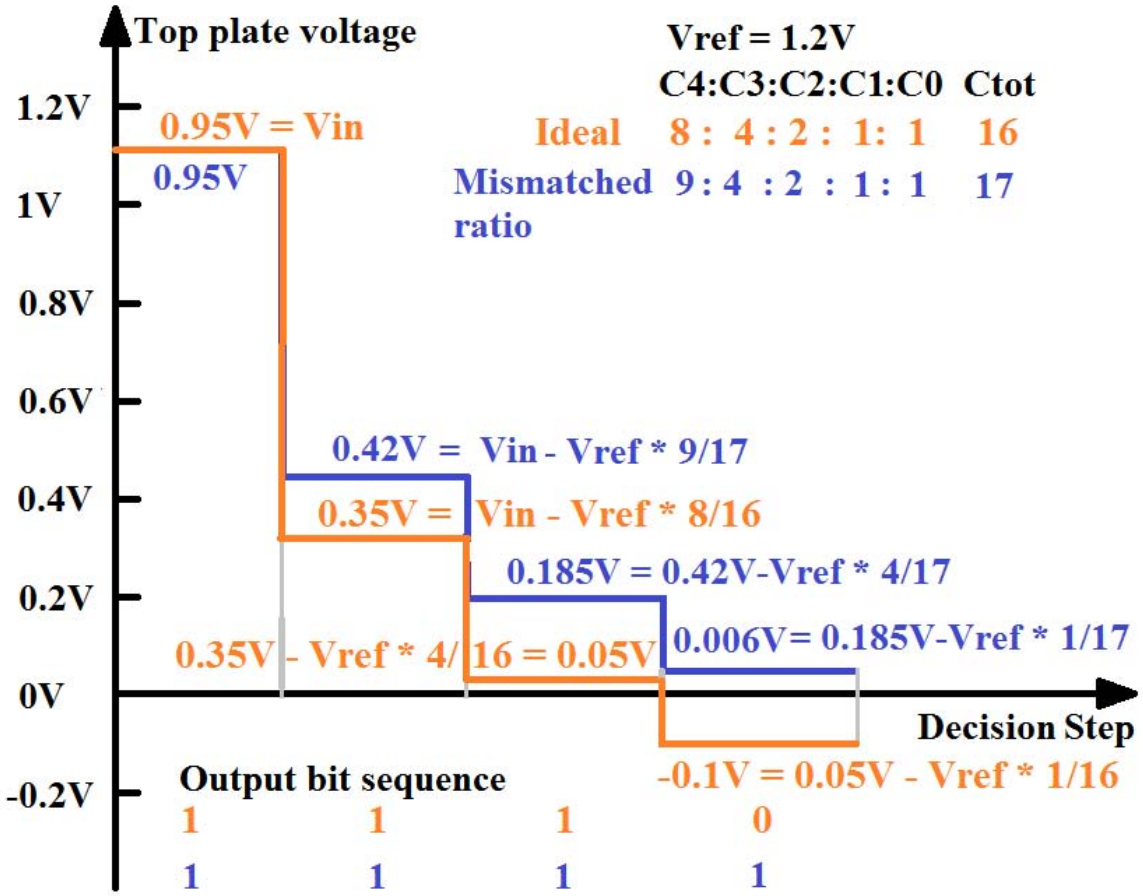


Figure 2.3: Binary search algorithm.

Currently, the designer needs to manually layout the capacitor array. There are two potential issues. Firstly, It is hard to ensure the ratio of between different bits of the ADC matched in a manual layout. Secondly, it is difficult to verify thousands of connections. Shown in Fig. 2.3, a 4-bit CDAC example is used to explain why matching capacitance ratio is essential, and how it

contributes to the generation of accurate analog voltage. Supposed we have an ideal 1.2V V_{ref}. The input voltage (V_{in}) is 0.95V. The ideal case is shown in orange, the ratio between different bits is 2. The top plate voltage of the decision step x depends on the top plate voltage from the step $x-1$ and the ratio of C_x divides the total capacitance. If the top plate voltage is higher than 0V, we obtain a logic 1 for bit x. Otherwise, we have a logic 0. If the ratio between different bits is no longer 2, letâĂŹs say instead of the capacitor ratio of [8:4:2:1:1], we have [9:4:2:1:1]. The case is displayed in Blue. For each step, the top plate voltage is higher than the one for the ideal case in orange. The error is accumulated, which leads to the error in the last step. For the last step, the top plate voltage is higher than 0V, instead of the expected -0.1V. This change brings a logic 0 instead of the expected logic 1. To sum up, the mismatched capacitor ratio will bring performance degradation in an SAR-ADC.

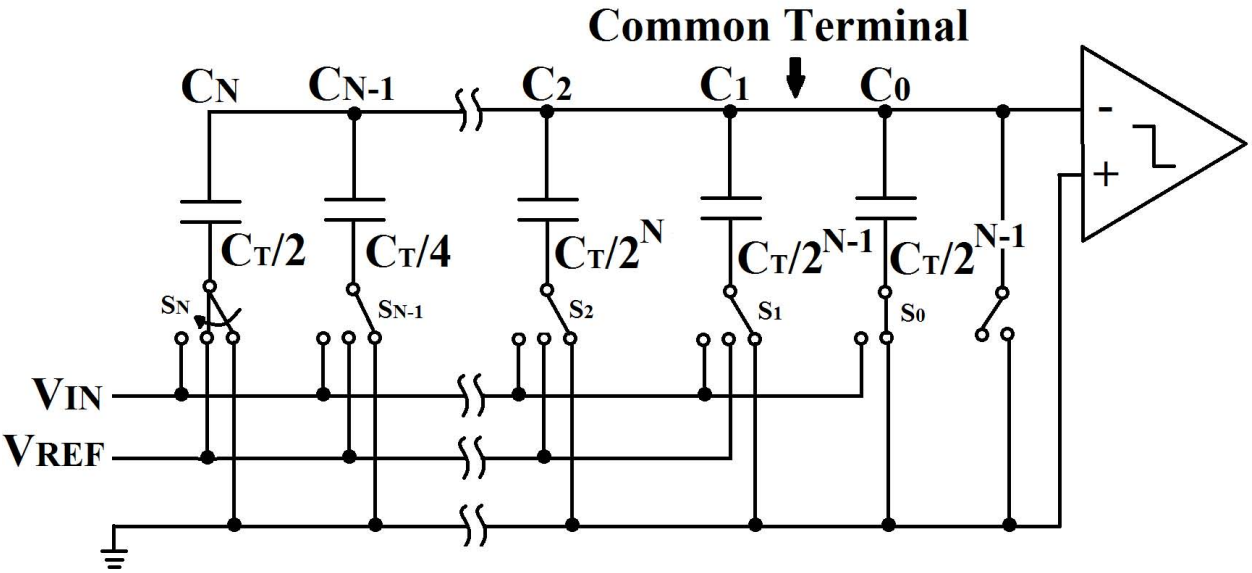


Figure 2.4: The capacitor array in SAR-ADC.

A further quantification of the relationship between the mismatched capacitance ratio SAR-ADC performance is carried out with the most significant bit (MSB). In an N-bit CDAC, the total capacitance is $C_T = 2^N \cdot C_u$, where C_u is the unit capacitance. Shown in the Fig. 2.4, all top plates

of the unit capacitors are connected together, and labeled as the common terminal. Before the conversion stage starts, the common terminal acquires the V_{in}, and all bottom plates connected to the ground. Thus the charge before the conversion is

$$Q_{before} = 2^N \cdot C_u \cdot (-V_{in} - 0) = -2^N \cdot C_u \cdot V_{in} \tag{2.4}$$

During the first conversion step, the bottom plate of the MSB C_N is switched from the ground to V_{ref}, and all other bottom plates are connected to the ground. Thus the charge after the first conversion is $Q_{after} = Q_{MSB} + Q_{C_{N-1} \cdots C_0}$. For the ideal case, the capacitance ratio between different bits of the ADC is 2. Thus

$$\begin{aligned} Q_{after\_Ideal} &= (2^{N-1} \cdot C_u) \cdot (V'_{in} - V_{ref}) + (2^{N-1} \cdot C_u) \cdot (V'_{in} - 0) \\ &= (2^N \cdot C_u) \cdot V'_{in} + (2^{N-1} \cdot C_u) \cdot (-V_{ref}) \end{aligned} \tag{2.5}$$

Due to the charge conservation,

$$\begin{aligned} Q_{before} &= Q_{after} \\ -2^N \cdot C_u \cdot V_{in} &= (2^N \cdot C_u) \cdot (V'_{in} - \frac{1}{2} V_{ref}) \\ -V_{in} &= V'_{in} - \frac{1}{2} V_{ref} \end{aligned} \tag{2.6}$$

Thus in the ideal case, the top plate voltage after the first conversion V'_{in} is

$$V'_{in} = -V_{in} + \frac{1}{2} V_{ref} \tag{2.7}$$

Assume a δ is added into the MSB to represent the mismatched capacitance ratio. The charge after the first conversion is

$$\begin{aligned} Q_{after\_Real} &= (2^{N-1} \cdot C_u + \delta) \cdot (V'_{in} - V_{ref}) + (2^{N-1} \cdot C_u) \cdot (V'_{in} - 0) \\ &= (2^N \cdot C_u + \delta) \cdot V'_{in} + (2^{N-1} \cdot C_u + \delta) \cdot (-V_{ref}) \\ &= (2^N \cdot C_u) \cdot (V'_{in} - \frac{1}{2} V_{ref}) + \delta \cdot (V'_{in} - V_{ref}) \end{aligned} \tag{2.8}$$

where δ denotes the mismatch of the MSB, V'_{in} is the voltage of the common terminal after the first conversion, V_{in} denotes the input voltage, and V_{ref} is the reference voltage.

Due to the charge conservation,

$$\begin{aligned} Q_{before} &= Q_{after\_Real} \\ -2^N \cdot C_u \cdot V_{in} &= (2^N \cdot C_u) \cdot (V'_{in} - \frac{1}{2}V_{ref}) + \delta \cdot (V'_{in} - V_{ref}) \\ -V_{in} &= (V'_{in} - \frac{1}{2}V_{ref}) + \frac{\delta}{2^N \cdot C_u} \cdot (V'_{in} - V_{ref}) \end{aligned} \tag{2.9}$$

Thus V'_{in} can characterized as

$$\begin{aligned} V'_{in} \cdot (1 + \frac{\delta}{2^N \cdot C_u}) &= \Big(-V_{in} + \frac{1}{2}V_{ref} \Big) + V_{ref} \cdot (\frac{\delta}{2^N \cdot C_u}) \\ V'_{in} \cdot \frac{2^N \cdot C_u + \delta}{2^N \cdot C_u} &= \Big(-V_{in} + \frac{1}{2}V_{ref} \Big) + V_{ref} \cdot (\frac{\delta}{2^N \cdot C_u}) \\ V'_{in} &= (-V_{in} + \frac{1}{2}V_{ref}) \cdot \frac{2^N \cdot C_u}{2^N \cdot C_u + \delta} + \frac{\delta}{2^N \cdot C_u + \delta} V_{ref} \\ &= (-V_{in} + \frac{1}{2}V_{ref}) \cdot \frac{C_T}{C_T + \delta} + \frac{\delta}{C_T + \delta} V_{ref} \end{aligned} \tag{2.10}$$

where C_T is the total capacitance, and C_u is the unit capacitance.

Compared Equation (2.7) and Equation (2.10), even at δ is 1% in C_u, V'_{in} can be degraded by 0.004% if size of the ADC is 10 bit, V_{ref} is 1.2V, and V_{in} is 0.95V. In this case, one LSB is $V_{ref}/2^N = 1.2V/2^{10}$. In another word, the degradation introduced by 1% standard deviation in C_u is roughly 1% of one LSB. This error can be accumulated to the last bit. Combined with Equation 2.2, 1% mismatch of the unit capacitor brings no less than 1 bit loss in ENOB [2]. Therefore, for a high-resolution SAR-ADC design, it is essential to calibrate the mismatches in capacitors for the performance of the ADC.

The synthesis of the layout of regular structures with symmetry and matching constraints was an area of active research. Mar et al. implemented a placement flow that simultaneously handles symmetry and matching constraints [16]. In CAD community, there is a number of existing works that specifically address placement and routing of the capacitor array in SAR-ADCs under process variations modeled by linear oxide gradient [17] [18] [19] [20].

Aforementioned works [17] [18] [19] [20] all make the following fundamental assumptions: systematic process variation of the capacitor array can be modeled by linear oxide gradient [21] of

the MOS capacitors. However, in newer SAR-ADC designs, metal-oxide-metal (MOM) capacitor has become prevalent in recent SAR-ADC designs [6] due to (1) the capacitance of the MOM capacitor is way lower than what the MOS capacitor can support. Significant power reduction is enabled by using the sandwiched-like metal structure as a capacitor; (2) MOM capacitor has relative loose layout design rules, good matching characteristics, and low parasitic capacitance [22]. The gradient of oxide thickness only marginally impacts the matching performance of MOM capacitors [23]. For this reason, the proposed methods in the aforementioned works are arguably less relevant in modern SAR-ADC designs. PCAST does not explicitly consider process variation in array placement and routing.

Furthermore, the previous works [17] [18] [19] [20] focus on the algorithmic aspects of placement and routing to optimize certain criteria, but do not actually synthesize a layout. These research approaches try to solve universal sizing problems in all analog circuits but pay less attention to passive components in integrated circuits, like capacitors. Furthermore, these tools do not allow the integration of designers knowledge, which adds a heavy cost when introducing a new task.

In contrast, a paramount design consideration of PCAST is to ensure the tool can be integrated with circuit design software. The resulted capacitor array layout from PCAST can be easily deployed in an SAR-ADC design project. A key advantage of PCAST over previous works is that PCAST can be seamlessly integrated with circuit design software, while the tools reported in previous works cannot be deployed in real-world circuit design projects.

Chapter 3

OVERVIEW OF PROPOSED METHODOLOGY

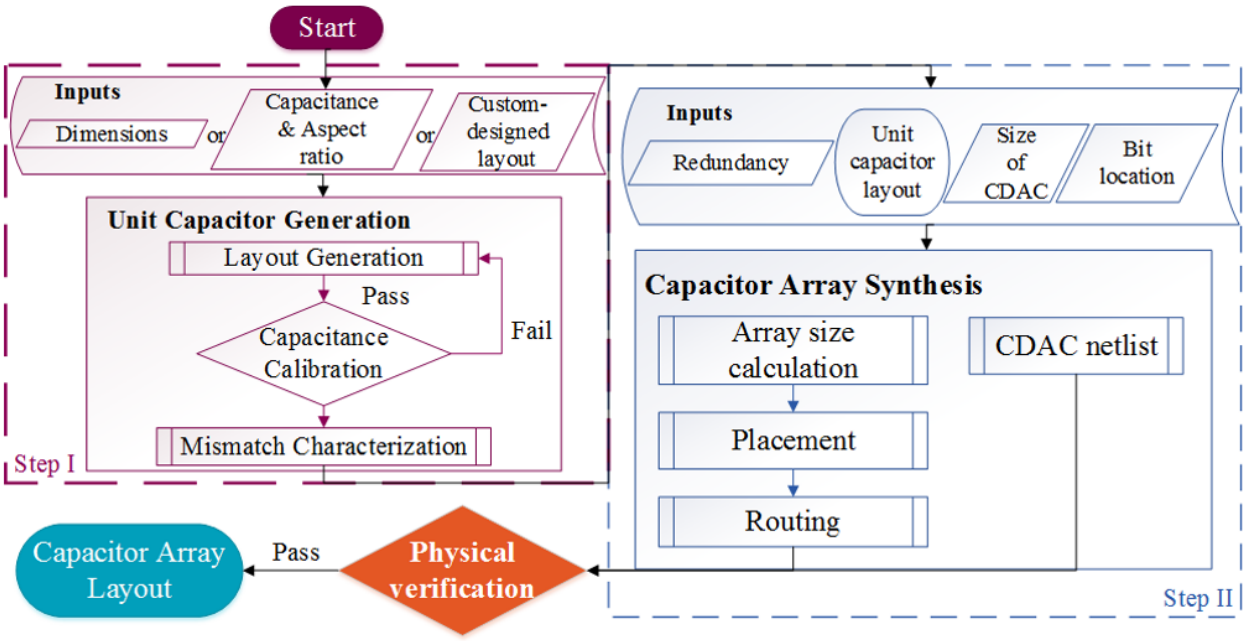


Figure 3.1: Flow diagram of the capacitor array synthesizer.

The overall flow diagram of PCAST is shown in Figure 3.1. There are two steps in capacitor array synthesis: (I) unit capacitor layout generation, followed by (II) capacitor array layout synthesis. In Step I, the user can specify the properties of the unit capacitor by providing the dimensions of the unit capacitor, or the desired capacitance value and aspect ratio, or a custom designed unit capacitor layout. In this step, PCAST also invokes a capacitance extraction tool to calibrate and characterize the capacitance of the unit capacitor. Capacitance mismatch is also characterized.

With the layout of the unit capacitor, in Step II PCAST performs placement and routing to synthesize the capacitor array layout. A netlist of the capacitor array is also synthesized in this step

to facilitate design simulation and verification. The synthesized capacitor array layout is validated by physical verification tools, such as Mentor Graphics Calibre®. A symbol is automatically generated for the LVS check.

Chapter 4

UNIT CAPACITOR GENERATION

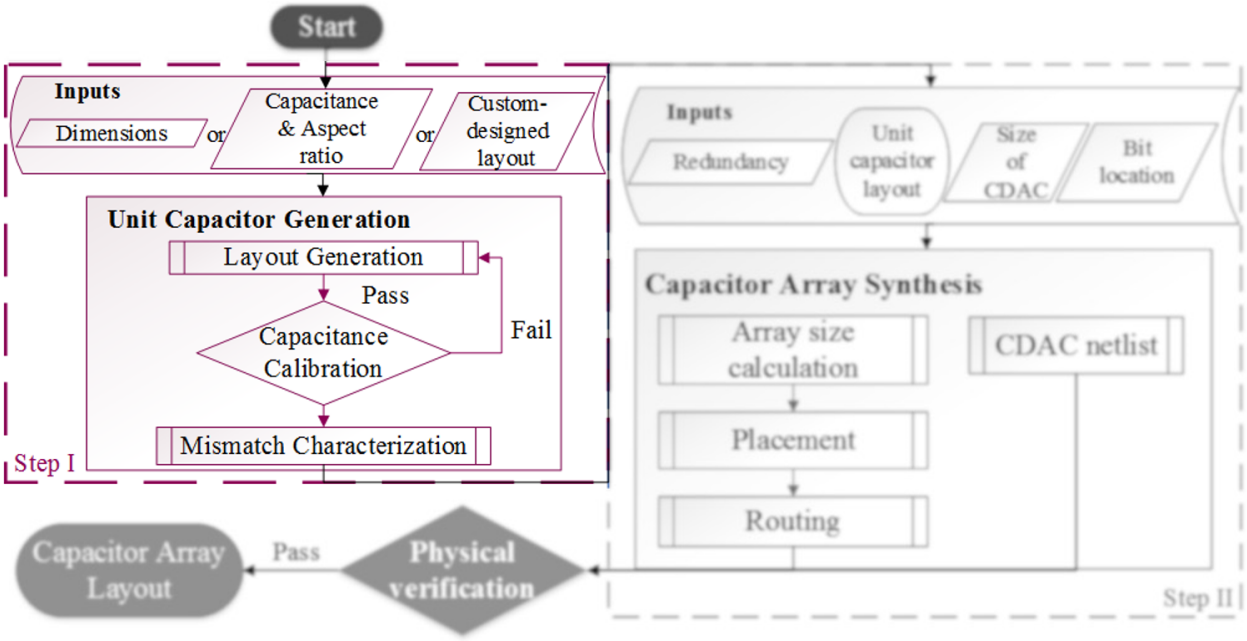
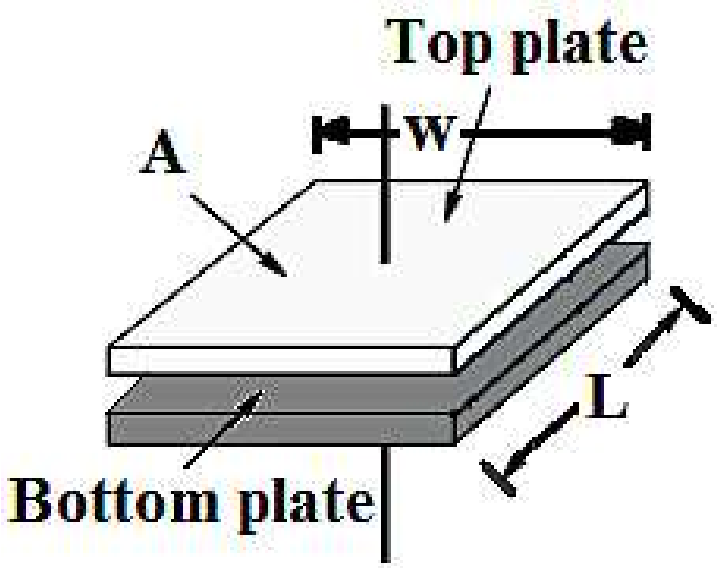


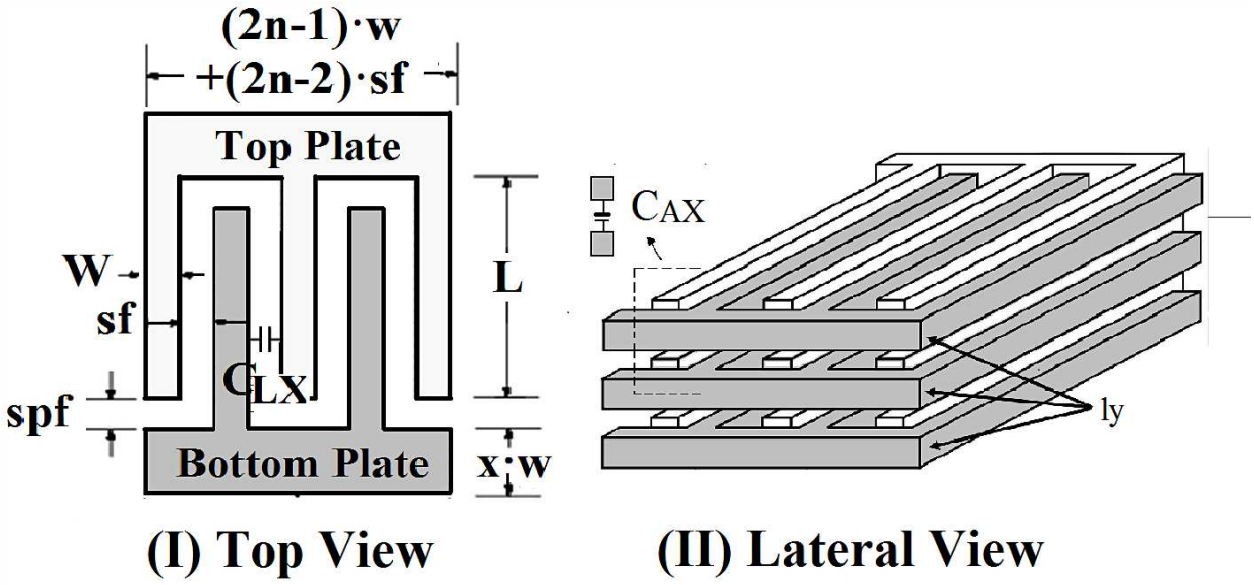
Figure 4.1: Unit capacitor generator.

The unit capacitor is the basic building block of the capacitor array. To generate the unit capacitor layout, the user could either specify the dimensions of the unit capacitor or provide the desired capacitance of the unit capacitor and aspect ratio, or simply a predefined unit capacitor layout.

Figure 4.2 shows the full list of required parameters to define the dimensions of a unit capacitor. Given the dimensions of a unit capacitor, PCAST interacts with Cadence Layout Editor® to create the unit capacitor layout through the SKILL® scripting interface. By default, PCAST supports the generation of parallel plate MOM capacitors (HPP) and interdigitated MOM capacitors (VPP) [4].



(a) Parallel plate capacitor (HPP).



(b) Interdigitated capacitor (VPP).

Figure 4.2: Mental capacitor structures.

Table 4.1: Capacitor Structures Comparison.

Capacitance Structure	Advantage	Disadvantage
HPP	1) Easy to design 2) Higher breakdown voltage	1) Higher bottom plate capacitance 2) Lower self-resonance frequencies 3) Lower quality factor
VPP	1) Lower bottom plate capacitance 2) Higher self-resonance frequencies 3) Higher quality factor	1) Difficult to predict the absolute value 2) Lower breakdown voltage

Table 4.1 compares these two default capacitor structures. In a 16nm CMOS process, PCAST utilizes higher metal layers (M4-M12) to minimize mismatch, at the cost of lower capacitative density due to the increased area. Alternatively, the user could provide a custom-designed unit capacitor layout. In this case, PCAST will bypass the unit capacitor generation stage.

4.1 Metal-Oxide-Metal Capacitor Structures

4.1.1 Parallel Plate Capacitor (HPP)

A standard HPP structure is shown in 4.2(a). The set of dimensions to define the HPP is listed in table 4.2. Two parallel metal plates are separated by a dielectric with permittivity ε. The capacitance can be estimated as

$$C_{HPP} = \frac{\varepsilon A_T}{d} = \frac{\varepsilon \cdot (wL)}{d} = \frac{\varepsilon K_{HPP} L^2}{d} \tag{4.1}$$

where d is the distance between two plates, A_T is the area of plates, $w(L)$ is the width(length) of the plates, and K_{HPP} denotes the desired aspect ratio.

Table 4.2: The required parameters to define the dimension of the HPP.

Parameter	**Description**
C_{HPP}	The desired capacitance
K_{HPP}	The desired aspect ratio
A_T	The area of the plates
w	The width of the plate
L	The length of the plate
ε	Permittivity
d	The distance between two plates

4.1.2 Interdigitated Capacitor (VPP)

Metal interconnections are used to realize the capacitance. Table 4.3 shows the set of dimensions to define the VPP. An interdigitated MOM capacitor consists of two comb-like metal plates (top plate and bottom plate). As shown in Figure 4.2(b), the comb teeth portions of the metal plates, or the "fingers", are arranged in an interleaving pattern to form the unit capacitor. See Table 4.3 for the set of dimensions that defined the VPP.

The capacitance between the fingers on the same layer is

$$C_{lateral} = L \cdot (2n-2) \cdot C_{LX} \tag{4.2}$$

where $L(w)$ is the length(width) of the fingers, n denotes the number of interdigitated p^+-fingers, and C_{LX} is the lateral capacitance per unit length.

Multiple metal layers can be stacked vertically to increase the capacitance density, as shown in Figure 4.2(b). Define the total interlayer capacitance $C_{vertical}$ to be

$$C_{vertical} = \frac{C_{AX}}{wL \cdot t_m} \cdot A_L \cdot (ly-1) \tag{4.3}$$

$$A_L = \left(2 \cdot W_{plate} \cdot L_{plate} + (2n-1) \cdot wL\right) \cdot t_m \tag{4.4}$$

Table 4.3: The required parameters to define the dimension of the VPP.

Parameter	**Description**
C_{VPP}	The desired capacitance
K_{VPP}	The desired aspect ratio
w	The width of the fingers
L	The length of the fingers
n	The number of interdigitated p^+-fingers
sf/spf	The space between fingers, and at the end plates
x	The ratio between the width of fingers and the height of plates
ly	The number of metal layers
t_m	The oxide thickness between adjacent metal layers
C_{LX}	The lateral capacitance
C_{AX}	The fringe capacitance

$$W_{plate} = (2n-1)\cdot w + (2n-2)\cdot sf \tag{4.5}$$

$$L_{plate} = x \cdot w \tag{4.6}$$

where W_{plate} is the width of plates, L_{plate} is the height of plates, A_L is the lateral area, sf denotes the finger spacing, ly is the number of metal layers, t_m is the oxide thickness between adjacent metal layers, and C_{AX} denotes the fringe capacitance.

The total capacitance of interdigitated capacitor (VPP) is

$$C_{VPP} = C_{lateral} + C_{vertical} \tag{4.7}$$

To obtain more accurate capacitance in this structure, the correction procedure performs the C_{LX} and the C_{AX} extractions before each calibration. In PCAST, a combination of test structures is used to extract the coefficients for all the parasitic capacitance effects. During the C_{LX} extraction, two adjacent fingers are placed. The C_{AX} extraction works on the edge-to-surface capacitance between two overlapping fingers on different metal layers. The capacitance is defined by C_{LX}, and it scales with the length L, the width w, the finger number n, and the finger spacing sf.

4.2 Unit Capacitor Layout Generation

In case the user chooses to provide the desired unit capacitance and aspect ratio instead of detailed metal plate dimensions, PCAST drives the capacitor dimensions and generates a unit capacitor layout, as shown in Algorithm 1.

The relationship between the lateral area A_L and the capacitance C can be roughly characterized by Equation (4.1) and (4.7). In Algorithm 1, a binary search procedure is employed to further refine the estimated A_L. Due to the quasi-convexity of the mapping from A_L to C, the binary search procedure in Algorithm 1 is valid and efficient in identifying the optimal achievable A_L given the desired C and aspect ratio K.

Algorithm 1 starts with an initial estimation of the lateral area A_{init}. Given a specific lateral area A_L, the next step is to identify the dimensions of the unit capacitor (see Figure 4.2). This is trivial for HPP where $L = \sqrt{A_T/K},\ w = \sqrt{A_T K}$. In the case of VPP, let $D_{VPP} = \{w, L, n, sf, x\}$

Algorithm 1 Unit Capacitor Generation

procedure UNITCAPGEN (C, K)
  Get initial estimate of lateral area $A_{L,init}$
  $D_{init} \leftarrow \text{SMT}(A_{L,init}, K)$ (VPP only)
  $C_{init} \leftarrow \text{Extract}(D_{init})$
  if $C_{init} < C$ **then**
    $A_{L,low} \leftarrow A_{L,init}$, $A_{L,high} \leftarrow 2 \cdot A_{L,init}$
  else
    $A_{L,low} \leftarrow 0.5 \cdot A_{L,init}$, $A_{L,high} \leftarrow A_{L,init}$
  while $|C' - C| > \varepsilon$ & max iteration not reached **do**
    $A_{L,mid} \leftarrow 0.5 \cdot (A_{L,low} + A_{L,high})$
    $D \leftarrow \text{SMT}(A_{l,mid}, K)$ (VPP only)
    $C' \leftarrow \text{Extract}(D)$
    if $C' < C$ **then**
      $A_{L,low} \leftarrow A_{L,mid}$
    else
      $A_{L,high} \leftarrow A_{L,mid}$

denotes the set of dimensions that defines the structure of the HPP, as shown in Figure 4.2(b). The relationship between A_L and D_{VPP} can be described by Equation (4.8). The SMT subroutine in Algorithm 1 takes A_L and K_{VPP} as inputs. A satisfiability modulo theories (SMT) solver Z3 [24] identifies a set of dimensions D_{VPP} that satisfies Equation (4.8), while minimizing the area.

$$\begin{aligned}\Big(K_{VPP}\cdot(1\pm 1\%) == \frac{(2n+1)\cdot w+2n\cdot sf}{L+sf+2\cdot xw}\Big)\wedge\Big(Eqn(4.4)\Big)\wedge\Big(n\in\mathbb{Z}^{+}\Big)\\ \wedge\Big(sf\geq s_{min}\Big)\wedge\Big(L\geq m_{min}\cdot(x+1)\Big)\wedge\Big(w\geq max(m_{min},v_{min}/x)\Big)\end{aligned} \tag{4.8}$$

where m_{min} is the minimum metal width, s_{min} denotes the minimum metal to metal spacing, and v_{min} is the minimum width of via.

With the dimensions of the unit capacitor computed, the Extract subroutine in Algorithm 1 generates the unit capacitor. The effective capacitance C' of the resulted layout is extracted using Calibre PEX®. The C' is considered to be accurate, and will be used to further refine A_L, so the capacitance of the generated layout is close to the desired capacitance. If the difference between C' and C is within $10\%\cdot C$, the length L and the width w will be modified. Otherwise, the finger number n will be adjusted.

Table 4.4 shows the simulated unit capacitance, dimensions of the unit capacitor, and area for each capacitor structures. The same 0.18 μm CMOS process is used as in [4]. Set H and Set V have three different capacitance values, namely, 2fF, 1fF, and 0.5fF. Set H has three HPPs that shown in Figure 4.2(a). The plate length L varies. Three VPPs (Figure 4.2(b)) are shown in Set V, where the finger length "L" varies, while keeping the finger width w, the finger spacing sf, the ratio between the width of the fingers and the height of plates x, and finger number n constant.

4.3 Mismatch Characterization

The mismatch in unit capacitors due to process variation affects the linearity of an SAR-ADC [5]. In PCAST, we adopt the techniques in [4][5] to estimate the mismatch of generated capacitor structures. The mismatch of unit capacitors follows Pelgrom's mismatch model [4].

For HPP, the top area is the effective capacitance area, thus Pelgrom's relation can be described

Table 4.4: Simulated unit capacitor value, dimensions, and area.

	Type	**Unit Cap (C) (fF)**	**Metal Usage**	**L** (μm)	**W** (μm)	**sf/spf** (μm)	**x**	**n**	A_t (μm^2)	A_l (μm^2)
H1	**HPP**	2	M4-M5	6.25	6.25	-	-	-	39.06	-
H2		1	M4-M5	4.15	4.15	-	-	-	17.22	-
H3		0.5	M4-M5	2.66	2.66	-	-	-	7.076	-
V1	**VPP**	2	M5	10.19	0.36	0.32	1	2	19.32	17.65
V2		1	M5	4.92	0.36	0.32	1	2	10.25	5.88
V3		0.5	M5	2.29	0.36	0.32	1	2	5.73	3.65

with $\kappa_{A,T}$.

$$\sigma(\frac{\Delta C}{C}) = \frac{\kappa_{A,T}}{\sqrt{A_T}} \tag{4.9}$$

If the effective area is the lateral area, the Pelgrom's mismatch model is

$$\sigma(\frac{\Delta C}{C}) = \frac{\kappa_{A,L}}{\sqrt{A_L}} \tag{4.10}$$

For VPP, the capacitance depends on both A_L and A_T, thus both $\kappa_{A,T}$ and $\kappa_{A,L}$ can be applied.

For both HPP and VPP, the capacitance is proportional to the area. Thus

$$\sigma(\frac{\Delta C}{C}) = \frac{\kappa_C}{\sqrt{C}} \tag{4.11}$$

where $\kappa_{A,top}$, $\kappa_{A,lateral}$, and κ_C are Pelgrom's coefficients.

The Pelgrom's coefficient κ_C can be estimated using experimental data, as shown in Fig. 4.3. Table 4.5 shows the extracted unit capacitance, $\sigma(\Delta C/C)$, area, the fitted Pelgrom's coefficients for each capacitor structure, and chacterizated mismatch. The same 0.18 μm CMOS process is used as in [4]. The experimental results in regards to $\sigma(\Delta C/C)$ matches the prediction of Equation 4.9, Equation 4.10, and Equation 4.11. For HPP, the top area is the effective capacitance area, thus Pelgrom's relation can be described with $\kappa_{A,T}$. For VPP, the capacitance depends on both A_L and A_T, thus both $\kappa_{A,T}$ and $\kappa_{A,L}$ can be applied.

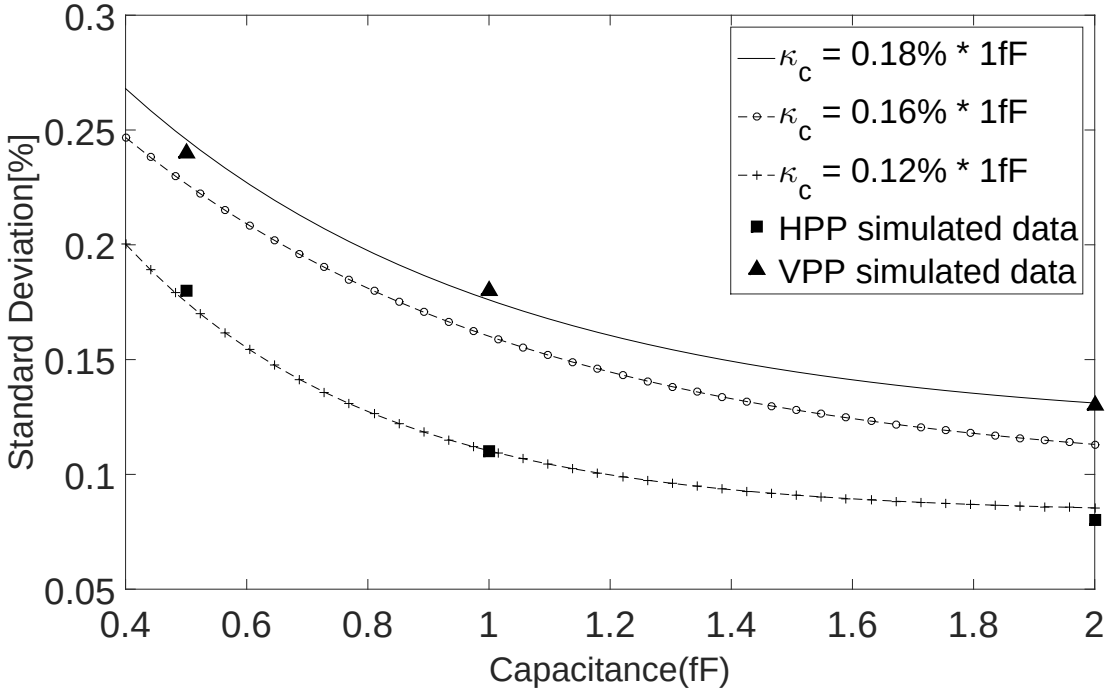


Figure 4.3: The capacitance standard deviation versus unit capacitor size. Fitted κ_C values are 0.18% $\times$ 1fF and 0.12% $\times$ 1fF for VPP and HPP respectively.

Table 4.5: Simulated unit capacitor value, σ(ΔC/C), area, and pelgrom's coefficients extracted by curve fitting

	Type	**Unit Cap (C) (fF)**	$\sigma(\frac{\Delta C}{C})$	A_t (μm^2)	A_l (μm^2)	$\kappa_{A,t}$	$\kappa_{A,l}$	κ_C
H1	**HPP**	2	0.08%	39.06	-	$0.49\% \cdot 1\mu m$	-	$0.12\% \cdot 1$fF
H2		1	0.11%	17.22	-			
H3		0.5	0.18%	7.076	-			
V1	**VPP**	2	0.13%	19.32	17.65	$0.57\% \cdot 1\ \mu m$	$0.48\% \cdot 1\mu m$	$0.18\% \cdot 1$fF
V2		1	0.18%	10.25	5.88			
V3		0.5	0.24%	5.73	3.65			

Chapter 5

CAPACITOR ARRAY SYNTHESIS

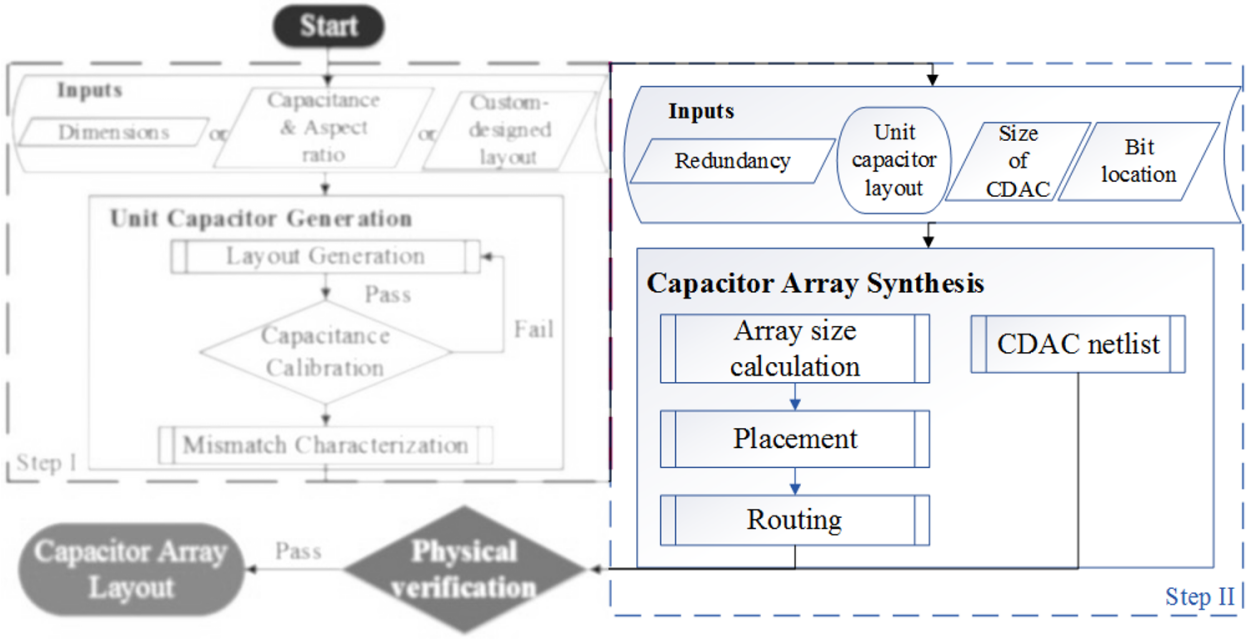


Figure 5.1: Capacitor array synthesizer.

In SAR-ADC designs, the linearity of the ADC is strongly dependent on how well the capacitor ratios are matched. Let C_1 through C_N be the effective capacitance of bit 1 through bit N, a key objective in capacitor array synthesis is to ensure C_N/C_{Total} is close to the desired value (2 for binary-weighted capacitor arrays), where C_{Total} is the total capacitance of the capacitor array. The absolute value of C_N is not as consequential as C_N/C_{Total}. A matched capacitor array ensures a good linearity of SAR-ADCs [13].

Routing parasitic capacitance accounts for a significant proportion of effective capacitance. To

the first order, wire parasitic capacitance is proportional to the length of the wire. Also, consider for each bit, the length of the routing metal is roughly commensurate with the number of unit capacitors. Thus the wire parasitic capacitance is roughly proportional to the number of unit capacitors. Ensuring the length of the routing metal is proportional to the desired capacitance is a key design consideration.

In capacitor array synthesis, the first step is unit capacitor placement, followed by creating physical connectivity using routing metals. Once the array dimensions are set, PCAST will start to route unit capacitors in term of matching the desired capacitance ratio. The wire capacitance, which is proportional to the length of wire, is also taken into considerations. The router has the capability to add extra dummy metals to achieve the desired capacitance ratio. Additionally, a netlist with accurate extracted capacitance is generated together with the layout to facilitate simulation and validation.

As shown in Fig. 5.1, the input to the procedure is the unit capacitor layout, the size of the capacitor array, the capacitor redundancy, and bit location specification. The sub-routines are discussed in details in the following sections.

5.1 Array Size Calculation

The capacitor array is a rectangular grid whose number of columns(P) and rows (Q) is determined by N (number of bits) and the aspect ratio (K_D). The supported features, such as redundant capacitors, and bit locations, would change the number of columns. Let N_{totC} denotes the total numbers of capacitor slots, where $P = Q \cdot K_D$, and $N_{totC} = P \cdot Q$.

5.2 Placement

Once we determine the array dimensions, the placement algorithms are simultaneously performed for each unit capacitor. In a binary-weighted CDAC, let bit C_K be the highest bit whose number of unit capacitors is less than the capacity of one column, thus C_{N-1} through C_{K+1} occupies no less than one column. PCAST assigns columns to bits C_{N-1} through C_{K+2} such that the layout is symmetric in respect of the middle column. As shown in Fig. 6.7, the columns of different bits are

placed in an interleaved manner.

If N (the size of capacitor array) is an odd number, the bit C_{K+1} will be assigned to the column that adjacent to the rightmost column of bit C_{N-1}. Otherwise, the bit C_{K+1} will occupy the column locates at the middle of the capacitor array.

For lower bits C_K through C_0, the user could specify whether the bit should occupy one full column (the unused slots will be filled by dummy capacitors), or multiple bits should share the same column. The default behavior is to assign at least one column to each bit.

There is weaker fringing effect for the unit capacitors on the edge of the array than those in the middle of the array [2]. To cancel out such difference, the capacitor array shall be surrounded by dummy capacitors.

An example of synthesized 5-bit capacitor array placement is shown in Figure 5.2. There are 32 unit capacitors in this design. PCAST assigns bit C_5 through C_3 symmetrically in respect of the middle column that occupies by bit C_3. Bit C_2 through C_0 takes at least one column.

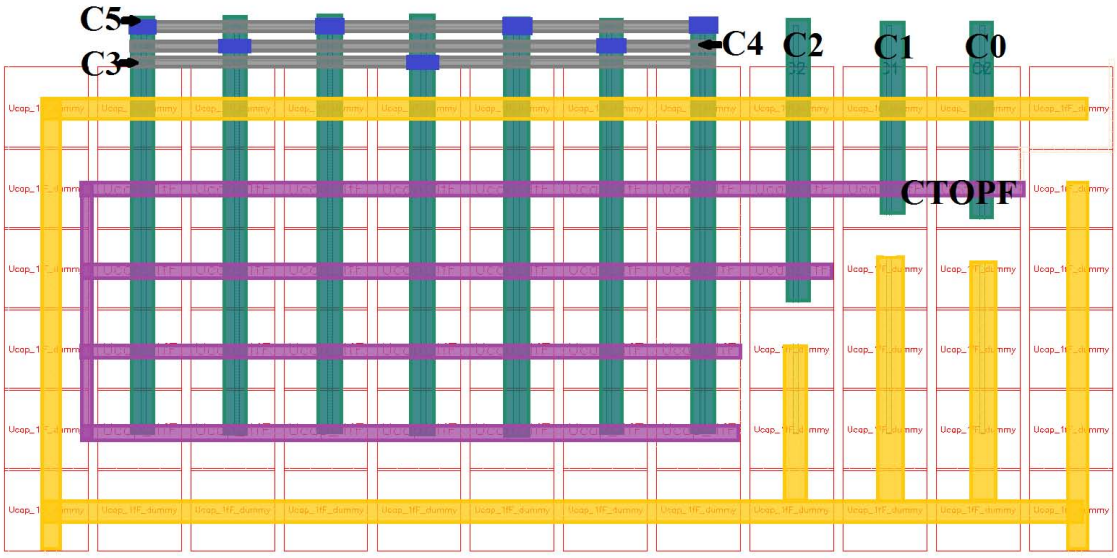


Figure 5.2: Capacitor array placement and routing.

An advanced SAR-ADC design technique is to insert redundant capacitors in the capacitor

array to reduce settling error. PCAST supports both binary radix weighting and non-binary radix weighting.

An additional bit (decision level) C_R is introduced to account for the binary weighted redundancy [6]. C_R is specified by the user. The columns that the redundant capacitor occupies can either automatically chosen by PCAST assuming the redundant capacitors are the R^{th} decision level, or be specified by the user.

In the case of non-binary weighted radix redundant capacitor, PCAST takes the user-specified the number of unit capacitors (s) in each bit as the input. Fig. 5.3 shows an example of a capacitor array with non-binary radix weighted capacitor redundancy. The user requests a CDAC of s = [8,2,2,1,1,1,1] with 3:5 aspect ratio. Due to the requested aspect ratio, $N_{totC} = P \cdot Q = 3 \times 5 \times I$ (I), where $I \in \mathbb{Z}^+$. There are 16 unit capacitors in this array. $N_{totC} = 16 + N_{DY}$ (II), where N_{DY} is the number of dummy capacitors. Each bit occupies at least one column. The leftmost and rightmost columns are dummy capacitors. Thus $P = \sum ceil(N_K/Q) + 2$ (III), where N_K is the number of unit capacitors in each bit. PCAST starts with the initial guess of I as one, and increments I by one for each iteration until Equation I to III are satisfied. For example, in Fig. 5.3, there are 16 unit capacitors and 44 dummy capacitors in this 6 by 10 array.

5.3 Routing

During the routing process, the bottom plates of the unit capacitors (and redundant capacitors if apply) are routed vertically so the capacitors of the same bits are connected together. The routing metal of bottom plate is different from the one of the top plate to avoid additional coupling capacitance that alters the value of the original capacitance ratio.

The routing direction of top plates is dependent on the existence of dummy capacitor and the radix of the redundant capacitors. PCAST connects the top plates of all the unit capacitors (and redundant capacitors if apply) to the same reference voltage. In the case of the binary weighted capacitor array, no dummy capacitor is necessary except for the dummy capacitors on the peripheral of the array. The user could specify the routing directions. Shown in Fig. 5.5(a), the routing direction of redundant capacitors is same to the one of unit capacitors.

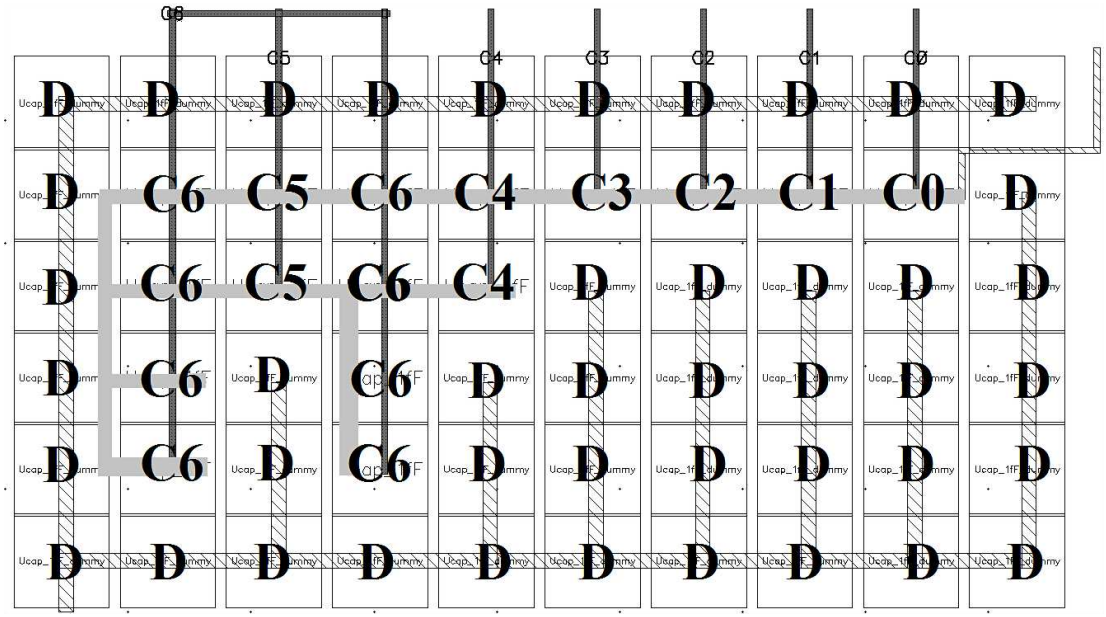


Figure 5.3: Synthesized CDAC with non-binary weighted redundancy.

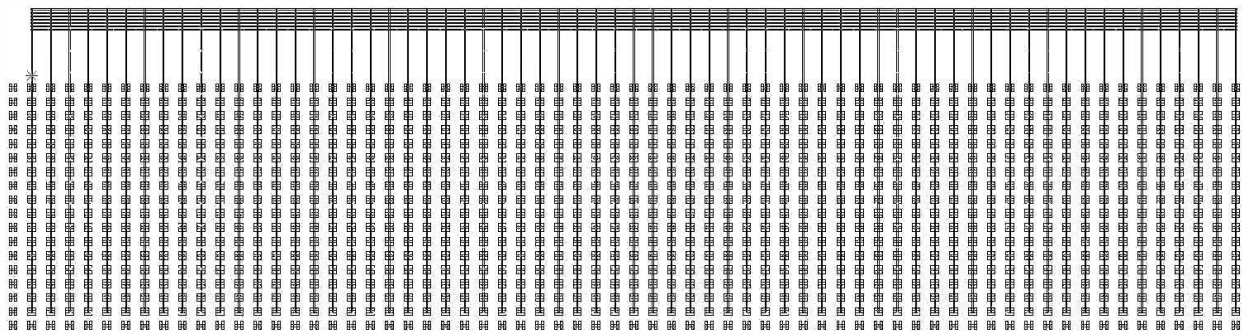
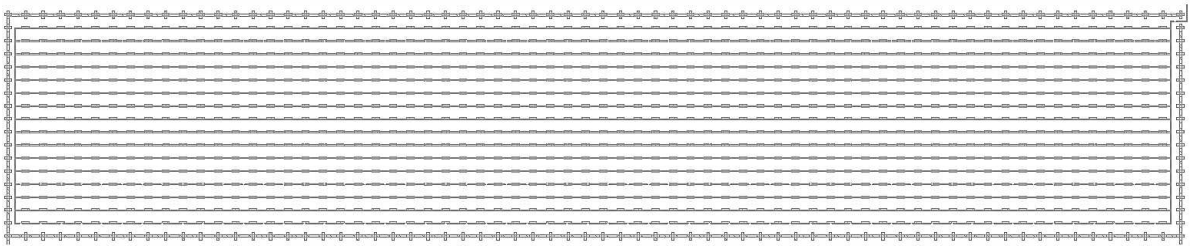
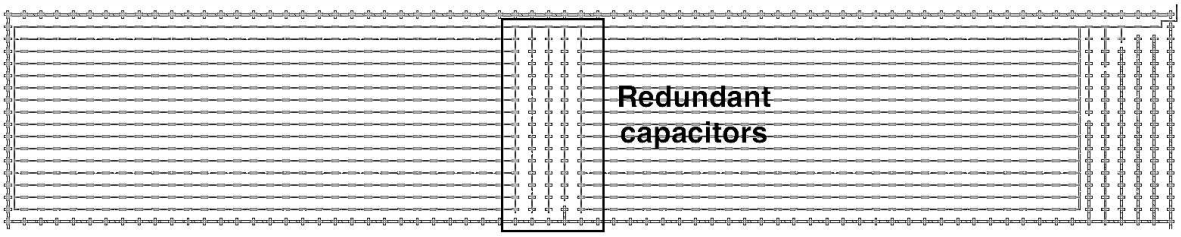


Figure 5.4: Capacitor array bottom plate connection.

In the case of the non-binary weighted capacitor array, the routing direction is chosen such that the dummy capacitors do not block the routing channel. For example, in Fig. 5.3, the top plates are routed horizontally (shown in gray), and the bottom plates are routed vertically (shown in black).



(a) With a binary radix weighted redundant bit.



(b) With a non-binary radix weighted redundant bit.

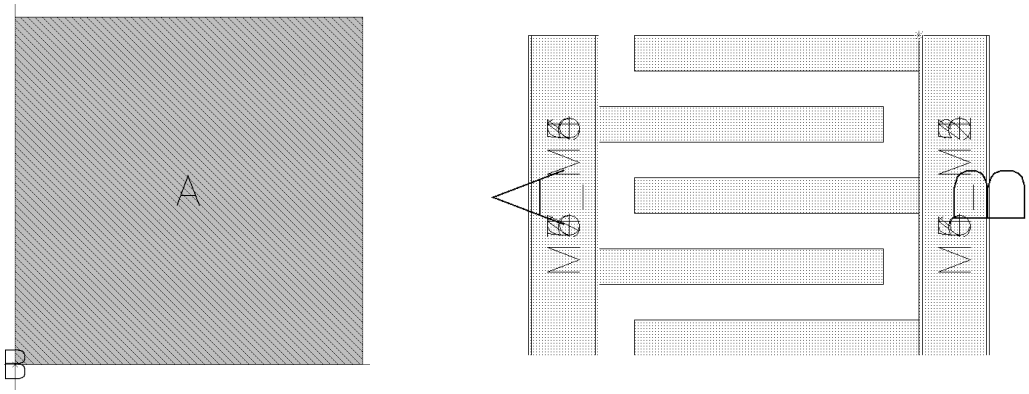
Figure 5.5: Capacitor array top plate connections.

Chapter 6

ANALYSIS AND RESULTS

6.1 Generated Layout of Unit Capacitor

Suppose the user requested the layout of a unit capacitor of 1fF in a 65nm CMOS Process. The resulted unit capacitor layouts from PCAST are shown in Figure 6.1. Figure 6.1(a) shows a generated 1fF HPP layout, with a core chip area of 2.4 μm $\times$ 2.4 μm. In Figure 6.1(b), the generated unit capacitor is a 1.03 fF interdigitated capacitor with 9:13 aspect ratio. The horizontal pitch is 0.9 μm, and the vertical pitch is 1.3 μm. The top plate, which is on the left side, includes two interdigitated p^+-fingers. Three interdigitated n^+-fingers are connected to the bottom plate. The two types of fingers (n^+ and p^+) are interleaved in an alternating pattern.



(a) HPP layout. (b) VPP layout.

Figure 6.1: Generated unit capacitor layout.

PCAST supports the layout generation in various process nodes. As an example, Figure 6.2 shows three auto-generated 0.5fF VPP unit capacitors with various required aspects ratios. Table

6.1 describes the dimensions and areas of 0.5fF VPPs in three process nodes.

Table 6.1: Statistics of 0.5fF VPPs in various processes

PDK	**Metal Usage**	**L** (μm)	**W** (μm)	**sf/spf** (μm)	**x**	**n**	A_T (μm^2)	A_L (μm^2)
28nm	M4-M6	0.336	0.07	0.05	2.2	4	0.36	0.19
65nm	M3-M6	0.4	0.1	0.1	2	3	0.56	0.45
180nm	M5	3.01	0.36	0.32	1	2	5.73	3.65

By carefully choosing the aspect ratio of the unit capacitor, one can more efficiently utilize the spacing between the unit capacitors as routing channels. Given a desired capacitance, PCAST has the flexibility to generate interdigitated capacitors with varying aspect ratios. In Figure 6.2, four auto-generated 0.5fF unit capacitors with various aspects ratios are shown.

HFSS 15.0 is used to modeling the effect of frequency on the effective capacitance. Figure 6.3 shows the simulated design of a synthesized 1.065 fF HPP and a user-provided 2.19 fF VPP.

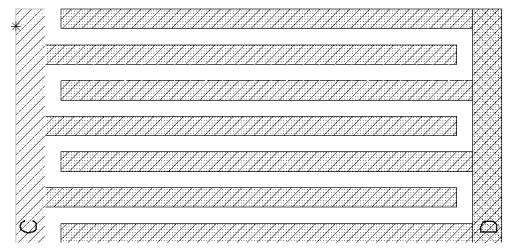
A two-port S-parameter simulation is performed to measure the capacitance of the generated unit capacitor layout. To calculate the capacitance, PCAST converts S parameter into Y parameters. The Im of Y-parameter of the Reverse Transmission Coefficient S12 (Im(Y)) of HPP and VPP are plotted in Figure 6.4 and Figure 6.5 respectively. The effective capacitance can be calculated as

$$C = \frac{-Im(Y)}{2\pi f} \tag{6.1}$$

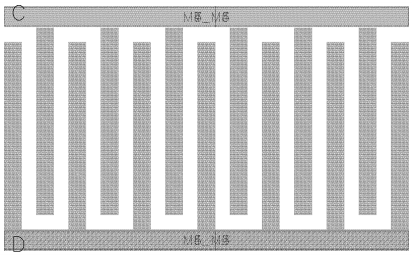
where f is the frequency.

The results of the capacitance extraction from 0.1MHz to 1.2 GHz is summarized in Table 6.2. Note the effective capacitance is inversely proportional to frequency. However, the changing of effective capacitance against frequency is small. With a 0.3 GHz increase in frequency, the effective capacitance drops 0.009% for both capacitor structures.

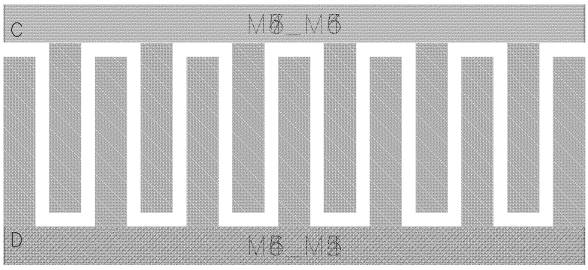
(a) A layout result with 8:15 aspect ratio.



(b) A layout result with 7:15 aspect ratio.

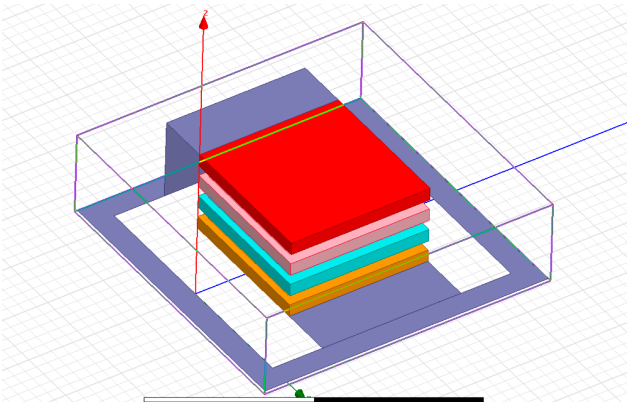


(c) A layout result with 7:4 aspect ratio.

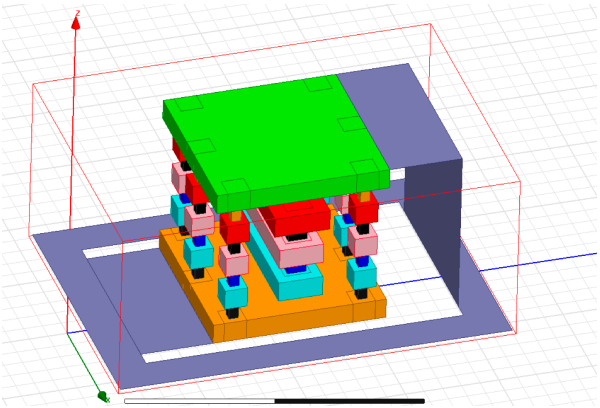


(d) A layout result with 11:5 aspect ratio.

Figure 6.2: Generated 0.5fF VPPs with various aspect ratios.



(a) HFSS HPP model.



(b) HFSS VPP model.

Figure 6.3: HFSS unit capacitor models.

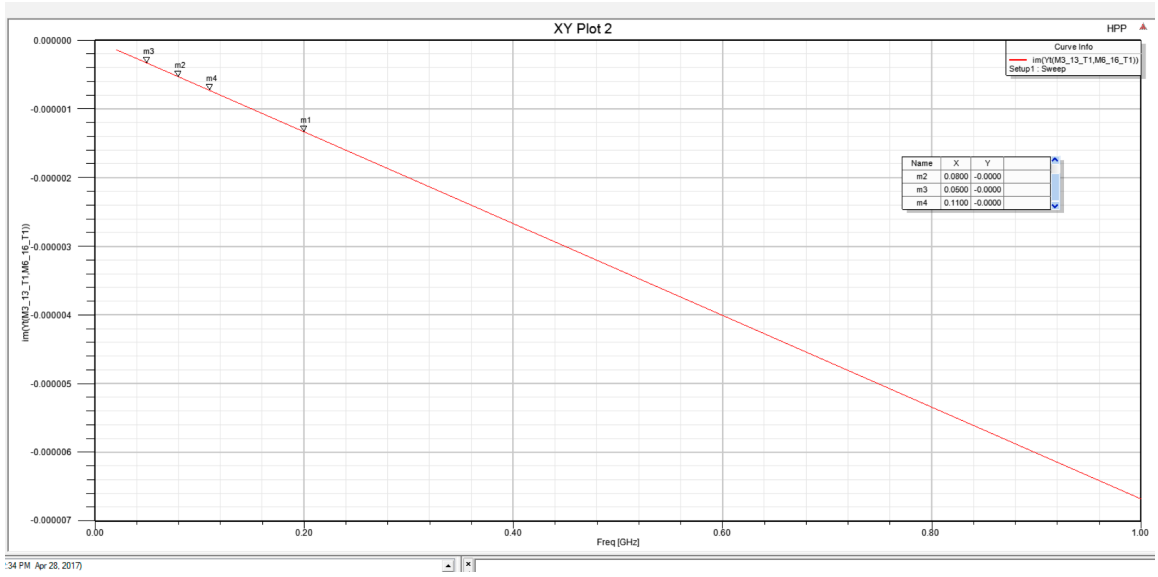


Figure 6.4: Simulated S-parameters for HPP layout.

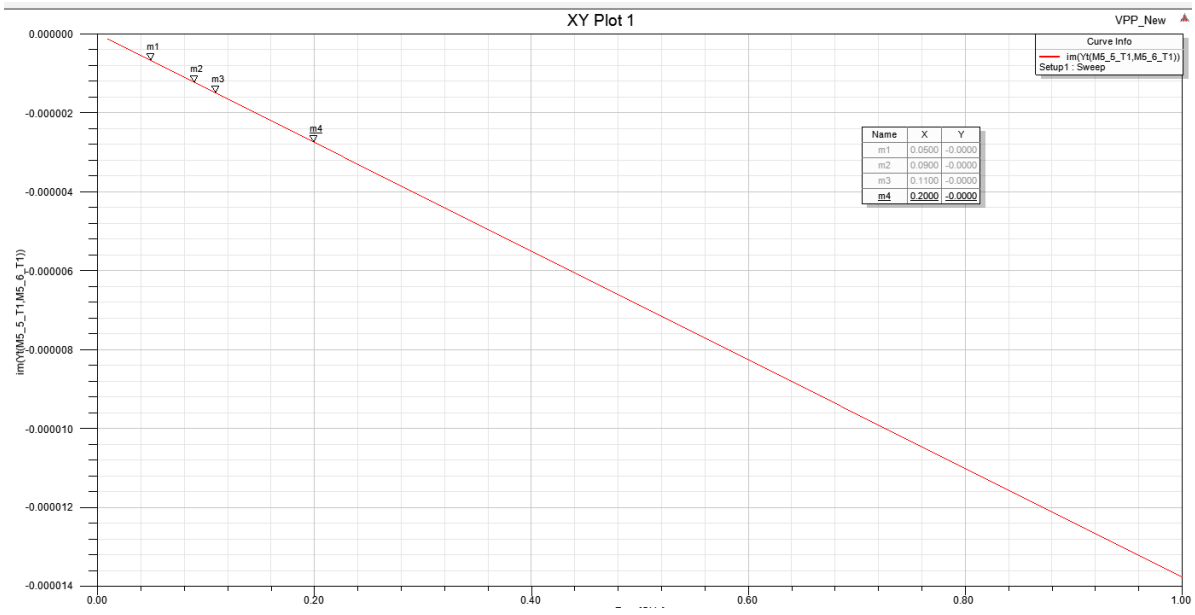


Figure 6.5: Simulated S-parameters for VPP layout.

Table 6.2: The extracted capacitance varies inversely with the frequency

	HPP		VPP	
Frequency(GHz)	**Im(Y)**	**Capacitance(fF)**	**Im(Y)**	**Capacitance (fF)**
0.05	-3.344e-7	1.064968153	-0.000000688	2.191082803
0.08	-0.000000535	1.064888535	-0.00000124	2.193913659
0.11	-7.3556e-7	1.064794441	-0.000001516	2.194557035
0.2	-0.000001337	1.064490446	-0.00000276	2.197452229

6.2 Synthesized Layout of Capacitor Array

Figure 6.6 is an example of synthesized 10-bit capacitor array layout. The core active area is 0.022 mm^2 (232 μm $\times$ 94.25 μm), with aspect ratio being 2.3:1. This capacitor array contains 1024 (2^{10}) unit capacitors and 31 redundant capacitors in a grid of 18 rows and 68 columns. Bit C_{6_b} contains non-binary radix weighting redundant capacitors. Bits C_4 through C_0, whose number of the unit capacitor is less than the capacity of one column (16), shares the rightmost column. Bit C_5, which fully occupies one column, is assigned to the middle column. The tool assigns bits C_{10} through C_6 (including the redundant bit C_{6_b}) symmetrically with respect to the middle column (used by bit C_5). The bottom plate of the unit capacitors is connected by vertical routing metals. The top plate is routed by horizontal routing metals.

An example of synthesized 5-bit capacitor array with roughly 2:1 aspect ratio is shown in Figure 6.7. The area of the array is 1.06 mm^2 (455.8μm $\times$ 231.68 μm). In this example, a user-provided layout of a 2fF capacitor is used. This array layout consists of 32 (2^5) unit capacitors, one redundant capacitor (C_{1_b}), and 27 dummy capacitors. In contrast to Figure 6.6, the size of capacitor array (N) is an even number. Thus PCAST assigns bit C_3 adjacent to the rightmost column of bit C_5. In this case, the routing metal for the top plate is in the horizontal direction, compared to a vertical top plate routing channel in Figure 6.6.

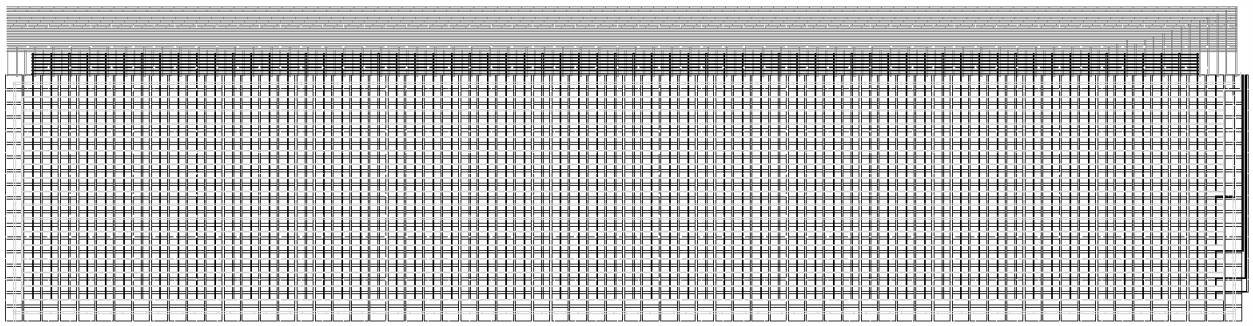


Figure 6.6: Synthesized 10-bit capacitor array layout.

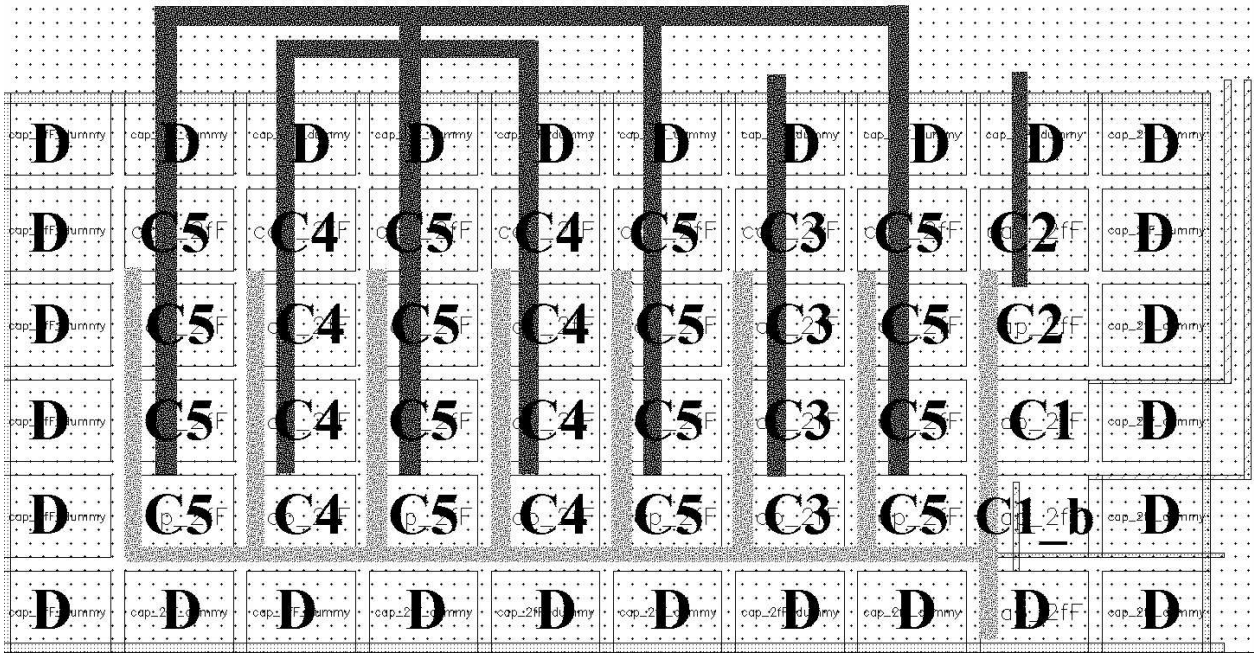


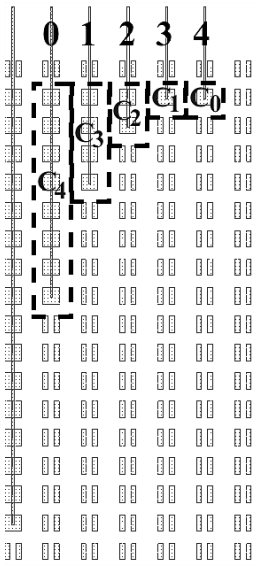
Figure 6.7: Synthesized 5-bit capacitor array.

PCAST supports user-specified bit locations of redundant bits and lower bits that do not fully occupy one column. This feature increases flexibility in capacitor array placement. For example, in Figure 6.8, bit C_4 through C_0 are placed in four configurations, depending on how the available columns are shared by the bits. By default, each bit occupies one column of the capacitor array, as shown in Figure 6.8(a).

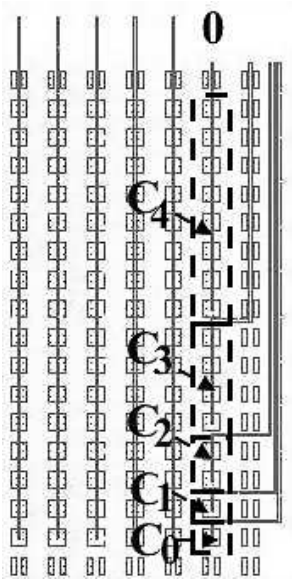
Our capacitor array synthesizer supports both binary radix weighting and non-binary radix weighting redundant bits. Shown in Figure 6.9(a), redundant capacitors with binary radix weighting are routed with horizontal metals, which is the same routing direction as the other unit capacitors. In the case of non-binary radix weighting capacitor redundancy (Figure 6.9(b)) , the user requests 31 redundant capacitors are inserted in a 10 bit capacitor array. Each column has 18 slots. Two of them are occupied by dummy capacitors. PCAST allocates two columns to place redundant capacitors. Among these slots, one unused slot is filled by a dummy capacitor. Horizontal routing metal connects the bottom plate of redundant capacitors.

The synthesized layouts pass the design rule check (DRC), the layout versus schematic (LVS), and the parasitic extraction (PEX) verifications.

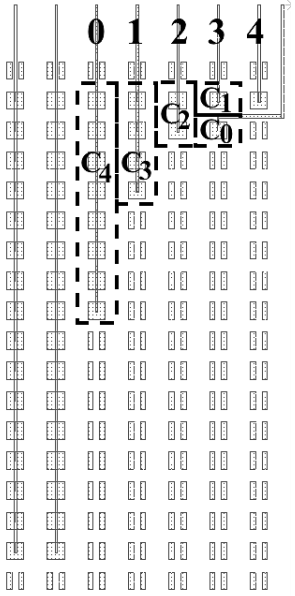
The effective capacitance (including routing parasitic capacitance) of each bit can be extracted using PEX tools. The extracted effective capacitance of each bit (including routing parasitics) are summarized in Table 6.3 and Table 6.4. Both capacitor arrys contain redundant capacitors (C_{6_b} and C_{1_b} respectively). As shown in Table 6.3 and Table 6.4, the measured capacitance ratios are very close to the ideal value. Compare to assigning lower bits (C_4 through C_0) into one column, a much lower mismatch can be achieved by assigning a column to each lower bits. Furthermore, set HPP(1) and VPP(1) show both capacitor structures have the same mismatch behavior when the actual capacitor area is considered. With the similar level of $\sigma(\Delta C/C)$, VPP is more area efficient.



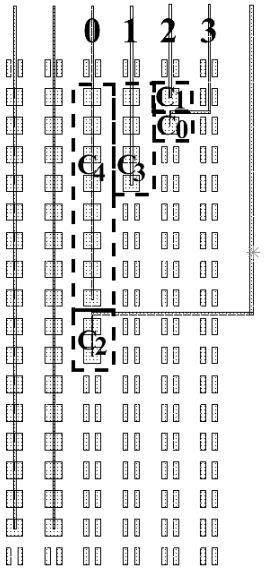
(a) Each bit occupies one column.



(b) Bits C_4 through C_0 fills one column.



(c) Bit C_1 and C_0 occupies column 4. Bit C_4 through C_2 occupy one column by themselves.

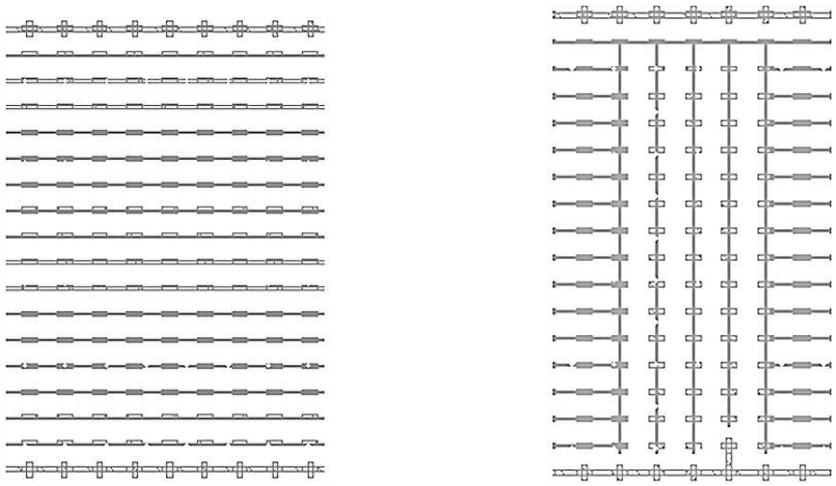


(d) Bit C_4 and C_2 occupies the column 0, bit C_3 fills one column, and bit C_1 and C_0 occupies column 2.

Figure 6.8: Synthesized capacitor array with specified bit locations of C_4 through C_0.

Table 6.3: Comparison of simulation results of the automated 10-bit capacitor array layouts (including routing parasitic). If default lower bits assignment is true, bit C_4 through C_0 occupies one column each; otherwise, lower bits are combined in one column.

Bits	**Capacitance (fF)**			**Cap Ratio Mismatch** C_N/C_{total}		
	HPP(1)	**VPP(1)**	**VPP(2)**	**HPP(1)**	**VPP(1)**	**VPP(2)**
C0	1.211	1.067	1.085	0.21%	0.08%	1.57%
C1	1.212	1.068	1.089	0.12%	0.01%	1.94%
C2	2.427	2.135	2.422	0.001%	0.003%	13.4%
C3	4.854	4.271	4.32	0.001%	0.001%	1.1%
C4	9.708	8.541	8.585	0.001%	0.02%	0.46%
C5	19.42	17.09	17.09	0.02%	0.03%	0.01%
C6	38.83	34.17	34.17	0.006%	0.003%	0.04%
C6_b	38.83	34.17	34.17	0.006%	0.003%	0.04%
C7	77.67	68.33	68.33	0.007%	0.018%	0.06%
C8	155.3	136.7	136.7	0.019%	0.012%	0.03%
C9	310.7	273.3	273.3	0.014%	0.025%	0.06%
C10	621.3	546.8	546.8	0.003%	0.012%	0.03%
	Default lower bits assignment			**Area**		
	True	True	False	6733.32 μm^2	1267.73 μm^2	1196.98 μm^2



(a) With a binary radix weighting redundant bit.

(b) With a non-binary radix weighting redundant bit.

Figure 6.9: Capacitor array top plate connection.

Table 6.4: Comparison of simulation results of the 5-bit capacitor array schematic, the automated layout.

Bits	**Capacitance (fF)**	**Capacitance Ratio** C_N/C_{total}		
		Ideal	**Extracted**	**Mismatch**
C0	1.9723	0.03125	0.0296	5.32%
C1	1.9979	0.03125	0.03	4.1%
C1_b	2.0012	0.03125	0.03	3.94%
C2	3.9715	0.0625	0.0596	4.68%
C3	8.1006	0.125	0.1215	2.79%
C4	16.2037	0.25	0.2431	2.77%
C5	32.4161	0.5	0.4863	2.75%

Chapter 7

CONCLUSION

A practical and flexible capacitor array synthesizer developed in SKILL® language, named PCAST, has been introduced. Targeted for metal-oxide-metal capacitor automatic generation (layout and symbol) and characterization (capacitance and mismatch) for SAR-ADC implementation, PCAST has been seamlessly integrated with circuit design tools and design environment. A wide range of user inputs is supported to capture designer knowledge and increase re-usability. This capacitor array synthesizer reduces the design effort and the chance of cockpit error of manual layout of the regular structures significantly. The results from commercial physical verification tools demonstrate that the capacitor array layout synthesized by PCAST is functionally correct with accurate capacitor ratios and the required match.

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