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Efficient Power Splitters and Couplers in Silicon Nanophotonics

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A thesis
submitted in partial fulfillment of the
requirement for the degree of

Master of Science in Electrical Engineering

University of Washington
2012

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Program Authorized to Offer Degree:
Electrical Engineering

DEDICATION

To my wife and parents

ACKNOWLEGEMENTS

I wish to express sincere appreciation to the Department of Electrical Engineering for their support, especially Professor Michael Hochberg for his mentorship. I would like to thank Dr. Tom Baehr-Jones in the Nanophotonics Lab for his guidance and help on my way of exploring the scientific world and pursuing my own interests. I would also like to thank my family and friends for their encouragement and devotion over the years.

University of Washington

Abstract

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There has been a recent explosion of interest in the optical properties of silicon in the near infrared regime, and in particular using Silicon-on-Insulator (SOI) as a platform for integrated optics. Due to the high refractive index contrast between silicon and silicon dioxide, the optical mode for typical waveguides is tightly confined in a submicron region, creating a number of advantages and disadvantages. On the one hand, the small mode volume enables compact layout, thus high device density. However, the high index contrast also raises the requirements for fabrication resolution and uniformity. For example, a simple silicon waveguide Y-branch usually has over 1 dB insertion loss because the required sharp corners will not resolve in a typical CMOS process. Another challenge is efficient coupling between the very small modes in silicon waveguides, and the larger modes often found in other material systems. Here I demonstrate the solution to a number of key optical design problems in silicon photonics. I report on a novel Y-branch with insertion loss of 0.13 dB and minimum feature size of 0.2 μm, followed by a discussion on cascaded directional couplers that are insensitive to evanescent coupling coefficient variations. I also report on a new approach to

achieving edge coupling on the silicon platform, which utilizes thin waveguides with an expanded mode size. This approach can be used to couple a silicon waveguide efficiently to an external laser cavity in a III-V material, and so may play an important role in the development of an on-chip laser. This is one of the first proposals in the literature to address the gain-chip/silicon waveguide coupling problem. An external cavity laser using the new Y-branch and thin waveguide coupler is proposed.

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Chapter 1. Silicon as A Photonic Platform

Silicon has been the overwhelmingly preferred substrate material for integrated circuits (ICs) for the past half-century. Device density has scaled up according to the Moore's law, providing great benefits in terms of performance and economics. However, in terms of fundamental performance metrics such as free carrier mobility, silicon doesn't win over other semiconductor materials such as Germanium. Silicon's capability to form a stable and high quality oxide favors device yield and makes it the best material for the integrated circuits platform. As a result of the continuous efforts of the electronics industry and academia, it has also become one of the most well understood material systems. Mature theoretical models and fabrication technologies have been developed for the growing, etching, patterning, doping and oxidization of silicon.

A number of properties of silicon make it also an attractive material system for integrated optical circuits in the near infrared regime. The 1.12 eV band gap of silicon indicates that it is transparent at communication wavelength, 1.3 μm to 1.6 um. It also has a refractive index of 3.4, high enough to confine light by total internal reflection in a waveguide consisting of a submicron silicon core and a silicon dioxide cladding. Silicon-on-Insulator (SOI) wafers readily available from industry greatly aid the construction of silicon waveguides. A cross-section of an SOI wafer, SOI with patterned top silicon film and silicon waveguide fabricated on SOI are shown in Fig. 1.1. The top silicon film thickness is usually 200 nm ~ 400 nm. SOI wafer with a 220 nm thick silicon film on top of 2 μm buried oxide (BOX) layer is used in this work.

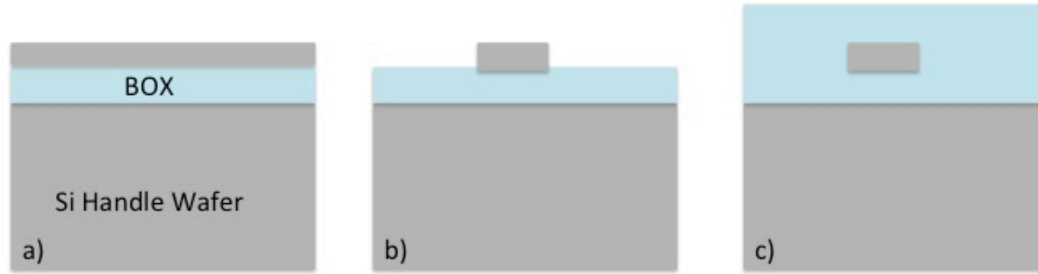

Figure 1.1 Cross sections showing the formation of waveguide on SOI wafer. a). Cross-section of an SOI wafer. BOX stands for buried oxide. b). Top silicon film is patterned to form the core of silicon waveguide. c). Silicon oxide is deposited as the top cladding.

The optical field distribution and propagation constant of the waveguide shown in Fig 1.1 c) can be obtained by solving Maxwell equations, with boundary conditions determined by the waveguide geometry. Each solution is called a mode of the waveguide. Usually the waveguide width is tailored to allow only one guide mode. Waveguide width of 500 nm is chosen in this work for single mode operation at 1550 nm wavelength. A contour plot of major electric field component of a 500 nm x 220 nm waveguide is shown in Fig. 1.2. The mode is solved numerically using Lanczos method. It can be seen that electric field is tightly confined within the silicon core. The propagation loss is measured to be 2.4 ± 0.3 dB/cm, which is low enough for building integrated optical circuits. The propagation loss mainly comes from scattering by the roughness of the sidewall.

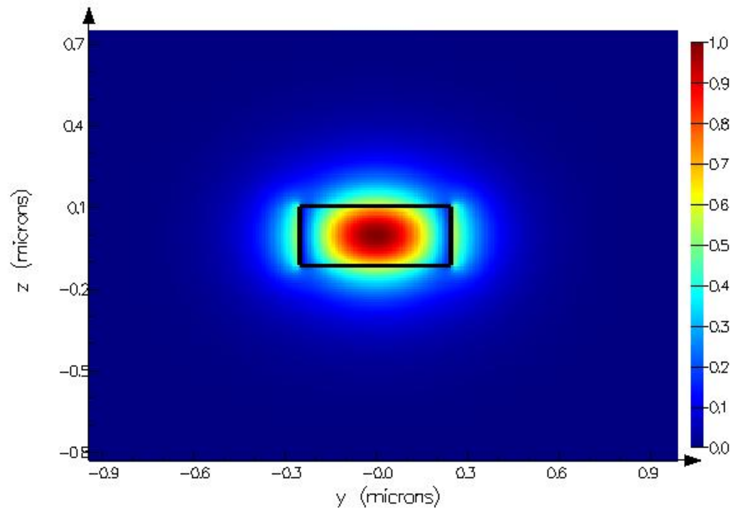

Figure 1.2 E_y of TE mode of 500 nm x 220 nm silicon waveguide

The waveguide described above is the most basic building blocks silicon integrated optical circuits. Its submicron size enables compact layout and high device density. In this chapter, coupling between waveguide and single mode fiber, light modulation and detection schemes will be introduced. In the end, we discuss the advantages and challenges of silicon as a photonic system.

I. Grating couplers

The silicon waveguide discussed above needs to be connected to a single mode fiber somehow to couple light on and off the chip. A typical single mode fiber has a core diameter about 10 μm and a cladding diameter of 125 μm. So there is a large mode size mismatch between the fiber mode and silicon waveguide mode, thus the coupling efficiency is very low. Grating couplers are usually used to reduce the coupling loss between silicon waveguide and single mode fiber. A schematic of a grating coupler is shown in Fig. 1.3 a). Light coming from the waveguide is scattered by the gratings, and the mode is effectively expanded. The trench size and grating pitch can be engineered to

match grating coupler output field pattern to the fiber mode profile. Test structure layout is shown in Fig. 1.3 b). A typical measured spectrum is shown in Fig. 1.3 c). The cross-wafer average grating coupler insertion loss on our platform was measured to be 4.4 ± 0.2 dB, with a peak wavelength near 1545 nm and a typical 1.5 dB bandwidth of 45 nm. The loss is low and stable enough for device characterization.

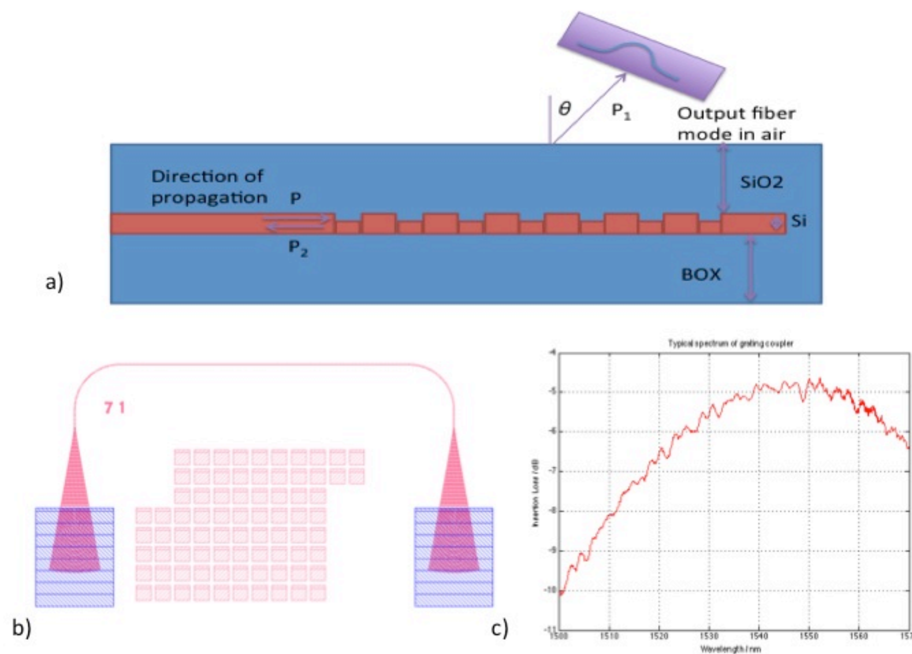

Figure 1.3 Grating couplers, a) schematic cross-section, b) test structure layout and c) typical spectrum. Red squares in b) are dummy tiles to reach the required device density by the design rules. Red stands for unetched 220 nm silicon layer; red and blue together means a final silicon thickness of 170 nm.

II. Silicon waveguide modulators

As we have discussed, silicon has a high refractive index that allows the waveguide geometry to be submicron, which benefits device integration. We also want to have a tuning nub to adjust its refractive index, thus the phase of the propagation mode.

Unfortunately silicon's refractive index does not respond linearly to electric field due to its inversion symmetric structure. The free carrier dispersion effect [1], change of refractive index as a function of free carrier concentration expressed in Eq. 1.1, is commonly used to modulate light.

$$\Delta n = -[8.8\times 10^{-22}\times \Delta n_e + 8.5\times 10^{-18}\times (\Delta n_h)^{0.8}] \tag{1.1}$$

Note the depletion region width of a reversed biased pn junction is determined by the applied voltage. Therefore, modulating the depletion region width of a pn junction built in waveguide will effectively control the phase of the propagation mode. Doping profile of such a pn junction is illustrated in Fig. 1.4. This junction can be built by ion implantation of a rib waveguide. The implantation recipe is summarized in Table 1.1, simulated by Sentaurus Process TCAD. Two-step implantation is used to get uniform doping in all 220 nm silicon.

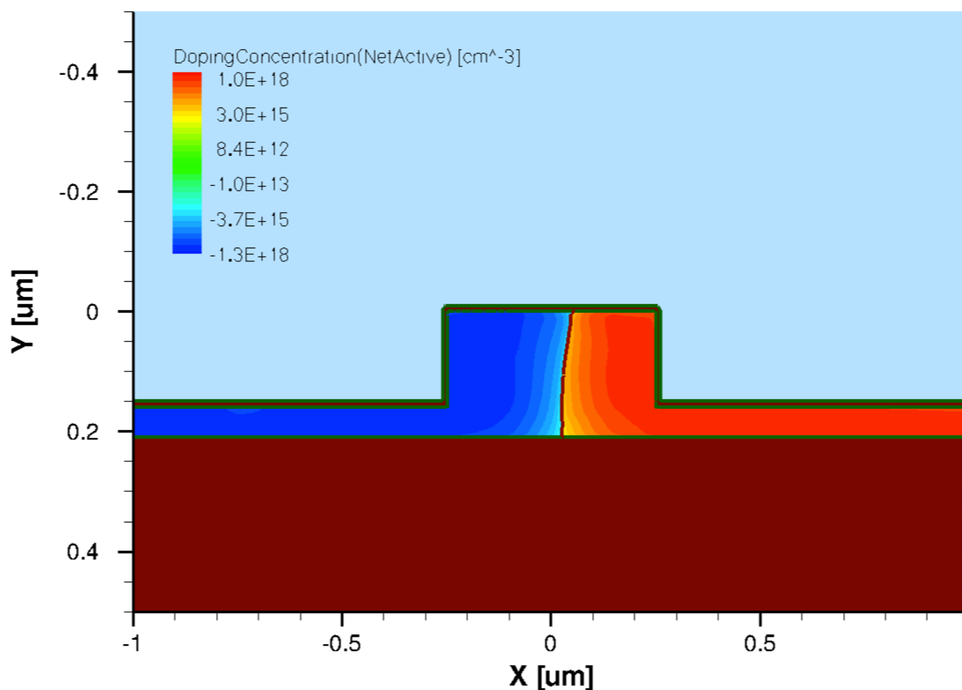

Figure 1.4 Simulated doping profile of waveguide pn junction

Species	Energy (KeV)	Dose (cm^-2)	Tilt (degree)
Boron	**10**	**4.6e12**	**7**
Boron	**40**	**1.7e13**	**7**
Phosphorus	**35**	**3.0e12**	**7**
Phosphorus	**110**	**1.6e13**	**7**

Table 1.1 Implantation recipe of waveguide pn junction

Phase change can be converted to resonance peak shift of a ring resonator or output intensity difference of a Mache-Zehnder interferometer (MZI). Either one can be used for electrooptic modulation. For a dual bus ring modulator consists of a 30 μm radius ring and a lateral pn junction centered in a rib waveguide. The ring FSR was around 3.2 nm, and typical Q was 7000. An average cross wafer tunability of 10.6 ± 0.1 pm/V was determined by measuring the resonance shift as bias voltage varied from -200 mV to 200 mV. The average bandwidth was 18.7 ± 0.1 GHz at 0V dc bias. For MZI modulator, transmission line electrodes were designed to match the RF and optical signal velocity. Device impedance was 33 ohms. Two arms were intentionally unbalanced to allow quadrature biasing by tuning the wavelength. The average cross-wafer modulator insertion loss was 6.2 ± 0.5 dB, excluding losses from routing waveguide. Average cross-wafer 3 dB bandwidth at 0 V bias was 15.5 ± 0.2 GHz for the lower arm and 17.6 ± 0.8 GHz for the upper arm. An extinction ratio of 4.4 dB was obtained with a 1 Vpp signal.

III. Germanium photodetector

The primary disadvantage of silicon as an optical material is its indirect band gap, thus unable to lase or detect light. On the other hand, Germanium has good absorption at

communication wavelength. Note that germanium is a CMOS compatible material and is widely used for high performance heterojunction bipolar transistors (HBTs). Ge-on-Si photodetectors has been the most promising solution for the silicon photonics platform. Schematic and simulated light propagation in a Ge-on-Si detector is shown in Fig. 1.5.

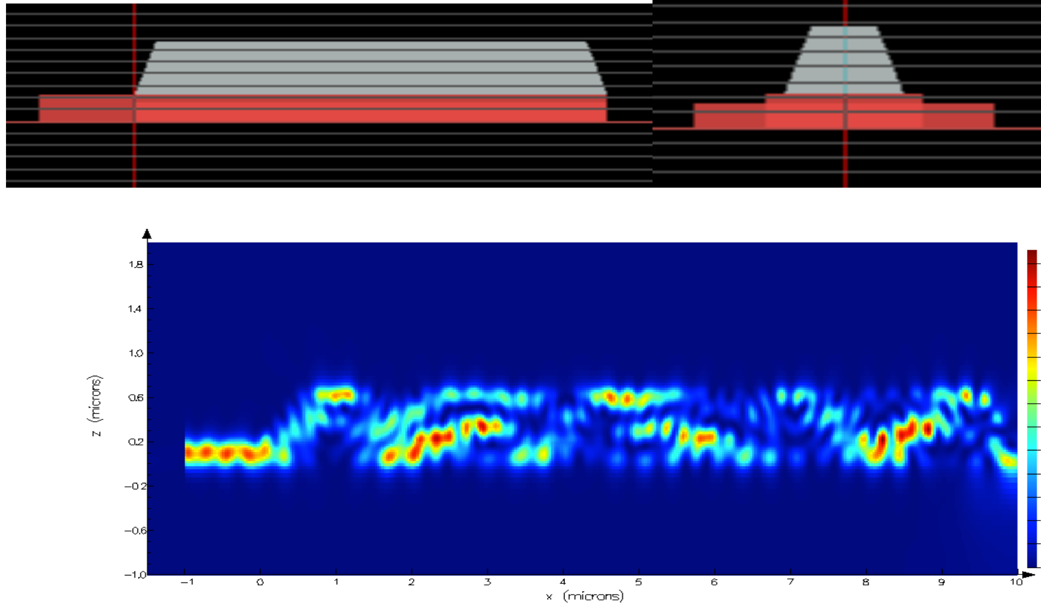

Figure 1.5 Ge-on-Si detector device cross-section and optical field distribution

Photodetectors constructed using vertical Ge-on-Si p-i-n junction are 11 μm long and 8 μm wide in our platform. Average responsivity is 0.54 ± 0.05 A/W and dark current 4.8 ± 0.4 μA with 4 V reverse bias. Average device 3 dB bandwidth was measured to be 20.2 ± 1.4 GHz.

IV. Silicon photonics process flow

Silicon waveguide fabrication on an SOI wafer was illustrated in Fig. 1.1. To support grating couplers, modulators, and detectors, more fabrication steps are needed. A CMOS compatible process flow to fabricate all the devices above is described in this section. The final wafer cross-section is shown in Fig. 1.6. Starting substrate is an 8-inch SOI

wafer, with 220nm, 10 ohm-cm p-type top silicon film, 2um BOX and a 750 ohm-cm handle wafer. High resistivity wafer is used to reduce RF coupling between modulator electrodes and silicon substrate. The top silicon layer is patterned using standard lithography and dry etching technologies. Three anisotropic etch steps (60nm, 130nm, and 220nm) are applied to create grating couplers, rib, and channel waveguides. We provide a more detailed discussion about this step in Chapter 3. After patterning, the wafer was implanted by p and n dopants for silicon modulator junction formation, p+ for anode of Germanium detectors, and p++, n++ for low resistivity metal contact. Dopants in silicon are activated using rapid thermal annealing (RTA). Then a layer of Germanium about 500 nm thick is epitaxially grown by chemical vapor deposition (CVD). Usually a thin layer, 30 nm ~ 50 nm, is deposited first at a low temperature of about 300 degrees, then the majority of Germanium is deposited at a high temperature of about 700 degrees to reduce dislocations caused by lattice mismatch between silicon and germanium crystal. Germanium is relaxed at depositing temperature and under tensile strain after cooling down to room temperature because its thermal expansion coefficient is larger than that of silicon. The tensile strain narrows its band gap slightly and allows absorption up to 1600 nm. Another n++ implantation and RTA process are performed to form the cathode of detectors. Tungsten plug and aluminum or copper interconnects are then added for routing and wiring. Chemical mechanical polishing (CMP) can be used to remove surface topography.

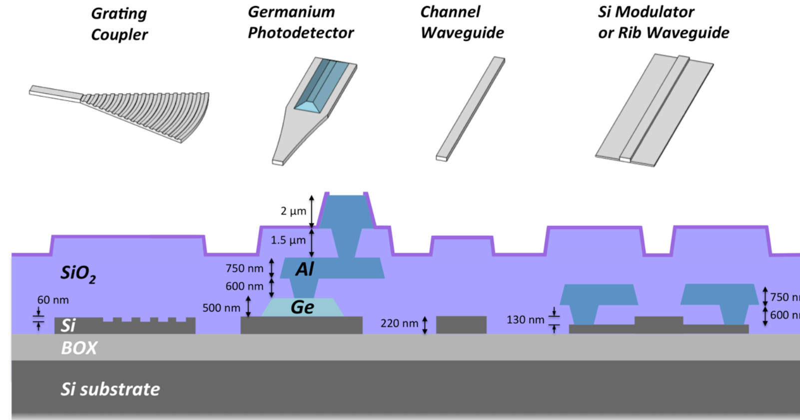

Figure 1.6 Cross-section of silicon photonic platform

V. The silicon photonic platform

Modulators and detectors are the basic building blocks of integrated optical circuits, and they can be readily fabricated by state of the art CMOS technology, as shown in last section. A photonic link is promising to provide enough bandwidth for inter-chip communication. Other possible applications of silicon photonics include bio sensing, optical communications, etc. As we emphasized in the beginning of this chapter, silicon wins as the dominate material for ICs because its capability to ensure yield of complex systems. Silicon photonic system complexity scaling in the first decade of 21st century is summarized in Fig. 1.7. We have noted that components count doubles every 12 to 18 months, similar to IC scaling rate predicted by Moore's law. It is very likely that this trend will continue. And more system level functionalities will be demonstrated using silicon as a photonic platform.

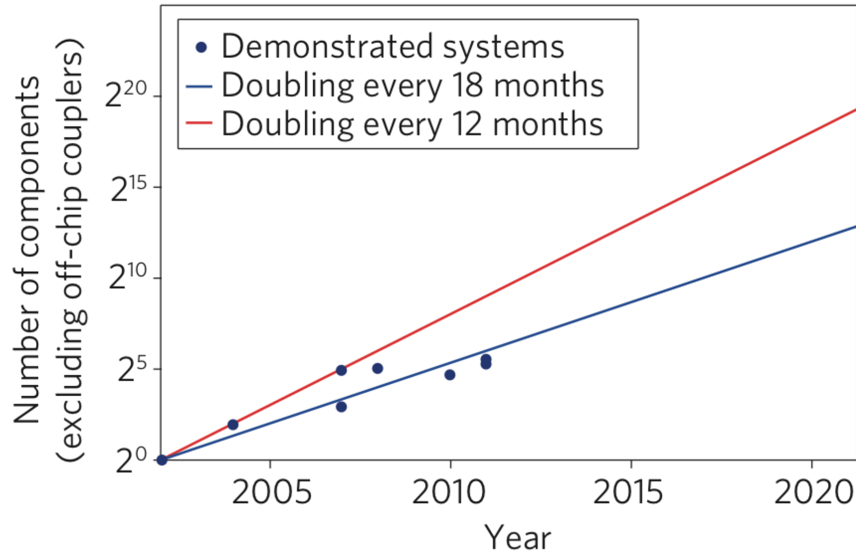

Figure 1.7 Component count of photonic components doubles every 12 to 18 months in the first decade of 21st century [2].

However, there are also challenges need to be addressed. Confining the optical field in a submicron silicon strip create unique difficulties for modal coupling. For example, a simple Y-branch intended to split the power in a waveguide equally into the two branches has over 1 dB excess loss, because the sharp corner required for low loss coupling will not yield in typical CMOS processes. Evanescent coupling widely used in ring resonators is also sensitive to fabrication variations. Similar to the fiber coupling, there is also large mode mismatch between a silicon waveguide mode and a semiconductor laser mode. Low loss coupling between silicon waveguides and semiconductor lasers hasn't been demonstrated without significantly increasing process complexity.

Solutions to solving these problems are proposed in this thesis. In Chapter 2, waveguide fabrication process is detailed to further explain fabrication limitations. In Chapter 3, a new Y-junction with a minimum feature size of 0.2 μm and ultralow insertion loss of

0.13 dB is designed. In Chapter 4, a discussion on robust evanescent coupling is presented. In Chapter 5, a low loss silicon waveguide and semiconductor laser coupler making use of the expanded mode of ultrathin waveguide is presented. An external cavity laser using the new Y-junction and thin waveguide coupler is proposed.

Chapter 2. Waveguide Fabrication

In Chapter 1, a full process flow of a silicon photonic platform is briefly reviewed. In this chapter, we focus on waveguide fabrication at the very beginning of the flow. The rest fabrication steps can be adopted from standard CMOS processes without much change. The first step of fabrication is to transfer the layout pattern to a layer of resist on top of the wafer. Nanoscale resist patterning can be done either by electron beam lithography (EBL) or ultraviolet (UV) photolithography. Both will be covered in this chapter. The second step is etching the SOI wafer using patterned resist layer as a mask. An inductively coupled reactive ion etch (ICP RIE) process is presented. Sidewall smoothing is sometimes performed since sidewall roughness determines propagation loss. A few cycles of oxidation and oxide stripping are usually used for this purpose. Our post-etched waveguide sidewall is already very smooth. So we didn't include further sidewall smoothing to keep the process in an academic cleanroom simple and stable.

I. Lithography

Lithography was first invented for publishing theatrical works. It is now a standard step in semiconductor planar process. A few drops of resist, which is usually some polymer dissolved in solvents, is first spun onto the wafer to form a uniform thin film. The wafer is then baked at around 100 ^{o}C to fully drive out the solvents. Then the wafer is selectively exposed to UV light or electron beams. After exposure the wafer is dipped in a chemical solution called developer. The exposed or unexposed part (determined by the property of the resist) is dissolved in the developer. The first pattern transfer is over after rinsing the wafer by deionized (DI) wafer and spin-drying. The resolution of

photolithography tools is usually determined by its diffraction limit, roughly half the wavelength. A mask carrying the layout information is needed to partially block the light during exposure. However, no mask is needed by EBL since the software that controls beam position can read layout data stream directly. Hence EBL is faster for small area exposure, because fabricating high quality mask takes time. The wavelength of electrons accelerated to 100 KeV is 0.004 nm, so it is not a limit of resolution anymore. The resolution of an EBL can be well blow 10 nm, and is usually limited by the proximity effect, as will be discussed blow. Both short turn around time and high resolution are ideal for prototyping devices.

A. *Electron beam Lithography*

EBL tools expose the desired position on a wafer by controlling the motion of electrons using electro-magnetic lenses. It usually consists of an electron emitter, a column with multiple focusing and deflection lenses, a high-resolution stage to hold the wafer and a controlling computer. Dose and other control information are specified in job files. The EBL process in this work was developed in the Micro-Fabrication Facility of College of Engineering, University of Washington. A picture of the system is shown in Fig. 2.1.

The first step of an EBL exposure of a certain resist is to determine the dose, which is the number of electrons received per unit area on the wafer. For positive resist, the dose should be high enough to clear the resist in exposed area after develop. For negative resist, dose should be able to cause enough crosslinking of resist and keep the exposed part on wafer after develop. In general, the required dose is determined by chemical properties of the resist and developer. For EBL, the dose is also pattern dependent. High-energy

electrons will be scattered the by the resist and wafer matrix, thus affecting the proximity of the collision site. As a result, dense patterns usually need lower dose than sparse ones. And large patterns need lower dose than small ones. This is called the proximity effect. As shown in Fig. 2.2, lines in the middle are affected by electrons intended to expose its vicinity and get blurry. The actual dose received by a pixel on the wafer is determined by the electron beam dwelling time on top of it. And the dwelling time can be pre-adjusted to compensate the proximity effect regarding pattern size and density. Dose received by a specific pattern can also be scaled up or down empirically from the baseline dose, which is called dose modulation. The final goal of dose experiment, proximity effect correction (PEC) and dose modulation is to make sure the pattern come out as they are defined in the GDS file.

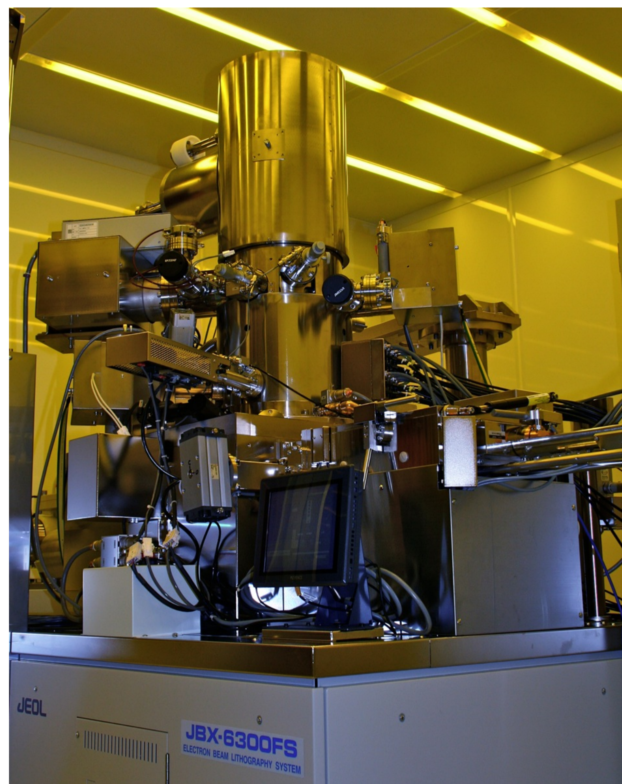

Figure 2.1 The JBX-6300FS EBL tool in Microfabrication Facility of College of Engineering, University of Washington.

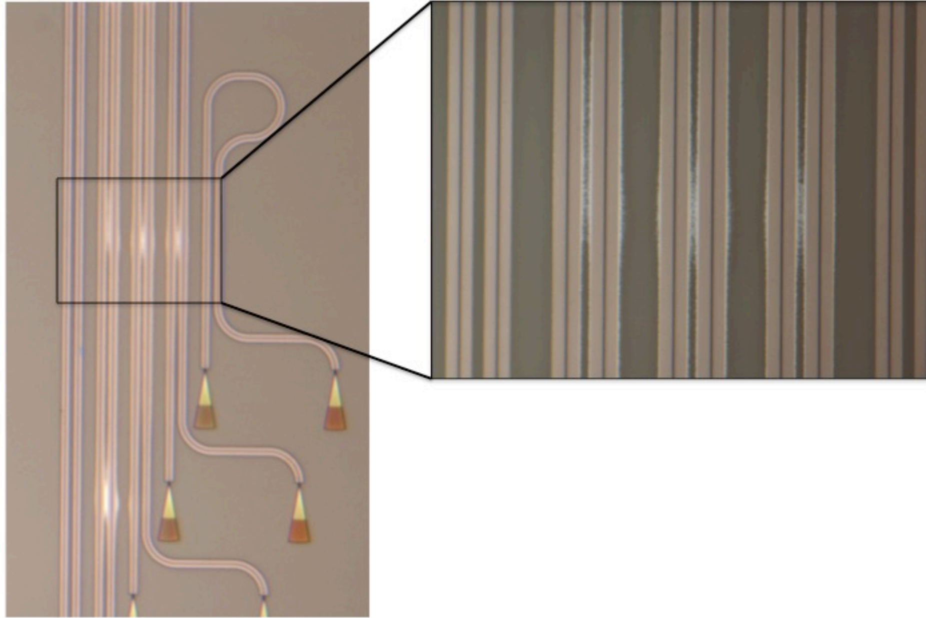

Figure 2.2 A microscope image shows EBL proximity effect in rib waveguide fabrication. Substrate is an SOI wafer with a 220 nm silicon film on top of 3 μm buried oxide layer. 6% HSQ resist was spun at 4000 rpm for 60 s to get a 150 nm thick film. Uniform dose of 2800 μC/cm^2 was used. Wafer was developed in 25% TMAH for 4 min and etched using chlorine plasma.

In terms of passive photonic device fabrication, critical dimensions include waveguide width, grating size, waveguide separation in directional couplers, etc. Deviation from the designed size due to improper resist thickness, dose, developer concentration, and develop time will degrade device performance. Here we show a calibrated EBL process for building waveguides. A scanning electron beam microscope (SEM) image of a test pattern with straight lines of different width is shown in Fig 3.3. It is seen that lines from 100 nm to 500 nm wide come out correctly at the same time. ZEP520A positive resist was spun at 2000 rpm for 60 s, followed by a softbake at 180 ^{o}C for 3 min. Base dose is 200 μC/cm^2, and PEC was used. Proximity effect was modeled by two Gaussian

functions. Default parameters for PMMA resist of similar thickness were used. After exposure the wafer was developed in amyl acetate for 30 s and rinsed in isopropanol for 15 s. Wafer is etched in fluorine plasma. Etch recipe is detailed in Section 2.2.

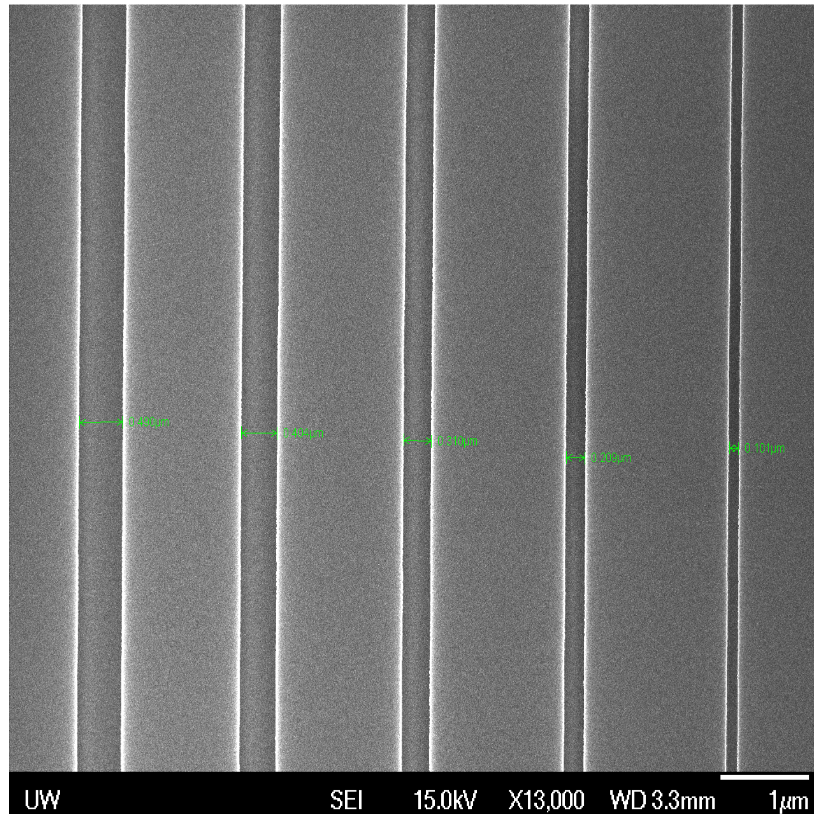

Figure 2.3 Lines with width of 100nm ~ 500nm were accurately fabricated. Substrate was SOI wafer with a 220 nm silicon film on top of 2 μm BOX. ZEP520A was spun at 2000 rpm for 60 s and baked at 180 C for 3 min. Baseline dose is 200 μC/cm^2 and PEC was used. Wafer was developed in amyl acetate for 30 s and rinsed in isopropanol for 15 s. Wafer was etched in fluorine plasma.

When multi-layers are needed, new layers need to be aligned to the patterns already on the wafer. There is no visible optics to determine the position of the alignment marks. The only way is to use the primary electron beam. Alignment marks are fully etched crosses in this process, as shown in Fig. 2.4. The mark position is determined by contrast felt by the reflection beam detector. Usually a long-range scan was used first to find the mark. Then a short-range scan is used to determine the exact position. Any area scanned

by the beam gets exposed, and will be developed and etched. So the mark should be far away enough from key devices.

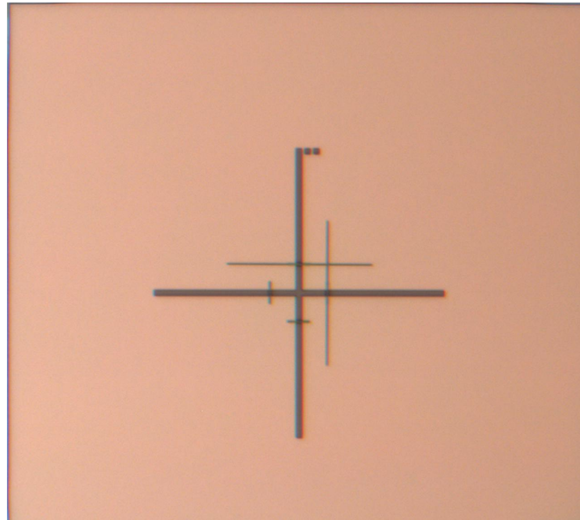

Figure 2.4 EBL alignment mark after develop but before etch. Substrate is SOI wafer with a 220 nm silicon film on top of 3 µm BOX. 6% HSQ resist was spun at 4000 rpm for 60 s to get about a 150 nm thick film. Uniform dose of 2800 µC/cm^2 was used. Wafer was developed in 25% TMAH for 4 min.

B. UV photolithography

The EBL expose the wafer by scanning with electron beams, which makes it very slow when the area to be exposed is large. Photolithography tools can expose the whole pattern by turning on the bulb for seconds. Therefore, photolithography is preferred for large volume production. Basic idea of UV photolithography is the same as that of EBL, and in many cases UV light is easier to control than electrons. However, there are other challenges such as exposure uniformity across the reticle. The main variables for users to determine are the exposure dose and develop time.

II. Reactive ion etching

After a successful exposure, the next step is to transfer the pattern in the resist film to the wafer by etching silicon. Dry etching is widely used because of its better anisotropy

compared to wet etch. An Oxford Plasmalab100 inductively coupled plasma reactive ion etcher located in the University of Washington Microfabrication Facility cleanroom is used in this work. The schematic of that etcher is shown in Fig. 2.5. Etching gases are injected from the top of the chamber. The RF powered coil strikes and maintains plasma. Ions in the plasma are accelerated to the wafer surface and volatile etching products are pumped out of the chamber. Helium gas flows at the backside the wafer to conduct heat. The ions etch silicon either by physically knocking a silicon atom off the matrix or chemically react with silicon. Argon is usually used for sputtering. Fluorine ions can react with silicon and the product is volatile, so gases containing fluorine such as SF_6 are commonly used for etching silicon. Chlorine is conventionally used as a metal etching gas, but can also be used for nanoscale silicon etch.

Compared to the conventional parallel plate RIE ethers, the ICP etchers decouple the plasma generation and ion acceleration process. To the first order, plasma generation and ion density is controlled by the RF power, and ion acceleration to the wafer surface is determined by the forward power, which allows more freedom in tuning the etch. The chamber pressure is kept low as long as the plasma sustains. At low pressure, species have less collision and large mean free path. So their velocity is maintained maximally vertical to the wafer surface. The RF power, forward power, gas ratio if multiple gases are used, and temperature are main parameters in tuning an etch recipe.

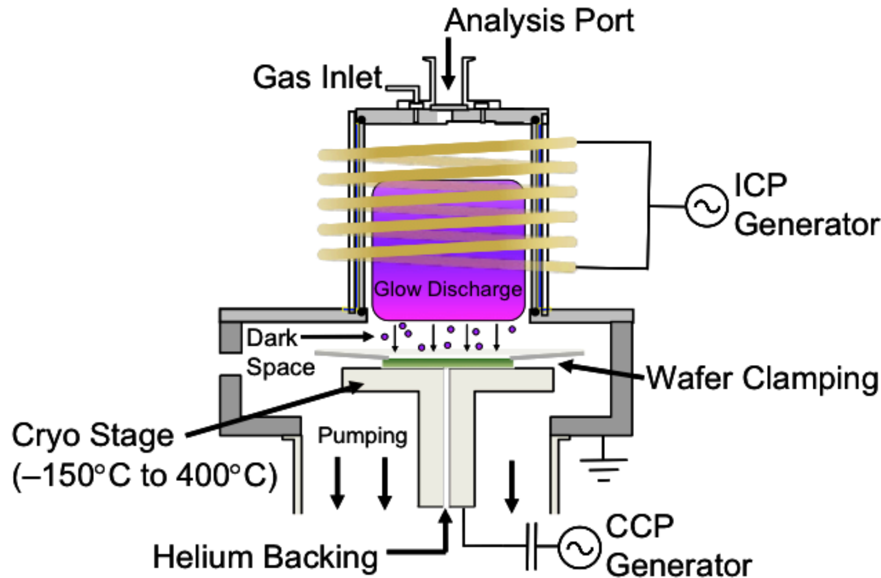

Figure 2.5 Schematic showing principles of an ICP RIE etcher [3]

Sidewall angle of a dry etched silicon trench or ridge is usually between 80 and 90 degrees. In the particular case of waveguide etching, a smooth sidewall is the primary goal since sidewall roughness determines the scattering loss. It is believed certain balance between the physical part and chemical part of etching produces smooth sidewalls. A so-called pseudo Bosch etch process is calibrated for waveguide etching. SF_6 and C_4F_8 are injected into the chamber at the same time. Fluorine ionized from SF_6 accounts for the chemical etching part. The cyclic C_4F_8 breaks in the plasma to produce CF_2 and longer chain radicals. They are deposited at the silicon surface as passivation fluorocarbon polymers. The etching is faster in the direction vertical to the wafer surface than parallel to the wafer, so polymer at trench bottom gets sputtered but the sidewall is protected. Chamber was kept at 20 ^oC by liquid nitrogen. Pressure was 15 mTorr, close to the minimum to maintain the plasma. Forward power is 20 W and ICP power was 600 W. A DC bias of 120 V to 128 V was observed. SF_6 flowed at 25 sccm (stands for standard

cubic centimeter per minute), and C_4F_8 flowed at 40 sccm. Helium backside cooling pressure is 7 Torr. The helium pressure is maintained by a butterfly and a mass flow controller (MFC). Etching time was set to 150 s, a bit more than needed by etching away 220 nm silicon, to ensure silicon was cleared beside the waveguide.

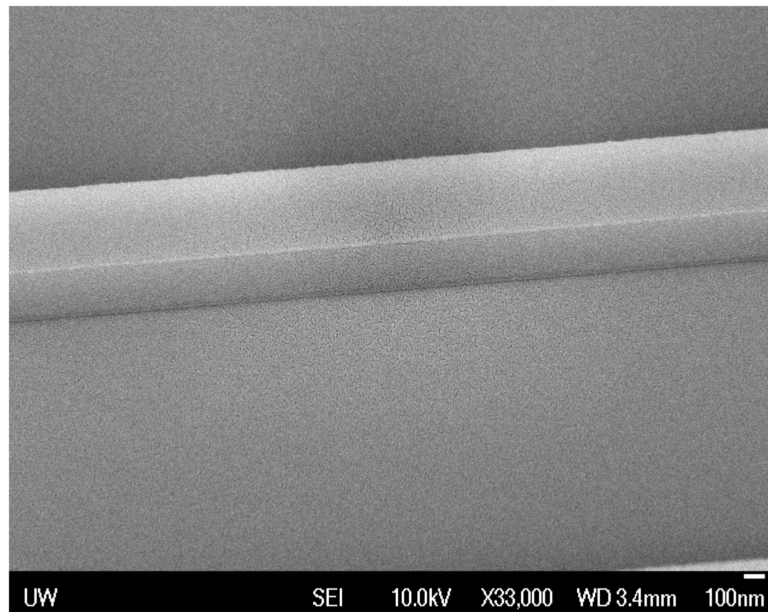

Figure 2.6 SEM image of etched waveguide sidewall. Chamber pressure is 15 mTorr. Temperature is 20 ^{o}C. And Helium backside cooling pressure is 7 Torr. Froward power is 20 W and ICP power is 600 W. SF_6 flows at 25 sccm and C_4F_8 40 sccm. Etch time was 150 s. Resist etching mask had been stripped. A very thin layer, 0.5 nm to 2 nm, of gold was sputtered to enhance conductivity.

Oxygen plasma was run for 20 min to clean the chamber. Then the recipe was run on a dummy silicon wafer for 15 min to condition the chamber. These two steps were performed trying to minimize the effects of other recipes ever run on the etcher in a multi-user facility. The SOI piece was mounted on a 4-inch silicon wafer using fomblin oil. The chamber was pump down to a threshold level, such as 10^{-5} Torr before flowing the etching gases. After the gas flow had been stabilized and chamber reached the target

pressure, RF power was turned on and etch started. The chamber was pumped down again to evacuate the toxic etch gases and etch products before the wafer was unloaded. Resist was stripped by soaking the sample in solvent for 15 min. The sample was then sputter-coated with a very thin film of gold, about 0.5 nm, to enhance conductivity during the SEM imagine. A side view SEM image of a waveguide is shown in Fig. 2.6. A very smooth sidewall is observed.

Sometimes the 220 nm silicon film needs to be partially etched. For electrical connection of a pn junction modulator, etch depth is usually about 170 nm. To form shallow gratings of grating coupler, 50 nm to 60 nm etch is common. Rib waveguide is also used in directional couplers to enhance evanescent coupling. A slow etch rate is critical for these partial etches. Partial etch with the Pseudo Bosch described above was performed using ZEP520A as an etching mask. The sample was manually cleaved and inspected in an SEM at a tilt angle of about 90 degrees. The cross-section SEM image of rib waveguide with 50 nm remaining silicon is shown in Fig. 2.7. The measured thickness of remaining silicon is 51.1 nm after etching 70 s, indicating that the etch depth is well controlled. Note that the resist on top of the waveguide was not stripped.

To conclude, a calibrated EBL and ICP RIE process for waveguide fabrication is presented. Features of varying critical dimension can be fabricated accurately. Sidewall of waveguide after the dry etching is smooth. And partially etch is achieved by adjusting the etch time.

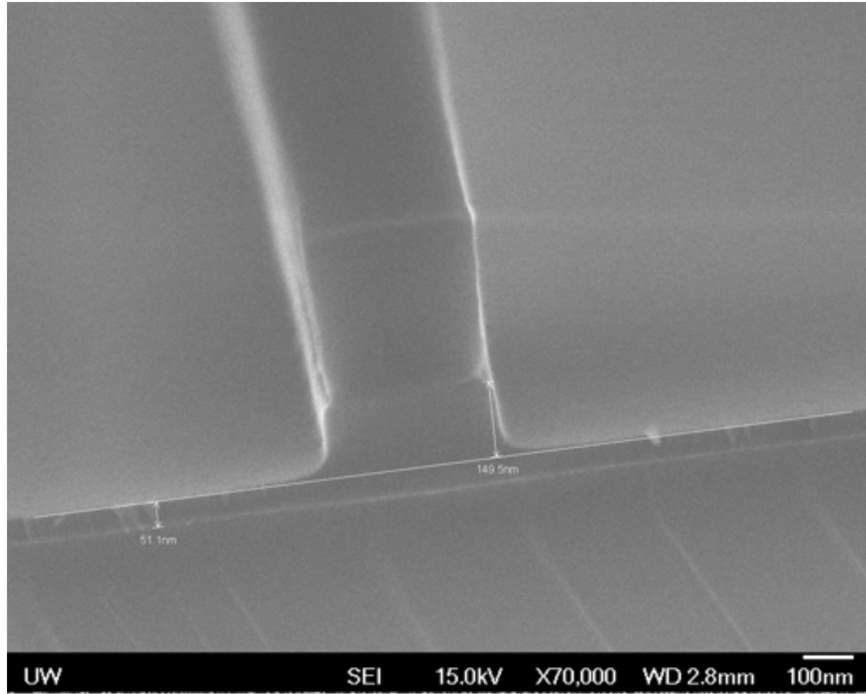

Figure 2.7 SEM image of a rib waveguide. ZEP520A was used as etching mask. Etch recipe was the same to that in Fig. 2.6. Etch time was 70 s and remaining silicon thickness was 51 nm.

Chapter 3. Y-Junction

A low loss and compact Y-junction that splits power of the input waveguide equally into two branches is one of the most basic components of a silicon photonic system. It could be readily used in the MZI structure to build a low loss modulator. Theoretically a Y-junction with small enough splitting angle will have low loss. Unfortunately such Y-junction could not be fabricated in a standard CMOS process due to the sharp corner. Usually sharp corners are a violation of CMOS foundries' minimum feature design rule. In this chapter, we present the measurement of a Y-junction with an abrupt waveguide discontinuity showed in Fig. 1.6, and introduce self-imaging property of multimode waveguides by mode propagation analysis. In the end, a novel Y-junction designed by finite difference time domain (FDTD) method and particle swarm optimization (PSO) design is presented.

I. Conventional Y-junctions

The layout of a junction consisting of two circular bends without breaking the design rule is shown in Fig. 3.1. It consists of a straight waveguide with a taper and two branches. Constrained by a minimum feature size of 0.2 μm in the design rule, an abrupt discontinuity at the splitting position is intentionally placed. Test structure of the Y-junction is shown in Fig. 3.1. Grating couplers showed in Chapter 1 is used for coupling light on and off the chip. A very conservative bend radius of 30 μm is used to ensure negligible losses from waveguide bends.

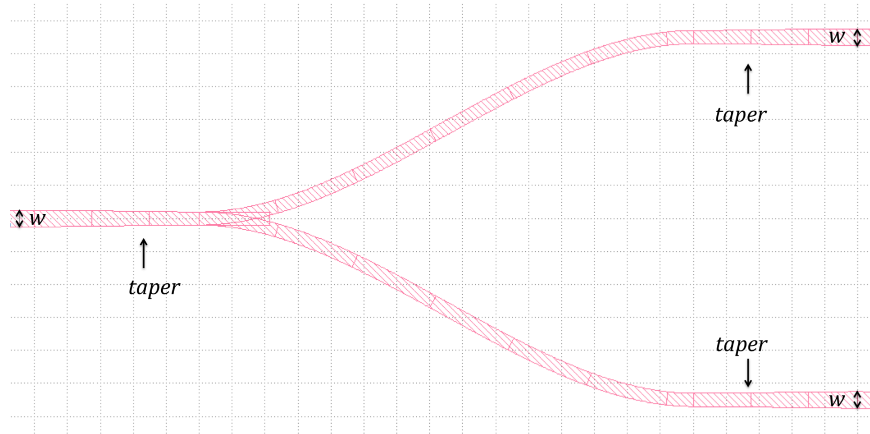

Figure 3.1 Layout of the conventional Y-junction. Red means 220 nm thick silicon. 500 nm waveguide is tapered down to 400 nm and then splits into two branches of equal length.

The device was tested by coupling light from a single mode fiber into Port A, as shown in Fig. 3.2, and detecting light coming out of Port B and Port C. Assuming two branches are symmetric, optical power split into Port B and Port C should be the same. Ideally the Y-junction is adiabatic, i.e., there is no excess splitting loss. Power from either Port B or Port C should be 3 dB lower than that of the input Port A. On the other hand, there is also 3 dB loss for light coupling into either Port B or Port C and out of Port A. Although this is true based on reciprocity, it might be a little bit counterintuitive at first look since one usually expects all light goes into Port B will come out of Port A. The 3 dB power loss in this case can be explained by the mode evolution in the structure. As the optical mode in Port B approaches the Y-junction, it is not the fundamental mode the waveguide system any more due to the presence of the other branch. The field in the original mode can be decomposed equally into symmetric and anti-symmetric mode of the branch structure. The symmetric and anti-symmetric modes are also called even or odd modes in literature. The symmetric mode is squeezed into the fundamental mode of waveguide connected to Port A, and then coupled off the chip via the grating coupler. The anti-symmetric mode is

squeezed into the first order mode of the waveguide to Port A, which is not a guided mode and the power leaks out of the waveguide gradually. Hence half of the power is lost.

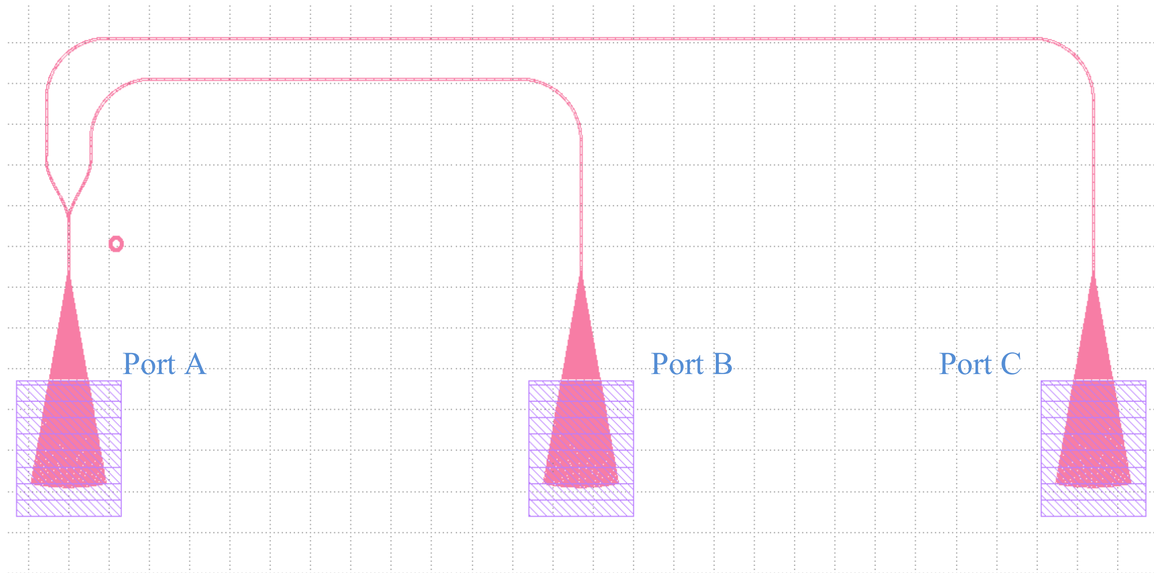

Figure 3.2 Layout of Y-junction test structure. Red means 220 nm silicon; blue and red together means 160 nm silicon. 0 near the left grating coupler is device ID.

Typical spectrum of the test structure is shown in Fig. 3.2. The parabola curvature is from the grating couplers, as shown in Fig. 1.3. The fringes with a periodicity of about 5 nm are from non-ideal TE polarization of light fed into the grating coupler. The TM component of input fiber is partly accepted by the grating coupler. TE and TM light of the single mode fiber have different phases and interference after they are coupled into the fundamental mode of the silicon waveguide. These fringes can be minimized to sub-0.5 dB with a polarization controller. The "high frequency" fringes with a periodicity of about 1 nm are from the Fabry-Perrot cavity formed by the grating coupler loop. For an adiabatic Y-junction, the difference between the spectra is 3 dB. Actual difference is larger due to excess loss from scattering and back reflection. The average excess loss is

determined to be 1.5 ± 0.3 dB. Over 1 dB excess loss per junction is too much for system level integration.

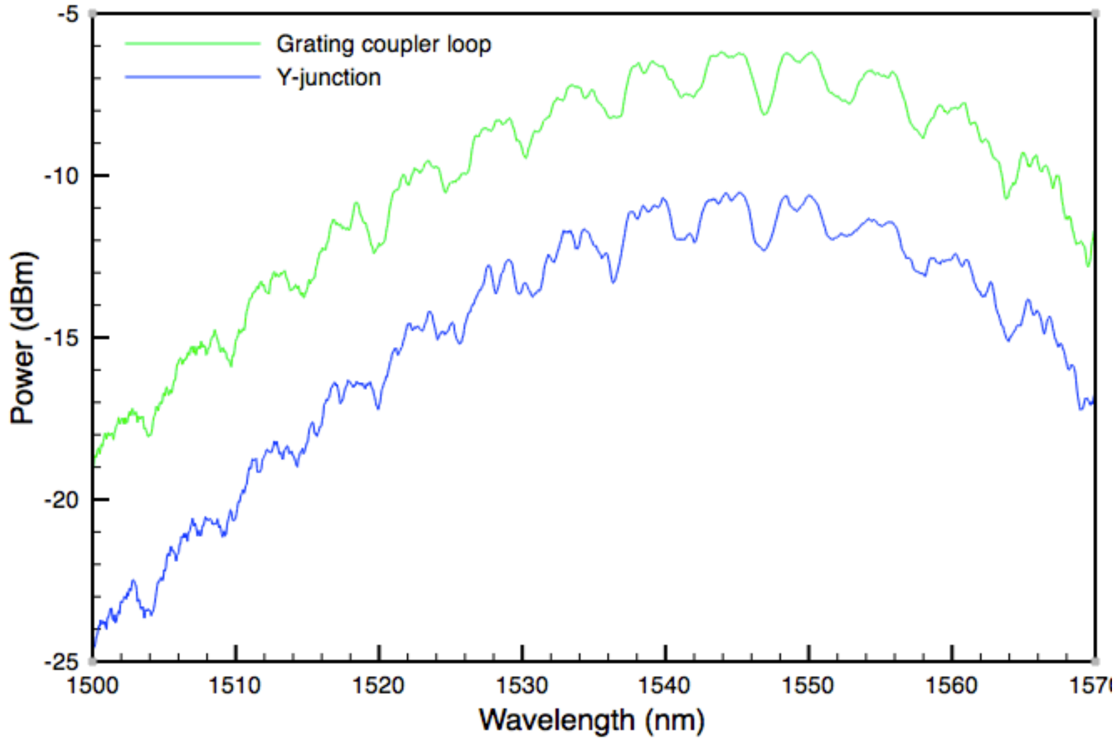

Figure 3.3 Spectra of Y-junction test structure and grating coupler loop

II. Multimode interference couplers

The major source of excess loss of conventional Y-junction is the abrupt waveguide discontinuity at the very center of waveguide, where the modal field has its peak value, as shown in Fig. 1.2. The optimal case should be that modal field at splitting position is zero at the center and maximum at the interface with access waveguides. This can be achieved by using multimode interference (MMI) couplers. We follow Ref. 4 for a 2D mode propagation analysis to illustrate the self-imaging effect of MMIs. As shown in Fig. 2.3, z is the propagation direction and y is the transverse direction. The incidental field can be decomposed into the eigenmodes of the multimode region.

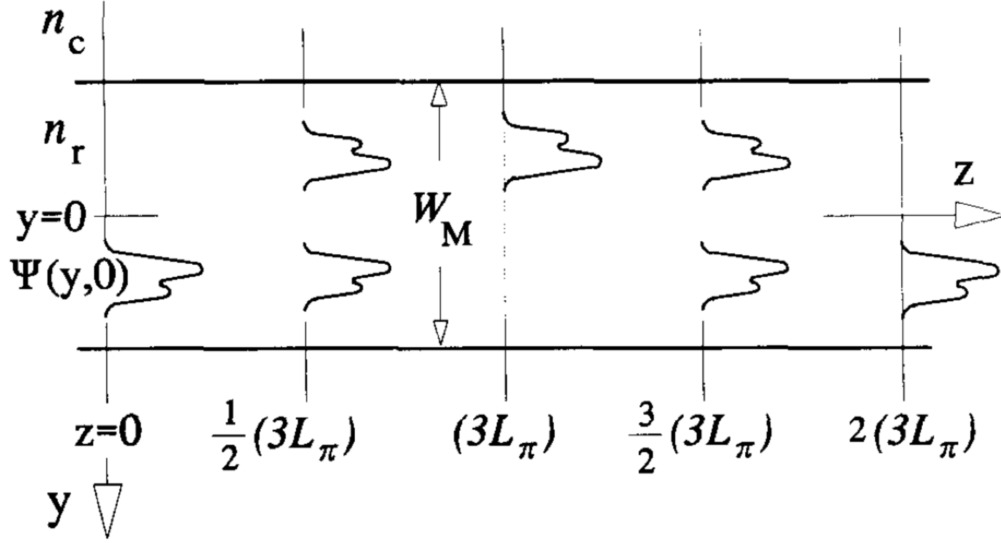

Figure 3.4 Sketch of MMI mode propagation and self-imaging effect [4]. n_c is the cladding material refractive index, and n_r is the waveguide ridge refractive index. $\Psi(y,0)$ is the incidental field. W_M is the width of the waveguide. L_π is the beating length of two lowest modes.

$$\psi(y,0) = \sum_{i=0}^{N-1} c_i \varphi_i(y) \tag{3.1}$$

where

$$c_i = \int \psi(y,0) \varphi_i(y) dy \tag{3.2}$$

After propagation over some distance z,

$$\psi(y,z) = \sum_{i=0}^{N-1} c_i \varphi_i(y) e^{-j\beta_i z} = e^{-j\beta_0 z} \sum_{i=0}^{N-1} c_i \varphi_i(y) e^{-j(\beta_0-\beta_i)z} \tag{3.3}$$

Assume strong confinement approximation,

$\varphi_i = \cos(k_i y)$ for symmetric mode and

$\varphi_i = \sin(k_i y)$ for anti-symmetric mode

where $k_{y,i} = \frac{(i+1)\pi}{W}$, and $k_{y,i}^2 + \beta_i^2 = k_0^2 n_r^2$,

hence,

$$\beta_i \approx k_0 n_r - \frac{(i+1)^2 \pi \lambda_0}{4 n_r W^2}, \tag{3.4}$$

The difference in propagation constants,

$$\beta_0 - \beta_i = i(i+2)\frac{\pi\lambda_0}{4n_r {W_M}^2} = \frac{i(i+2)\pi}{3L_\pi} \tag{3.5}$$

where $L_\pi = \frac{\pi}{\beta_0 - \beta_1}$. So the field distribution at distance z can be expressed in terms of L_π,

$$\psi(y,z) = \sum_{i=0}^{N-1} c_i \varphi_i(y) e^{-j\frac{i(i+2)\pi}{3L_\pi}z} \tag{3.6}$$

For $L = 6L_\pi, \psi(y, 6L_\pi) = \psi(y, 0)$ (3.7)

For $L = 3L_\pi, \psi(y, 3L_\pi) = \psi(-y, 0)$ (3.8)

For $L = \frac{3m}{2}L_\pi$, where m is an odd number,

$$\psi\left(y, \frac{3m}{2}L_\pi\right) = \frac{1+(-j)^m}{2}\psi(y,0) + \frac{1-(-j)^m}{2}\psi(-y,0) \tag{3.9}$$

From the mode propagation analysis, we can see single or multiple images of the input field appears at different positions of the multimode waveguide. If we choose $L = \frac{3m}{2}L_\pi$, the MMI can be used as 1 x 2 power splitters. In the above analysis, no assumption is made on mode excitations. If the input single mode waveguide is placed in the center, y=0 in Fig. 3.3, only even mode will be excited, i.e. $c_i = 0$ if i is an odd number. If the excited modes are reduced in Eq. 3.3, the length needed for 1 x 2 self-imaging will also be reduced. The insertion loss of a 1 x 2 MMI coupler with multimode section of size 3 µm x 7.6 µm is reported to be lower than 0.3 dB [5], which is 1 dB lower than that of a conventional Y-junction. However, the footprint is increased. For such a basic device, we want it to be very compact.

III. Y-junction design by FDTD and Particle Swarm Optimization

More advanced structures than a section of multimode waveguide is needed to build a low loss and compact Y-junction. For non-translational symmetric structures, modal

propagation analysis become much more complicated. Sanchis et al reported design, fabrication and measurement of a low insertion loss and low crosstalk waveguide crossing [6]. Device geometry optimization was done by FDTD combined with genetic algorithm (GA). Similar design methodology is applied to Y-junction design here. PSO, instead of GA, is used for optimization.

A. Introduction to FDTD

When the device size is comparable to the operating wavelength, its electromagnetic properties are usually simulated by FDTD. In the differential form of Maxwell's equations 3.10 – 3.11, it can be seen that the time derivative of H-field is dependent on the curl of E-field, vice versa for H-field.

$$\nabla \times E = -\mu \frac{\partial H}{\partial t} \tag{3.10}$$

$$\nabla \times H = \varepsilon \frac{\partial E}{\partial t} - J \tag{3.11}$$

In Cartesian coordinate system, the Eq. 3.10 is equivalent to the following scalar Eq. 3.12 – 3.14,

$$-\mu \frac{\partial H_x}{\partial t} = \frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z} \tag{3.12}$$

$$-\mu \frac{\partial H_y}{\partial t} = \frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x} \tag{3.13}$$

$$\mu \frac{\partial H_z}{\partial t} = \frac{\partial E_x}{\partial y} - \frac{\partial E_y}{\partial x} \tag{3.14}$$

To solve the equations numerically, the electromagnetic fields are discretized in a style proposed by Yee [7], in which the field components are discretized at slightly different special positions as shown in Fig. 3.4. After discretization, the H-field at any point can be updated in time using the stored H-field value and curl of E-field at the same spatial volume, for example, discrete form of Eq. 3.12 is shown below.

$$\mu \frac{H_x^{n+\frac{1}{2}}\left(i,j+\frac{1}{2},k+\frac{1}{2}\right)-H_x^{n-\frac{1}{2}}\left(i,j+\frac{1}{2},k+\frac{1}{2}\right)}{\Delta t} = \frac{E_y^n\left(i,j+\frac{1}{2},k+1\right)-E_y^n\left(i,j+\frac{1}{2},k\right)}{\Delta z} - \frac{E_z^n\left(i,j+1,k+\frac{1}{2}\right)-E_z^n\left(i,j,k+\frac{1}{2}\right)}{\Delta y} \quad (3.15)$$

Other field components can be updated next in the same way. This process is repeated until the desired transient or steady state electromagnetic field behavior is fully solved.

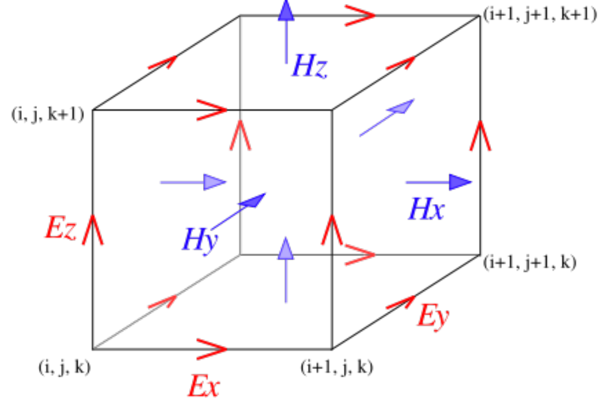

Figure 3.5 Yee cell used in FDTD discretization

B. *Introduction to PSO*

PSO is a computational stochastic optimization method similar to the GA. It is initially inspired by the social behavior of flocks of birds or schools of fish, and has been successfully applied to electromagnetic optimization problems [8]. In PSO, the potential solutions, called particles or agents, are initialized at random positions with random velocities in the parameter space. A figure of metric function is defined to evaluate the particle position according to the optimization goal. The best position for each individual particle is recorded, as well as a global best position ever achieved by any particle in the swarm. The position of a particle is updated by the following equation,

$$x_n = x_n + \Delta t * v_n \quad (3.16)$$

$$v_n = \omega * v_n + c1 * rand() * \left(p_{best,n} - x_n\right) + c2 * rand() * \left(g_{best,n} - x_n\right) \quad (3.17)$$

where $v_n$and x_n are particle's velocity and position in nth dimension of the parameter space, and $p_{best,n}$ and $g_{best,n}$ are individual and global best positions. Apparent from Eq. 3.17, the new velocity is the old velocity scaled by ω and increased the direction of $p_{best,n}$ and $g_{best,n}$. ω , known as the inertial weight, is a measurement of how much a particle would like to stay at the old velocity. $c1$ determines how much a particle is influenced by the memory of its best position, thus sometimes called cognitive rates. And $c2$ is a factor demining how much the particle is affected by the global best position of the whole swarm, hence called social rates. The two random numbers are used to simulate the unpredictable behavior of natural swarm. It can be seen that the particle velocity is large when it is far from $p_{best,n}$ or $g_{best,n}$, becomes smaller as it is closer to the best position and gets pulled back after flying over. The optimization is stopped when the figure of merit is good enough or a large number of iteration is reached.

C. *Y-junction design by FDTD and PSO*

The goal for this design optimization is to be able to split the power in the fundamental mode of a 500 nm x 220 nm waveguide into two branches of identical waveguides with minimal insertion loss and device footprint. The device has to live in the design rules, i.e. minimum feather size 0.2 μm. The Y-junction schematic is shown in Fig. 3.5. The taper from 500nm to 1.2 μm is chosen to be 2 μm long. It was discretized into 13 segments along the direction of propagation. The widths of each segment are the parameters to be optimized. The edge of the taper is determined by spline interpolation of these 13 points. Figure of merit during the PSO optimization is the power in TE0 mode at either branch. It was calculated by the mode integral of TE0 mode of a 500 nm x 220 nm waveguide with the detected filed at the output branch. The swarm population was set to 30. 2D FDTD

was used as an approximation of 3D FDTD for computation efficiency. A commercially available FDTD code wad used [9]. Within 50 iterations, one solution with sub-0.2 dB insertion loss emerged, as shown in Table 3.1.

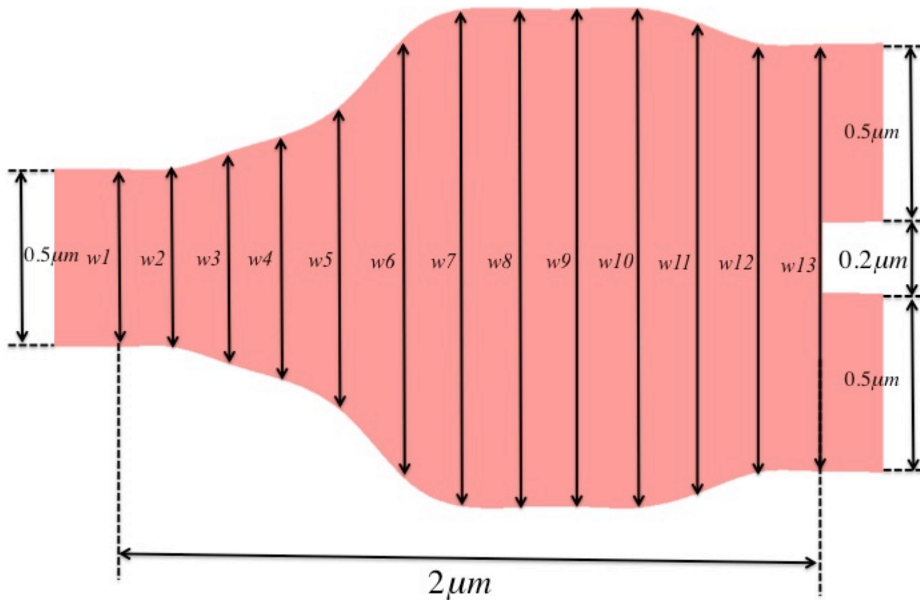

Figure 3.6 Discretization of the Y-junction taper in PSO simulation.

w1	w2	w3	w4	w5	w6	w7	w8	w9	w10	w11	w12	w13
0.5	0.5	0.6	0.7	0.9	1.26	1.4	1.4	1.4	1.4	1.31	1.2	1.2

Table 3.1 A solution of Y-junction optimization problem. Units in μm

Then 3D FDTD was run on this solution to double check the result with a mesh equal to 1/34 of the free space wavelength. The insertion loss was determined to be 0.13 dB. No noticeable scattering is seen in the major electric field component, as shown in Fig. 6. The device is currently being fabricated at Institute of Microelectronics, Agency for Science Technology and Research (IME A*STAR) in Singapore via the OpSIS silicon photonics foundry service.

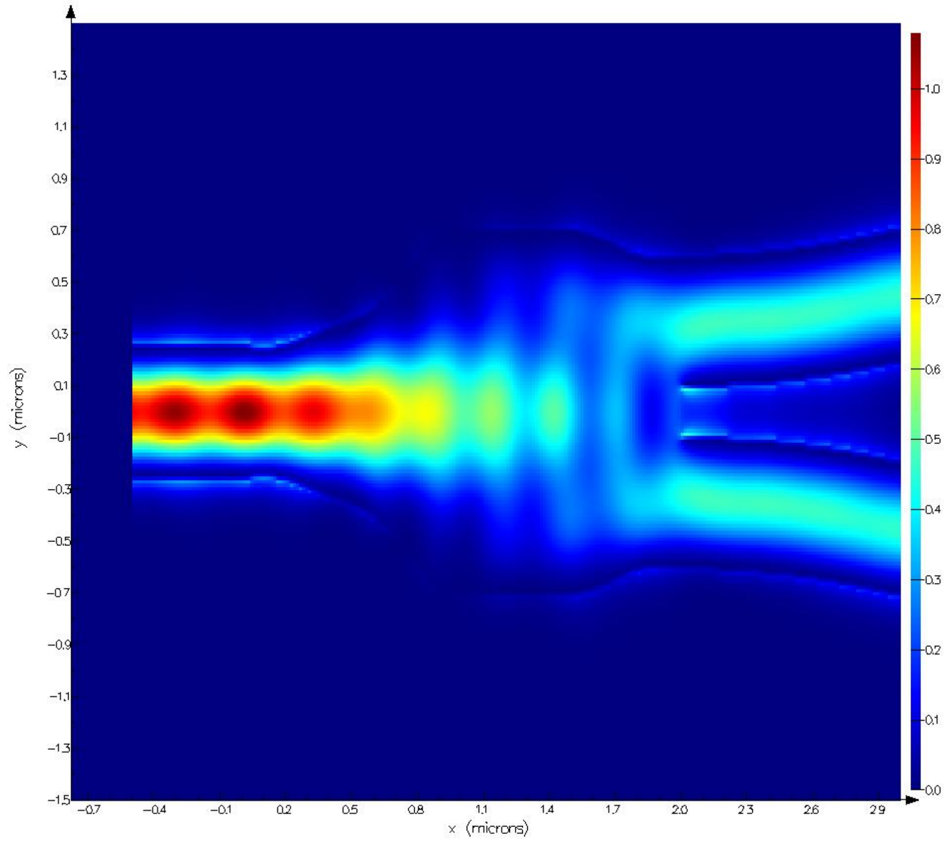

Figure 3.7 Electric field distribution in the optimized Y-junction simulated by 3D FDTD

Chapter 4. Directional Couplers

In addition to 50% power splitters as described in Chapter 3, other coupling ratios, such as 1%, 5%, and 10%, also have important applications in a photonic system. Directional coupler (DC) has the advantage of conveniently achieving arbitrary coupling ratio by adjusting the coupling length. A key device relying on evanescent coupling between waveguides is the ring resonator, which can be used as biosensors or ring modulators. In this chapter, principle of DCs is briefly reviewed, then measurements of silicon waveguide DCs is presented. In the end, designs on robust DC are discussed.

I. Introduction to DCs

A schematic layout of a simple DC and corresponding cross-section is shown in Fig. 4.1. At y=0 WG II appears in the vicinity of WG I, where the evanescent field is not zero. A mathematical description of the electromagnetic behavior can be derived by assuming WG II as a perturbation of the refractive index of WG I. A more intuitive way of explaining the power coupling is from the aspect of modal excitation and propagation analysis.

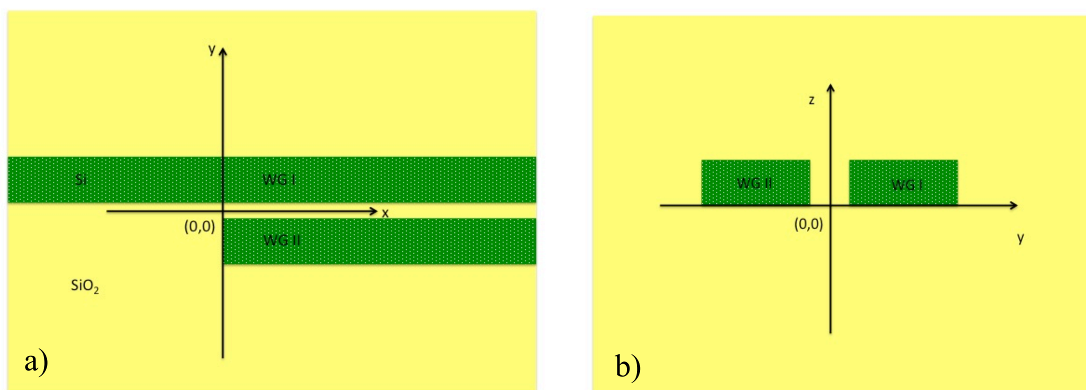

Figure 4.1 Top view a) and cross-section b) of a directional coupler

The mode of a single waveguide is shown in Fig. 1.2. For the waveguide system in presence of WG II, there are two propagation modes, as shown in Fig. 4.2. One mode is symmetric and the other is anti-symmetric, similar to what we have discussed in Chapter 3. These two modes will be excited by the fundamental mode of WG I with equal modal power, and they will be in phase at y=0. However, the symmetric and anti-symmetric modes have different propagation constant, their relative phase will change periodically, causing interference. Beating between the two modes is the source of evanescent power coupling.

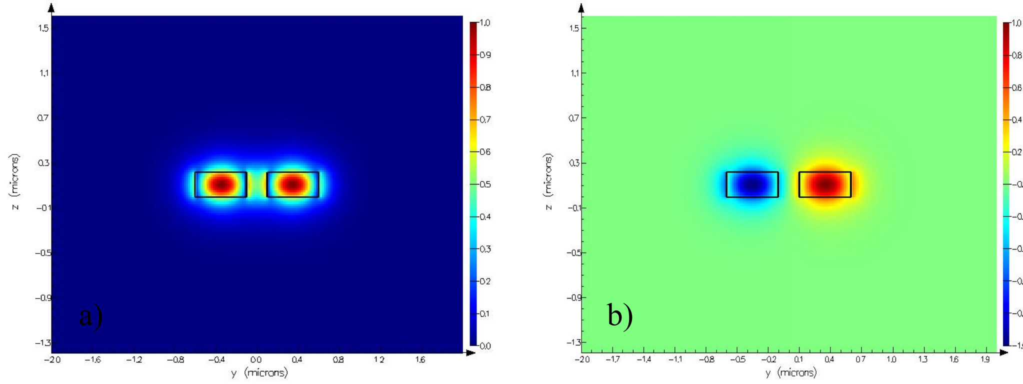

Figure 4.2 Symmetric a) and anti-symmetric mode b) of directional coupler

The symmetric and anti-symmetric modes can be approximated by the sum and difference of unperturbed waveguide mode, as shown in Eq. 4.1 – 4.2. n_{symm} and n_{asym} are the effective indices of symmetric mode and asymmetric mode respectively.

$$E_{symm} = E_{WG\,I} + E_{WG\,II} \tag{4.1}$$

$$E_{asym} = E_{WG\,I} - E_{WG\,II} \tag{4.2}$$

$$\Delta n = n_{symm} - n_{asym} \tag{4.3}$$

$$n_0 = \frac{1}{2}(n_{symm} + n_{asym}) \tag{4.4}$$

The field pattern as a function of x can be expressed by Eq. 4.5. It can be seen that powers in both waveguide have a sinusoidal dependence on the coupling length.

$$E(x) = E_{symm}\exp\left(i\frac{2\pi n_{symm}}{\lambda_0}x\right) + E_{asym}\exp\left(i\frac{2\pi n_{asym}}{\lambda_0}x\right)$$

$$= (E_{WG\,I} + E_{WG\,II})\exp\left(i\frac{2\pi n_{symm}}{\lambda_0}x\right) + (E_{WG\,I} - E_{WG\,II})\exp\left(i\frac{2\pi n_{asym}}{\lambda_0}x\right)$$

$$= 2E_{WG\,I}\exp\left(i\frac{2\pi n_0}{\lambda_0}x\right)\cos\left(\frac{\pi\Delta n}{\lambda_0}x\right) + 2iE_{WG\,II}\exp\left(i\frac{2\pi n_0}{\lambda_0}x\right)sin\left(\frac{\pi\Delta n}{\lambda_0}x\right) \quad (4.5)$$

II. A silicon waveguide DC

Usually the second waveguide is introduced to the vicinity of the first waveguide gradually by a bend or a taper to reduce reflection. In our silicon photonic platform, rib waveguide instead of strip waveguide is used to enhance the coupling between the waveguides, thus reducing the coupling length needed for a specific coupling ratio. The test structure of the rib waveguide DC is shown in Fig.4.3. Light is coupled into silicon waveguide via the grating coupler on the left. The strip to rib waveguide transition is almost adiabatic by using a taper in the 90 nm thick silicon layer. Coupling length is varied from 0 μm to 25 μm by a step of 0.5 μm. The measured spectrum is parabolic due to the use of grating couplers, but the difference in peak power value is determined by the coupling efficiency.

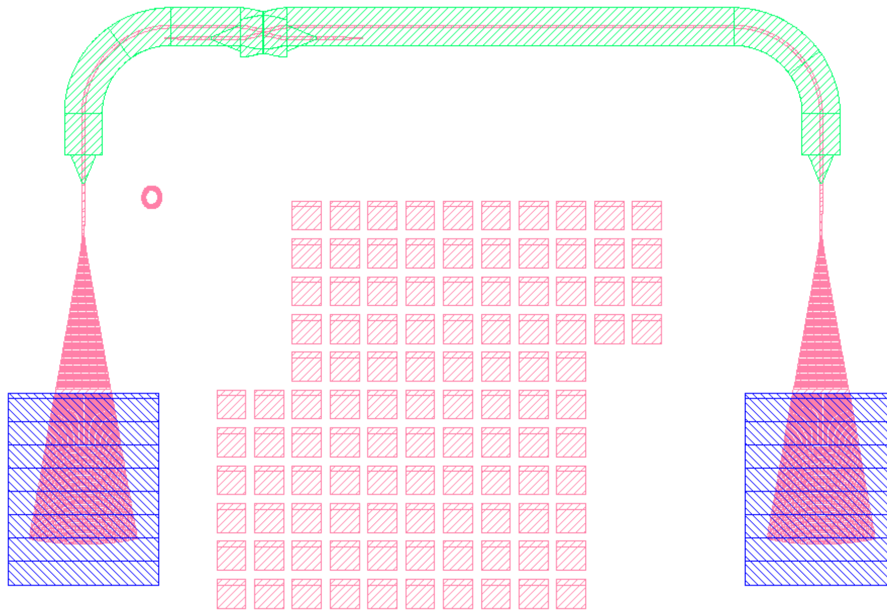

Figure 4.3 Layout of rib waveguide DC test structure. GC layout is the same to that of Fig. 1.3. Green only means 90 nm thick silicon will be left. Red only or red overlapping with green means silicon thickness is 220 nm.

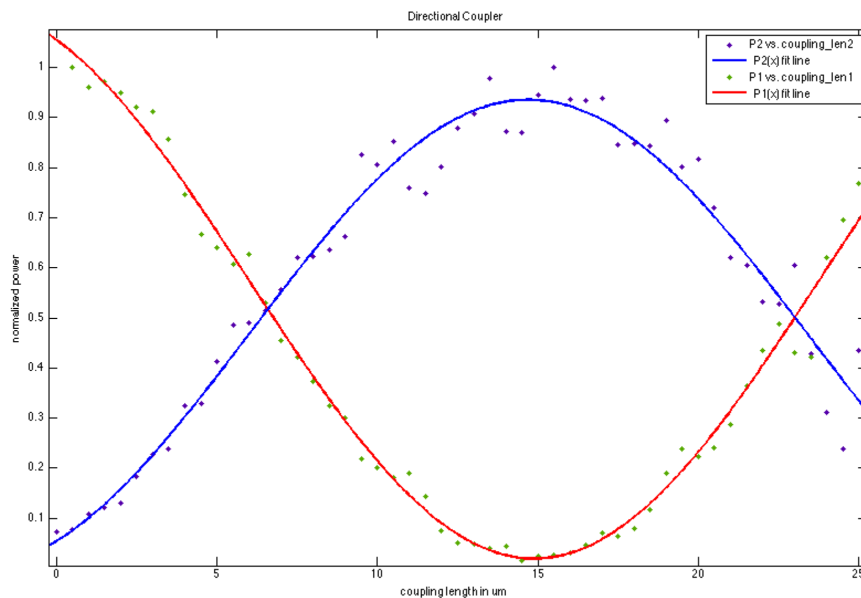

Figure 4.4 Directional and cross-coupled power as a function of coupling length. Dots are measured data; solid lines are fitted curves using sinusoidal functions.

Measured peak power as a function of coupling length is plotted in Fig. 4.4. Test data were fitted by the sinusoidal function in Eq. 4.6.

$$f(x) = a0 + a1 * \cos(x * w) + b1 * \sin(x * w) \quad (4.6)$$

w=0.1777 with a 95% confidential bound (0.1635,0.2026) for directional coupled power and w = 0.1806 with 95% confident bounds (0.1586, 0.2026) for cross coupled power were obtained. The corresponding coupling length for 100% power coupling is 17.6792 μm and 17.3953 μm respectively.

III.Robust evanescent coupling

The coupling ratio of directional couplers is sensitive to fabrication variations, since the evanescent field drops exponentially. Waveguide variation can be from variation of rib width or thickness of partially etched layer. Cascading two directional couplers, with the second one undo the coupling ratio shift introduced by the first one, can reduce coupling ratio sensitivity. The idea appeared in literature first as a solution to the wavelength dependent of coupling ratio [10], and could also be used to fix fabrication variation sensitivities. Here I follow Ref. 11 to demonstrate this improvement.

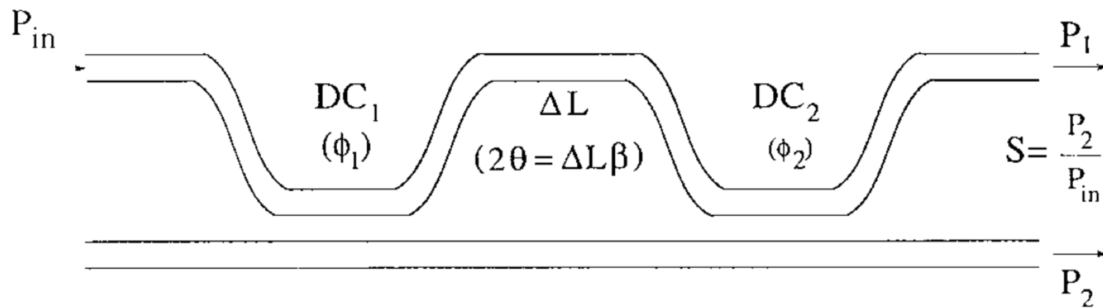

Figure 4.5 Schematic of cascaded DC [11]

As shown in Fig. 4.5, a phase delay of 2θ is introduced between two cascaded directional couplers DC1 and DC2. The coupling ratio of cascaded DC is expressed by Eq. 4.7.

$$S = cos^2\theta sin^2(\phi_1 + \phi_2) + sin^2\theta sin^2(\phi_1 - \phi_2) \tag{4.7}$$

where

$$\phi_i = \int_0^{L_i} K(\lambda, z)dz \tag{4.8}$$

$$2\theta = \beta(\lambda)\Delta L \tag{4.9}$$

We can express $\phi_i = (1 + \delta)\phi_{i0}, (i = 1,2)$, where ϕ_{i0} is the designed value. δ is a detune factor to quantify the deviation of ϕ_i from ϕ_{i0} due to fabrication variations. A plot of coupling ratio as a function of δ for different targeting coupling ratio S_0 is shown in Fig. 4.6. The dashed line is a normal DC for 50% coupling. It can be seen that the coupling ratio of cascaded DC is extremely flat over a wide range, while normal DC depends almost linearly on δ. So the cascaded DC is a good solution for achieving robust coupling for an arbitrary coupling ratio.

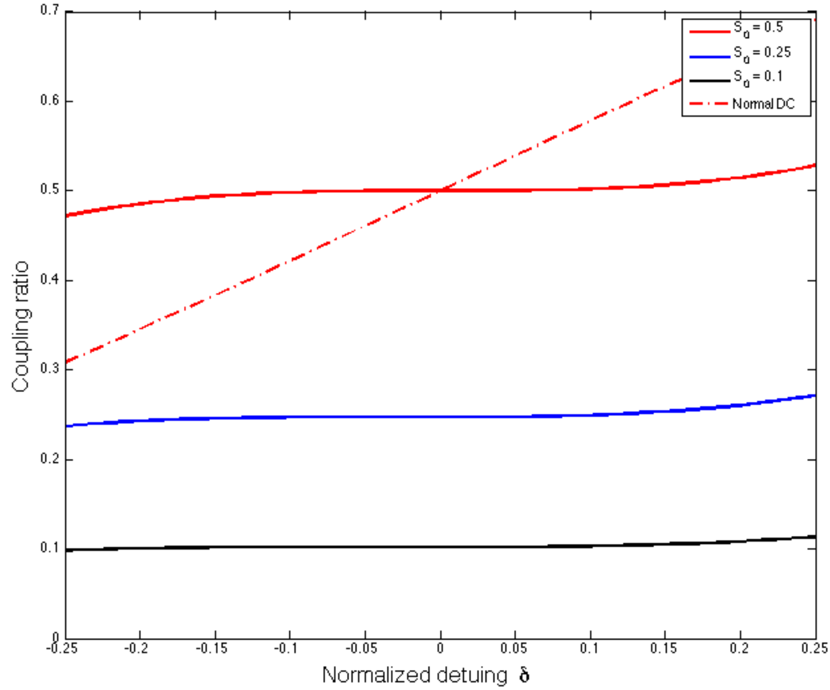

Figure 4.6 Coupling ratio as a function of detuning factor

Chapter 5. Semiconductor Laser Coupler

There have been investigations by adding erbium, or using strained germanium to make a laser on silicon photonic platform [12, 13]. But an efficient electrically pumped laser hasn't emerged by the time of this thesis. Edge couple a semiconductor laser die to the silicon photonic chip is one of the most practical solutions. Similar to coupling between silicon waveguides and optical fiber, a coupler need to be carefully designed to buffer the mode mismatch between a silicon waveguide and a IIIV gain waveguide. In this chapter, a coupler made by ultra thin waveguide, as well as an external cavity laser structure based on such coupler, is proposed.

I. Thin waveguide coupler

A typical semiconductor laser usually outputs a Gaussian beam of mode field diameter (MFD) 3 μm x 1 μm. The near field mode profile is plotted in Fig. 5.1. It is much larger compared with the mode pattern of a 500 nm x 220 nm silicon waveguide, as shown in Fig. 1.2. The mismatch in horizontal direction can be fixed relatively easily by tapering the waveguide width from 500 nm slowly to about 3 μm. However, the thickness of silicon is determined by the SOI wafer and cannot be made larger without significantly increasing the process complexity.

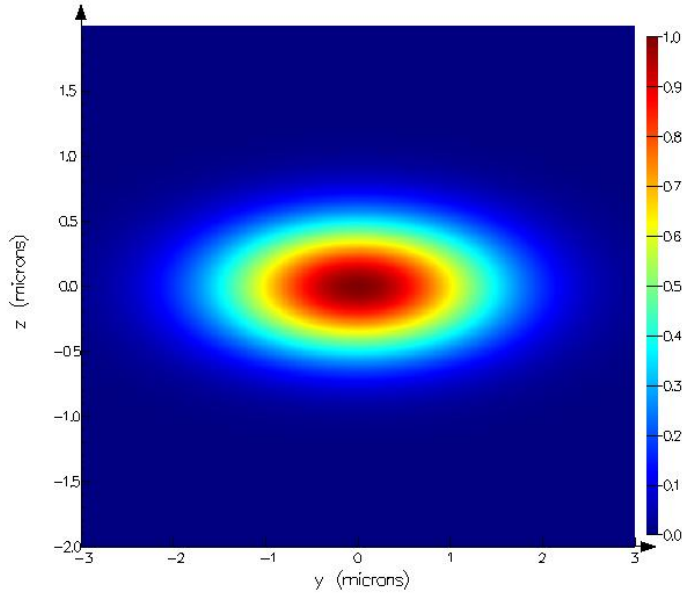

Figure 5.1 Typical modal profile of a semiconductor laser

Lipson et al reported efficient edge coupling between silicon waveguide and optical fiber by tapering the silicon waveguide width down to 80 nm [ref]. As the waveguide becomes narrower, it is not a guiding structure any more. Light will leak out and matches the mode of an optical fiber. Similarly, modal field of a thin waveguide consisting a 3 μm x 0.05 μm silicon core is not tightly confined. The thin waveguide modal profile is shown in Fig. 5.2. It can be seen that although optical field leaks out from the high index silicon part, it is still a guide mode. Test data from runout devices agree with the conclusion above, and show a propagation loss of 6 dB/cm. This expanded mode have much better overlap with the semiconductor laser output mode, thus effectively reduce the coupling loss. A mode overlap integral shows a sub-1 dB insertion loss if two waveguides are flush. By observing the mode, we could determine that the vertical direction is more critical compared to the horizontal direction. A slight increase of the waveguide width will cause the mode to shrink. If the waveguide thickness becomes 90 nm, over 1.5 dB insertion loss is expected. Insertion loss as a function of waveguide facet separation is

simulated by 3D FDTD and summarized in Fig. 5.3. It can be seen that coupling loss is lower than 1 dB for a sub-200 nm facet spacing. This is within the resolution of our optical stages.

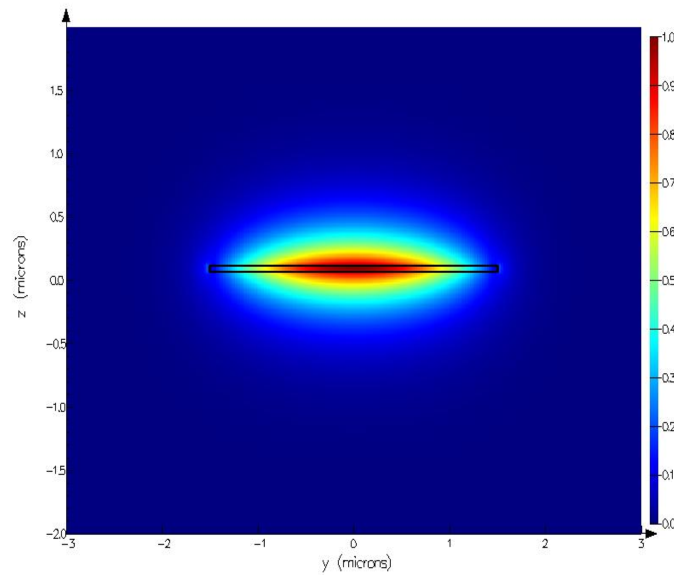

Figure 5.2 Modal profile of a 3 μm x 0.05 μm silicon waveguide

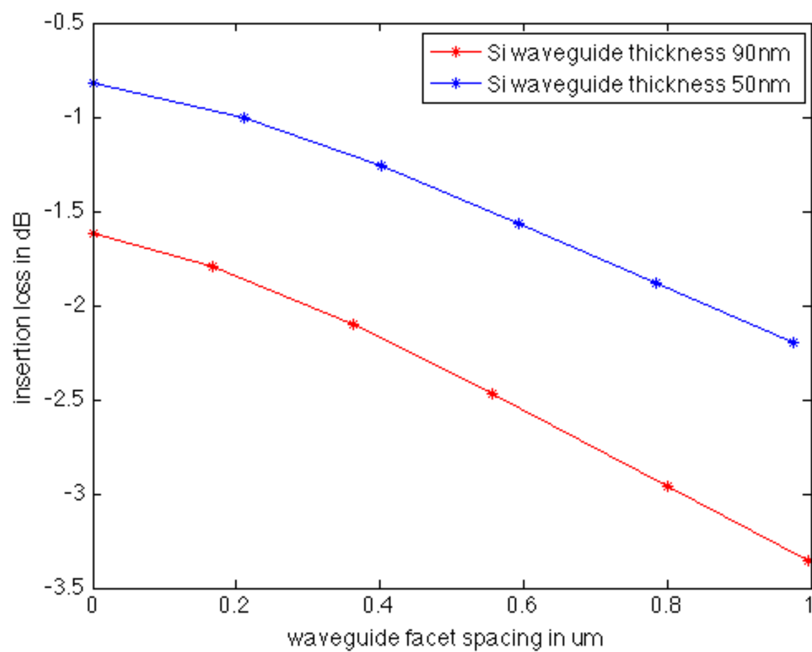

Figure 5.3 Insertion loss as a function of waveguide facet spacing

Also, there is always misalignment of the center of two waveguides. Dependence of insertion loss on the misalignment value in both horizontal and vertical direction are simulated assuming a waveguide facet separation of 200 nm. From Fig. 5.4 we can see insertion loss is still sub-2 dB with in the 200 nm resolution of our optical stage.

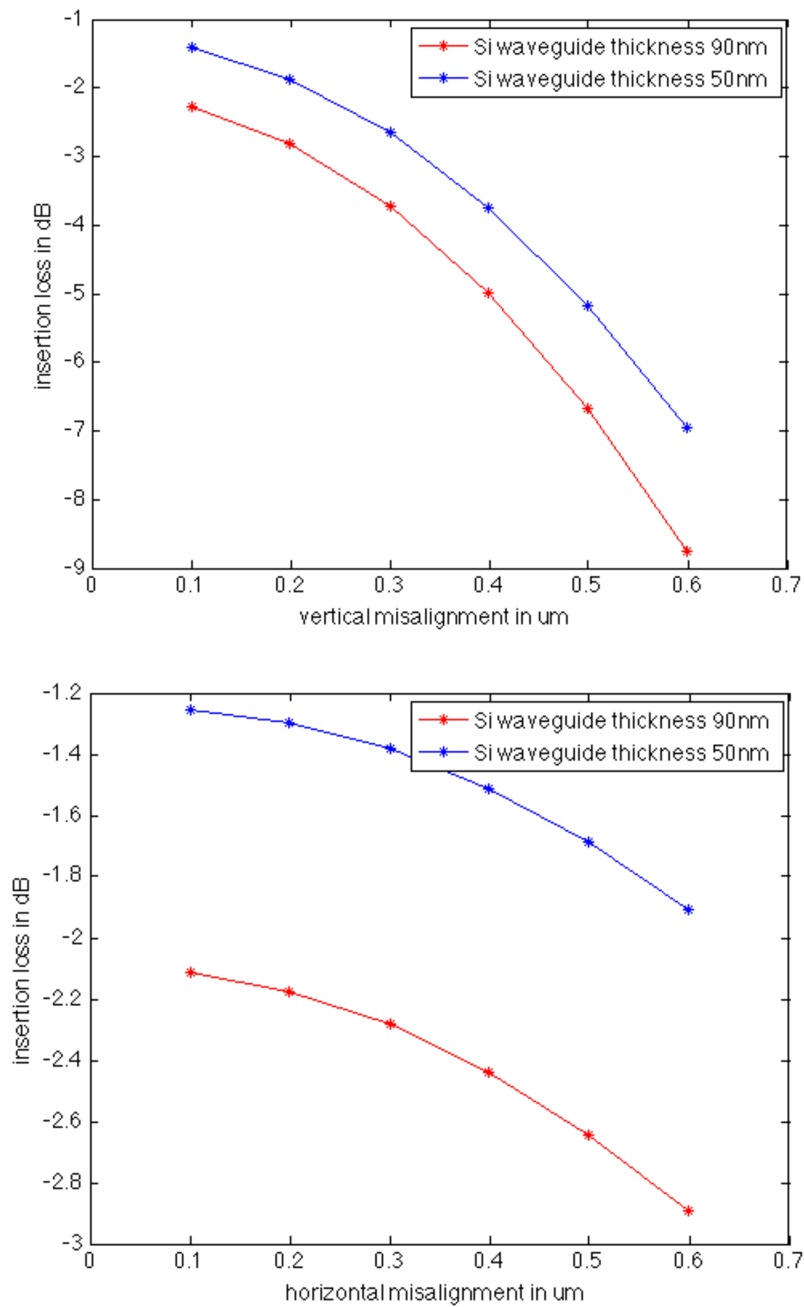

Figure 5.4 Dependence of insertion loss on waveguide misalignment

II. External cavity lasers

Efficient coupling between a IIIV gain waveguide and a silicon waveguide brings more than a light source to the silicon photonic platform. It means part of the cavity can be on the silicon chip, providing much more design flexibility. The schematic design of such laser is shown illustrated in Fig. 5.5. Note that angled facets are used to reduce back reflection into the waveguide, similar to the APC fiber connectors. The front facet of IIIV waveguide is coated with anti-reflection (AR) film. The narrow band reflector on the silicon chip consists of a ring resonator and Y-junction, with two branches tied together. Laser output is extracted from the cavity by directional couplers. The laser die is first aligned to the silicon chip virtually using a high magnification scope. A wide area detector is placed on top of the grating coupler pair to monitor their output. Laser die position is fine tuned by maximizing the large area detector photocurrent. The two chips are then wire bonded. UV cured glue is applied to firm waveguide connection. This laser can be tested using probes and fiber array. If we assume 2 dB coupling loss, and 1dB loss from the cavity on silicon chip in total, in round trip cavity loss is 6 dB, much less than a typical gain of 15 dB available from a semiconductor laser. A tunable laser is readily available by replacing the passive ring by a thermal or electrical tuned ring modulator. More functions such as narrowing the lasing line width and mode locking can also be explored. So this low loss coupler not only provide an compact light source to the silicon photonic platform, enabling applications like a transmitter right away, but also opens the door for on chip laser designs.

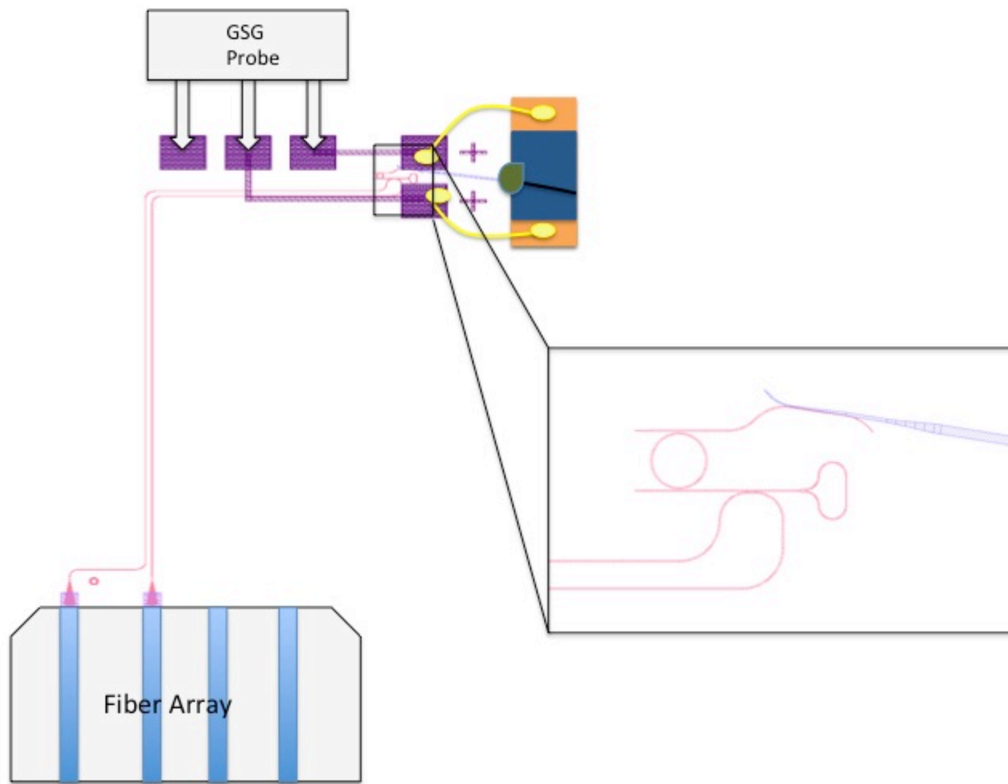

Figure 5.5 Schematic of a silicon photonic external cavity laser

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