Area and Power Reduction Techniques for Millimeter-Wave Phased-Array Transceiver Front-ends

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Abstract

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The demands for higher data rates continue to drive research for consumer products to develop new techniques for low-cost and long battery-life wireless radios. This dissertation explores and implements several single-chip CMOS integrated circuits which aim to enable high data rates for the new spectrum opportunity in future mm-Wave 5G radios as well as to improve the spectrum efficiency for current sub-6GHz communication systems.

In the mm-Wave design, a 50-58GHz 2x2 phased-array receiver (RX) for 5G communication and radar systems is described. The RX utilizes a G_m-assisted matching network (MN) to reduce the noise figure (NF) of a conventional passive mixer-first RX by placing an extra gain of ~5dB prior to the down-conversion mixers with minimal additional components. In addition to the G_m-assisted MN, this prototype phased-array RX integrates a proposed G_m-assisted MN, mixer-first RX with translational feedback, Cartesian phase shifters as a baseband beamformer, poly-phase

filters, and LO generation in TSMC 28nm CMOS, occupying a total area of 0.53mm^2. This RX achieves a NF of 7dB, gain of 26dB, input $P_{1\text{-}dB}$ of -20dBm with an 8-GHz 3-dB BW and a S_{11} lower than -10dB over 22-GHz BW. Second, a novel highly-digital 2x2 phased-array receiver implemented in TSMC 28-nm CMOS with several techniques, including a feedforward noise-suppressing front-end, reconfigurable 0-3 SMASH CT-ΔΣ ADC, and digital beamformer. This proposed receiver enables the development of digital multi-beam phased-array with improved front-end NF, reduced silicon area, and low power consumption for future wireless systems. Third, a dual-mode V-band power amplifier (PA) that utilizes a reconfigurable 2/4-way power combiner is introduced to enable two discrete modes of operation and enhance the efficiency at power back-off. The power combiner employs two techniques to further improve the PA efficiency at power back-off: 1) usage of transformers with non-uniform turns ratios to reduce the difference in impedance presented to the PA cores between the two modes and 2) utilize a proposed switching scheme to eliminate the leakage inductance associated with the disabled path in back-off power mode. The 2-stage PA achieves a peak gain of 21.4dB with a fractional BW (fBW) of 22.6% (51-64GHz). At 65GHz, the PA has a P_{sat} of +17.9dBm with an OP_{1dB} of +13.5dBm and a peak PAE of 26.5% in full-power mode. In back-off power mode, the measured P_{sat}, OP_{1dB}, and peak PAE are +13.8dBm, +9.6dBm, and 18.4%, respectively. The PAE is enhanced by 6% points at a 4.5-dB back-off. The PA is capable of amplifying a 6-Gb/s 16-QAM modulated signal with an EVM_{rms} of -20.7dB at an average P_{out}/PAE of +13dBm/13.6%, respectively. This PA was implemented in 16-nm FinFET, occupies a core area of 0.107mm^2, and operates under a 0.95-V supply.

Lastly, to improve spectrum usage of the current sub-6GHz systems, a triple-path transmitter (TX) self-interference cancellation (SIC) transceiver for full-duplex (FD) systems which achieves greater than 73dB of SIC is reported. An integrated electrical balance duplexer (EBD) is employed

and works in concert with two pre- and post-LNA RF feedforward cancelers implemented as analog finite impulse response (FIR) filters to form a combined three-path cancellation architecture that achieves a deep on-chip TX SIC over a very wide bandwidth (BW). The on-chip self-interference cancellation of 72.8/70.1/65.2dB was measured by comparing integrated channel power difference at the receiver (RX) baseband (BB) output while applying orthogonal frequency-division multiplexing (OFDM) multi-carrier 64-QAM Wi-Fi packages at the transmitter input with a 20/40/80-MHz bandwidth, respectively. The receiver noise figure (NF) degradation due to the TX SI leakage improves from 8dB to 1.6dB after turning on both RF cancelers. TX SI leakage reciprocal mixing with the RX LO phase noise (PN) was also significantly reduced by 11dB up to 1-MHz offset frequency measured at RX BB output. This work integrates the whole transceiver signal path from the analog baseband to RF. The FD prototype chip is fabricated in TSMC 40nm CMOS process with a die size of 4mm^2 that consumes 106mW (excluding PA). An Altera Cyclone III FPGA with ADC/DAC daughter board is used to emulate the digital baseband (BB) and executes a nearest neighbor search (NNS) algorithm to close the filter adaptation loop. The RX operates from 1.6GHz to 1.9GHz with a total noise figure of 8.09dB and an IIP_3 of -17dBm while operating at the highest gain of 42dB. The TX has an output P_{-1dB}/P_{sat} of 10.6dBm/12.5dBm measured at the antenna port, respectively. This chip also integrates an integer-N synthesizer with a measured locking range from 3.52GHz to 4.28GHz. The synthesizer consumes 10.4mW with a phase noise performance of -117dBc/Hz measured at 1-MHz frequency offset.

These four prototypes demonstrate various techniques to reduce power and area for future wireless systems, including the applications in mm-Wave front-ends for new spectrum opportunities with increased data rates as well as improved spectral efficient full-duplex radios for existing sub-6GHz bands.

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ACKNOWLEDGEMENTS

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Chapter 1. INTRODUCTION

The demands for higher-level wireless access and increased data rates continue to drive research to enable new spectrum opportunities, reduce form factor and lower the cost [1]. Spectrum above 24GHz, with dedicated bands of a few GHz, provides wide bandwidth (BW) and the opportunity for achieving the data rate of several Gbps. Phased-array systems are usually applied at these frequency bands to provide directional beams for data transmission using phase shifters and combiners. Traditional phased arrays employ phase shifters in the analog domain, either in the signal path or in the LO path [2] to provide only a single beam. This is because the analog implementations cannot handle the heavy loading for more than one set of phase shifters. In addition, the analog approach requires a large area and power consumption, which is not practical in multi-beam applications. In contrast, digital beamformers make multi-beam generation possible since digital circuits are less sensitive to loading, as compared to the analog blocks.

To illustrate potential applications of generating multiple beams, Figure 1.1 depicts the concept. As shown in Figure 1.1, if all devices, including base stations and mobile devices, can generate several data beams simultaneously, they can transmit and receive data using different beams at the same time, as well as serving as data relays for other users. For instance, if the data needs to be transferred from node A to node B, there are three different paths, path 1, path 2, and path 3, that can perform the transmission (see Figure 1.1). Moreover, assuming each device can generate 8 beams at the same time, the devices at node A and B can use 3 beams to transmit and receive the data through 3 different paths to increase the overall data rate, while the other 5 beams can work as relays for other users.

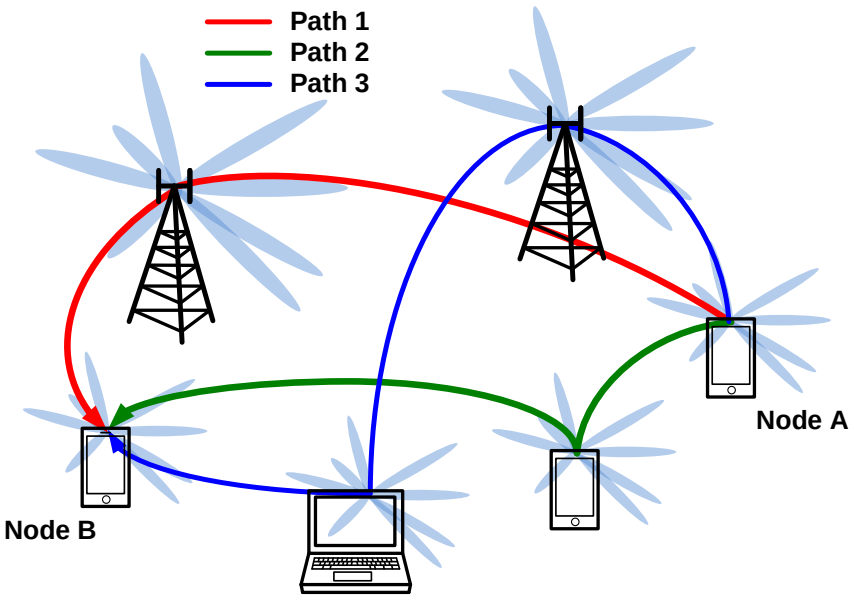


Figure 1.1. A potential application of multi-beam communication systems.

1.1 Research Objectives

This dissertation will focus on exploring and implementing novel system/circuit-level techniques to address the need for high data rates, low cost, and low power radio applications for use in new emerging 5G radios and current sub-6GHz communication systems.

1.2 Overview and Organization of the Thesis

The remainder of this dissertation is organized as follows:

Chapter 2: A brief overview of the mm-Wave system and phased-array receiver architectures is provided. The power efficiency of implementing gain stages at different operating frequency in a receiver chain will be discussed. Different beamforming topologies and their trade-offs are described.

Chapter 3: This chapter introduces a technique to improve the noise performance of conventional mixer-first receiver by incorporating the already existing matching network with a

feedforward gain path implemented in TSMC 28nm CMOS. The design and measurement results from the prototype chip are described in detail.

Chapter 4: This chapter describes the design challenges of a low-resolution phased-array front-end. The discussion comments on the considerations and feasibility of implementing phased-array receivers using very low-bit resolution analog-to-digital converters (ADC)s, even as low as 1-bit, within each element, while recovering a sufficient effective number of bits (ENOB) for the entire system. .

Chapter 5: A novel highly-digitized phased-array receiver with digital beamforming is explored in the chapter. Several novel system/circuit ideas are introduced including a feedforward nosie-suppressing front-end, a reconfigurable 0-3 SMASH CTΔΣ ADC, and the digital beamformer. The design of this TSMC 28nm prototype chip is described.

Chapter 6: This chapter presents a V-band mm-Wave power amplifier implemented in TSMC 16-nm FinFET CMOS with a novel non-uniform power combining technique. This chip demonstrates an improved PA efficiency at power backoff by reducing the impedance difference in a conventional load modulation approach. The design and measurement results of the prototype chip are described in detail.

Chapter 7: A full-duplex transceiver front-end with three cancellation paths is introduced to mitigate the transmitter self-interference. The three cancelling circuits include an electrical balanced duplexer (EBD) and two RF feedforward cancelers. The design and results of this 40nm CMOS prototype chip is given in this chapter.

Chapter 8: This chapter gives a summary of the dissertation and lays out future directions for research on mm-Wave and full-duplex radio designs. This discussion comments on the application of the proposed circuit techniques and possible improvements to the implemented systems.

Chapter 2. MILLIMETER-WAVE RADIOS AND 5G SYSTEMS

5G technology has evolved to address all new applications in the next-generation wireless communication systems. Figure 2.1 depicts some of these applications, including 1) extremely high data-rate communication to enable ultra-high quality video streaming and Virtual Reality (VR) / Augmented Reality (AR) applications, 2) massive connectivity to bring the massively increased radio components for Internet of Things (IoT) and Smart Home to people's daily lives, 3) and low latency / high reliability such as car radar and industrial automation applications. All aforementioned applications require new technologies to realize these aspects. More specifically, new communication protocols and new spectrum opportunities are required to achieve low-latency and high data-rate communications.

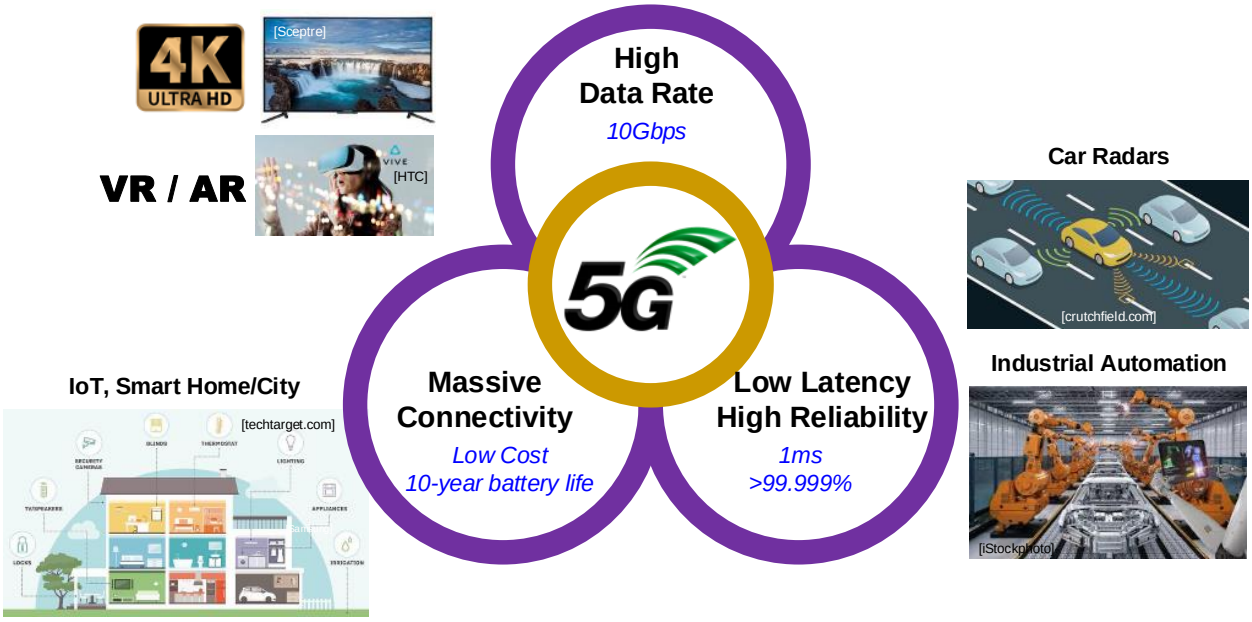


Figure 2.1. New applications in 5th-generation communications.

Mm-Wave bands offer new spectrum opportunities with ultra-wide bandwidth which allows massive and high data-rate communications. There are several design challenges associated with circuit design at mm-Wave frequencies.

2.1 Aspects of mm-Wave Circuit Designs

There are several aspects to the future radio systems at mm-Wave frequency. Figure 2.2 shows the band allocation for 5G systems. As shown in the figure, the mm-Wave bands provide significantly wider BW from 28 to 90GHz to allow ultra-high data-rate communications as compared with conventional RF bands below 6GHz (sub-6GHz). Moreover, wider bandwidth indicates more radio systems can be accommodated thereby making massive connectivity possible. To cover all mm-Wave bands, wide BW front-end modules (FEM) are desired to allow multi-band operation and reduce hardware complexity. In this example, instead of having 4 dedicated front-ends, only two ultra-wide BW FEMs can be used to cover all the 5G mm-Wave frequency bands, for example, one FEM covers the bands of 28GHz and 39GHz and the other FEM covers the bands from 60GHz to 90GHz.

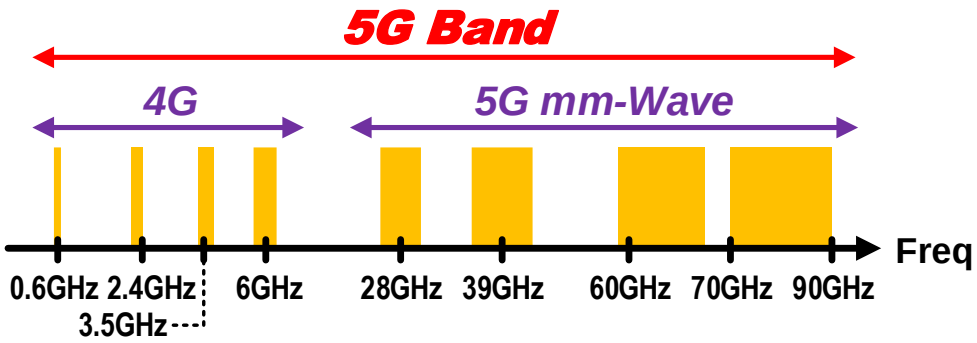


Figure 2.2. Band allocation of the 5G system.

Secondly, the radios operating at higher frequency allows a smaller silicon size and the antenna aperture size. To understand this, Doherty PA is a good example since it requires a λ/4 impedance rotation for the output combiner where the λ/4 is inverse proportional to the carrier frequency. Figure 2.3 shows three Doherty PAs operating at 2.4GHz, 35GHz, and 82GHz. The physical size of these implementations is significantly scaled-down when the carrier frequency moves up to a higher frequency.

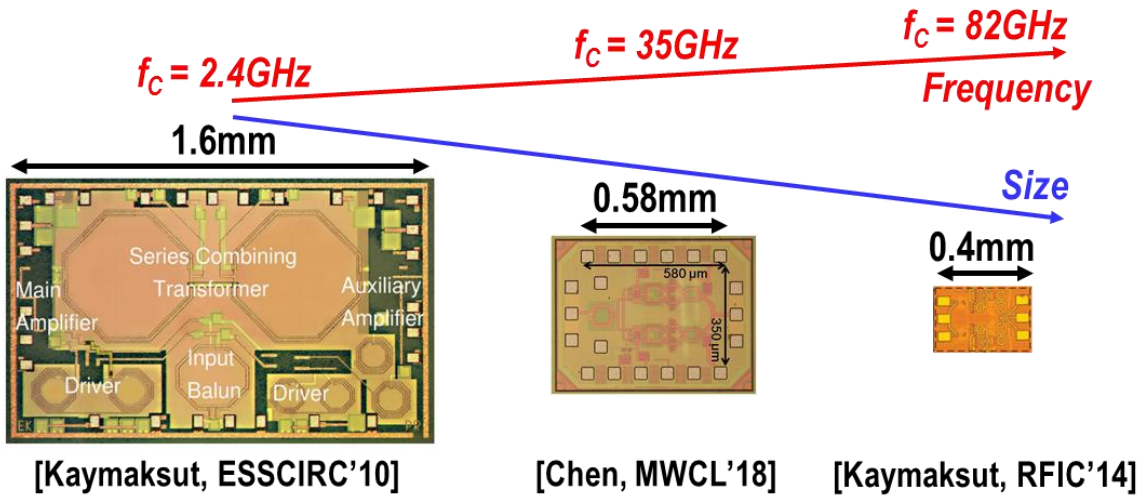


Figure 2.3. Doherty PAs at different carrier frequencies.

One drawback of moving to a higher carrier frequency relates to more path loss will be experienced thereby reducing the transmission range. Figure 2.4 shows the atmospheric attenuation with different radio frequencies [3]. We can see as the carrier frequency moving to a higher frequency, more attenuation will be expected. Fortunately, mm-Wave radios are usually implemented with phased arrays to provide long-range and directional transmissions which produce less spatial interference that relaxes the linearity requirement for receiver designs, see Figure 2.5 (a). In contrast, though the path loss of traditional sub-6GHz systems is low which are ideal for long-range communication, they adapt omni-directional antennas which introduce massive interferences to nearby radios, see Figure 2.5 (b).

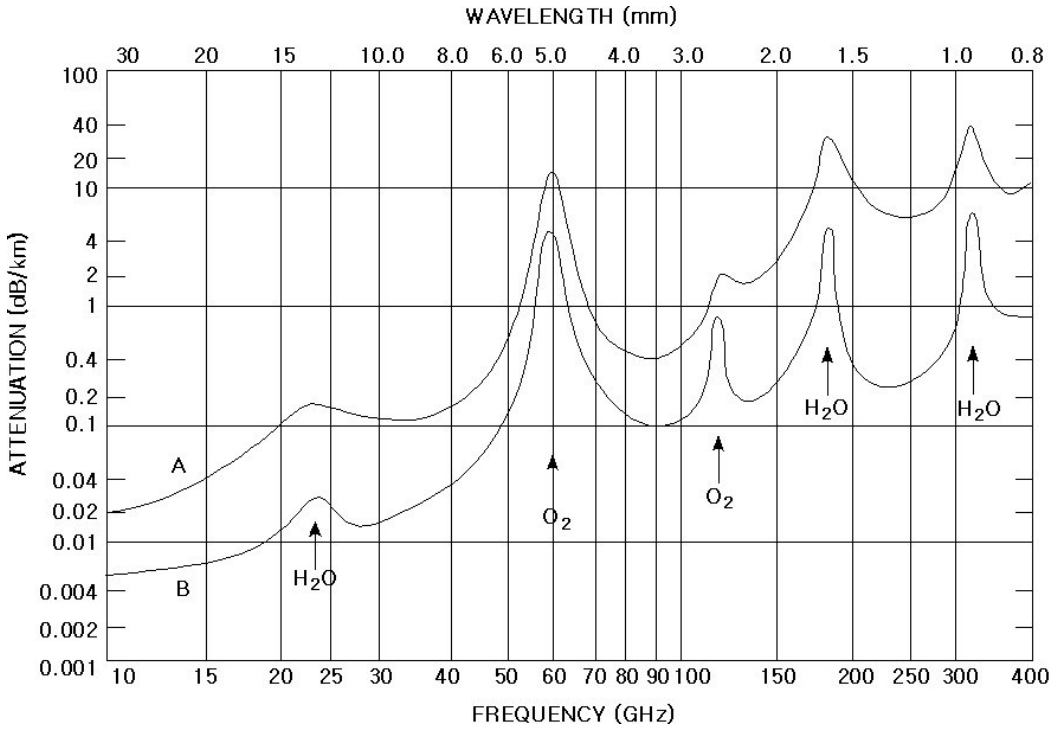


Figure 2.4. Atmospheric attenuation [3]

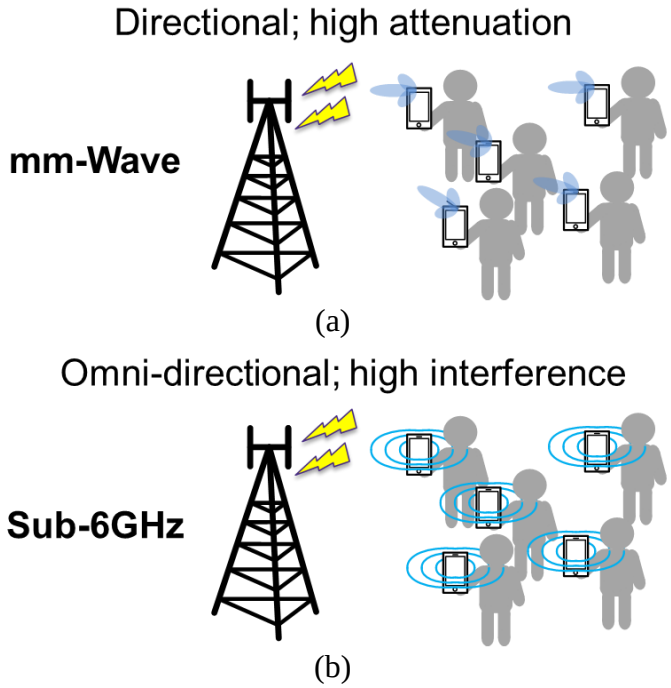


Figure 2.5. Data radiation for different systems. (a) Direction antenna phased-arrays for mm-Wave systems. (b) Omni-directional antennas for conventional, sub-6GHz systems.

2.2 Carrier Frequency and Power Efficiency

In CMOS mm-Wave circuit design, one key challenge associated with mm-Wave receiver relates to producing sufficient gain with low power consumption. To understand the relationship between gain and frequency. Let's consider a generic direct-conversion receiver, as shown in Figure 2.6.

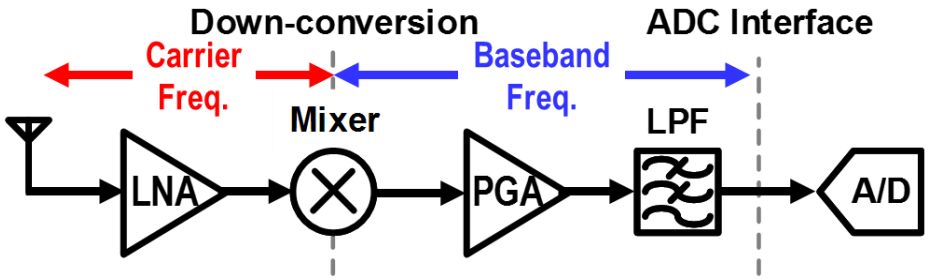


Figure 2.6. A typical direct-conversion receiver.

In a conventional heterodyne receiver, there are multiple opportunities along the receiver chain to apply gain. The emphasis is on applying gain with low noise earlier in the chain. Thus, with gain, the noise performance of the later stages in the receiver can be relaxed. However, applying gain at the carrier frequency is relatively power inefficient, as compared to the baseband frequency, particularly when the front-end operates at mm-Wave frequencies. This is illustrated by showing a G_{max} simulation for an NMOS common-source (CS) amplifier as shown in Figure 2.7. Figure 2.8 show the G_{max} simulation of a10-um-wide NMOS amplifier in TSMC 28nm CMOS technology with a current density of 125μA/μm. As shown in Figure 2.8, the G_{max} decreases when the carrier moves up to a higher frequency. More specifically, we compare the maximal stable gain (MSG) at two frequencies where the NMOS device can provide 36dB gain at 200MHz but only 10.5dB at 60GHz. As a result, if a total receiver gain of 30dB is required, implementing the gain purely at 60GHz consumes 3 times more power consumption as compared to the gain purely implemented at 200MHz. As a result, implementing gain at mm-Wave is power-inefficient.

In contrast, mixer-first receivers implement signal amplification at baseband that is more power-efficient. This type of RX front-end becomes more popular in mm-Wave designs for a number of reasons: 1) It is more power-efficient. 2) The mm-Wave radio systems usually adapt phased-arrays where the signal quality can be enhanced by the array gain. Therefore, the noise performance of each FE element is more forgiving. 3) Mixer-first RXs exhibit high linearity, wide bandwidth, and a compact size.

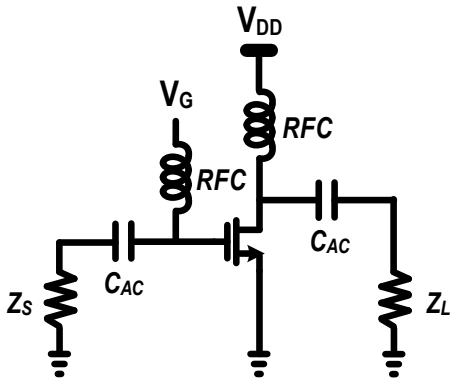


Figure 2.7. Schematic for running a G_{max} simulation of a common-source NMOS amplifier.

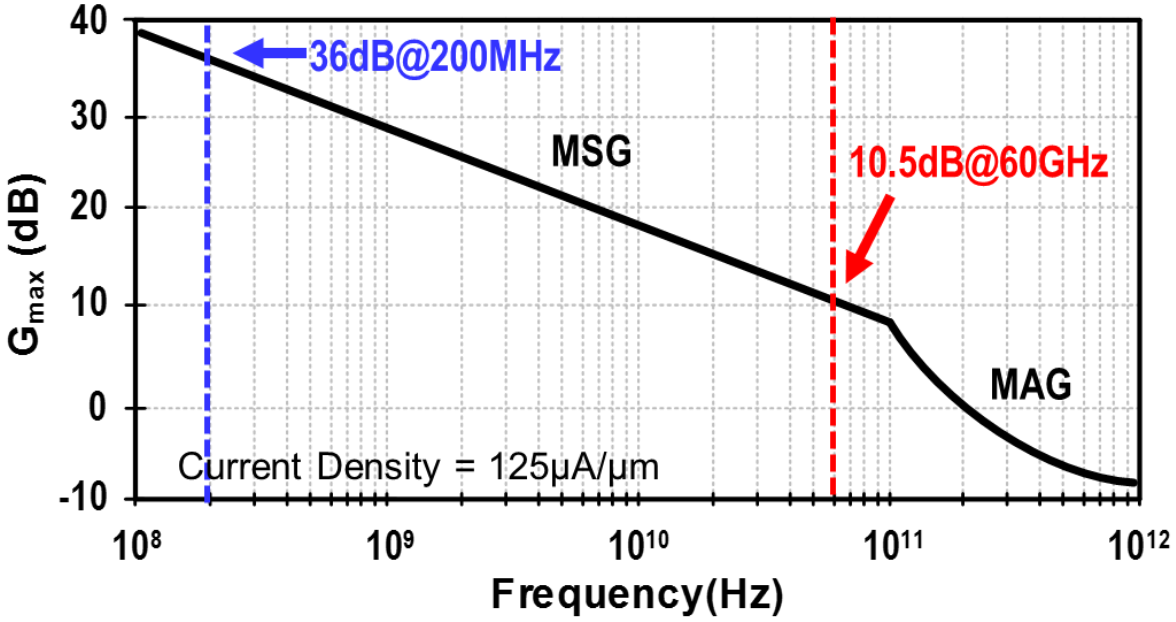


Figure 2.8. G_{max} simulation result for the 10-um-wide common-source NMOS amplifier in TSMC 28nm CMOS technology with a current density of 125μA/μm.

2.3 PHASED-ARRAYED RECEIVERS

There are several types of phased-array receiver and beamformers (BFs). They are identified by where the phase-shifting and beamforming are performed. The types of the BFs will be described in the next few sections.

2.3.1 *RF Beamforming*

The RF beamformer is the most intuitive implementation, see Figure 2.9 (a). The phase shifters and the beamformer (signal combiner) are at the carrier frequency right after LNAs [4]. RF BFs have a few advantages such as: 1) TX and RX can share the same set of phase shifters, 2) wide bandwidth. However, the implementations of RF phase shifters usually require large passive components (inductors and capacitors) which not only introduce loss but also occupy a large silicon size. The major drawback of RF BF relates to the high-loss phase shifters being introduced early in the chain, thereby degrading the noise figure.

2.3.2 *LO Beamforming*

The LO beamformer relaxes the noise burden of RF BFs since the phase shifters are not in the signal path [2], as shown in Figure 2.9 (b). However, the increased system complexity due to the requirement for more down-conversion mixers makes LO BFs less attractive.

2.3.3 *Baseband Beamforming*

The BB BF shown in Figure 2.9 (c) enables compact-size implementations as compared to the RF BF counter-part [5]. The Cartesian phase rotator is one popular implementation for BB BF. However, the receiver adapting BB BF requires high linearity because of the lack of the spatial rejection at the carrier frequency.

2.3.4 *Digital Beamforming*

Digital BF provides the maximum flexibility for generating directional beams [6], see Figure 2.9 (d). The analog BFs mentioned in Section 2.3.1, 2.3.2, and 2.3.3 usually can provide only one directional beam since they can only drive one set of phase shifters limited by the loading. In contrast, the Digital BF can generate multiple beams simultaneously since it is possible to duplicate more digital phase shifters.

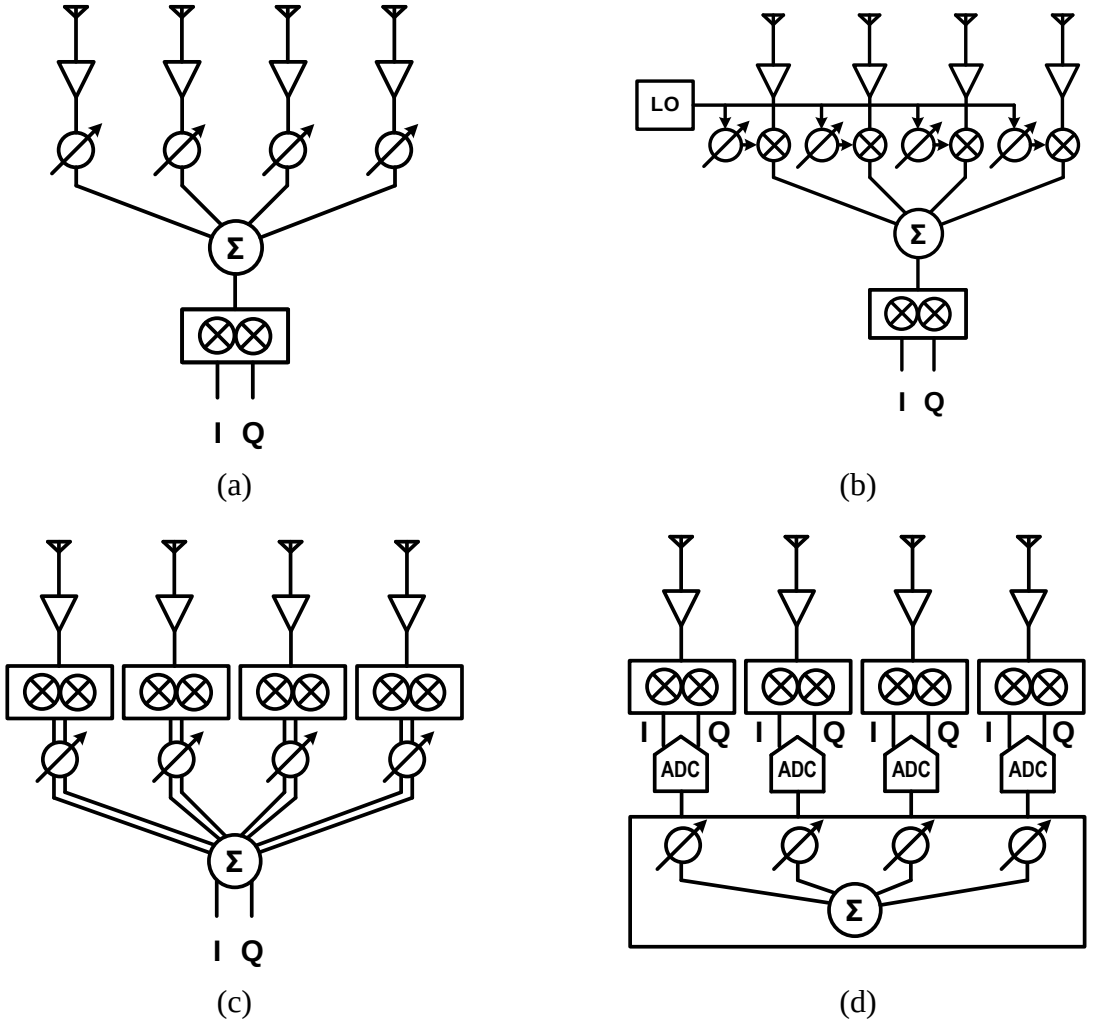


Figure 2.9. Types of phased-array receiver and beamformer (BF): (a) RF BF, (b) LO BF, (c) Baseband BF, (d) and Digital BF.

2.4 Proposed Highly-Digitized Phased-Array Front-Ends for Next-Generation Radios

The focus of the next-generation radio systems will be to increase data rates by exploring new spectrum in the higher frequency mm-Wave bands. The ability to support a massive number of users, in addition to lowering the power, and cost of the transceiver hardware. Mm-Wave bands appear to be an obvious solution to achieve higher data rates and massive accessibility given by the available bandwidth of several gigahertz. However, the CMOS transistors are not power-efficient running at mm-Wave frequencies, as mentioned in Section 2.2. Moreover, high-speed data converters are also power-consuming. Furthermore, mm-Wave circuits are sensitive to parasitic capacitance and require massive passive/inductive components to resonate out parasitic in order to obtain sufficient gain. Having massive passive components results in large silicon size thereby increasing the cost.

Figure 2.10 proposes a new architecture for ultra-wideband, highly-digitized phased-array receivers for backhaul communications and next-generation radios using a novel elemental digital beamforming approach. A key innovation of the proposed architecture is to digitize the input signal as close to the antenna as possible, using low-resolution ADCs. Therefore, the mm-Wave front-end circuitry is significantly reduced. Moreover, instead of narrowband phase shifters, broadband true time delay blocks are implemented in the digital domain [7]. As a result, the number of beams can be easily achieved by duplicating the number of digital front-ends in parallel, and combined in the digital phased array summation block.

The analog front-end of the proposed receiver is significantly reduced to achieve low power and compact silicon area. To recover the performance deficiency in the analog front-end, the highly intensive digital back-end will provide RF calibrations. Given by recent development in Machine

Learning, one possible approach is to apply these high-level algorithms to solve traditional RF impairments, such as gain error, linearity, mismatch, PVT variation, interferences, blocking conditions, and so on to simplify the analog front-end designs.

This dissertation intends to address some of the issues by developing circuit techniques as well as system-level understanding. A mixer-first receiver for low power and compact size, a system-level study of low-resolution ADC, and a first prototype phased-array receiver employing low-resolution ADC with digital beamforming, have been explored, and are discussed in subsequent chapters.

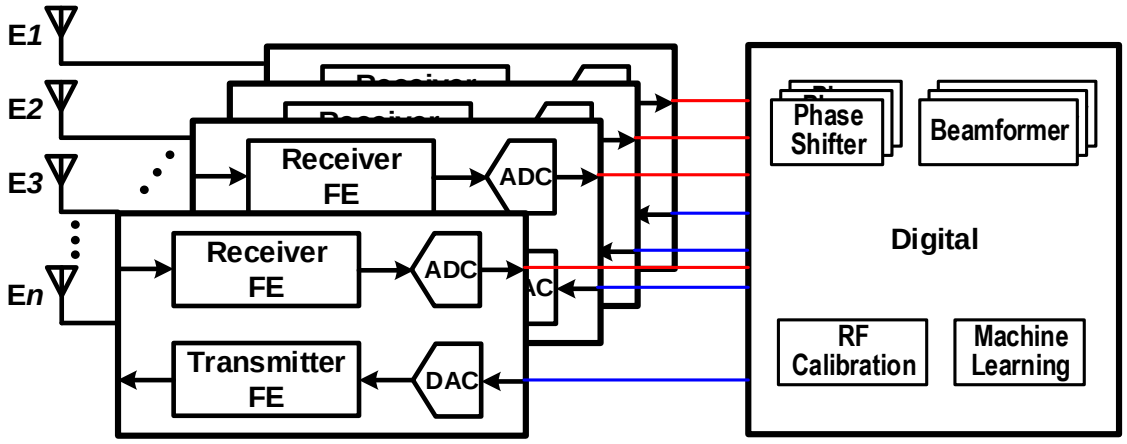


Figure 2.10. Proposed highly-digitized phased-array front-end with digital multi-beamforming.

Chapter 3. V-BAND PSEUDO-MIXER-FIRST 2X2 PHASED-ARRAYED RECEIVER

This chapter describes a V-band 2x2 phased-array receiver (RX) for 5G radios and radar systems [8]. The pseudo-mixer-first RX utilizes a G_m-assisted matching network (MN) to reduce the noise figure of conventional passive mixer-first RX front-ends. The MN consists of an inverting transformer in parallel with a G_m amplifier to place an extra gain of ~5dB prior to the down-conversion mixers, thus improving the noise figure with minimal additional components. This prototype 2x2 phased-array RX front-end integrates a proposed G_m-assisted MN, mixer-first RX with translational feedback, Cartesian phase shifters as a baseband beamformer, poly-phase filters, and LO generation in TSMC 9L 28nm CMOS, occupying a total area of 0.53mm^2. This work achieves a cascaded RX noise figure of 7dB, conversion gain of 26dB, input referred 1-dB compression point of -20dBm with an input return loss lower than -10dB over 22-GHz bandwidth. The current consumption is 28.5mA for one RX element (RX core: 15.5mA excluding output buffer) from a 0.95-V supply.

3.1 INTRODUCTION

The pervasive nature of future 5th Generation (5G) wireless systems has motivated research and development efforts towards low-cost, ultra-broad bandwidth, low power wireless communication systems which exploit the spectral availability offered by millimeter-wave (mm-Wave) frequencies. Although highly-integrated CMOS mm-Wave phased-array solutions hold potential to address traditional consumer concerns with respect to cost and silicon size, the lack of power gain at high frequency creates a challenge for low-power solutions. Specifically, a key

challenge associated with mm-Wave CMOS RX front-ends (FE) relates to the power inefficiency of producing gain at the carrier frequency. Assuming a fixed amount of required gain between the antenna and baseband to leverage the full range of analog-to-digital converters (ADC), several points along the RX chain may be used for signal amplification.

Figure 3.1 shows a direct-conversion architecture, as is widely implemented in radio transceivers. As seen in the figure, the amplification can be done prior to the down-conversion mixers at the carrier frequency, or at baseband after down-conversion. An LNA is most commonly used for signal amplification prior to the down-conversion mixers at carrier frequencies to improve the RX noise performance [5], [9], [10], see Figure 3.1. However, in the mm-Wave bands (above ~20GHz), the gain at the carrier frequency, prior to the down-conversion mixers, becomes extremely power-inefficient due to the loss in CMOS device gain. As mentioned in Chapter 2, the G_{max} of a 10-um-wide NMOS transistor in 28nm technology with a current density of 125μA/μm, is only 10.5dB at 60GHz. By comparison, the same transistor with identical bias current achieves ~24dB of gain for RX carrier frequencies below 6GHz, see Figure 2.8. Thus, implementing gain at mm-Wave frequencies is a relatively unattractive choice in terms of power efficiency.

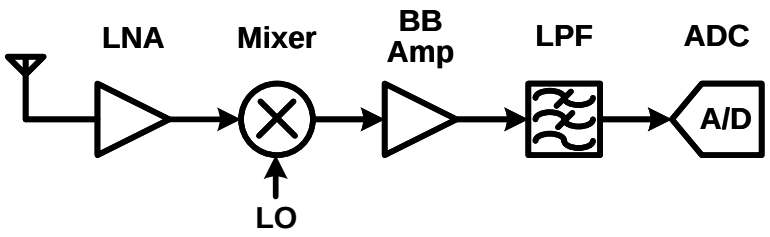


Figure 3.1 Typical amplification-and-downconversion RX

For example, Figure 3.2 shows the block-level diagram of a state of the art mm-Wave receiver described in [11]. This receiver achieves 20-dB gain and 7.8-dB noise figure over 20-GHz RF bandwidth. In [11], every node at mm-Wave frequencies has a transformer used to perform inter-stage matching as well as provide inductive loads to resonate out the parasitic capacitance, as

shown in Figure 3.2. This receiver requires a total of 7 transformers to provide enough gain and bandwidth which occupies a big portion of the silicon area (see Figure 3.3 for the die photo). Also, the receiver consumes a significant amount of power (115mW).

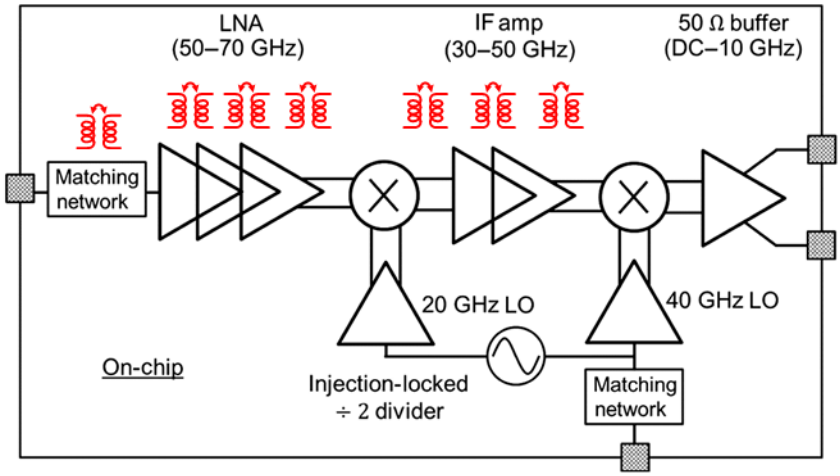


Figure 3.2 The block diagram of LNA-MIX (amplification and down-conversion) receiver example described in [11]

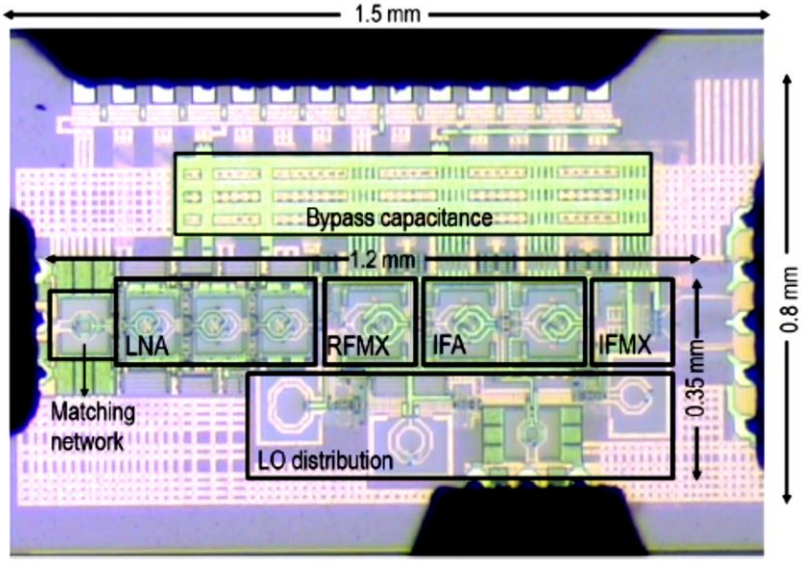


Figure 3.3 Die photo of the receiver described in [11]. There are 7 transformers along the signal path which occupy most of the silicon area.

In contrast, mixer-first RX FEs were introduced to achieve gain prior to the ADC using a

more power efficient approach by placing the burden of gain at baseband [12], [13], see Figure 3.4. Moreover, passive mixer-first RXs have shown promise particularly for the applications that demand high linearity, such as 5G and radar systems, as well as with a compact size, see Figure 3.5. For example, baseband Cartesian phase shifters and digital beamforming architectures enable opportunities for compact-size phased-arrays in 5G radios [5] but require highly linear front-ends due to the absence of spatial selectivity in the RF front-ends. Although recent passive mixer-first RXs have shown promise towards achieving high linearity, wide bandwidth, and compact silicon area, this class of front-end topology suffers from relatively poor noise figure (NF) performance due to the lack of gain at the RX input [4][5]. This project describes a CMOS pseudo-mixer-first (PMF) phased-array RX which exploits the already existing MN to provide a modest amount of gain prior to the mixer, to improve NF performance for a passive mixer-first RX FE in the mm-Wave bands above 50GHz.

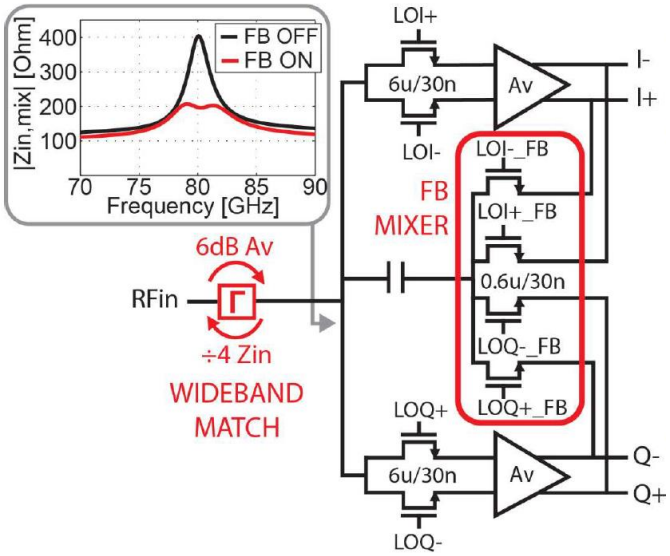


Figure 3.4 The block diagram of the mixer-first receiver described in [12].

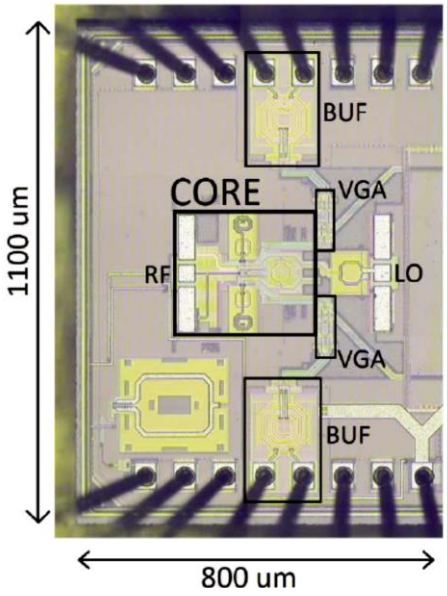


Figure 3.5 The die photo of the mixer-first receiver described in [12].

3.2 Pseudo-Mixer-First Rx and Gm Assisted Matching Network

Matching networks serve multiple purposes including impedance matching and single-to-differential signal conversion. Thus, MNs are necessary, independent of the RX architectural choice. Figure 3.6 (a) shows a single-element block diagram of a 2x2 phased-array PMF RX with the proposed G_m-assisted MN. Similar to [12], this RX includes a translational feedback loop to significantly reduce the power consumption of the LO driver by using smaller dimension switches, while maintaining a low mixer input impedance. However, in contrast to [12], this PMF RX utilizes the on-chip MN not only to preserve the advantages of wideband input match of a passive mixer-first as was done in [12], but also functions as an amplifier when combined with a G_m stage to deliver a modest amount of gain prior to the noisy down-conversion mixers. It is important to note that this proposed RX is not an active mixer-first RX, as the G_m stage is in parallel to a matching network, nor an LNA+mixer topology (will be described next), hence it is referred to here as a pseudo-mixer-first receiver.

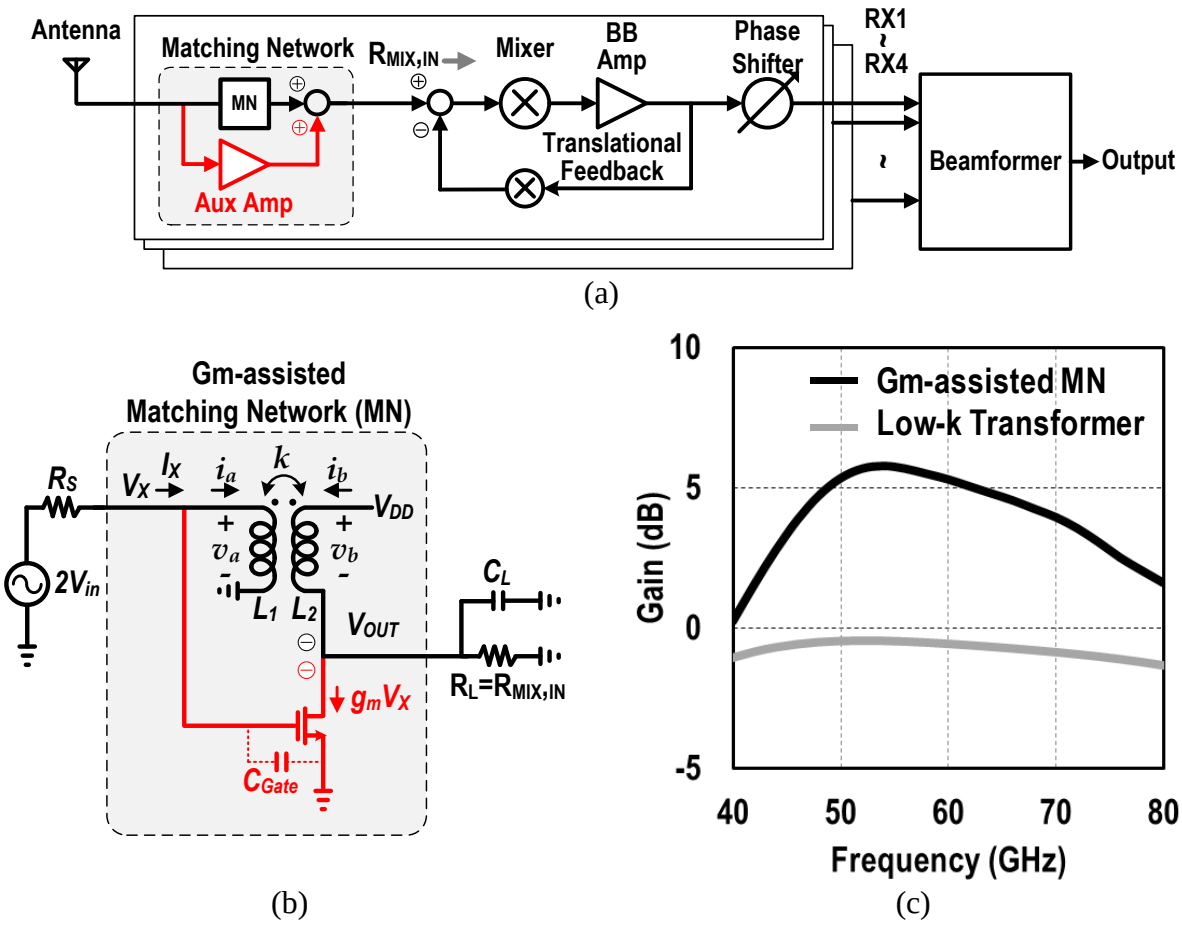
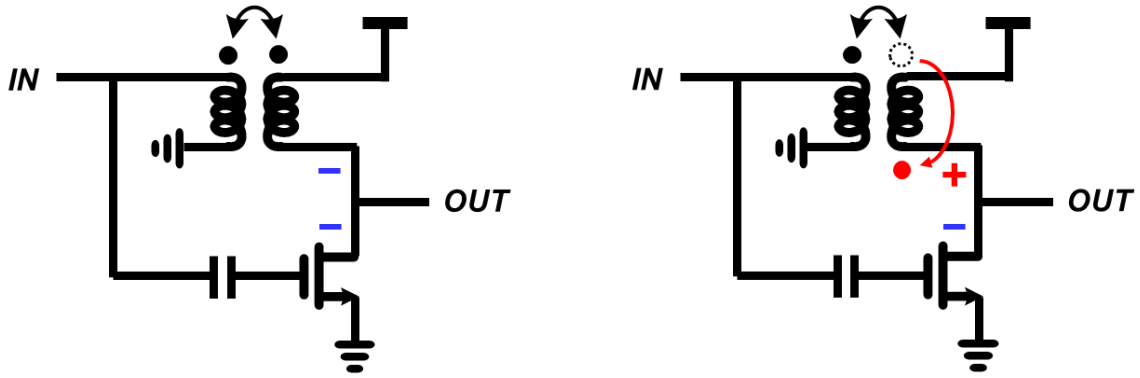


Figure 3.6 (a) The proposed 2x2 pseudo-mixer-first RX with Gm-assisted matching networks. (b) the detailed circuit diagram of the Gm-assisted matching network. (c) Comparison between Gm-assisted matching network and conventional low-k transformers, simulated gains from the antenna to the mixer input.

The G_m-assisted MN uses an auxiliary G_m amplifier inserted in parallel with a transformer-based MN to provide active gain from the antenna port to the mixer input, as shown in Figure 3.6 (a). With the auxiliary amplifier, both gain and noise performance of the RX can be improved. The MN is implemented with an inverting transformer, as the same polarity is required for these two parallel paths, see Figure 3.6 (b). Although the G_m-assisted MN (see Figure 3.7a) resembles a drain-to-gate transformer-based feedback amplifier (see Figure 3.7b) introduced in [6][7], there are subtle, yet significant differences between the two topologies which include: 1) the transformer

used in the G_m-assisted MN has the opposite polarity as compared to [14], 2) the G_m-assisted MN has weak amount of positive feedback with a loop gain of less than -10dB, allowing a modest amount of forward gain while the output drives a relatively low-input impedance mixer and maintaining a high-linearity. In contrast, [14] uses negative shunt-shunt feedback and can only achieve gain when loaded with a high-input-impedance mixer. A key advantage of this topology relates to the auxiliary amplifier placed in parallel with the existing MN so both input and output nodes of the auxiliary amplifier can utilize the existing transformer to resonate out the extra parasitic capacitance introduced by the auxiliary amplifier.



(a) (b)

Figure 3.7 The comparison between (a) Gm-assisted matching network and (b) conventional shunt-shunt feedback amplifier.

The design equations of input impedance and gain of the Gm-assisted matching network are shown in Eq. (3.1), (3.2), and (3.3):

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{2}{1 + R_s Y_{IN}} \frac{V_{OUT}}{V_X} \tag{3.1}$$

where,

$$\frac{V_{OUT}}{V_X} = \frac{-\left[\frac{k}{n} + sg_m L_2(1-k^2)\right]}{1 + \frac{sL_2(1-k^2)}{R_{MIX,\,IN}} + s^2 C_L L_2 (1-k^2)} \tag{3.2}$$

$$Y_{IN} = \frac{I_X}{V_X} = sC_{Gate} + \frac{\frac{1}{sL_1} + s\frac{C_L}{n^2} + \frac{1}{n^2 R_{MIX,\,IN}} - g_m \frac{k}{n}}{1 + \frac{sL_2(1-k^2)}{R_{MIX,\,IN}} + s^2 C_L L_2 (1-k^2)} \tag{3.3}$$

In short, the MN serves a dual purpose of providing both matching to the antenna impedance, and as a load to the auxiliary G_m amplifier realized as a gain stage, while occupying a negligible amount of silicon area. Figure 3.6 (c) compares the simulated gains from antenna to mixer input with the G_m-assisted MN and a conventional 4th-order low-k transformer described in [2][3]. The G_m-assisted MN shows a ~5dB increase in gain with an expense of a 7-mA current consumed by the G_m-assisted amplifier. Though a single-stage amplifier at the carrier frequency could achieve similar gain with the same amount of current, the proposed approach needs no additional passive components, therefore the overall solution can be made compact.

3.3 Circuit Implementation

The block diagram of the 2x2 phased-array RX is shown in Figure 3.8. This work employs baseband Cartesian phase shifters to perform current-mode signal combining in the baseband. The down-conversion mixers are driven by 4-phase IQ LOs which are generated locally by poly-phase filters (PPF). A single-ended LO is brought on-chip then converted to a differential signal with a matching transformer, after which delivered to each of the 2x2 arrays through H-tree LO distribution.

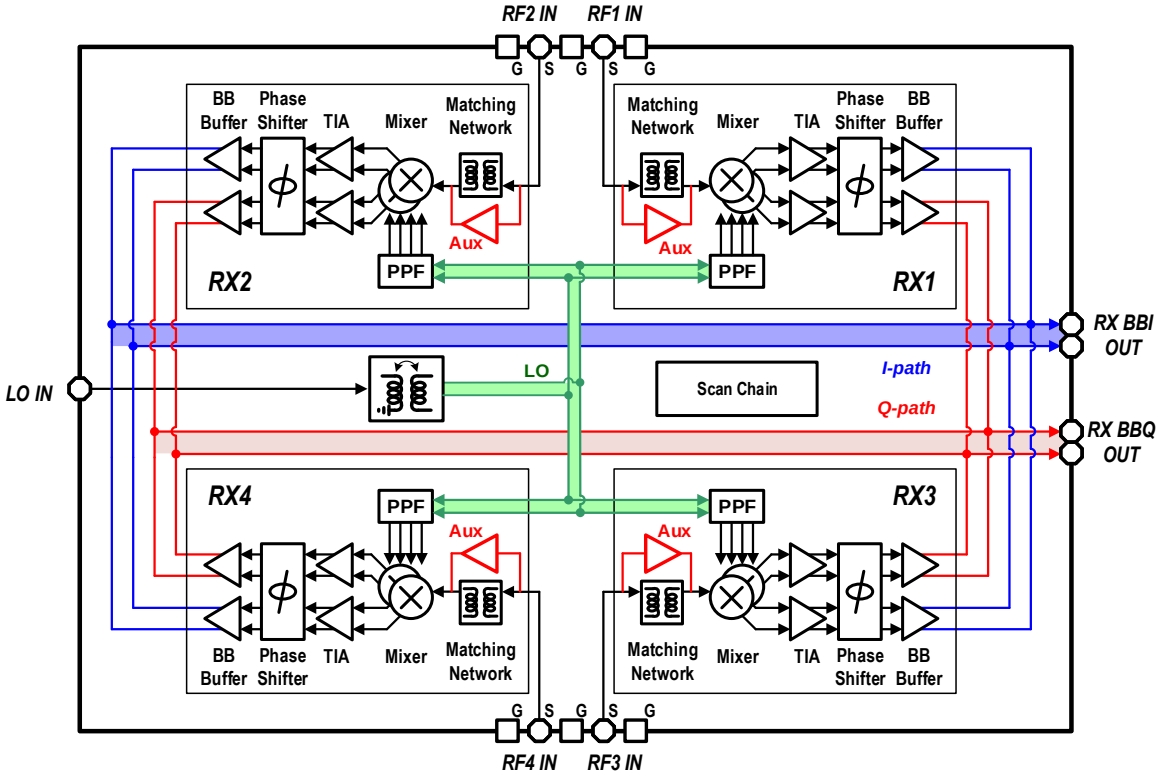


Figure 3.8 Block-level diagram of the V-band 2x2 phased-array PMF RX.

Figure 3.9 depicts a simplified RX signal path schematic of one element in the 2x2 phased array. The RX is composed of a G_m-assisted MN followed by a translational feedback loop formed by mixers and transimpedance amplifiers (TIA), as well as a baseband Cartesian phase shifter. The matching transformer is designed with an *inductance ratio* of 70pH:110pH and a coupling factor of 0.15. The G amplifier is made of a 34-um-wide NMOS transistor which is placed in parallel with the inverting transformer and biased at a current density of 200μA/μm. The translational shunt-shunt feedback is formed by mixer-TIA chain with a mixer switch ratio of 5:1 between the receiving and feedback paths. The Cartesian phase shifter is implemented with variable gain amplifier (VGA) controlled by the gate voltage of the cascode device using a voltage-mode DAC similar to [16], which performs vector current summing to modulate the phase. The phase shifter can also be used to compensate static phase errors created by the H-tree LO distribution and the

2x2 phased-array outputs. Figure 3.10 shows the quadrature LO phase generation. The differential outputs of the transformer are shared with 4 RX elements and fed to a 2-stage poly-phase filter and followed by LO drivers. The LO driver is implemented with capacitance-neutralized differential pairs for an increased G_{max} [17].

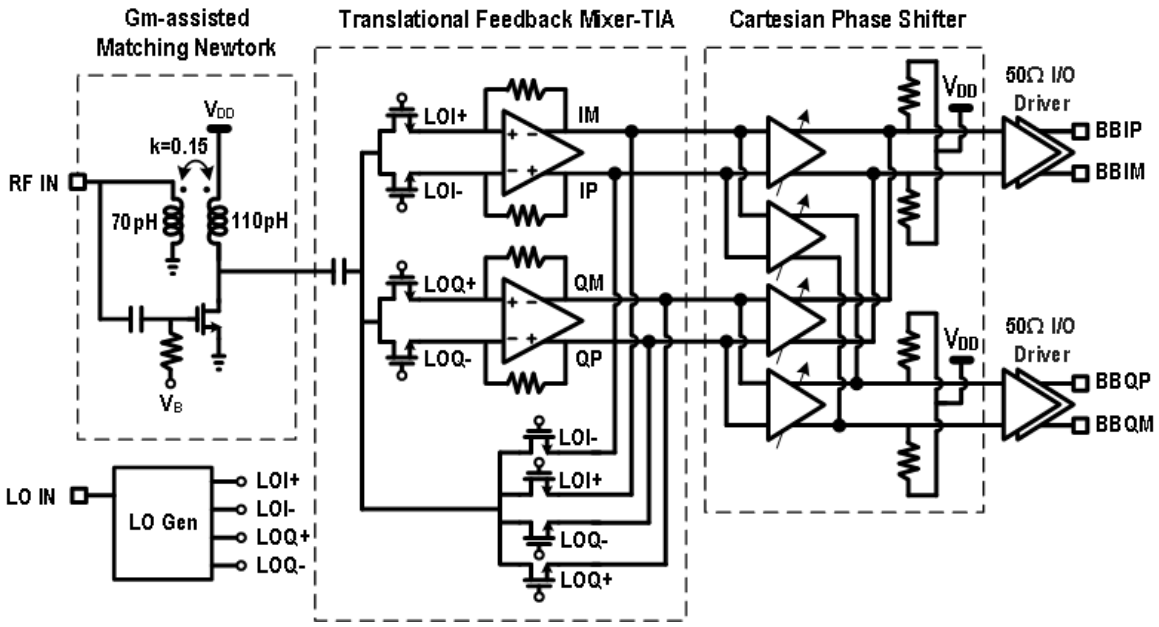


Figure 3.9 Detailed schematic showing the RX signal chain of one phased-array element.

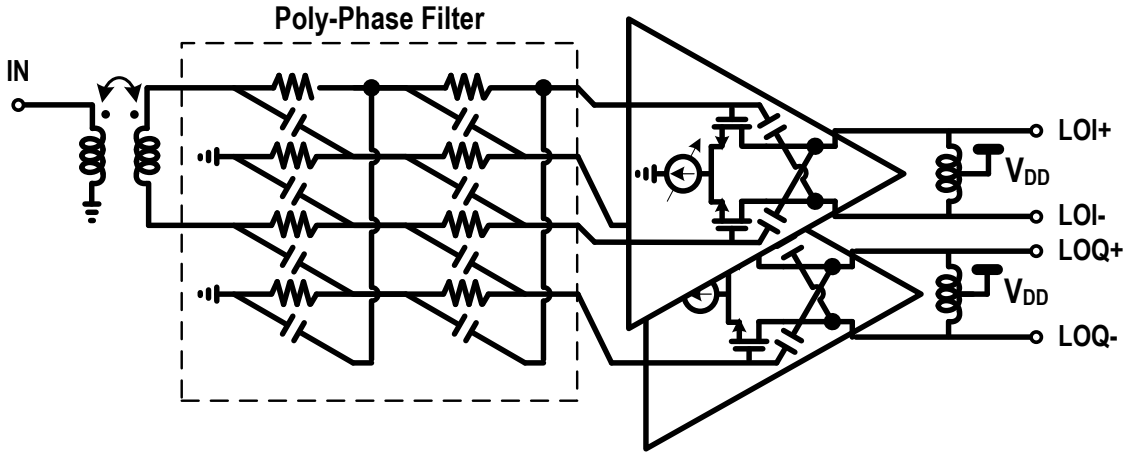
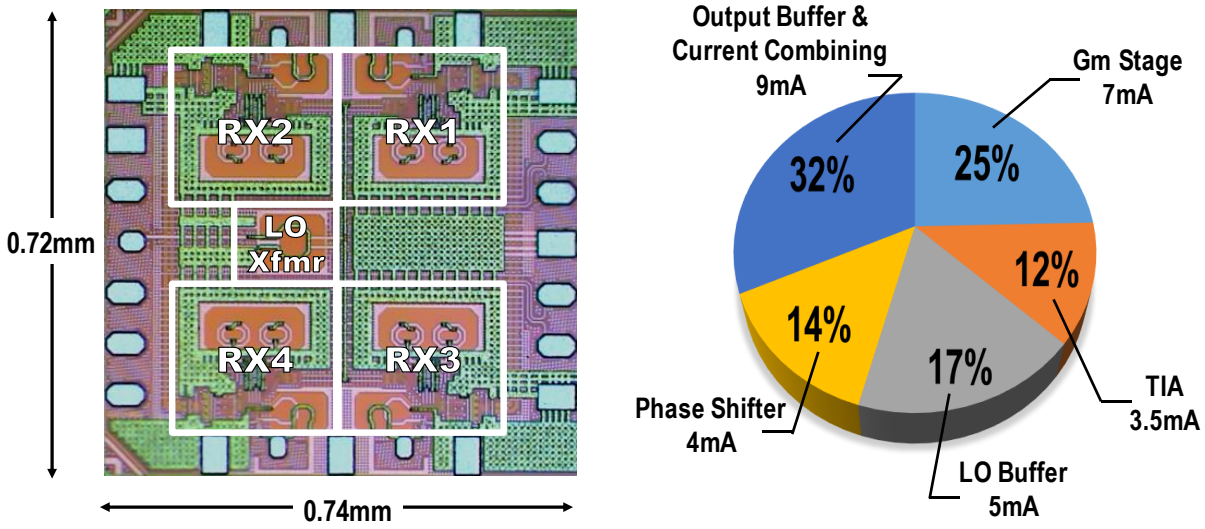


Figure 3.10 Detailed diagram of the local quadrature phase generation of each RX element.

3.4 MEASUREMENT RESULTS

This 2x2 phased-array PMF RX was fabricated in TSMC 9L 28nm HPC+ CMOS process. The die photo is shown in Figure 3.11 (a). The 4-element RX occupies 0.53mm^2 including pads. 4 identical RX elements are on the top and bottom of the die with inputs from North and South. The external LO comes from the left side, passing through the LO matching transformer before distribution to the 2x2 phased array. The differential quadrature baseband outputs exit on the chip's right side, see Figure 3.11 (a). This chip was measured using on-chip probing of all external I/O signals and DC bias. The active die area of one RX element is 0.049mm^2 where the G_m-assisted stage occupies an insignificant area of 0.0004mm^2, including AC-coupling capacitor and bias circuitry. The single RX element consumes a total current of 28.5mA from a 0.95-V supply. Figure 3.11 (b) shows the breakdown of current consumption for a single RX element.



(a) (b)

Figure 3.11 (a) The die photo of V-band 2x2 phased-array RX. (b) The current breakdown of a RX element.

This phased array front-end is measured on a probe station. All signal IO, supply and ground are provided by on-chip probing on the 4 sides of the DUT, see Figure 3.12.

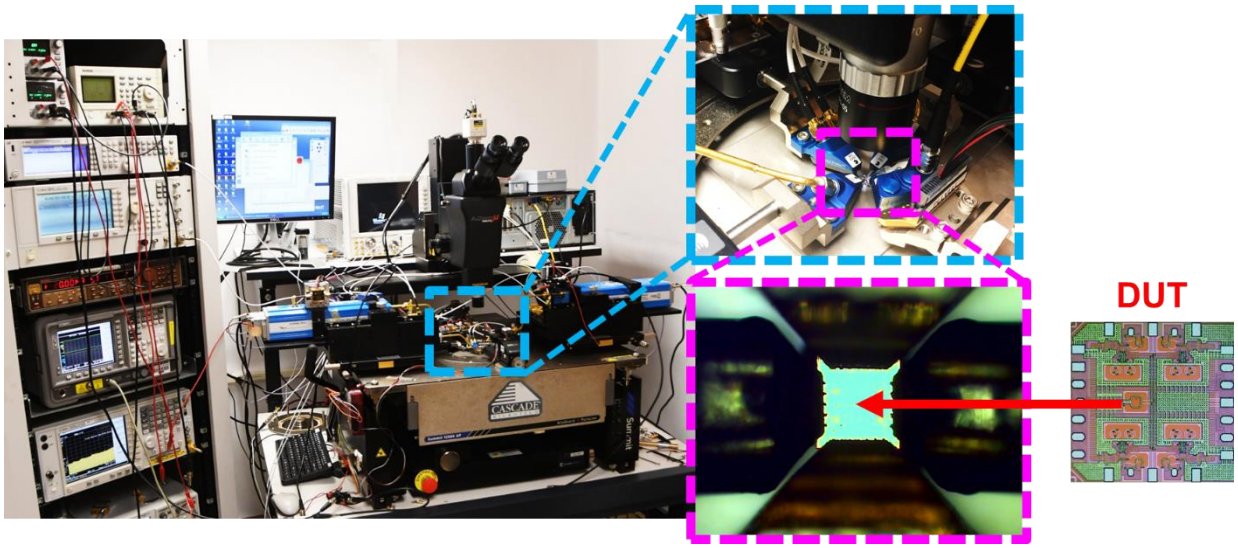


Figure 3.12 Measurement setup for the DUT. All the signal IOs are provided by on-chip probing on the 4 sides of the chip.

3.4.1 *Single Receiver Measurement*

The single-element RX was measured using a standalone structure on the same chip. An Agilent N5247A Network Analyzer (PNA) with OML E-band frequency extension module was used to perform S-parameter measurements. For gain, noise, and linearity measurements, PNA Port 1 was used as input signal where the source power was first calibrated with Agilent N1913A Power Meter, while Port 3 was used as external LO source. The NF was measured using the gain method with a Mini-Circuits Amplifier inserted between the DUT baseband output and Agilent N9010A Spectrum Analyzer to increase measurement accuracy by raising the DUT output noise floor.

The RX achieves a 26-dB measured peak gain, as shown in Figure 3.13 and a 7-dB noise figure, see Figure 3.14. Figure 3.15 shows the with a S_{11} < -10dB from 56GHz to 78GHz for the receiver. The input-referred P1dB is -20dBm, see Figure 3.16. The aforementioned metrics were measured at the RX baseband output with a 20-MHz offset from the carrier frequency. The RX core consumes a total power of 15mW (excluding phase shifters and combining buffers)

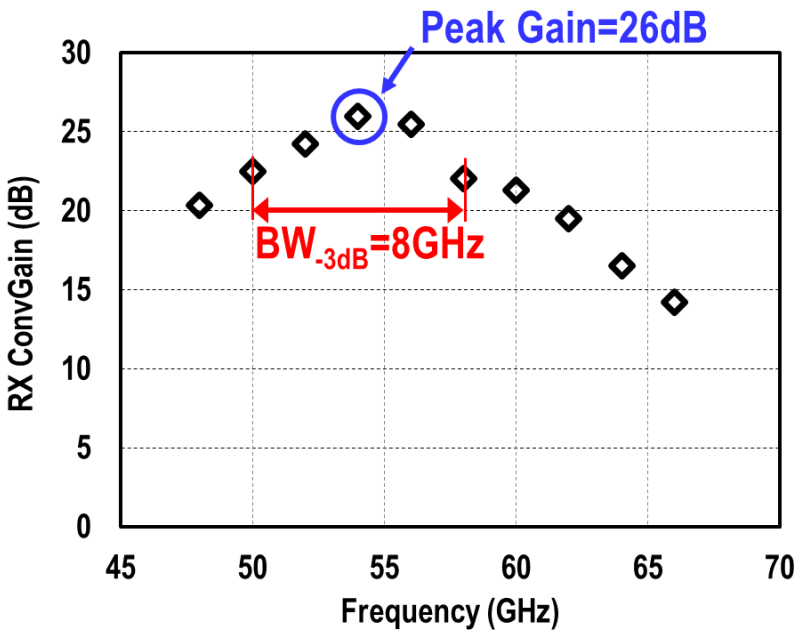


Figure 3.13 Measured S_{21}.

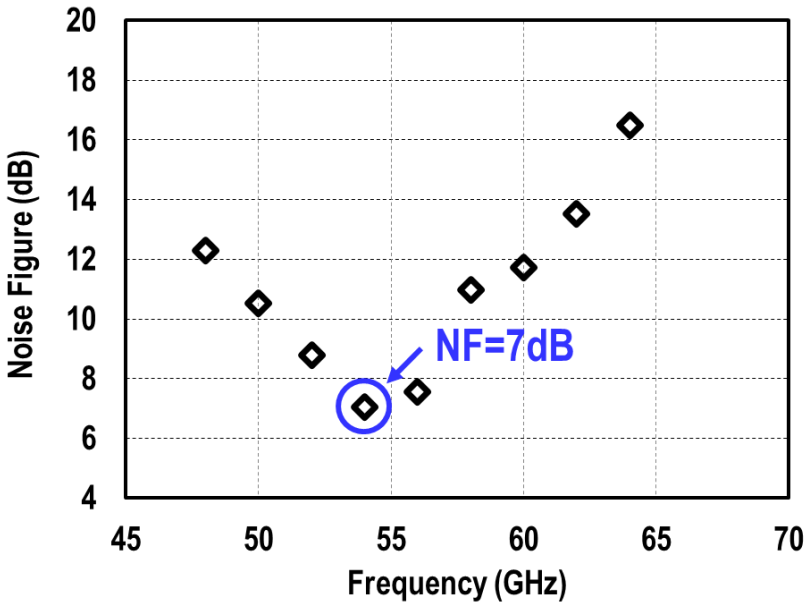


Figure 3.14 Measured RX noise figure.

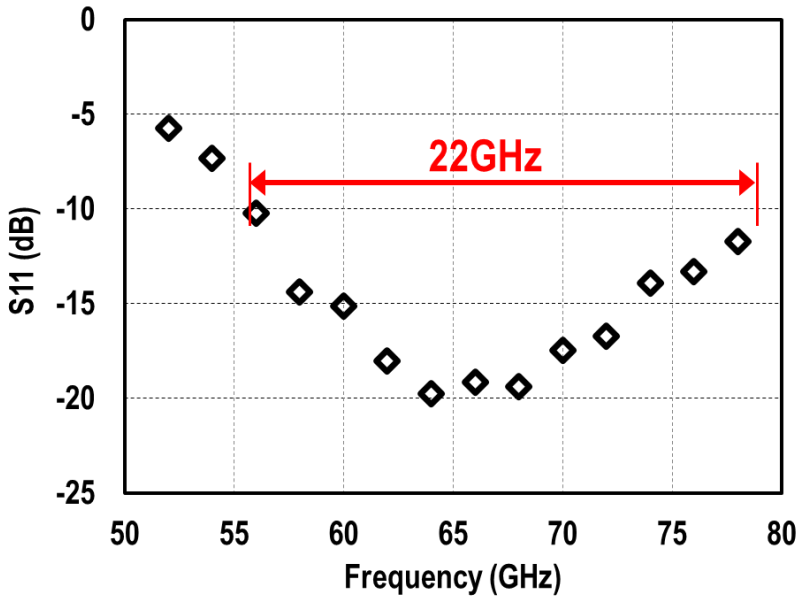


Figure 3.15 Measured input return loss (S_{11}).

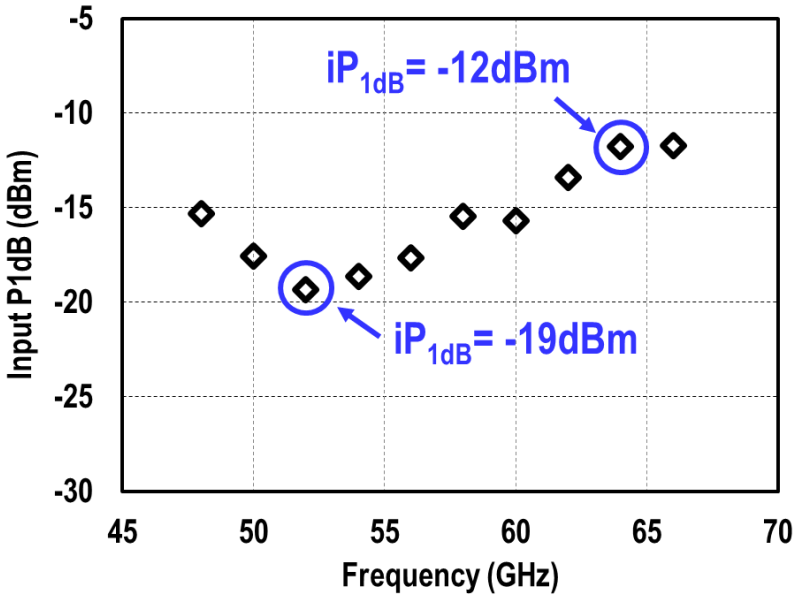


Figure 3.16 Measured RX input P_{1dB}.

3.4.2 *Phased-Array Measurement*

The setup for the 2x2 phased-array measurement is shown in Figure 3.17. A Signatec PXDAC4800 arbitrary waveform generator (AWG) card with 4-ch outputs was used to generate a uniform phase difference between the 4 RX inputs, to emulate different delays associate with

incident angle of an incoming signal. The 4 baseband signals were then up-converted by a SAGE Millimeter E-band Mixers. The mixers were driven by an Agilent E8254A Signal Generator as LO was passed through an external PA (SAGE Millimeter) and a 4-way power divider (Mini-Circuits). Two dual probes (GSGSG) were used to provide the 4 signals for each of the 4 RX inputs from North and South. The RX LO was generated by an Agilent MXG through an active X4 Frequency Multiplier (SAGE Millimeter). Two Signal Generators and the PXDAC4800 AWG card were synchronized by sharing a common 10-MHz reference clock to ensure the frequency alignment (static phase errors) for the whole system. The beam patterns were measured at RX baseband quadrature outputs using Agilent MSO9404A Oscilloscope.

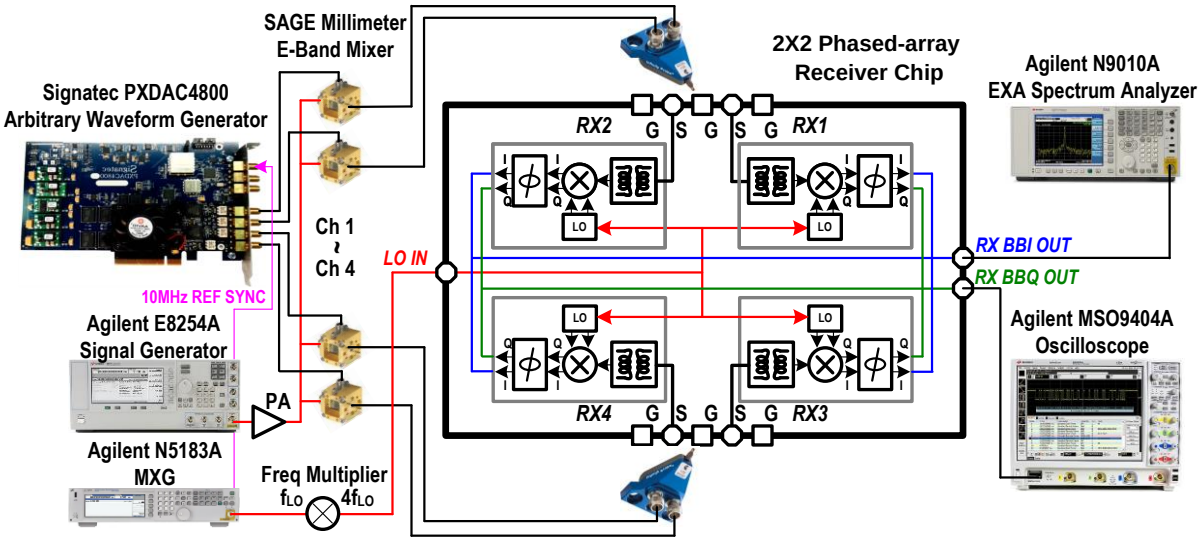
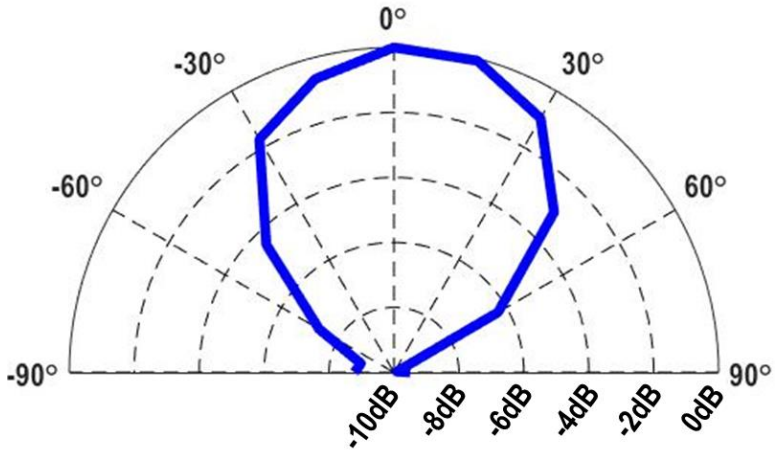
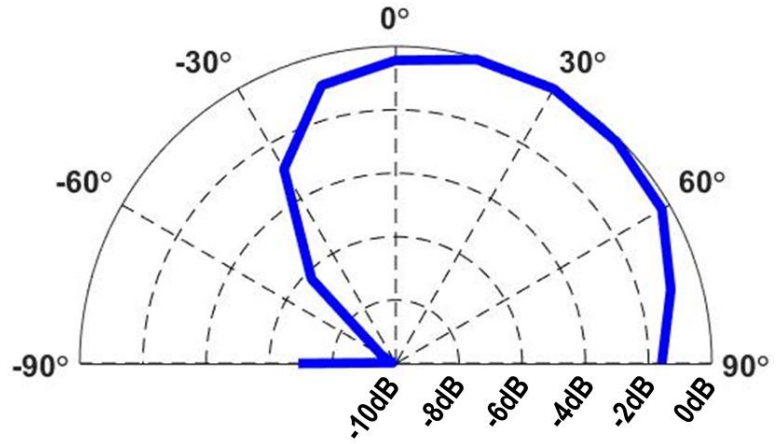


Figure 3.17 Lab bench setup and measurement results of the proposed 2x2 phased-array receiver

To measure the beam pattern, the phase shifters of 4 RXs were first set to a steering angle with the static phase errors among all RX elements being compensated. The 4 input signals were provided conductively by manipulating the phase difference among the 4-ch outputs of the AWG card with different incident angles from -90^{o} to +90^{o}. Figure 3.18 (a) and (b) show two beam patterns with steering angles of 0^{o} and 45^{o}, respectively.



(a)



(b)

Figure 3.18 Measured beam patterns with two steering angles: (a) 0^o and (b) 45^o.

3.5 CONCLUSION

This chapter presented the design and measurement of a V-band 2x2 phased-array RX fabricated in TSMC 28nm process. Table 3.1 summarizes the performance of the RX and compare with prior-art mm-Wave RXs. The measured noise figure of proposed pseudo-mixer-first RX is 1-dB better than prior-art passive mixer-first RXs. In conclusion, this work demonstrates the feasibility for compact, low-power, wide bandwidth, and high-performance mm-Wave radios.

Table 3.1 Comparison to Prior-Art Mm-wave Receivers

		[11]	[5]	[13]	[12]	**This Work**
Technology		28nm	22nm FinFET	65nm	28nm	**28nm**
Topology	**Single RX**	Sliding-IF	Direct Conv.	Direct Conv. Mixer-first	Direct Conv. Mixer-first	**Direct Conv. Pseudo Mixer-first**
	Phased Array	-	BB Beamformer	-	-	**BB Beamformer**
Matching Network		Transformer	Transformer	Low-pass π	Shunt LC + L	**Gm-assisted Transformer**
V_{DD} (V)		0.9	1	1.2	1	**0.95**
Freq. Range (GHz)		61-89[e]	71-76 [e]	49-67[f]	70-100[f]	**56-78[f]**
RF fBW (%)		36.7	6.8	31	35.3	**17.9**
BB BW (GHz)		-	2[b]	0.32	1.8	**1.2[b]**
Single RX Gain (dB)		30.8	36.7	13	25.3	**26**
Single NF (dB)		7.3	6[g]	11	8	**7**
Input P1dB (dBm)		-30.7	-28[d]	-12	-16.8	**-20**
Power (mW)	**Receiver Core**	57	-	14	12	**15[c]**
	Single Element	-	168	-	-	**29**
Active Area Single RX (mm^2)		0.675	0.6[a]	0.39[a]	0.085	**0.049**

[a] Estimated from die photo, without pads. [b] I+jQ bandwidth. [c] The power of buffer driving off-chip is not included. [d] Calculated from reported IP_3. [e] Frequency range based on gain response. [f] Frequency range based on S_{11} response. [g] Including T/R SW loss.

Chapter 4. DIGITAL FRONT-END RECEIVER USING LOW-RESOLUTION ADCS

This chapter explores the opportunity of applying receiver front-end architectures using low-resolution ADCs for ultra-wideband highly-digitized phased-array receivers with low power consumption for backhaul communications. The motivation is to digitize the input signal as close to the antenna as possible, using low-resolution ADCs. Therefore, the radio frequency (RF) front-end circuitry is significantly reduced. We will discuss these challenges starting with an extreme case where 1-bit digitizers (or comparators) are employed to achieve high bandwidth at a low power consumption.

Figure 4.1 shows two receiver architectures including direct-conversion receiver (DCRX) (Figure 4.1a) and direct-sampling receiver (DSRX) (Figure 4.1b). The main difference between these two topologies is the direct-sampling receiver does not utilize a down-conversion mixer to move the carrier frequency down to around DC. Instead, it relies on the sampling event to down-convert the frequency of interest by a certain aliasing copy which will be described next.

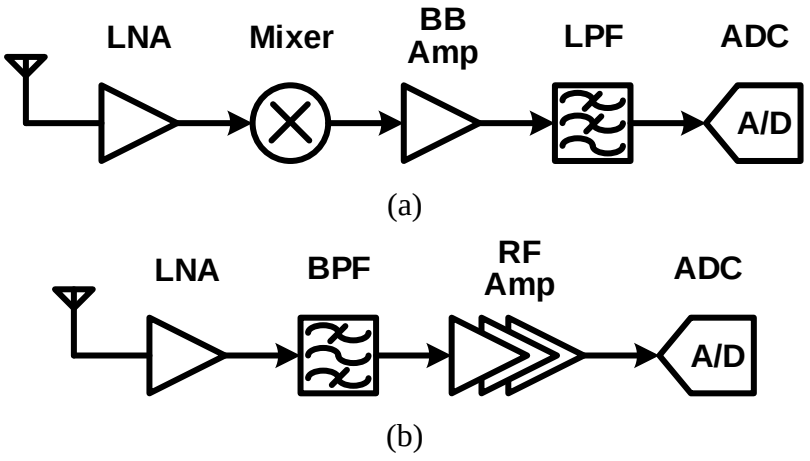


Figure 4.1 Receiver architectures of: (a) Direct-conversion and (b) direct-sampling.

4.1 UNDER-SAMPLING ADCS

In most applications, ADCs are designed to meet the Nyquist sampling theorem [18], that is, the sampling rate must be at least two times larger than the highest frequency of the desired signal, to avoid signal aliasing. The direct-sampling architecture (Figure 4.1b) utilizes the aliasing property of a sampling event in the ADC to effectively down-convert the carrier signal to baseband frequency. As illustrated in Figure 4.2, assuming the wanted signal is centered at 4*Fs, the ADC frequency could be designed as 2 times of 4*Fs, which is 8*Fs, to satisfy the Nyquist theorem. However, in this way, all signals below 4*Fs will be digitized, including the un-wanted signals located at 2*Fs and 3*Fs. As a result, it consumes considerably higher power to drive the extremely high-speed digitizer running at 8*Fs.

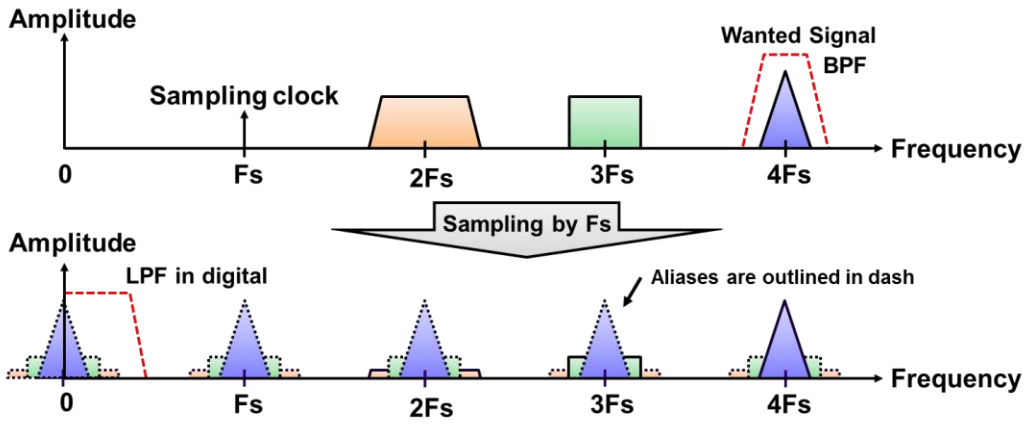
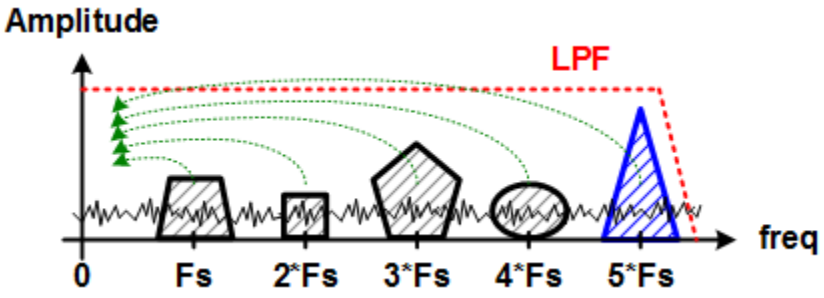


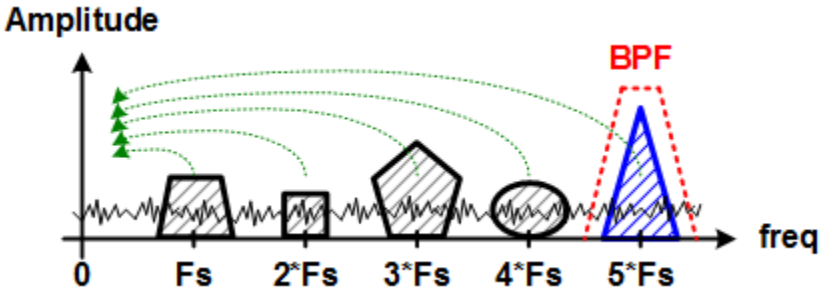
Figure 4.2 The sampling procedure of under-sampling ADCs

One alternative approach is to run an ADC at an under-sampling rate. In Figure 4.2, the ADC sampling clock is set to Fs with a band-pass filter (BPF) centered at the wanted signal frequency (4*Fs). After the sampling procedure, all signals located at an integer multiple of Fs will be duplicated at an integer multiple of Fs [19], while all signals at other frequencies will be attenuated by BPF except for the wanted signal at 4*Fs. The output can be obtained simply by adding a low-pass filter (LPF) in the digital domain. Note that the sampling frequency, Fs, still needs to be two

times larger than the signal bandwidth to meet the Nyquist sampling theorem. As such, the ADC can run at a much lower rate to save power, in this example, only 1/8 of the Nyquist frequency. In addition, the under-sampling ADC works as a down-conversion mixer, so no frequency conversion circuits are needed between the LNA and the ADC.



(a)



(b)

Figure 4.3 Noise folding in under-sampling ADCs with: (a) low-pass anti-aliasing filter; (b) band-pass anti-aliasing filter.

The disadvantage of employing under-sampling ADCs is the noise folding issue, that is, the thermal noise located at an integer multiple of F_S will be folded back into the desired band (see Figure 4.2), degrading the receiver noise performance. This degradation is generally not acceptable for most systems. The mechanism of SNR degradation in under-sampling ADCs is depicted in Figure 4.3 (a), and can be calculated by:

$$SNR\ degradation = 10\log_{10} N \tag{4.1}$$

where N is the number of how many bands are folded into the in-band. In this example, the thermal

noise floor is folded by 6 times (0~5*Fs) and the SNR degradation is 7.78dB. The SNR degradation can be relaxed by using a band-pass filter (Figure 4.3b) instead of the low-pass filter (Figure 4.3a). The MATLAB simulation shows that the SNR degradation can be reduced from 7.89dB to 1.38dB by replacing the LPF with a 2^{nd}-order BPF, assuming the LPF and BPF have similar insertion loss, which makes the noise folding issue less significant.

4.2 Receiver Thermal Noise

Noise is one of the most important metrics in the receiver design. Traditionally, the receiver noise floor, comprised of kTB and noise figure (NF) of the receiver, dominates the overall noise performance. The quantization noise of ADC, on the other hand, is typically designed to be 10 dB lower than the receiver noise floor, contributing only a negligible portion (~0.1dB) to the total noise. Therefore, the quantization noise is usually ignored in most communication systems.

However, it is not the case in a low-resolution receiver. The ADC quantization noise is no longer negligible. Figure 4.4 depicts a link budget analysis of thermal noise for a direct-sampling receiver. Assuming the power available at the transmitter is 40dBm (PA is 30dBm and antenna is 10dBi) with a carrier frequency of 28GHz, the signal received at LNA input is -31dBm after free space transmission over 10 meters (Friis transmission equation). Further, assume the full scale of ADC is 280mV, which is -1dBm, under 1.2V supply voltage. Being the only gain stage in the receiver, the LNA is designed to have a gain of 30dB to provide sufficient amplification. From a noise perspective, on the other hand, the noise power at the LNA input is -81dBm (from kTB, given that the signal bandwidth is 2GHz and the antenna impedance is 50 Ohms). Assuming the cascaded LNA and anti-aliasing filter NF is 10dB. The resulting noise power at ADC input is - 81 + 30 + 10 = - 41dBm.

The quantization noise of an ADC can be obtained by (for sinusoidal inputs):

$$SNR = 1.76 + 6.02N_{bit} \tag{4.2}$$

where N_{bit} is the number of bits of the ADC. The quantization noise of 1-bit ADC can thus be obtained: -1 - 7.8 = -8.8dBm (Figure 4.4). Here we assume the bandpass filter (BPF) in the receiver provides an infinite rejection so no aliasing noise will be added to the receiver thermal noise floor. Based on this analysis, the quantization noise is ~30dB higher than the receiver noise floor. Therefore, the quantization noise dominates the overall noise performance.

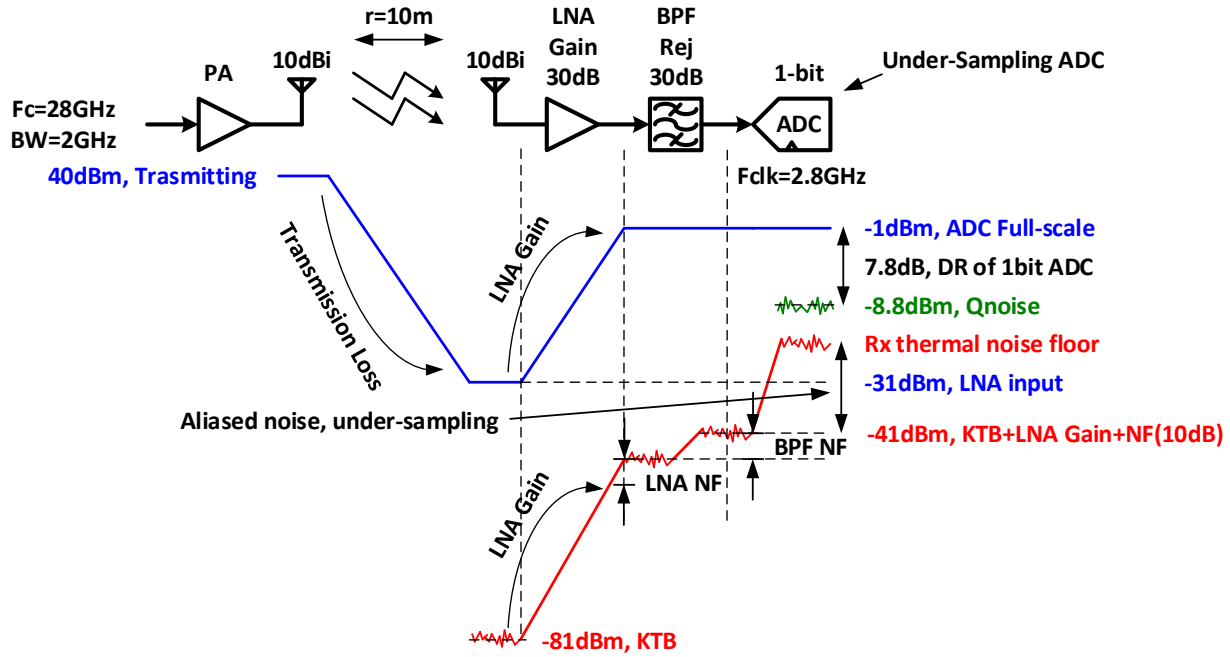


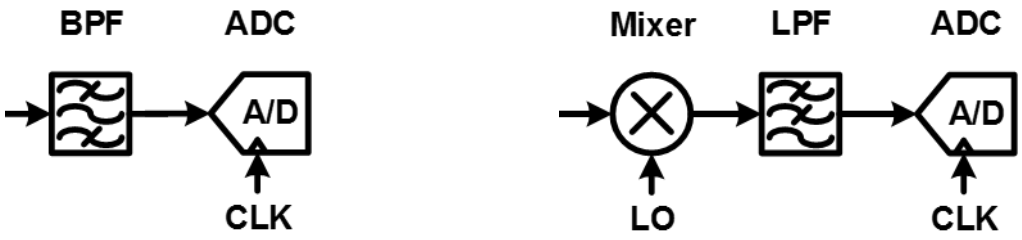
Figure 4.4 Link budget analysis of thermal noise for a direct-sampling receiver.

The analysis above highlights an important concept in designing receivers with low-resolution ADCs. Different from the traditional approach, the NF of receiver building blocks is no longer one of the most important metrics, since the major noise contributor (30dB higher) is the quantization noise of the low-resolution ADC. The purpose of the receiver gain is to provide sufficient amplification to increase the signal strength high enough to meet the full scale of the ADC, and has less concern about suppressing the noise contributed by the following stages.

To mitigate the aliasing noise folded back to the baseband, a direct-conversion receiver can be used which enables the use of high-rejection LPFs as anti-aliasing filters. The addition of a down-conversion mixer introduces phase noise to the receiver noise budget.

4.3 Jitter and Phase Noise in Direct-Conversion and Direct-Sampling Receivers

Figure 4.5 shows a simplified back-end portion of the direct-sampling RX and direct-conversion RX. Both topologies contain an ADC which suffers from clock jitter thereby limiting the upper bound of SNR. The DCRX shown in Figure 4.5 (b), however, is affected by LO phase noise through the down-conversion mixer. [20] provides analyses of SNR, considering clock jitter and phase noise, which can be applied to our discussion here.



(a) (b)

Figure 4.5 The clock jitter and LO phase noise in (a) DSRX (b) DCRX.

The SNR of DSRX can be expressed as [20]:

$$SNR_{DSRX} = \frac{1}{\left(2\pi f_{BW}\sigma_{jitter}\right)^2} \tag{4.3}$$

where f_{BW} is the signal bandwidth and σ_{jitter} is the clock jitter noise. Moreover, the SNR of DCRX can be derived as [20]:

$$SNR_{DCRX} \cong \frac{1}{\left(2\pi\sigma_{jitter}\right)^2 \cdot \left(f_{BW}^2 + 2 \cdot f_{LO}^2\right)} \tag{4.4}$$

where f_{LO} is the LO frequency. With Eq. (4.3) and Eq. (4.4), we can now compare the SNR of the two topologies:

$$\frac{SNR_{DCRX}}{SNR_{DSRX}} \cong \frac{f_{BW}^2}{f_{BW}^2 + 2 \cdot f_{LO}^2} \tag{4.5}$$

It is not surprising that the DSRX has better SNR since it is impacted by fewer noise sources. However, as mentioned in Section 4.1, the DSRX suffers from aliasing noise caused by insufficient BPF rejection. Therefore, the selection of f_{BW} and f_{LO} as well as the rejection provided by the BPF (in DSRX) and LPF (in DCRX) determines which receiver architecture provides better SNR.

Note that SNR is not the only consideration in the receiver design. As mentioned in Section 2.2, the gain stages in DSRX need to be implemented at a high carrier frequency thereby consuming higher power. In contrast, the gain stages in DCRX can be distributed between the carrier frequency and down-converted baseband frequency which makes it a better choice in terms of power consumption.

4.4 Quantization Noise and Phased-Array Gain

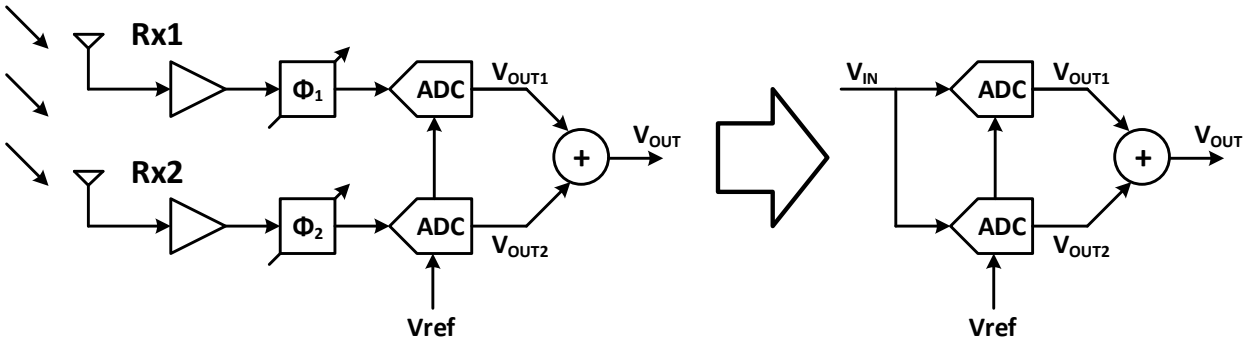
The main purpose of phased-array transceivers is to deliver directional data transmission. One added benefit of phased-array systems is the signal-to-noise ratio (SNR) improvement (often referred to as array gain), which can be expressed as:

$$SNR\ improvement = 10\log_{10} 2^{N_{element}} \tag{4.6}$$

where $N_{element}$ is the number of phased-array elements. From the equation above, 3-dB SNR improvement can be obtained every time the number of elements is doubled. This 3-dB

improvement is based on the assumption that by summing the two signals from two different arrayed elements, the signal is correlatively summed (6dB) and noise is un-correlatively summed (3dB).

This assumption stands for most phased-array systems: as discussed in Section 4.2, the noise performance is dominated by the receiver noise floor in most communication systems. The receiver noise floor is mainly thermal noise, which is un-correlated between different receiver paths. In contrast, in this research, the noise performance is dominated by the quantization noise of the ADC, which is highly correlated between different elements. Therefore, there is very minimal SNR improvement after the output signals being summed because the quantization noise remains correlated.



(a) (b)

Figure 4.6 (a) A two-element phased-array receiver. (b) Simplified circuit when the phased difference between the two elements are perfectly compensated by phase shifters Φ_1 and Φ_2.

To understand why the quantization noise is correlated among the different receiver elements, a two-element phased-array receiver is considered, as shown in Figure 4.6. Rx1 and Rx2 receive the same signal but with a phase offset (Figure 4.6a). Assuming phase shifters Φ_1 and Φ_2 compensate the phase difference perfectly, the two-element phased-array can be simplified as an identical V_{IN} feeding the two ADC inputs, see Figure 4.6 (b). Further assuming the Vref for the two ADCs in Figure 4.6 (b) are the same, the digital outputs of the two ADCs are:

$$V_{OUT1} = a_{n-1}2^{n-1} + a_{n-2}2^{n-2} + \cdots + a_0 2^0 = V_{OUT2} \quad (4.7)$$

where n is the number of the bits, a_{n-1},…, a_0 are either 0 or 1. From Eq. (4.7), we can see V_{OUT1} equals to V_{OUT2}. As a result, the quantization noise or quantization error for the two ADCs is identical, since they are converting the same analog input to the corresponding digital output based on the same Vref.

One potential technique that can de-correlate the ADC quantization noise is dithering [21]. Dithering is widely used in audio systems to eliminate periodic quantization error and increase spurious-free dynamic range (SFDR) performance of the ADC, see Figure 4.7. Applying a similar technique, each receiver element with a comparator (1-bit ADC) quantizes the incoming signal compared to random dithered levels to break the correlation between different arrayed elements. In a comparator, the dither can be applied to either the signal path or the V_{REF}, see Figure 4.8.

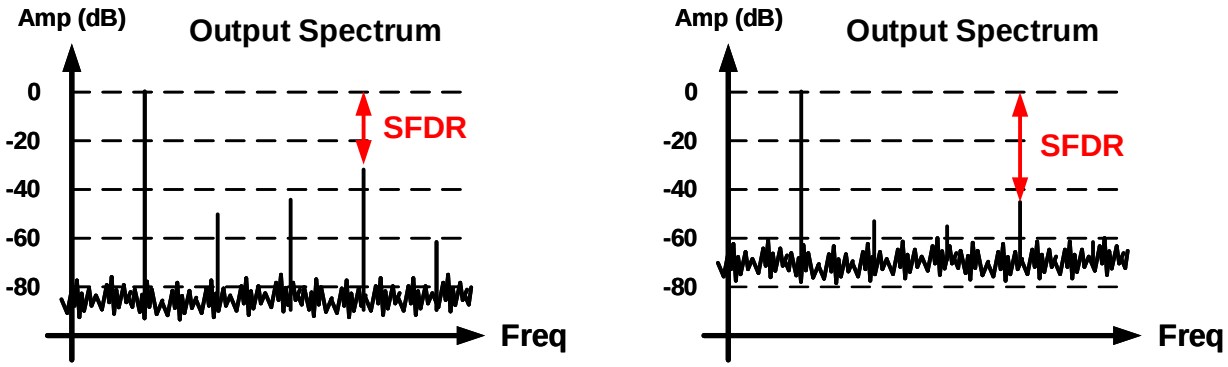
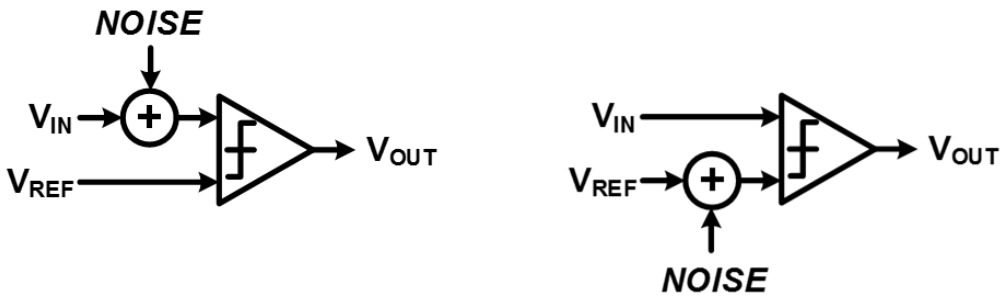
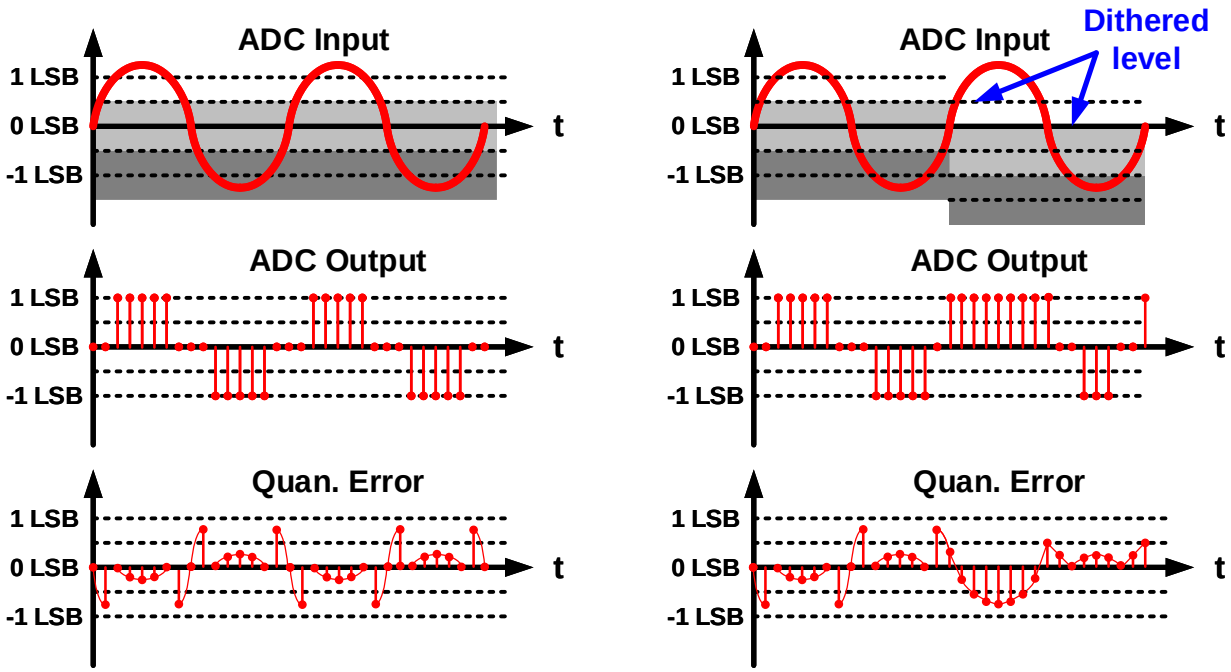


Figure 4.7 Output spectrum of an ADC (a) without and (b) with the dithering noise.



(a) (b)

Figure 4.8 Apply dither noise to the (a) signal path or (b) to the V_{REF}.



(a) (b)

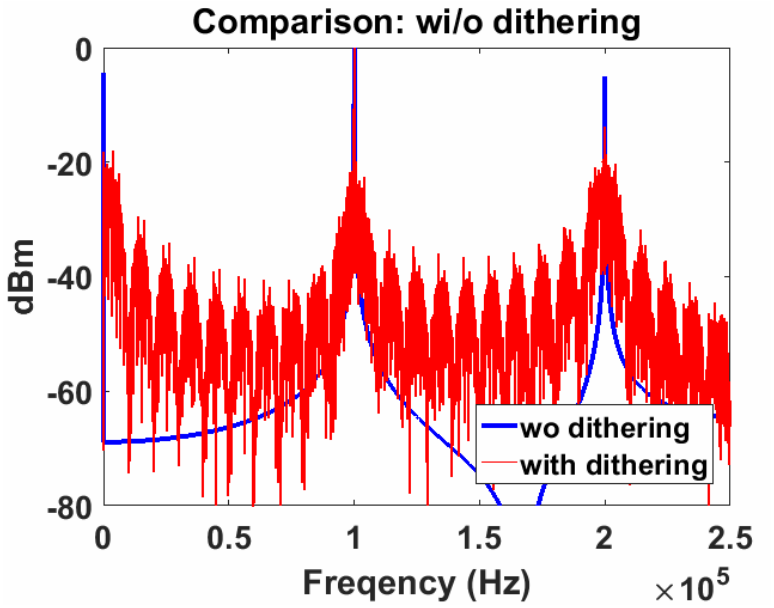
Figure 4.9 The ADC outputs with a sinusoidal input when the dithering noise (a) is not applied to the V_{REF} and (b) is applied to the V_{REF}.

To understand the benefit of adding dithering when applied to the V_{REF} of an ADC we start by observing Figure 4.9 which depicts the ADC outputs when two cycles of a sinusoidal are applied to the RX input, show here for two scenarios where the V_{REF} is without dithering noise in Figure 4.9 (a) but with dithering noise in Figure 4.9 (b). In Figure 4.9 (a), the relationship between

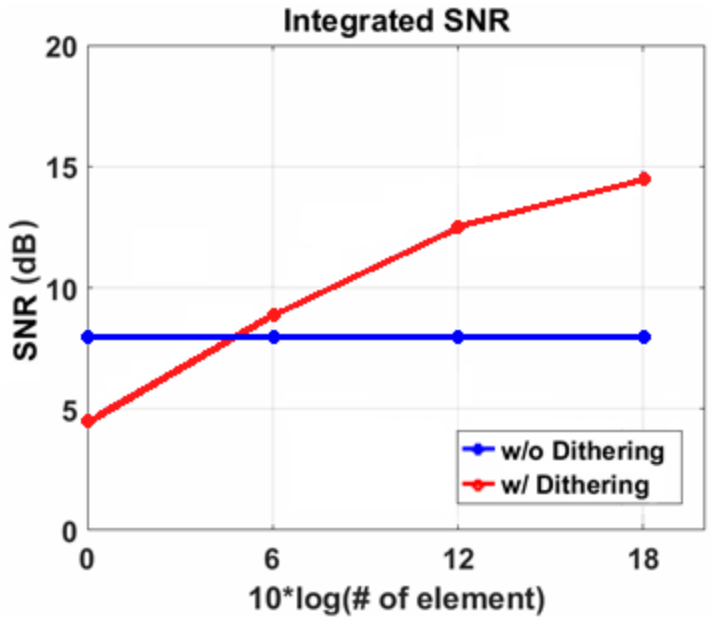
comparator input and output is:

$$V_{OUT} = \begin{cases} 1, & when\ V_{IN} > 0.5LSB \\ -1, & when\ V_{IN} < -0.5LSB \\ 0, & when\ 0.5LSB > V_{IN} > -0.5LSB \end{cases} \quad (4.8)$$

As shown in Figure 4.9 (a), the quantization error is the difference between ADC input and output. We can clearly see that the quantization error is periodic so significant harmonics can be observed in the ADC output spectrum, see Figure 4.7 (a). Figure 4.9 (b) shows the ADC output when a dithering noise is applied to the V_{REF}. Because of dithering, the V_{REF} varies from the first sinusoidal cycle to the second cycle thereby breaking the periodicity of the quantization error. As a result, the SFDR can be improved with an increased noise floor, see Figure 4.9 (b). Similarly, applying independent but uniformly-distributed dither generator to each receiver elements can make the quantization error among the phased array un-correlated.



(a)



(b)

Figure 4.10 Sinusoidal input simulations: (a) output spectrum of 1-bit ADC with and without dithering noise; (b) SNR v.s. the number of elements of the phased-array receiver.

The MATLAB SNR simulations of a sinusoidal input with and without dithering are shown in Figure 4.10. The dithering noise is applied to the V_{REF} levels of a 1-bit comparator. Figure 4.10 (a) shows the 1-bit ADC output spectrum for a single receiver element. The blue line and the red line indicate the fast Fourier transforms (FFT) with and without dithered levels where the integrated SNR are 7.94dB and 3.37dB, respectively. The one with dithered levels shows a lower SNR of 3.37dB, which is expected since the dithered levels behave like a random noise added to the output waveform. Figure 4.10 (b) shows a comparison of SNR versus the number of phased-array elements for a simple 1-bit ADC array and a 1-bit ADC arrays with pseudo-random dithering in blue and red, respectively. The SNR of the un-dithered 1-bit ADC array is shows no improvement when adding more elements (the blue line in Figure 4.10b). This is because the quantization noise between each element is correlated. In contrast, the 1-bit comparator with pseudo-random dithering begins with a lower SNR because of the added dither noise, as compared

to the one without the dither noise. When summing the outputs of more elements, the comparators with dithering provide a significant SNR improvement (see Figure 4.10b, the red line). Again, since the random dithering makes the quantization noise among the phased-array elements un-correlated, the phased-array gain can be obtained.

4.5 Modulation Simulation

The challenges and considerations about the 1-bit ADC design have been discussed in the last few sections. Now the exploration will be extended to modulated signals. Figure 4.11 shows an example MATLAB test bench used for simulating the data modulation and demodulation with different conditions. This bench provides flexibilities such as changing different modulation schemes (QPSK, 16QAM, etc.), data rates, and the number of bits for the ADC. Note that there is no frequency conversion in this simplified test bench. As mentioned in Section 4.4, the phase difference among receiver elements is assumed to be compensated perfectly by the phase shifters in each of the receivers. Therefore, the inputs of each ADC in individual receiver elements are the same.

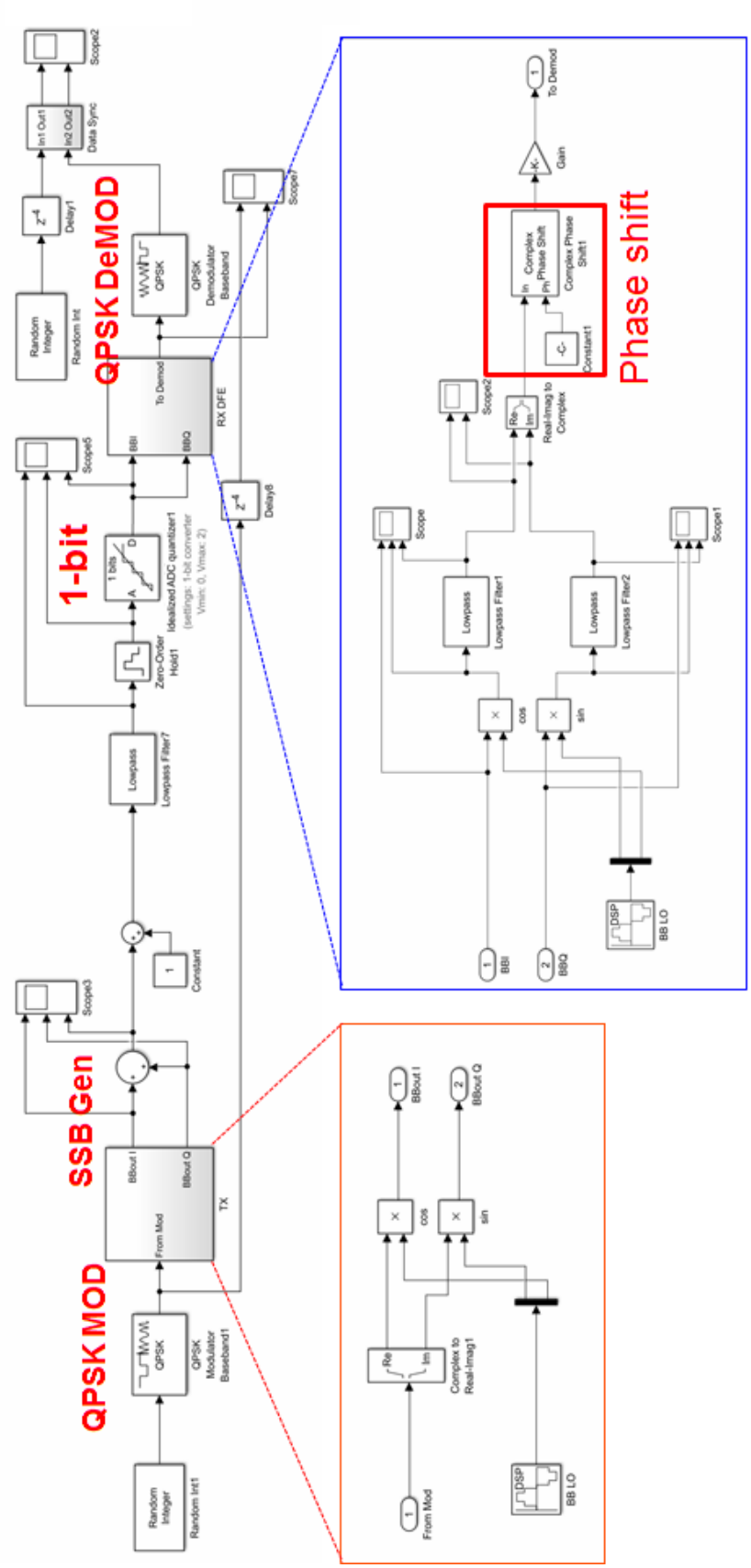


Figure 4.11. An example of the MATLAB test bench for the QPSK modulation simulations.

Figure 4.12 shows the implementation of a 1-bit comparator with dithering added to the V_{REF} in MATLAB. The 1-bit comparator is modeled as a compare-to-zero function where its input is subtracted by V_{REF} plus a uniform random dither and then compares with zero, see Figure 4.12.

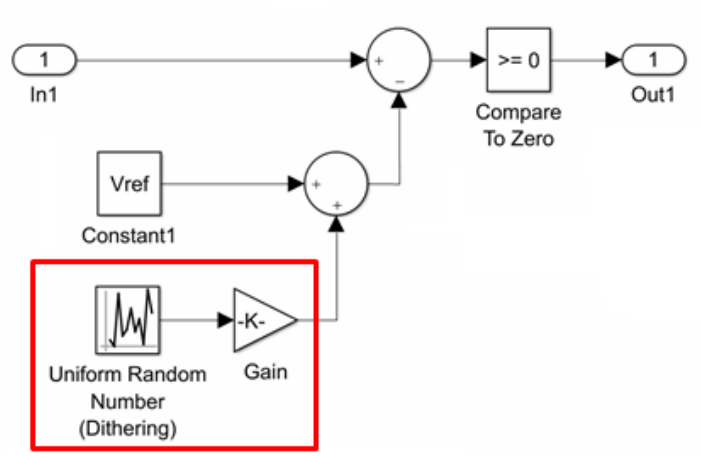
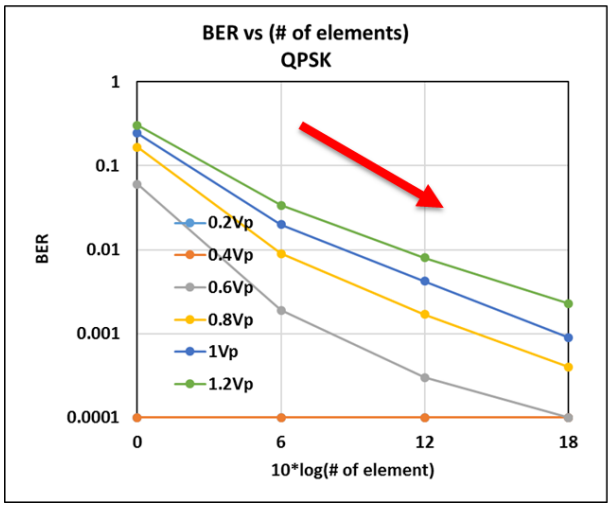


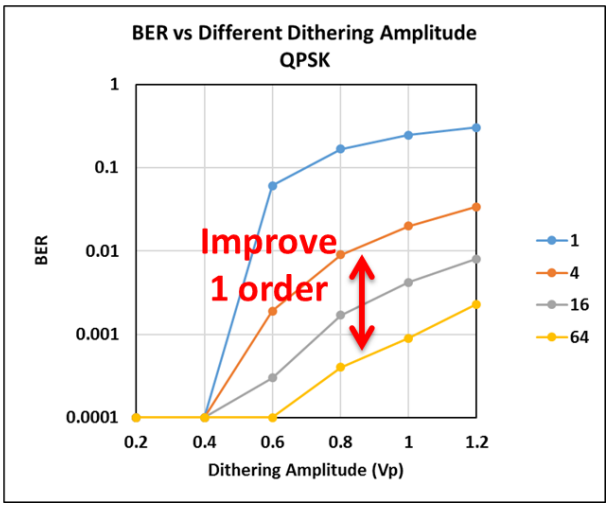
Figure 4.12 Implementation of a 1-bit comparator with dithering added to the V_{REF}.

With the abovementioned MATLAB environment, Figure 4.13 presents some simulation results with different modulation schemes, dither noise amplitudes, and the number of elements. Figure 4.13 (a) shows the results for QPSK modulation. In this MATLAB setup, 10,000 QPSK symbols were simulated to calculate the bit error rate (BER) which sets the BER floor of $1x10^{-4}$. Moreover, this simulation covers the number of elements (N_{EL}) of 1, 4, 16, and 64 and dithering amplitude of 0.2Vp, 0.4Vp, 0.6Vp, 0.8Vp, 1Vp, 1.2Vp. All the BER numbers are shown in the table. The BER vs. $10\log_{10}(number\ of\ element, N_{EL})$ is plotted on the left and BER vs. dithering amplitude is plotted on the right. The plot on the left shows the BER is improving when adding more elements. This is aligned with the expectation which more elements provide high array gains and thus better SNR can be achieved. In the plot on the right, the BER becomes worse when a higher dithering amplitude is applied. This is also expected since higher dithering amplitude introduces more noise power into the ADC. Note that the BER numbers are $<10^{-4}$ when dithering amplitudes are 0.2Vp and 0.4Vp for all rows in the table. This implies the SNR for a 1-

bit ADC is good enough to demodulate QPSK signals.

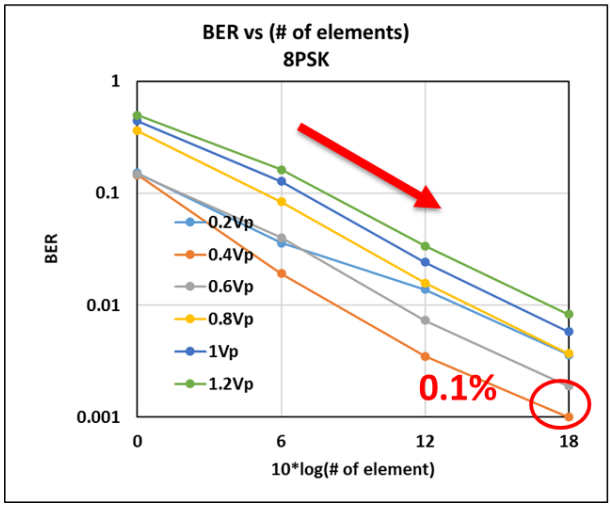
Modulation: QPSK		Dithering Amplitude (Vpeak)						
N_{EL}	$10*\log_{10}(N_{EL})$		0.2Vp	0.4Vp	0.6Vp	0.8Vp	1Vp	1.2Vp
1	0	BER	$<10^{-4}$	$<10^{-4}$	0.0606	0.1671	0.2456	0.304
4	6		$<10^{-4}$	$<10^{-4}$	0.0019	0.009	0.02	0.0338
16	12		$<10^{-4}$	$<10^{-4}$	0.0003	0.0017	0.0042	0.008
64	18		$<10^{-4}$	$<10^{-4}$	$<10^{-4}$	0.0004	0.0009	0.0023

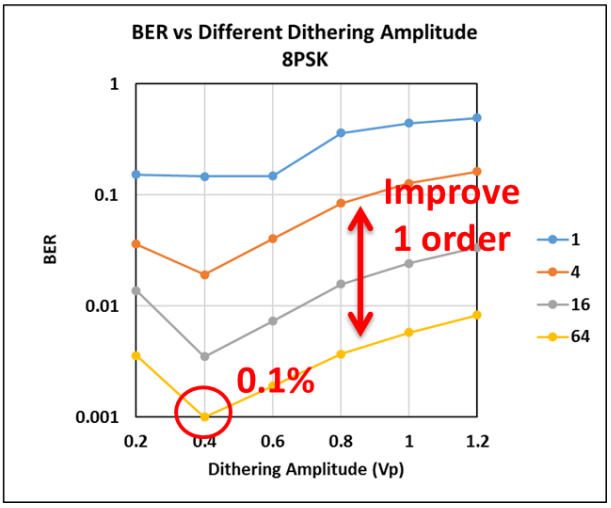




(a)

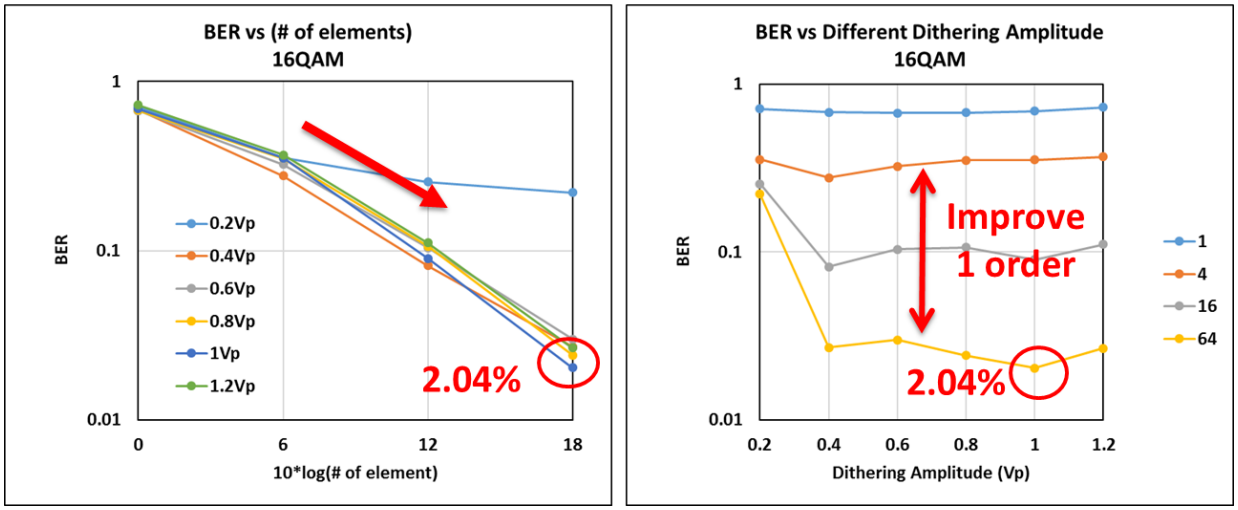
Modulation: 8PSK		Dithering Amplitude (Vpeak)						
N_{EL}	$10*\log_{10}(N_{EL})$		0.2Vp	0.4Vp	0.6Vp	0.8Vp	1Vp	1.2Vp
1	0	BER	0.1521	0.1463	0.1477	0.3616	0.4437	0.4958
4	6		0.0361	0.0192	0.0402	0.0841	0.1274	0.163
16	12		0.0138	0.0035	0.0073	0.0158	0.0242	0.0337
64	18		0.0036	0.001	0.0019	0.0037	0.0058	0.0083





(b)

Modulation: 16QAM		Dithering Amplitude (Vpeak)						
N_{EL}	$10*\log_{10}(N_{EL})$		0.2Vp	0.4Vp	0.6Vp	0.8Vp	1Vp	1.2Vp
1	0	BER	0.7104	0.6791	0.6724	0.6748	0.689	0.7267
4	6		0.3556	0.2767	0.3239	0.3523	0.3539	0.369
16	12		0.2551	0.0814	0.1038	0.1063	0.09	0.1113
64	18		0.2207	0.027	0.03	0.0242	0.0204	0.0267



(c)

Figure 4.13 MATLAB simulation results of modulated signals. The simulations were performed with different dithering amplitude and number of elements. The results for different modulation schemes are shown: (a) QPSK, (b) 8PSK, and (c) 16QAM.

Figure 4.13 (b) shows the same simulation but with 10,000 8PSK symbols. Again, the plot on the left shows that the BER is improving as expected when more elements are added into the system. The plot on the right shows a local optimal point is observed when the dithering amplitude is 0.4Vp. This optimal point indicates that the dithering amplitude of 0.4Vp is high enough to break the correlation among the receiver elements so a good amount of array gain can be obtained. It is worth mentioning that, unlike QPSK, the BER is initially high so a 1-bit ADC is not sufficient to demodulate 8PSK signals well. However, with more uncorrelated elements summing up together, a good BER can be obtained.

Figure 4.13 (c) shows the simulation for 16QAM signal. The best obtainable BER is still as high as 2% even with 64 elements. This implies even with the help of the array gain, the 1-bit ADC

is still not good enough for 16QAM.

4.6 CONCLUSION

This chapter highlights some in-depth discussions of the design challenges for 1-bit low-resolution phased-array receivers. The link budget analysis is done in terms of thermal noise, clock jitter, and phase noise with two receiver topologies. In the low-resolution front-end designs, un-correlating the ADC quantization noise among the receiver elements is essential to obtain the improved SNR from the phased-array gain. The MATLAB simulations are presented to demonstrate the idea of applying dithering noise to break the correlation with both sinusoidal and modulated signals.

Given by the system-level analysis, using purely 1-bit low-resolution ADC for high-level data modulations such as 16QAM is still not practical. A reconfigurable 0-3 SMASH continuous-time delta-sigma ADC is described in the next chapter. This ADC is utilized in a 2x2 phased-array receiver and supports an open-loop 1-bit comparator with dithering (to obtain the array gain) and a closed-loop delta-sigma ADC when a high SNR is required for a 16QAM modulation. This prototype chip serves as a platform to demonstrate the study done in this chapter.

Chapter 5. HIGHLY-DIGITIZED MILLIMETER-WAVE PHASED-ARRAYED RECEIVER WITH RECONFIGURABLE CONTINUOUS-TIME DELTA-SIGMA ADC

Phased-array receivers are usually adapted to provide a directional spatial notch and enhanced performance at mm-Wave frequency bands. A number of different architectures are proposed [2][4][5]. As mentioned in Chapter 2, RF beamformers (BF) introduce lossy phase shifters [2]. LO BFs suffer from hardware complexity [4]. Baseband BFs occupy only a small silicon size but require high linearity and can generate only one directional beam [5]. In contrast, though digital BFs require high linearity since they also lack spatial notch in the front-end similar to baseband BF, they can provide multiple directional beams simultaneously [6]. Moreover, though mm-Wave provide ultra-wide BW of a few GHz for high data rates, most recent reported single-chip implementations usually use expensive table-top Arbitrary Waveform Generators (AWG) and Vector Signal Analyzers (VSA) to generate the multi-Gbps modulated signal at the TX input and demodulate the signal at the RX output, respectively [22], [23]. Therefore, new technologies to develop Gbps ADCs and DACs with low power are highly desirable to replace these high-end and power-hungry instruments. Furthermore, as discussed in Chapter 3, though mixer-first receivers are compact in size and highly linear, the noise performance is poor due to the absence of the gain stage in front of the noisy down-conversion mixer.

This chapter describes a highly-digitized mm-Wave phased-array receiver with a digital beamformer to address the abovementioned issues.

5.1 System Architecture and Link Budget

Figure 5.1 depicts the receiver architecture for the unlicensed mm-Wave band around 60GHz

for the backhaul wireless communications. The proposed 2x2 (4-element) phased-array receiver contains a noise-suppressing direct-conversion receiver (DCRX) front-end, a baseband amplification with low-pass filtering, a reconfigurable 0-3 sturdy MASH (SMASH) continuous-time delta-sigma (CT-ΔΣ) ADC, a digital poly-phase decomposition, and synthesized digital back-end (DBE). With the discussion from Section 2.2, the mixer-first DCRX architecture is employed for good power efficiency with a feedforward path to improve the gain and noise performance. The reconfigurable 0-3 SMASH CT-ΔΣ ADC can operate in two modes:

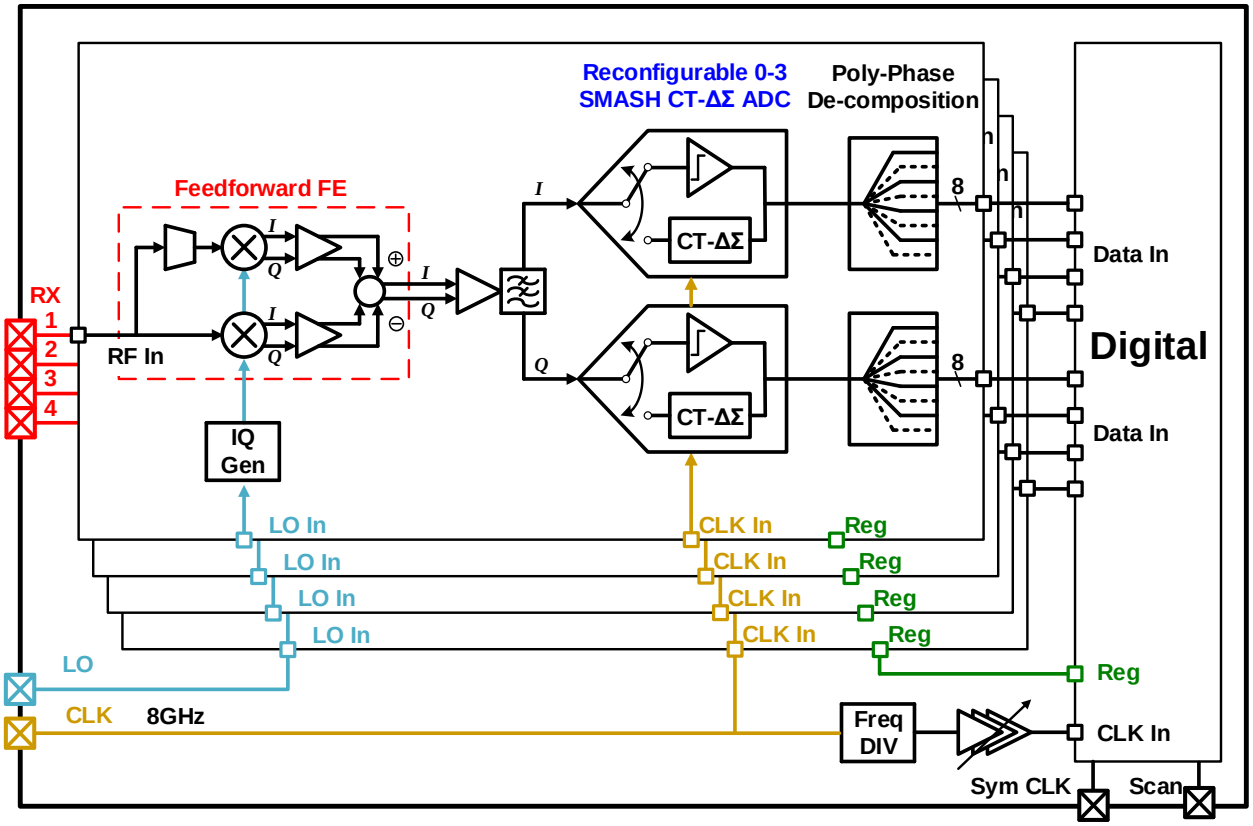


Figure 5.1 System architecture of the mm-Wave 4-element phased array receiver with reconfigurable ADC and highly-digital elements for radar and communication applications.

(1) An open-loop 1-bit digitizer (i.e. a comparator) to save power consumption when only low SNR (~10dB for QPSK) is required (for example, beam search).

(2) A closed-loop of the 0-3 SMASH CT-ΔΣ which can achieve high dynamic range (DR)

with the penalty of additional power consumption needed for the ADC third-order feedback loop.

5.1.1 *Frequency Plan*

The proposed direct-conversion RX operates at V-band with a LO around 60GHz. The 8-GHz clock is given independently via a dedicated pad, see Figure 5.1. This clock is then provided to the 2x2 phased-array for the 2-way time-interleaving (TI) comparators as well as a divide-by-4 frequency divider to generate a 2-GHz system clock sending to the digital backend. The over-sampling rate (OSR) of the ΔΣ ADC is 2^3 (will revisit this in the next Section). Therefore the Nyquist bandwidth is $8GHz \times 2 \div 2^3 = 2GHz$. The baseband signal bandwidth is $2GHz \div 3 = 666MHz$ for I or Q path.

5.1.2 *ADC Specification*

The dynamic requirement (DR) of the ADC is composed of several components. Figure 5.2 shows the breakdown of each component in this design. The 16-dB SNR requirement specified in this design is for a 16-QAM modulation scheme. The ADC noise floor is 8dB lower than the receiver noise floor which contributes a minor 0.6-dB degradation to the overall SNR. The margin of 2dB is reserved for some non-idealities such as gain error. 5dB of the peak to average power ratio (PAPR) is assigned here which is accounted for the instantaneous peak power of a 16QAM signal. All these numbers add up to a total dynamic range of 31dB for the ADC. The approximated SNR for continuous-time (CT) delta-sigma (ΔΣ) ADC can be expressed in dB with an OSR of 2^n as [24]:

$$SNR_{dB} = 3.01\mathrm{n}(2L + 1) - 9.36\mathrm{L} - 2.76 \quad (5.1)$$

where L is the loop order and n is the OSR. We can now generate a table of CT-ΔΣ ADC SNR

using Eq. (5.1), see Table 5.1. Here, we choose to use a third-order loop with OSR of 2^3 where a theoretical achievable SNR of 32.4dB.

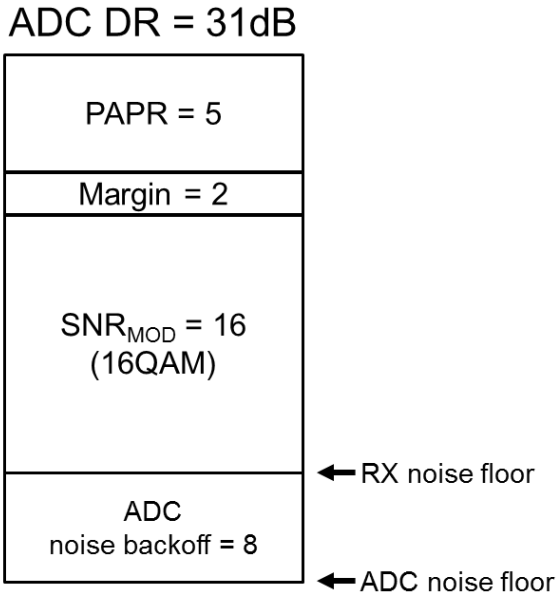


Figure 5.2 Breakdown of ADC dynamic range requirement.

Table 5.1 Achievable ADC dynamic range as function of loop order and oversampling rate.

		OSR (2^n)				
		2^1	**2^2**	**2^3**	**2^4**	**2^5**
Loop Order	**1**	-3.09	5.94	14.97	24	33.03
	2	-6.43	8.62	23.67	38.72	53.77
	3	-9.77	11.3	**32.37**	53.44	74.51
	4	-13.11	13.98	41.07	68.16	95.25
	5	-16.45	16.66	49.77	82.88	115.99

5.2 FEEDFORWARD NOISE-SUPPRESSING RECEIVER FRONT-END

As mentioned in Section 3.2, mixer-first architectures (see Figure 5.3a) are shown to have a broad bandwidth and down-convert the signal to baseband, however, this class of receivers suffers from poor noise figure (NF). Figure 5.3 (b) shows the proposed mixer-first receiver with feedforward G_m path to provide an additional gain in parallel with the original mixer-first receiver.

This additional gain is summed at the baseband with the same polarity. A side-benefit of this architecture is it performs noise-suppressing to the noise generated from the mixer-first receiver. This technique is analogous to a mixer-first noise-canceling front-end [25], however, there are differences. First, this is the first implementation of its kind that has not been published in the mm-Wave bands. Strictly speaking, the intention is not to cancel the noise generated from the mixer but to provide a feedforward path to increase RX gain to reduce noise (Figure 5.3c).

To understand the proposed architecture, we will look at Figure 5.3 (b) when the desired signal is presented at the RF input. Again, this receiver has two paths to amplify the signal which are the mixer-first RX path and the feedforward G_m path. Note that the mixer-first path is designed to perform the input match where the G_m path is designed to provide additional gain. The G_m path provides a higher gain than the mixer-first path. As shown in Figure 5.3 (b), the signal travelling through the mixer-first receiver path remains positive polarity. On the other hand, the G_m path is positive at the RF input, negative at the G_m output, and becoming positive polarity again after the subtraction at the baseband output. The signal is summed constructively at the baseband output.

In contrast, Figure 5.3 (c) shows the situation considering the mixer-first receiver noise is presented. Similar to conventional noise-canceling receivers [25], the mixer noise, $\overline{V_{n,mix}^2}$, generated from the mixer-first receiver exhibit an inverse polarity at the G_m input. Therefore, the mixer noise, $\overline{V_{n,mix}^2}$, can be suppressed at the baseband output after subtraction. The mixer noise is only *suppressed* but not *canceled* because the gains from the RF input to the receiver output seen by the mixer noise are not aligned. As a result, the noise can only be suppressed. Note that the noise-canceling receiver in [25] is built for the frequency <2.7GHz. It is worth to match the gains and cancel the mixer noise since the it is the dominant contributor. However, in this design, both mixer-first and G_m paths contribute significant noise. Having an aligned gain to cancel out the

mixer noise is not the best solution.

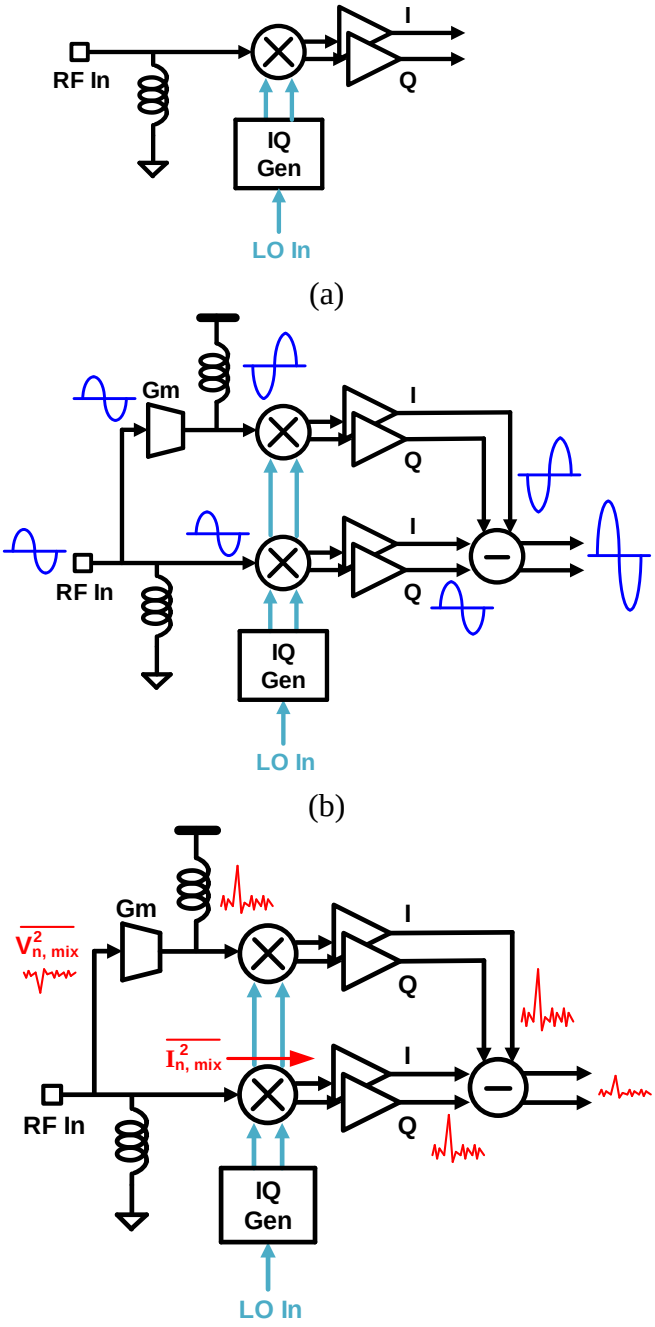


Figure 5.3 (a) Conventional mixer-first receiver. Conceptual diagram of the mixer-first receiver with feedforward noise-suppressing when (b) signal is presented at RF IN and (c) mixer noise is presented.

Figure 5.4 shows the detailed schematic of the proposed feedforward noise-suppressing receiver. The two paths are identical except for an added G_m amplifier for the feedforward path. The G_m amplifier is implemented with a cascode common-source stage. The subtraction is done by inverting the connection at the TIA baseband output, see Figure 5.4.

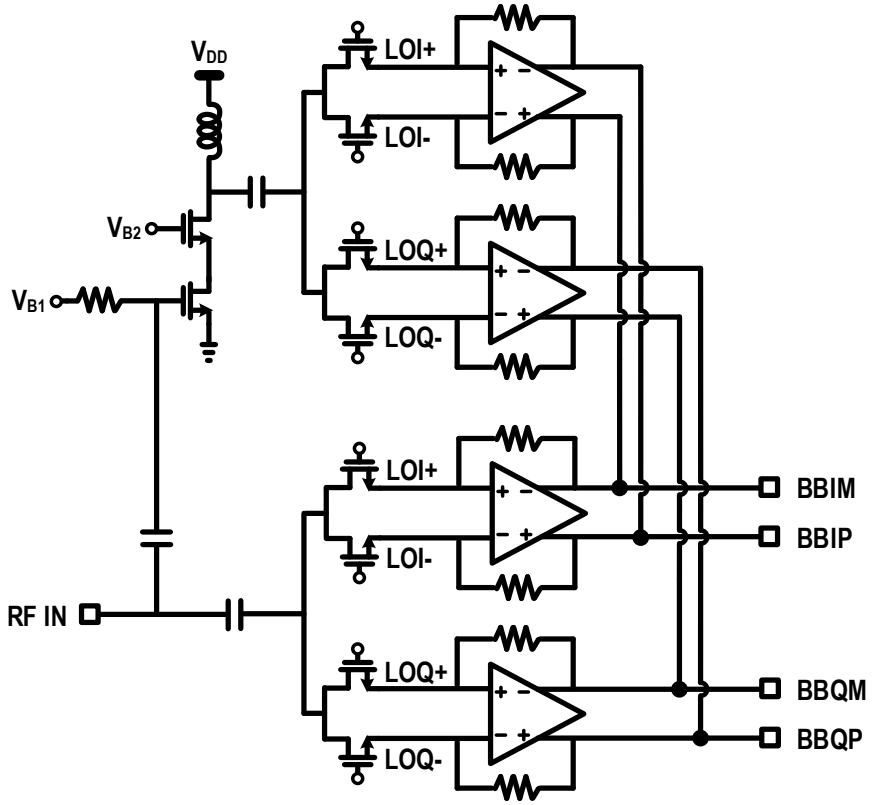


Figure 5.4 The circuit schematic of the feedforward noise-suppressing receiver front-end.

The RX front-end layout is shown in Figure 5.5, including the active functional blocks, passive inductors, and V_{DD}/GND planes with de-coupling caps (Figure 5.5b). At mm-Wave frequencies, the interaction between inductors and the non-ideal V_{DD}/GND degrade the accuracy of the passive component modeling. Therefore, the whole passive portion in this design is characterized by the EM simulation using Lorentz Peakview simulator [26], including inductors and V_{DD}/GND planes for the best accuracy. The layout view and field view of Peakview simulation are shown in Figure 5.5 (c) and Figure 5.5 (d), respectively.

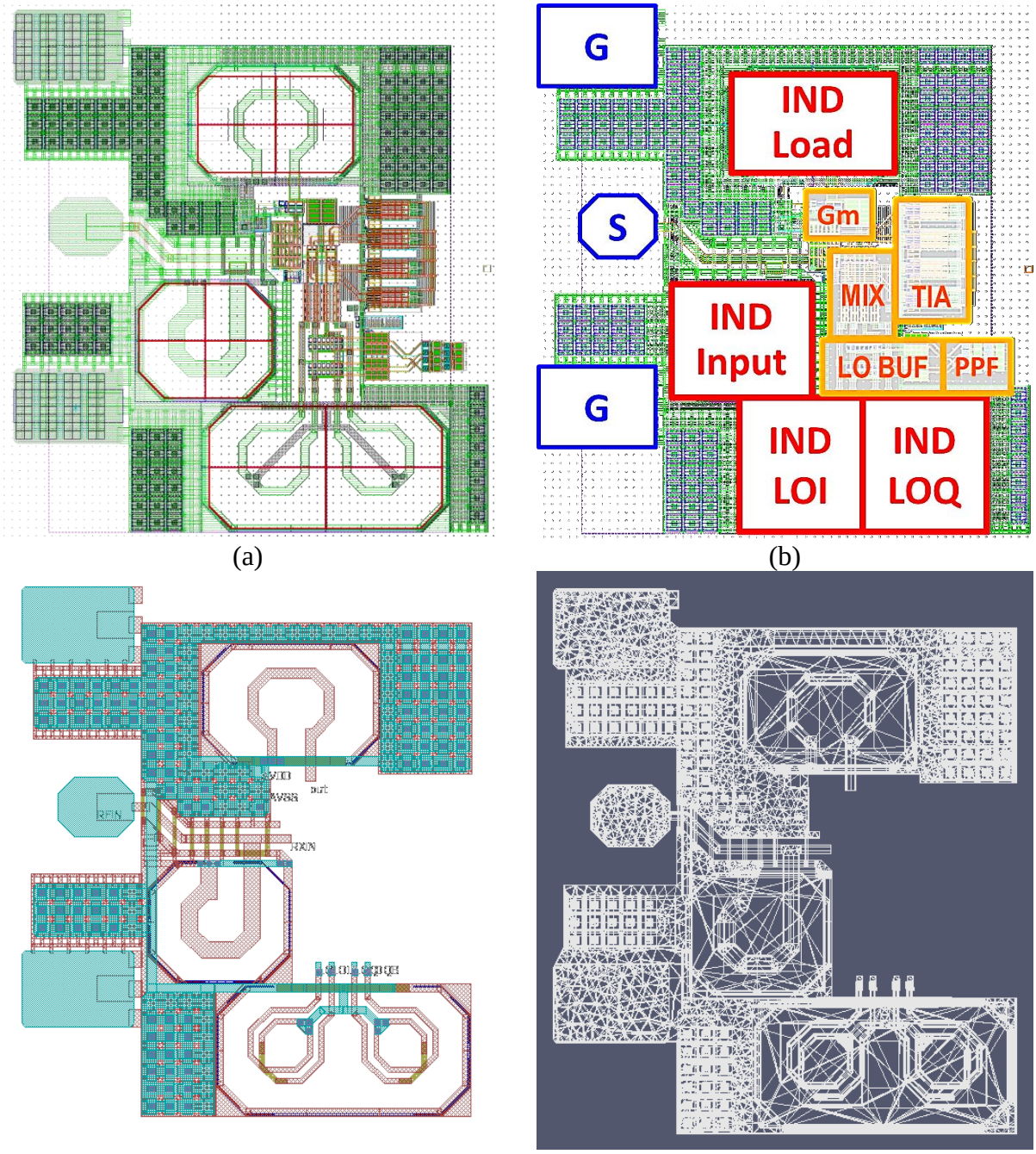


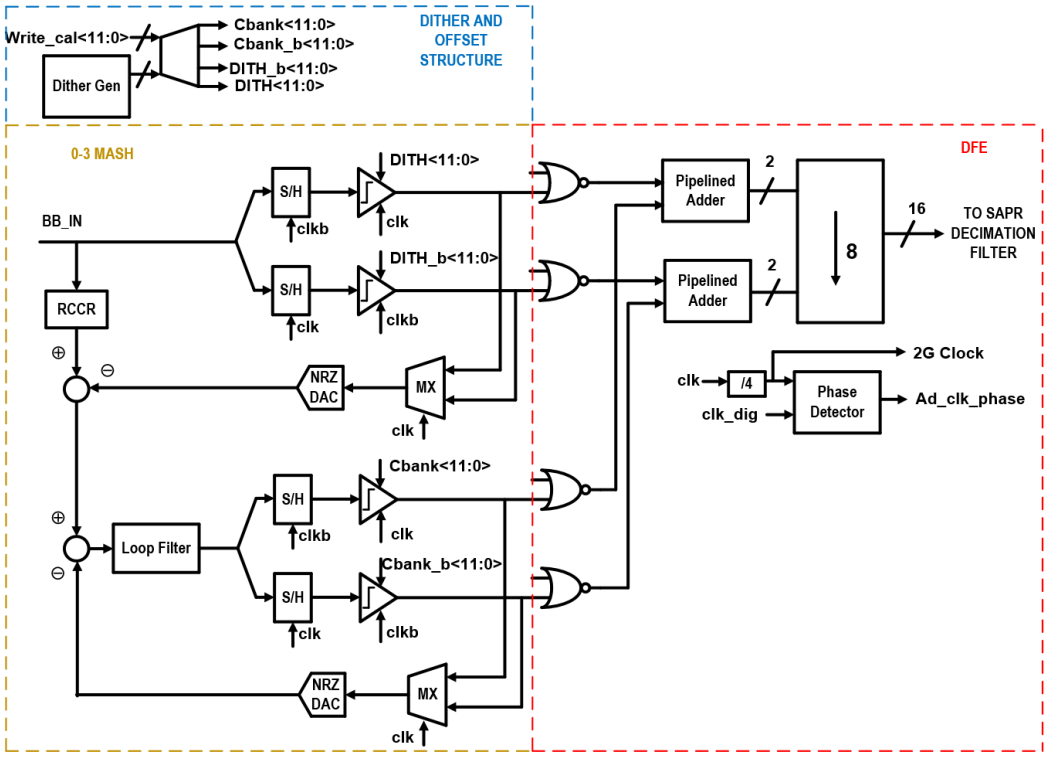
Figure 5.5 (a) The layout of the proposed feedforward noise-suppressing receiver. (b) Notation to different functional blocks. (c) The passive portion of the layout simulated in Peakview, including inductors and VDD/GND planes. (d) The field view of the simulated passive structure.

5.3 RECONFIGURABLE ADC AND DITHER GENERATOR

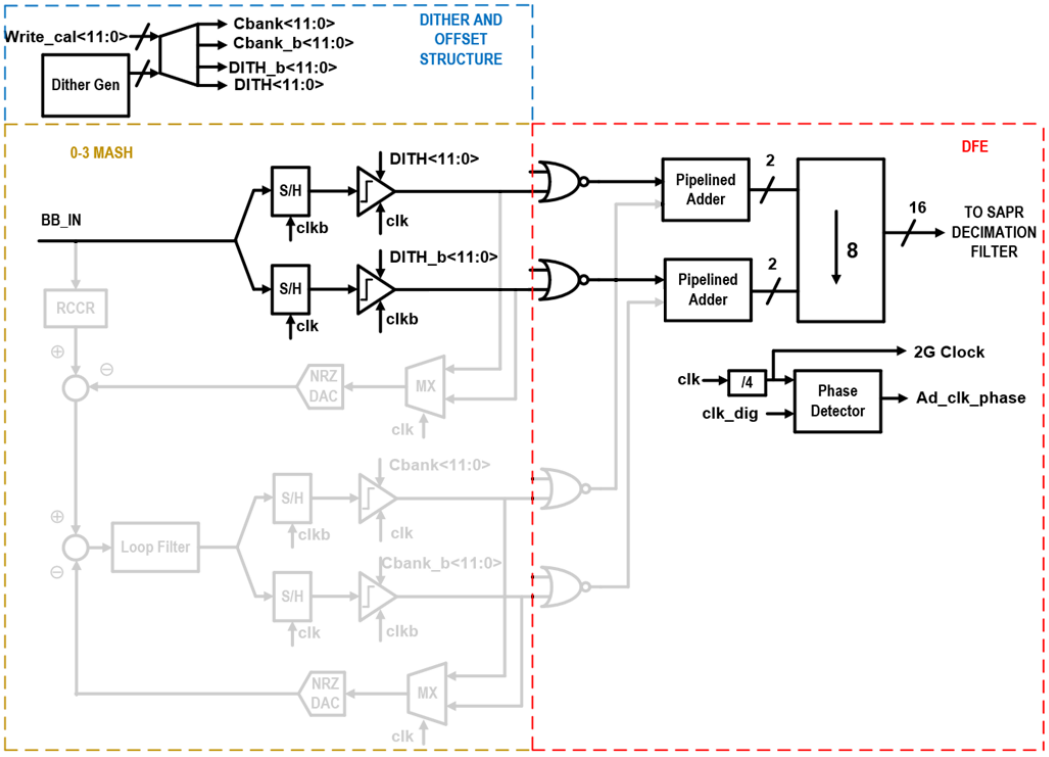
The ADC in the design can be configured as an open-loop 1-bit comparator and a closed-loop 0-3 SMASH CT-ΔΣ ADC. Figure 5.6 shows the block-level diagram of this reconfigurable ADC. When all the blocks are ON (except for the dither generator), it is a 0-3 SMASH CT-ΔΣ ADC [27]. The 0-3 SMASH architecture is composed of two parallel paths, an open-loop comparator, and a 3^{rd}-order CT-ΔΣ loop, see Figure 5.6 (a). The comparator employs a 2-way time-interleaving topology to increase the sampling rate for achieving a high oversampling rate (OSR). The outputs of the two paths are gated for the configurations between open-loop and closed-loop modes. The pipelined adders are used for summing the outputs from the two paths followed by an 8-way poly-phase decomposition before being sent to the digital front-end.

Figure 5.6 (b) depicts the open-loop configuration where the 3^{rd}-order CT-ΔΣ loop is OFF. The ADC is now a simple 1-bit comparator. As mentioned in Chapter 4, the phased-array gain can be obtained only if the quantization noise among the arrays is un-correlated. To make the quantization noise un-correlated among, a dither generator is employed which is combined with the DC offset compensation of the comparator, see Figure 5.6 (b). The dither generator is implemented with linear feedback shift registers (LFSR) [28] to provide uniformly-distributed random bitstream to un-correlate the quantization noise among the 4 receiver elements.

Figure 5.7 shows the architecture of the 3^{rd}-order continuous-time (CT) delta-sigma (ΔΣ) ADC. The loop filter utilizes a capacitive feedforward architecture with an excess loop delay (ELD) compensation through resistors R1, R2, R3 and Rf [29]. The noise transfer function (NTF) is derived as:



(a)



(b)

Figure 5.6 The block-level diagram of the ADC configured as: (a) closed-loop 0-3 SMASH CT-ΔΣ ADC, and (b) open-loop comparator with dither generator

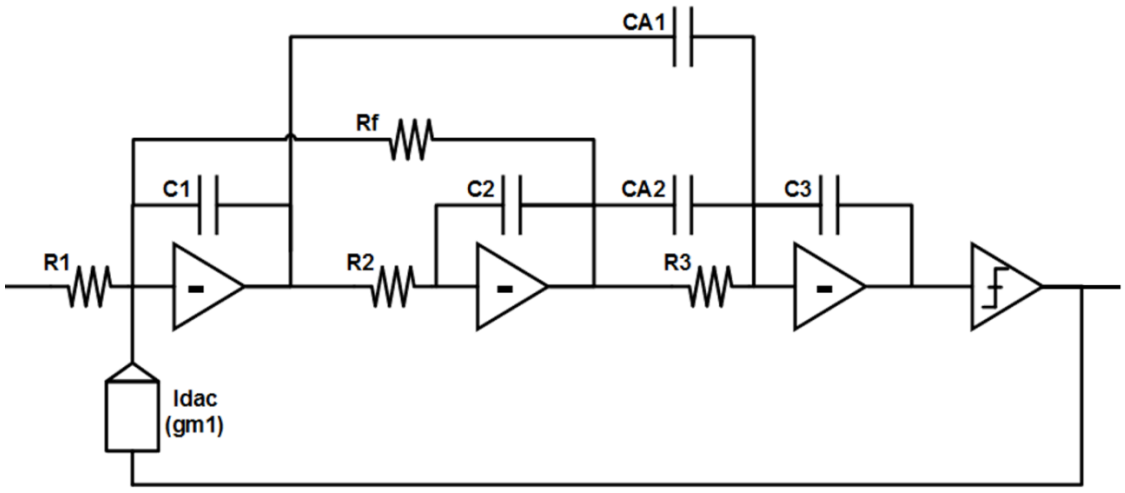


Figure 5.7 The 3rd-order CT-ΔΣ ADC.

$$NTF = \frac{\frac{s^3 C_{A1} R_3 C_2 R_2 C_1}{gm_1}}{1 + sC_{A2}R_3 + s^2 C_{A1} R_3 C_2 R_2 + \frac{s^3 C_{A1} R_3 C_2 R_2 C_1}{gm_1}} \tag{5.2}$$

For an ideal 3rd-order high-pass Chebyshev response (as shown in Figure 5.7) synthesized from MATLAB:

$$NTF_{MATLAB} = \frac{s(s^2 - 0.16s + .09)}{(s + 0.43)(s^2 - 0.43s + .18)} \tag{5.3}$$

Equating (5.2) and (5.3), we can get:

$$\frac{gm_1}{s^3 C_1 R_2 C_2 R_3 C_3} + \frac{gm_1 C_{A2}}{s^2 C_1 R_2 C_2 C_3} + \frac{gm_1 C_{A1}}{sC_1 C_3} = \frac{0.67(s^2 + 0.27s + .077)}{s(s^2 + 0.093)} \tag{5.4}$$

Solving Eq. (5.4), the design equations would result in:

$$\frac{C_{A2}}{C_3} = 0.27 \tag{5.5}$$

$$\frac{C_{A1}}{C_3} = 0.67 \tag{5.6}$$

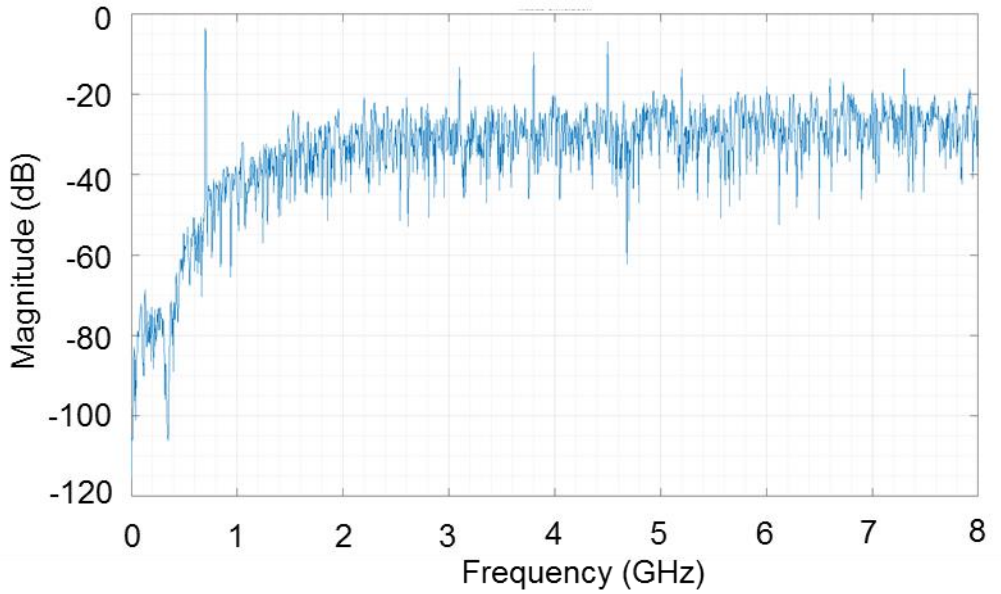


Figure 5.8 The frequency response of the ideal 3rd-order high-pass Chebyshev response synthesized from MATLAB

5.4 MEASUREMENT PLAN

This prototype 2x2 V-band phased-array receiver is designed using TSMC 28nm CMOS HPC+ technology. There are standalone test structures of feedforward mm-Wave front-end and the reconfigurable ADC that can be characterized independently.

5.4.1 *Test Structure and Test Mode*

Figure 5.9 shows the test structure of this prototype chip that contains four identical receiver elements with I/Q ADC outputs to the digital back-end, a standalone front-end, and a standalone test ADC. To measure the phased-array, the signals RX1-RX4, LO_60g, and Clk_8g will be given from a custom probe. The digitized ADC outputs are routed to the digital back-end for the digital signal processing for beamforming and data demodulation. Moreover, these digitized ADC outputs

also have the access to the memory for downloading to the computer for further data analysis and post-processing.

The front-end standalone test structure is identical to the feedforward mm-Wave front-end used in the phased-array elements with the access points to the mm-Wave receiver input and the baseband analog output through probing pads. The key performance metrics of the FE can be characterized independently, such as gain, noise figure, and linearity. The input and the clock of the standalone ADC can also be accessed through bond wires or by using probes. The ADC digital output can be saved in on-chip memory for the data analysis using computers.

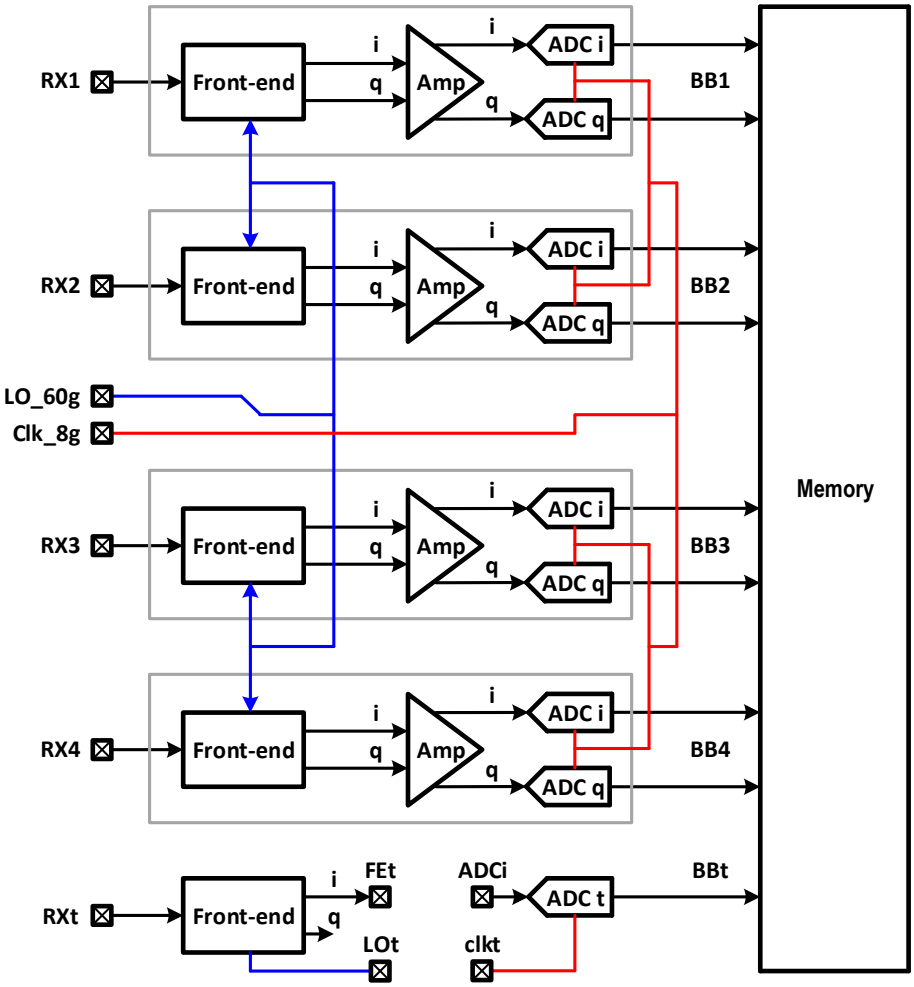
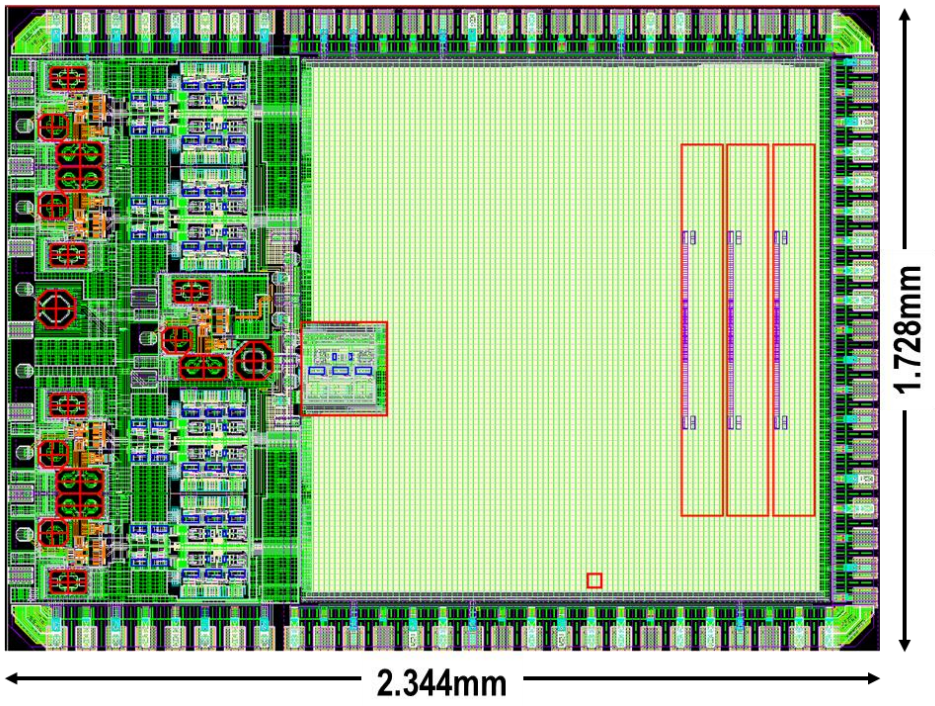
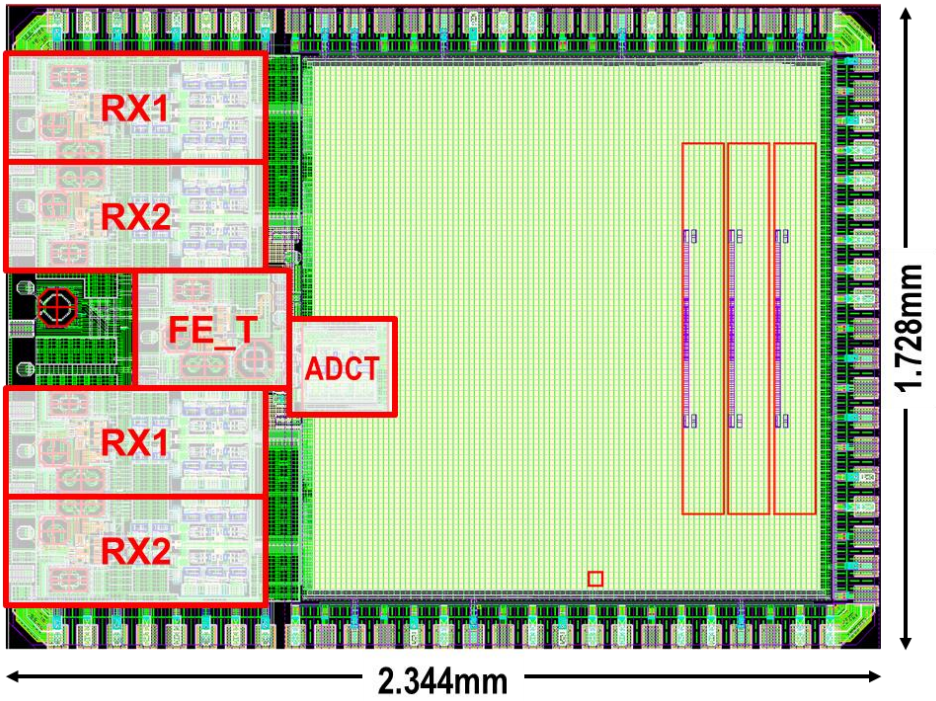


Figure 5.9 Test structure of the prototype chip.



(a)



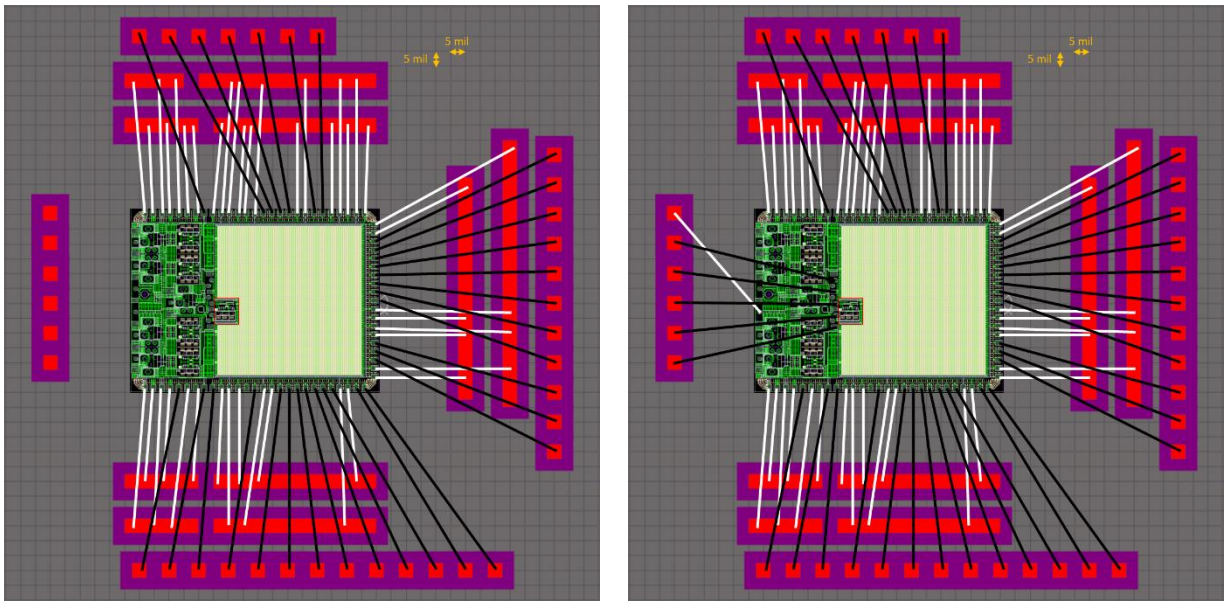
(b)

Figure 5.10 The layout of the proposed highly-digitized 2x2 phased-array receiver (a) layout only (b) layout with notations.

With these test structures, this prototype chip can support the measurement features as follows: 1) phased-array measurements: tone-based measurements, beamforming and beam pattern, modulated signal tests. 2) standalone mm-Wave front-end measurements: input return loss (S_{11}), conversion gain, noise figure, input P_{1dB}, and OP_{1dB}. 3) standalone ADC characterization: frequency response, dynamic range, INL, DNL, open-loop operation, closed-loop operation. This ADC test structure also allows running some extensive dithering experiments, such as different dithering amplitude and pattern rate.

5.4.2 *Layout*

Figure 5.10 shows the layout of the proposed receiver. The drawn size is 2.344x1.728mm^2. The 4-element receiver front-end is on the left of the chip with a massive synthesized digital back-end to the right. Figure 5.10 (b) shows the layout with notations of each of the 4-element receiver as well as the test structures of standalone mm-Wave front-end and the reconfigurable ADC.



(a) (b)

Figure 5.11 Two bonding options for measuring (a) the phased-array and the standalone front-end structure and (b) the ADC test structure.

5.4.3 *Bonding Diagram*

To accommodate for different testing requirements, there are two bonding options, as shown in Figure 5.11. Figure 5.11(a) is used for phased-array measurements so the East of the chip is left clean for high-frequency probing. Figure 5.11(b) shows the bonding for testing the ADC structure where the bondings to the left are the connections to the different inputs and the clock of the ADC.

5.4.4 *Measurement Setup*

The mm-Wave front-end will be measured using a standalone structure on the same chip. An Agilent N5247A Network Analyzer (PNA) with OML E-band frequency extension module was used to perform S-parameter measurements. Figure 5.12 shows the measurement setup for the standalone receiver. For gain, noise, and linearity measurements, PNA Port 1 was used as input signal where the source power was first calibrated with Agilent N1913A Power Meter, while Port 3 was used as an external LO source. The NF was measured using the gain method with a Mini-Circuits Amplifier inserted between the DUT baseband output and Agilent N9010A Spectrum Analyzer to increase measurement accuracy by raising the output noise floor of the DUT.

The setup for the 2x2 phased-array measurement is shown in Figure 5.13. The Tektronix AWG7000A-150 arbitrary waveform generator (AWG) will be used to generate a modulated data pattern to an IF frequency of 6GHz. The uniform phase difference between the four RX inputs will be generated through two 2-channel Colby Instrument programmable delay lines, to emulate different delays of an incident angle of an incoming signal. The four IF modulated signals were then up-converted by a SAGE Millimeter E-band Mixers. The mixers were driven by an Agilent E8254A Signal Generator as LO with an external PA (SAGE Millimeter). A custom GGB probe will be used to provide the 4 signals for each of the 4 RX inputs from the East of the chip, see Figure 5.11(a). The modulated signals will be down-converted by the DUT and digitized by the

on-chip ADCs. The digitized signal will be then sent to the digital back-end for beamforming and demodulation or to the memory for post-processing using a computer.

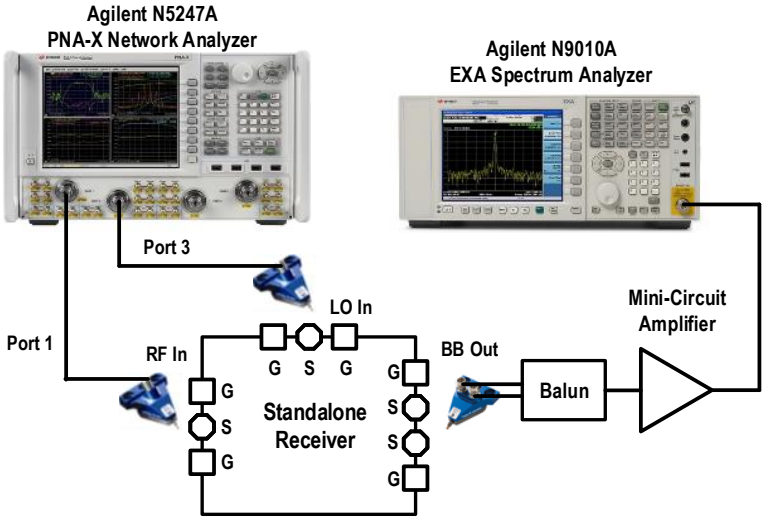


Figure 5.12 Measurement setup for the standalone mm-Wave front-end.

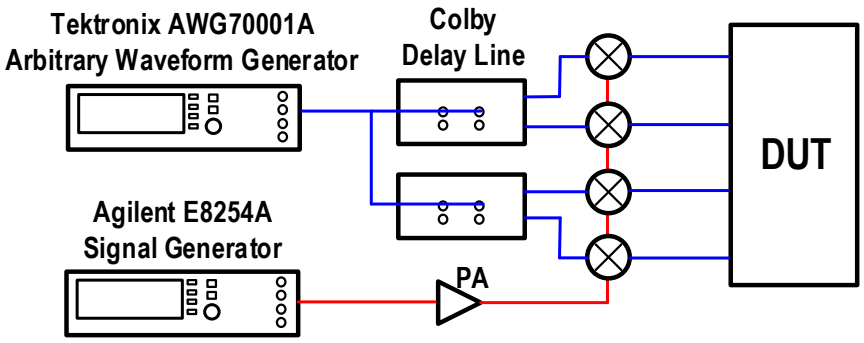


Figure 5.13 Modulated measurement setup for the phased-array receiver.

5.5 Expected Performance

Based-on simulations, the expected receiver front-end performance and the comparison to prior art are summarized in Table 5.2.

5.6 CONCLUSION

This chapter describes the first prototype of the proposed novel highly-digital element phased-array receiver implemented in TSMC 28-nm CMOS. This work contains several techniques, including a feedforward noise-suppressing front-end, reconfigurable 0-3 SMASH CT-ΔΣ ADC, and digital beamformer. This proposed receiver enables the development of digital multi-beam phased-array with improved front-end NF, reduced silicon area, and low power consumption for the future wireless systems.

Table 5.2 Comparison to mm-Wave Phased-Array Receiver

		[11]	[5]	[13]	[12]	**This Work**
Technology		28nm	22nm FinFET	65nm	28nm	**28nm**
Topology	**Single RX**	Sliding-IF	Direct Conv.	Direct Conv. Mixer-first	Direct Conv. Mixer-first	**Direct Conv. FF Mixer-first**
	Phased Array	-	BB Beamformer	-	-	**Digital Beamformer**
Matching Network		Transformer	Transformer	Low-pass π	Shunt LC + L	**Shunt L**
V_{DD} (V)		0.9	1	1.2	1	**0.95**
Freq. Range (GHz)		61-89[e]	71-76 [e]	49-67[f]	70-100[f]	**45-70[f]**
RF fBW (%)		36.7	6.8	31	35.3	**40**
BB BW (GHz)		-	2[b]	0.32	1.8	**1.2[b]**
Single RX Gain (dB)		30.8	36.7	13	25.3	**32**
Single NF (dB)		7.3	6[g]	11	8	**6.4**
Input P1dB (dBm)		-30.7	-28[d]	-12	-16.8	**-14**
Power (mW)	**Receiver Core**	57	-	14	12	**24[c]**
	Single Element	-	168	-	-	**33**
Active Area Single RX (mm^2)		0.675	0.6[a]	0.39[a]	0.085	**0.044**

[a] Estimated from die photo, without pads. [b] I+jQ bandwidth. [c] The power of buffer driving off-chip is not included. [d] Calculated from reported IP_3. [e] Frequency range based on gain response. [f] Frequency range based on S_{11} response. [g] Including T/R SW loss.

Chapter 6. V-BAND 2/4-WAY POWER-COMBINING POWER AMPLIFIER

With the introduction of 60GHz, 5th-generation (5G) communications, and radar systems for autonomous driving, the demand for highly-integrated millimeter-wave (mm-wave) wireless front-ends has intensified with an emphasis on reducing the form factor and cost. Mm-wave bands provide expanded bandwidth (BW) of several gigahertz for various wireless applications to operate at increased data rates. As the feature size of CMOS technologies continue to scale to allow high-speed operation and high-level system integration, major challenges exist for the development of wireless radio system-on-chips (SoCs). One such challenge is achieving high efficiency PA designs with wide BW and high output power. Although a number of mm-wave CMOS PAs [30]–[55] and SiGe PAs [56]–[58] have been published, only a few of these publications were implemented in a FinFET (FF) CMOS technology [32], [33], which is a prime candidate technology to implement next-generation mm-wave SoCs.

Though challenges of mm-wave design in a FF process have previously been discussed in [59], [60], some of the considerations are worth mentioning here which can be applied to achieve an improved PA efficiency. Self-heating is a well-known concern in FinFET due to the confined geometry which makes the heat dissipation through substrate difficult [59]. As a result, FinFET transistors are usually biased at a lower current density that leads to a lower gain. Secondly, the high parasitic capacitances contributed by the 3D FinFET gate and deeply scaled interconnect can limit the device f_t and f_{max} as well as increase the effective input/output quality factor of the devices if careful layout optimization is not followed [30]. These challenges limit attainable gain per unit current, and thus limit attainable PA efficiency. To combat this, the capacitively-neutralized differential pair is commonly used to boost G_{max} by 4-5dB [61]. Another challenge that is not

specific to FinFET, but plagues non-SOI processes in general, is the limited output power from a single-stage. FinFET has similar limits to device stacking as bulk CMOS which thereby limits the max output power that can be generated reliably. To circumvent this, power combining is often employed to increase transmit power.

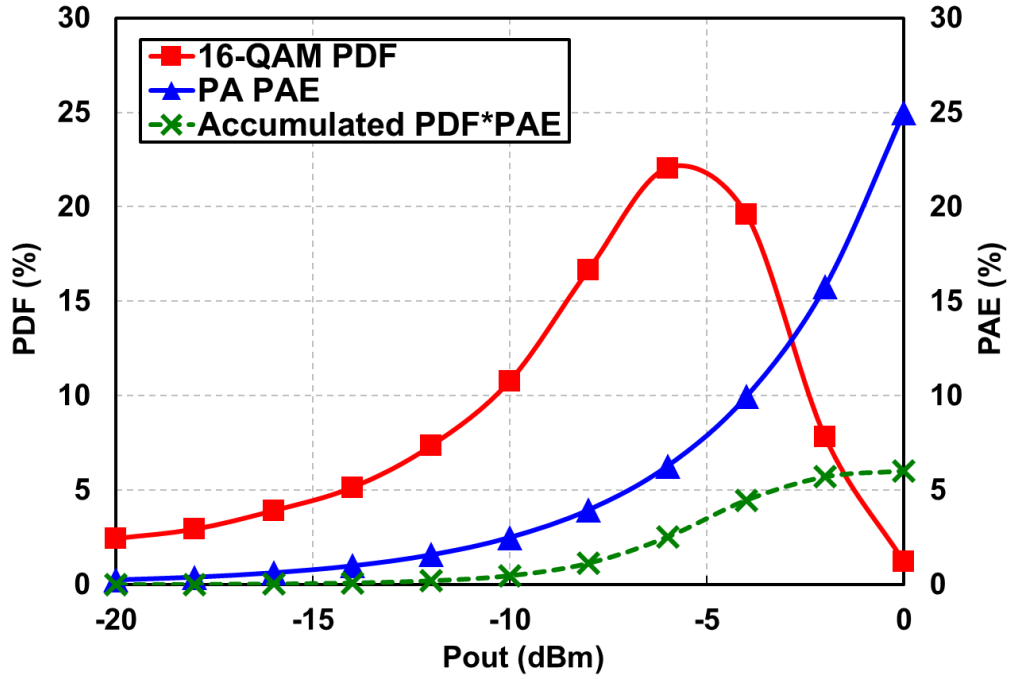


Figure 6.1. Conceptual diagram illustrating PA average efficiency. 16-QAM PDF and PA PAE curves are depicted as functions of normalized PA P_{out}.

The efficiency of PAs plays an important role for improving battery lifetime as PAs often consume the majority of power in radio transceivers. However, the average efficiency of the PA is usually significantly lower than its peak efficiency due to the characteristics of the data-modulated signal. As the demand for high data rate grows, spectrally efficient modulation methods are desired. Unfortunately, these modulation schemes exhibit high peak-to-average power ratio (PAPR), thereby degrading PA average efficiency. As an example, the probability density function (PDF) of a 16-QAM modulation as a function of normalized PA P_{out} is shown in Figure 6.1 along with the power added efficiency (PAE) of a typical class-A PA. The average PAE is the sum of

the product of the PDF and PAE. As shown in the figure, the PA rarely operates in the peak PAE region and most often operates in the lower PAE region which leads to an average PAE much lower than its peak PAE. In this example, though the peak PAE is 25%, the average PAE is only 6%. As a result, several techniques have been proposed to enhance efficiency at power back-off (PBO) in order to improve the average PA efficiency.

One such effective and popular technique is the Doherty PA. Doherty PAs show impressive back-off efficiencies, with one implementation at 60GHz exhibiting a peak PAE of 26% with an enhanced PAE of 16.6% at 7-dB PBO [30]. However, the large footprint associated with Doherty PAs complicates SoC integration. In addition, Doherty PAs suffer from narrow BW imposed by the $\lambda/4$ impedance rotation on the auxiliary path. Furthermore, as next-generation systems are likely to utilize several mm-wave bands from 28 to 90GHz, a wideband PA will be desirable in order to reduce the number of required front-end modules for multi-band operation and thus lower system cost. While some wideband mm-wave PAs have been demonstrated [2][3], their back-off efficiencies typically drop by more than half at PBOs greater than 3dB. As a result, it is of interest to develop compact, wideband, high-output-power PAs in deeply-scaled FinFET CMOS with enhanced efficiency at PBO.

This work presents a wideband reconfigurable 2/4-way power-combining PA with compact form factor implemented in 16-nm FinFET CMOS [62]. The PA can be configured in two discrete output power modes: full-power mode (FPM) and back-off power mode (BPM). The PA applies a load modulation technique similar to [63] for efficiency enhancement in BPM but is further improved by utilizing a proposed non-uniform power combiner. Moreover, a load modulation switching scheme is proposed which minimizes the variation in frequency response between the two modes and improves performance in BPM.

It should be noted that while the presented PA achieves both wide bandwidth and efficiency enhancement at PBO in a compact area, the efficiency enhancement is *static* in nature as indicated by the two discrete modes of operation. In contrast, a Doherty PA dynamically provides efficiency enhancement (i.e. no explicit reconfiguration required) and is well-suited for high-PAPR modulations with low-to-moderate BW requirements. Nonetheless, there are several applications that still benefit from discrete power control while maintaining wide bandwidth and high efficiency (e.g. power-control loops in communication links).

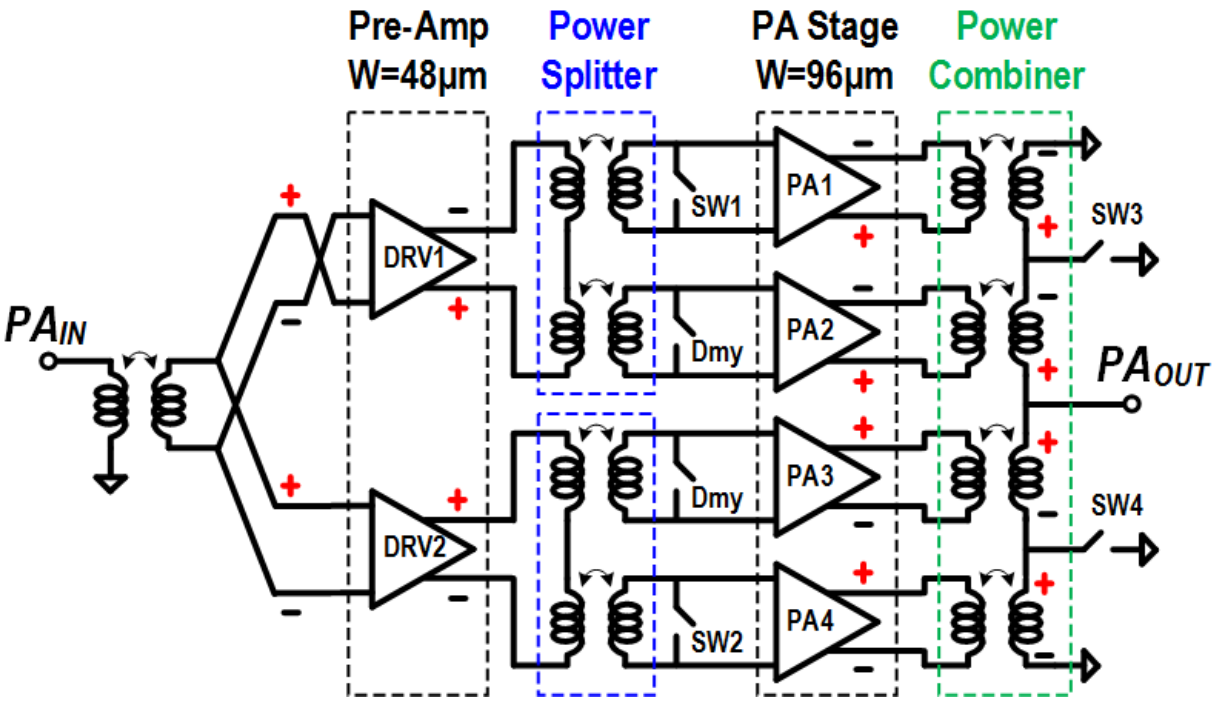


Figure 6.2. The 2-stage PA architecture with a reconfigurable 2/4-way series-parallel power combiner. Polarities of the gain stages are shown.

6.1 2/4-Way Power-Combining PA Architecture

Figure 6.2 depicts the PA topology. It is composed of two gain stages, an input matching transformer, two interstage power splitters, and a reconfigurable 2/4-way series-parallel power combiner at the output. In FPM, all gain stages are ON with SW1-4 open, thereby placing the PA

in its highest P_{out} mode. In BPM, DRV1-2 and PA2-3 are ON, while PA1 and PA4 are OFF and SW1-4 are closed. In this configuration, the PA output stage becomes a parallel 2-to-1 combiner and ideally operates at 6-dB PBO as compared to FPM, assuming uniform power combining (i.e. all transformers have *identical* turns ratios). Figure 6.3 shows simulations of some large-signal performance with extracted differential pairs under different current densities. The output stage (PA1-4) is biased at 125µA/µm (class-AB) for a better efficiency at PBO [33].

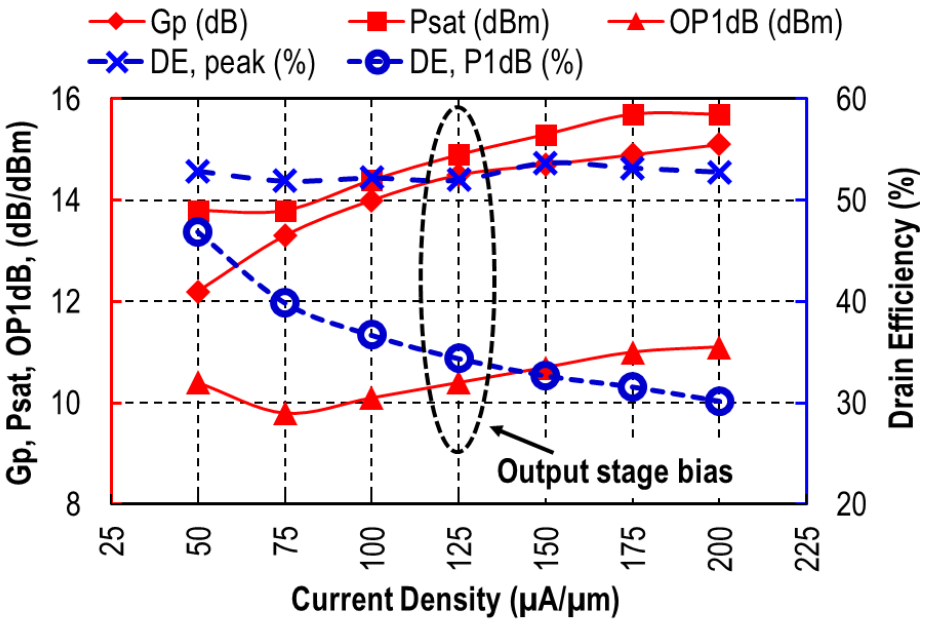


Figure 6.3. Large-signal performance of extracted NMOS pairs vs. bias condition with different current density.

6.1.1 *PA Core*

Figure 6.4 shows the detailed transistor-level schematic for the bottom-half of the PA. Capacitively-neutralized differential pairs are employed in all gain stages for an increased G_{max} [61]. The capacitances are obtained by overlapping drain and gate routing in layout, similar to [33]. The driver stages are biased in class-A region for higher gain while the PA stages are biased in class-AB region with a current density of 125µA/µm for better efficiency at PBO [3][7]. A

common-mode (CM) source degeneration inductor of 145pH is placed in the driver stage for better common-mode stability and common-mode rejection, as the driver stage contributes to the majority of gain and is more susceptible to oscillation.

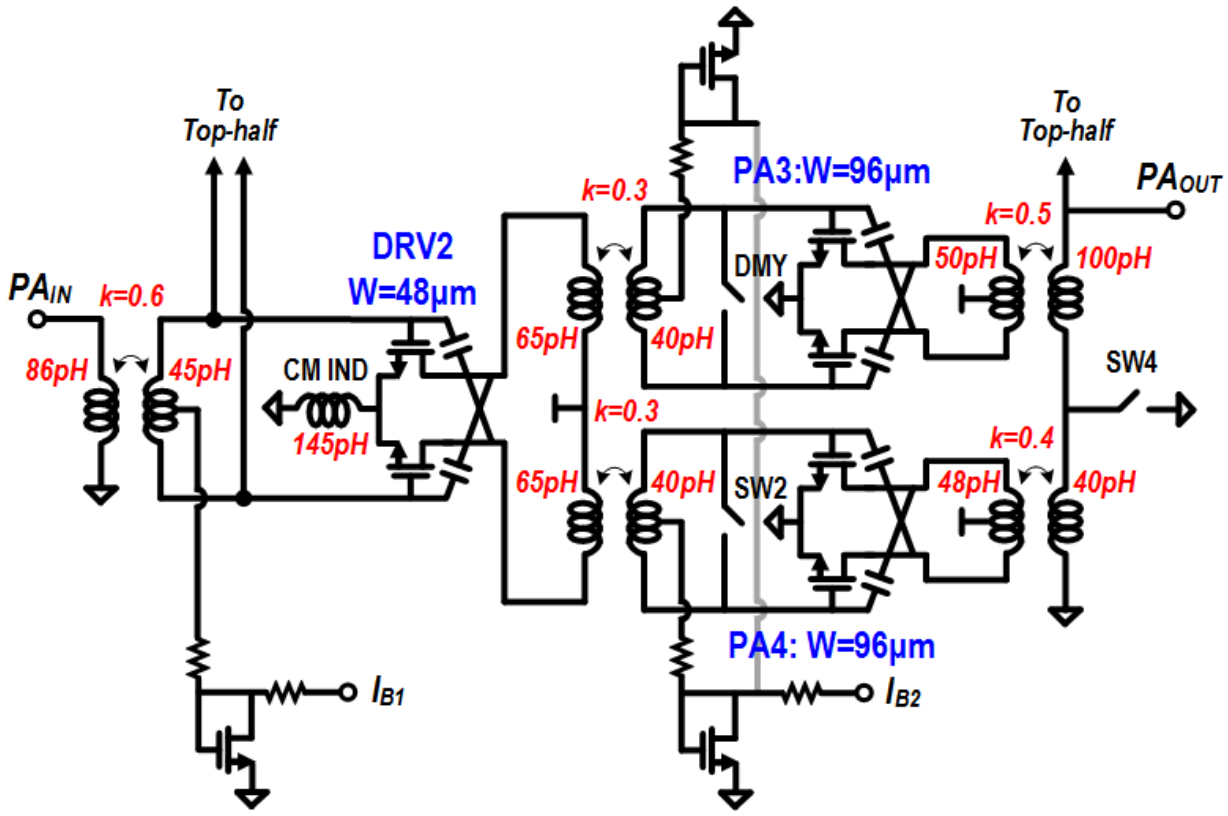


Figure 6.4. Detailed transistor-level schematic for the bottom-half of the PA.

6.1.2 *Input Matching and Interstage Power Splitter*

The input matching network uses a high-k (k=0.6) transformer for minimal loss while low-k (k=0.3) transformers are used for the interstage power splitters to enhance the bandwidth [10]. Series power splitting is utilized for two reasons. First, the resulting transformer *inductance ratio* (1.6:1) is much lower than that of a parallel splitter (6.5:1) [31], thereby resulting in lower transformer insertion loss [65]. Secondly, series power splitting enables the use of shunt switches at the front of PA1 and PA4 to disable these paths in BPM (SW1-2 in Figure 6.2). In contrast, a parallel power splitter would require a large OFF impedance from PA1 and PA4, which is

challenging to achieve at mm-wave frequencies due to large input capacitance associated with the PA devices. As such, the shunt switch in a series splitter leads to reduced loading of the OFF paths in BPM (PA1 and PA4). Note that adding a switch to reduce the signal swing at the disabled PA input is necessary. This is because the swing accumulated (or the V_{rms}) at the gate of disabled PA might partially turn on the PA and degrade the overall efficiency.

6.1.3 *Output Matching Network and Power Combiner*

The transformer-based output matching network is designed using a holistic optimization approach to improve PA efficiency by performing active/passive device co-design [32]. The reconfigurable 2/4-way series-parallel power combiner applies a non-uniform turns ratio to further improve the performance which will be described in the next section

6.2 NON-UNIFORM POWER COMBINING AND SWITCHING

Power combining is a commonly used technique for increasing PA output power in deep sub-micron CMOS process with limited voltage supply. As described in [63], the combiner can also be designed to properly adjust the load presented to the PA, thus improving the PA efficiency at PBO. This technique is commonly referred to as load modulation. The following subsections discuss the techniques used in the power combiner design in this work to improve performance when configured in BPM with minimal impact to FPM performance.

6.2.1 *Non-Uniform Power Combining*

The PA employs a reconfigurable 2/4-way series-parallel power combiner to perform load modulation with non-uniform turns ratios for the transformers presented at the load of each PA driver. Applying a non-uniform turns ratio improves the PA performance in BPM by reducing the

change in PA load impedance that occurs when switching between the two modes. Figure 6.5 (a) shows the conceptual diagram of a non-uniform power combiner with the 50-Ω antenna load modeled as two 100-Ω resistors in parallel. Here, the characteristic of *non-uniform* is identified as the different turns ratios used in each pair of transformers that make up the half-circuit of the combiner. As shown in Figure 6.5 (a), the non-uniform turns ratios of transformers for PA1, PA2, PA3, and PA4 are 1:1, 1:$\sqrt{2}$, 1:$\sqrt{2}$, and 1:1, respectively. Figure 6.5 (b) shows the configuration of the combiner in FPM. When all the paths are ON, the voltages across each transformers' secondaries are V_{in}, $\sqrt{2}V_{in}$, $\sqrt{2}V_{in}$, and V_{in}, respectively, assuming each PA outputs the same V_{in}. Moreover, the currents flowing through each transformer's secondary are equal. As a result, each of the 100-Ω terminations are distributed as 59-Ω and 41-Ω impedances across the secondaries of the transformers of PA2/PA3 and PA1/PA4, respectively. These impedances are then transformed, via the respective turns ratios, to 29-Ω and 41-Ω loads which are presented to each PA core. In BPM, PA2 and PA3 will see a load impedance of 50Ω as shown in Figure 6.5 (c), where PA1 and PA4 are OFF and SW3 and SW4 are ON.

By contrast, with the conventional uniform power combining where the turns ratio is 1:1 for all transformers (i.e. identical transformer turns ratios in the combiner), the impedance presented to each PA is 50Ω/100Ω in FPM/BPM. Now, assuming the impedance presented to the PA in FPM is its optimal load, r_{opt}, this impedance should also be presented to PA2 and PA3 in BPM as well for optimal performance. Therefore, by applying non-uniform power combining, the impedance change between FPM and BPM is reduced to 1.72x (29Ω:50Ω), as compared to 2x (50Ω:100Ω) in uniform combining, and improves the output power and efficiency in BPM.

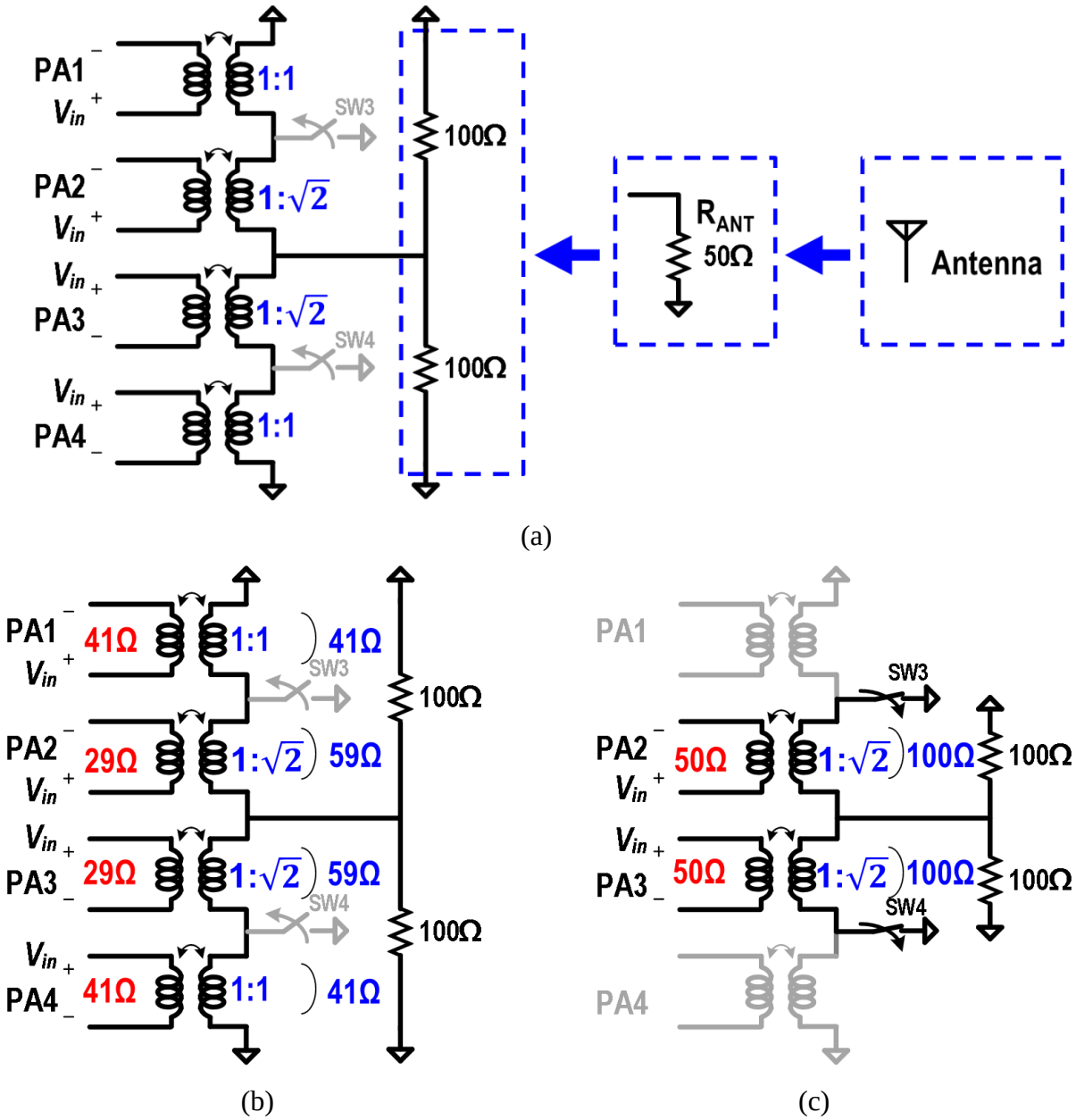


Figure 6.5. Conceptual diagram of non-uniform power combining. (a) The combiner model. The impedances seen from each PA stage in (b) FPM and (c) BPM.

Note that the impedance change between FPM and BPM can be further minimized by choosing a more aggressive non-uniform combining turns ratios. For instance, the turns ratios of 1:1, 1:$\sqrt{3}$, 1:$\sqrt{3}$, and 1:1 can reduce the impedance mismatch to 1.57x (21Ω:33Ω), thereby improving the P_{sat} and PAE in BPM further. However, implementing a turns ratio of 1:$\sqrt{3}$ (or 1:3

inductance ratio) is challenging and exhibits higher loss at mm-wave frequencies [65].

Lastly, it is worth noting that the back-off efficiency can also be improved by reducing the drive strength of each PA while simultaneously adjusting the PA load line [34]. The PA published in [34] is segmented into a few PA cells and capable of adjusting the PA load line to accommodate the impedance at PBO. In this scenario, an *increase* in the impedance presented to the PA for BPM is desirable so that the PA can utilize the full voltage swing in BPM and which is why a uniform combiner was adequate for previous designs such as [5]. However, the PA design in [34] is a digital PA. Applying the same technique to linear PAs would require the insertion of a tail switch device into the PA unit cell which has implications on performance. Simulations show that although insertion of such a switch device would not significantly affect P_{sat} and linearity, the PAE would degrade by approximately 5% points. As a result, instead of adjusting the PA load line by using a tail switch, the load line of each PA device in this design remains constant between FPM and BPM and the passive combiner is reconfigured to reduce the impedance difference between the two modes.

6.2.2 *Comparison of Non-Uniform and Uniform Power Combining*

This section compares non-uniform and uniform power combining by presenting transistor-level simulation results. As shown in Figure 6.6, we will only consider the bottom-half PA and an ideal switch for simplicity. Figure 6.6 (a) shows the schematic for the uniform power combining which is comprised of two PAs (PA3 and PA4), an ideal switch, and a 2-way series power combiner with uniform turns ratios of 1:1.2 for both transformers. The quality factor of the inductors (Q=15) and coupling factor of the transformers (k=0.65) are applied to emulate the passive loss of the combiner. Since it is the half-circuit of the series-parallel combiner, the load presented to the bottom-half PA is now a 100-Ω resistor in parallel with a 12-fF pad parasitic.

Figure 6.6 (b) shows the schematic for non-uniform power combining which is the same as Figure 6.6 (a) except that the transformer turns ratios for PA3 and PA4 are 1:$\sqrt{2}$ and 1:1, respectively.

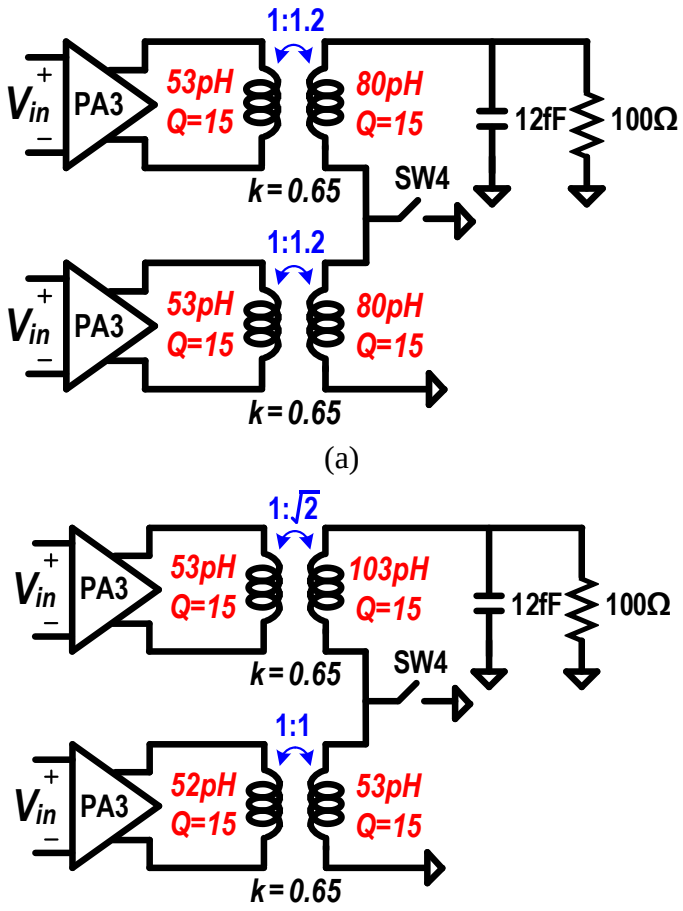


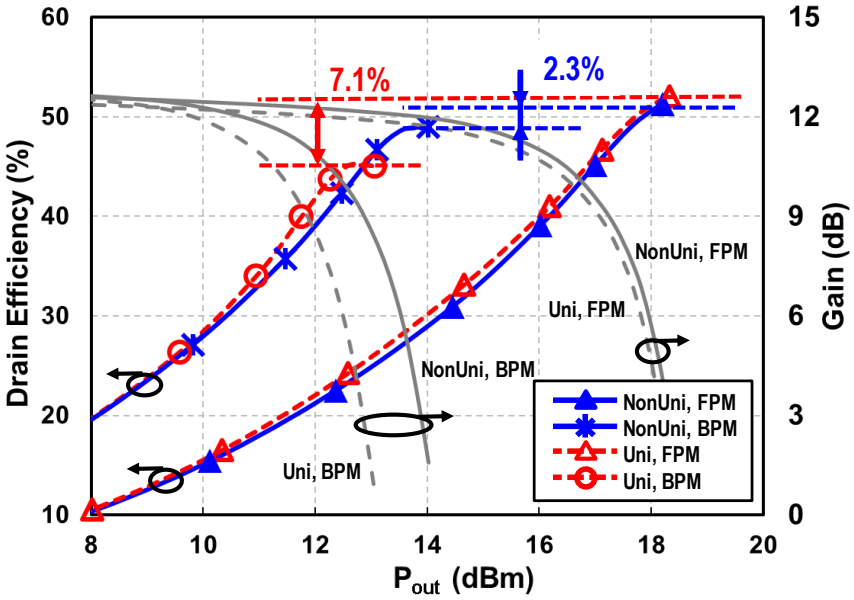
Figure 6.6. Simplified half-circuit schematic with a 2-way series combiner for comparison between (a) uniform and (b) non-uniform power combining.

Figure 6.7 (a) plots the drain efficiency (DE) versus P_{out} for uniform and non-uniform combiners in both FPM and BPM. For uniform power combining, the simulated DE drops by 7.1% points (52.1% to 45%) when switching from FPM to BPM. This is expected as the impedance presented to PA3 is increased and shifted from the r_{opt} of the PA, as discussed in the previous section. By contrast, the simulated DE of non-uniform power combining shows a difference of only 2.3-% points (51.3% to 49%) between the two modes.

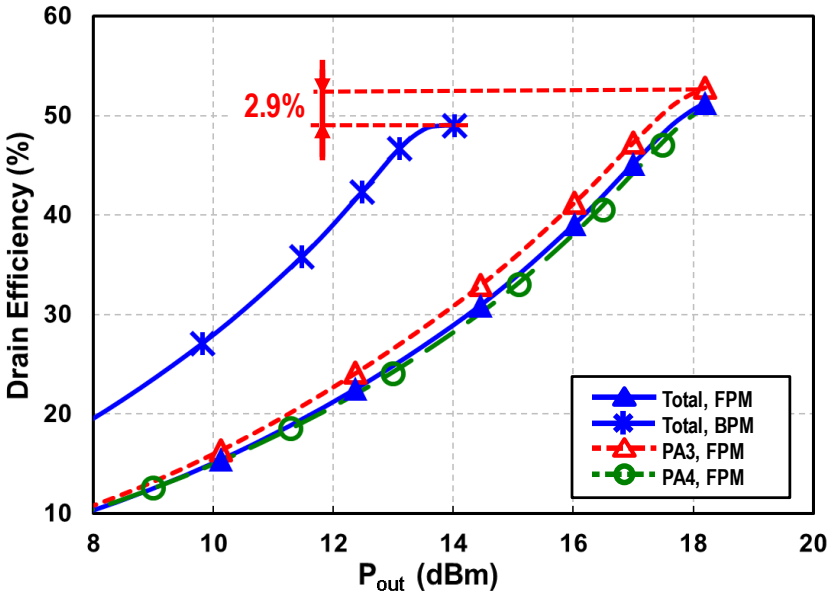
We can further break down the drain efficiency of each PA in the non-uniform combining case. As shown in Figure 6.7 (b), the PA3 and PA4 contribute slightly different DEs to the total DE of 51.3% in FPM where the peak DEs for PA3 and PA4 are ~52.8% and ~50.8%, respectively. This is also expected since the impedances presented to PA3 and PA4 are different (Figure 6.6b). Note that the DEs for PA3 and PA4 are the same in uniform power combining.

The efficiency difference between FPM and BPM is mainly contributed by the PA3 as it is always ON but is presented with different impedances in the two modes. By applying non-uniform power combining, the simulated DE degradation of PA3 between two modes can be improved from 7.1% points to 2.9% points, see Figure 6.7 (a) and Figure 6.7 (b), respectively.

To provide another view of how non-uniform power combining improves the efficiency, Figure 6.8 (a) plots the simulated load-pull of DEs for uniform output combining using the half-circuit schematic depicted in Figure 6.8 (a). The peak DE occurs at a real 100Ω in FPM since the included combiner network should transform the 100-Ω resistance and present r_{opt} to both PA3 and PA4. In BPM, as the impedance presented to the PA3 (Figure 6.6a) is now 2x of r_{opt}, the peak DE can be obtained at a real 50Ω, which is half of 100Ω. With the load impedance fixed at 100Ω in the two modes, the DEs in FPM and BPM are 52% and 45%, respectively, based on the contours shown in Figure 6.8 (a). These results agree with Figure 6.7 (a). In contrast, Figure 6.8 (b) presents the load-pull contours with non-uniform combining as shown in Figure 6.7 (b). The peak DE in FPM still occurs at a real 100Ω but the peak DE in BPM is now closer to 100Ω. With a fixed 100-Ω load, the DE of 51.3% in FPM and an improved DE of 49% in BPM are obtained.

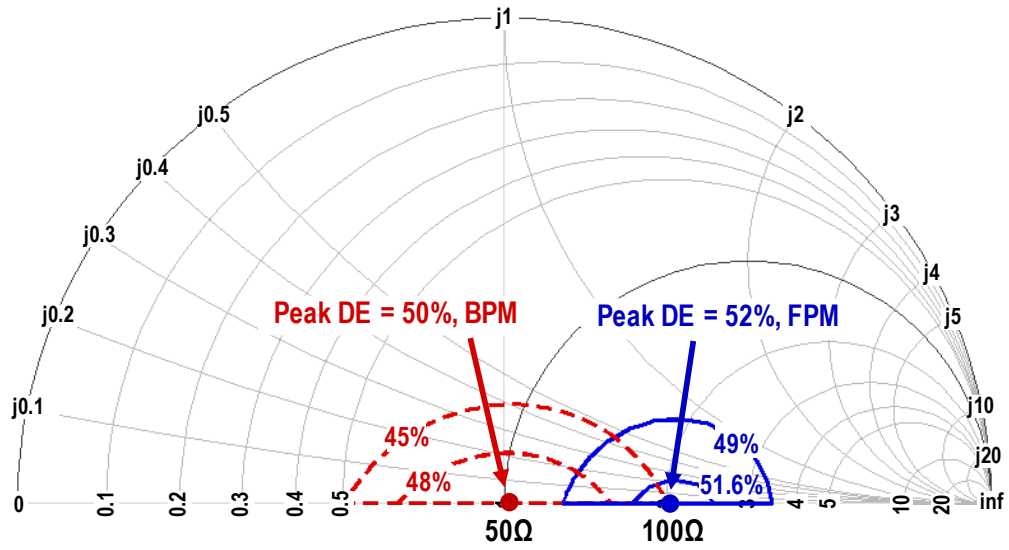


(a)

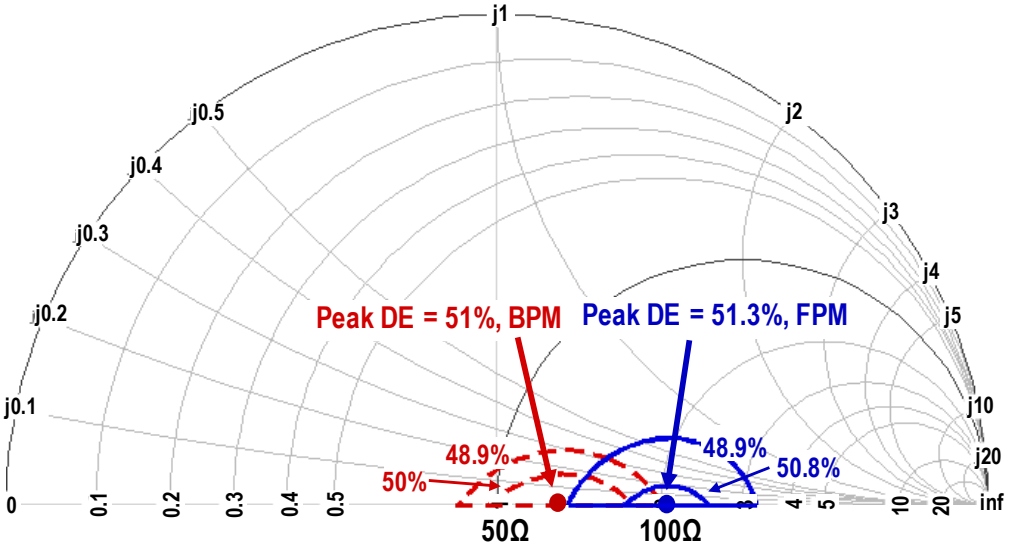


(b)

Figure 6.7. Large-signal simulation results. (a) Drain efficiency (and gain) comparison between non-uniform and uniform power combining in FPM and BPM. (b) Further breakdown in drain efficiency for non-uniform power combining.



(a)



(b)

Figure 6.8. Load-pull simulations of drain efficiency show how r_{opt} shifts between two modes for (a) uniform and (b) non-uniform power combining.

Note that the purpose of this *simplified* example is to illustrate how non-uniform power combining reduces the change in load impedance presented to the PA output stage (PA1-4 in Figure 6.2) between the two modes. The change in peak efficiency between FPM and BPM will be larger in the final design than what is shown in Fig. 6 due to several non-idealities associated with practical implementations (e.g. loss introduced by switch on combiner secondary side in

BPM, non-ideal short of PA1 and PA4 inputs in BPM results in power loss, etc.).

6.2.3 *Proposed Switching Scheme*

The proposed load modulation is implemented by placing the switch at the transformer's secondary side to eliminate both the coupling and leakage inductances for the OFF path of the combiner. To understand the switching scheme of the power combiner, we will focus on the bottom half of the combiner as shown in Figure 6.9 (a) which is composed of two transformers and a switch. The simplified transformer model uses an ideal 1-to-n transformer, coupling inductance kL, and leakage inductance $(1\text{-}k)L$ [66]. Looking at Fig. 8 (b) where an ideal switch is placed at the secondary side, both the coupling inductance, kL_2, and the leakage inductance, $(1\text{-}k)L_2$ will be shorted to ground. In contrast, Figure 6.9 (c) shows a technique commonly used to implement load modulation which places a shunt switch at the outputs of the PAs (transformer's primary side). In this configuration, the switch can short the kL_2 term, but not the $(1\text{-}k)L_2$ term. As a result, the leakage inductance becomes an undesired reactance in series with the secondary of the ON path to ground, thereby degrading the performance and frequency response in BPM. This effect is more severe at mm-wave frequencies where the transformer's coupling factor is usually lower and thus leakage inductance is non-negligible.

The switches are implemented using thick-oxide devices with both gate and bulk terminals biased through kΩ-order resistors, R_B and R_G, to form a high-pass response which stabilizes the switch on-resistance under a high-voltage swing, see Figure 6.9 (d). This technique is commonly used in T/R switch designs [67].

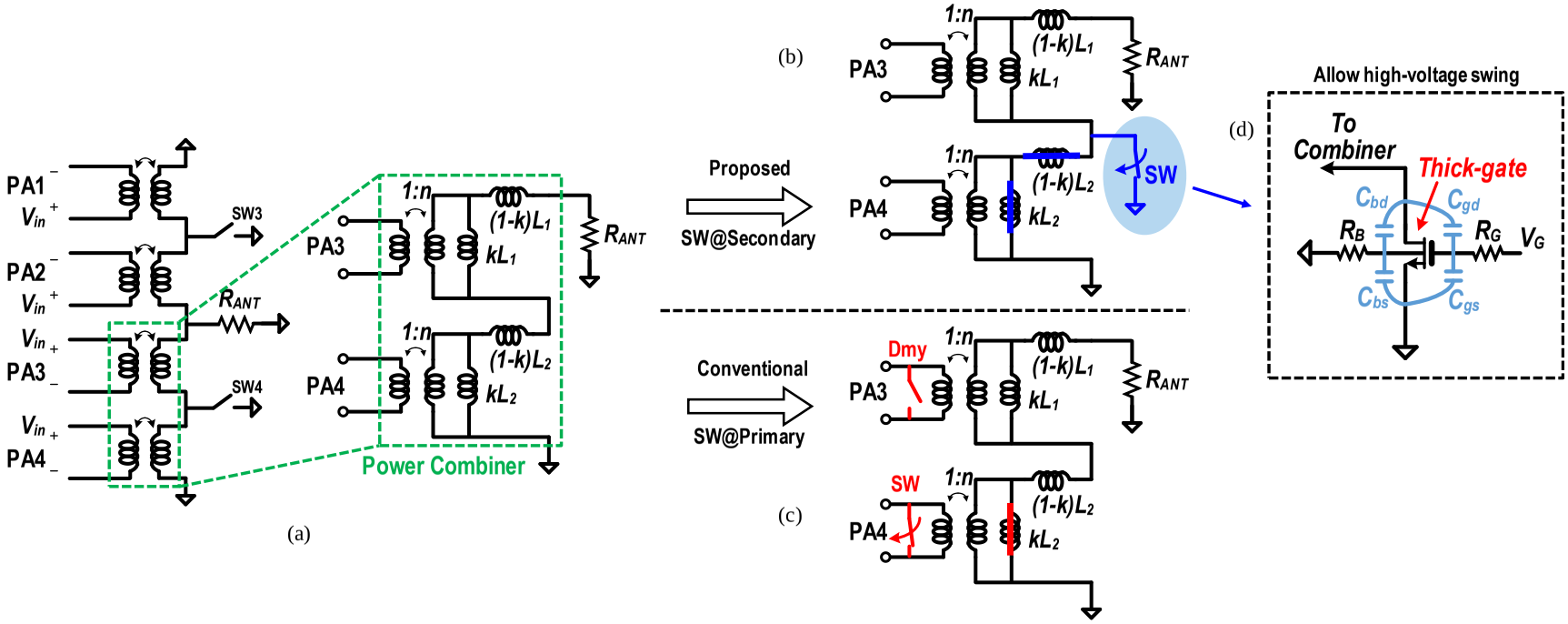


Figure 6.9. Comparison of implementing the switching scheme. (a) The power combiner model. (b) Proposed switch placement at secondary side. (c) Conventional switch placement at transformer' s primary. (d) The thick-oxide switch architecture which accommodates a high-voltage swing.

6.2.4 *Power Combiner*

Figure 6.10 shows a sketch of the proposed 2/4 way non-uniform power combiner implemented using RDL, ultra-thick metal (UTM), and 4x-thick metal (M_Z) layers of the process. The combiner occupies a drawn area of 210x50µm^2 with a drawn metal width of 3.4µm. The simulated power combiner insertion loss is 2.7/2.9dB in FPM/BPM. This loss is higher than what was reported in [62] due to estimation error in the earlier publication. Asymmetry between the differential terminals of each primary coil (e.g. primary-to-secondary capacitive coupling) can be observed in Figure 6.10 and is most pronounced for PA1/PA4. Figure 6.11 shows the magnitudes of the impedances seen from the two single-ended outputs (+ and – terminals) of PA1-4. This asymmetry causes imbalance between the single-ended impedances presented to each transistor and degrades the combiner efficiency. Efficiency can be further improved by minimizing the magnitude of this imbalance, although it was not fully optimized for this design.

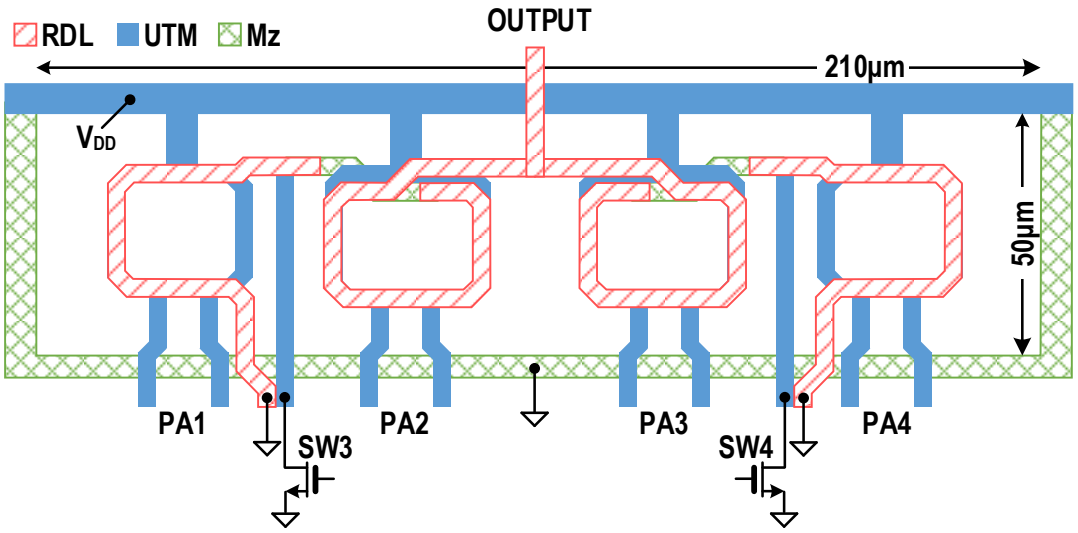


Figure 6.10. 2/4-way series-parallel power combiner with non-uniform turns ratios of (from left to right) 1:1, 1:$\sqrt{2}$, 1:$\sqrt{2}$, and 1:1.

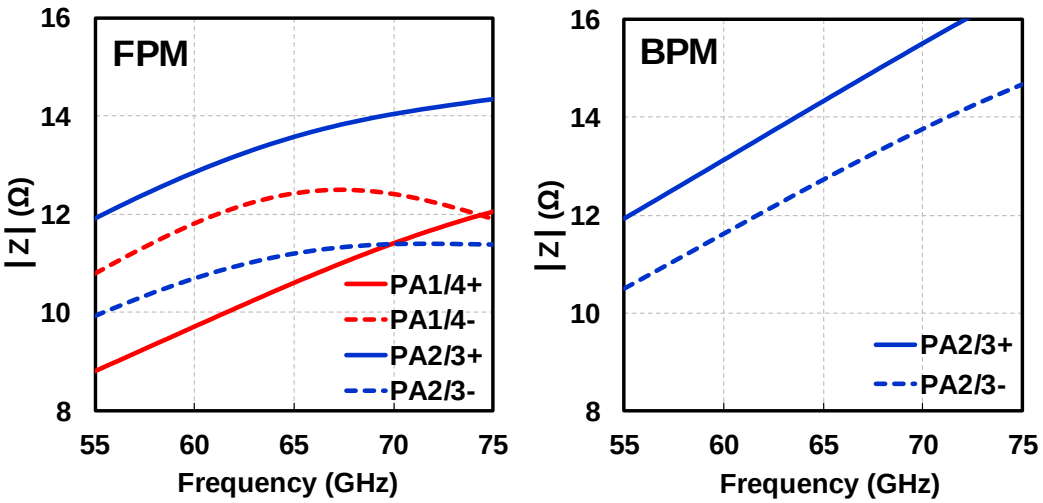


Figure 6.11. The magnitude of impedances seen from the two single-ended outputs (+/-) of PA1-4 in (a) FPM and (b) BPM.

In FPM, SW3 and SW4 are OFF and the drain terminals see the most voltage stress. The simulated instantaneous peak voltages of V_D and V_{DG} are 1.35V and 1.23V, respectively, which are well within the reliability margin for 18ud12 (1.8V underdrive to 1.2V) devices. In BPM, SW3 and SW4 are ON. The drain terminals are pulled close to ground. The peak V_D is 139mV and V_{GD} has a quiescent voltage of ~1.2V in BPM.

6.3 Experimental Results

This PA is fabricated in16-nm FinFET CMOS and operates under a 0.95-V supply. The die photo is shown in Figure 6.12. The core area of the PA is 0.107mm^2.

The measured and simulated S-parameters in FPM and BPM are shown in Figure 6.13. In FPM, the PA achieves a measured peak gain of 21.4dB at 54GHz and a 13-GHz BW (51-64GHz), see Figure 6.13 (a). In BPM (Figure 6.13b), the PA achieves a measured peak gain of 18.5dB at 55GHz and a 14-GHz BW (52-66GHz). S_{11}<-5.5dB and S_{22}<-5.2dB are achieved with S_{12} <-45dB (not shown) over the band of interest. The measured results show good agreement with the

simulations for S_{21} and S_{22} while the measured S11 null is shifted ~6GHz lower.

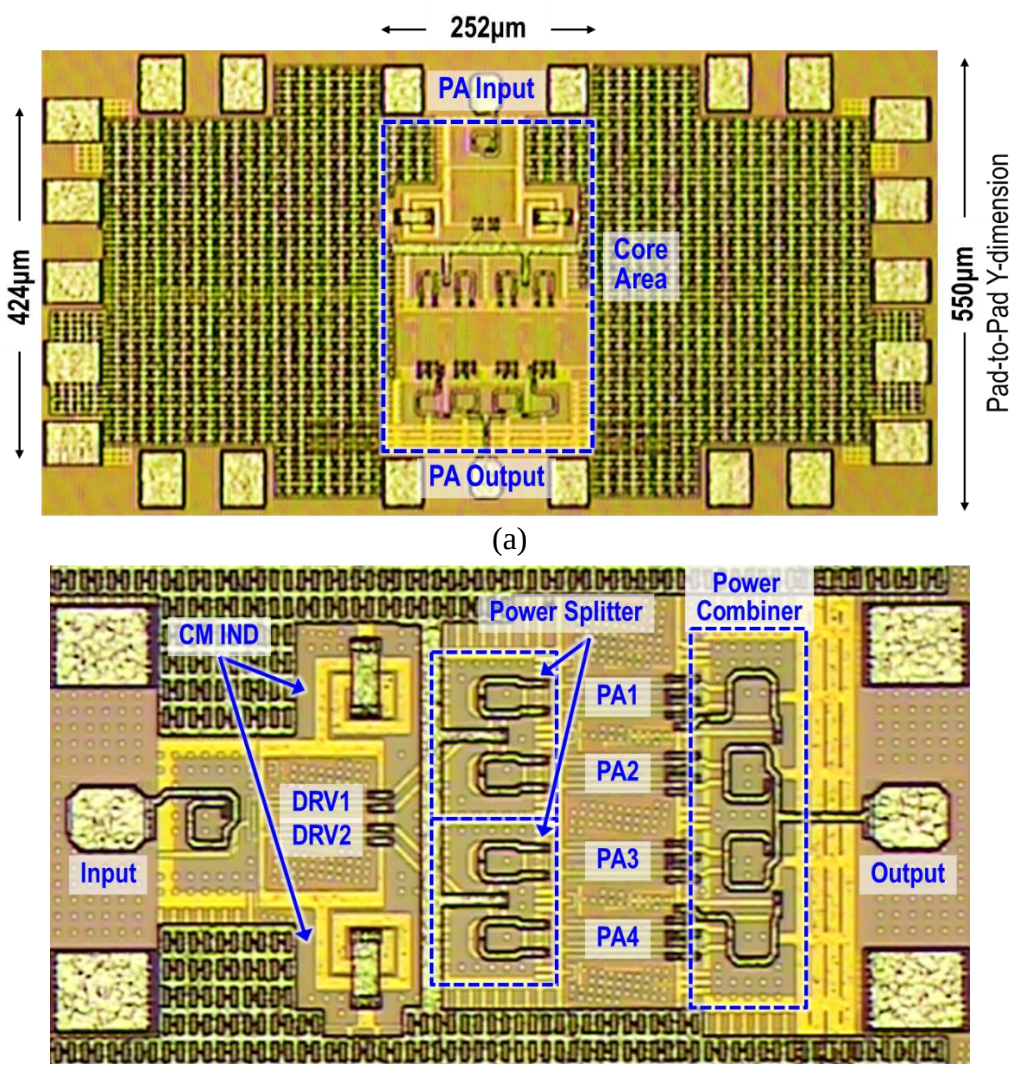
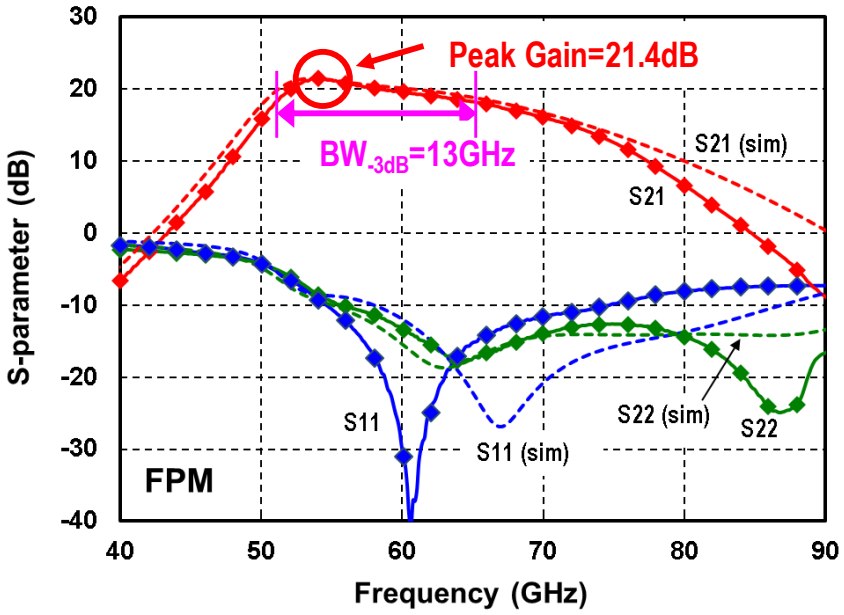
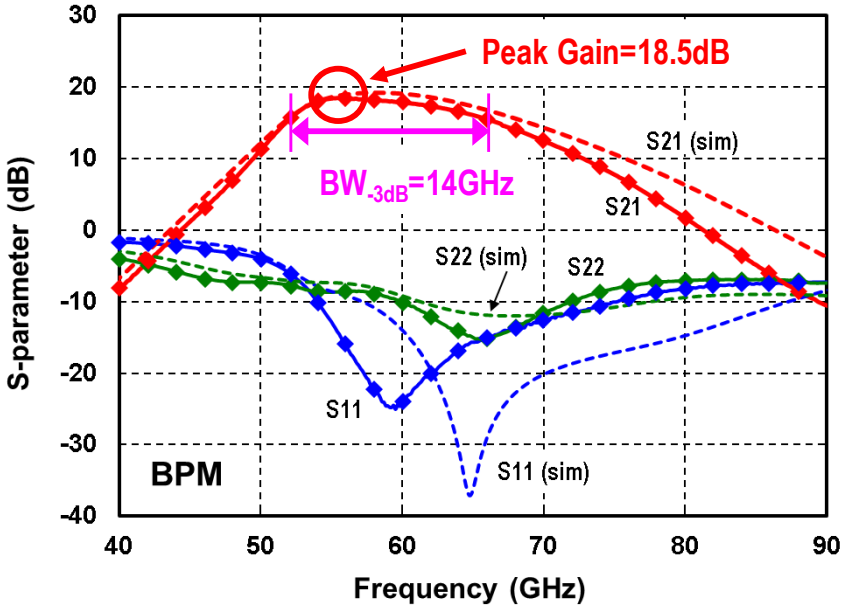


Figure 6.12. The die photos of the PA in 16-nm FinFET CMOS. (a) The PA test chip including pads. (b) Zoom-in PA core (with 90^{O} counter-clockwise rotation).

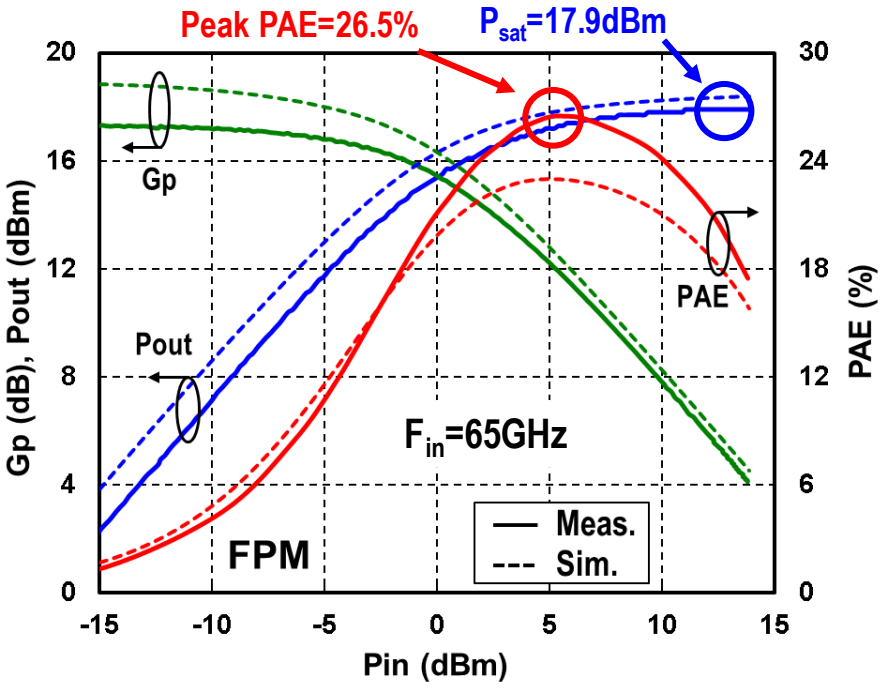


(a)

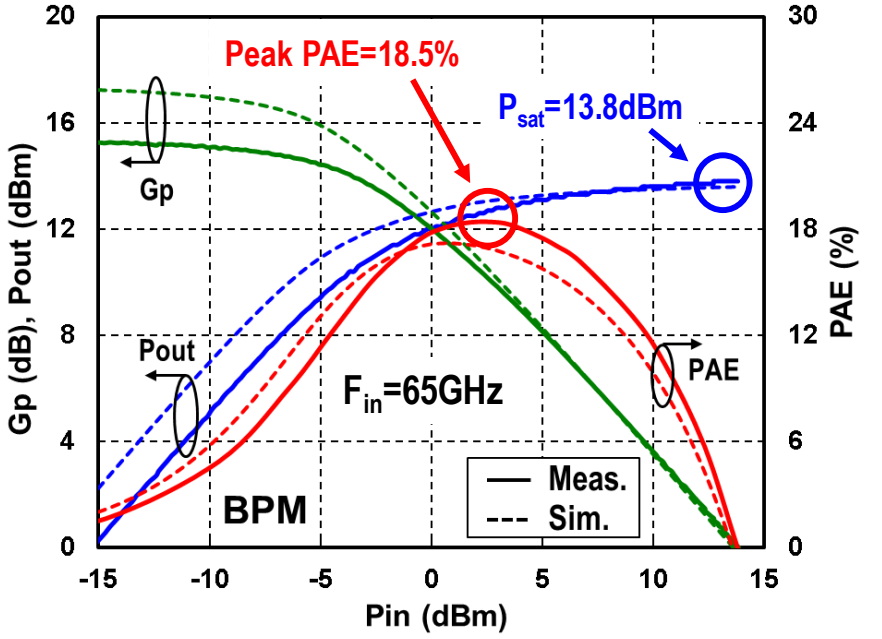


(b)

Figure 6.13. Measured vs. simulated S-parameters in (a) FPM and (b) BPM



(a)



(b)

Figure 6.14. Measured vs. simulated large-signal performance (G_p, P_{out}, and PAE) vs. P_{in} in (a) FPM and (b) BPM at 65GHz.

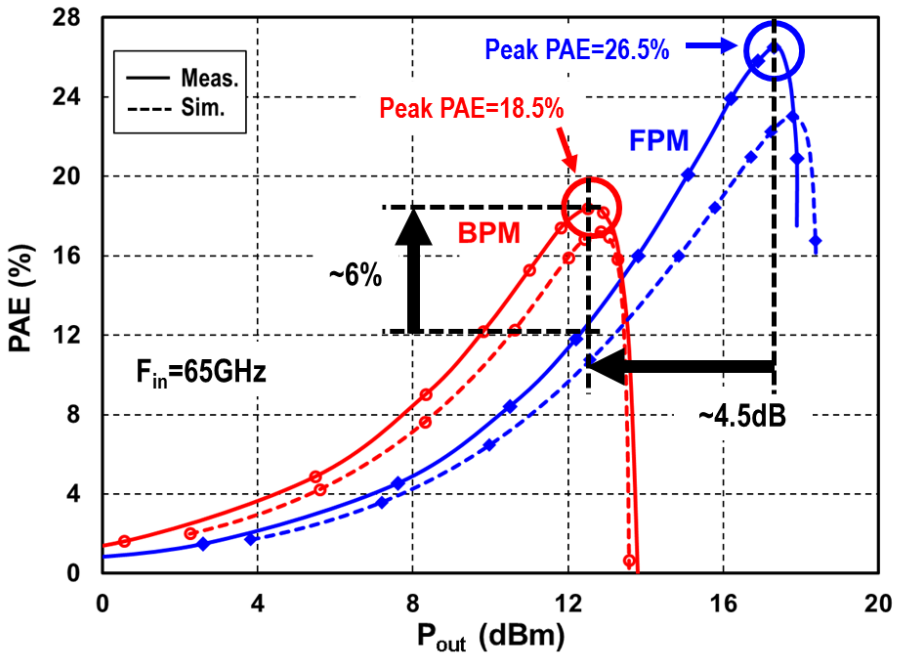


Figure 6.15. Measured vs. simulated PAE vs. Pout in FPM and BPM at 65GHz

Figure 6.14 shows the measured and simulated large-signal performance at 65GHz. In FPM, the PA delivers a Psat of +17.9dBm with a +13.5-dBm OP_{1dB} and a 26.5-% peak PAE. In BPM (Figure 6.14b), the measured P_{sat}, OP_{1dB}, and peak PAE are +13.8dBm, +9.6dBm, and 18.4%, respectively. A reasonable agreement is achieved between measurements and simulations. Note that the cascaded compression response in this two-stage PA contributes to the gap between P_{sat} and OP_{1dB}. The first stage is biased closer to class-A in order to boost gain, thereby introducing a non-negligible impact on overall linearity. Secondly, PAs 1/4 see higher load impedances than PAs 2/3 in FPM which also contributes to the soft compression of the PA.

Figure 6.15 plots the measured and simulated PAE curves vs. P_{out} at 65GHz. In FPM, the PA can deliver an output power of +12 to +18dBm with >12-% PAE. For output powers below +12dBm, the PA can be switched to BPM for an enhanced efficiency. The PAE is ~6-% higher in BPM over an output power range of +8 to +12dBm.

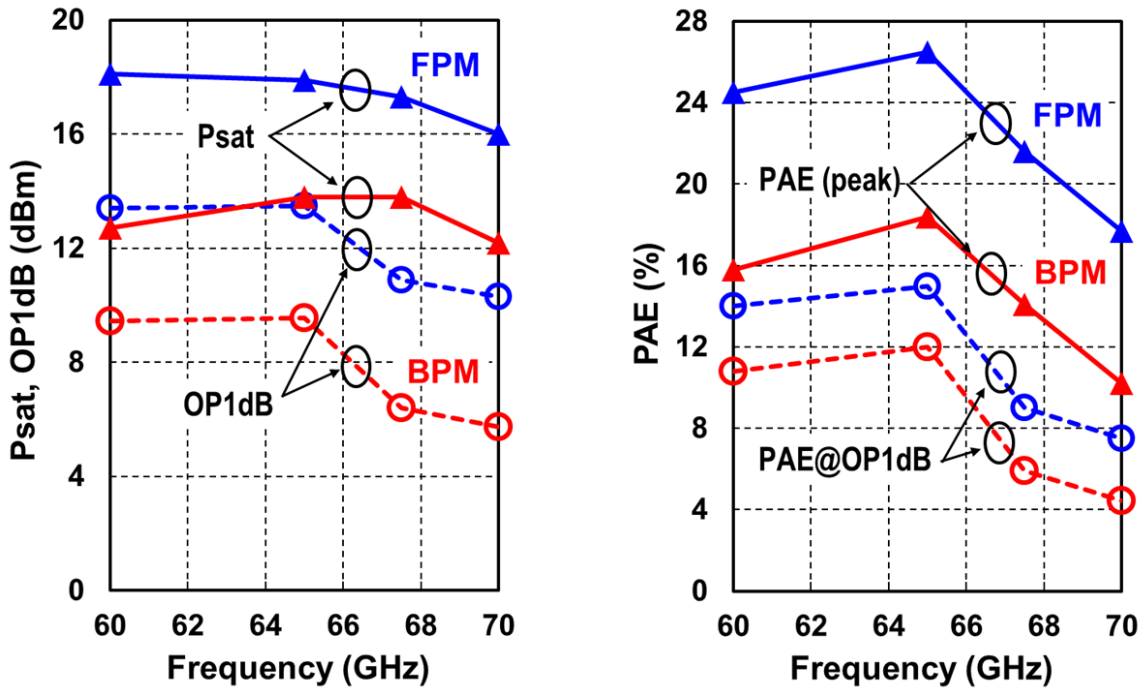
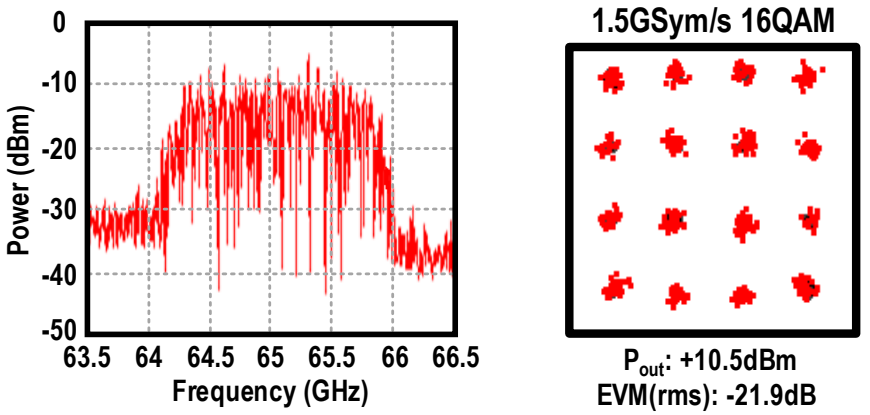
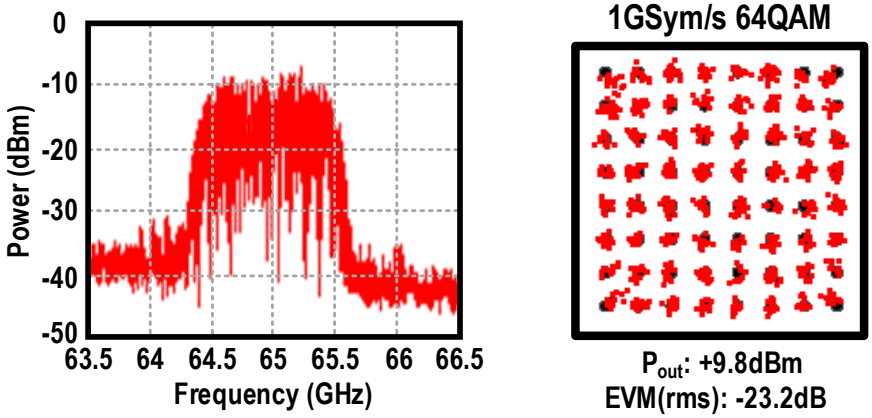


Figure 6.16. Large-signal measurements in FPM and BPM across 60-70GHz: (a) Psat and OP1dB. (b) peak PAE and PAE at OP1dB.

Figure 6.16 shows key large-signal performance vs. frequency, including P_{sat}, OP_{1dB}, peak PAE, and PAE at OP_{1dB}. The PA maintains good performance within the bandwidth of 60-70GHz. The lowest frequency of large-signal test is limited to 60GHz due to the band-limited test setup. However, the PA is expected to still maintain good performance down to 52GHz since it is within the 3-dB BW.



(a)



(b)

Figure 6.17. Measured spectrums and constellations for (a) 1.5GSym/s 16QAM and (b) 1GSym/s 64QAM at 65GHz.

The PA was also tested with modulated signals at 65GHz. Figure 6.17 shows constellations for two test cases. The measured 65-GHz spectrum shown in Figure 6.17 was down-converted to a 3.5-GHz IF and captured by a VSA. In Figure 6.17 (a), the PA has an average EVM_{rms} of -21.9dB with an average P_{out} of +10.5dBm and an average PAE of 7.2% for 1.5GSym/s 16QAM. For 1GSym/s 64QAM shown Figure 6.17 (b), an average EVM_{rms} of -23.2dB with an average P_{out} of +9.8dBm and an average PAE of 8.2% is achieved. Figure 6.18 (a) shows the EVM_{rms} vs. P_{out} in FPM and BPM for various modulations. The measurement setup has an EVM_{rms} floor of -22dB/-24dB for 6Gb/s 16-/64-QAM, respectively. Therefore, the true PA performance is expected to be

better than what is reported. Figure 6.18 (b) plots the PAE vs. P_{out} in FPM and BPM which is similar to Figure 6.15, but in this case it is for modulated signals at 65GHz. As seen in the figure, the average PAE can be improved by 4.5% points at the P_{out} of +9dBm when switched to BPM while maintaining reasonable EVM_{rms} of -20dB for 4Gb/s 16QAM modulation. Note that the simulated AM-PM distortion was below 3°/1° for FPM/BPM up to OP_{1dB} (13.5dBm/9.6dBm), respectively. Therefore, the AM-PM conversion is not suspected limiting the overall EVM performance.

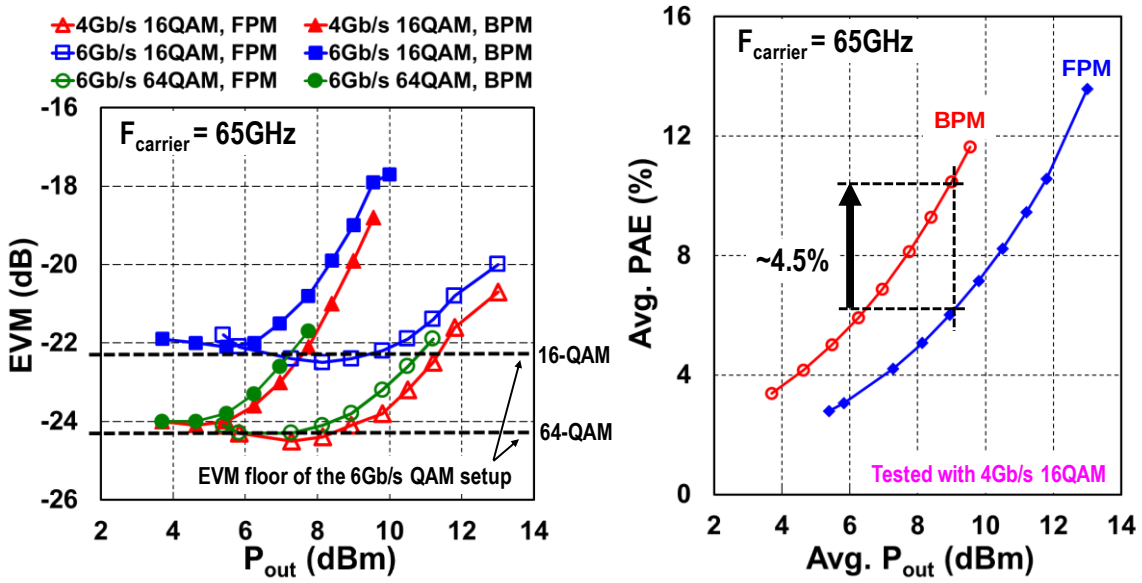


Figure 6.18. Measurements of modulated signals. (a) EVM_{rms} vs. P_{out} for various modulations. (b) PAE vs. P_{out} with 4Gb/s 16QAM modulation in FPM and BPM.

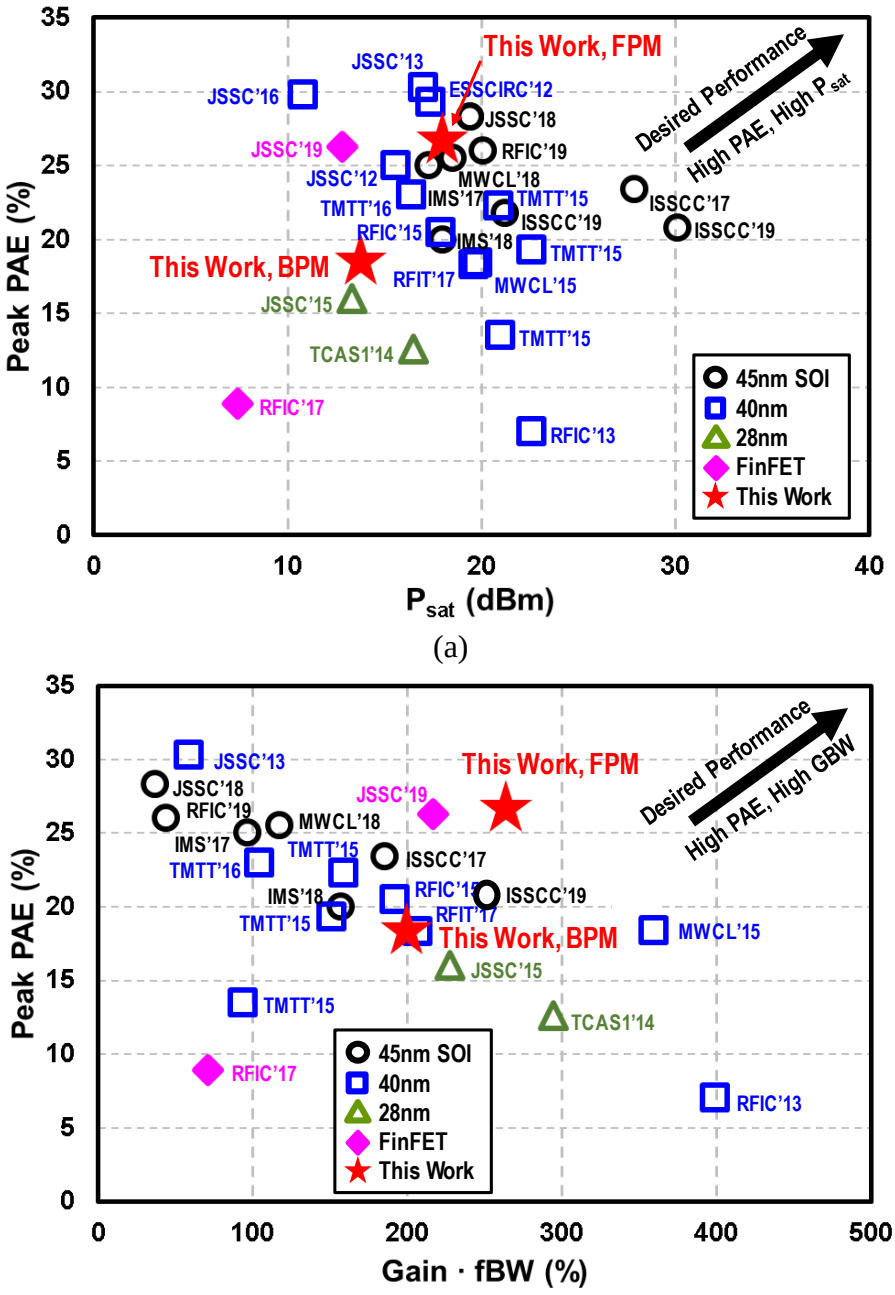


Figure 6.19. Performance comparison of mm-wave (50-75GHz) PA prior art. (a) Peak PAE v.s. PA Psat. (b) Peak PAE v.s. gain-fBW product.

Figure 6.19 plots selected prior art [30]–[49], [51]–[55], [68] of advanced 50-75GHz (V-band) CMOS PAs, with technologies varying from 45-nm SOI to 14-nm FinFET. The PAE versus P_{sat} is shown in Figure 6.19 (a), while the PAE versus gain-fractional BW (fBW) product is shown in

Figure 6.19 (b), where the fBW is defined as the small-signal 3-dB BW divided by the center frequency. The desired performance is on the upper-right corner, meaning high PAE, high P_{sat}, and high gain-fBW product. As seen from Figure 6.19 the FPM of this design improves upon prior art for FinFET mm-wave PA designs [3] while also obtaining a respectable performance in BPM. Table 6.1and Table 6.2 compare the PA's performance with prior-art.

6.4 CONCLUSION

This work presented the design of a reconfigurable V-band 2/4-way non-uniform power-combining PA implemented in 16-nm FinFET CMOS. The PA achieves a high gain with large fractional bandwidth while also demonstrating back-off efficiency enhancement when switching from full-power mode (FPM) to back-off power mode (BPM). This work demonstrates the viability of high-power PA design in deeply-scaled FinFET CMOS, thus enabling development of mm-wave SoCs for next-gen wireless communication systems.

Table 6.1. Continuous Wave Performance Comparison to Prior-Art Mm-Wave Power Amplifiers

	This Work		[1]	[2]	[4]	[3]
Technology	16nm FF		45nm SOI	40nm	14nm FF	22nm FF
Topology	2/4-Way Non-Uni Power Comb.		Doherty	4-Way Power Comb	3-Stage CS	2-Stage CS
V_{DD} (V)	0.95		2	0.9	1	1
Frequency (GHz)	65		60	80	71	74
Peak Gain (dB)	21.4	18.5	12.9	18.1	16.7	16.6
Frac. BW[2] (%)	22.6	23.7	10[1]	19.1	10.4	32
P_{sat} (dBm)	17.9	13.8	20.1	20.9	7.4	12.8
O_{P1dB} (dBm)	13.5	9.6	19.3	17.8	2	5.7
Peak PAE (%)	26.5	18.4	26	22.3	8.9	26.3
PAE @ OP_{1dB} (%)	15	12	25.9	10[1]	4.8	11.6
Enhanced PAE @ PBO[4] (%)	18.4[3,5] @ 4.5dB PBO		18.5[1,3,6] @4.5dB PBO	-	-	-
Core Area (mm^2)	0.107		0.76	0.19	0.1	0.054

[1] Estimated from figures. [2] Fractional BW is defined as $\frac{BW_{3dB}\ (small\ signal)}{Center\ Frequency}$. [3] Tone-based tests.
[4] PBO from Psat. [5] Achieved by switching between two static power modes.
[6] Achieved dynamically without switching modes.

Table 6.2. Modulation Performance Comparison to Prior-Art Mm-Wave Power Amplifiers

	Technology	V_{DD} (V)	Frequency (GHz)	Modulation (M-QAM)	Data Rate (Gb/s)	RMS EVM (dB)	Avg. P_{out} (dBm)	Avg. PAE (%)
This Work	16nm FF	0.95	65	16	4	-20.7[2,3]	13	13
					6	-21.6[2,3]	11.8	10.6
				64	6	-23.2	9.8	7.2
[1]	45nm SOI	2	65	64	3	-23.1	13.8	15.7
[2]	40nm	0.9	73	16	3	-25[3]	11.9	4.5[1,4]
[3]	22nm FF	1	75	16	3	-26[2]	5.6	11
					6	-26[2]	5	10
				64	9	-28[2]	1.3	5

[1] Estimated from figures. [2] w/ equalizer ON. [3] Limited by setup. [4] Tested at 80GHz

Chapter 7. DEEP TRIPLE-PATH TX SELF-INTERFERENCE CANCELLATION TECHNIQUE FOR FULL-DUPLEX TRANSCEIVER

7.1 INTRODUCTION

Numerous research efforts over the last decade have focused on full-duplex techniques to potentially improve spectral efficiency [69]–[76]. However, for long-range and wideband radios which require high-output-power PAs, the transmitter self-interference becomes a major challenge to receiver sensitivity. This work explores the use of multi-point self-interference cancellation to achieve a deep cancellation over a broad bandwidth.

The motivation of applying full-duplex technique to wireless systems becomes self-evident by noting that the spectrum below 6GHz is completely occupied by various existing wireless applications. Conventional frequency-division-duplex (FDD) is widely used by wireless communications that has two dedicated bands, one for transmitting and the other for receiving. To better utilize and address the scarcity of spectrum below 6GHz, the full-duplex technique has been suggested [69]–[76]. In full-duplex systems, the transmit and receive channels are combined into one single band, thus potentially improving the spectral efficiency up to 2X [69]–[71]. However, a key challenge in FD systems relates to the fact that the transmitter becomes a very strong interferer to its own receiver. Depending on different standards, up to 120-dB self-interference cancellation might be needed [69]–[71]. The requirement of 120-dB SIC is difficult to achieve by relying on a single component. To achieve a deep cancellation depth over a wide bandwidth, distributing the cancellation along the receive signal path is the method that has been proven promising. The places to perform TX SIC in the FD transceiver can be generally categorized into three types, which are air interface, RF/analog front-end and digital front-end, see Figure 7.1.

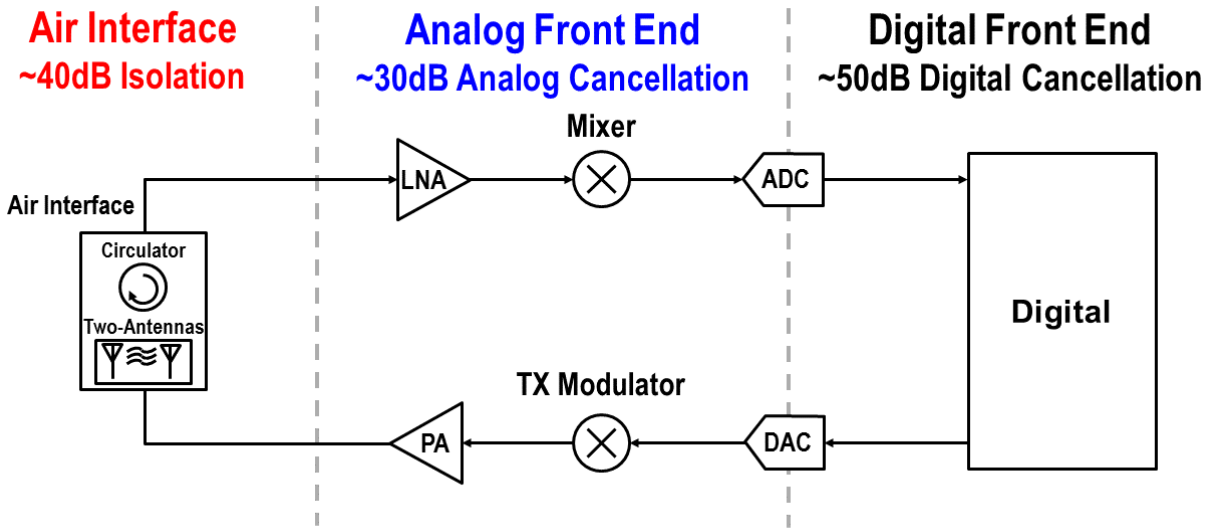


Figure 7.1. Assumed distribution of the transmitter self-interference cancellation along receiver signal chain.

The air interface can be off-chip circulators and two antenna approach [19], on-chip EBDs, or n-path-filter-based approaches that serves as a three-port element among antenna, TX and RX to provide the isolation or the first cancellation between TX and RX. Furthermore, to prevent the RX from saturation and to relax the dynamic range (DR) requirement of analog-to-digital converters (ADC), the feedforward RF/analog cancelers can be employed to perform cancellation early in the receive path [69]–[71]. The goal is to suppress the TX SI to a small enough level that the ADC has sufficient dynamic range to digitize both residual TX SI leakage and the desired signals. The residual TX SI can then be removed with fine-resolution and long-delay cancellation functions implemented in digital.

One possible distribution of the SI cancellation along the RX chain is shown in Figure 7.1, including a 40dB isolation achieved at the air interface and a 30dB cancellation in the analog front-end, with another 50dB in the digital portion of the RX to achieve a total 120dB SI cancellation [22]. The focus of this work is from the SI suppression at air interface to the RF/analog front-end using feedforward cancelers.

7.2 CANCELLATION ARCHITECTURE

7.2.1 *MultiMulti-point Feedforward Cancellation*

A number of previous works have demonstrated the use of feedforward RF/analog FIR filters as cancelers to synthesize the inverse response of the TX SI signals and inject the synthesized signals into the receive path to perform TX SI cancellation [69]–[71]. In full-duplex transceivers, there are multiple opportunities along the receiver chain to suppress the TX SI leakage, see Figure 7.2. The suppression could be achieved by using a circulator-like element at the antenna interface, along with multiple feedforward cancellation paths that potentially inject the synthesized TX SI into the LNA input and output, as well as some nodes at the analog baseband. For a feedforward canceler, the best point of capturing the TX SI signals is at the PA output because it contains not only TX signals but also the noise and non-linearities generated from the TX circuitry [69]. The advantages and disadvantages of two possible injection points in the receive path will be discussed.

(A) TX Output to RX Input: In full-duplex radios, the LNA input is the most vulnerable node to TX SI in the receive path. For example, assume an air interface that can provide 40dB TX-to-RX isolation and a Wifi TX that can deliver a 20dBm peak power that results a -20dBm TX SI leakage at LNA input after being attenuated by 40dB. The residual TX SI leakage of -20dBm will become an issue to the receiver especially at the sensitivity level which is at LNA's highest gain. Therefore, a sufficient amount of cancellation must be performed at the RX input to prevent LNA gain saturation from strong TX SI leakage, see Figure 7.2.. However, the effect of NF degradation will be significant since not only the inversed TX SI but also the noise of the feedforward canceler circuitry is all injected into the RX input without any gain stages to suppress the noise upfront. Furthermore, the number of taps of the FIR filters at RF frequencies will be limited by the driver-stage bandwidth and affordable extra loading to the TX output and RX input [2, 19, 23].

There are a few advantages of performing cancellation at carrier frequency: 1) Although the signal bandwidth is high (as high as 80MHz), it is still a small fractional bandwidth with respect to RF frequencies; 2) the silicon area of RF canceler is small at the cost of providing short-delay inverse response of the leakage paths (a few hundreds of picosecond) [69]–[71]

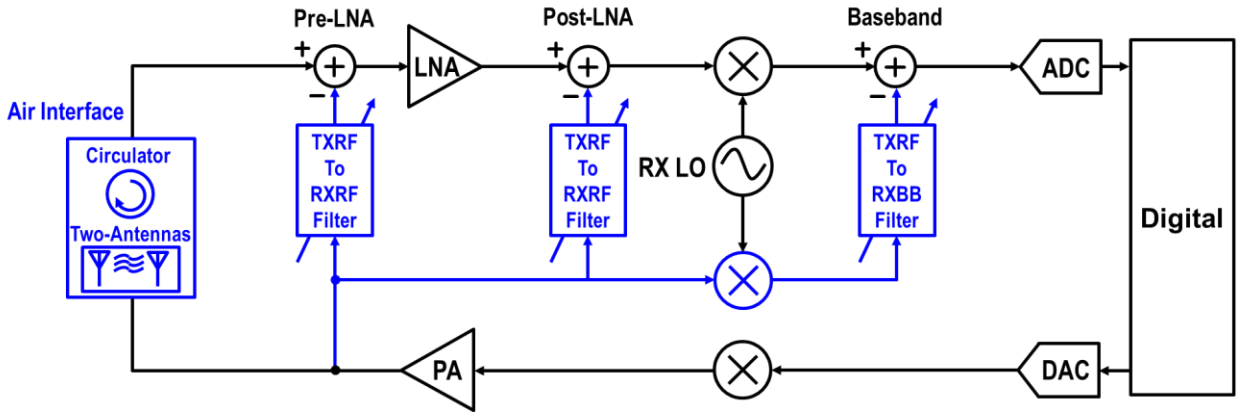


Figure 7.2. Some possible injection points of TX self-interference cancellation along the receiver chain.

(B) TX Output to RX Baseband: To provide the cancellation for long-delay TX SI leakage, the canceler can be implemented in RX baseband with a high RC time constant FIR filter [70]. Furthermore, the BB cancelers can provide fine resolutions (more loading) since they have less impact on bandwidth to the normal receiving path at baseband frequencies. However, this approach requires an extra auxiliary path to down-convert the TX SI signal that is latter fed into the I-Q baseband canceler to perform TX SIC at both I and Q paths of the RX (Figure 7.2.) [70]. One of the major issue is the complexity of performing cancellation for both I and Q paths. The mismatch between I and Q paths will degrade the cancellation capability. Another issue relates to the TX SI leakage reciprocally mixes with RX LO phase noise and appears at the cancellation node of RX baseband. Fortunately, the LO of driving RX-signal-path and SI-cancellation-path mixers are from the same LO source which are highly correlated, but it requires a time-delay block in LO path to

compensate the delay in auxiliary-path mixer to retain the cancellation at RX baseband [70].

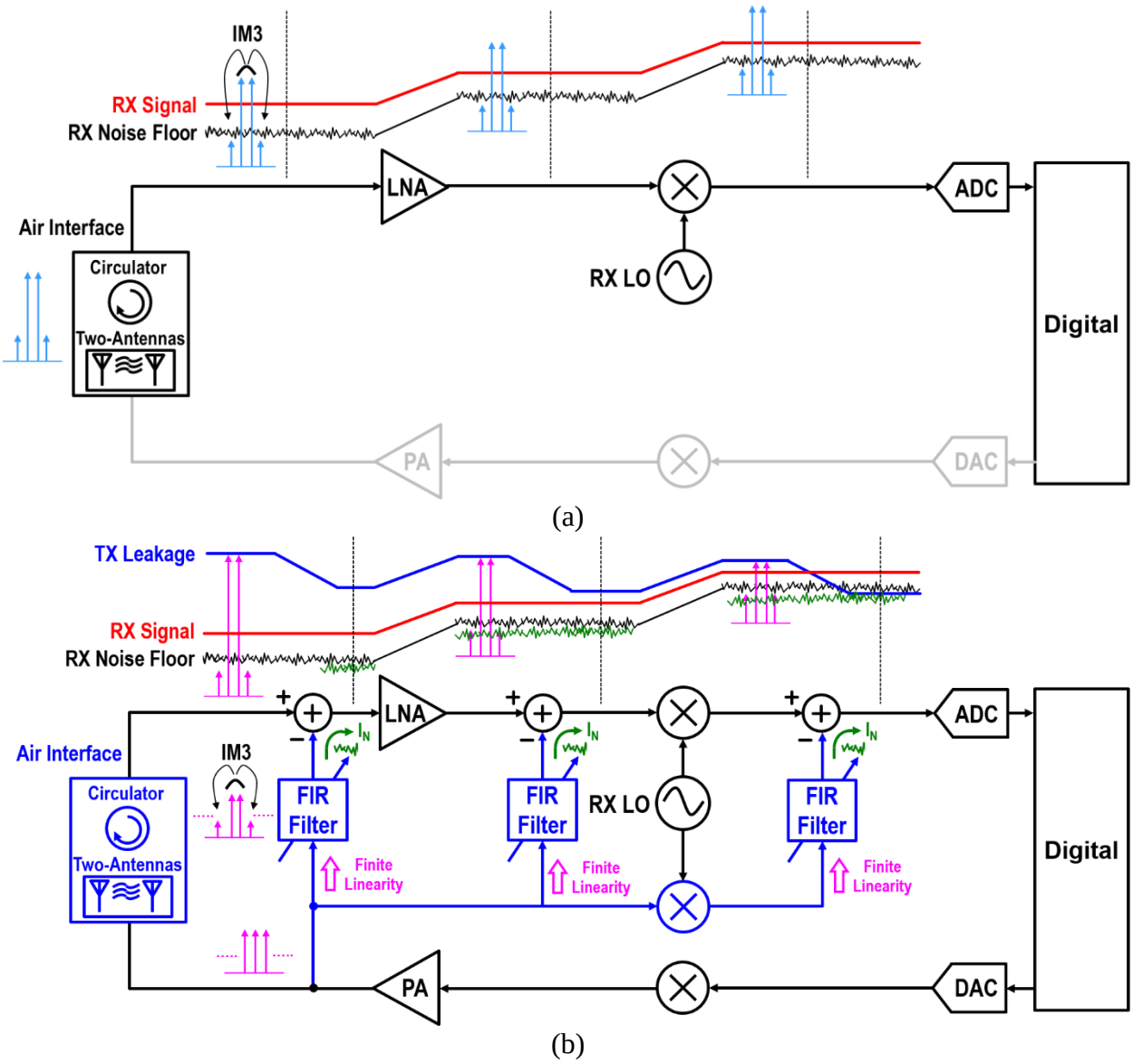


Figure 7.3 The trends of noise the linearity in (a) conventional RX signal path and (b) feedforward cancellation path, as moving down to the backend of RX chain.

7.2.2 *Noise and Linearity in Feedforward Cancelers*

In a conventional receiver design, to obtain a good sensitivity, the emphasis is on applying gain circuits with low noise earlier in the chain, see Figure 7.3(a). Therefore, with gain stages, the noise of the later stages in the receiver will be suppressed and thus their noise requirements can be

relaxed. Conversely, the gain in the receiver will amplify desired signals, placing the burden of linearity towards the backend of the receiver.

Unlike the desired signal which experiences the gain all along the receive chain, the TX leakage is attenuated at multiple points by the cancelers with some gain along the signal receive path, see Figure 7.3 (b). Any cancellation component will contribute noise that degrades the signal-to-noise ratio (SNR) of the desired signal. Similar to classic receiver design, the noise contributed by the first cancellation component has the most impact on the receiver noise figure, while the impact from later cancellation stages are less significant.

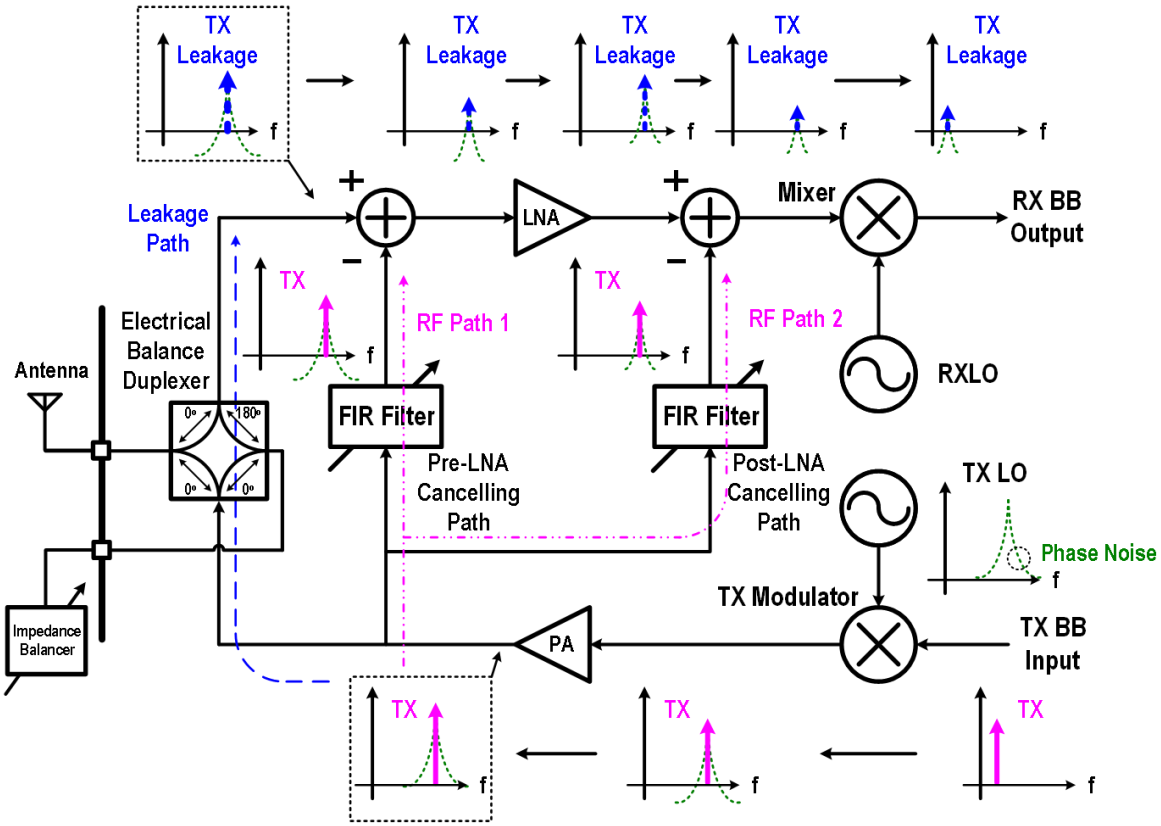


Figure 7.4 Conceptual diagram of TX self-interference suppression as signal passes from the transmitter to the receiver.

A high canceler linearity is desired since any intermodulation (IM) products produced by the cancelers will directly contribute to the noise and distortion floor of the receiver and degrade the

signal-to-noise-and-distortion ratio (SNDR) of the desired signals. The ultimate goal of the canceler linearity is to make the IM products lower than the receiver noise floor (Figure 7.3b)). Again, the self-interference is decreasing as we move down the receiver chain, thus the canceler linearity requirement can potentially be relaxed toward the receiver backend. This is due a few facts: (1) the receiver noise floor has been amplified; (2) the TX leakage has been suppressed; (3) and less canceler gain is needed to match the leakage path with cancellation path (Figure 7.3b). Interestingly, the requirement of the feedforward canceler linearity is direct contrast to traditional receiver design.

7.2.3 *Dual-RF Cancellation at Carrier Frequency*

A dual-path cancellation architecture was presented in [70] that achieved an on-chip cancellation depth of 50dB over a 40-MHz BW. This approach applies an RF cancellation at the receiver input, while a second path performs a suppression in the analog baseband through an auxiliary down-conversion path. Each cancellation path contains an analog FIR filter supplied by the PA output which generates the inverse response of the leakage path. This approach is challenged by the introduction of the additional I-Q down-conversion mixers and a complex FIR filters to perform cancellation. Lastly, the circulator in this publication was off-chip. The work described in this work relies on three components to suppress the TX SI along the receive chain, with an integrated Electrical Balance Duplexer (EBD) which provides a circulator-like function along with two feedforward RF cancelers, see Figure 7.4. In this implementation, the output of the second cancellation path has been moved from the analog baseband to the LNA output. This has several advantages as compared to [70]. First, it obviates the need for additional IQ down-conversion mixers in the baseband cancellation path. Moreover, the second canceler output precedes the downconversion mixer, thus relaxing the linearity demand on the mixers. Thirdly,

both RF cancelers perform suppression before SI signals hit the down-conversion mixer to reduce the reciprocal mixing products at the receiver output (Figure 7.4). Lastly, a wide cancellation bandwidth can be achieved by using two RF cancellation paths with a significantly lower fractional bandwidth, as compared to the equivalent BB implementation used in prior art [70]. In this dual-RF cancellation scheme, the two RF cancelers are identical with attenuators in front of each canceler and variable gain stages. The first canceler provides a coarse cancellation while the second canceler suppresses the TX SI in an effective finer step as the SI being amplified by LNA.

7.3 Linearity Issues in Post PA Interference Cancellation Circuits

Ultimately, utilizing frontend components which provide suppression of transmitted signals with a high output power PA (24dBm) and sophisticated multi-carrier modulation methods will demand linearity performance which may be challenging to achieve using purely an electronic solution. Take a feedforward canceler as an example, see Figure 7.4, the PA delivers a multi-carrier signal which is fed into the canceler and coupled to LNA input with a proper inverse response for cancellation. The canceler with limited linearity generates a bunch of inter-modulation products which is also known as spectral regrowth. The nonlinearities injected from the canceler at LNA input act as an added noise floor to the RX input that will degrade the sensitivity of the RX. For example, a PA transmits a two-tone signal at the canceler input with an output power of 24dBm (21dBm each tone). For a 20dB isolation between the PA the LNA, the canceler gain is set to be -20dB to match the SI signal at LNA input, which introduces two 1dBm-power tones at the LNA. Now, assuming a -90dBm RX noise floor at the LNA input and leaving 10dB as the margin, the third-order intermodulation products need to be as low as -100dBm. This makes the required input IP3 of the canceler to be 71.5dBm (101/2+21dBm) which is unachievable if purely an electronic solution is used.

While significant prior work has performed the non-linear models of components at the output of the a PA for a variety of elements [77], [78], this analysis attempts to simplify the linearity challenge for the CMOS technology, by reducing the problem to a high-output power signal driving a simple switch, or even a junction drain capacitance.

When a switch is biased in a triode region (ON state, V_{GS}=V_{DD}), a large signal swing at a drain/source node modulates the on-resistance r_{on} which produces nonlinearity. However, even if the switch is in the OFF state (V_{GS}=0), the large signal swing also modulates reverse-biased junction capacitances of the transistor which contributes nonlinear currents flowing into the signal path.

Here we first analyze the nonlinear behavior of a simple reverse-biased diode. The junction capacitance of a diode, C_j, is expressed as:

$$C_j = A\frac{C_{j0}}{\left(1+\frac{V_R}{V_j}\right)^{m_j}} \tag{7.1}$$

where A is the area of the junction, C_{j0} is the junction capacitance at zero bias, V_R is the reverse-biased voltage, V_j is the junction built-in potential, and m_j is the bottom junction capacitance grading coefficient. To derive the linearity of a reverse-biased diode, a simple circuit is used that includes a reverse-biased diode and a linear capacitor in parallel, Figure 7.5 (a). C_j is the junction capacitance of the diode and C_L is a linear capacitance from signal routings and other parasitic. In this setup, the DC content of V_R is 0V while an AC two-tone signal, $A\sin\omega_1 + A\sin\omega_2$ is applied to V_{ac}. The IIP3 can thus be derived as [79]:

$$A_{IP3} = 2 \times \sqrt{\frac{C_j + C_L}{\frac{C_j}{1 + \frac{V_R}{V_j}} \frac{m_j(m_j + 1)}{V_j{}^2}}} \tag{7.2}$$

Eq. (7.2) shows that a reverse-biased junction capacitor contributes to nonlinearity.

Now consider a NMOS switch which be modeled by several capacitances and diodes, as shown in Figure 5.1. (b). C_{sb} and C_{db} are the junction capacitances. C_{gs}, C_{gd}, and C_{ov} are the capacitances formed between gate and drain/source. R_{sub} is the substrate resistance which is assumed to be zero in this analysis. A simple circuit is used to examine the linearity of a NMOS switch, see Figure 7.5 (c). V_G sets the ON/OFF state for transistor M_1 through resistor R_G, while the resistor R_{BIAS} pulls the drain node to ground, which again makes the reverse-biased voltage of the drain diode to be 0V. C_C and C_L are linear ac-couple capacitor and linear parasitic capacitance from the of signal routing parasitic, respectively.

When the switch is OFF, effectively C_{gs}=C_{gd}=0. The equivalent circuit is simplified as shown in Figure 7.5 (d). The nonlinear capacitance C_{db} is composed of three parts: bottom, oxide- and gate-edge sidewall junction capacitances, which is given as [80]:

$$\begin{aligned} C_{db} = {} & A_d \frac{C_{j0}}{\left(1 + \frac{V_R}{V_j}\right)^{m_j}} + (P_d - W) \frac{C_{jsw0}}{\left(1 + \frac{V_R}{V_{jsw}}\right)^{m_{jsw}}} \\ & + W \frac{C_{jswg0}}{\left(1 + \frac{V_R}{V_{jswg}}\right)^{m_{jswg}}} \end{aligned} \tag{7.3}$$

where A_d is the area of drain, P_d is the periphery of drain, C_{jsw0} and C_{jswg0} are the oxide- and gate-edge sidewall junction capacitance per length, V_{jsw} and V_{jswg} are the oxide- and gate- edge sidewall built-in potential, m_{jsw} and m_{jswg} are the oxide- and gate-edge side wall junction capacitance grading coefficients. When V_{ac}=$A \sin \omega_1 + A \sin \omega_2$, the IIP3 is obtained as Eq. (7.4). In this particular circuit, the linearity is determined by the ratio between the linear capacitance C_L and the nonlinear capacitance C_{db}. There are not many things can do to improve the linearity except for

reducing the transistor size, thus lowering the nonlinear current generated from the junction capacitances.

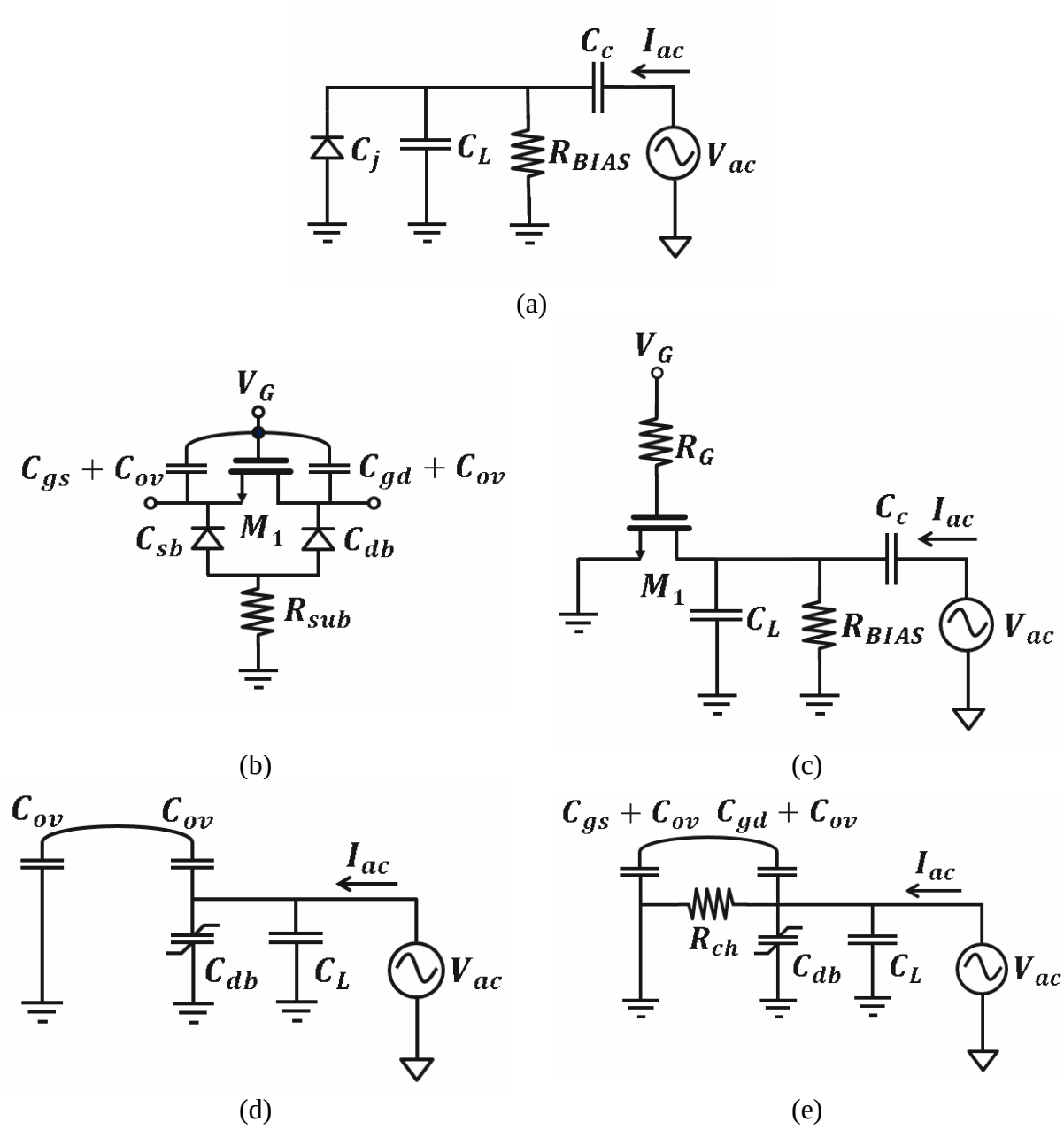


Figure 7.5. (a) A test circuit for a simple diode; (b) Capacitances in a NMOS transistor; (c) A test circuit for a NMOS transistor as a switch; (d) The equivalent circuit when the switch is OFF; (e) The equivalent circuit when the switch is ON.

$$A_{IP3} = 2 \times \sqrt{\frac{C_{db} + C_L}{C_j \frac{m_j(m_j+1)}{V_j^{\,2}} + C_{jsw} \frac{m_{jsw}(m_{jsw}+1)}{V_{jswg}^{\,2}} + C_{jswg} \frac{m_{jswg}(m_{jswg}+1)}{V_{jswg}^{\,2}}}} \tag{7.4}$$

$$A_{IP3} = \sqrt[4]{\frac{\left(\mu_0 C_{ox}(V_{GS} - V_T)\left(\frac{W}{L}\right)\right)^2 + \omega^2 (C_{db} + C_L)^2}{\left(\mu_0 C_{ox}\left(\frac{W}{L}\right)\right)^2 \left(\frac{3}{8LE_c}\right)^2 + Coe1^2}} \tag{7.5}$$

$$Coe1 = \frac{C_j}{4} \frac{m_j(m_j+1)}{V_j^{\,2}} + \frac{C_{jsw}}{4} \frac{m_{jsw}(m_{jsw}+1)}{V_{jsw}^{\,2}} + \frac{C_{jswg}}{4} \frac{m_{jswg}(m_{jswg}+1)}{V_{jsw}^{\,2}} \tag{7.6}$$

On the other hand, when switch is ON, the equivalent circuit is shown in Figure 7.5 (e), where R_{ch} is the nonlinear channel resistance. The IIP3 of the circuit is derived as Eq. (7.5), where E_C is the critical field strength (V/m).

The above test circuits are calculated and simulated using TSMC 40nm CMOS process with C_L=500fF and two-tone signals at 2.4 and 2.401GHz. Figure 7.6 (a) shows the simulated results of VIP3 for a diode junction capacitance as shown in Figure 7.5 (a). The results show consistency between Spice simulation and the calculation. For a diode size of 200µm×0.04µm, which the junction capacitance is 10.7fF, Eq. (7.2) gives us a VIP3 of 23dBV or 33dBm when the diode is in parallel with a 50Ω impedance. On the other hand, for an OFF-state NMOS switch of the same 200µm×0.04µm size, the nonlinear capacitance is 76fF, resulting in a VIP3 of 13dBV, as shown in Figure 7.6 (b). In both the case of a diode and an OFF NMOS switch, the linearity drops as the diode/switch size increases, because the nonlinear AC portion of the total current I_{ac} increases.

When the switch is on (Figure 7.6e), the I_{ac} is almost equal to the nonlinear current generated by R_{ch} because the on-resistance is low. The VIP3 is 0dBV for different width as shown in Figure 7.6 (c).

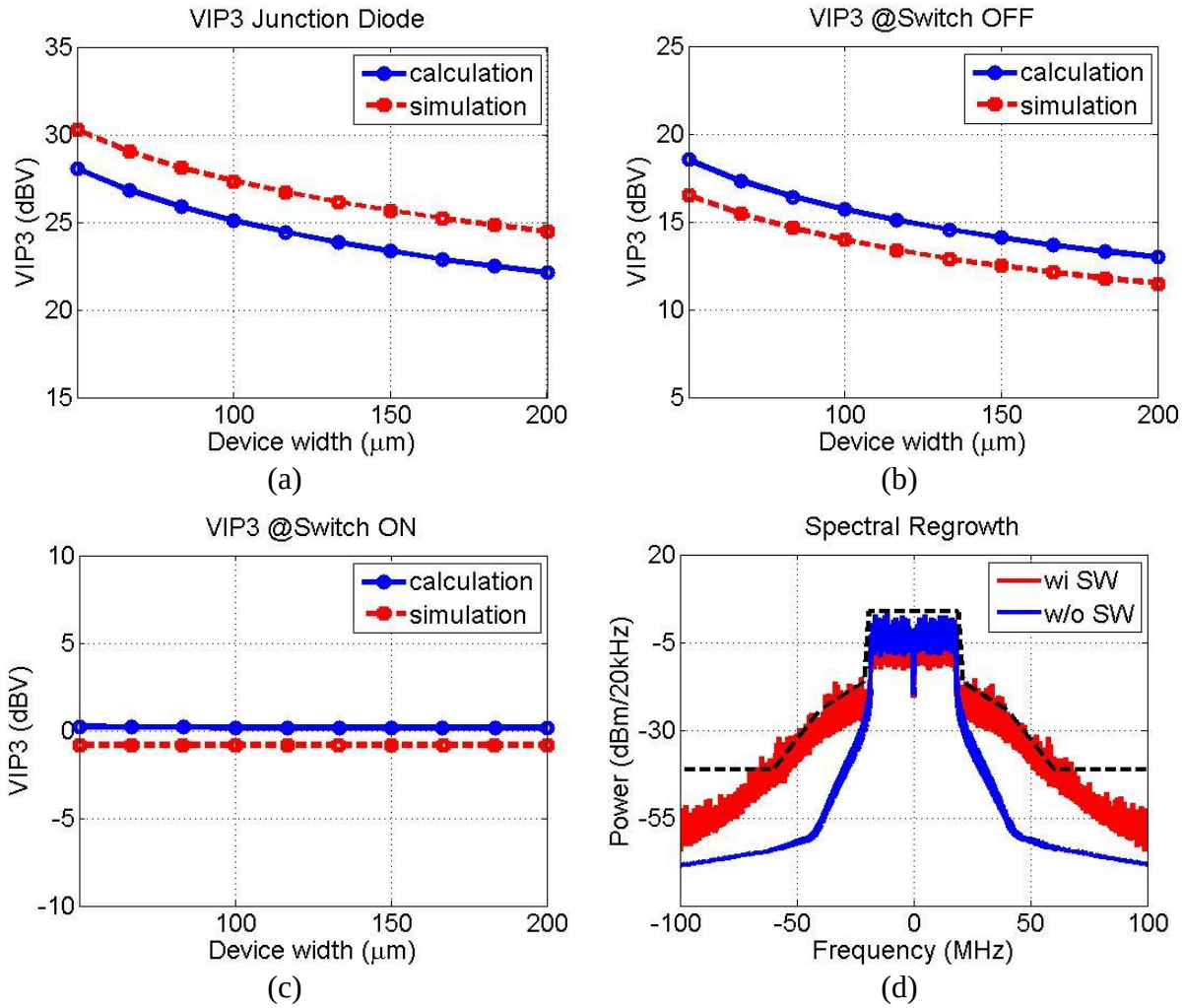


Figure 7.6. The calculation and Spice simulation results of IP3: (a) Diode junction capacitance, (b) NMOS switch is OFF, (c) NMOS switch is ON; and (d) The spectral regrowth due to limited switch linearity.

The insufficient linearity of an interface circuitry at TX output causes several problems. One of them is the spectral regrowth. As an example in WiFi with a 40MHz OFDM signal, the TX emission mask fails when an ideal PA delivers 29dBm output power through a 35dBm IIP3 switch, see Figure 7.6 (d). As mentioned in Section II, in FD applications, the insufficient linearity of a TX-RX interface circuit creates intermodulation products that not only increase the RX noise floor but also limit the maximum achievable SI cancellation from the feedforward cancelers.

A commonly used technique to improve the linearity of the MOS switches is by adding linear resistors/capacitors to build a voltage divider to reduce the voltage swing seen at drain/source nodes of the MOS switches [81]. Another method is to form a current divider to reduce the nonlinear portion of the total signal current [82]. Nonetheless, these methods still have limitations that make the TX-RX interface circuit implementation with high linearity remain extremely challenging. In fact, for high power output applications, an electronic solution to implement the circulator may not be possible, leaving the solution to the domain of other materials such as [83], [84].

7.4 CIRCUIT IMPLEMENTATION

The block diagram of the full-duplex transceiver system is shown in Figure 7.7 which depicts the components implemented on the chip. The transmitter includes the TX up-conversion path from analog baseband to the PA output. The TX modulator takes I-Q baseband signals and up-coverts them to the carrier frequency with a single-sideband generation. The PA delivers signals through a differential-to-single-ended transformer and an electrical balance duplexer to the antenna port. The receiver path starts from the antenna port, passing through the EBD that generates differential signals to LNA. The LNA converts and amplifies a power-mode signal input to a current-mode output as well as feeds them to the passive down-conversion mixers. The passive I-Q down-conversion mixers are driven by 25% duty-cycle LOs. The TIAs and baseband buffers provide signal amplification and driving strength to the offchip testing environments. This radio transceiver incorporates three blocks to improve the TX-to-RX isolation and perform TX SI cancellation, which are the EBD and two aforementioned RF cancelers. The EBD is connected among PA output, LNA input, and antenna port as a three-terminal air interface. The two RF cancelers pick up the PA differential outputs, synthesize the inverse response of the EBD leakage

path, and latter inject the synthesized current-mode signals into the LNA input and output to suppress the TX SI. This chip also includes an integer-N synthesizer for RX LO and a bandgap for circuitry bias.

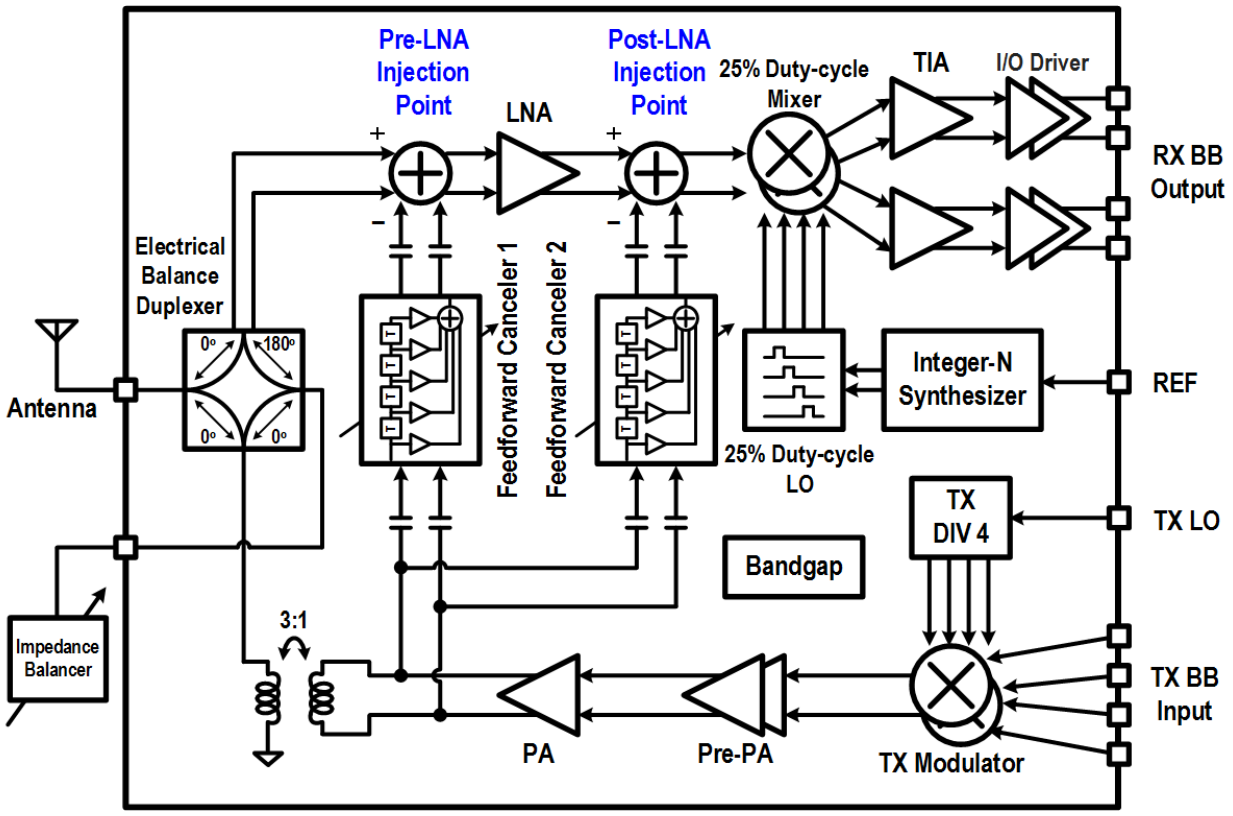


Figure 7.7. Block-level diagram of proposed full-duplex transceiver architecture.

7.4.1 *RF Front-end*

Figure 7.8 shows the detailed implementation of the RF frontend which contains an EBD as an air interface among PA, LNA, and antenna. The PA delivers a differential signal output to the matching transformer that transfers the signal to a single-ended current flowing into the EBD primary (see Figure 7.8, signals marked in red). The PA employs a Gm-linearization technique similar to under a 2.5V supply. The 1-to-3 transformer provides a conversion from a single-ended 50Ω antenna impedance to a differential 6Ω impedance, which is the r_{opt} of the PA.

The voltage-mode EBD provides a suppression of the differential TX leakage at the secondary

side and also serves as the single-to-differential conversion for the LNA input. The turn ratio of EBD is 2-to-4 that increases the matching impedance of the LNA to 200Ω for a good noise performance. Both antenna and balance impedance ports are connected to onboard connectors via bondwires. When the impedance on both side of the EBD primary are matched, the PA current signal will be divided into two equal part (Figure 7.8, red arrows at EBD primary). As a result, the PA currents induced at the secondary side have the same magnitude but are out-of-phase, which produce cancellation at the LNA input (Figure 7.8, blue arrows at EBD secondary). The EBD also generates the common-mode leakage which is mainly introduced by parasitic caps (Figure 7.8, signals marked in green).

The residual TX SI leakage at LNA input now can be divided into differential- and common-mode leakages. To further suppress the differential TX SI, the inputs of two RF cancelers are taped to the differential PA output to copy not only TX signal but also the noise and nonlinearities generated along the transmit path, see Figure 7.8. The cancelers are set to produce differential currents with the frequency response that matches leakage path but with opposite priorities. These currents are then injected at the LNA input and output, to further suppress the differential TX leakage (Figure 7.8, signals in blue). To minimize the possible degradation on the PA output power and LNA noise performance, both canceler present a high impedance at both the input (~3kΩ) and output (~1kΩ) to prevent loading the PA output and LNA input/output. On the other hand, for the common-mode TX SI at the receiver input node, the LNA is supplied under a 1.8V VDD to accommodate the common-mode voltage swings from TX SI. Moreover, the LNA employs tail current sources to provide a first-order common-mode rejection in the receiving path.

7.4.2 *TX Modulator*

The architecture of the TX modulator or up-conversion mixer is depicted in Figure 7.9. This

TX modulator employs the double-balance and I-Q single-side band (SSB) generation topology under a 2.5V supply. The baseband input of the modulator is made up with diode-connected NMOS that provides 50Ω - matching to off-chip interface by $1/g_m$. This input stage also performs signal conversion from power input to the current output flowing into the switch-quad.

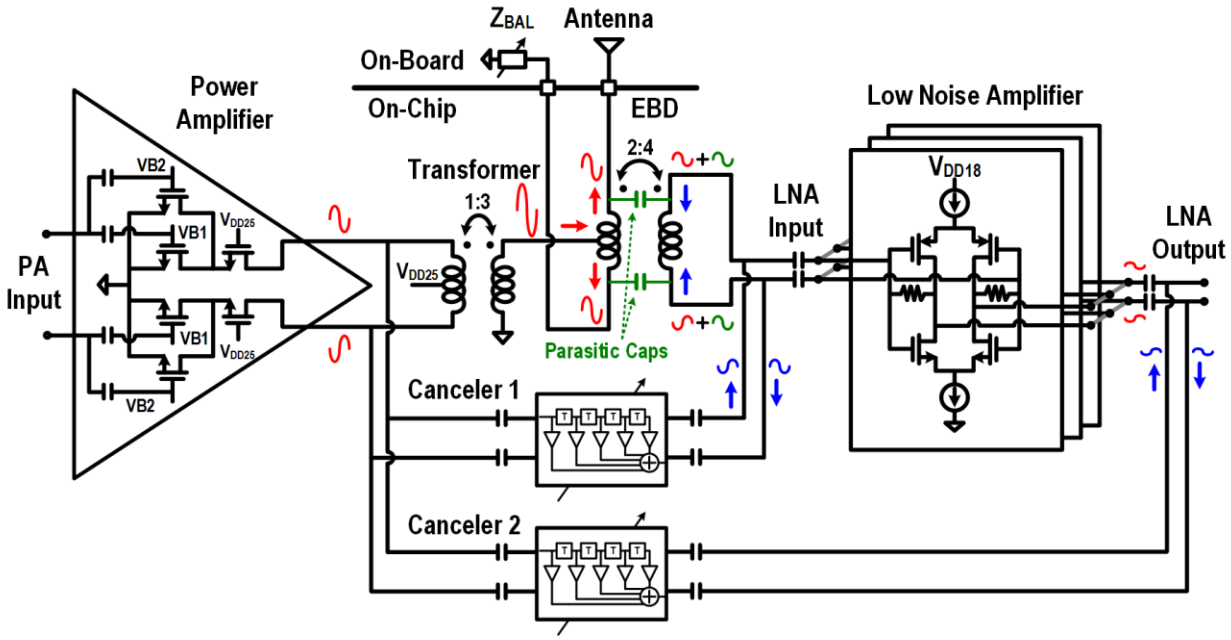


Figure 7.8. The RF front-end interface among TX output, RX input and antenna as well as the configuration of two feedforward RF cancelers.

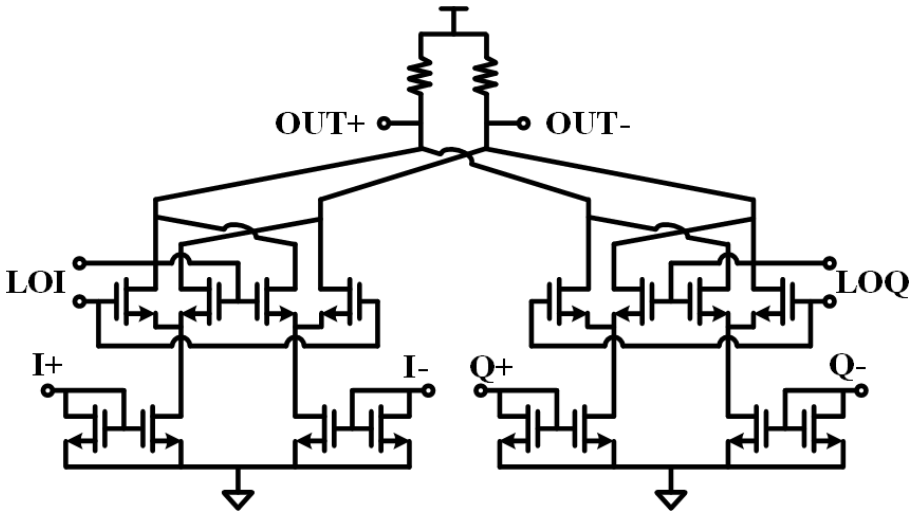


Figure 7.9. TX modulator with 50-input matching.

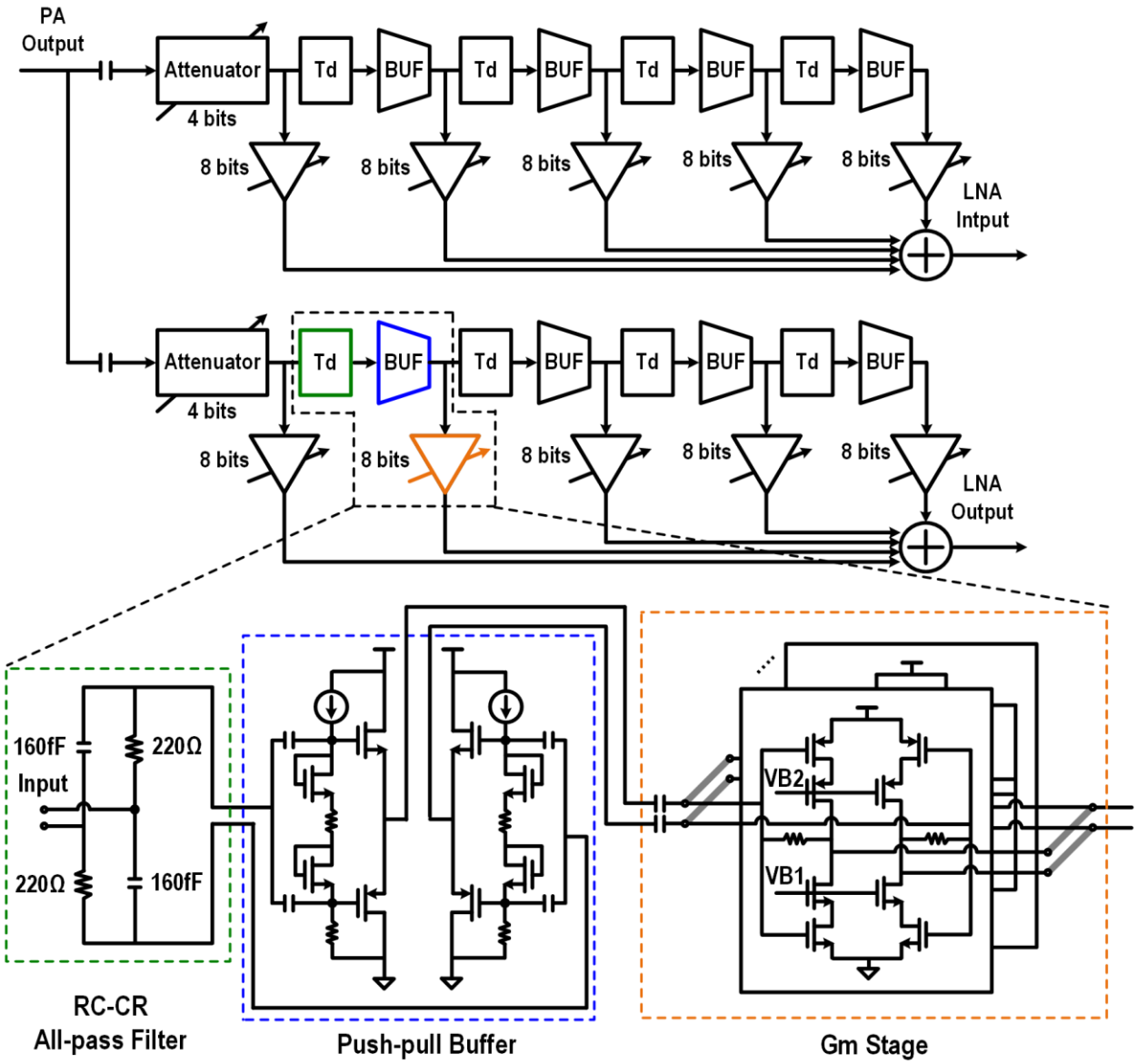


Figure 7.10. The block diagram of two real-number 5-tap and 8-bit FIR filters as RF cancelers.

7.4.3 *RF Cancelers and Linearity*

The block diagram of RF cancelers is shown in Figure 7.10. The cancelers are implemented with real-number 5-tap FIR filters, similar to the architecture in [70]. The time delay cell is made up of an RC-CR all-pass filter (APF), where the values of R and C are 220 and 160fF, respectively. The inter-tap buffer is implemented with a class-AB push-pull amplifier and has enhanced driving capability for wide bandwidth as well as high linearity, as compared to the implementation in [70].

The programmable transconductance (G_m) amplifiers employ complementary common-source with cascode stages and resistive feedback that act as filter coefficients to generate output currents with 8-bit resolution. In order to minimize the extra output loading attached to the RX nodes, the G_m stages are designed to have 7-bit binary-weighted unit cells with an added half-gain LSB implemented by stacking the common-source amplifiers to effectively double the length.

The effective high linearity of the canceler is achieved by attaching the canceler input to the PA output. The PA is designed to have a low optimal resistance (r_{opt}, differential resistance of 6Ω) for delivering a high output power by consuming high current under a limited supply voltage. The IIP_3 simulation of the canceler was performed by placing the PA r_{opt} in parallel with the canceler input, which is significantly lower than the real part resistance of canceler input itself (~3kΩ). This simulation approach most accurately reflects the voltage levels experienced at the canceler input when the PA is operating. The linearity of canceler is further enhanced by inserting a capacitive attenuator at the input. The simulated IIP_3 of the canceler is 40dBm, that is with respect to PA r_{opt} of 6Ω.

7.4.4 *Cancellation Algorithm*

A cancellation algorithm is built to adapt the FIR filter coefficients. The algorithm employs nearest neighbor search. The detailed flow chart is shown in Figure 7.11. An FPGA runs the algorithm to emulate a digital baseband and closes the filter adaptation loop. An ADC is connected to the RX baseband output to calculate the error signal of TX SI leakage. The error signal is obtained by calculating the total sum of squares (TSS) or the signal power. This algorithm starts by setting all the tap coefficients of the canceler to half gain. The search direction is decided by comparing the error signal levels between increasing and decreasing the gain for one step (1 LSB) at the first tap. The gain is then increasing or decreasing in one direction while continuously

monitoring the error signal till a lowest error signal is obtained. The coefficient is saved and the same process starts at the next tap. Several iterations might be needed to get the best result.

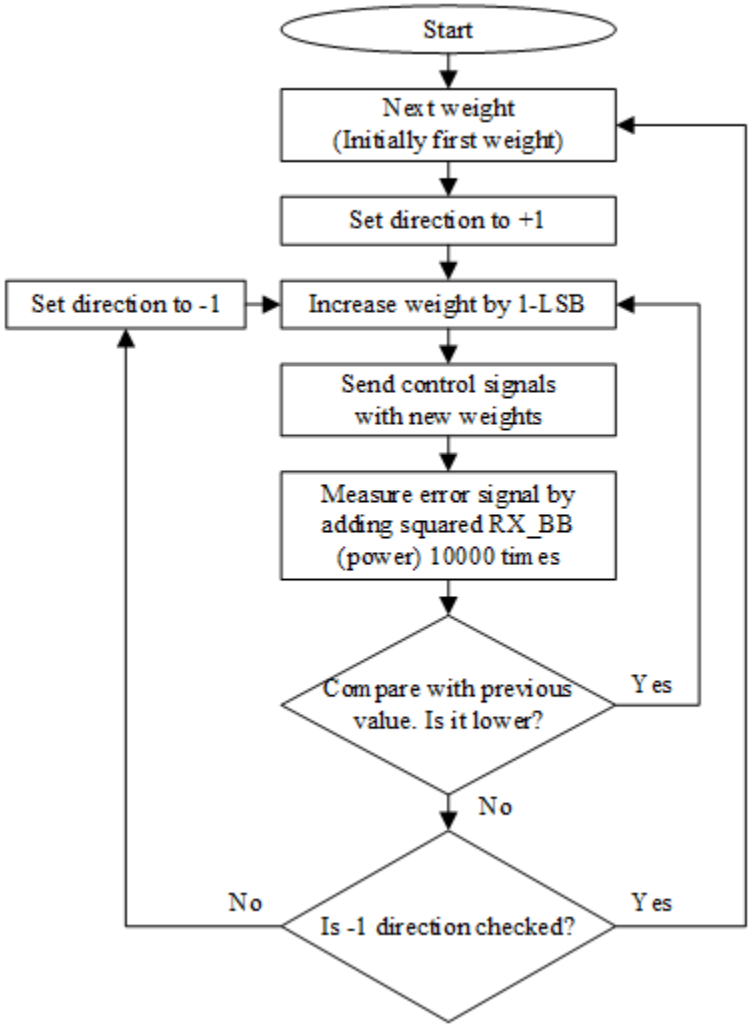


Figure 7.11. The algorithm for the cancelers.

7.5 MEASUREMENT RESULT

This prototype chip is fabricated in TSMC 40nm CMOS with 6-metal stack and 1 UTM layer. The total area is 4mm^2, Figure 7.12. The TX BB signal is fed from the top, going down through the TX up-conversion mixers, PA, EBD, and exiting at the bottom of the chip, to the antenna port. The receiver signal is brought from the bottom and outputs to the right. The cancellation path runs from the PA output to the canceler inputs (red arrow). The EBD occupies an area of 0.23mm^2

while both RF cancelers occupy an area of 0.12mm^2.

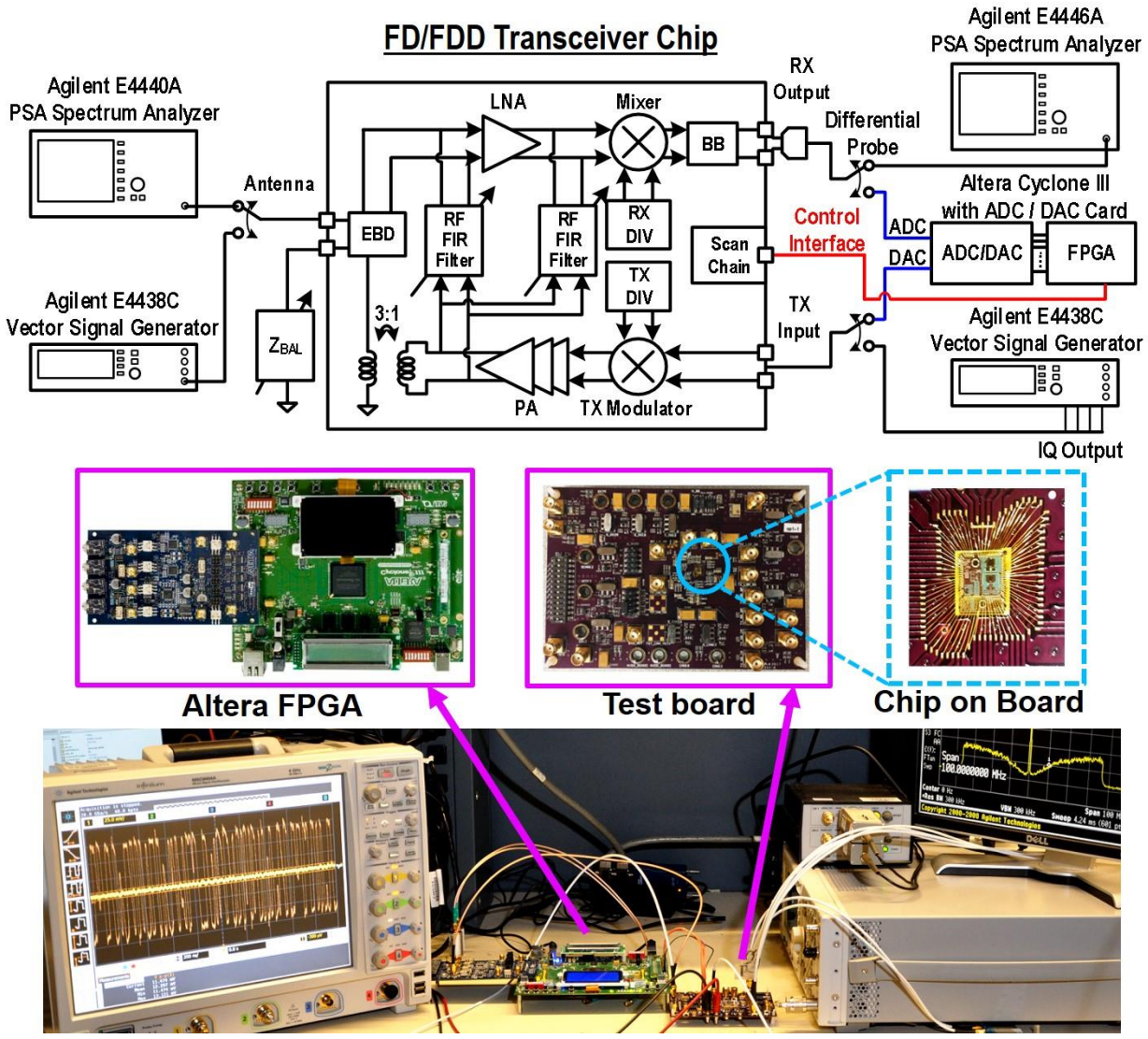


Figure 7.12. Measurement bench setup in lab for various modes of testing. Chip testboard with chip on board (COB) package and Altera Cyclone III FPGA board are shown.

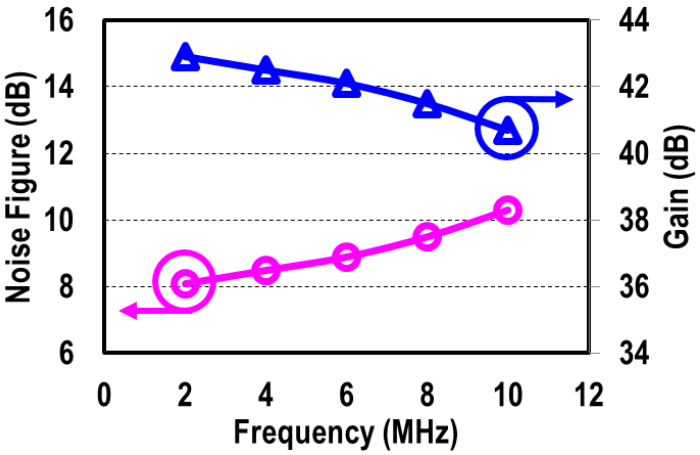
7.5.1 *Measurement Setup*

To characterize the performance of this full-duplex transceiver, the chip is assembled on a test board using a chip on board (COB) package, see Figure 7.12. The antenna port is connected to an equipment while the balance impedance port is terminated by a SMA 50 terminator. To measure

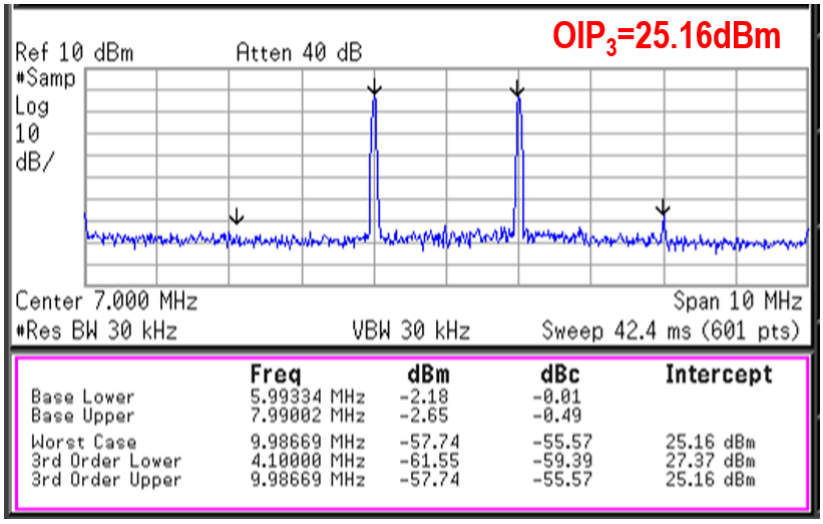
the transmitter, the TX signal is generated by a vector signal generator (VSG, Agilent E4438C) to provide continuous-wave (CW) or I-Q modulated signals. A spectrum analyzer (Agilent E4440A) is connected to the antenna port and captures signals from the transmitter. To measure the receiver, a signal generator is connected to the antenna port while a spectrum analyzer being attached at receiver baseband output through a differential probe (Tektronix P6246, DC-400MHz) or an on-board balun (Pulse CX2041NL, 50k-450MHz). To measure the chip in fullduplex operation, an Altera Cyclone III FPGA with a 14-bit ADC/DAC module board (Data Conversion HSMC) operating at 100MHz is used to execute the NNS cancellation algorithm and close the filter adaptation loop. The TX baseband I-Q inputs can take either DAC outputs from FPGA memory or the VSG with pre-recorded OFDM multicarrier packages for various testing purposes.

7.5.2 *Standard RF Transceiver Measurements*

The RX operates from 1.6GHz to 1.9GHz with a measured conversion gain of 42dB and a total noise figure (NF) of 8.09dB, see Figure 7.13(a), 5.6dB of which was contributed by the measured passive loss of the EBD. The IIP3 of the RX is -16.8dBm which is calculated from an OIP_3 of 25.2dBm under 42dB RX gain, Figure 7.13 (b). The PA has a measured output P_{-1dB}/P_{sat} of 10.6dBm/12.5dBm and an OIP3 of 16.5dBm, see Figure 7.14. The integer-N synthesizer has a measured locking range from 3.52GHz to 4.28GHz while consuming 10.4mW with a phase noise of -117dBc/Hz at 1-MHz frequency offset (Figure 7.15).



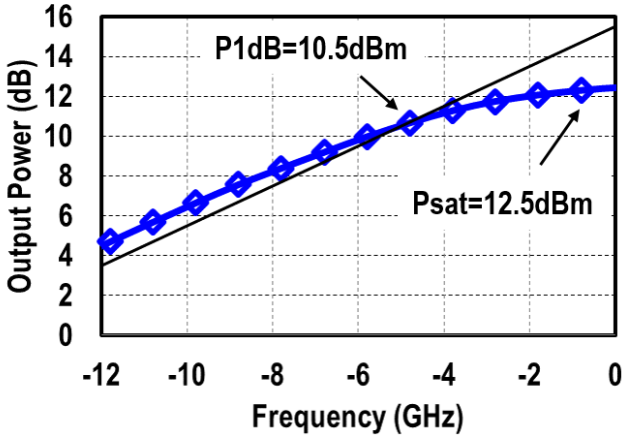
(a)



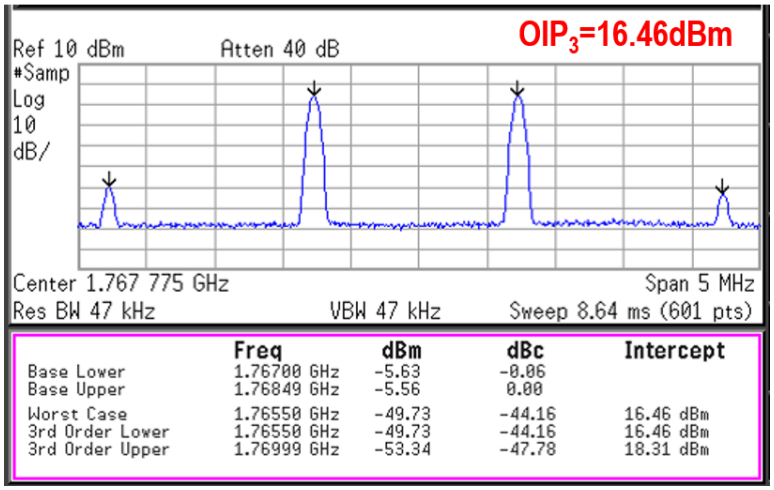
(b)

Figure 7.13. RX performance taken at RX baseband output at highest gain setting (42dB): (a) Noise figure and conversion gain; (b) OIP_3.

The canceler linearity measurement was performed using a standalone canceler circuit which is taped-out along with the main chip. The input IP3 was measured with respect to thePA optimal resistance, $r_{opt} = 6\Omega$. The measured IIP_3 depends on different settings of filter coefficients. Three different filter settings and the corresponding measured IIP_3 are shown, see Figure 7.16.



(a)



(b)

Figure 7.14. TX performance taken at antenna port: (a) P_{-1dB} and P_{sat}; (b) OIP_3.

7.5.3 *Full-duplex and TX SI Cancellation Measurements*

To obtain the coefficients of the two feedforward cancelers, the TX baseband was fed with OFDM multicarrier signals and the error signals were captured and calculated at the RX baseband output by the FPGA with an ADC module. Using the NNS algorithm described in 7.4.4, the canceler coefficients are obtained and saved for later use in measurements. We can also keep the algorithm running to adapt real-time changes of the coefficient if needed.

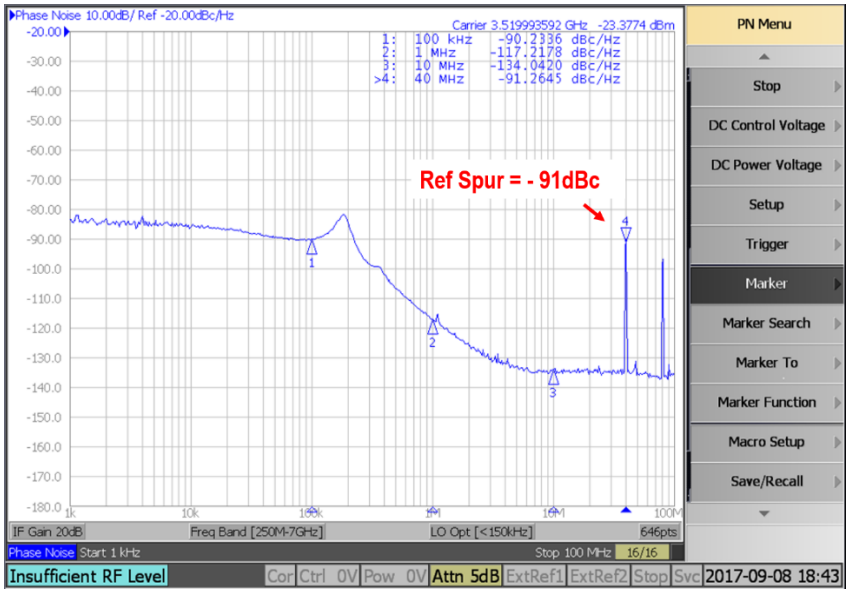


Figure 7.15. Phase noise measurement of the integer-N synthesizer.

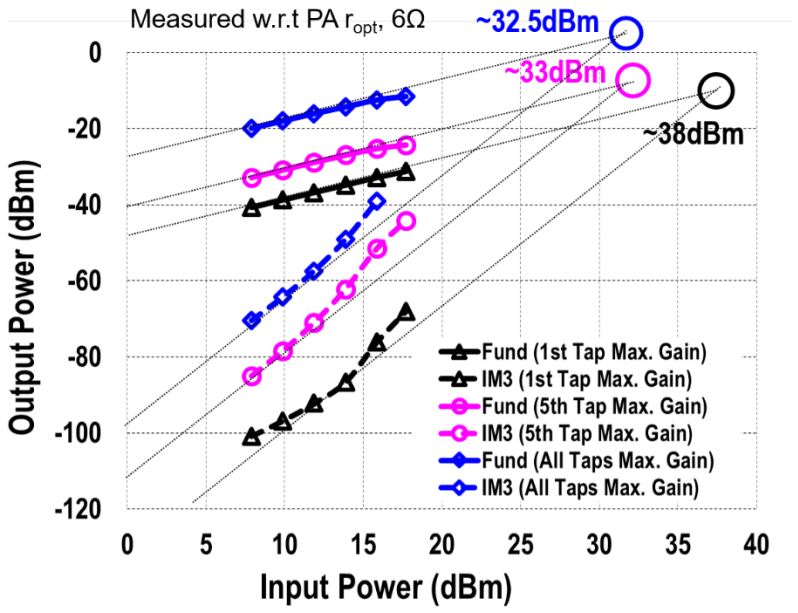


Figure 7.16. The experiment result of RF canceler measured with respect to PA r_{opt} of 6Ω using standalone test structure.

(A) *Tone-based Measurements*: After training and saving the canceler coefficient with modulated signals, the frequency response of the total cancellation is shown in Figure 7.17 that has a peak cancellation depth of 78dB. The measurement was done by sweeping the frequency of

a sinusoidal CW signal applied at TX baseband input. The contribution of each cancellation components is shown in Figure 7.17. The EBD response was characterized using an on-chip test structure and has a measured TX-to-RX isolation of 39dB over 200MHz with an on-board 50-Ω terminator. Two RF cancelers contributed a peak total TX SI suppression of 35dB. From the response in Figure 7.17, different signal bandwidth maps to different cancellation depth. For instance, a 65dB cancellation depth can be obtained with an 80-MHz bandwidth signal.

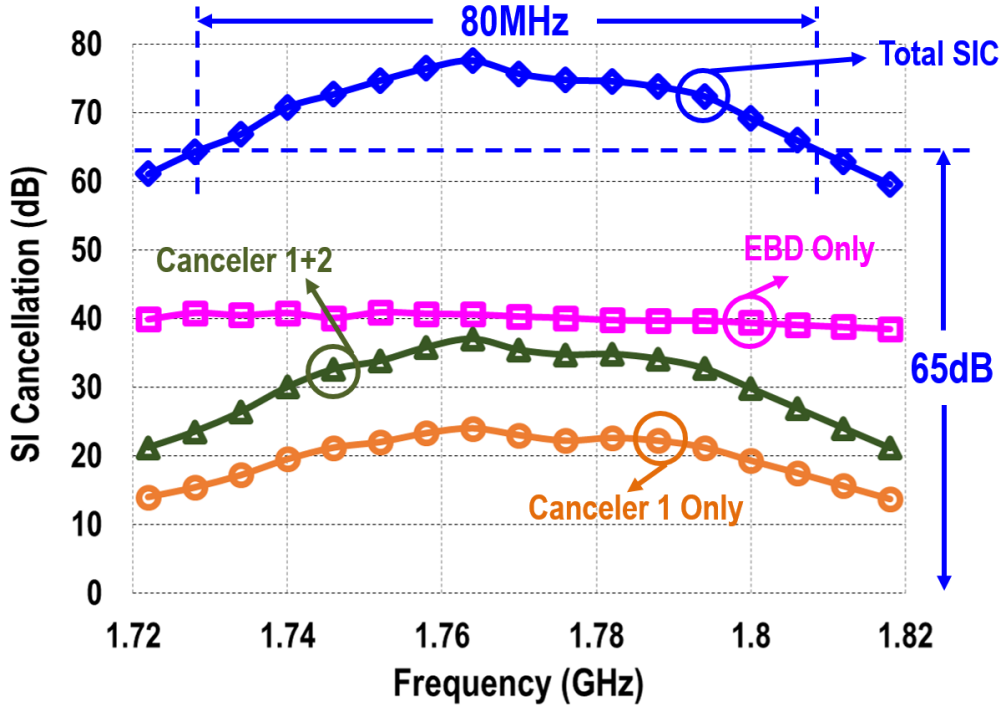


Figure 7.17. The frequency response of TX self-interference cancellation tested with sweeping sinusoidal-wave signal.

The degradation in the receiver noise figure is a key metric to evaluate how well the cancelers do in an in-band full duplex radios. The RX NF measurements were performed by monitoring the SNR at the RX baseband output with a desired RX CW signal applied at antenna input and comparing the SNR numbers with and without the presence of the TX SI CW signal at 1-MHz frequency offset. The measurement results are shown in Figure 7.18. The black curve is the NF

without the presence of TX SI. The receiver NF degrades by 8dB (pink curve) due to the severe gain saturation with the TX turned on at 5dBm output power. The NF degradation drops to 1.6dB after both cancelers are enabled (Figure 7.18).

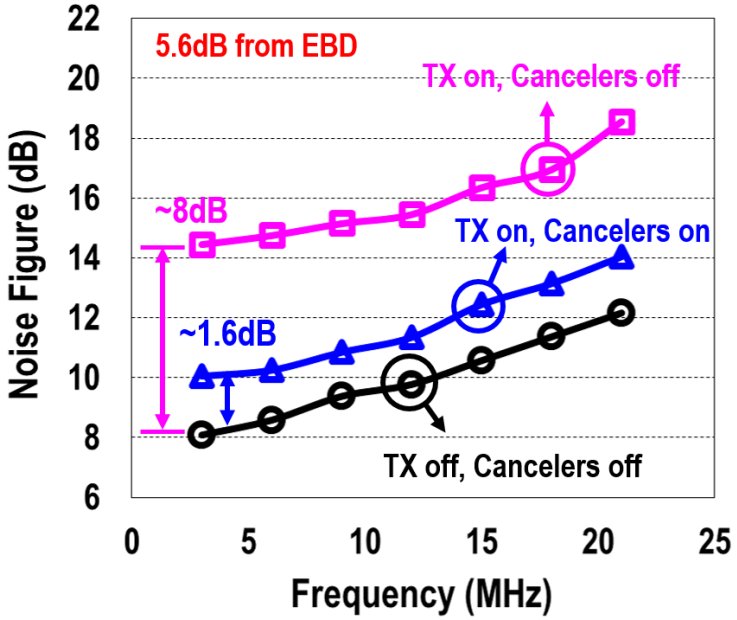


Figure 7.18. NF measurements and NF degradation of feedforward canceler turning on and off.

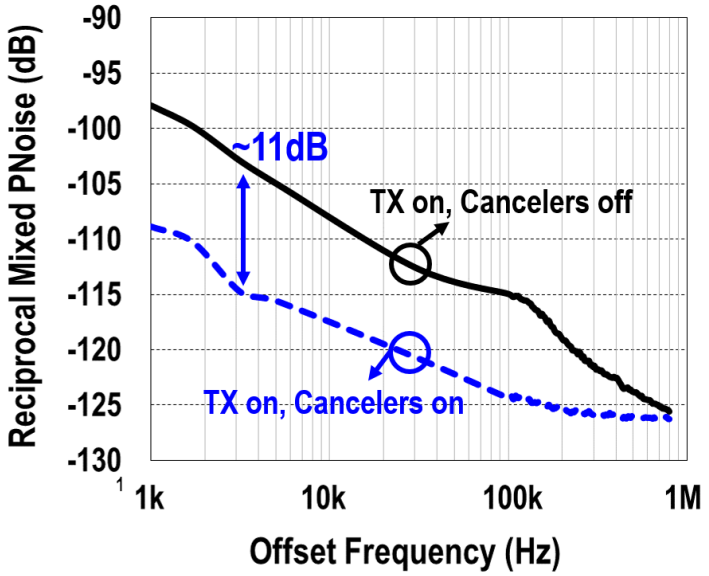
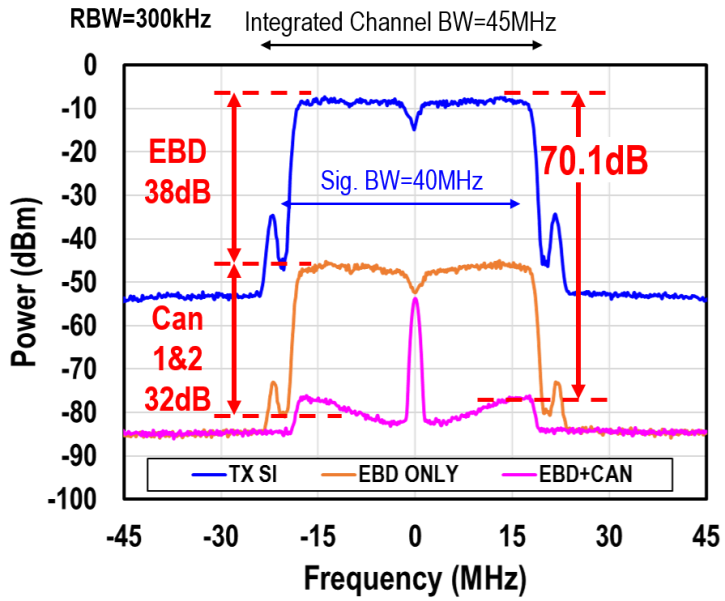


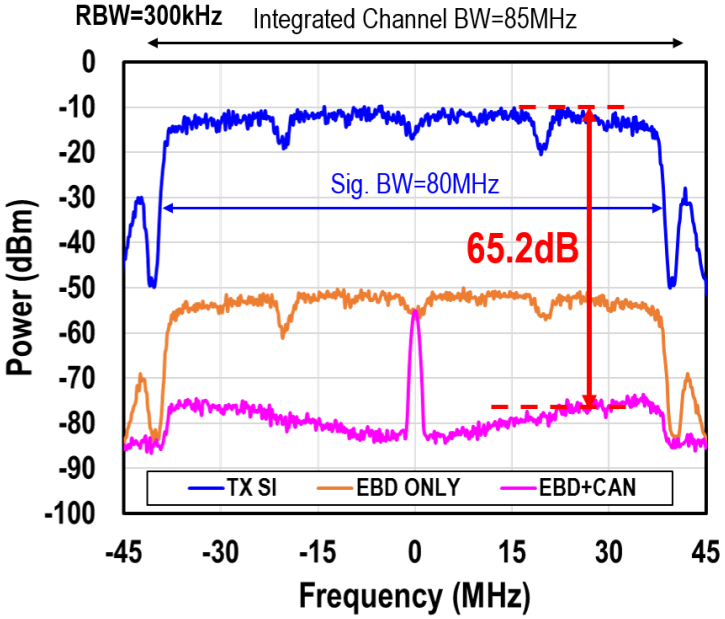
Figure 7.19. The self-interference mitigation on TX leakage reciprocal mixing with RX LO phase noise.

The TX leakage reciprocal mixing with the phase noise of RX LO, further degrades the SNDR at the receiver output. To characterize the suppression of reciprocal mixing products, the transmitter was set to output a CW signal. The signal is taken at receiver baseband output and measured with respect to the TX carrier with the cancelers disable and enable. This measurement shows that the reciprocal mixing products were suppressed by 11dB up to 1MHz offset frequency, see Figure 7.19.

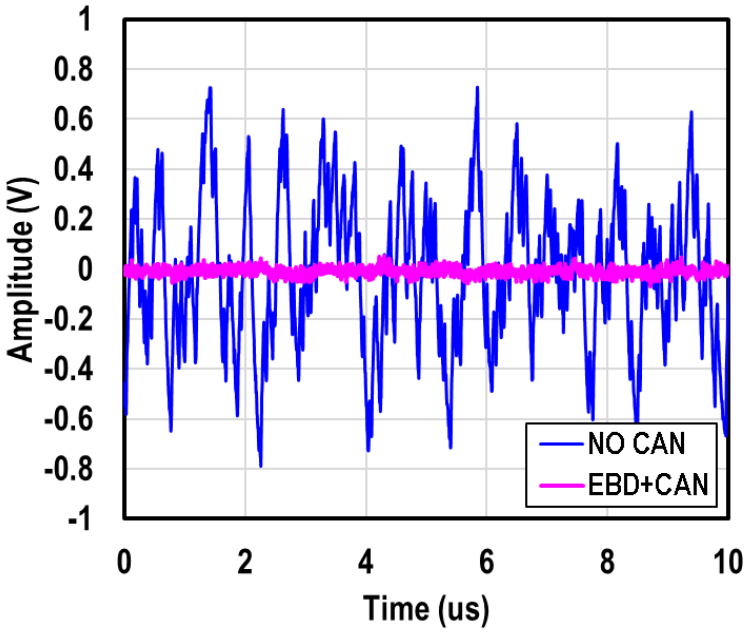
(B) *Modulated-signal Measurements*: The SI cancellation was also verified with modulated signal directly, see Fig. 20. The cancellation depth was obtained by comparing the channel power difference with an integration bandwidth. For a signal bandwidth of 40MHz (Figure 7.20a), the integrated channel bandwidth is 45MHz, the measured channel power difference is 70.1dB (blue curve to pink curve), which the EBD contributes 38dB and two RF cancelers contribute 32dB. The DC component (pink curve) is the artifact associated with the spectrum analyzer. Another example of an 80-MHz bandwidth, see Figure 7.20(b), the channel power difference is 65dB, tested with 85-MHz integrated channel bandwidth. These results agree to the single-tone sweeping measurements shown in Figure 7.17. Figure 7.20(c) shows the time-domain waveforms of a 40-MHz signal with and without cancellation, captured by oscilloscope (also see Fig. 12, left-lower side).


RBW=300kHz
Integrated Channel BW=45MHz
EBD
38dB
Sig. BW=40MHz
70.1dB
Can
1&2
32dB
TX SI
EBD ONLY
EBD+CAN
Power (dBm)
Frequency (MHz)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-45
-30
-15
0
15
30
45

(a)


RBW=300kHz
Integrated Channel BW=85MHz
Sig. BW=80MHz
65.2dB
TX SI
EBD ONLY
EBD+CAN
Power (dBm)
Frequency (MHz)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-45
-30
-15
0
15
30
45

(b)



(c)

Figure 7.20. Various measurement results with OFDM multicarrier Wifi packages captured at RX output: (a) spectrum of 40-MHz modulated signal BW with 45-MHz integrated channel BW; (b) spectrum of 80-MHz modulated signal BW with 85-MHz integrated channel BW; (c) the time-domain version of (a) captured by oscilloscope.

7.5.4 *Canceler Tap Delay Measurements*

The tap delays of the RF canceler were measured in a loopback configuration, see Figure 7.21. In the loop-back configuration, the TX baseband input was supplied with a CW signal and the signal was measured at RX baseband output when the LNA and the first canceler are OFF. As a result, the signals captured at RX output are purely the signals that travel from TX up-conversion to RX down-conversion, going through the second RF canceler path, see Figure 7.21(a). The TX and RX mixers were driven by two external signal generators that are synced with the same reference clock. The static waveforms were captured at RX BB by oscilloscope (Agilent MSO9404A). By turning one tap at its maximum gain at a time (others are kept to minimum gain), the waveforms from different tap outputs were collected, see Figure 7.21(b). The measured phase

difference of each tap is 32.6°. As a result, the average time delays of each taps is 50.9psec which were obtained by comparing the phase difference and then converted back to carrier frequency.

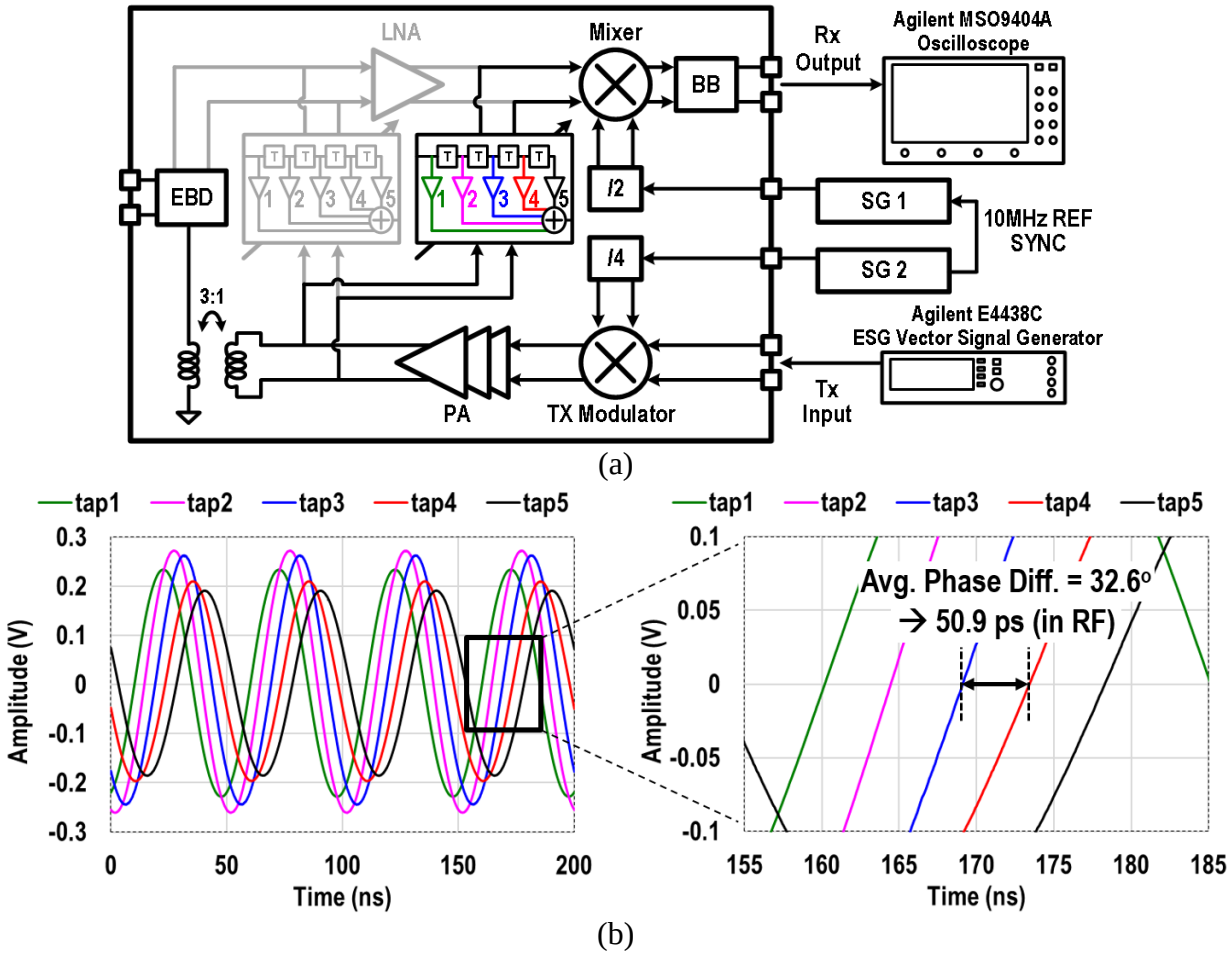


Figure 7.21. Feedforward canceler tap delay measurement: (a) bench setup and (b) time-domain waveform captured by Oscilloscope.

7.5.5 *Discussion on Limitation of SIC Depth*

The measurement results show that this FD radio can provide 70dB cancellation depth over 40MHz bandwidth, 35dB of which is contributed by two RF cancelers. However, in the system-level simulations, the expected total cancellation from two cancelers is more than 50dB with the designed the resolution of the filter coefficient. Two possible factors might contribute to the limitation of SIC depth. As discussed in Section 7.2.2, the insufficient canceler linearity will

generate intermodulation products that will limit the achievable cancellation. However, the measured IIP_3 of the canceler is 33dBm, which allows the around 50dB cancellation depth given that the TX SI at LNA input is - 20dBm and the IM3 level is 50dB lower than the leakage signal (Figure 7.16).

7.6 CONCLUSION

This chapter presents a complete full-duplex wireless transceiver system with the entire analog TX up-conversion and RX downconversion paths which achieves a combination with more than 72.8/70.1/65.2dB on-chip SI cancellation over20/40/80MHz bandwidths, respectively. A performance summary and comparison with prior arts is shown in Table 7.1. This was achieved by cascading three TX-to-RX isolation blocks along the receiver signal chain. The proposed front-end includes an EBD and two feedforward cancelers, which are implemented as filters to provide an inverse response of the leakage channel. The pre-LNA canceler is attached at the RX input, to relax the linearity requirements of LNA and the subsequent RX blocks, while the post-LNA canceler injects its output into the mixer input.

Future wireless applications could potentially have both FD and FDD mode. When network traffic is low, FDD would likely be more optimal from a power consumption perspective. With more wireless traffic and a demand for higher data rates, the device would have the option of moving to a FD mode of communication.

Table 7.1. Comparison Table with State-of-Art Full-Duplex Publications

	RFIC' 2017 S. Ramakrishnan	ISSCC' 2017 N. Reiskarimian	TMTT' 2017 B. Liempd	JSSC' 2018 T.Zhang	**This Work**
Architecture	Replica Cancellation DAC	N-path-filter Circulator	EBD+SAW Filter	Dual-Path + Adaptive Filter	**EBD + Dual-RF Adaptive Filter**
Technology	65nm	65nm	0.18μm SOI	40nm	**40nm**
Frequency (GHz)	1 -2	0.61-0.975	0.7 – 1.0	1.7 – 2.2	**1.6 – 1.9**
RX Gain (dB)	35	28	8.8	36	**42**
Noise Figure (dB)	3.6	6.3	7.6	4	**8.1 (5.6dB from EBD)**
RX in-band IIP3 (dBm)	-10 @ 35dB gain[5]	-18 @ 28dB gain	-3 @ 8.8dB gain	-5 @ 30dB gain	**-17 @ 42dB gain**
TX-to-RX Isolation (dB)	N/A External Circulator	40[1] On-chip Circulator	50 On-chip EBD	N/A External Circulator	**39[2] On-chip EBD**
Canceler IIP3 (dBm)	N/A	N/A	N/A	36 (RF) / 34.5 (BB) w.r.t 9Ω	**33~38[7] w.r.t 6Ω**
SIC under TX Power (dBm)	5 (w/o Circulator)	8	27	25	**5 at antenna port**
SIC NF Degradation (dB)	3.4[6]	1.7	N/A	1.5	**1.6**
SI Circuitry Power (mW)	N/A	36[8]	0 (passive)	11.5 (RF+BB)	**14.3 (RF*2)**
TX SI to RX LO Suppr. (dB)	N/A	N/A	N/A	10	**11**
Canceler Area (mm^2)	N/A	N/A	N/A	0.349 (RF+BB)	**0.12 (RF*2)**
Integrated TX Upconv. Path	Yes	No	No	No	**Yes**
Inttegrated PA	Yes	No	No	Yes	**Yes**
Integrated PLL	No	No	No	Yes	**Yes**
Active Area ($mm^{2)}$	6.25	0.94	6.62	3.5	**4**

[1] Averaged over 20MHz. [2] Measured with on-chip test structure. [3] Measured channel power difference with 40MHz 64QAM and 45MHz integration BW. [4] Measured channel power difference with 80MHz 64QAM and 85MHz integration BW. [5] Calculated by P1dB+10dB. [6] Calculated by the difference between system NF and RX NF. [7] Measured with on-chip test structure at 1.6GHz. [8] Antenna interface.

Chapter 8. CONCLUSION

The continued development of wireless communications has progressed to push higher data-rates in two directions – exploring new spectrum opportunities in mm-Wave bands and improving the spectrum usage for existing sub-6GHz systems. This dissertation proposes hardware front-end solutions which aim to increase data rates that further the goal of increasing data rates by developing mm-Wave front-end circuitry with good efficiency, low power, and low-cost techniques as well as improving the spectrum efficiency with full-duplex communications.

8.1 THESIS SUMMARY

8.1.1 *Mm-Wave Phased-array*

The goal of the research proposed in this thesis is to explore area and power efficiency techniques for future 5G and mm-Wave phased-array systems. Three chips have been designed, taped out to demonstrate these proposed techniques.

The G_m-assisted matching network receiver described in Chapter 3 utilizes the already existing matching network to provide a modest amount of gain before the noisy down-conversion mixer to improve the receiver noise performance. This 28nm CMOS prototype chip achieves a measured noise figure of 7dB which is 1-dB better than prior-art passive mixer-first RXs.

An in-depth discussion of the 1-bit front-end is presented in Chapter 4 which highlights several aspects and challenges when employing a 1-bit digitizer to the receiver. The system using QPSK signals seems promising and is verified by MATLAB system-level simulations.

Chapter 5 presents the design of a high-digitized phased-array receiver with digital beamforming implemented in TSMC 28nm CMOS. This receiver employs a number of novel techniques including a feedforward noise-suppressing front-end, a reconfigurable 0-3 SMASH

CTΔΣ ADC, and the digital beamformer. The design of this TSMC 28nm prototype chip is described.

A reconfigurable V-band 2/4-way non-uniform power-combining PA implemented in 16-nm FinFET CMOS is discussed in Chapter 6. To date, this PA presents the best Psat, PAE, and gain-fBW product in FinFET CMOS technologies. By employing non-uniform turns ratios to the output combiner with switch placement on the transformer's secondary side, the PA achieves 6-% PAE enhancement at a 4.5dB power back-off.

8.1.2 *Full-duplex Front-end*

The full-duplex prototype transceiver described in Chapter 7 demonstrates the validity of self-interference (SI) canceling architecture by using a 3-point injection. This chip is fabricated in TSMC 40nm CMOS and is tested with modulation signals which achieves more than 72.8/70.1/65.2dB on-chip SI cancellation over20/40/80MHz bandwidths, respectively.

8.2 FUTURE DIRECTIONS

8.2.1 *Mm-Wave Front-end*

Mm-Wave bands enable new spectrum opportunity for high data-rate (a few Gbps) communications. Many recent papers have shown significant improvement for the mm-Wave systems and circuits. Nevertheless, the focus of the future mm-Wave circuits will still be in two directions:

(1) Increasing the bandwidth: mm-Wave bands are significantly wider bandwidth than conventional sub-6GHz bands to provide sufficient BW for high data-rate communications. Assuming the same fractional BW can be achieved, the wider BW can be obtained with higher carrier frequencies in mm-Wave bands. However, as mentioned

in Chapter 6, ultra wideband front-end modules (FEM) will be desired to cover multiple bands using one FEM thereby reducing the system complexity. Though distributed amplifiers (DA) suffer from large silicon size, some recent distributed amplifiers show promising results with the power amplifier described in [85] showing the BW from DC to 108GHz. More new techniques need to be explored to keep increasing the obtainable FEM BW.

(2) Reducing the power consumption: the increased demand of longer usage time for handheld devices continue to drive more power-efficient techniques to improve the battery lifetime. However, implementing gain at mm-Wave carrier frequency is power in-efficient, as described in Chapter 2. Techniques to reduce the power consumptions while maintaining good gain and noise performance are still of interest in the future.

8.2.2 *Low-resolution and Highly-digitized Receiver*

Section 2.4 describes a proposed novel highly-digitized phased-array receiver for ultra-wideband, low power and compact size receiver front-end with intensive effort in digital back-end. The intension is to simplify the analog front-end and leave the burden to the digital back-end for some possible RF calibration so the complexity and power consumption of the analog front-end can be significantly reduced. There are several further studies can be done to achieve this ultimate goal:

(1) Low-resolution ADC: Chapter 4 discusses the extreme case for low-resolution ADC of using just an 1-bit digitizer. Though some interesting results were presented, the 1-bit digitizer can only handle simple modulations like QPSK and can hardly sustain the performance under blocking condition. Therefore, the low-resolution ADC of more than 1-bit might be a more convincing approach. The best solution still needs to be explored

considering the design trade-off among the number of bit of an ADC, the front-end circuit complexity, the power consumption of the whole system.

(2) Subtractive dithering: The dithering approach in Chapter 4 and Chapter 5 will contribute to the noise floor thereby degrading the noise figure for a single receiver. This is necessary for de-correlate the quantization noise between elements. However, though there's no a silicon demonstration available, a subtractive dithering has been proposed in prior art to suggest that the added dither can be subtracted out later in the signal path. As a result, there's no noise penalty of applying dither. Methods of applying a dither without degrading the baseline noise performances can be further explored.

(3) Reduced front-end requirements and calibrations: Given by the use of low-resolution ADC, the requirements for the receiver front-end would differ from conventional designs. Moreover, a more relaxed front-end specification is possible to further simplify the front-end design if some digital-assisted calibrations can be done.

(4) Higher-level algorithm for performance enhancement: Machine learning has caught a lot of attention for its application to graphical pattern analysis and the use for autonomous driving. There might be a possibility to use a classifier instead of a conventional demodulator to decompose the signal. This algorithm can also be trained to deal with different complex conditions, such as adjacent channel interferences, blocking, and IQ mismatch.

8.2.3 *Full-duplex Front-end*

A number of publications have proposed new techniques to improve full-duplex radios. However, none of them can provide cancellation for long-delay reflections (~nsec) on the chip. Implementing long-delay cancellation on the chip in the analog domain is not feasible since it

requires a large silicon size. In contrast, implementing long-delay element in the digital domain seems a convincing approach. This would require more research effort and new ideas before full-duplex systems can be applied to the commercial wireless radios.

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