The Design, Characterization, and Deployment of a Bipolar ±0.5-mV-Minimum-Input DC-DC Converter with Stepwise Adiabatic Gate-Drive and Efficient Timing Control for Thermoelectric Energy Harvesting

Eric Joel Carlson

A dissertation

submitted in partial fulfillment of the

requirements for the degree of

Doctor of Philosophy

University of Washington

2023

Reading Committee:

Joshua R. Smith, Chair

Visvesh S. Sathe

Jay Rajagopalan

Program Authorized to Offer Degree:

Electrical and Computer Engineering

University of Washington

Abstract

The Design, Characterization, and Deployment of a Bipolar ±0.5-mV-Minimum-Input DC-DC Converter with Stepwise Adiabatic Gate-Drive and Efficient Timing Control for Thermoelectric Energy Harvesting

Eric Joel Carlson

Chair of the Supervisory Committee:
Joshua R. Smith
Department of Electrical and Computer Engineering

This work presents a step-up DC-DC converter that is optimized to extract power from thermoelectric generators that generate extremely low voltages from small temperature differentials. The DC-DC converter uses a stepwise gate-drive technique to reduce the power FET gate-drive energy by 82%, allowing positive efficiency down to an input voltage of ±0.5 mV—the lowest input voltage ever achieved for a DC-DC converter as far as the author knows. Below ±0.5 mV the converter automatically hibernates, reducing quiescent power consumption to just 255 pW. The converter has an efficiency of 63% at ±1 mV and 84% at ±6 mV. The input impedance is programmable from 1 Ω to 600 Ω to achieve maximum power extraction. A novel delay line circuit controls the stepwise gate-drive timing, programmable input impedance, and hibernation behavior. Bipolar input voltage is supported by using a flyback converter topology with two secondary windings. A generated power good signal enables the

load when the output voltage has charged above 2.7 V and disables when the output voltage has discharged below 2.5 V. The DC-DC converter was used in a thermoelectric energy harvesting system that effectively harvests energy from small indoor temperature fluctuations of less than 1°C. To aid in efficiency optimization, an analytical model with unprecedented accuracy of the stepwise gate-driver energy consumption was developed. A test fixture that can accurately measure the efficiency, input impedance, and quiescent power consumption of the DC-DC converter was designed and utilized. Lastly, a method for characterizing the leakage current of capacitors was developed so that capacitors of the lowest leakage can be selected for the DC-DC converter output energy storage.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I would like to thank Nick Purcell and James Stevens for their help with winding the flyback transformers, Matthew Dillingham for help assembling the circuit boards, and Body Mahoney for all of his help with getting the CAD software working. I would like to thank Visvesh Sathe for helping with literature search and manuscript review and Jay Rajagopalan for design and manuscript review. I would like to thank my advisor Josh Smith for accepting me as a student, helping me navigate the world of academia, and patiently supporting my work. I would like to thank my previous advisors Kai Strunz and Brian Otis for encouraging me to start this endeavor so many years ago and introducing me to power electronics and integrated circuit design. Lastly, I would like to thank my wife, Ngocman Carlson, for winding that first transformer, helping with the chip photographs, and helping me get the time and motivation to complete this endeavor.

DEDICATION

To Ian:

May this be inspiration to pursue your passion.

Chapter 1.
INTRODUCTION

In recent years, many works have proposed using thermoelectric generators (TEGs) [1], [2] to power wireless devices from heat sources. Some describe using active heat sources such as the human body [3]–[7], trees [8]–[9], or vehicles [10]–[11]. Others have demonstrated that power can be harvested from the temperature differences that exist between air and structures [12], rocks [13], or soil [14]–[16] due to diurnal fluctuations in air temperature, as the temperature of a mass lags that of the air due to thermal storage. The mass for the thermal storage can be integrated within the energy harvesting unit as done in [17]. Even indoors there is a small amount of thermal energy available from room temperature fluctuations. This dissertation presents a circuit that can efficiently harvest and store this energy.

A TEG produces a voltage V_{TEG} that is proportional to the temperature difference across it ΔT, so for the proposed system, the voltage produced by the TEG is small in magnitude and fluctuates in polarity. TEGs can be placed in series electrically to produce more voltage at the expense of higher resistance R_{TEG} as done in [17] and [18], but at some point adding more TEGs becomes impractical. Pairing the TEG with a step-up DC-DC converter enables harvesting energy when ΔT and V_{TEG} are very low. The minimum TEG voltage that can be utilized invariably becomes limited by the DC-DC converter efficiency. Therefore, a DC-DC converter that can efficiently step up very small voltages of fluctuating polarity is needed.

The DC-DC converter with the lowest reported operational input voltage [6] requires at least 3.5 mV and does not work with negative voltages from the TEG, while the converter with the lowest bipolar operating voltage [19] requires ±10 mV. This work [20] proposes a step-up flyback

DC-DC converter that has a minimum input voltage of ±0.5 mV—twenty times lower than the state of the art. This extremely low input voltage is achieved by utilizing an adiabatic stepwise gate-drive technique that reduces the energy required to drive the gate of the primary power FET M_1 (the dominant source of energy losses) by 82%. Although stepwise gate-drive for inductive DC-DC converters was theorized in [21], until now it was not physically demonstrated in this application. The challenge with successfully implementing a beneficial stepwise gate driver is that the energy required to control the timing signals for each step must not negate the energy savings that stepwise gate-drive provides. To address this, a novel low-power delay line circuit was developed to provide the timing signals for the stepwise gate driver.

The DC-DC converter also needs to be able to match to the source resistance R_{TEG} of the TEG for maximum power extraction. The TEG resistance R_{TEG} is specific to the material properties of the TEG, the number of TEGs in series, and to the thermal impedance between the TEG and the environment. Making the DC-DC converter input impedance programmable from 1 Ω to 600 Ω allows it to be optimized for a wide range of TEG configurations, including many TEGs in series. This is done by leveraging the novel delay line circuit to also set the switching frequency with lots of programmability.

Because the control circuitry cannot operate on just 1 mV, the converter must derive its power supply from its own output. As long as the amount of converted energy per cycle exceeds the power required by the control circuitry, gate drivers, and leakage (including storage capacitors), the output voltage will remain high enough to maintain functionality. If the input power remains too low for too long, then the output voltage will discharge below the minimum level required for operation. Works such as [6], [19], [22], [23], [25], [26], [27] use self-start techniques to recover after this happens. The lowest self-start voltage reported was 5 mV [27] and requires special startup

circuitry. In this work, with the typical operating voltage of just ±1 mV, the need for self-start is avoided by putting the DC-DC converter into a low-power hibernation state that sustains V_{OUT} for several weeks when there is insufficient power available from the TEG. A timing-based technique determines when the input voltage is too low to sustain operation, at which point the switching frequency—controlled by the novel delay line—is reduced to just 0.2 Hz, reducing the total quiescent power to just 255 pW, including capacitor leakage.

1.1 Energy Harvesting System

The energy harvesting system, shown in Figure 1.1, consists of a thermoelectric generator (TEG) that harvests power from environmental temperature differences, a load circuit such as a wireless device that utilizes the power generated from the TEG, and a DC-DC converter that converts the power from the TEG to a voltage that is usable by the load.

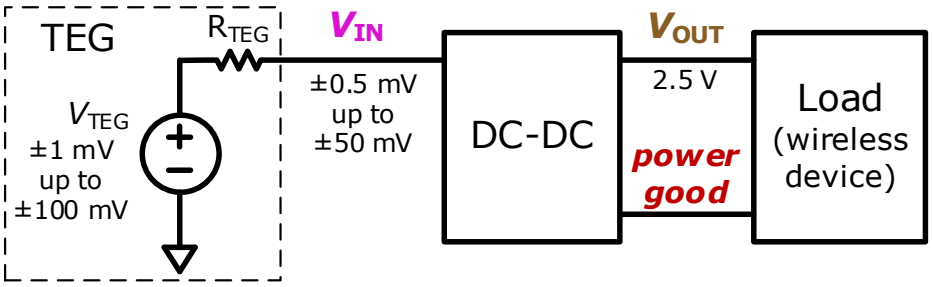

Figure 1.1. Energy harvesting system diagram.

1.2 The Thermoelectric Generator

A thermoelectric generator (TEG) [1], [2], [28], [29], shown in Figure 1.2 is a device that utilizes the Seebeck effect [30] to generate a voltage from a temperature difference across its two faces. Heat exchangers [1] are used to thermally couple each face to thermal reservoirs of different

temperatures. In applications such as [8]–[17], one side is coupled to the ambient air through a heat sink and the other side is coupled to a heat (or cold) source. Throughout the literature, many different heat sources have been paired with a TEG to generate electrical power. In [10], a vehicle exhaust pipe is used as the heat source. In [8] and [31], the trunk of a tree was used as the heat source. The tree trunk temperature was found to be somewhat regulated while the ambient air temperature fluctuates [32]. In [12], it is demonstrated that the "heat" source can be no more than a passive object with sufficient thermal mass. Since ambient air temperature naturally fluctuates diurnally, objects with substantial thermal capacity such as a concrete wall will have a temperature that lags that of the air, thereby creating a temperature difference that can be utilized for thermal energy.

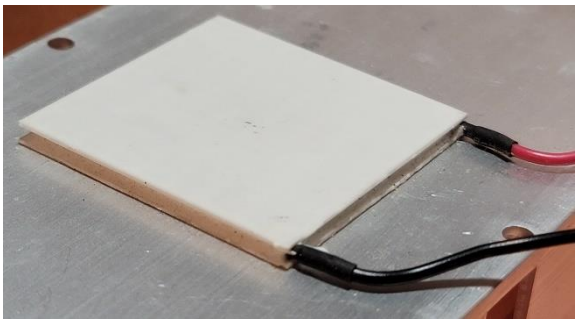

Figure 1.2. Photograph of a typical thermoelectric generator.

The output voltage of the TEG is directly proportional to the temperature difference between the faces of the TEG. This is shown in Figure 1.3. The plot shows the open-circuit output voltage of a typical TEG versus the temperature difference ΔT between the "hot" face and "cold" face as measured in [33]. The relationship is linear for practical values of ΔT and the slope is called the Seebeck coefficient [17], [33]. The slope in Figure 1.3 shows a Seebeck coefficient of $\alpha_s = 37$ mV/°C.

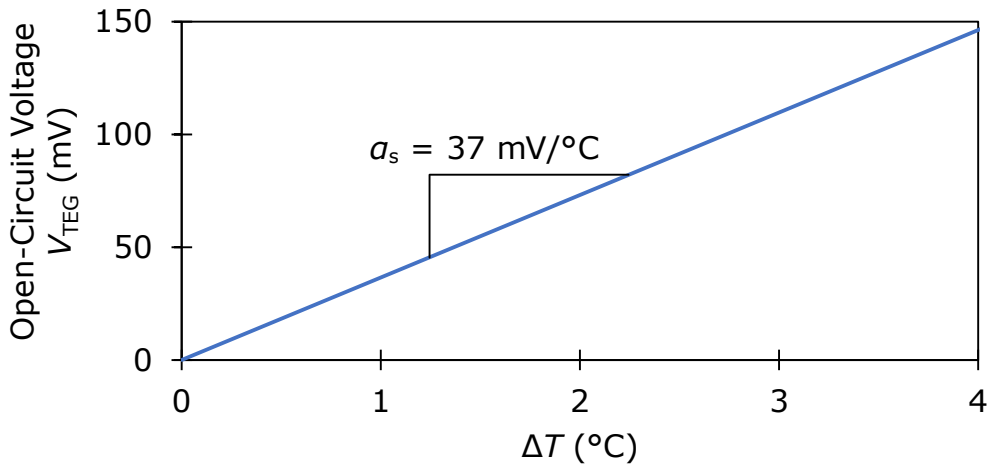

Figure 1.3. Open circuit voltage (V_{TEG}) vs. temperature difference ΔT for a typical thermoelectric generator. The cold-side temperature is held at 22°C. Data source: [33].

Although not shown in Figure 1.3, the relationship between V_{TEG} and ΔT continues in the negative direction, i.e. V_{TEG} is negative when the "hot" face becomes colder than the "cold" face. Figure 1.4 shows this by extrapolating the data from Figure 1.3 for negative ΔT. This means that to be able to extract power from the TEG under all conditions the DC-DC converter connected to the TEG must be able to utilize both positive and negative input voltages.

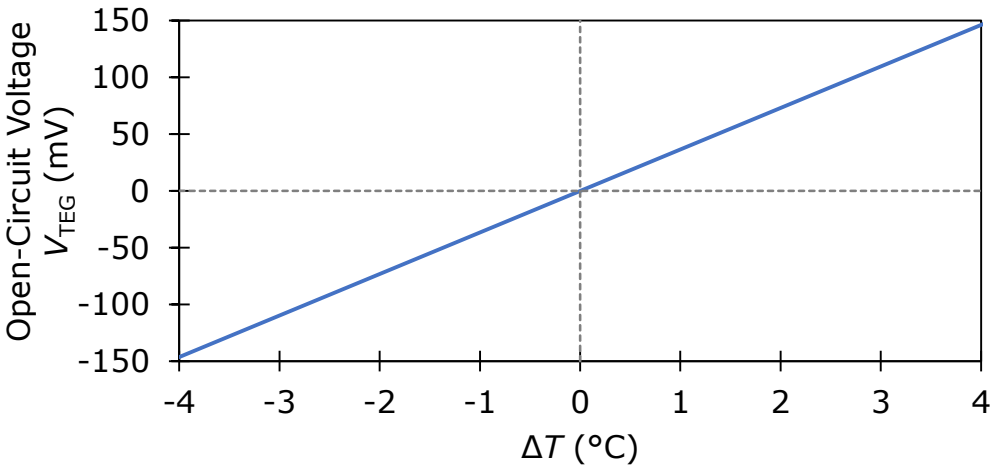

Figure 1.4. Open circuit voltage (V_{TEG}) vs. temperature difference ΔT from Figure 1.3 extrapolated to negative ΔT.

To extract the maximum possible power from a TEG, there is an optimal amount of current to draw from the TEG for a given hot-side and cold-side temperature. Figure 1.5 shows the load line (I-V) curves of a typical TEG. Here, "TEG output voltage" (or $V_{TEG,Out}$) is the voltage between the TEG terminals, which will also be the input voltage (V_{IN}) of the DC-DC converter. The TEG output voltage when the TEG load current is 0 A is equal to the TEG open-circuit voltage V_{TEG}, and the TEG output voltage drops linearly with TEG output current, behaving like a Thevenin voltage source and Thevenin resistance like in the model shown in Figure 1.6. Maximum power is extracted from the TEG when the current drawn from the TEG is such that the TEG output voltage is equal to half the open-circuit voltage. This can be achieved by loading the TEG with an equivalent resistance equal to the TEG source resistance R_{TEG} as an impedance match.

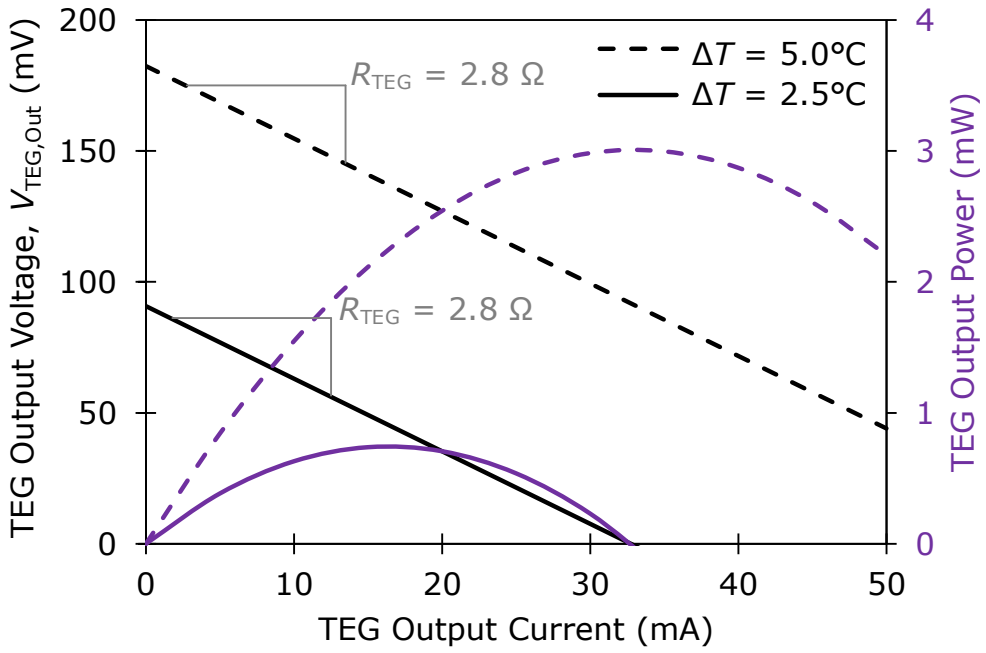

Figure 1.5. I-V and output power curves of a typical thermoelectric generator. Data source: [33].

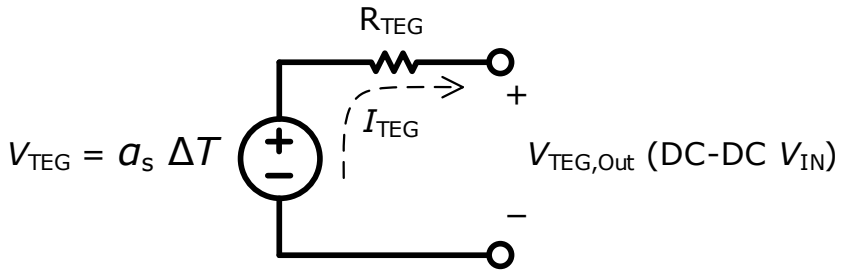

Figure 1.6. Thermoelectric generator (TEG) equivalent circuit model.

Using the TEG model in Figure 1.6, the TEG output voltage is

$$V_{\mathrm{TEG,Out}} = V_{\mathrm{TEG}} - R_{\mathrm{TEG}} I_{\mathrm{TEG}} = \alpha_s \Delta T - R_{\mathrm{TEG}} I_{\mathrm{TEG}}, \quad (1.1)$$

where α_s is the Seebeck coefficient of the TEG. The output power of the TEG is

$$P_{\mathrm{TEG,Out}} = V_{\mathrm{TEG,Out}} I_{\mathrm{TEG}} = (V_{\mathrm{TEG}} - R_{\mathrm{TEG}} I_{\mathrm{TEG}}) I_{\mathrm{TEG}}. \quad (1.2)$$

It is up to the DC-DC converter to draw the appropriate amount of current from the TEG such that maximum power is extracted from the TEG. This is referred to maximum power-point tracking, (or MPPT) and can be achieved by designing the DC-DC converter to have a constant input impedance that matches R_{TEG} [5].

1.3 The DC-DC Converter

In order to utilize the voltage supplied by a TEG, a power conditioning circuit is needed to convert the voltage to a level that is usable by the load circuit and store the harvested energy. Since the voltage from a TEG is proportional to temperature difference across it, a typical energy harvesting application could see a wide range of voltages supplied by the TEG, including negative voltages. Therefore, a DC-DC converter [34] is used to take the TEG voltage as an input (V_{IN}) and output a regulated voltage (V_{OUT}) that can be used by the load circuit. If the TEG voltage were consistently higher than the desired output voltage such as when the TEG is exposed to very high temperature differences as in [11] then the DC-DC converter could be a step-down (buck)

converter or even a linear voltage regulator. However, if a buck converter or linear regulator is used then the DC-DC converter would not be able to harvest power from the TEG when the TEG voltage is less than the desired output voltage. The goal of this work is to harvest energy from a TEG voltage that is much less than the output voltage, so a step-up DC-DC converter is needed. The most basic step-up DC-DC converter is a boost converter like in [3], but a boost converter inherently does not support bipolar input voltages (input voltages of positive and negative polarity). A boost converter also has some efficiency challenges when the input voltage is much less than the output voltage. A flyback converter topology was chosen to best accommodate these design challenges, as will be detailed in Chapter 2.

1.4 THE CMOS LEAKAGE PROBLEM

As explained in [3], for DC-DC converters designed for very low input voltages, the primary power FET that is in the input path becomes the dominant source of power losses. The losses due to this power FET are primarily from the conduction losses due to the FET channel resistance and the switching losses due to periodically driving the power FET gate capacitance. Typically, the designer balances these losses at a chosen operating point for maximum efficiency. To reduce these losses, the switching frequency can be reduced. However, to keep the power the same, the amount of energy transferred through the DC-DC converter per switching cycle would need to increase accordingly. This requires an increase of the (already large) inductor and input capacitors to accommodate the increased energy per cycle. Another way to address these losses is to fabricate the power FET in an advanced short channel-length CMOS process that has a very low gate-charge energy for a given channel resistance. The problem with using such a process is that losses due to leakage currents can exceed the savings from lower gate capacitance [35]. In CMOS processes below 180-nm, gate leakage of the power FET alone can exceed the capacitive losses for the

application proposed in this work. Therefore, this work proposes to fabricate the DC-DC converter in a low-leakage 600-nm CMOS process and reduce the gate-drive losses by driving the power FET gate with an adiabatic stepwise gate driver.

1.5 Design Targets

The goal of this work was to create a DC-DC converter for energy harvesting that sets a new state-of-the-art in the following criteria:

- Support bipolar input voltage from the TEG
- Greater than 60% efficiency at $|V_{IN}| = 1$ mV
- Greater than 0% efficiency at $|V_{IN}| = 0.5$ mV
- A nominal output voltage of $V_{OUT} = 2.5$ V to support common transceiver voltage requirements
- A minimum functional output voltage of $V_{OUT} = 1.5$ V
- A *power good* signal that:
    - Informs the load circuit when the output voltage has charged to the appropriate level and is ready to deliver power
    - Disables the DC-DC converter when the output voltage has charged above 2.8 V to protect devices from excessive voltage
- 100 pA quiescent current (250 pW) quiescent power at $V_{IN} = 0$ mV, $V_{OUT} = 2.5$ V
- A programmable input impedance of 1 Ω – 600 Ω to match to a wide range of TEG source impedances
- A circuit board area of 50 cm^2

1.6 ORGANIZATION

This dissertation is organized as follows:

- Chapter 2: Provides an overview of the DC-DC converter architecture, topology, and high-level design decisions.
- Chapter 3: Explains the theory of stepwise adiabatic charging, provides an analytical model of the stepwise driver energy consumption, and presents the circuitry that controls the stepwise driver.
- Chapter 4: Discusses additional DC-DC converter Features: Active rectification (zero-current-switching), input voltage detection, and output voltage monitoring.
- Chapter 5: Describes efficiency optimization of the DC-DC converter, including the stepwise driver.
- Chapter 6: Describes the integrated circuit (IC) layout and printed circuit board (PCB) design.
- Chapter 7: Discusses the hardware test and characterization methodologies, including DC-DC converter efficiency, quiescent current, and input impedance, as well as capacitor leakage measurements. Also discusses methods for waveform capture.
- Chapter 9: Shows the deployment of the DC-DC converter in a complete energy harvesting system.
- Chapter 10: Concludes this dissertation and proposes ideas for future work.

Chapter 2.
DC-DC CONVERTER ARCHITECTURE

The proposed DC-DC converter block diagram is shown in Figure 2.1. A flyback transformer with a 1:20 turns ratio is used to transfer power from the input V_{IN} to the output V_{OUT}. An additional secondary winding of opposite polarity enables bipolar operation. The converter operates in discontinuous conduction mode (DCM), with a constant but programmable switching frequency. The internal V_{DD} power supply comes from the DC-DC converter output, V_{OUT}.

The primary power FET M_1, with a resistance of 34 mΩ and gate capacitance of 250 pF, is the most significant source of power losses in the circuit. A stepwise gate driver drives the M_1 gate adiabatically to reduce these losses. It drives the gate voltage v_{G1} with a staircase pattern of nine steps (only three steps are shown in Figure 2.1). The stepwise switch drivers generate staggered pulses that drive the switches S_R/S_F in the stepwise gate driver to create the stepwise waveform for the gate voltage v_{G1}.

The delay line circuits provide the edges that set the timing for the pulsed outputs of the stepwise switch controllers. In addition to providing the stepwise timing signals, the slow delay line sets the switching frequency and on-time for M_1. An output of the slow delay line feeds back to the reset input of the slow delay line, making an oscillator that sets the DC-DC converter switching frequency. A mux selects which delay line output is used for the switching frequency, allowing 64 different switching frequencies ranging from 350 Hz to 0.6 Hz, externally programmable with the 6-bit frequency set. The chosen frequency sets the input impedance of the DC-DC converter, ranging from 1 Ω to 600 Ω. A 65th output from the slow delay line is selected when the DC-DC converter enters the hibernate state, lowering the switching frequency to 0.2 Hz.

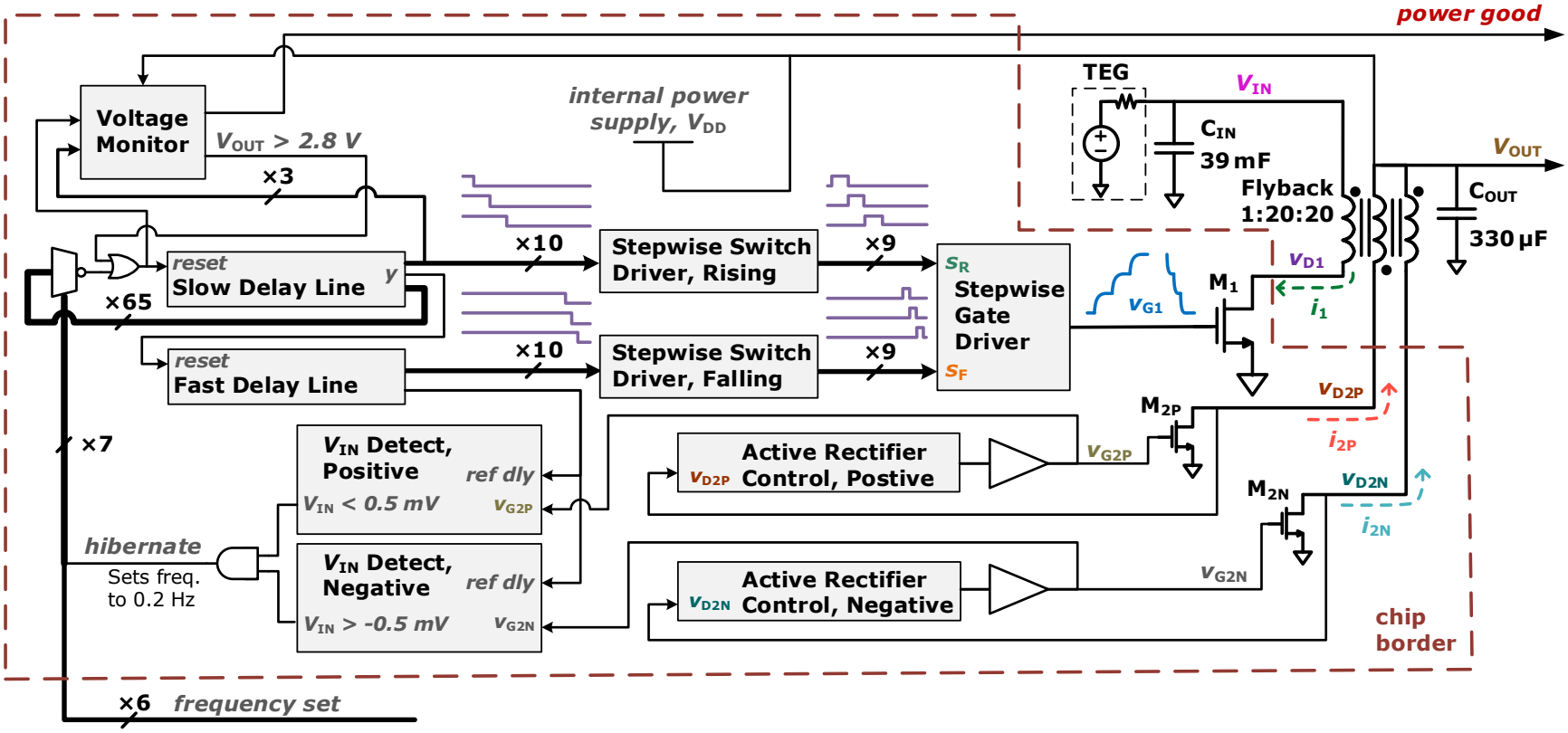

Figure 2.1. DC-DC converter block diagram. © 2023 IEEE

The secondary power FETs M_{2P} and M_{2N} are used as active rectifiers with zero-current-switching. The V_{IN} detect circuits compare the time that secondary power FETs M_{2P} and M_{2N} are conducting against a reference delay that is generated by the fast delay line. This is used to detect whether $|V_{IN}|$ is less than 0.5 mV. When $|V_{IN}|$ is detected to be less than 0.5 mV, the converter is put into the hibernate state.

A voltage monitor circuit provides a power good signal like in [36] that goes high when V_{OUT} has charged above 2.7 V and it stays high until V_{OUT} drops below 2.5 V. It operates at a very low duty cycle when power good is low to conserve power. Switching of M_1 is stopped when $V_{OUT} > 2.8$ V to avoid excessive voltages.

The circuit is implemented in a 600-nm CMOS process, chosen for its very low-leakage-current properties. This allows the quiescent current that the DC-DC converter draws from its own output while in hibernation mode to be limited to just 100 pA (including the leakage of the 330 μF C_{OUT}). Since 600-nm CMOS devices require a relatively large gate charge (for a given on-state channel resistance) to switch on/off compared to devices fabricated in CMOS process nodes of smaller feature sizes, the adiabatic stepwise gate driver compensates for this by substantially reducing the energy required to drive the gate of M_1.

2.1 DC-DC Converter Topology Considerations

There are many DC-DC topologies that can be used to step up voltage. One option would be a switched capacitor circuit such as in [37], but using a switched capacitor circuit to step up a voltage from 1 mV to 2.5 V would require a large number of conversion stages. An inductive architecture can theoretically achieve any step-up ratio in just one conversion stage. The simplest form of inductive architecture is a single-inductor boost converter as in [3]. The two main problems with the single-inductor boost converter are poor efficiency for very low input voltages and

difficulty supporting bipolar inputs. These two problems are solved by using a flyback converter topology.

2.1.1 *Efficiency considerations*

For very low V_{IN}, the conversion losses in a boost converter are dominated by the resistance, gate capacitance, and drain capacitance of M_1 [3]. The resistance of M_1 can be reduced by increasing the channel width at the expense of higher capacitive losses. The losses due to gate capacitance can then be reduced by using stepwise gate-drive. However, losses due to drain capacitance are difficult to address using a simple boost topology since the drain node v_{D1} must charge from 0 V to V_{OUT} for each cycle. Zero-voltage-switching (ZVS) techniques [38] reduce these losses, but only to an extent. If the energy required to charge the drain node capacitance exceeds the energy stored in the inductor, then v_{D1} will not be able to charge up to V_{OUT} and no current would flow to the output. The energy required to charge the drain node capacitance on a boost converter is

$$E_{C,D1} = \frac{1}{2} C_{D1} \hat{V}_{D1}^2, \tag{2.1}$$

where C_{D1} is the total capacitance on the drain node and $\hat{V}_{D1}$ is the peak voltage of v_{D1}. For a boost converter, $\hat{V}_{D1} = V_{OUT}$.

Another source of losses in a boost converter is the energy consumed during the transition of M_1 from the "on" state to the "off" state—referred to here as "transition losses". These losses are only significant when the falling edge of gate voltage v_{G1} is slow, such as when stepwise gate drive is used. If v_{G1} transitions from V_{DD} to 0 V before v_{D1} has risen significantly, then there is little power lost. If v_{G1} transitions slowly, then M_1 will spend time in a region of operation where the channel current is low enough such that the drain voltage v_{D1} is rising, but current is still being

conducted through the channel—causing transition losses [39]. These transition losses are separate from the energy that gets stored in the power FET drain capacitance. To calculate the transition losses from simulation data, the power p_1 flowing into the drain of M_1 is integrated across the time that the transition occurs. Then the portion of that energy that goes into charging the drain capacitance and the energy associated with standard conduction losses are subtracted out. The energy that remains are the transition losses:

$$E_{\text{Tran-Loss}} = \int_{T_1}^{T_3} p_1 dt - E_{\text{C,D1}} - \hat{I}_1^2 R_{\text{on1}}(T_2 - T_1), \tag{2.2}$$

where

$$p_1 = i_1 v_{\text{D1}}, \tag{2.3}$$

i_1 is the current through M_1, $\hat{I}_1$ is the peak value of i_1, and R_{on1} is the resistance of the channel of M_1 while v_{G1} is highest. T_1 and T_3 are the times that v_{G1} starts and ends the transition from high to low ($T_3 - T_1 = T_{\text{F}}$, the v_{G1} fall-time). T_2 is the time that v_{G1} crosses the threshold voltage of M_1, where the channel current becomes effectively zero. Transition losses during the rising edge of v_{G1} are generally negligible for a converter operating in DCM because, at M_1 turn-on, i_1 is initially zero and ramps up slowly due to inductance. There are no losses when the current is zero. Transition losses at turn-on would only be significant if the v_{G1} risetime T_{R} was comparable to that of the inductor current risetime $T_{\text{i1,rise}}$. Therefore, T_{R} can be much longer than T_{F}.

To address the drain capacitance losses and transition losses associated with a boost converter, a flyback topology is used. By using a flyback transformer in place of a single inductor, the peak $\hat{V}_{D1}$ of the drain voltage v_{D1} can be reduced by the turns ratio N_{t} of the flyback transformer:

$$\hat{V}_{\text{D1}} = V_{\text{IN}} + \frac{V_{\text{OUT}}}{N_{\text{t}}}. \tag{2.4}$$

This in turn reduces the energy required to charge the drain node capacitance per (2.1) and the transitions losses per (2.2), (2.3). To illustrate the transition losses, Figure 2.2 shows the current, voltage, and power waveforms for M_1 during a very slow v_{G1} high-to-low transition. It shows that the power p_1 flowing into M_1 with a 1:2 flyback transformer is lower compared to a boost converter, while a 1:1 flyback transformer does not provide the same benefit. A higher turns ratio reduces transition losses caused by a slow v_{G1} slew rate. Figure 2.3 shows the simulated relationship between transition losses and the time v_{G1} takes to transition from 2.5 V to 0 V. In this simulation, v_{G1} was transitioned linearly rather than in a stepwise fashion.

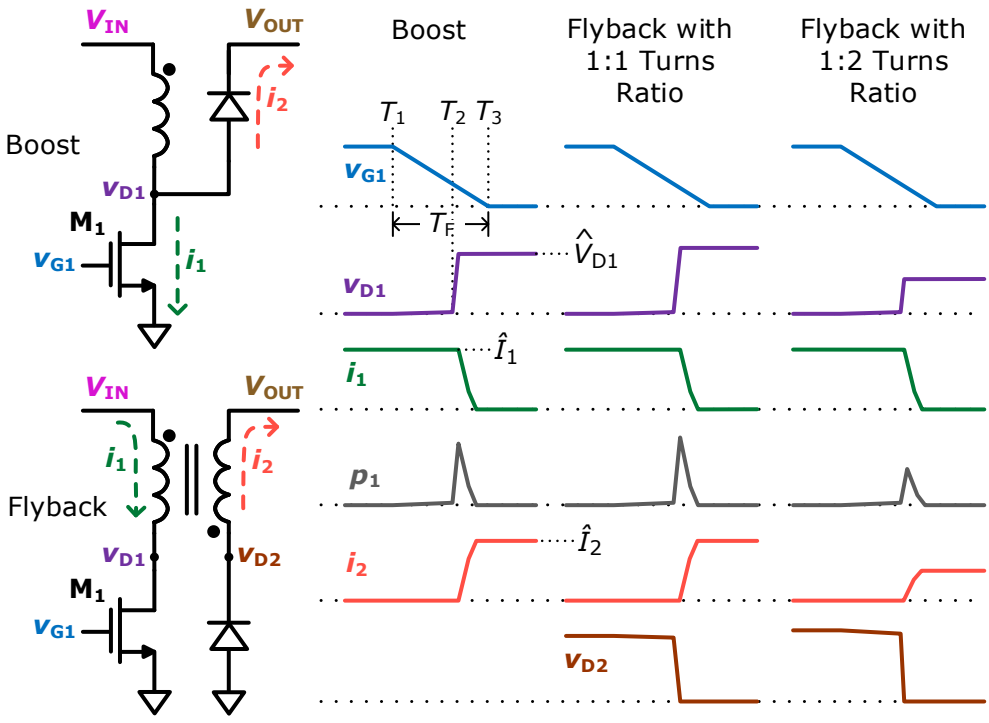

Figure 2.2. Demonstrating the reduced transition losses when using a flyback converter.

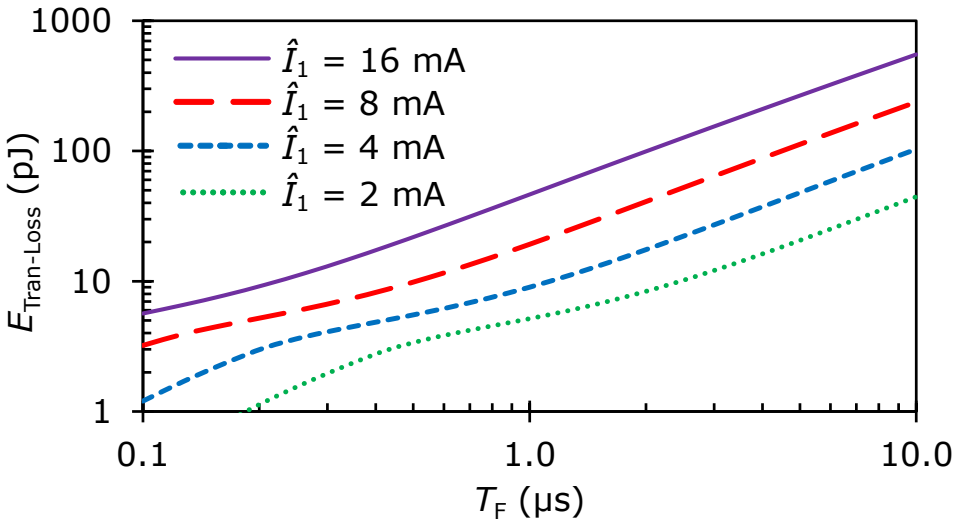

Figure 2.3. Simulated M_1 transition losses vs. gate voltage transition time T_F.

Using a flyback topology does introduce a new switching node v_{D2} that still must swing from 0 V to V_{OUT}, but in the proposed DC-DC converter the capacitance on node v_{D2} is much less than the capacitance on v_{D1}. This is because the transformer secondary current i_2 is much lower than the primary current i_1 and the duration that i_2 flows ($T_{i2,fall}$) is less than the duration that i_1 flows ($T_{i1,rise}$). So, the rectifier device can be much smaller than M_1, with much higher resistance and lower capacitance.

2.1.2 *Supporting a bipolar input*

Since a TEG can produce either positive or negative voltages, the DC-DC converter must support input voltages of either polarity. Alhawari [7] addresses this for a boost converter by using a power FET H-bridge to reverse the polarity, while [19] reconfigures the boost converter to an inverting buck-boost converter for negative V_{IN}. For the proposed application, the additional switches in the input path used in [7] and [19] would require prohibitively large power FETs to keep the total parasitic resistance similar to a single M_1. Cao [26] uses a boost-flyback hybrid

technique where the DC-DC converter acts as a single-coil boost converter for one polarity and as a flyback converter for the opposite polarity. Because this method operates similar to a single-inductor boost converter for positive V_{IN}, it cannot take full advantage of the benefits of a flyback transformer. Bipolar implementations in [25] and [36] require two transformers.

Here, the proposed solution to bipolar input voltage uses one flyback transformer with two secondary windings (or a single center-tapped secondary winding), shown in Figure 2.4. Each secondary winding is dedicated to one input voltage polarity and each has its own rectifier. The rectifier devices can have much higher resistance than M_1 due to conducting less current and for a shorter duration. Therefore, M_1 dominates the losses and the active area of the chip (not including C_{Tank}).

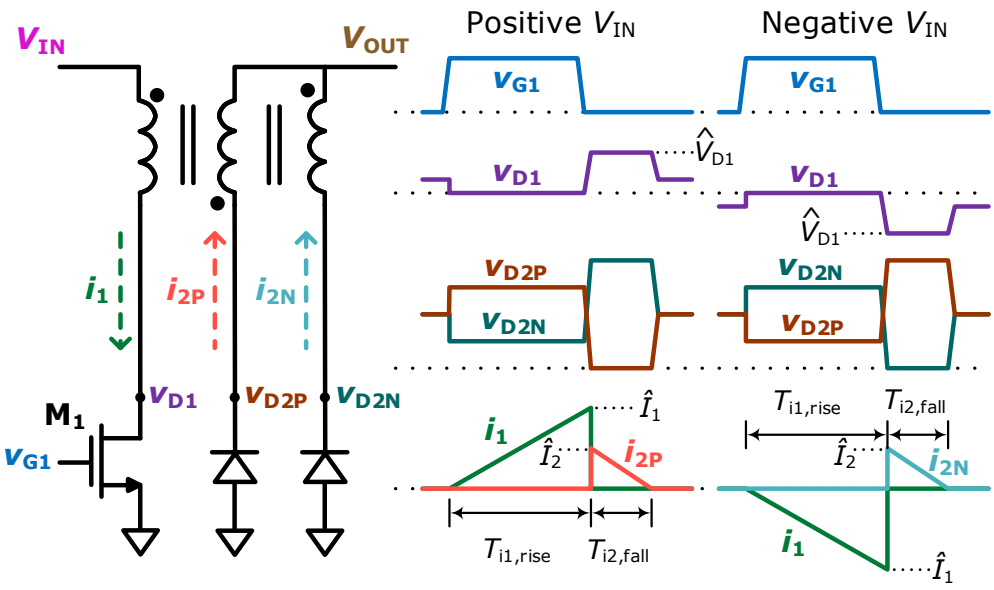

Figure 2.4. Using a flyback transformer with two anti-parallel secondary windings supports a bipolar input. The turns ratio in this illustration is 1:2:2. Rectifier devices M_{2P}/M_{2N} are drawn as diodes for simplicity. © 2023 IEEE

This method of supporting bipolar inputs has two considerations. First, the method only works when the voltage v_{D1} does not exceed the turn-on voltage of the M_1 body diode:

$$v_{\mathrm{D1}} > -V_{\mathrm{Diode}}. \tag{2.5}$$

Rewriting in terms of V_{IN} and V_{OUT} yields

$$V_{\mathrm{IN}} - \frac{V_{\mathrm{OUT}}}{N_{\mathrm{t}}} > -V_{\mathrm{Diode}}. \tag{2.6}$$

This limitation only applies to negative V_{IN} and is mitigated by a large transformer turns ratio N_{t}.

The second consideration is that if either voltage $v_{\mathrm{D2P}}/v_{\mathrm{D2N}}$ goes significantly below 0 V while M_1 is conducting (due to large V_{IN}) then the rectifier diode will conduct and the DC-DC converter will behave like a forward converter as in [40]. Consequently, the inductance of the primary winding will stop limiting the input current and i_1 will increase drastically. This effectively clamps V_{IN} such that

$$|V_{\mathrm{IN}}| < \frac{V_{\mathrm{OUT}}}{N_{\mathrm{t}}}. \tag{2.7}$$

The clamping effect is not catastrophic, but it decreases the DC-DC converter's input impedance, affecting maximum power transfer from the TEG. In this work, the transformer turns ratio was set to $N_{\mathrm{t}} = 20$, avoiding clamping at $V_{\mathrm{IN}} = 50$ mV.

2.2 The Flyback Transformer

The design of the flyback transformer requires the following performance criteria must be considered:

- Transformer size
- Primary coil inductance
- Primary coil saturation current
- Transformer turns ratio
- Primary coil resistance

- Secondary coil resistance

The performance criteria listed above are set by the following transformer design parameters:

- Transformer core dimensions
- Transformer core type
- Number of windings on the primary coil, N_1
- Wire gauge (thickness/diameter) of the primary coil
- Number of windings on the secondary coil, N_2
- Wire gauge of the secondary coil

The process of designing the flyback transformer started with deciding the maximum tolerable physical size and choosing the magnetic core dimensions accordingly. It was decided that a toroid-shaped transformer of 20 mm diameter and 7 mm thickness would be acceptable. Next, a core type was selected. The proposed application for this transformer is relatively low-current, so it benefits to choose a core type that results in the maximum inductance, which comes at the expense of lower saturation current. Higher inductance allows for higher energy transfer per-cycle for a given peak current (when operating the DC-DC converter in DCM). With this, a T38 core type was selected, which has an initial relative magnetic permeability of $\mu_i = 10000$ [41].

Next, the number of turns on the transformer primary coil was determined. The magnetic core datasheet [41] specifies that the coil inductance is

$$L = A_L N_1^{\,2}, \tag{2.8}$$

where $A_L = 9.74\ \mu\text{H/turn}^{0.5}$ (with ±30% tolerance). Although higher inductance is better for DC-DC converter efficiency (for a given peak current), increasing the number of turns will increase the coil resistance and also decrease the saturation current. The peak primary coil current $\hat{I}_1$ was determined by the minimum specified input impedance R_{IN} of the DC-DC converter. With

M_1 switching at a duty ratio of D = 50% (this is the duty ratio at the maximum frequency setting), the necessary peak current is calculated:

$$R_{\mathrm{IN}} = \frac{V_{\mathrm{IN}}}{I_{\mathrm{IN}}}, \tag{2.9}$$

$$I_{\mathrm{IN}} = \frac{1}{2} D \hat{I}_1, \tag{2.10}$$

where I_{IN} is the average input current and is equivalent to the average of i_1. At R_{IN} = 1 Ω (the minimum specified input impedance) and V_{IN} = 50 mV (the maximum specified input voltage), $\hat{I}_1$ is calculated to be 200 mA. Therefore, the saturation current needs to be above 200 mA.

The saturation current is determined by the number of turns in the coil N_1 as

$$\hat{I}_{1,\mathrm{sat}} = \frac{B_{\max} l_c}{\mu_{\mathrm{i}} \mu_0 N_1}, \tag{2.11}$$

where $\mu_0 = 1.26 \times 10^{-6}$ N/A^2 is the permeability of free space, l_{c} is the effective magnetic path length of the core, and $B_{\max}$ is the maximum magnetic flux density of the core at saturation [42]. The effective magnetic path length is given in the core datasheet [41] as l_{c} = 43.55 mm and the maximum magnetic flux density is given in the T38 core material datasheet [43] as $B_{\max}$ = 430 mT at 25°C. Using a target saturation current of $\hat{I}_{1,\mathrm{sat}}$ = 240 mA (10% above the target $\hat{I}_1$ at V_{IN} = 50 mV), the number of turns in the primary coil solves to N = 6. From (2.8), the inductance of the primary coil is calculated to be 350 μH. The actual inductance was measured to be L = 300 μH, which is within the ±30% tolerance specified in the magnetic core datasheet.

After the number of turns in the primary coil was determined, the wire gauge (thickness) was chosen. The thickness of the copper wire used for the coil determines the coil resistance. Lower resistance is better for efficiency and therefore the thickest wire that can be practically wound around the core was chosen. This was determined to be 18 AWG (1.0 mm) wire. This resulted in a resistance of 5 mΩ in the primary coil.

The number of turns in the secondary coil N_2 is determined by the number of turns in the primary coil N_1 and the chosen turns ratio N_t. The optimal turns ratio was discussed in Section 2.1 and determined to be $N_t = 20$. Therefore, the number of windings on the secondary coils is 120 turns for each secondary coil. The wire gauge for the secondary windings was chosen to be as thick as possible to fit on the transformer core without needing multiple winding layers. Multiple winding layers were avoided to minimize parasitic coupling capacitance between the windings. The chosen wire thickness for the secondary coils was 40 AWG (0.08 mm) wire. The resulting resistance of each secondary coil was measured to be 11 Ω.

2.3 Input Capacitor Selection

The DC-DC converter input capacitor C_{IN} serves the role of providing the transient currents to the flyback transformer primary coil. Without C_{IN}, the TEG resistance R_{TEG} would be directly in series with the transformer primary coil. Since R_{TEG} could be on the order of 100s of ohms, the resistance would render the DC-DC converter unusable due to the voltage drop. The goal of C_{IN} is to minimize the ripple on the input voltage V_{IN}. Assuming the worst-case condition were M_1 is operating at a very low duty ratio, a first-order approximation of this ripple voltage is

$$\frac{\Delta V_{IN}}{V_{IN}} = \frac{L}{2C_{IN}} \frac{\hat{I}_1^2}{V_{IN}^2}. \tag{2.12}$$

Assuming a minimum tolerable ripple of $\Delta V_{IN}/V_{IN}$ = 30% (±15%) and using $\hat{I}_1$ = 200 mA at V_{IN} = 50 mV and L = 300 μH results a minimum input capacitance of C_{IN} = 8 mF. However, ripple voltage is not the only concern. Additionally, capacitors have a parasitic equivalent series resistance (ESR) that dissipates power just as the resistance of the transformer coil and the channel resistance of M_1 does. The chosen capacitor was a 2.5 V-rated 3.9 mF aluminum polymer electrolytic capacitor, with an ESR of 8 mΩ [44]. Two of these capacitors in parallel would put

the total capacitance and ESR at acceptable levels. However, since there was plenty of space available on the circuit board, a total of ten capacitors were used, with a total capacitance of 39 mF and a combined ESR of 0.8 mΩ, which ensured that ESR and ripple voltage does not degrade efficiency.

2.4 Output Capacitor Selection

The output capacitor C_{OUT} stores the harvested energy at the DC-DC converter output voltage V_{OUT} until it is ready to be used by the load. It also absorbs the current spikes output by the DC-DC converter after each switching cycle. The minimum tolerable C_{OUT} capacitance is determined by two criteria. The first criterion is the output voltage ripple. V_{OUT} ripple is inherent in the DC-DC converter architecture. It is designed to charge from 2.5 V up to 2.7 V and then dump its charge into the load until V_{OUT} drops below 2.5 V. The load would see an input voltage varying from 2.7 V to 2.5 V. The voltage monitor circuit that provides the *power good* signal after V_{OUT} charges above 2.7 V only samples V_{OUT} once every 32 switching cycles (to save power). Also, the voltage monitor stops the DC-DC converter from switching altogether when V_{OUT} is greater than 2.8 V. If C_{OUT} is too small, then V_{OUT} could charge well above 2.8 V before the voltage monitor samples V_{OUT}. The change in V_{OUT} per switching cycle is determined by

$$\Delta V_{OUT} = \frac{L}{2C_{OUT}} \frac{\hat{I}_1^2}{V_{OUT}} \eta, \tag{2.13}$$

where η is the efficiency of the DC-DC converter. The voltage monitor might be 32 switching cycles away from sampling V_{OUT} when V_{OUT} is as low as 2.7 V. Assuming that V_{OUT} should not be allowed to charge above 2.9 V in 32 switching cycles, this puts the maximum ΔV_{OUT} at 6.3 mV. Using L = 300 μH, $\hat{I}_1$ = 200 mA, V_{OUT} = 2.7 V, and η = 80% results in a minimum tolerable C_{OUT} of 280 μF. C_{OUT} was chosen to be 330 μF to provide additional margin and fill circuit board space.

Leakage currents through the output capacitors are a concern due to the low-power nature of the DC-DC converter. The quiescent current consumption of the DC-DC converter during hibernation is specified at 100 pA. The leakage current of C_{OUT} is included in the total quiescent current budget. Therefore, extremely low-leakage capacitors are needed. Many capacitors were tested for leakage and ultimately the chosen capacitor was a 100 V-rated 47 μF capacitor [45], [46]. Capacitors were tested for leakage individually and the units with the lowest leakage were used in the fabricated circuit. Capacitors from [46] were found to have a lower leakage current on average. Seven 47 μF capacitors were used in the design for a total capacitance of C_{OUT} = 330 μF and a combined leakage current of approximately 50 pA.

Chapter 3.
THE STEPWISE GATE DRIVER

For very low input voltages, the gate-drive of the primary power FET M_1 dominates the losses [3], [4] so reducing those losses allows the DC-DC converter to operate efficiently at lower input voltages. A common approach to reducing these losses is to use a deep submicron CMOS technology with very low FET gate capacitance for a given channel resistance. However, such processes have high leakage currents that result in high static power consumption [35]. Therefore, a low-leakage 600-nm process is used and the gate of M_1 is driven with an adiabatic driver to reduce gate-drive energy. One option would be an inductive resonant gate driver such as in [47], but implementing quality inductors on-chip can be impractical. Alternatively, this paper [48] proposes using the inductor-less stepwise charging technique introduced in [49] and [50] to reduce the gate-drive losses. Stepwise charging has been utilized to reduce power in ADCs [51], [52], clock drivers [53], touch sensors [54], and switched-capacitor DC-DC converters [55] but until now use in inductive DC-DC converters has only been theorized [21] and has not been demonstrated in hardware.

3.1 STEPWISE CHARGING

Stepwise charging involves driving the capacitive load to intermediate voltages in a stepping pattern when transitioning the load voltage v_{Load} from low to high and then from high to low, as shown in Figure 3.1. There are variations of how the intermediate voltages are generated [56]. The focus of this work is on the first and simplest variation, introduced in [49], [50]. The intermediate voltages V_k are held by capacitors $C_{\text{Tank},k}$ which naturally become evenly spaced between 0 V and supply voltage V_{DD} in steady-state, after several step-high/step-low transitions have been

performed [50]. In practice, how evenly-spaced the V_k voltages settle to depends on how large the tank capacitance C_{Tank} is compared to load capacitance C_{Load} and how much time each step is given to settle.

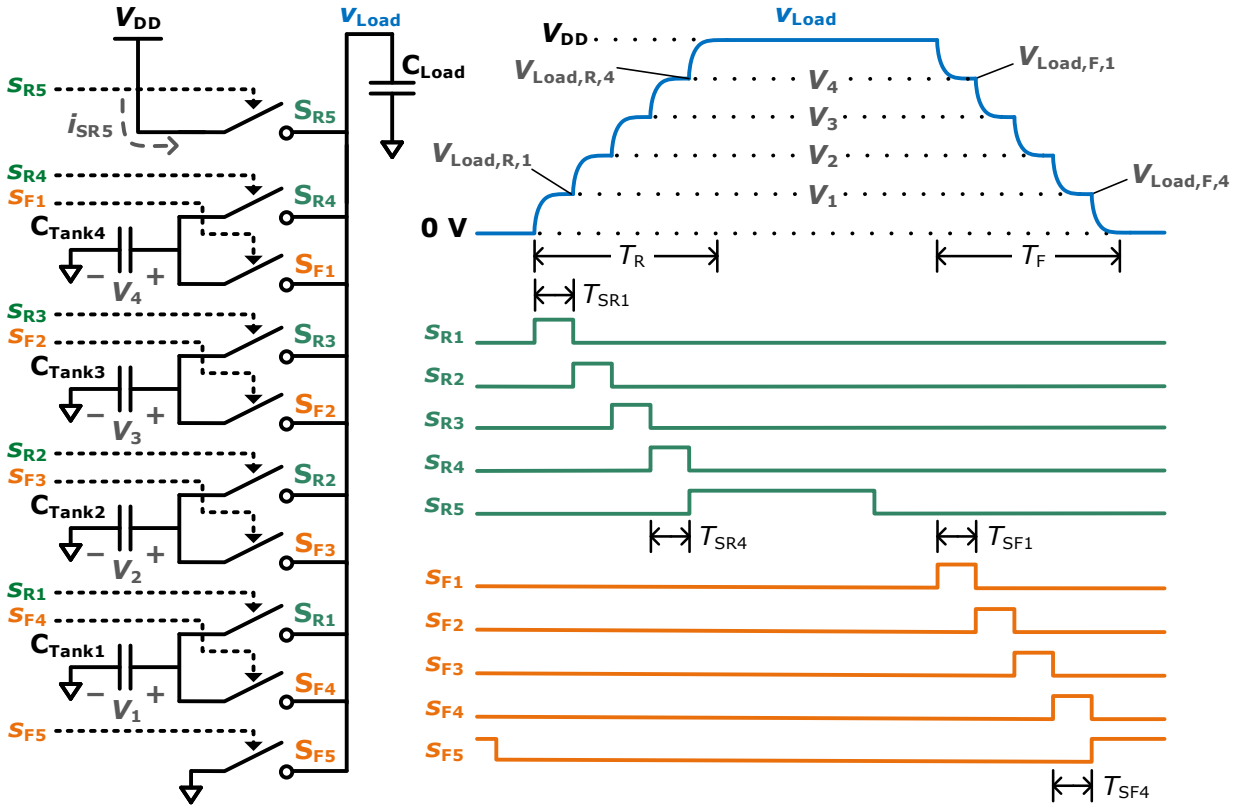

Figure 3.1. Schematic and waveforms of an $N = 5$ stepwise driver.

The number of rising/falling steps in a stepwise driver is defined as N. A stepwise driver has $N - 1$ C_{Tank} capacitors, N rising-edge switches S_{R}, and N falling-edge switches S_{F}. In the application used in this work, the falling-edge switches need to be much lower resistance than the rising-edge switches to enable fast falling transitions to minimize transition losses as described in Section 2.1.1). If the resistance of the switches can be equal, then $S_{\text{R},k}$ and $S_{\text{F},N-k}$ (for $k = 1$ to $N - 1$) can be one and same device as in [49]. The amount of time that each rising step is given to settle is $T_{\text{SR},k}$ and the amount of time that each falling step is given to settle is $T_{\text{SF},k}$. Figure 3.1 shows an $N = 5$

stepwise driver. The v_{Load} voltage at the end of each rising step is defined as $V_{\text{Load,R,}k}$, such that $V_{\text{Load,R,1}}$ is the voltage at the end of the first step and $V_{\text{Load,R,}N}$ is the voltage at the end of the last step. Here, it is assumed that the final step fully settles, such that $V_{\text{Load,R,}N} = V_{\text{DD}}$. $V_{\text{Load,R,0}} = 0$ V is the pedestal—the starting point of the rising edge. The v_{Load} voltage at the end of each falling step is defined as $V_{\text{Load,F,}k}$, such that $V_{\text{Load,F,0}} = V_{\text{Load,R,}N} = V_{\text{DD}}$ and $V_{\text{Load,F,1}}$ is the first falling step. The final falling step, $V_{\text{Load,F,}N}$, is assumed to fully settle, such that $V_{\text{Load,F,}N} = V_{\text{Load,R,0}} = 0$ V.

From [50], in the most ideal case, where $C_{\text{Tank}} >> C_{\text{Load}}$, S_{R} and S_{F} are ideal switches, and all steps fully settle, then the energy consumed by the stepwise driver to complete one charge/discharge cycle is

$$E_{\text{Load-Driver}} \approx C_{\text{Load}} \frac{V_{\text{DD}}^2}{N}. \tag{3.1}$$

A single step driver of $N = 1$ is identical to conventional driver that steps directly from 0 V to V_{DD}. The next section explains how to calculate the $E_{\text{Load-Driver}}$ energy for the non-ideal case.

3.2 Stepwise Driver Energy Consumption Model

In order to properly optimize the design of a stepwise driver, an accurate analytical model of the stepwise driver energy consumption is needed. Prior works [50], [21], [56] provide formulas to model this energy consumption, but all are inaccurate when voltage steps are not given time to fully settle. Park [54] provides the foundation of a model that does not have such a limitation, but stops short of deriving a complete closed-form formula. This section presents a complete closed-form analytical formula for calculating stepwise driver energy that is accurate for any amount of step settling.

This section calculates the amount of energy consumed by a stepwise adiabatic driver—like the one shown in Figure 3.1—based on the following parameters:

- The number of steps: N
- The load capacitance: C_{Load}
- The tank capacitance: C_{Tank}
- The rising-edge switch (S_{R}) resistance: R_{SR}
- The falling-edge switch (S_{F}) resistance: R_{SF}
- The rising-edge switch (S_{R}) on-time: T_{SR}
- The falling-edge switch (S_{F}) on-time: T_{SF}
- The switch quality factor (defines the energy required to turn a switch $S_{\text{R}}/S_{\text{F}}$ on then off, for a given switch resistance $R_{\text{SR}}/R_{\text{SF}}$): ρ

The stepwise driver energy is divided into two parts. The first part is the energy that is dissipated within the switches of the stepwise driver as it drives the load voltage v_{Load} high and then low for one cycle. This energy will be called $E_{\text{Load-Driver}}$ and is the focus of this section. The second part is the energy that is consumed by that circuitry that drives the stepwise switches $S_{\text{R}}/S_{\text{F}}$ for each cycle. This energy is discussed in detail in [50] and is briefly discussed at the end of this section.

To simplify the derivation of $E_{\text{Load-Driver}}$, the following assumptions are made:

- All C_{Tank} are equal.
- T_{SR} is the same for every rising step, except for the final step.
- T_{SF} is the same for every falling step, except for the final step.
- R_{SR} is the same for all rising switches S_{R}.
- R_{SF} is the same for all falling switches S_{F}.
- The final rising step is allowed to fully settle to V_{DD}.
- The final falling step is allowed to fully settle to 0 V.

The stepwise driver energy $E_{\text{Load-Driver}}$ is the total energy dissipated by the switches in the stepwise driver after one cycle. Svensson [50] approximates this energy by integrating the power consumed by each switch while it is on, but is not fully accurate because it assumes that the tank capacitor voltages V_k are uniformly distributed, which is an approximation. Park [54] proposes to instead find the energy that is drawn from the power supply V_{DD}. Since all of the dissipated energy must come from V_{DD}, $E_{\text{Load-Driver}}$ must also equal the energy that flows from V_{DD} on the final rising step:

$$E_{\text{Load-Driver}} = \int_{T_{\text{SR},N,\text{on}}}^{T_{\text{SR},N,\text{off}}} V_{\text{DD}} i_{\text{SR},N}\,, \tag{3.2}$$

where $T_{\text{SR},N,\text{off}} - T_{\text{SR},N,\text{on}} = T_{\text{SR},N}$ are the times that switch $S_{\text{R},N}$ turns off (opened) and on (closed), and $i_{\text{SR},N}$ is the current that flows through $S_{\text{R},N}$ while it is conducting. $S_{\text{R},N}$ is the only switch connected to V_{DD}. Equation (3.2) can be re-written in terms of the total charge that flows from V_{DD} through $S_{\text{R},N}$ per cycle:

$$E_{\text{Load-Driver}} = V_{\text{DD}} Q_{\text{SR},N}, \tag{3.3}$$

where $Q_{\text{SR},N}$ is the charge that flows from V_{DD}, through the final rising-edge switch $S_{\text{R},N}$, and to C_{Load} on the final rising step, such that:

$$Q_{\text{SR},N} = C_{\text{Load}}\left(V_{\text{Load},R,N} - V_{\text{Load},R,N-1}\right), \tag{3.4}$$

where $V_{\text{Load,R,N}} = V_{DD}$ is the resting voltage of the final rising step (step N) of the load voltage v_{Load}. $V_{\text{Load,R,N-1}}$ is the resting voltage of the second-to-last rising-edge step and it is the step that connects to the highest C_{Tank} capacitor: $C_{\text{Tank},N-1}$. In the case that the final rising step is given enough time to fully settle to the final value (V_{DD}) the energy becomes

$$E_{\text{Load-Driver}} = C_{\text{Load}} V_{\text{DD}}\left(V_{\text{DD}} - V_{\text{Load,R},N-1}\right). \tag{3.5}$$

To find $E_{\text{Load-Driver}}$, $V_{\text{Load,R,N-1}}$ must be determined. Park [54] provides some of the equations required to solve for $V_{\text{Load,R,}N\text{-1}}$, but stops short of deriving a final solution. The first step in finding $V_{\text{Load,R,}N\text{-1}}$ is to define terms r (for rising-edge) and f (for falling-edge), which represent the percentage that each step reaches the average of the voltage of the $C_{\text{Tank},k}$ capacitor that is being stepped into V_k, defined as:

$$r_k := \frac{V_{\text{Load,R},k} - V_{\text{Load,R},k-1}}{V_k - V_{\text{Load,R},k-1}}, \tag{3.6}$$

$$f_k := \frac{V_{\text{Load,F},k} - V_{\text{Load,F},k-1}}{V_{N-k} - V_{\text{Load,F},k-1}}, \tag{3.7}$$

for $0 < k < N$ and such that $0 < r < 1$ and $0 < f < 1$. The analysis that follows will assume that r and f are equal for all steps k (except for the final rising step r_N and the final falling step f_N, which equal 1):

$$r = r_k, \tag{3.8}$$

$$f = f_k. \tag{3.9}$$

For an ideal stepwise driver (where $C_{\text{Tank}} >> C_{\text{Load}}$ and each step is given time to fully settle), $r = f = 1$. There are two reasons why r and f will be less than one. First, due to the RC settling time constant τ_R/τ_F, the switch S_R/S_F might open before v_{Load} fully settles. Second, charge redistribution between C_{Load} and C_{Tank} will cause the voltage v_k across capacitor $C_{\text{Tank},k}$ to have ripple ΔV_k. Even if the v_{Load} step fully settles such that $v_{\text{Load}} = v_k$, at the end of the step v_k will be less than the average $C_{\text{Tank},k}$ voltage V_k due to this ripple. Figure 3.2 illustrates the charging behavior of one step k, while Figure 3.3 illustrates the discharging behavior for one falling step $N - k$. The dashed lines represent what the settled voltages would be if switches $S_{R,k}$ ($S_{F,N\text{-}k}$) never opened and $S_{R,k+1}$ ($S_{F,N\text{-}k+1}$) never closed.

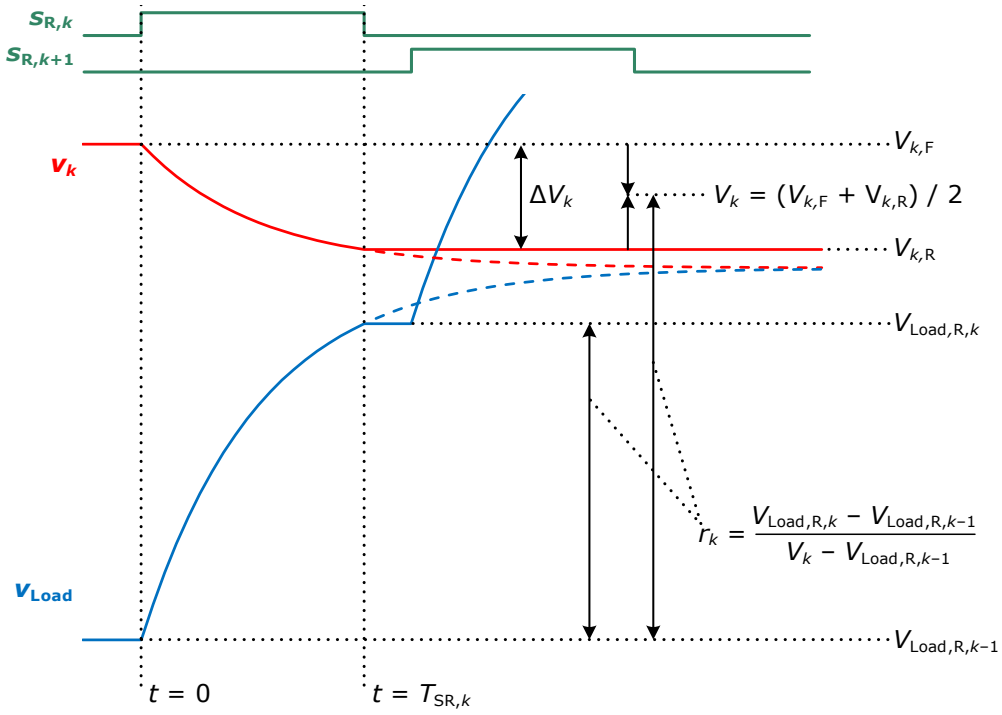

Figure 3.2. Waveforms of the load voltage v_{Load} and $C_{\text{Tank},k}$ capacitor voltage v_k, for one rising step k.

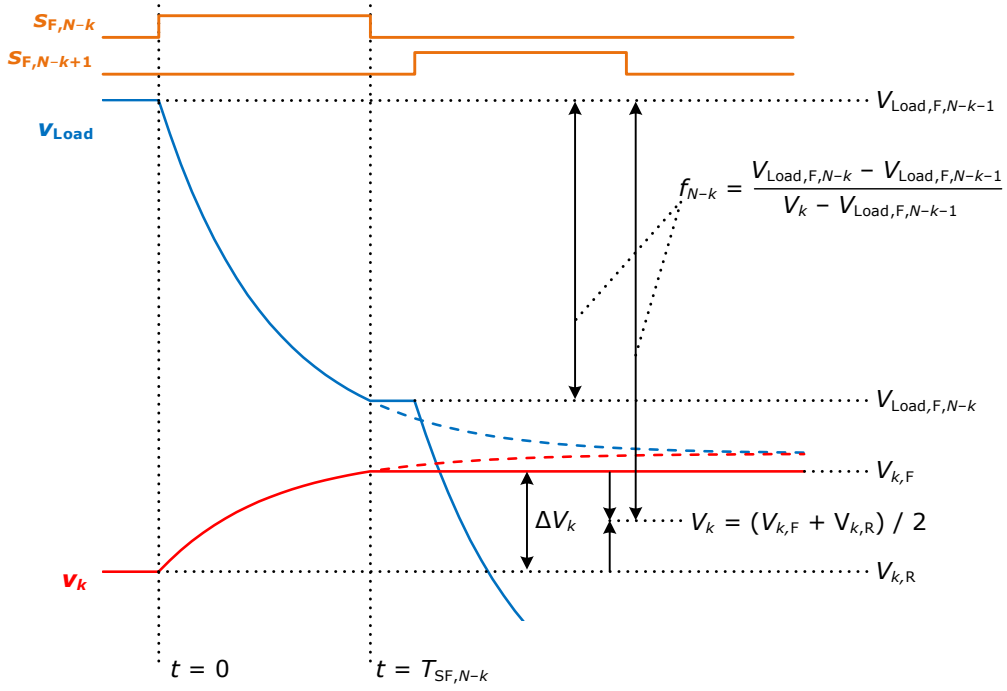

Figure 3.3. Waveforms of the load voltage v_{Load} and $C_{\text{Tank},k}$ capacitor voltage v_k, for one falling step $N - k$.

The voltage across capacitor $C_{\text{Tank},k}$ is defined as v_k for the continuous time voltage, and V_k for the average of v_k. However, it is very important to recognize that V_k is not the average of v_k across time. Instead, it is the average of two discrete voltages: the final voltage after rising step k completes, $V_{k,\text{R}}$, and the final voltage after falling step $N - k$ completes, $V_{k,\text{F}}$:

$$\Delta V_k := V_{k,\text{F}} - V_{k,\text{R}}, \tag{3.10}$$

$$V_k := \frac{V_{k,\text{F}} + V_{k,\text{R}}}{2}. \tag{3.11}$$

For rising steps, the load voltage at the beginning of a step ($t = 0$), when the switch $S_{\text{R},k}$ first closes is equal to the final voltage of the previous step, right after switch $S_{\text{R},k\text{-}1}$ opens:

$$v_{\text{Load},(t=0)} = V_{\text{Load,R},k-1}. \tag{3.12}$$

The $C_{\text{Tank},k}$ voltage that is connected to the load through $S_{\text{R},k}$ at $t = 0$ is equal to the voltage level at the end of the last falling step, when $S_{\text{F},N\text{-}k}$ opened:

$$v_{k,(t=0)} = V_{k,\text{F}}. \tag{3.13}$$

The load voltage v_{Load} and $C_{\text{Tank},k}$ voltage v_k follow an RC-charging waveform such that

$$v_{\text{Load}} = \left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(\frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{t}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1}, \tag{3.14}$$

$$v_k = \left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(e^{-\frac{t}{\tau_{\text{R}}}} + \frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{t}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1}, \tag{3.15}$$

where

$$C_{\text{Series}} = \frac{C_{\text{Tank}} C_{\text{Load}}}{C_{\text{Tank}} + C_{\text{Load}}}, \tag{3.16}$$

$$\tau_{\text{R}} = C_{\text{Series}} R_{\text{SR}}, \tag{3.17}$$

and R_{SR} is the resistance of the rising-edge switches S_{R}.

The v_{Load} and v_k voltages at the time that the switch $S_{\text{R},k}$ opens ($t = T_{\text{SR}}$) become

$$V_{\text{Load,R},k} = v_{\text{Load},(t=T_{\text{SR}})} = \left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(\frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1}. \quad (3.18)$$

$$V_{k,\text{R}} = v_{k,(t=T_{\text{SR}})} = \left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}} + \frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1}. \quad (3.19)$$

Combining (3.11) and (3.19) gives

$$V_k = \frac{V_{k,\text{F}} + \left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}} + \frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1}}{2}. \quad (3.20)$$

Combining (3.6) and (3.8) with (3.20) gives

$$r = \frac{V_{\text{Load,R},k} - V_{\text{Load,R},k-1}}{\frac{V_{k,\text{F}} + \left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}} + \frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1}}{2} - V_{\text{Load,R},k-1}}, \quad (3.21)$$

which can be simplified to

$$r = 2\frac{V_{\text{Load,R},k} - V_{\text{Load,R},k-1}}{\left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(1 + e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}} + \frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right)}. \quad (3.22)$$

Substituting (3.18) into (3.22) produces

$$r = 2\frac{\left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(\frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right) + V_{\text{Load,R},k-1} - V_{\text{Load,R},k-1}}{\left(V_{k,\text{F}} - V_{\text{Load,R},k-1}\right)\left(1 + e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}} + \frac{C_{\text{Series}}}{C_{\text{Load}}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)\right)}, \quad (3.23)$$

which can be simplified to

$$r = \frac{2C_{\text{Series}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)}{C_{\text{Load}}\left(1 + e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right) + C_{\text{Series}}\left(1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}\right)}, \quad (3.24)$$

and further simplified to

$$r = \frac{2C_{\text{Series}}}{C_{\text{Series}} + C_{\text{Load}} \dfrac{1 + e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}}{1 - e^{-\frac{T_{\text{SR}}}{\tau_{\text{R}}}}}}. \tag{3.25}$$

Applying a trigonometric identity, (3.25) can be written as

$$r = \frac{2C_{\text{Series}}}{C_{\text{Series}} + C_{\text{Load}} \coth\left(\frac{T_{\text{SR}}}{2\tau_{\text{R}}}\right)}. \tag{3.26}$$

From symmetry, the falling-edge step term f can be reached in the same way:

$$f = \frac{2C_{\text{Series}}}{C_{\text{Series}} + C_{\text{Load}} \coth\left(\frac{T_{\text{SF}}}{2\tau_{\text{F}}}\right)}, \tag{3.27}$$

where

$$\tau_{\text{F}} = C_{\text{Series}} R_{\text{SF}}. \tag{3.28}$$

Now that the r and f terms have been defined and derived, the next step is to use those terms to set up a system of equations to determine the value of v_{Load} at the end of each rising step $V_{\text{Load,R},k}$ as a function of r, and V_k. In the case of an $N = 5$ step driver, v_{Load} at the end of each step is:

$$\begin{aligned}
\text{pedistal: } & V_{\text{Load,R},0} = 0\ \text{V} \\
\text{step 1: } & V_{\text{Load,R},1} = rV_1 \\
\text{step 2: } & V_{\text{Load,R},2} = V_{\text{Load,R},1} + r\left(V_2 - V_{\text{Load,R},1}\right) \\
\text{step 3: } & V_{\text{Load,R},3} = V_{\text{Load,R},2} + r\left(V_3 - V_{\text{Load,R},2}\right) \\
\text{step 4: } & V_{\text{Load,R},4} = V_{\text{Load,R},3} + r\left(V_4 - V_{\text{Load,R},3}\right) \\
\text{step 5: } & V_{\text{Load,R},5} = V_{\text{DD}}
\end{aligned} \tag{3.29}$$

In general, for arbitrary N:

$$V_{\text{Load,R},k} = \begin{cases} 0, & k = 0 \\ V_{\text{Load,R},k-1} + r\left(V_k - V_{\text{Load,R},k-1}\right), & 0 < k < N \\ V_{\text{DD}}, & k = N \end{cases} \tag{3.30}$$

This can be re-written as:

$$\begin{aligned}
\text{pedistal: } & V_{\text{Load,R},0} = 0 \\
\text{step 1: } & V_{\text{Load,R},1} = rV_1 \\
\text{step 2: } & V_{\text{Load,R},2} = rV_1 + r(V_2 - rV_1) \\
\text{step 3: } & V_{\text{Load,R},3} = rV_1 + r(V_2 - rV_1) + r\big(V_3 - rV_1 + r(V_2 - rV_1)\big) \\
\text{step 4: } & V_{\text{Load,R},4} = rV_1 + r(V_2 - rV_1) + r\big(V_3 - rV_1 + r(V_2 - rV_1)\big) + \\
& \quad r\Big(V_4 - rV_1 + r(V_2 - rV_1) + r\big(V_3 - rV_1 + r(V_2 - rV_1)\big)\Big) \\
\text{step 5: } & V_{\text{Load,R},5} = V_{\text{DD}}
\end{aligned}, \tag{3.31}$$

which can be re-written as:

$$\begin{aligned}
\text{pedistal: } & V_{\text{Load,R},0} = 0 \\
\text{step 1: } & V_{\text{Load,R},1} = rV_1 \\
\text{step 2: } & V_{\text{Load,R},2} = r(1-r)V_1 + rV_2 \\
\text{step 3: } & V_{\text{Load,R},3} = r(1-r)^2V_1 + r(1-r)V_2 + rV_3 \\
\text{step 4: } & V_{\text{Load,R},4} = r(1-r)^3V_1 + r(1-r)^2V_2 + r(1-r)V_3 + rV_4 \\
\text{step 5: } & V_{\text{Load,R},5} = V_{\text{DD}}
\end{aligned}. \tag{3.32}$$

In general, for arbitrary N:

$$V_{\text{Load,R},k} = \begin{cases} 0, & k = 0 \\ \displaystyle\sum_{i=1}^{k} r(1-r)^{k-i}\, V_i\,, & 0 < k < N\,, \\ V_{\text{DD}}, & k = N \end{cases} \tag{3.33}$$

Where V_i in this case is $C_{\text{Tank},k}$ voltage V_k, but with k replaced with i for the summation.

Next, the load voltage at the end of each falling step $V_{\text{Load,F},k}$ is determined as a function of f and V_k. For the falling-edge steps, the k^{th} step of v_{Load} does not distribute charge to $C_{\text{Tank},k}$ (V_k) as it does with the rising steps. Instead, on step k, $S_{\text{F},k}$ closes and discharges v_{Load} into $C_{\text{Tank},N-k}$ (V_{N-k}). This is the reverse of the rising steps. For an $N = 4$ step driver:

$$\begin{aligned}
\text{plateau: } & V_{\text{Load,F},0} = V_{\text{DD}} \\
\text{step 1: } & V_{\text{Load,F},1} = V_{\text{Load,F},0} - f\big(V_{\text{Load,F},0} - V_3\big) \\
\text{step 2: } & V_{\text{Load,F},2} = V_{\text{Load,F},1} - f\big(V_{\text{Load,F},1} - V_2\big). \\
\text{step 3: } & V_{\text{Load,F},3} = V_{\text{Load,F},2} - f\big(V_{\text{Load,F},2} - V_1\big) \\
\text{step 4: } & V_{\text{Load,F},4} = 0\ \text{V}
\end{aligned} \tag{3.34}$$

In general, for arbitrary N:

$$V_{\text{Load,F},k} = \begin{cases} V_{\text{DD}}, & k = 0 \\ V_{\text{Load,F},k-1} - f\left(V_{\text{Load,F},k-1} - V_{N-k}\right), & 0 < k < N \\ 0, & k = N \end{cases}. \tag{3.35}$$

This can be rewritten as:

$$\begin{aligned} \text{plateau: } & V_{\text{Load,F},0} = V_{\text{DD}} \\ \text{step 1: } & V_{\text{Load,F},1} = V_{\text{Load,F},0} - f\left(V_{\text{Load,F},0} - V_3\right) \\ \text{step 2: } & V_{\text{Load,F},2} = V_{\text{Load,F},1} - f\left(V_{\text{Load,F},1} - V_2\right), \\ \text{step 3: } & V_{\text{Load,F},3} = V_{\text{Load,F},2} - f\left(V_{\text{Load,F},2} - V_1\right) \\ \text{step 4: } & V_{\text{Load,F},4} = 0\ \text{V} \end{aligned} \tag{3.36}$$

which can be expanded to become

$$\begin{aligned} \text{plateau: } & V_{\text{Load,F},0} = V_{\text{DD}} \\ \text{step 1: } & V_{\text{Load,F},1} = V_{\text{DD}} - f(V_{\text{DD}} - V_3) \\ \text{step 2: } & V_{\text{Load,F},2} = V_{\text{DD}} - f(V_{\text{DD}} - V_3) - f(V_{\text{DD}} - f(V_{\text{DD}} - V_3) - V_2) \\ \text{step 3: } & V_{\text{Load,F},3} = V_{\text{DD}} - f(V_{\text{DD}} - V_3) - f(V_{\text{DD}} - f(V_{\text{DD}} - V_3) - V_2) - \\ & f(V_{\text{DD}} - f(V_{\text{DD}} - V_3) - f(V_{\text{DD}} - f(V_{\text{DD}} - V_3) - V_2) - V_1) \\ \text{step 4: } & V_{\text{Load,F},4} = 0\ \text{V} \end{aligned}. \tag{3.37}$$

This can be simplified to

$$\begin{aligned} \text{plateau: } & V_{\text{Load,F},0} = V_{\text{DD}} \\ \text{step 1: } & V_{\text{Load,F},1} = (1-f)V_{\text{DD}} + fV_3 \\ \text{step 2: } & V_{\text{Load,F},2} = (1-f)^2 V_{\text{DD}} + f(1-f)V_3 + fV_2 \\ \text{step 3: } & V_{\text{Load,F},3} = (1-f)^3 V_{\text{DD}} + f(1-f)^2 V_3 + f(1-f)V_2 + fV_1 \\ \text{step 4: } & V_{\text{Load,F},4} = 0\ \text{V} \end{aligned}. \tag{3.38}$$

In general, for arbitrary *N*:

$$V_{\text{Load,F},k} = \begin{cases} V_{\text{DD}}, & k = 0 \\ V_{\text{DD}}(1-f)^k + \sum_{i=0}^{k-1} f(1-f)^i\, V_{N-k+i}, & 0 < k < N \\ 0, & k = N \end{cases}. \tag{3.39}$$

For N = 5:

$$\begin{aligned}
&\text{plateau: } V_{\text{Load,F},0} = V_{\text{DD}} \\
&\text{step 1: } V_{\text{Load,F},1} = (1-f)V_{\text{DD}} + fV_4 \\
&\text{step 2: } V_{\text{Load,F},2} = (1-f)^2V_{\text{DD}} + f(1-f)V_4 + fV_3 \\
&\text{step 3: } V_{\text{Load,F},3} = (1-f)^3V_{\text{DD}} + f(1-f)^2V_4 + f(1-f)V_3 + fV_2 \\
&\text{step 4: } V_{\text{Load,F},4} = (1-f)^4V_{\text{DD}} + f(1-f)^3V_4 + f(1-f)^2V_3 + f(1-f)V_2 + fV_1 \\
&\text{step 5: } V_{\text{Load,F},5} = 0\ \text{V}
\end{aligned} \quad . \tag{3.40}$$

Sets of equations (3.33) and (3.39) leave 3(N−1) unknowns: V_k, $V_{\text{Load,R},k}$, $V_{\text{Load,F},k}$ (for k = 1 to N − 1), with only 2(N−1) equations. The final set of equations needed to solve for these variables is derived from the fact that, when in steady-state, the charge leaving a given $C_{\text{Tank},k}$ capacitor on a rising step ($-\Delta Q_{k,\text{R}}$) must equal the charge entering the capacitor on the falling step ($\Delta Q_{k,\text{F}}$), such that:

$$-\Delta Q_{k,\text{R}} = \Delta Q_{k,\text{F}}. \tag{3.41}$$

This means that the voltage step size when connecting the load capacitor C_{Load} to capacitor $C_{\text{Tank},k}$ on the rising edge (when $S_{\text{R},k}$ is closed) must equal the voltage step size when connecting C_{Load} to $C_{\text{Tank},k}$ on the falling edge ($S_{\text{F},N-k}$ is closed):

$$V_{\text{Load,R},k} - V_{\text{Load,R},k-1} = V_{\text{Load,F},N-k-1} - V_{\text{Load,F},N-k}. \tag{3.42}$$

This can be rewritten as

$$V_{\text{Load,R},k} + V_{\text{Load,F},N-k} = V_{\text{Load,R},k-1} + V_{\text{Load,F},N-k-1}. \tag{3.43}$$

For N = 5, (3.43) becomes

$$\begin{aligned}
&k = 1\text{: } V_{\text{Load,R},1} + V_{\text{Load,F},4} = V_{\text{Load,R},0} + V_{\text{Load,F},3} \\
&k = 2\text{: } V_{\text{Load,R},2} + V_{\text{Load,F},3} = V_{\text{Load,R},1} + V_{\text{Load,F},2} \\
&k = 3\text{: } V_{\text{Load,R},3} + V_{\text{Load,F},2} = V_{\text{Load,R},2} + V_{\text{Load,F},1} \\
&k = 4\text{: } V_{\text{Load,R},4} + V_{\text{Load,F},1} = V_{\text{Load,R},3} + V_{\text{Load,F},0}
\end{aligned}. \tag{3.44}$$

Substituting (3.33) and (3.39) into (3.44) yields

$$\begin{aligned}
&k=1\text{: } rV_1+(1-f)^4V_{\mathrm{DD}}+f(1-f)^3V_4+f(1-f)^2V_3+f(1-f)V_2+fV_1\\
&\qquad=0\text{ V}+(1-f)^3V_{\mathrm{DD}}+f(1-f)^2V_4+f(1-f)V_3+fV_2\\
&k=2\text{: } r(1-r)V_1+(1-f)^3V_{\mathrm{DD}}+f(1-f)^2V_4+f(1-f)V_3+fV_2\\
&\qquad=rV_1+(1-f)^2V_{\mathrm{DD}}+f(1-f)V_4+fV_3\\
&k=3\text{: } r(1-r)^2V_1+r(1-r)V_2+rV_3+(1-f)^2V_{\mathrm{DD}}+f(1-f)V_4+fV_3\\
&\qquad=r(1-r)V_1+rV_2+(1-f)V_{\mathrm{DD}}+fV_4\\
&k=4\text{: } r(1-r)^3V_1+r(1-r)^2V_2+r(1-r)V_3+rV_4+(1-f)V_{\mathrm{DD}}+fV_4\\
&\qquad=r(1-r)^2V_1+r(1-r)V_2+rV_3+V_{\mathrm{DD}}
\end{aligned}, \tag{3.45}$$

which can be simplified to

$$\begin{aligned}
&k=1\text{: } -r^2(1-r)^2V_1-r^2(1-r)V_2-r^2V_3+(r+f)V_4=fV_{\mathrm{DD}}\\
&k=2\text{: } -r^2(1-r)V_1-r^2V_2+(r+f)V_3-f^2V_4=f(1-f)V_{\mathrm{DD}}\\
&k=3\text{: } -r^2V_1+(r+f)V_2-f^2V_3-f^2(1-f)V_4=f(1-f)^2V_{\mathrm{DD}}\\
&k=4\text{: } (r+f)V_1-f^2V_2-f^2(1-f)V_3-f^2(1-f)^2V_4=f(1-f)^3V_{\mathrm{DD}}
\end{aligned}. \tag{3.46}$$

This can be formed into a matrix equation:

$$\boldsymbol{AV}=\boldsymbol{B}, \tag{3.47}$$

$$\begin{bmatrix}
-r^2(1-r)^2 & -r^2(1-r) & -r^2 & r+f\\
-r^2(1-r) & -r^2 & r+f & -f^2\\
-r^2 & r+f & -f^2 & -f^2(1-f)\\
r+f & -f^2 & -f^2(1-f) & -f^2(1-f)^2
\end{bmatrix}\begin{bmatrix}V_1\\V_2\\V_3\\V_4\end{bmatrix}=\begin{bmatrix}fV_{\mathrm{DD}}\\f(1-f)V_{\mathrm{DD}}\\f(1-f)^2V_{\mathrm{DD}}\\f(1-f)^3V_{\mathrm{DD}}\end{bmatrix}. \tag{3.48}$$

These matrices form a clear pattern, which is more visible when including all (1-*r*) and (1-*f*) exponents:

$$\begin{bmatrix}
-r^2(1-r)^2 & -r^2(1-r)^1 & -r^2(1-r)^0 & r+f\\
-r^2(1-r)^1 & -r^2(1-r)^0 & r+f & -f^2(1-f)^0\\
-r^2(1-r)^0 & r+f & -f^2(1-f)^0 & -f^2(1-f)^1\\
r+f & -f^2(1-f)^0 & -f^2(1-f)^1 & -f^2(1-f)^2
\end{bmatrix}\begin{bmatrix}V_1\\V_2\\V_3\\V_4\end{bmatrix}=\begin{bmatrix}f(1-f)^0V_{\mathrm{DD}}\\f(1-f)^1V_{\mathrm{DD}}\\f(1-f)^2V_{\mathrm{DD}}\\f(1-f)^3V_{\mathrm{DD}}\end{bmatrix}. \tag{3.49}$$

The pattern can be extrapolated to any value for $N > 1$.

For $N = 2$:

$$(r+f)V_1=fV_{\mathrm{DD}}. \tag{3.50}$$

For $N = 6$:

$$\begin{bmatrix} r^2(1-r)^3 & -r^2(1-r)^2 & -r^2(1-r)^1 & -r^2(1-r)^0 & r+f \\ -r^2(1-r)^2 & -r^2(1-r)^1 & -r^2(1-r)^0 & r+f & -f^2(1-f)^0 \\ -r^2(1-r)^1 & -r^2(1-r)^0 & r+f & -f^2(1-f)^0 & -f^2(1-f)^1 \\ -r^2(1-r)^0 & r+f & -f^2(1-f)^0 & -f^2(1-f)^1 & -f^2(1-f)^2 \\ r+f & -f^2(1-f)^0 & -f^2(1-f)^1 & -f^2(1-f)^2 & -f^2(1-f)^3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = \begin{bmatrix} f(1-f)^0 V_{\mathrm{DD}} \\ f(1-f)^1 V_{\mathrm{DD}} \\ f(1-f)^2 V_{\mathrm{DD}} \\ f(1-f)^3 V_{\mathrm{DD}} \\ f(1-f)^4 V_{\mathrm{DD}} \end{bmatrix}. \quad (3.51)$$

With this, all V_k voltages can be solved for. Once all V_k voltages are known, $V_{\mathrm{Load,R,}N\text{-}1}$ can be solved for with (3.33). After $V_{\mathrm{Load,R,}N\text{-}1}$ is known, $E_{\mathrm{Load\text{-}Driver}}$ can be determined from (3.5).

The following pseudocode builds the **A** matrix and **B** vector:

```
A = zero array of size (N-1) by (N-1)
B = zero array of size (N-1) by 1
for i in [1,2,3,...,(N-1)] :
   B[i] = f * (1-f)**i * VDD
   for j in [1,2,3,...,(N-1)] :
        if (i+j == N-2) :
             A[i,j] = r+f
        else if (i+j < N-2) :
             A[i,j] = -(r**2) * (1 - r)**(N-3-i-j)
        else if (i+j > N-2) :
             A[i,j] = -(f**2) * (1-f)**(i+j-(N-1))
```

In the pseudocode above, ****** symbolizes "to the power of".

Equation (3.5) does not consider the energy required to drive the switches $S_{\mathrm{R}}/S_{\mathrm{F}}$ on and off. The total energy required to drive the load is

$$E_{\mathrm{Driver,Total}} = E_{\mathrm{Load\text{-}Driver}} + E_{\mathrm{Switch\text{-}Driver}}, \quad (3.52)$$

where $E_{\mathrm{Switch\text{-}Driver}}$ is the combined total of the energy consumed to drive all of the switches $S_{\mathrm{R}}/S_{\mathrm{F}}$ in the stepwise driver, such that

$$E_{\text{Switch-Driver}} = \sum_{k=1}^{N} E_{\text{SR},k} + \sum_{k=1}^{N} E_{\text{SF},k}\,. \tag{3.53}$$

If the switches S_R/S_F are implemented as MOSFET devices, the energy required to drive each individual switch is inversely proportional to the on-state (closed) resistance of the switch:

$$E_{\text{SR},k} = \frac{\rho_{\text{R},k}}{R_{\text{SR},k}}, \qquad E_{\text{SF},k} = \frac{\rho_{\text{F,k}}}{R_{\text{SF},k}}. \tag{3.54}$$

Terms $\rho_{R,k}$ and $\rho_{F,k}$ are the quality factor of the MOSFET switch and symbolizes the energy required to turn a switch of a given resistance on then off. If one assumes that all S_R are identical and all S_F are identical, then (3.53) simplifies to

$$E_{\text{Switch-Driver}} = NE_{\text{SR}} + NE_{\text{SF}}. \tag{3.55}$$

The remaining discussion focuses on $E_{\text{Load-Driver}}$.

3.3 Validation of Stepwise Driver Energy Consumption Model

This section investigates the accuracy of the stepwise driver model for $E_{\text{Load-Driver}}$ derived in the previous section by comparing it to the results of a circuit simulator. This section also compares the accuracy with models from previous work.

3.3.1 *Comparison to simulated data*

To validate the model, the calculated $E_{\text{Load-Driver}}$ was compared to results from a circuit simulator. In the simulation, switches S_R/S_F were modeled as ideal switches with a series resistance of $R_{SR} = R_{SF}$. All capacitors were modeled as ideal capacitors. Simulations were run for a sufficient number of step-up/step-down cycles such that all V_k voltages reached their steady-state values. $E_{\text{Load-Driver}}$ was measured in simulation using (3.2). $E_{\text{Load-Driver}}$ was compared for combinations of $N = 4$ and $N = 9$, as well as $C_{\text{Tank}} = C_{\text{Load}}$ and $C_{\text{Tank}} = 4C_{\text{Load}}$. Switch on-time was swept such that $T_{SR} = 0$ through 6τ. Here, $\tau = \tau_R = \tau_F$. Figure 3.4 compares calculated results (dotted lines) with

simulated results (solid lines) for the case that $T_{SF} = T_{SR}$. Figure 3.5 compares calculated results with simulated results for the case that $T_{SF} = 2T_{SR}$. The $E_{Load\text{-}Driver}$ energy is normalize to that of a conventional ($N = 1$) driver. The $E_{Load\text{-}Driver}$ energy calculated using the proposed analytical model closely matches the results from the circuit simulator.

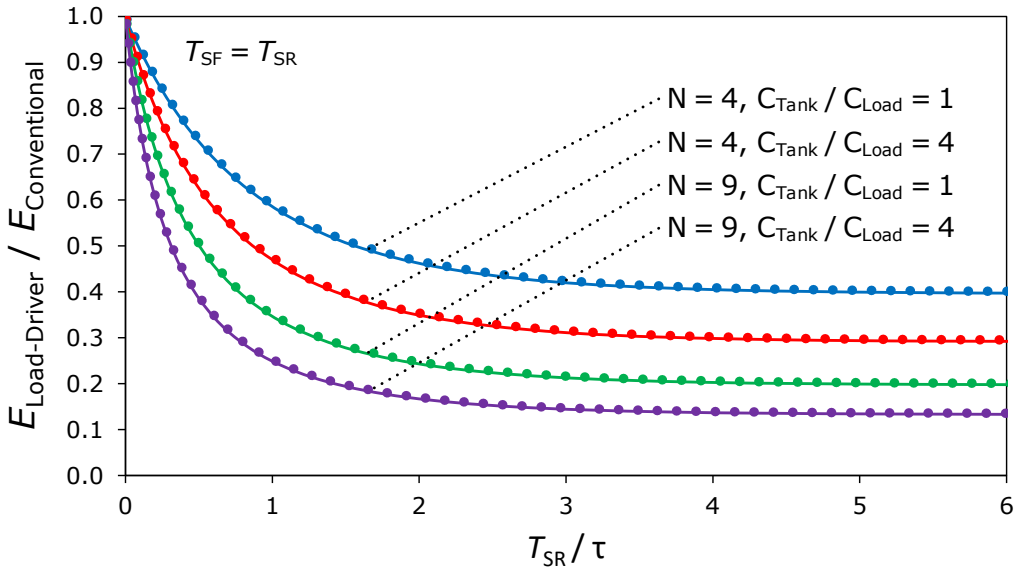

Figure 3.4. Comparing the proposed stepwise driver model results (dotted line) with results from a circuit simulator (solid line) for various N, C_{Tank}, and T_{SR} values. Stepwise driver energy is normalized to that of a conventional driver ($N = 1$). Switch S_R on-time T_{SR} is normalized to the RC settling time constant, $\tau = \tau_R = \tau_F$. Switch S_F on-time equals the S_R on-time: $T_{SF} = T_{SR}$.

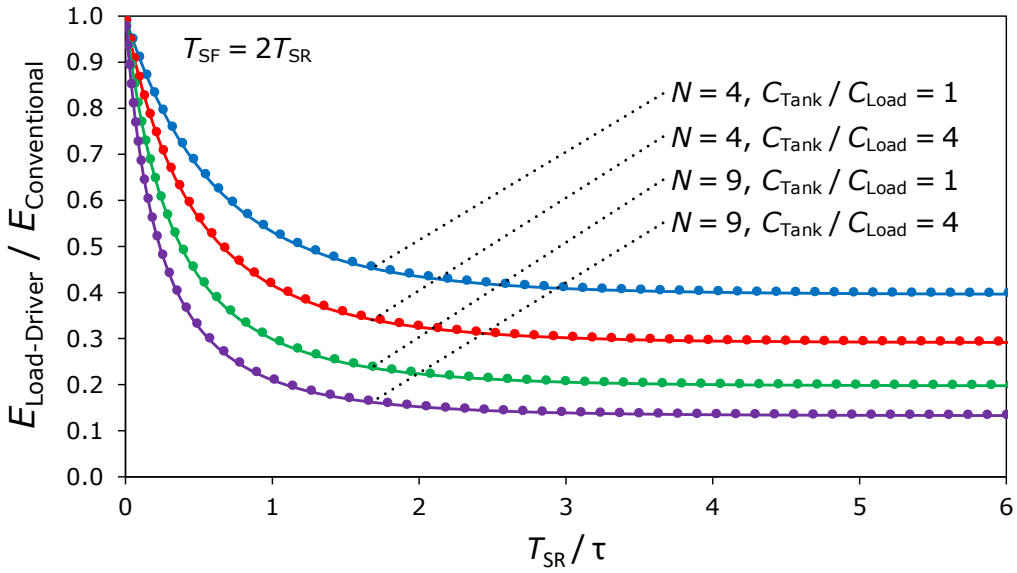

Figure 3.5. Comparing the proposed stepwise driver model results (dotted line) with results from a circuit simulator (solid line) for various N, C_{Tank}, and T_{SR} values. Stepwise driver energy is normalized to that of a conventional driver (N = 1). Switch S_R on-time T_{SR} is normalized to the RC settling time constant, $\tau = \tau_R = \tau_F$. The S_F on-time is double the S_R on-time: $T_{SF} = 2T_{SR}$.

3.3.2 *Comparison to prior work*

Svensson [50] introduced stepwise charging and provides an approximation of the energy consumed by the stepwise driver based on the number of steps N and the amount of time that each step is given to settle. From [50]:

$$E_{\text{Driver,Total[50]}} = \left(\frac{1}{N}\coth\left(\frac{m}{2}\right) + 2N^2 m\frac{\bar{\rho}}{T}\right) C_{\text{Load}} V_{\text{DD}}^2. \tag{3.56}$$

In [50], m is the number of time constants that the stepwise driver switches are kept closed. In the terminology of this paper

$$m := \frac{T_{\text{SR}}}{\tau_{\text{R}}}, \tag{3.57}$$

assuming that $T_{SR} = T_{SF}$ and $\tau_R = \tau_F$. Svensson [50] defines $\bar{\rho}$ as the gate capacitance of a stepwise driver switch for a given resistance. Setting $\bar{\rho} = 0$ gives the [50] analogue of $E_{\text{Load-Driver}}$:

$$E_{\text{Load-Driver[50]}} = \frac{1}{N}\coth\left(\frac{T_{\text{SR}}}{2\tau_{\text{R}}}\right)C_{\text{Load}}V_{\text{DD}}^2. \tag{3.58}$$

Equation (3.58) from [50] does not take into account finite C_{Tank}. Dancy [21] provides the energy dissipated in the stepwise driver switches for half a charging cycle (only charging the load, not discharging the load) as

$$E_{\text{diss[21]}} = \frac{V_{\text{DD}}^2 C_{\text{Load}}(C_{\text{Tank}} + C_{\text{Load}})}{2(C_{\text{Load}} + NC_{\text{Tank}})}. \tag{3.59}$$

This is only half of the total energy dissipated by the stepwise driver per complete charge/discharge cycle. It must be doubled to find the total energy:

$$E_{\text{Load-Driver[21]}} = \frac{V_{\text{DD}}^2 C_{\text{Load}}(C_{\text{Tank}} + C_{\text{Load}})}{C_{\text{Load}} + NC_{\text{Tank}}}. \tag{3.60}$$

This approximation takes into account finite C_{Tank}, but assumes each step fully settles ($T_{\text{SR}} >> \tau_{\text{R}}$, $T_{\text{SF}} >> \tau_{\text{F}}$). Although not explicitly stated in [21], it can be deduced that adding the settling-time-inclusive model from [50] into the C_{Tank}-inclusive model in [21] will produce

$$E_{\text{Load-Driver[50][21]}} = \frac{V_{\text{DD}}^2 C_{\text{Load}}(C_{\text{Tank}} + C_{\text{Load}})}{C_{\text{Load}} + \dfrac{N}{\coth\left(\dfrac{T_{\text{SR}}}{2\tau_{\text{R}}}\right)}C_{\text{Tank}}}. \tag{3.61}$$

Although more accurate than (3.58) and (3.60), this is still an approximation that loses accuracy when $T_{\text{SR}} / \tau_{\text{R}} < 2$ (or $T_{\text{SF}} / \tau_{\text{F}} < 2$).

Figure 3.6 and Figure 3.7 compare the derived analytical models for the stepwise driver ($E_{\text{Load-Driver}}$) from Section 3.2 of this work, Equation (3.58) based on [50], Equation (3.60) based on [21], and Equation (3.61) from combining [50] and [21] against the results of a circuit simulator. The figures show that the model presented in this work is the only analytical model that accurately takes into account finite C_{Tank} and the step settling time T_{SR} (or T_{SF}).

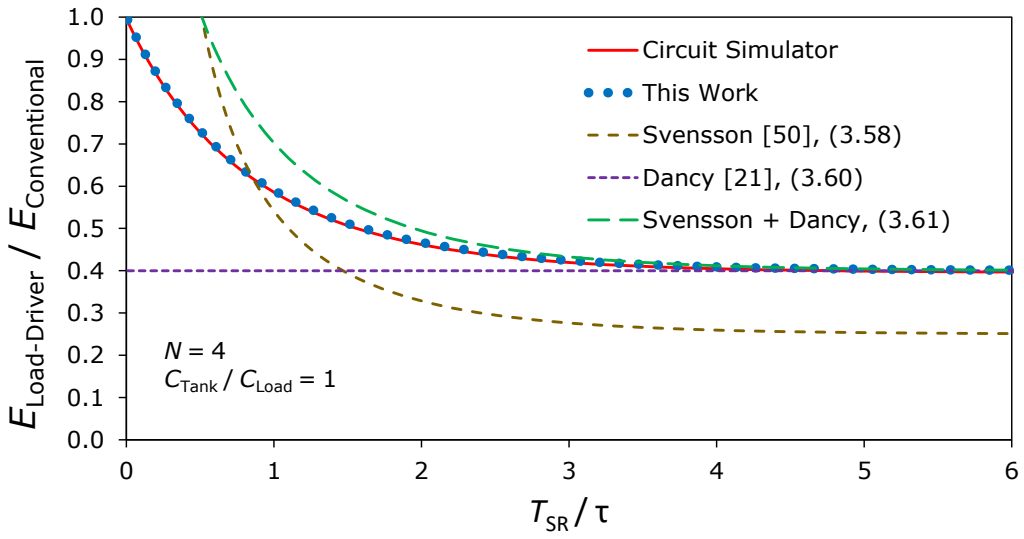

Figure 3.6. Comparing analytic model results of this work, Svensson [50], Dancy [21], and a combination of Svensson + Dancy against the results from a circuit simulator. Stepwise driver energy is normalized to that of a conventional driver (N = 1). Switch S_R on-time T_{SR} is normalized to the RC settling time constant, $\tau = \tau_R = \tau_F$. $T_{SF} = T_{SR}$. N = 4. C_{Tank} / C_{Load} = 1.

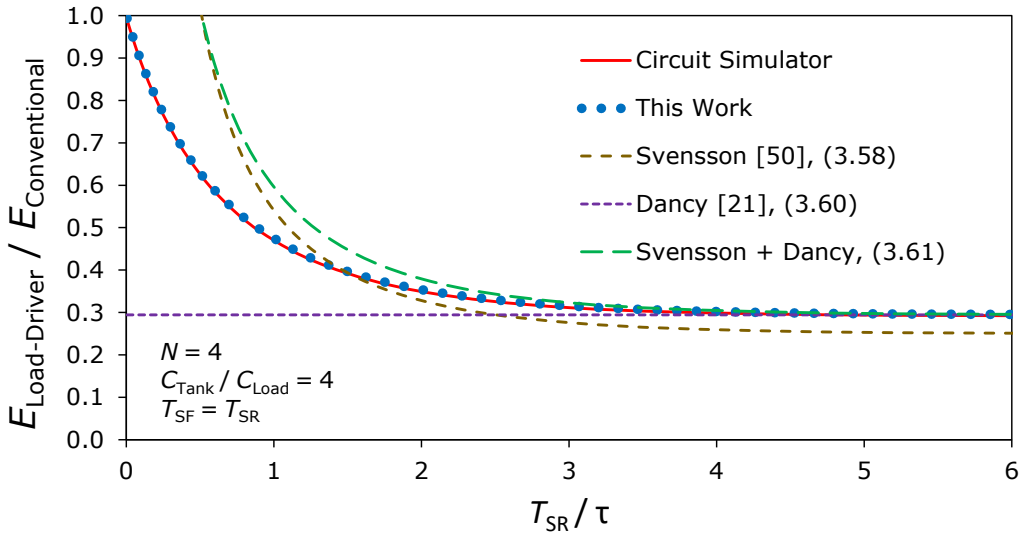

Figure 3.7. Comparing analytic model results of this work, Svensson [50], Dancy [21], and a combination of Svensson + Dancy against the results from a circuit simulator. Stepwise driver energy is normalized to that of a conventional driver (N = 1). Switch S_R on-time T_{SR} is normalized to the RC settling time constant, $\tau = \tau_R = \tau_F$. $T_{SF} = T_{SR}$. N = 4. C_{Tank} / C_{Load} = 4.

An accurate analytical model of a stepwise adiabatic driver has been presented. The model solves for all intermediate voltage levels (steps) for both rising and falling edges and calculates the energy consumed by the stepwise driver. The solution can be obtained by solving a matrix equation that can be built using the provided pseudocode. The accuracy of the model was compared with results from a circuit simulator as well as results from models from prior works. The model presented here provides the only closed-form solution that accurately takes into account the number of steps, step settling time, and the tank capacitance of the stepwise driver. The next section describes how a stepwise driver is used to drive the gate of the CMOS power FET.

3.4 Stepwise Gate Driver Implementation in the DC-DC Converter

A stepwise driver similar to the one in Figure 3.1 was designed and implemented to drive the gate of the DC-DC converter primary power FET M_1. Figure 3.8 shows the stepwise gate driver design used to drive M_1. Eight 1500 pF C_{Tank} capacitors are used in this design, making this an $N = 9$ stepwise driver. The terms used for the DC-DC converter stepwise gate driver correspond to those in Section 3.2 as follows:

$$v_{\text{G1}} := v_{\text{Load}}. \tag{3.62}$$

$$C_{\text{Gate}} := C_{\text{Load}}. \tag{3.63}$$

$$E_{\text{Gate-Drive}} := E_{\text{Load-Driver}}. \tag{3.64}$$

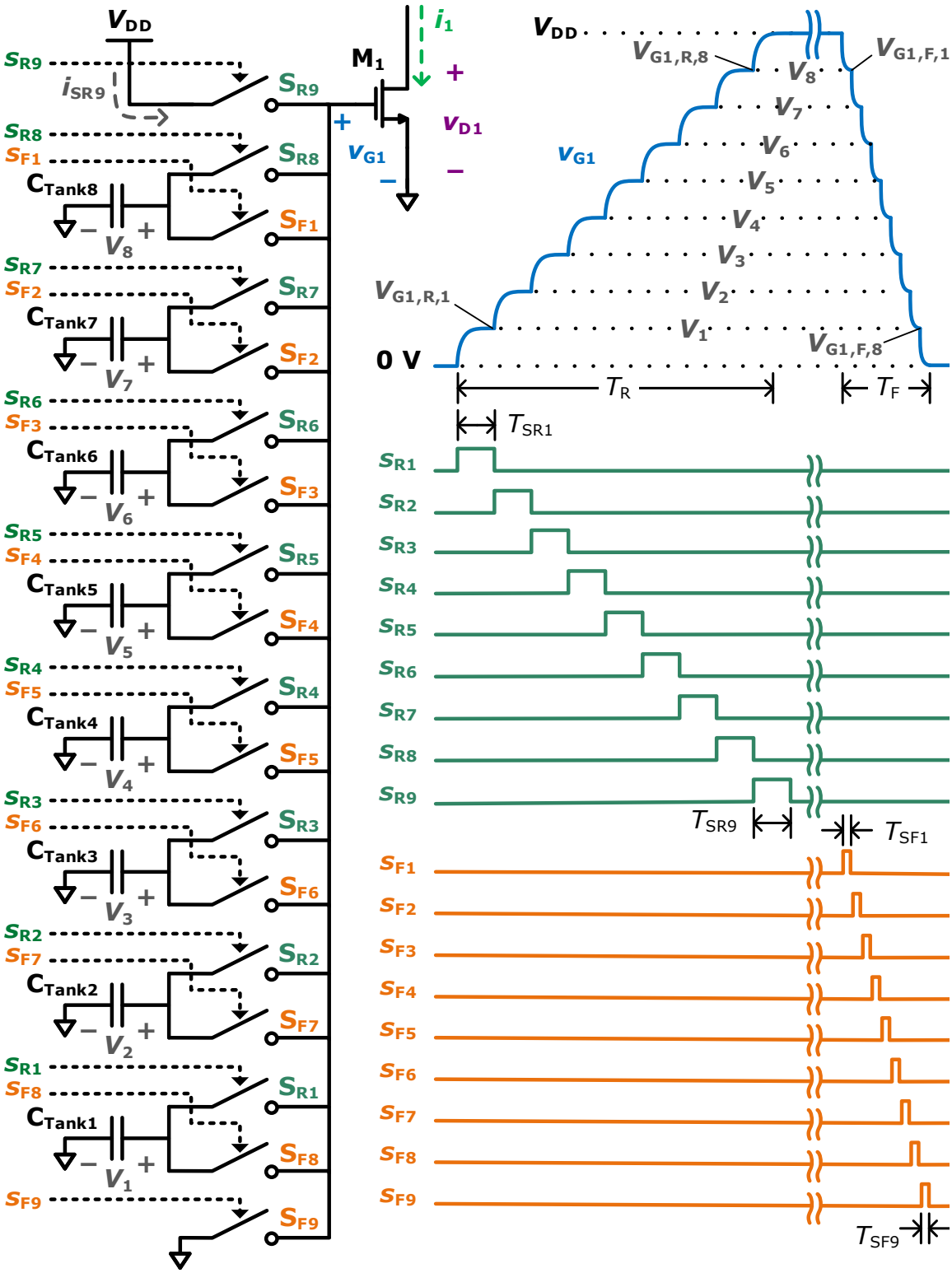

Figure 3.8. Stepwise gate driver used in the DC-DC converter and waveforms for one switching cycle. © 2023 IEEE

The v_{G1} fall-time T_F needs to be fast in order to minimize the transition losses described in Section 2.1.1. The rise-time T_R, on the other hand, has little effect on transition losses, the on-time $T_{SR,k}$ of each rising-edge switch $S_{R,k}$ can be relatively long and thus the resistance R_{SR} of the rising-edge switches can be relatively high.

3.4.1 *Stepwise switch driver*

The stepwise switch driver, shown in Figure 3.9, provides staggered pulses s_R and s_F to drive the switches S_R and S_F in the stepwise gate driver. Svennson [49] uses complimentary NMOS and PMOS devices for the switches. The problem with that architecture is that the switches connected to the V_k voltages near $V_{DD} / 2$ will not turn on when V_{DD} is less than the combined threshold voltages of the PMOS and NMOS. To address that deficiency, the proposed circuit uses only NMOS devices for S_R and S_F, driven with a voltage doubler similar to that in [57] to provide sufficient voltage to fully turn on the NMOS devices. This allows the circuit to operate down to $V_{OUT} = V_{DD} = 1.5$ V, even though the NMOS threshold voltage is 1.0 V. The circuit was fabricated in a CMOS process rated for 5.5 V, so the doubled voltage does not exceed the voltage ratings when $V_{OUT} = V_{DD} = 2.7$ V. If voltage ratings were a problem, then the circuit in [58] could be used to drive S_R/S_F. Although not used in this design, a non-overlap (break-before-make) circuit would be beneficial to ensure that no two stepwise switches are on at the same time.

3.4.2 *Stepwise timing control*

The stepwise switch driver in Figure 3.9 requires consecutive timing signals, y_n, to generate the staggered stepwise switching signals s_R and s_F. The timing circuit in [49] uses a finite state machine to produce the timing signals, which requires a clock and substantial logic, while [55] utilizes the inherent delay of current-starved logic gates. The proposed approach is to use the delay

line circuit included in Figure 3.9. Two of these delay line circuits are used: a “slow” delay line generates the timing for the rising edge of v_{G1} and a “fast” delay line generates the timing for the faster falling edge. In the delay line circuits, many series PMOS devices share a common gate bias voltage V_{SG}, which is set by a bias generator consisting of a gate-to-drain connected PMOS device and a resistor R_B. The bias generator operates at a low duty cycle to save power and V_{SG} is held with a capacitor C_B while the bias generator is disabled.

At reset, every *dly* node is pulled low. Once reset is low, the first *dly* is released and rises. Once the first *dly* rises to near V_{DD}, the next *dly* starts to rise, thereby producing a series of successive rising edges. Each successive *dly* signal does not start to rise until the previous *dly* is near V_{DD} due to the corresponding PMOS transistor being in the cutoff region. The time it takes each *dly* node to rise from 0 V to near V_{DD} is determined by the effective total intrinsic capacitance C_{dly} on each *dly* node and the charging current I_n sourced by the PMOS current sources:

$$T_{dly,n} = C_{dly}\frac{V_{DD} - (V_{SG} - V_{TH})}{I_{dly,n}}, \tag{3.65}$$

where V_{TH} is the PMOS threshold voltage and a positive number. As each successive *dly* node voltage rises, the corresponding PMOS connected to that node effectively becomes an additional device in the series PMOS current source chain, resulting in the charging current $I_{dly,n}$ to be slightly less for each successive *dly*:

$$I_{dly,n} \approx \frac{V_{DD} - V_{SG}}{R_B}\frac{K}{(M+n)}, \tag{3.66}$$

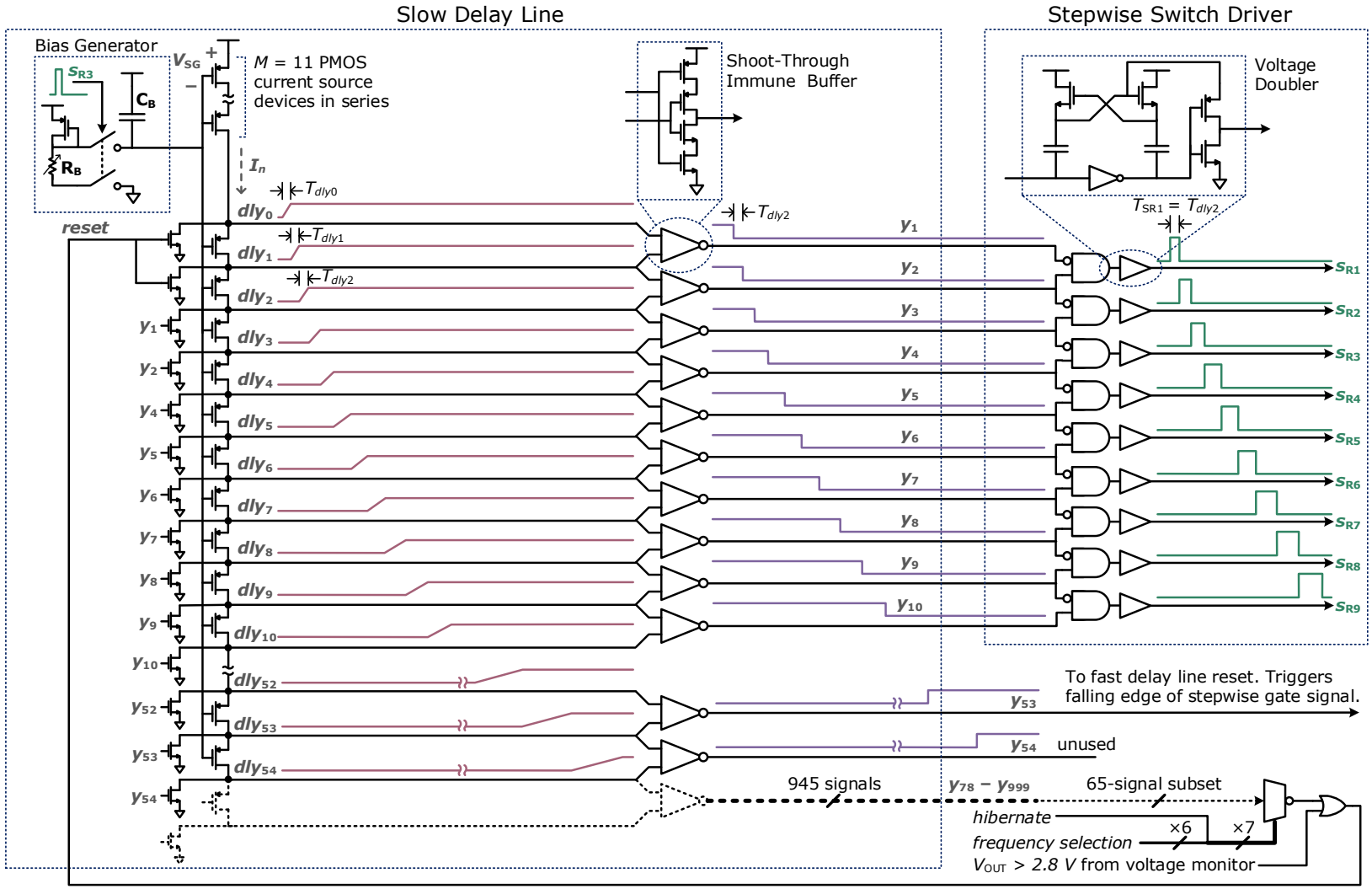

Figure 3.9. Stepwise control circuit for the rising edge of the stepwise gate signal, including the slow delay line and the stepwise switch driver. The circuit generating the falling edge of the stepwise gate voltage uses the fast delay line with a similar architecture.

with M = 11 being the number of series PMOS devices without a *dly* node on the source and K being the ratio of the W/L ratios between a "*dly*" PMOS device and the PMOS device in the bias generator. Equation (3.66) only holds if V_{SG} is constant, and for small n it practically is. However, capacitive coupling causes V_{SG} to reduce slightly each time a *dly* node voltage rises and this becomes significant for large n, resulting in an additional reduction in each $I_{dly,n}$. Per the charge-sharing equation, the amount that V_{SG} reduces by for each successive *dly* is

$$\Delta V_{\mathrm{SG}} = \frac{C_{\mathrm{GS}} + C_{\mathrm{GD}}}{C_{\mathrm{B}} + (C_{\mathrm{GS}} + C_{\mathrm{GD}})N_{dly}}, \tag{3.67}$$

where C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitance of each "*dly* PMOS" respectively and N_{dly} = 1000 is the total number of *dly* nodes. ΔV_{SG} was determined in simulation to be 0.13 mV. At n = 0, $V_{SG} - V_{TH}$ = 64 mV, which is low enough to be considered subthreshold operation. Using the subthreshold current formula from [59] (omitting channel-length modulation), the charging current becomes

$$I_{dly,n} = I_0 \frac{M}{M+n} e^{\left(1 - \frac{V_{\mathrm{SG0}} - n\Delta V_{\mathrm{SG}} - V_{\mathrm{TH}}}{\alpha V_{\mathrm{T}}}\right)^2}, \tag{3.68}$$

where I_0 = 8.8 nA and V_{SG0} = 1.10 V are the current and gate-to-source voltage before any *dly* node rises (at n = 0). V_T = 25 mV is the thermal voltage and α (referred to as n in [59]) was determined empirically in simulation to be 2.2. Another factor that can affect the $I_{dly,n}$ current is the static leakage on each *dly* node. Simulation showed that under typical conditions the leakage is negligible, but under hot temperatures or very large N_{dly} leakage can have a significant effect on T_{dly}, even preventing *dly* transitions altogether.

Figure 3.10 shows the simulated waveforms of the slow delay line. Figure 3.11 shows the time between *dly* signals $T_{dly,n}$ as determined from equations, simulation, and measurement of the silicon. Simulated and calculated results match closely with the measured results up to n = 300,

where the measured delays start to deviate from the predicted values. This difference could be attributed to unmodelled leakage current on the *dly* nodes or from inaccurate modelling of the subthreshold behavior of the PMOS devices. There is a gap in the silicon measured data between $n = 10$ and $n = 90$ due to a lack of visibility into the circuit.

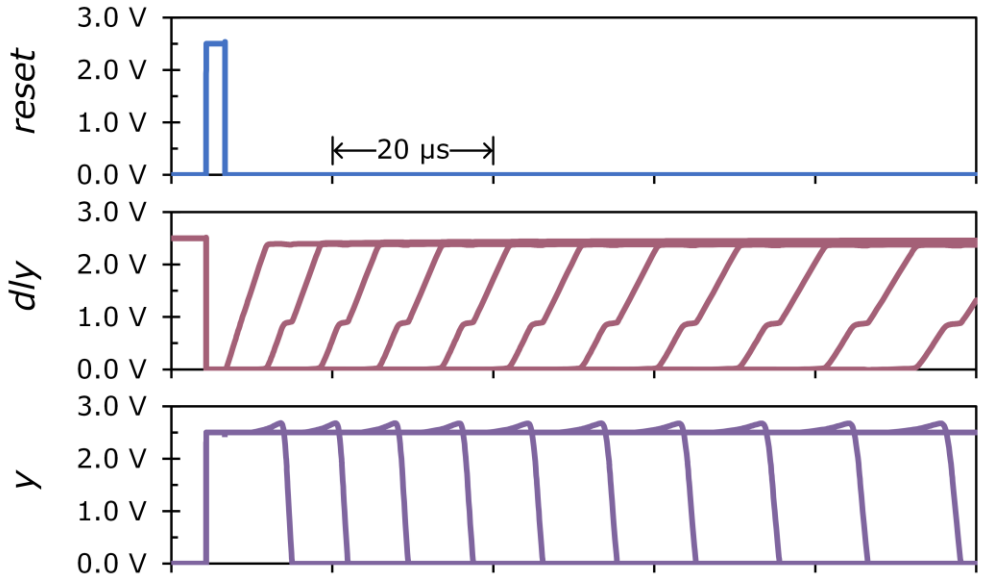

Figure 3.10. Simulated waveforms of the slow delay line, at 20°C. © 2023 IEEE

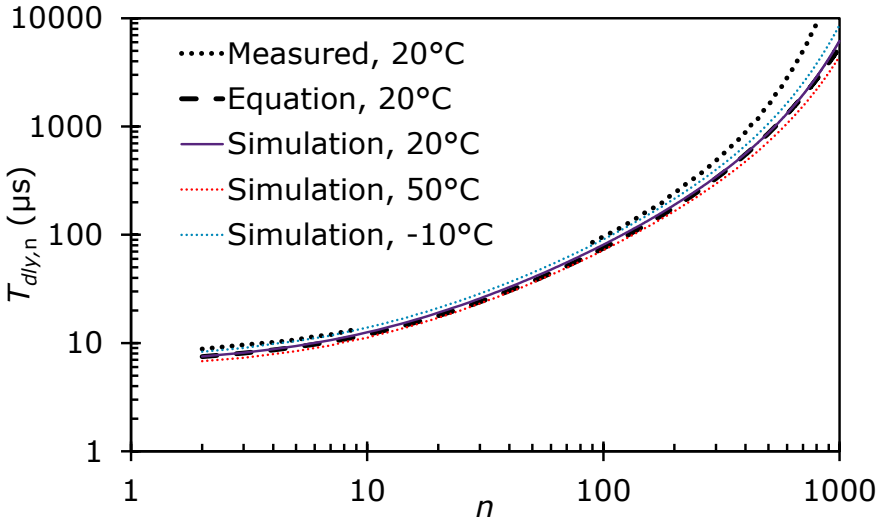

Figure 3.11. Time between *dly* signals, $T_{dly,n}$, vs. n as determined by simulation, equations (3.65), (3.67), (3.68), and measurement of the silicon. © 2023 IEEE

The slow edge rates of the *dly* signals would result in shoot-through currents in the downstream logic. An inverting buffer that is immune to shoot-through currents prevents this by using two NMOS and PMOS pairs, which are switched in a staggered fashion. The output of the shoot-through immune buffer is briefly undriven during the time after the first input has transitioned and before the second input has transitioned, so special care was taken in layout to prevent parasitic capacitive coupling from causing the output of the buffer to drift low during this time.

It is clear from Figure 3.11 that each successive $T_{dly,n}$ is slower than the previous. This behavior is not ideal for the stepwise gate driver but is useful for generating very slow timing signals when many stages are used, making the slow delay line useful for controlling the on-time and switching period of the DC-DC converter primary power FET M_1, and replacing the need for more timing circuits. The 53rd output y_{53} triggers the falling edge of the stepwise gate signal (controlled by the fast delay line), setting the duration in which power FET M_1 is on: $T_{i1,rise}$. One of 65 delay outputs is selected through a mux and is fed back to the *reset* signal to set the oscillation frequency (the switching frequency of M_1). The selectable switching frequency enables the input impedance to be programmed to match with the TEG for maximum power extraction, or "MPPT" as described in [60], [5], [6], [7], [61], [62] (this is opposed to the "open-circuit voltage" MPPT method described in [63] or the "perturb and observe" method described in [64]). When the *hibernate* input is high, the final delay output y_{999} is used, setting the frequency to 0.2 Hz to minimize quiescent power consumption.

Chapter 4.
ACTIVE RECTIFICATION, INPUT VOLTAGE DETECTION, AND OUTPUT VOLTAGE MONITORING

So far, the circuitry that controls the gate of primary power FET M_1 has been discussed, driving the adiabatic stepwise pattern to the M_1 gate voltage as well as setting the M_1 on-time and switching period. In this chapter, the circuitry that controls the gate of the secondary power FET rectifier devices M_{2P}/M_{2N} is discussed. Also, input voltage detection—used for enabling hibernation mode, and the output voltage monitor—used to both enable the load when V_{OUT} has reached the appropriate threshold and keep V_{OUT} from charging above tolerances—are discussed.

4.1 Active Rectification

The DC-DC converter operates in DCM and requires a form of rectification to allow current to flow to the output while preventing current from flowing from the output back into the converter. A diode like those shown in Figure 2.2 and Figure 2.4 is the simplest implementation but is inefficient due to the large forward voltage drop. Replacing the diodes with MOSFETs reduces the voltage drop significantly when switched at the appropriate times. Switching the MOSFET off as the current crosses 0 A is referred to as zero-current-switching (ZCS). To achieve ZCS, this work uses a modified version of the feedback technique that was introduced in [65] and later adapted in [24], [3], followed by [5], [6], [19], [23], [26], [66] for low V_{IN} converters.

Figure 4.1 shows the proposed active rectifier implementation. The rectifier device M_2 is switched on when the polarity of the drain voltage v_{D2} crosses negative (zero-voltage-switching,

ZVS) and off when v_{D2} crosses positive (i.e. when i_2 crosses negative, ZCS). A comparator is used to detect this polarity. However, when M_2 is in the "on" state the voltage drop is very small, making it difficult to accurately sense the polarity. To avoid this problem, the polarity of v_{D2} is only sampled while M_2 is in the "off" state. For turn-on, M_2 already starts in the "off" state, so the comparator directly controls when M_2 is switched on. But for turn-off, an adaptive timing method is used. A voltage-controlled timer sets the on-time of M_2. The polarity of v_{D2} is sampled *after* M_2 turns off and the duration of the on-time for the next cycle is adjusted based on when the polarity reversed. If the polarity reversed shortly after M_2 turned off—plus a short delay—then the on-time is increased for the next cycle. Otherwise, the on-time is decreased. Since M_2 is much smaller than M_1 it is driven with a conventional gate driver and stepwise gate-drive is not needed.

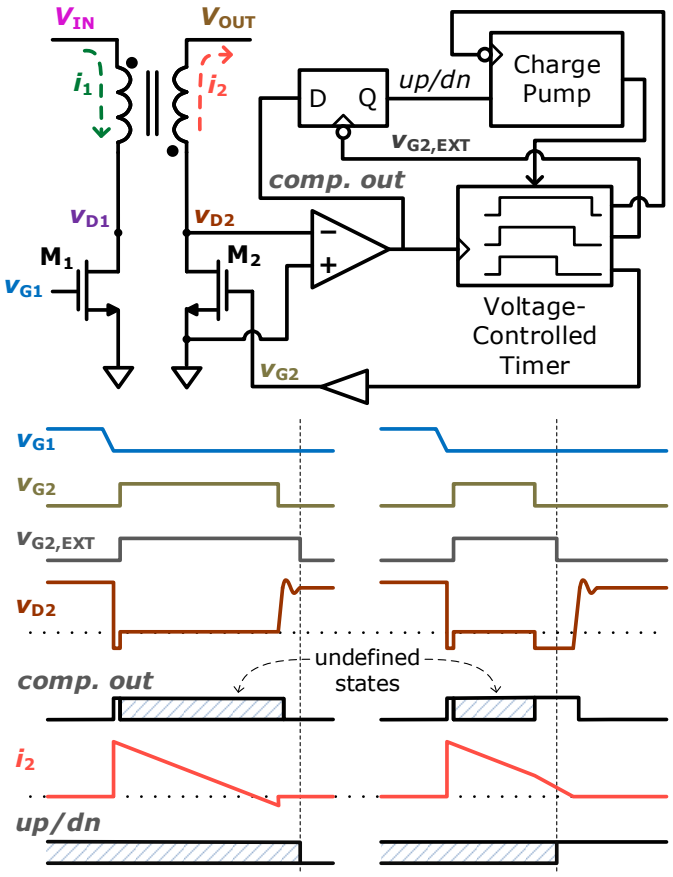

Figure 4.1. Active rectifier circuit for zero-current-switching. © 2023 IEEE

4.2 INPUT VOLTAGE DETECTION

When $|V_{IN}|$ is too low, the input energy per cycle E_{IN} is less than the energy consumed by losses and efficiency becomes less than 0%. Running the DC-DC converter at the normal operating frequency would quickly discharge the output storage capacitors due to the quiescent power consumption. Desai [67] proposes hibernating the converter when V_{IN} is so low that v_{D1} does not transition high enough to deliver any current to the output, but that is less than the 0% efficiency threshold. With that approach the converter could be wasting power with negative efficiency while V_{IN} is barely high enough to cause v_{D1} transitions but not delivering power to the output. The proposed approach is to hibernate as close as possible to when the efficiency crosses below 0%. In the proposed DC-DC converter, that typically occurs when $|V_{IN}| < 0.5$ mV. Sensing V_{IN} directly is impractical because it is so small. Instead, V_{IN} is measured indirectly through timing as proposed in [3] and [6] and illustrated in Figure 4.2. Ignoring parasitics, the relationship is

$$V_{\mathrm{IN}} \approx \frac{V_{\mathrm{OUT}}}{N_{\mathrm{t}}} \cdot \frac{T_{\mathrm{i2,fall}}}{T_{\mathrm{i1,rise}}}, \tag{4.1}$$

where N_t is the transformer turns ratio. By comparing $T_{i1,fall}$ to a pre-programmed reference delay T_{Ref}, V_{IN} can be estimated and compared to a threshold $V_{IN,Th}$ (0.5 mV) such that

$$V_{\mathrm{IN,Th}} \approx \frac{V_{\mathrm{OUT}}}{N_{\mathrm{t}}} \cdot \frac{T_{\mathrm{i2,fall}}}{T_{\mathrm{Ref}}}. \tag{4.2}$$

Equation (4.2) shows that $V_{IN,Th}$ is proportional to V_{OUT}. This relationship is desirable for setting the hibernation threshold voltage because the minimum V_{IN} (V_{IN} where the efficiency is 0%) is also approximately proportional to V_{OUT}. If $T_{i1,rise}$, and T_{Ref} were fixed, then the V_{IN} threshold would inherently track the 0% efficiency point. In this work, $T_{i1,rise}$ and T_{Ref} are sensitive to V_{OUT} due to the delay line design, so the hibernation threshold does not track the 0% efficiency point as well as it would if the timing were better controlled.

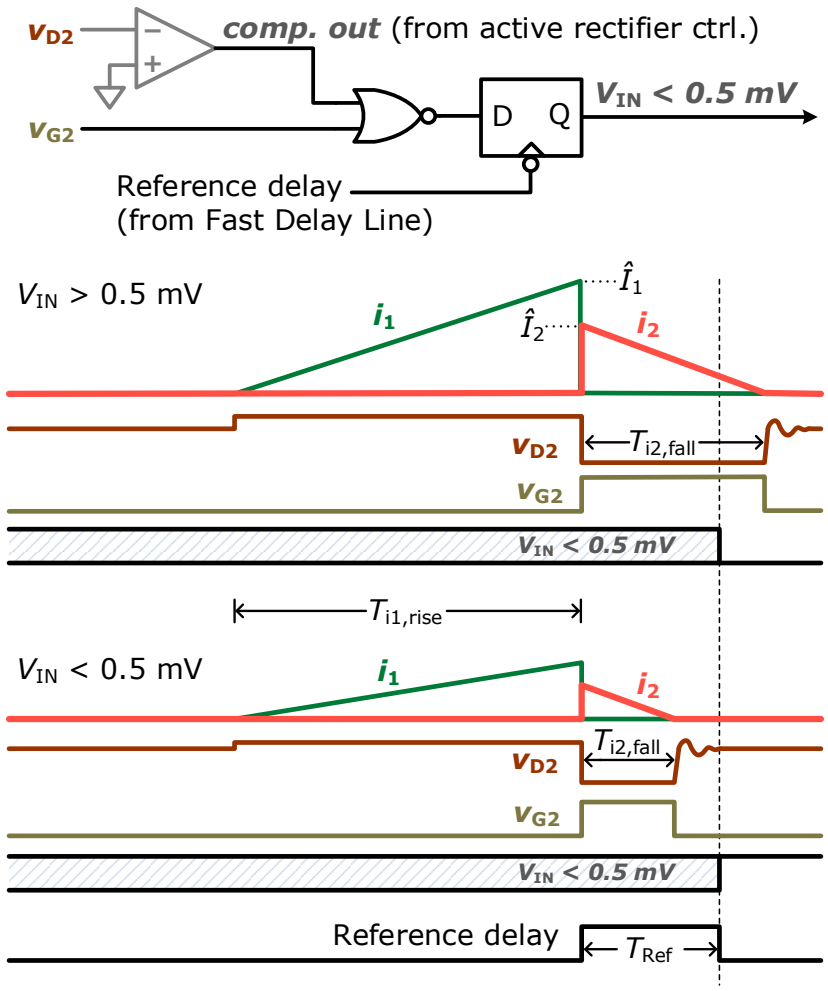

Figure 4.2. Input voltage detection. © 2023 IEEE

4.3 Output Voltage Monitor

The voltage monitor circuit in Figure 4.3 was implemented to enable the load when the output voltage is above 2.5 V and the power supply is at a good level, similar to the *power good* function in [36]. This function is achieved by comparing a divided version of V_{OUT} with a reference voltage generated by a bandgap circuit. Hysteresis is achieved by adjusting the divide ratio, so *power good* transitions high when V_{OUT} > 2.7 V and low when V_{OUT} < 2.5 V.

To minimize power consumption when *power good* is low, the comparator and bandgap circuit are enabled only while y_5 from the slow delay line is high and only once every 32 cycles.

When *power good* is high it is assumed that the load current will overshadow the 4 μA current consumption of the comparator and bandgap, so the comparator and bandgap are left on. Here, *reset*, y_4, y_5, and y_6 are the same signals as shown in Figure 3.9.

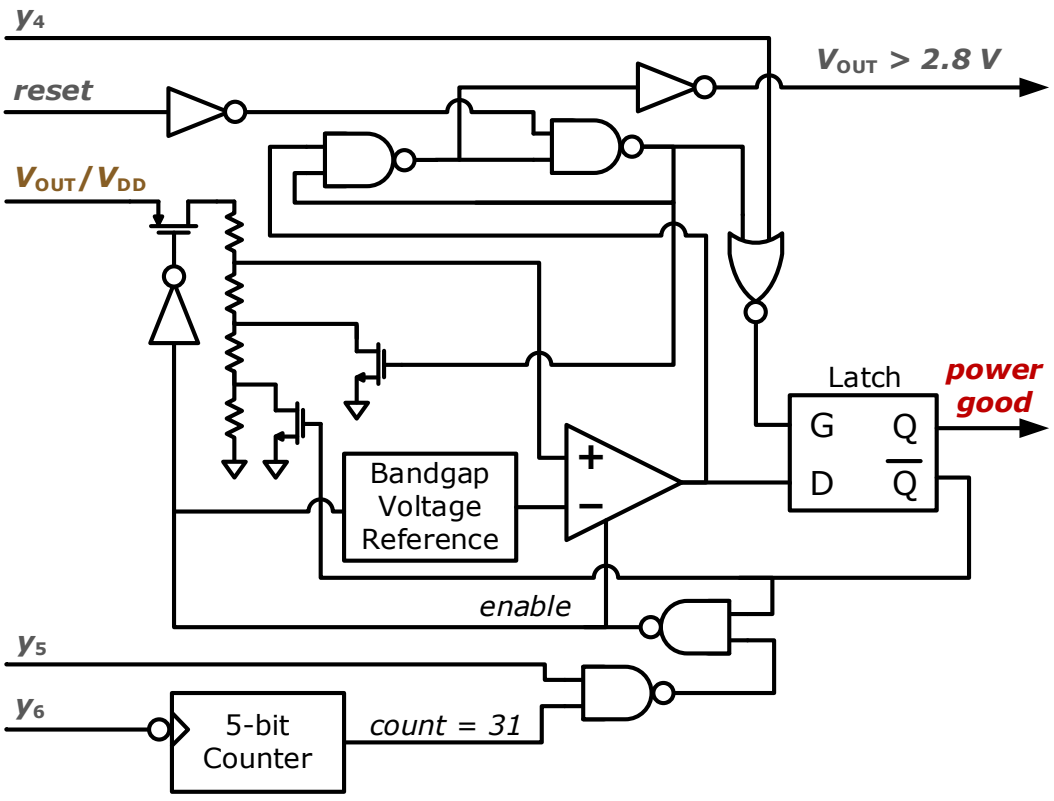

Figure 4.3. Voltage monitor circuit. © 2023 IEEE

The voltage monitor also keeps the DC-DC converter from allowing V_{OUT} to charge above 2.8 V. If *power good* is high and the slow delay line is in the *reset* state, the comparator threshold is set to 2.8 V. If $V_{OUT} > 2.8$ V then the slow delay line is kept in reset—preventing further DC-DC converter switching—until V_{OUT} drops below the 2.8 V threshold.

Chapter 5.

EFFICIENCY OPTIMIZATION

There are many design parameters that need to be set in the DC-DC converter. Chapter 2 covered the design decisions with regards to the parameters involving the flyback transformer, including the inductance of the primary coil (L = 300 μH), the transformer turns ratio (N_t = 20), and the peak current of the primary coil ($\hat{I}_1$ = 200 mA at V_{IN} = 50 mV). As explained in [26], keeping the on-time and switching frequency of M_1 fixed allows the DC-DC converter input impedance to be independent of V_{IN}. The peak current $\hat{I}_1$ scales linearly with V_{IN}. So, at V_{IN} = 1 mV, $\hat{I}_1$ = 4 mA. The M_1 on-time $T_{i1,rise}$ needed to achieve this peak current was determined by

$$T_{\mathrm{i1,rise}} \approx L\frac{\hat{I}_1}{V_{\mathrm{IN}}}, \tag{5.1}$$

which solves to $T_{i1,rise}$ = 1.2 ms. This is an approximation. Due to the resistance of M_1 and the transformer primary coil, the actual value needed to be $T_{i1,rise}$ = 1.3 ms.

To maximize DC-DC converter efficiency, traditionally the sizing of power FET M_1 is adjusted to balance the conduction losses due to the channel resistance $E_{M1,cond}$ and the losses due to driving the M_1 gate plus the drain capacitance losses at the most important operating point (here it is at V_{IN} = 1 mV), such that

$$E_{\mathrm{M1,cond}} = E_{\text{Gate-Drive}} + E_{\mathrm{C,D1}}, \tag{5.2}$$

while assuming that

$$E_{\mathrm{M1,cond}} \propto \frac{1}{E_{\text{Gate-Drive}} + E_{\mathrm{C,D1}}}, \tag{5.3}$$

where

$$E_{\mathrm{M1,cond}} = \frac{1}{3}\hat{I}_1^2 R_{\mathrm{on1}} T_{\mathrm{i1,rise}}. \tag{5.4}$$

Due to the high turns ratio of the flyback transformer in this application, $E_{C,D1}$ losses are practically zero and can be ignored (see Section 2.1.1). With the use of stepwise gate-drive, the energy required to drive the gate of M_1 is determined by the many parameters of the stepwise gate driver, which goes through its own optimization. Taking this into account, the goal is now to adjust the sizing of M_1 to balance the losses of the stepwise gate driver with the M_1 conduction losses such that,

$$E_{\text{Gate-Drive}} + E_{\text{Switch-Drive}} \approx E_{\text{M1,cond}}, \tag{5.5}$$

where $E_{\text{Gate-Drive}}$ is defined as $E_{\text{Load-Driver}}$ in Chapter 3 and $E_{\text{Switch-Drive}}$ is the energy required to drive the switches within the stepwise gate driver as described on page 40.

The stepwise gate driver was optimized based on the following parameters

- The number of steps, N
- Resistance R_{SF} of the falling-edge stepwise switches S_F
- The total v_{G1} fall-time, T_F.

The fall time of the M_1 gate T_F affects the M_1 transition losses as explained in Section 2.1.1. Therefore, an appropriate T_F must be chosen that balances the M_1 transition losses with the gate-drive and switch-drive losses within the stepwise gate driver. The stepwise gate driver was optimized by minimizing the net losses $E_{SW,net}$ that are sensitive to stepwise driver design parameters N, R_{SF}, and T_F:

$$E_{\text{SW,net}} = E_{\text{Gate-Drive}} + E_{\text{Switch-Drive}} + E_{\text{Tran-Loss}}, \tag{5.6}$$

where $E_{\text{Gate-Drive}}$ and $E_{\text{Switch-Drive}}$ are calculated using the method described in Section 3.2 (terminology equivalence defined by (3.62)-(3.64)). For calculating $E_{\text{Switch-Drive}}$, the MOSFET quality factor is approximated as $\rho_{R,k} = \rho_{F,k} = \rho = 670$ pJ-Ω as determined through simulation.

$E_{\text{Tran-Loss}}$ is determined by interpolating the simulated data of Figure 2.3. The total v_{G1} transition time T_F is a function of step duration T_{SF} and number of steps N:

$$T_F = NT_{SF}. \tag{5.7}$$

C_{Tank} should be as large as possible for the available die area, with C_{Total} being the total capacitance that can fit on the die:

$$C_{\text{Total}} = (N-1)C_{\text{Tank}}. \tag{5.8}$$

For the available die area in this design, C_{Total} = 12 nF.

Figure 5.1 shows $E_{SW,net}$ and its components plotted against N, R_{SF}, and T_F. These parameters were iteratively adjusted to give approximately the lowest $E_{SW,net}$ for the chosen M_1 sizing. The values used in the design do not exactly correspond to the lowest $E_{SW,net}$ in Figure 5.1 due to choosing to limit N to 9 for easier implementation and also due to the losses in the voltage doubler circuit in Figure 3.9 that drives the stepwise switches S_F consuming more energy than predicted.

Since the rising edge of v_{G1} does not have a significant effect on transition losses, T_R, T_{SR}, and R_{SR} were omitted from the optimization algorithm. Instead, the resistance of rising-edge switches S_R was set to be $R_{SR} = 8R_{SF}$, and the total v_{G1} rise-time was set to be $T_R = 70T_F$, giving ample time for settling.

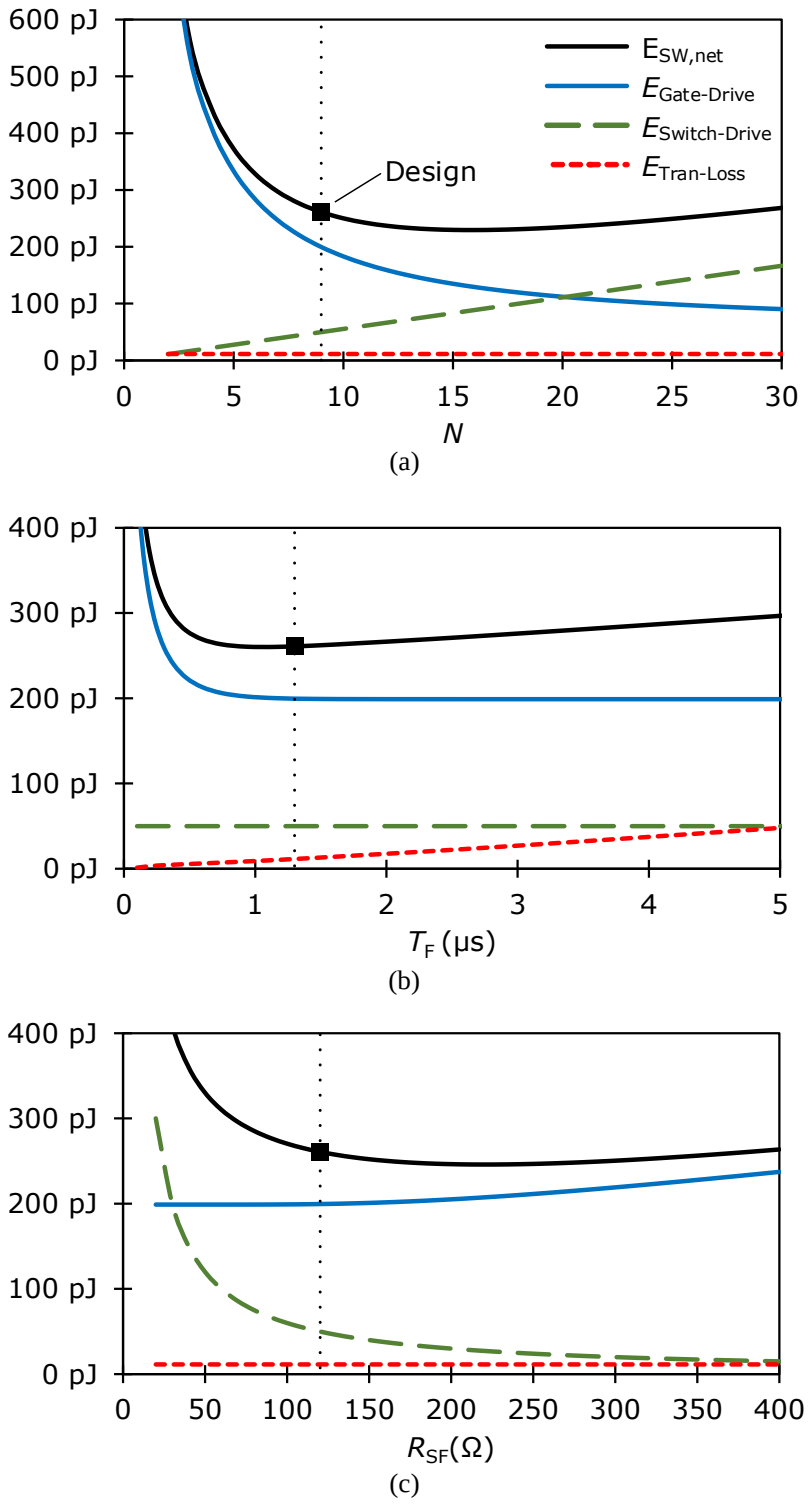

Figure 5.1. Optimizing the energy losses of stepwise gate-drive for number of steps N (a), total v_{G1} fall-time T_F (b), and S_F switch resistance R_{SF} (c). When not swept: $N = 9$, $T_F = 1.3$ µs, $R_{SF} = 120$ Ω (the values used in the design). $V_{DD} = V_{OUT} = 2.5$ V, $\hat{I}_1 = 4$ mA.

Chapter 6.
PHYSICAL DESIGN

This chapter explains the physical design of the DC-DC converter. Section 6.1 describes the physical design of the integrated circuit (IC), while Section 6.2 describes the printed circuit board (PCB) design.

6.1 INTEGRATED CIRCUIT LAYOUT

The DC-DC converter integrated circuit was designed in a 600-nm CMOS process with three available metal layers for routing. Figure 6.1 shows the integrated circuit layout. There are 59 bondpads around the parameter. The bondpads were sized at 120 μm wide to accommodate 2-mil gold bondwires, which have one-fourth the resistance of a standard 1-mil gold bondwire. Along the top of the die are 15 ground (GND) pads and 14 v_{D1} pads. These two nets require very low resistance to maintain good DC-DC converter efficiency, which is why so many pads are allocated to these two nets. Primary power FET M_1 runs parallel just below the GND/v_{D1} pads. Placing M_1 in this position and aspect ratio minimizes the metal routing resistance from the source and drain of M_1 to the pads. The GND and v_{D1} pads alternate to minimize the horizontal current flow, which affects the total resistance. The total resistance of the metal routing and bondwires connecting M_1 to GND and v_{D1} is estimated to be 6 mΩ, which effectively adds to the channel resistance of M_1.

Toward the top of the right side of the die, secondary power FETs M_{2P} and M_{2N} are located, with the corresponding pads for nets v_{D2P} and v_{D2N}. Located just below is net V_{OUT}, which is used to power the control circuitry as well as for monitoring through the voltage monitor circuit. The M_1 gate voltage v_{G1} is routed from M_1, down the right-side of the die to the control circuitry on the

bottom-right corner of the die, where it is driven by the stepwise gate driver switches. The gate voltage v_{G1} is then brought to a pad on the bottom-left of the die for experimental measurements.

The C_{Tank} capacitors for the stepwise gate driver consume the majority of the die area. Since the efficiency of the stepwise gate driver is improved with larger C_{Tank} capacitance, it is beneficial to use all available die area to maximize this capacitance. Die area could be reduced by reducing the C_{Tank} capacitance at the expense of stepwise gate driver efficiency as shown in Figure 5.1.

The control circuitry is located at the bottom-right of the die—far from the switching power FETs, minimizing interference from power FET switching. The slow delay line circuit extends the entire length of the die as it contains a thousand delay stages—all in a row. Each control input has a dedicated pad on the bottom and lower-right of the die. This was done for simplicity. A more efficient use of die area would be to use a serial interface to shift in the values for each control bit, thereby only requiring pads for clock and data. No pads are placed on the left side of the die because the circuit board ground plane would make it difficult to route bond wires to those pads.

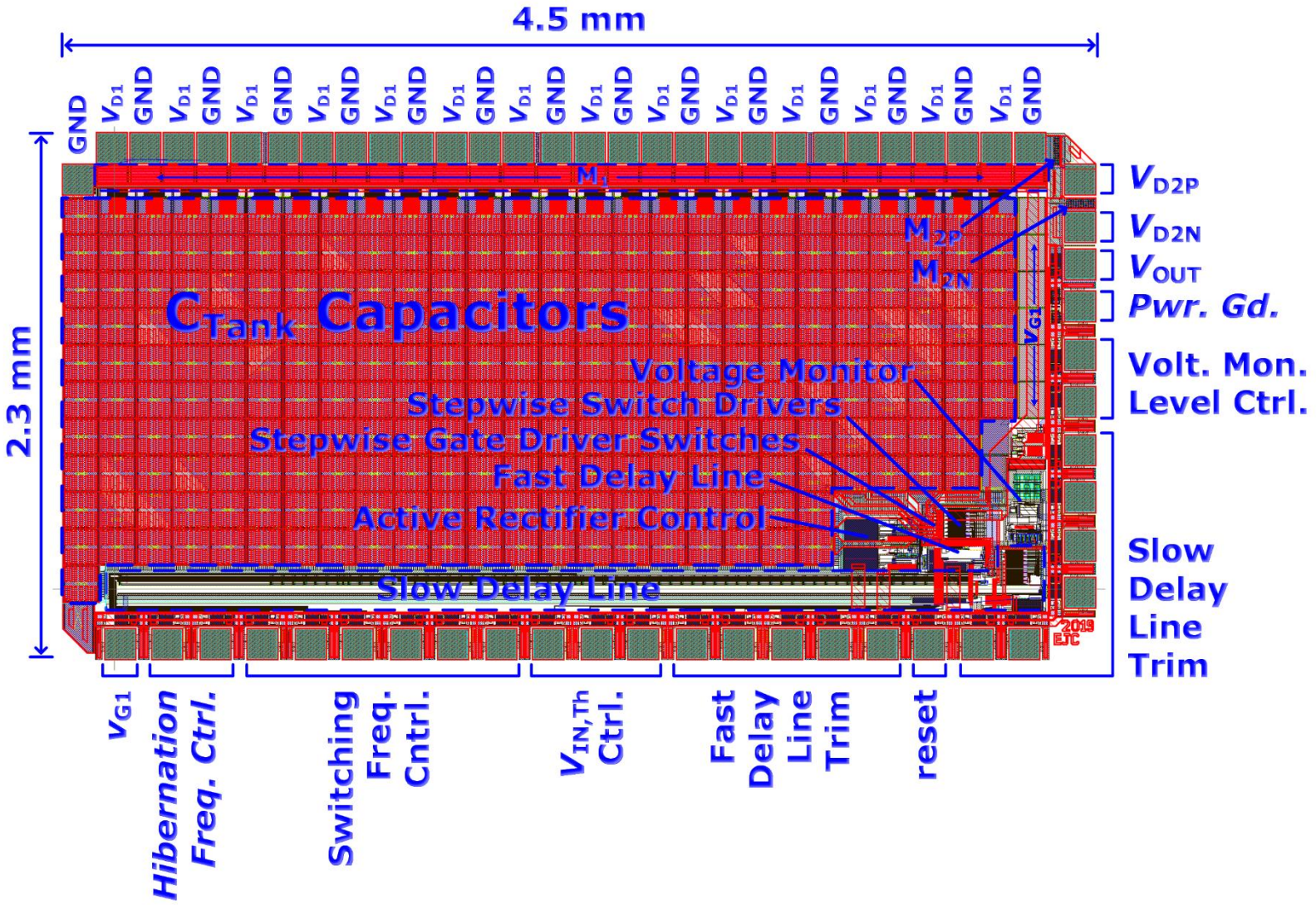

Figure 6.1. Integrated Circuit Physical Layout Design.

6.2 PRINTED CIRCUIT BOARD LAYOUT

Figure 6.2 shows the printed circuit board layout. To minimize parasitic resistances the board was designed such that the IC die can be mounted directly to the circuit board without a semiconductor package. Bondwires electrically connect the die bondpads directly to the circuit board. The flyback transformer is placed just north of the IC, with a small copper plane dedicated to the high-current v_{D1} node. The v_{D2P} and v_{D2N} connections for the transformer secondary windings are located near the top-right corner of the IC.

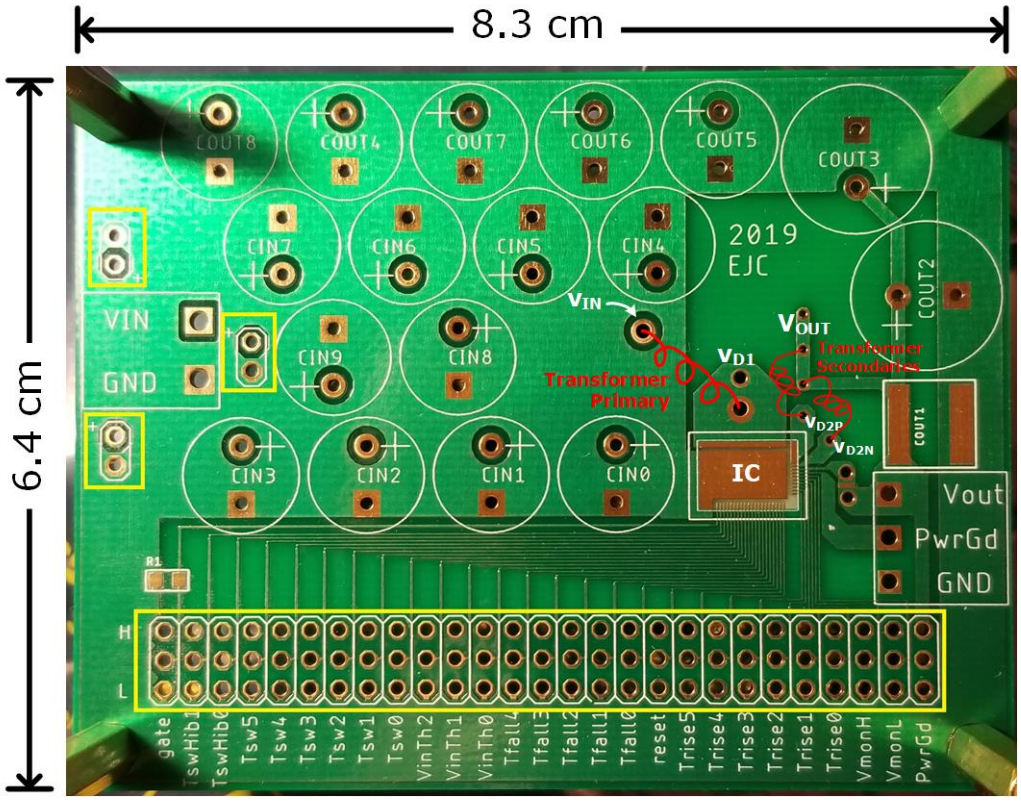

Figure 6.2. Printed Circuit Board layout.

Footprints for input capacitors C_{IN} fill the center of the circuit board. DC-DC converter efficiency is sensitive to resistance in the V_{IN} path—including C_{IN} ESR—so all C_{IN} are placed as close to the transformer primary as possible. The top PCB copper layer has a ground plane under

the C_{IN} footprints, while there is a V_{IN} plane on the bottom PCB copper layer. This circuit board has only two copper layers. Output capacitors C_{OUT} were placed at the periphery since circuit performance is less sensitive to C_{OUT} ESR. A ceramic capacitor (470 nF) was placed close to the IC to suppress noise on the V_{OUT} node entering the IC, although this is probably not necessary.

Input and output signals are routed from the IC to jumper pins on the PCB (outlined in yellow). The center jumper row is the signal, the top row is V_{OUT} ("H"), and the bottom row is ground ("L"). Each control input is programmable by adjusting the jumper position. The M_1 gate signal is routed with more spacing around it to minimize parasitic capacitance, which would slightly degrade DC-DC converter efficiency but also degrade measurement bandwidth. A footprint for a 3 GΩ resistor between the M_1 gate signal and ground is included. This resistor keeps v_{G1} from drifting high when not driven by the stepwise gate driver (this was added because the gate driver design did not include a v_{G1} pulldown during disable or hibernation). Jumpers are also placed on the left side of the PCB for Kelvin connections [68], [69] to the V_{IN} and ground planes. Low-impedance screw-type power jack connectors are used for the current-carrying V_{IN} and V_{OUT} connections.

6.3 Finished Product

Figure 6.3 shows a micrograph of the fabricated integrated circuit. The details of which are shown in the IC layout design in Figure 6.1. Figure 6.4 shows a zoomed-in micrograph of the IC control circuitry on the bottom-right corner of the die. It shows the voltage monitor, stepwise switch drivers (voltage doublers), stepwise gate driver switches, active rectifier control, fast delay line, and part of the slow delay line as located in Figure 6.1. It also shows the metal routing to the C_{Tank} capacitors and the M_1 gate (v_{G1}).

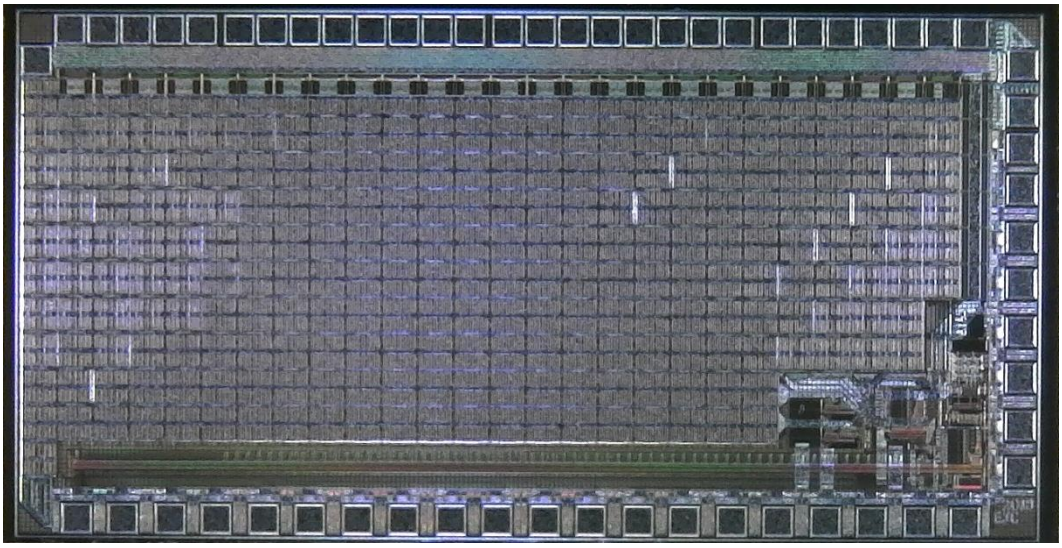

Figure 6.3. Integrated circuit micrograph.

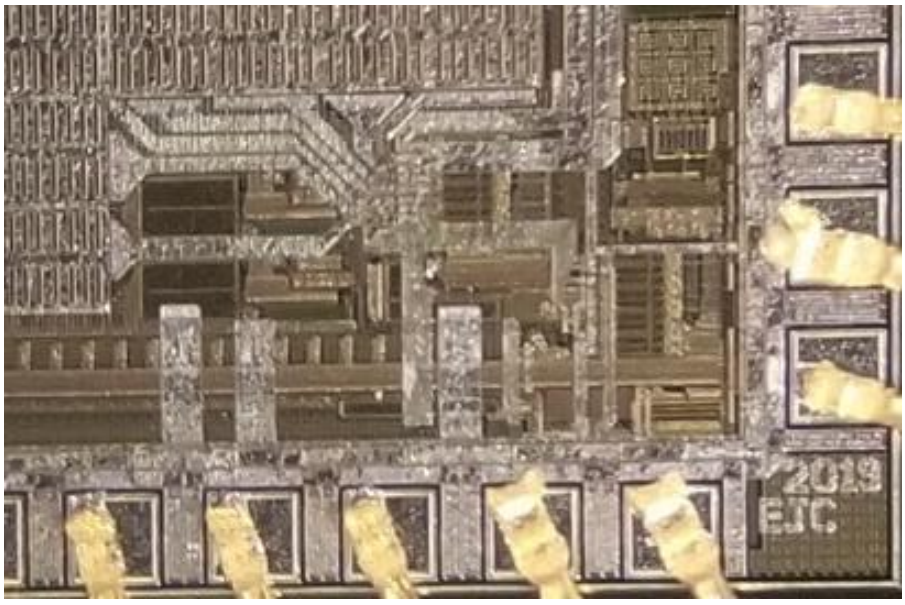

Figure 6.4. Integrated circuit micrograph zoomed in on the control circuitry.

Figure 6.5 shows the IC as it is attached and bonded to the circuit board. The die was epoxied directly to the exposed PCB ground plane and each GND pad was bonded to that ground plane. The v_{D1} plane is located above the ground plane and also bonded to the IC v_{D1} pads with 2-mil bondwires. 2-mil gold bondwires were used to provide one fourth the resistance as 1-mil bondwires.

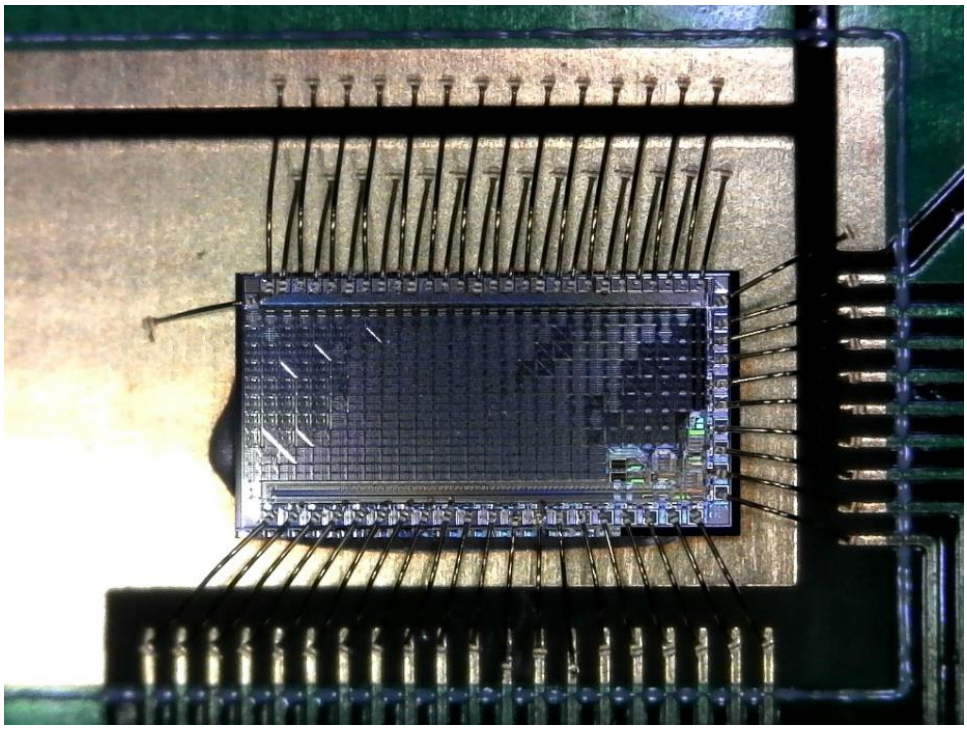

Figure 6.5. Integrated circuit die attached and bonded to the circuit board.

A photograph of the finished DC-DC converter circuit is provided in Figure 6.6. The IC die is encapsulated in a black glob. The toroid flyback transformer stands upright. Connections for the V_{IN}/GND input and V_{OUT}/*power_good*/GND outputs are made with top-loading screw-type connectors. Jumpers allow setting the control signals.

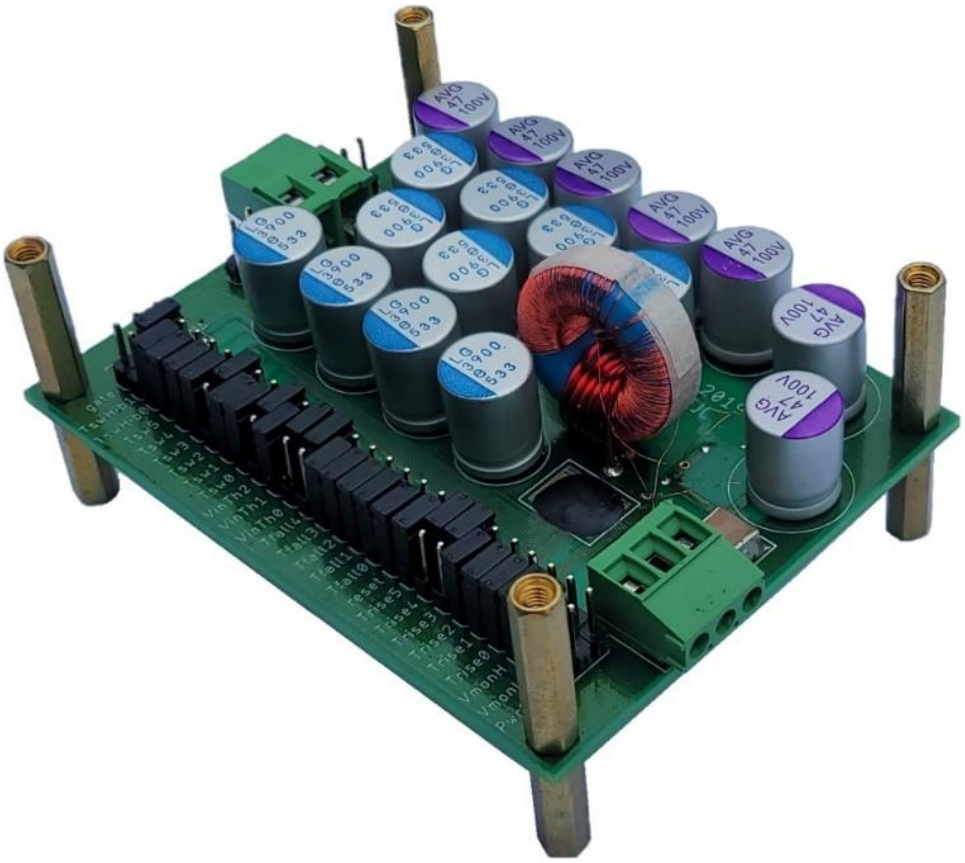

Figure 6.6. Finished DC-DC converter circuit.

6.1 BONDING FAILURES

Initially five dice were mounted and bonded to circuit boards, using 2-mil gold bondwires attached to the bondpads using “wedge” [70] bonds as in Figure 6.4 and Figure 6.5. Four of these five units were found to have a short circuit to ground on one or more bondpad. Only one unit was free of short circuits. Problems with the die itself were ruled out by probing three unmounted dice—showing no shorts on any pad. It was determined that during the bonding process the bondwire wedge joint would occasionally break through the insulating layer on the bondpad and contact with the underlying silicon substrate. Since the silicon substrate is electrically connected to ground, the pad became connected to ground through the substrate. To resolve this problem for subsequent

productions, only the v_{G1} and GND bondpads (the nets most sensitive to resistance) were bonded with 2-mil bondwire. The remaining bondpads were bonded with 1-mil wire, which is attached using the “ball” [70] bonding method, which does not create shorts. This reduced the number of pads susceptible to shorting from 44 to 14 (GND pads are already connected to ground). Five new units were mounted using this method and the resulting yield was 80%, a vast improvement to the initial yield of 20%.

Chapter 7.
HARDWARE MEASUREMENT AND CHARACTERIZATION METHODOLOGY

This chapter describes the challenges, methods, circuitry, and equipment used to test and characterize the DC-DC converter and its components. In order to characterized the circuit and components, the low voltages and circuits within the circuit need to be measured without significantly affecting the circuit performance.

7.1 Capacitor Leakage Measurement

Low-leakage output capacitors are required to achieve the total quiescent current of 100 pA drawn by the DC-DC converter from its output. Capacitor leakage current is not typically specified in datasheets and therefore finding the right capacitor required the characterization of many different capacitor types to find that which has acceptable leakage current. Measuring a capacitor leakage current that is in the order of pico-amps requires a measurement setup that can measure currents with this level of accuracy, while also driving the capacitor voltage to the application voltage of 2.5 V. The device typically used to perform such a measurement is a sourcemeter such as the Keithley 6430 [71]. This device can force a 2.5 V voltage at 6.4 mV accuracy while simultaneously measuring the current with 17 fA accuracy. However, per the manual [72], excessive ringing occurs when the capacitance is greater than 100 pF. The proposed DC-DC converter uses 47 μF capacitors for the output, so an off-the-shelf sourcemeter is unlikely to work. Instead, custom test fixtures were developed to measure capacitor leakage current. Two measurement methods were utilized: one that utilizes feedback and is more accurate but can only

measure one capacitor at a time, the other less accurate but can measure large batches of capacitors at a time.

7.1.1 *The feedback method*

A common sourcemeter implementation uses a feedback method to drive the DUT (device under test) through a current-sensing resistor with a voltage source while also sensing the voltage across the DUT and continuously adjusting the voltage to keep the voltage across the DUT at the target value. This feedback loop can be implemented using a properly compensated op-amp. The problem with using an opamp with standard RC compensation is that when trying to measure ~10 pA of leakage current for a 47 μF capacitor, the current sense resistor needs to be on the order of 1 GΩ for a sense voltage of 10 mV (smaller sense voltages are more difficult to measure accurately). This results in an RC time constant of 13 hours, which is difficult to compensate for using an RC compensation network with an op-amp. This is probably why the Keithley 6430 manual [72] states that excessive ringing will occur if measuring DUTs with capacitance greater than 100 pF.

To avoid hours-long time constants in an RC compensation network, a digitally controlled approach was used. This is shown in Figure 7.1. With this approach, a DAC drives the DUT capacitor through the current-sensing resistor and a digital PI controller [73] (implemented in software) adjusts the DAC voltage to keep the voltage across the DUT capacitor at 2.5V. The voltage across the capacitor is buffered with an AD8627 JFET-input op-amp [74] before being measured by a Keysight U2741A digital multimeter (DMM 2) [75]. The op-amp buffer is needed to prevent the input current of the DMM from affecting the measurement. The AD8627 datasheet specifies a maximum room-temperature input bias current of ±1 pA and offset voltage of ±0.5 mV. These parameters [76] affect the accuracy of the leakage current measurement. However, errors

due to the bias current and offset can be mitigated by measuring the leakage current without the DUT capacitor in place and subtracting the result from the final measurement as a form of calibration. These parameters are sensitive to temperature, so it is important to keep the temperature consistent between calibrating the measurement circuit and measuring the leakage current of the DUT. Voltage offset drifts due to noise [77] cannot be calibrated out (since it changes randomly over time) but can be minimized by choosing an R_{Sense} value that is large enough such that V_{Sense} is much larger than the expected drift in offset voltage. Op-amp input bias current drift due to noise cannot be compensated for. It simply must be much less than the expected leakage current of the DUT capacitor to get an accurate measurement.

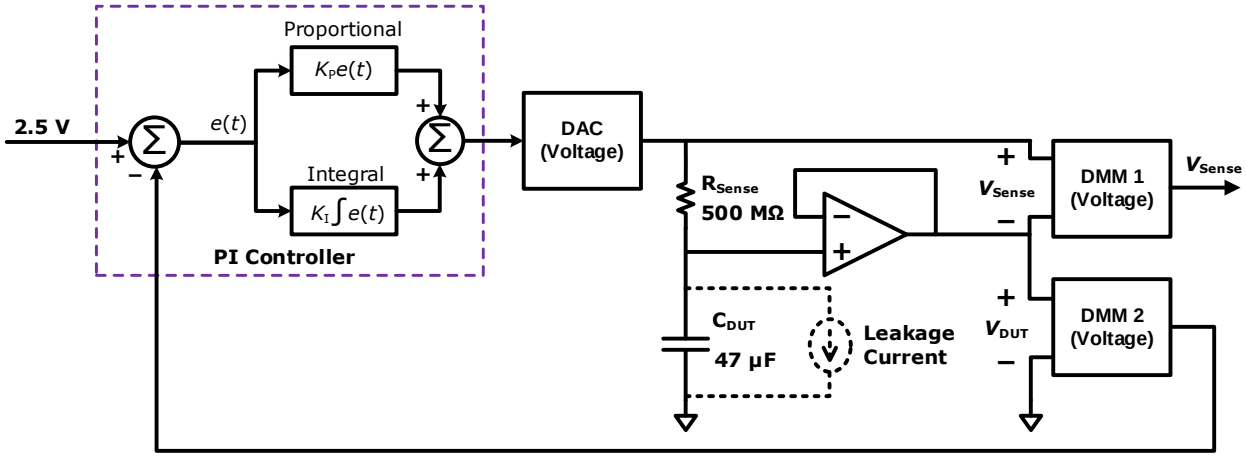

Figure 7.1. PI controlled capacitor leakage current measurement circuit.

The measured leakage current becomes

$$I_{\text{Leak,measured}} = \frac{V_{\text{Sense}} - V_{\text{OS}}}{R_{\text{Sense}}} + I_{\text{B}}. \tag{7.1}$$

where V_{Sense} is the voltage across the resistor (after the buffer) as measured by DMM 1 (a Keysight U2741A), V_{OS} is the offset voltage of the op-amp (and the offset of DMM 1 if it is significant), and I_{B} is the input bias current of the op-amp. The accuracy of this measurement can be determined by an offset error due to the op-amp offset voltage and bias current (and can be measured by

measuring V_{Sense} with no DUT capacitor connected) and a gain error due to the resistor tolerance of R_{Sense} (1% resistors were used).

Theoretically, the quality of the DAC does not have much effect on the measurement accuracy. High frequency DAC noise is filtered by the bandwidth of DMM 1 and by averaging many measurements. Low frequency noise and drift are cancelled by the feedback loop. Therefore, a cheap solution was used for the DAC: a Labjack U3-HV [78]. This device includes two 10-bit DACs among other features. The DAC output voltages range from 0 V to 5 V and are PWM controlled. A single 10-bit DAC only has a resolution of 5 mV. To get better resolution both DACs are combined with a resistor network as shown in Figure 7.2.

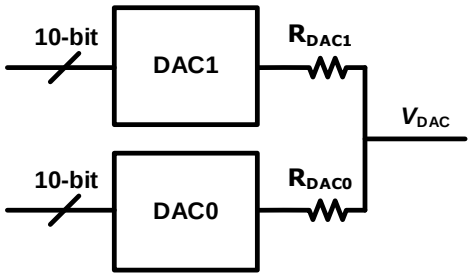

Figure 7.2. Using two 10-bit DACs to get finer resolution on the DAC output voltage V_{DAC}.

With this configuration the resolution becomes

$$\text{DAC Resolution} = \frac{5\text{ V}}{2^{10}} \frac{R_{\text{DAC0}}}{R_{\text{DAC0}} + R_{\text{DAC1}}}. \tag{7.2}$$

In this case DAC0 controls finer steps and DAC1 controls the larger steps. R_{DAC0} should be less than $R_{\text{DAC1}} \times 2^{10}$ so there is overlap in the DAC voltages. Note that this higher resolution DAC is not monotonic. This is tolerable if there is sufficient overlap such that once the feedback loop is mostly settled only DAC0 is adjusted. The chosen values were $R_{\text{DAC0}} = 4.7\text{ k}\Omega$ and $R_{\text{DAC1}} = 1.0\text{ M}\Omega$, which produces a DAC resolution of 23 μV.

Figure 7.3 shows the measured leakage current with no DUT capacitor in place to measure the offset current over 46 hours. The plotted current is averaged across a 1-hour window to better show the low-frequency drift among the noise. The plotted V_{DUT} voltage is averaged across a 1-minute window. The average of the measured current (ignoring the first hour) is 0.17 pA and the average of the measured V_{DUT} (ignoring the first hour) is 2.4999990 V (with a target of 2.5 V). The leakage current offset data suggests that one can be confident that the leakage current measurement offset will not exceed ±1 pA.

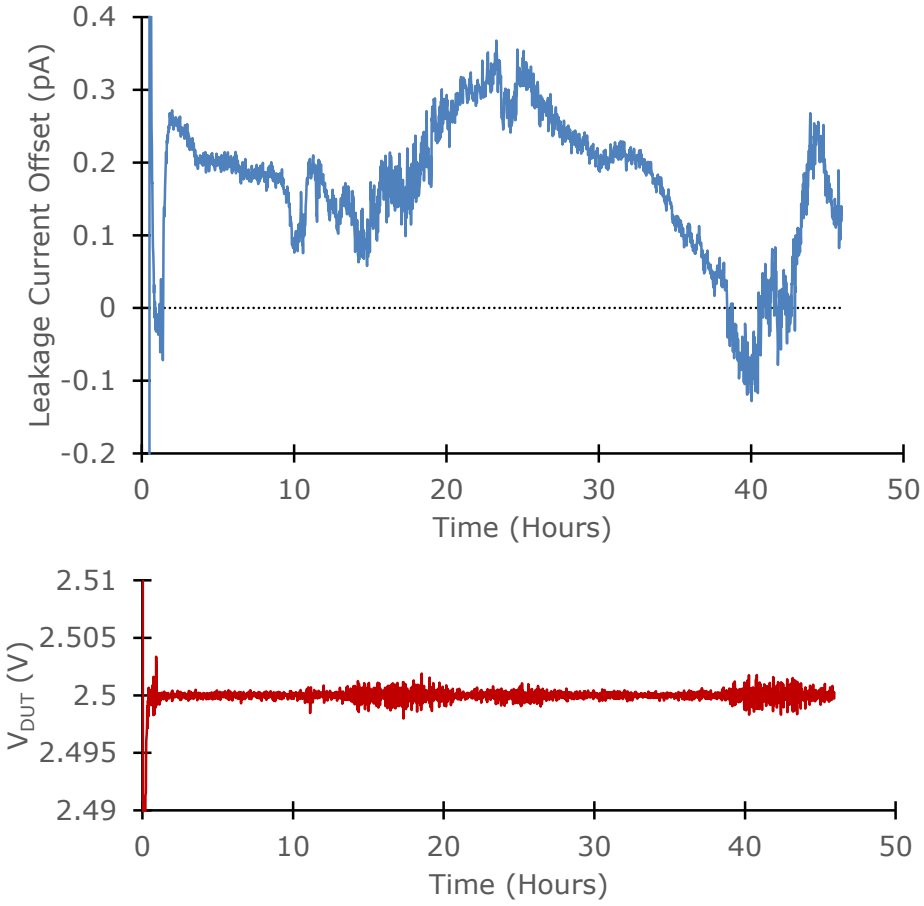

Figure 7.3. Capacitor leakage offset current and V_{DUT} voltage without a DUT capacitor in place to measure the leakage current offset of the test circuit. The current measurement is averaged over 1 hour and the V_{DUT} measurement is averaged over 1 minute. DMM readings are made once per second.

The leakage of the capacitor takes time to settle. This settling time is irrespective of the R_{Sense} resistance. Ike [79] explains the leakage settling as "pores" that are slowly filled with electrolyte. After all "pores" are filled—which can take several days—the leakage current reaches steady-state. Figure 7.4 shows capacitor leakage current settling over time, showing that it can take over a week for the leakage of the 47 μF capacitor [46] used for C_{OUT} to settle.

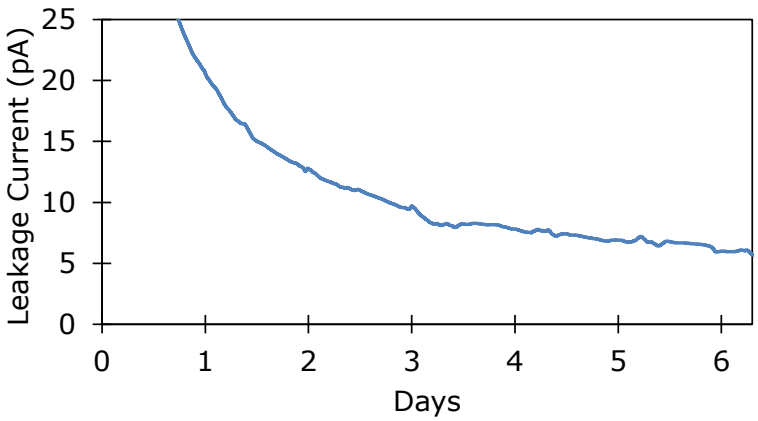

Figure 7.4. Leakage current of a 47 μF capacitor [46] measured over several days using the setup in Figure 7.1. Measured current was filtered with a 24-hour moving average filter.

7.1.2 *The batch method*

The feedback method works well for accurately measuring the leakage of a single capacitor, but it is inefficient for measuring a large number of capacitors at once. Since leakage can vary from one capacitor to another—even for capacitors coming from the same production batch—it is best to sort out only the lowest leakage capacitors to use in the design. This requires measuring the leakage of many capacitors at once. To do this, a batch of DUT capacitors are connected to a 2.5 V voltage supply through resistors as shown in Figure 7.5 and a DMM is moved quickly from one R_{Sense} to the next to measure each V_{Sense} voltage. R_{Sense} is 10 MΩ instead of 500 MΩ as used in the

more accurate leakage measurement circuit to keep the RC settling time reasonably low since there is no feedback loop to speed up the settling. When measuring the leakage of a 47 μF DUT capacitor the RC time constant is 8 minutes, so the capacitor voltage can be considered to be sufficiently settled after about 30 minutes. With an expected leakage current of about 10 pA, the voltage drop of R_{Sense} (V_{Sense}) is 100 μV, so the voltmeter that measured V_{Sense} must be sufficiently accurate. A Keysight (Agilent) 34401A DMM [80], which has a voltage measurement accuracy of ±3.5 μV was used for this measurement. This device has a high impedance (> 10 GΩ) mode, but the input bias current was found to still be about 30 pA for 100 μV-level voltages. Therefore, the DMM negative (black) probe would only be connected to the top plate of the DUT capacitor briefly, before the input current of the DMM changes the voltage of the capacitor significantly. Using the standard capacitor equation, the relationship between DMM leakage current and voltage drift is

$$I_{\text{DMM}} = C_{\text{DUT}} \frac{dv}{dt} \approx C_{\text{DUT}} \frac{\Delta V}{\Delta T}. \tag{7.3}$$

Solving with I_{DMM} = 30 pA, ΔV = 5 μV (maximum tolerable voltage drift), and C_{DUT} = 47 μF yields ΔT = 8 seconds. So, the DMM probe can connect to C_{DUT} for up to 8 seconds when taking the reading before DMM leakage current has a significant effect on the measurement.

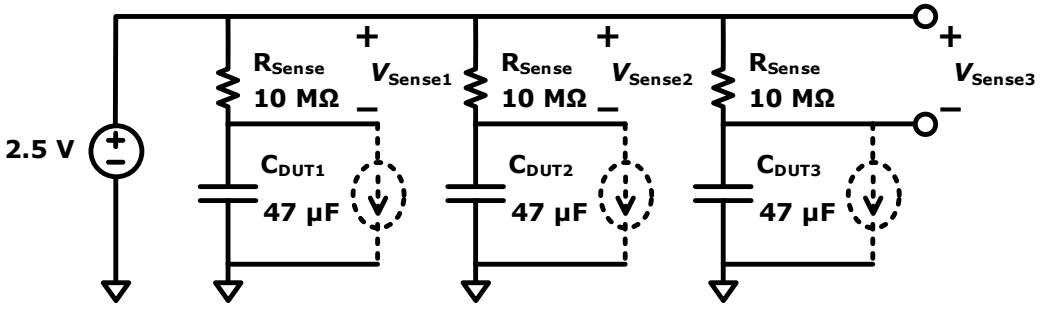

Figure 7.5. Capacitor leakage current batch measurement method.

Noise on the 2.5 V voltage source can influence the capacitor leakage measurement. With an expected V_{Sense} measurement of 100 μV, voltage source noise amplitudes greater than 10 μV would have a significant impact on the measurement. The frequency of the noise matters. The Keysight 34401A has a 3 Hz bandwidth on its minimum bandwidth setting, so at this setting voltage source noise greater than 3 Hz is less relevant. The measured RC corner frequency of C_{DUT} and R_{Sense} is 0.34 mHz. Voltage source noise below this frequency will have little effect on the measurement because the RC circuit will settle faster than the source voltage changes. Therefore, when selecting the regulator that provides the 2.5 V source, it should have less than 10 μV noise amplitude between 0.34 mHz and 3 Hz. The LT1019 is the regulator that was used for the 2.5 V source. The datasheet [81] claims a noise amplitude of 2.5 ppm or 6 μV peak-to-peak in the frequency range of 0.1 Hz to 10 Hz. It does not specify the noise less than 0.1 Hz, so the regulator had to be characterized to confirm that the noise is below 10 μV for 0.34 mHz to 0.1 Hz.

Like drift due to noise, drift due to temperature change is also a concern. The LT1019 datasheet claims a temperature coefficient of 5 ppm/°C (12.5 μV/°C) typical and 20 ppm/°C (50 μV/°C) worst-case. Assuming the typical temperature coefficient, temperature changes greater than 1°C in a 1-hour period (the RC bandwidth) should be avoided for reasonable measurement accuracy.

Figure 7.6 shows the output voltage of the LT1019 used for the 2.5 V source for a 10-hour period (measured with Keysight 34401A with 3 Hz bandwidth enabled). It also shows the measured data with a 0.34 mHz high-pass filter applied to the data to emulate the noise that would be seen across the R_{Sense} resistor (V_{Sense}). It shows that the regulator and measurement noise in the relevant band of 0.34 mHz to 3 Hz is less than 5 μV, which would correspond to 0.5 pA of noise

in the leakage current measurement, or a 5% error assuming a capacitor leakage of 10 pA. This voltage error is comparable to the ±3.5 μV voltage accuracy of the 34401A DMM.

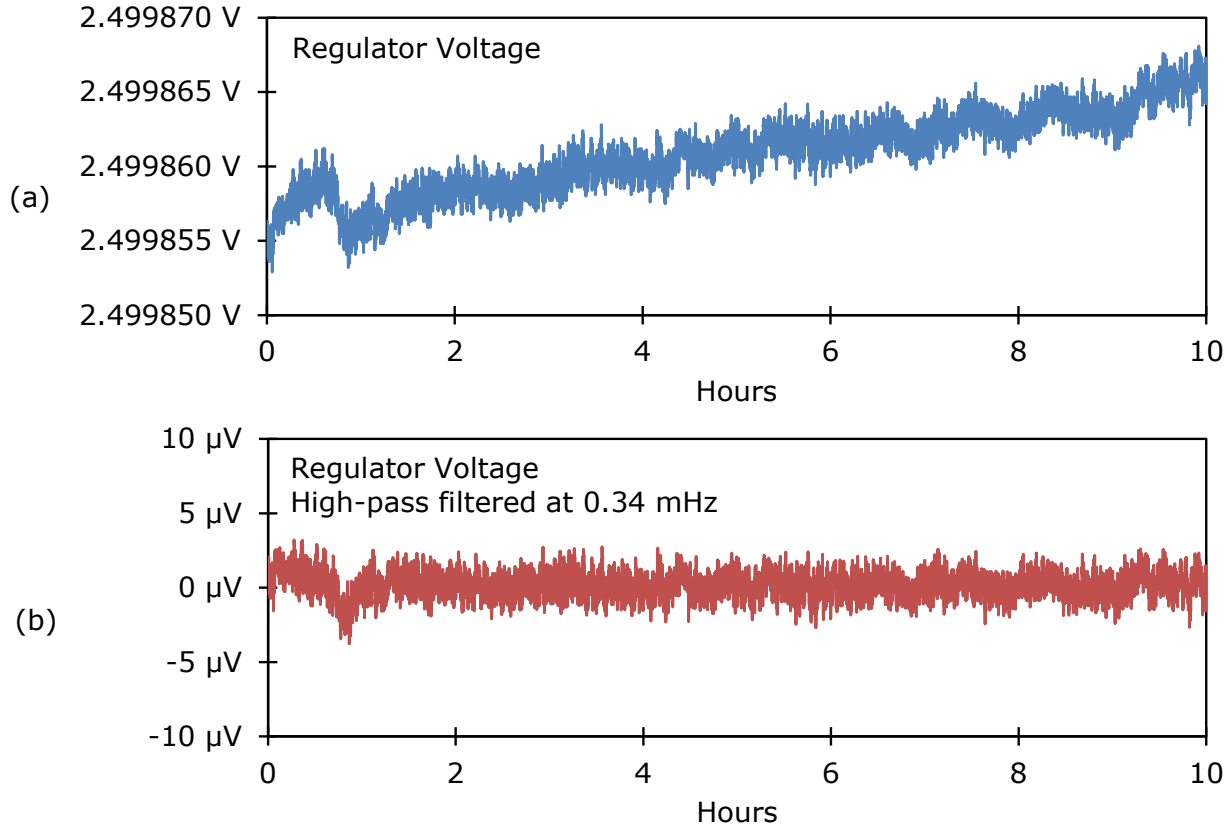

Figure 7.6. (a) Measured 2.5 V regulator output voltage. (b) Measured regulator output voltage with 0.34 mHz high-pass filter applied to emulate V_{Sense} noise.

Besides the input current of the DMM affecting the measured V_{Sense} voltage, also the input capacitance of the DMM can affect the measurement as charge accumulated on the probes before connecting across R_{Sense} will discharge into the DUT capacitor once connected. The charge redistribution will cause a small voltage error. The Keysight 34401A specifies a maximum input capacitance of 700 pF, which would cause a 15 μV (with C_{DUT} = 47 μF) shift in the V_{Sense} voltage (which corresponds to 1.5 pA) for every 1 V of pre-charge on the DMM probes. To avoid this error, both the positive (red) and negative (black) probes of the DMM are first connected to the

2.5 V node to eliminate any charge between the probes. Then the negative probe is connected to the top plate of the DUT capacitor to measure V_{Sense} and calculate the leakage current.

7.2 Quiescent Power Measurement

Measuring the quiescent power of the DC-DC converter uses the same measurement circuitry as the capacitor leakage measurement, with the DC-DC converter as the DUT instead of just a single capacitor. The PI controller gain values must be adjusted to accommodate the total output capacitance of 7×47 μF. The input to the DC-DC converter was forced to 0 V through a dead short so no power can be drawn from the input and all consumed power comes from the test fixture connected to the V_{OUT} pin. After allowing several days at V_{OUT} = 2.5 V for the leakage of the output capacitors to settle, the leakage current averaged to 102 pA. Figure 7.7 shows the measured leakage current over a 53-hour period after the capacitor leakage has already settled. The data is filtered with a moving-average filter to improve signal-to-noise ratio. Figure 7.7 (a) shows the measured current with a 5-second averaging window (5 data points 1 second apart), (b) shows with a 1-hour averaging window, and (c) shows with a 10-hour averaging window.

The offset error measured in Figure 7.3 shows that one can comfortably assume the worst-case offset error is less than ±1 pA. The plot with 5-second averaging shows large spikes in the current measurement. These spikes are due to the DMM 2 occasionally measuring V_{OUT} (V_{DUT}) to be about 1 mV lower on a single data point. It is unclear whether this is DMM instrument error or if the voltage is actually reducing by 1 mV. Regardless, these spikes are sparse and get averaged out over time. The feedback loop aggressively compensates for the sudden 1 mV dip causing the DAC voltage to increase substantially and thereby temporarily increasing V_{Sense}. The current measurement plot with a 1-hour averaging window is still considerably noisy. Using a 10-hour averaging window reveals a diurnal pattern that is believed to be due to daily fluctuations in room

temperature. This suggests that the accuracy of the current measurement is overshadowed by the variations in current due to changes in room temperature. Room temperature was not actually measured for this experiment.

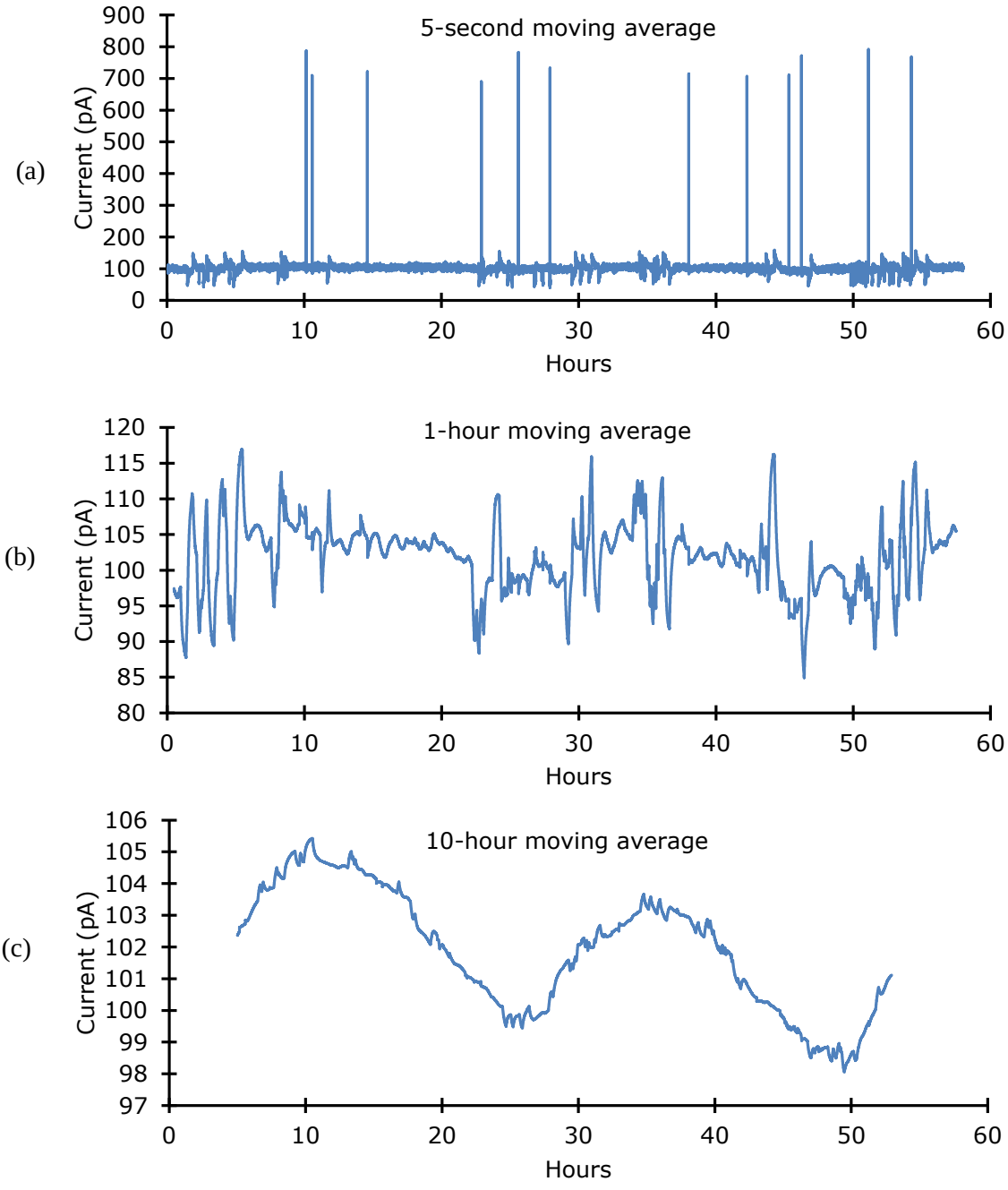

Figure 7.7. Quiescent current measurement over 53 hours with 5 second (a) 1 hour (b), and 10 hour moving average windows.

The average of the quiescent current measurement across the 53-hour duration is 101.9 pA. The measurement accuracy is the offset accuracy (due to op-amp V_{OS} and I_B) plus the gain accuracy (due to R_{Sense} resistor tolerance and DMM gain error). Table 7.1 shows the list of error sources and their affect on the accuracy of the quiescent current measurement, showing that the measurement accuracy for a 102 pA quiescent current measurement is ±2 pA.

Table 7.1. Quiescent current measurement error sources

Source of Error	**Error Amount**	**Effect on the 102 pA I_q Measurement**
op-amp V_{OS} and I_B	< 1 pA	±1 pA
R_{Sense} tolerance	±1%	±1.02 pA
DMM 1 gain error	±0.015%	±0.0153 pA
Total	1 pA + 1%	±2 pA

Measuring quiescent power also requires accurately measuring and controlling the voltage, V_{OUT}. Figure 7.8 shows the V_{OUT} (V_{DUT}) voltage with similar averaging windows as used in Figure 7.7. The 1 mV dips in voltage that cause the spikes in the current measurement are clearly visible in the plot with 5-second averaging. With 10-hour averaging a small 4 μV amplitude is seen as the system responds to the diurnal changes in temperature. The average measured voltage is 2.5 V + 1 μV, showing good regulation by the PI controller. Since V_{OUT} is relatively large at 2.5 V, the voltage error due to the op-amp offset (< 1 mV) and the voltage error of the DMM (±0.015%, 375 μV) are insignificant for the power measurement compared to the measurement error of the current. The quiescent power of the DC-DC converter then becomes the quiescent current multiplied by V_{OUT}. Therefore, the quiescent power measurement becomes 102 pA × 2.5 V = 255 pW with a measurement error of ±2 pA × 2.5 V = 5 pW.

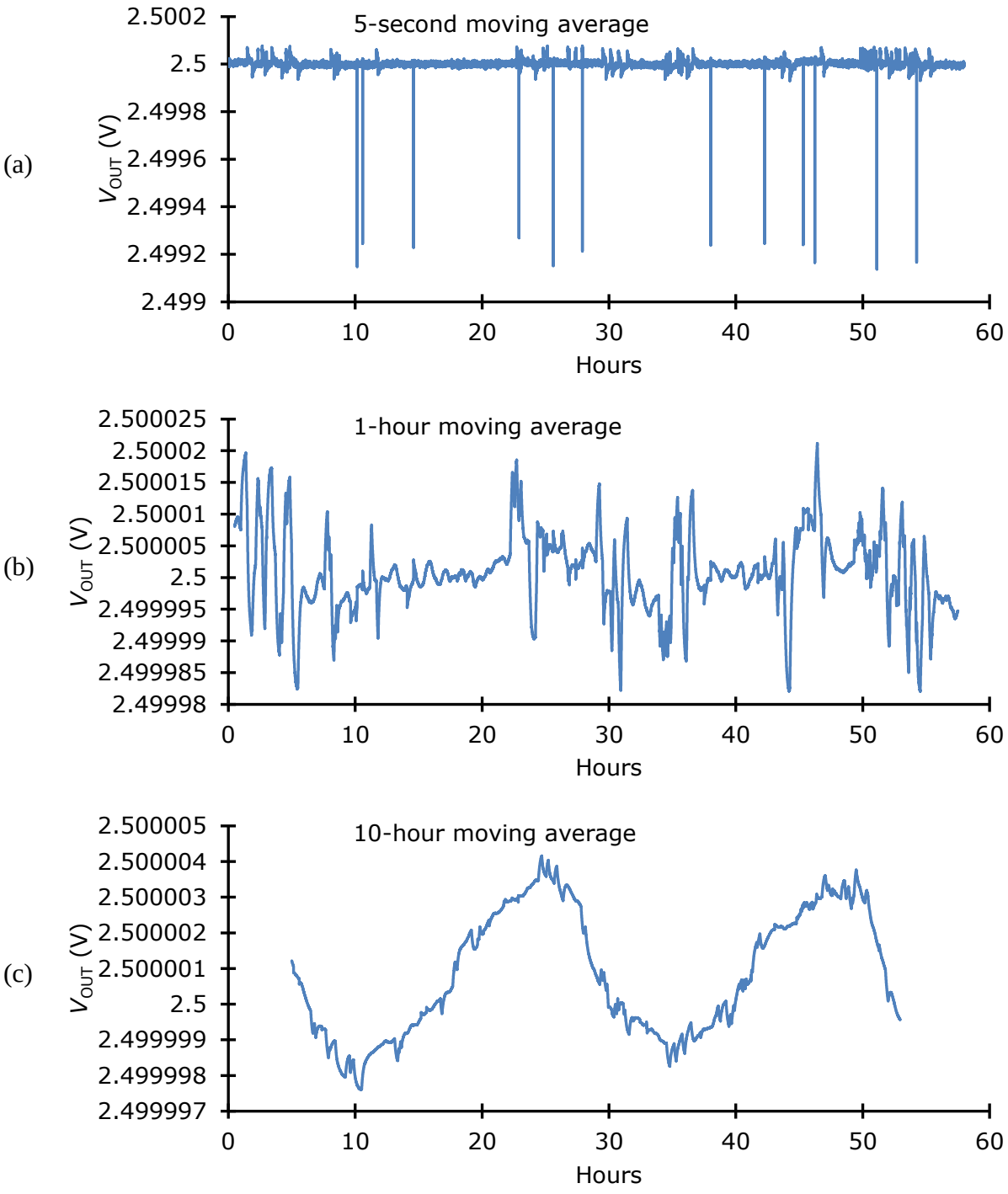

Figure 7.8. V_{OUT} (V_{DUT}) measurement over 53 hours with 5 second (a) 1 hour (b), and 10 hour moving average windows.

7.3 Efficiency Measurements

Measuring the efficiency of the DC-DC converter involves forcing V_{OUT} to a voltage while measuring the output current I_{OUT} (like what was done to measure the quiescent power consumption) and also forcing V_{IN} to a voltage while measuring the input current I_{IN}. The efficiency is calculated by:

$$\text{Efficiency} = \frac{P_{IN}}{P_{OUT}} = \frac{V_{IN}I_{IN}}{V_{OUT}I_{OUT}}. \quad (7.4)$$

The next two sections will explain how P_{OUT} and P_{IN} are measured.

7.3.1 *Measuring output power*

Forcing V_{OUT} for efficiency measurements was done in a slightly different way from the method used in the quiescent current measurement. I_{OUT} is much higher in normal operation than in hibernation. Therefore, instead of using a 500 MΩ R_{Sense} resistor, an R_{Sense} resistor ranging from 600 Ω to 500 kΩ (chosen depending on the expected I_{OUT}) was used. With this range of R_{Sense} resistance, an op-amp feedback circuit can be used and the compensation resistors can be practical values. The circuit in Figure 7.9 was used to force V_{OUT} to a target value while measuring I_{OUT}. V_{OUT} is connected to the negative input of the op-amp through a 10 MΩ resistor R_{FB} (used for stability compensation). The op-amp output sinks all of the I_{OUT} current. Most of that current flows through R_{Sense} while some flows through the 10 MΩ input impedance of the DMM (Keysight U2741A). I_{OUT} is measured from the parallel combination of R_{Sense} and the 10 MΩ DMM input impedance:

$$I_{OUT} = V_{Sense}\left(\frac{1}{R_{Sense}} + \frac{1}{10\ \text{MΩ}}\right). \quad (7.5)$$

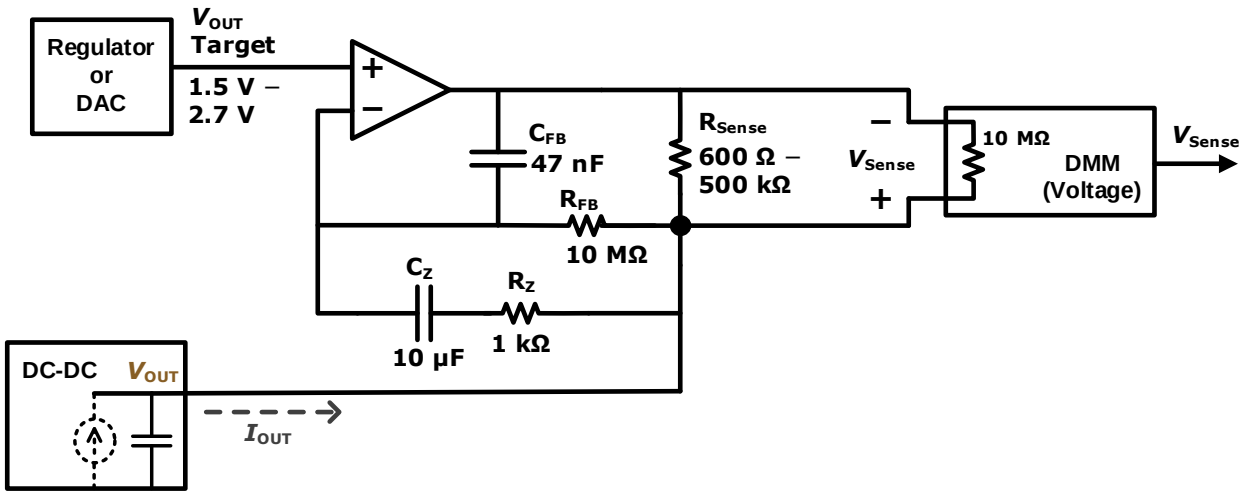

Figure 7.9. Circuit for forcing V_{OUT} and measuring I_{OUT} for efficiency measurements.

The op-amp is the same low-input-bias-current op-amp used for the quiescent current measurements (AD8627). With 1 pA of input bias current the voltage drop across the 10 MΩ R_Z is just 10 μV, while the worst-case op-amp offset is 500 μV per the datasheet, which is only 0.02% of V_{OUT} when V_{OUT} = 2.5 V. Components C_{FB}, R_{FB}, C_Z, and R_Z create a compensation network to keep the feedback loop stable while driving the 330 μF C_{OUT} of the DC-DC converter. C_{FB} is low-leakage (< 1 pA) to avoid causing a voltage offset across R_{FB}. C_Z and R_Z are optional, but without them $C_{FB}R_{FB}$ must be about 10x greater than $R_{Sense}C_{OUT}$ to get sufficient phase margin for stability. This would make the settling time take over one hour to settle. With C_Z and R_Z the $C_{FB}R_{FB}$ product can be much smaller by creating a zero in the transfer function that compensates for the pole created by $R_{Sense}C_{OUT}$. When R_{Sense} = 600 Ω the phase margin is better without C_Z and R_Z so they are removed.

Table 7.2 lists the error sources of the output power measurement for when V_{IN} = 1 mV and V_{OUT} = 2.5 V. Due to a limited number of DMMs, V_{OUT} is not continuously measured. Instead, V_{OUT} is measured once with the assumption that the 2.5 V regulator voltage and the op-amp offset does not change significantly over time. The accuracy of the initial V_{OUT} measurement is the

accuracy of the 34401A DMM that takes the measurement. The drift in the 2.5 V regulator and the op-amp over time are an additional source of error. Likewise, R_{Sense} is measured once. The initial resistance measurement accuracy is defined by the accuracy of the 34401A, but the resistance can drift due to changes in room temperature and also due to self-heating. Resistance sensitivity to temperature is provided in the resistor datasheet along with the expected temperature rise due to self-heating. Thin-film resistors are used as they have a much lower temperature sensitivity than carbon resistors.

Table 7.2. Output power measurement error sources for V_{IN} = 1 mV, V_{OUT} = 2.5 V, F_{SW} = 350 Hz.

Source of Error	**Effect on P_{OUT} Measurement**
V_{OUT} initial measurement (34401A voltage measurement accuracy)	±0.0055%
V_{OUT} drift after initial measurement (2.5 V regulator drift and op-amp offset drift)	±0.0105%
50 kΩ R_{Sense} initial measurement (34401A resistance measurement accuracy)	±0.0120%
R_{Sense} drift after initial measurement (due to temperature change)	±0.0125%
U2741A 10 MΩ input impedance accuracy (±3%) in parallel with R_{Sense}	±0.0150%
V_{Sense} measurement accuracy (U2741A voltage measurement)	±0.0823%
Total	±0.14%

7.3.2 *Measuring input power*

Measuring the DC-DC converter input power requires forcing V_{IN} while simultaneously measuring V_{IN} and I_{IN}. Two methods were used for forcing V_{IN} while measuring I_{IN}. The first

method simply drives V_{IN} through a resistor, while the second method drives V_{IN} using an op-amp feedback loop.

7.3.2.1 The resistor divider method

By driving V_{IN} through an R_{Sense} resistor, the input current I_{IN} can be determined by measuring the voltage across R_{Sense}. Since the input of the DC-DC converter is designed to have a resistance that is independent of V_{IN}, the approximate V_{IN} is set by a resistor divider equation. Figure 7.10 shows the circuit for when the DC-DC converter input impedance is programmed to be near 1 **Ω**. A $R_{||}$ = 1 **Ω** resistor is placed in parallel with V_{IN}, which serves three purposes. First, it prevents V_{IN} from being too high if the DC-DC converter is disabled by providing an additional current path. Second, it emulates the output resistance of a matched TEG. Third, it can improve the accuracy of the input power measurement when the measurement error is dominated by the accuracy of the V_{IN} voltage measurement. Since V_{IN} is very small—as low as 0.5 mV—the voltage measurement of V_{IN} is the most significant source of measurement error. The following paragraph explains this in more detail.

I_{IN} is determined through the equation

$$I_{\mathrm{IN}} = \frac{V_{\mathrm{Sense}}}{R_{\mathrm{Sense}}} - \frac{V_{\mathrm{IN}}}{R_{||}}. \tag{7.6}$$

Therefore, the input power becomes

$$P_{\mathrm{IN}} = V_{\mathrm{IN}} \left(\frac{V_{\mathrm{Sense}}}{R_{\mathrm{Sense}}} - \frac{V_{\mathrm{IN}}}{R_{||}} \right). \tag{7.7}$$

The *measured* input power becomes

$$P_{\mathrm{IN,measured}} = V_{\mathrm{IN,measured}} \left(\frac{V_{\mathrm{Sense,measured}}}{R_{\mathrm{Sense,measured}}} - \frac{V_{\mathrm{IN,measured}}}{R_{||,\mathrm{measured}}} \right). \tag{7.8}$$

Measurement accuracy is

$$\text{Measurement Accuracy} = 1 - \frac{P_{\text{IN,measured}}}{P_{\text{IN,actual}}}. \tag{7.9}$$

In this exercise we assume that the only measurement error is for $V_{\text{IN,measured}}$, such that $V_{\text{IN,measured}} = V_{\text{IN}} + V_{\text{IN,error}}$. Then

$$P_{\text{IN,measured}} = \left(V_{\text{IN}} + V_{\text{IN,error}}\right)\left(\frac{V_{\text{Sense}}}{R_{\text{Sense}}} - \frac{V_{\text{IN}} + V_{\text{IN,error}}}{R_{||}}\right). \tag{7.10}$$

Since $V_{\text{Sense}} / R_{\text{Sense}} = I_{\text{Sense}} = I_{\text{IN}} + I_{||}$, $I_{\text{IN}} = V_{\text{IN}} / R_{\text{IN}}$, and $I_{||} = V_{\text{IN}} / R_{||}$, so

$$P_{\text{IN,measured}} = \left(V_{\text{IN}} + V_{\text{IN,error}}\right)\left(\frac{V_{\text{IN}}}{R_{\text{IN}}} + \frac{V_{\text{IN}}}{R_{||}} - \frac{V_{\text{IN}} + V_{\text{IN,error}}}{R_{||}}\right). \tag{7.11}$$

$$P_{\text{IN,measured}} = \left(V_{\text{IN}} + V_{\text{IN,error}}\right)\left(\frac{V_{\text{IN}}}{R_{\text{IN}}} - \frac{V_{\text{IN,error}}}{R_{||}}\right). \tag{7.12}$$

If $R_{||}$ is set such that $R_{||} = R_{\text{IN}}$, then

$$P_{\text{IN,measured}} = \frac{V_{\text{IN}}^2 - V_{\text{IN,error}}^2}{R_{\text{IN}}}. \tag{7.13}$$

Since the $V_{\text{IN,error}}$ term is squared, it has a much reduced effect on the measured power compared to when there is no $R_{||}$. For example, if V_{IN} = 1 mV and $V_{\text{IN,error}}$ = 3.5 μV, then the measured output power has 0.0012% error instead of 0.35% error. Even if $R_{||}$ is 10% different from R_{IN}, the error is still only 0.031%, which is still over 10× better than when $R_{||}$ is not used.

However, even though the measured power becomes less sensitive to V_{IN} measurement error, the actual V_{IN} that the measurement is taken at still has a 3.5 μV uncertainty. This means that even though the actual efficiency might be accurately measured, the actual V_{IN} at which the efficiency is measured still could be 3.5 μV different from expected. To translate this to efficiency measurement error, the slope of the measured efficiency vs. V_{IN} curve can be applied to translate the V_{IN} uncertainty to efficiency uncertainty. For example, the slope of the efficiency vs. V_{IN} curve at 1 mV is 0.039 %/μV which means that a 3.5 μV V_{IN} uncertainty translates to a 0.14% efficiency

uncertainty at 1 mV. Without using $R_{||}$ the efficiency uncertainty due to the 3.5 μV V_{IN} uncertainty would be 0.36%. This isn't a tremendous improvement at 1 mV, but for future work if one wanted to measure the efficiency of a DC-DC converter with, say, 50 μV V_{IN}, the accuracy improvement by using $R_{||}$ would be more significant. The benefit depends on how steep the efficiency vs. V_{IN} curve is. For example, this method has no benefit for measuring at what V_{IN} the efficiency is 0%.

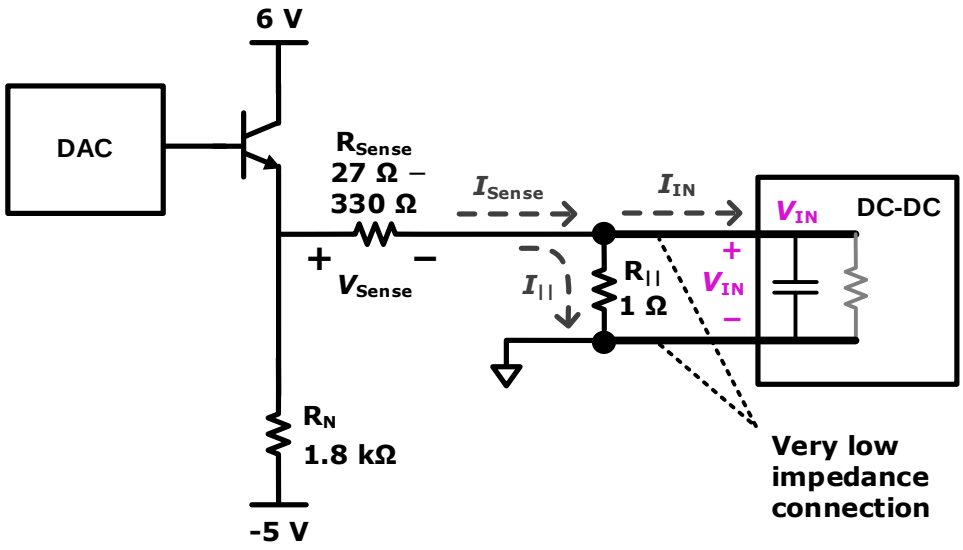

Figure 7.10. Bipolar circuit for forcing V_{IN} and measuring I_{IN} for efficiency and input impedance measurements. Used when the DC-DC converter input impedance is near 1 Ω.

The NPN transistor (2N3904) acts as a buffer for the DAC to provide more current than the DAC can provide. R_N keeps the NPN biased even when the emitter voltage is negative. $R_{||}$ [82] is a 30 W resistor with a low temperature coefficient so there is little temperature rise from self-heating and the resistance stays constant through the V_{IN} range. $R_{||}$ is connected directly to the DC-DC converter V_{IN} screw-mount power jack, giving a very low-impedance connection. $R_{||}$ is measured in-place by disabling the DC-DC converter and measuring I_{Sense} and V_{IN}, which eliminates connector impedance as a source of error. R_{Sense} = 330 Ω when setting V_{IN} from 0 V to 5 mV and 27 Ω when setting V_{IN} from 5 mV to 50 mV. Negative V_{IN} is achieved by either

outputting less than a V_{BE} (base-emitter voltage, ~0.6 V) from the DAC, or by reversing the input terminals on the DC-DC converter. If reversing the input terminals on the DC-DC converter, then care must be taken to avoid ground conflicting with the circuit driving V_{OUT}.

Table 7.3 lists the error contributors to the input power measurement. Because of the use of $R_{||}$, the ±0.355% error in the V_{IN} measurement using the 34401A DMM only has a ±0.019% effect on the input power measurement. However, the R_{Sense} and V_{Sense} measurement errors have an effect on the P_{IN} measurement that is greater than the absolute measurement errors. Overall, the total P_{IN} measurement error is ±0.23%, which is substantially less than the sum of each individual error contributor.

Table 7.3. Input power measurement error sources for V_{IN} = 1 mV, V_{OUT} = 2.5 V, F_{SW} = 350 Hz

Source of Error	**Error Amount**	**Effect on P_{IN} Measurement**
V_{IN} measurement (34401A accuracy for 1 mV)	±0.355%	±0.019%
330 Ω R_{Sense} initial measurement (34401A resistance measurement accuracy)	±0.013%	±0.021%
R_{Sense} drift after initial measurement (due to temperature change)	±0.010%	±0.013%
1 Ω $R_{||}$ initial measurement (using method described previously)	±0.107%	±0.112%
$R_{||}$ drift after initial measurement (due to temperature change)	±0.015%	±0.016%
V_{Sense} measurement accuracy	±0.023%	±0.046%
Total	±0.52%	±0.23%

Unlike the circuit that drives V_{OUT}, the circuit in Figure 7.10 does not regulate V_{IN}, which is a function of the DC-DC converter input impedance (R_{IN}), the DAC voltage, the NPN V_{BE}, R_{Sense}, and $R_{||}$. When driving V_{IN} to a specific voltage like 1 mV, a software feedback loop was used,

adjusting the DAC voltage to keep V_{IN} on target. When creating efficiency plots across many V_{IN} values, the DAC voltage was simply progressively incremented.

7.3.2.2 The op-amp feedback method

The second method used for forcing V_{IN} and sensing I_{IN} uses an op-amp feedback method similar to that used for forcing V_{OUT}. Figure 7.11 shows the circuit. The op-amp in this circuit needs to have very low offset in order to accurately control V_{IN}. The chosen op-amp is a MAX44241 [83], which has a maximum specified offset voltage of ±5 μV. However, the actual V_{IN} regulation error was found to be closer to ±10 μV, which was attributed to voltage drops in the wires that feedback from the DC-DC converter to the test circuit. It is believed that voltages were generated due to the Seebeck effect (the same affect that TEGs operate on) from the dissimilar metals in the wires/connectors and the wire temperature being slightly different from the temperatures of the test circuit and the DC-DC converter. Touching the wire with a warm hand shifted the voltage offset by an additional 10 μV, strengthening this hypothesis. This phenomenon is a known issue for low-voltage measurements and explained in [69].

R_1 and R_{FB} are both near 1 kΩ. The reason these values is that the specified maximum input bias current of the op-amp is 600 pA, which corresponds to an acceptable added input voltage offset of 0.6 μV. The N-channel MOSFET is an 2N7000 [84], which has a specified maximum input capacitance of 50 pF, which is lower than the 300 pF maximum rated load capacitance of the op-amp. C_{FB}, R_{FB}, R_Z and C_Z are needed to ensure stability in the feedback loop, similar to the circuit that drives V_{OUT} in Figure 7.9. V_{IN} and ground references are taken from dedicated points on the DC-DC converter circuit board as Kelvin connections [68] to minimize error due to voltage drop.

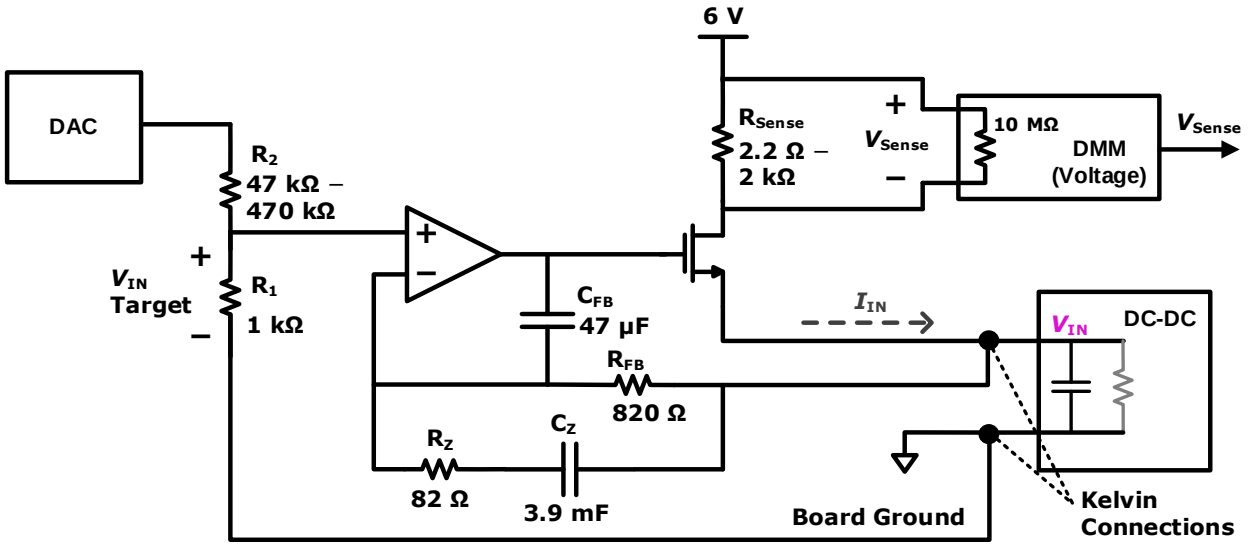

Figure 7.11. Feedback circuit for forcing V_{IN} and measuring I_{IN} for efficiency and input impedance measurements.

The main advantage of using an op-amp to drive V_{IN} over the method described in Section 7.3.2.1 is that the DAC voltage does not need to adjust to changes in I_{IN}, since the op-amp automatically compensates. This is useful for measurement sweeps where V_{IN} is kept constant but I_{IN} is varying, such as when measuring DC-DC converter efficiency versus switching frequency F_{SW}. Also, if the number of available DMMs is limited, then V_{IN} can be measured once and assumed to be constant for the duration of the measurement. The main drawbacks to using this circuit are accuracy due to the offset of the op-amp and feedback wires (intrinsic and thermoelectric offsets) and drive impedance. The drive impedance of the MOFSET is not well-controlled, while the drive impedance of the circuit in Figure 7.10 is well-controlled at 1 Ω to mimic the source impedance of a TEG.

7.4 WAVEFORM MEASUREMENT CIRCUITS

Measuring the transient waveforms of the DC-DC converter is tricky because of the low voltages and low currents of the circuit. The cycle-by-cycle transient waveforms were captured

using a Rigol DS1054Z [85]. The DS1054Z has limitations that necessitate additional support circuitry to be able to capture signal waveforms. The captured voltage vs. time points were saved to comma separated value (CSV) files and post-processed and plotted using Python code. The following signals were captured in bench measurements: V_{IN}, V_{OUT}, V_{G1}, V_{D1}, V_{D2P}, V_{D2N}, I_1. Transformer secondary winding currents I_{2P} and I_{2N} were not captured. The following sections describe in detail how each waveform was captured.

7.4.1 *Input voltage waveform*

Capturing the DC-DC converter input voltage waveform v_{IN} is not as simple as connecting the oscilloscope probe from the V_{IN} node to the GND node on the DC-DC converter. With V_{IN} = 1 mV, the noise and resolution of the oscilloscope dwarfs the ~50 μVpp (μV peak-to-peak) ripple that is to be captured. To capture the V_{IN} waveform with reasonable accuracy, an op-amp gain circuit was used, as shown in Figure 7.12. The circuit uses the same op-amp used for the input power measurements, the MAX44241 [83] with 5 μV maximum specified offset. The op-amp gain circuit amplifies the V_{IN} signal by a factor of 28. The actual gain is easily measured by forcing a known DC voltage on the amplifier input and measuring the DC output. The amplifier offset voltage can be measured and accounted for by forcing 0 V at the input and measuring the amplifier output voltage. The gain of 28 amplifies the 50 μVpp V_{IN} ripple into 1.4 mVpp. The gain and offset can then be accounted for in post-processing. Since the average of V_{IN} can be accurately measured with a DMM, the average of the V_{IN} signal captured by the oscilloscope can be compared against the DMM measurement to further check for accuracy. The MAX44241 has a bandwidth of 5 MHz. The closed-loop bandwidth reduces to 180 kHz with the 28× closed-loop gain. Which is plenty to measure the 350 Hz V_{IN} ripple. A 33 pF capacitor is placed in parallel with R_{FB} to improve stability. The RC frequency is 180 kHz, so it does not significantly impact bandwidth.

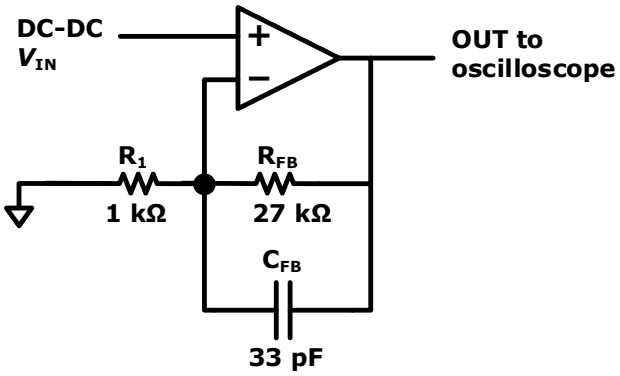

Figure 7.12. Circuit for amplifying V_{IN} before the oscilloscope probe.

There is still too much noise in the raw voltage waveform captured by the oscilloscope to be able to observe the V_{IN} ripple waveform. Therefore, a 2nd order lowpass Butterworth filter of corner frequency 1.25 kHz is applied to the waveform (36× the converter switching frequency). Figure 7.13 shows the captured input voltage before and after applying a 1.25 kHz filter to the waveform data.

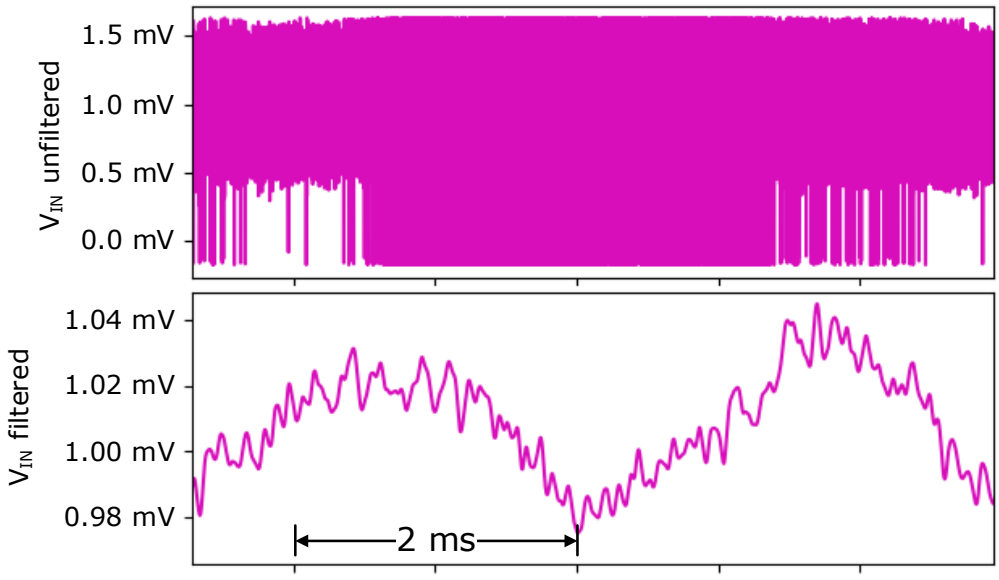

Figure 7.13. Captured DC-DC converter V_{IN} voltage with and without post filtering (V_{IN} = 1 mV, V_{OUT} = 2.5 V, F_{SW} = 350 Hz).

7.4.2 *Output voltage waveform*

The DC-DC converter output voltage rises very slowly when V_{IN} = 1 mV due to the large 330 μF output capacitance and low power levels. The expected output slew rate can be calculated with

$$I_{C,OUT} = C_{OUT}\frac{dv_{OUT}}{dt} = \frac{P_{C,OUT}}{V_{OUT}} = \frac{\eta P_{IN}}{V_{OUT}} = \frac{\eta \frac{{V_{IN}}^2}{R_{IN}}}{V_{OUT}}, \quad (7.14)$$

where $I_{C,OUT}$ and $P_{C,OUT}$ are the current and power that flows into C_{OUT}, from the rest of the DC-DC converter, and η is the efficiency of the DC-DC converter. Solving for dv_{OUT}/dt and using η = 63%, V_{IN} = 1 mV, R_{IN} = 1 mΩ, C_{OUT} = 330 μF and V_{OUT} = 2.5 V gives an output voltage slew rate of 760 μV/s. This is slow enough that the output voltage waveform can be easily captured by a periodically sampled DMM. DMM input impedance would affect the V_{OUT} measurement, so V_{OUT} is buffered with the same JFET-input op-amp that was used for quiescent current measurements.

7.4.3 *Gate voltage waveform*

The gate voltage v_{G1} of the DC-DC converter was brought out of the chip to a jumper connection so that the waveform of stepwise gate voltage can be captured on the bench. Measuring the voltage on this net is challenging because the stepwise gate driver was not designed to drive a static load current. The input impedance of the oscilloscope probe is too low for the stepwise gate driver. A low-input-current buffer is needed between the v_{G1} node and the oscilloscope probe. The buffer must have high enough bandwidth to be able to track the sub-100-ns steps on the falling edge of v_{G1}. Op-amps of 100 MHz bandwidth and less than 10 pA input bias currents are challenging, so a simpler open-loop buffer design was used instead. Figure 7.14 shows the circuit schematic. The NPN transistor is a CZT2222A [86] and the JFET is an MMBFJ310LT1G [87]. The simulated bandwidth of the circuit is 50 MHz. Since a JFET is a depletion mode device [88]

the source is a higher voltage than the gate. R_{Trim} is for offset correction. The input is forced to 0 V and R_{Trim} is adjusted until the output is also 0 V. The total gain is slightly less than one and it is dominated by the resistor divide ratio between R_{Trim} and R_0. The buffer gain is accounted for when post-processing the data captured by the oscilloscope. The circuit was designed to drive a 50 Ω transmission line to the oscilloscope, but the oscilloscope does not have a 50 Ω termination option, so instead the transmission line was simply kept short (12 inches) to avoid reflections.

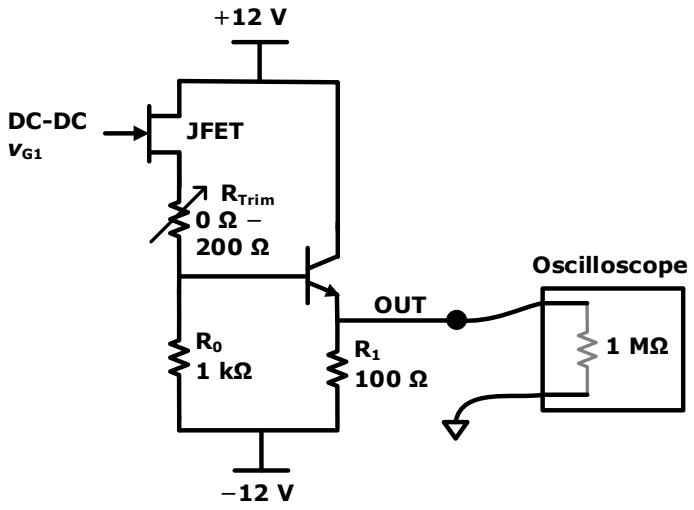

Figure 7.14. Low-input-current high-bandwidth buffer for capturing v_{G1} on the oscilloscope.

7.4.4 *Primary MOSFET drain voltage waveform*

Capturing the primary MOSFET drain voltage, v_{D2}, uses a pre-amplifier like the one used for V_{IN}, except the gain is reduced to 6.7. The reduced gain increases the bandwidth. Since v_{D1} swings several hundred milli-volts the reduced gain keeps the signal from clipping when the oscilloscope is set to its maximum zoom setting.

7.4.5 *Transformer primary current waveform*

Capturing the transformer primary current waveform, i_1, was the most challenging signal to capture. The current waveform cannot be captured directly. Instead, it is reconstructed using the v_{D1} voltage and the resistance of M_1. It is assumed that M_1 conducts only when v_{G1} is high. When v_{G1} is low i_1 is assumed to be zero. The current is calculated by

$$i_1 = \frac{v_{D1}}{R_{on1}}, \tag{7.15}$$

Where R_{on1} is the on-state resistance of primary power FET M_1. R_{on1} was calculated by disabling the DC-DC converter stepwise driver, forcing V_{G1} to 2.5 V, forcing a known current into V_{IN}, and measuring the voltage at v_{D1}. The accuracy of the i_1 waveform was checked by comparing the average value of the i_1 waveform with the DC I_{IN} measurement measured in Section 7.3.2. The v_{D1} voltage is very small when M_1 is on—on the order of 100 μV when V_{IN} = 1 mV. Consequently, the measurement noise overwhelms the v_{D1} voltage while M_1 is on. This is the same issue as was discussed in Section 7.4.1 about the V_{IN} measurement and so the lowpass filter that was described in the V_{IN} measurement is also applied to the v_{D1} measurement to extract the signal from the noise when generating the i_1 waveform.

Chapter 8.
MEASUREMENT RESULTS

The methods described in Chapter 7 were used to characterize the fabricated DC-DC converter. Converter efficiency, input impedance, quiescent power consumption, and dynamic behavior were characterized. Simulation models were updated with measured parameters from the fabricated circuit and the simulation data was analyzed to estimate the sources of all power losses within the circuit. Simulation data was also combined with measured data from the fabricated circuit to estimate the efficiency benefits of using the stepwise gate driver.

The 1:20:20 flyback transformer was characterized on the bench. The inductance of the primary coil was measured to be 300 μH and the resistance of the primary coil was measured to be 5 mΩ. The resistance of each secondary coil was measured to be 11 Ω. The coupling coefficient between the primary coil and each secondary coil was measured to be $k = 0.9987$. The on-resistance of the primary power FET M_1 was measured to be $R_{on1} = 34$ mΩ at $V_{OUT} = 2.5$ V. The on-resistance of the secondary power FETs M_{2P}/M_{2N} were measured to be $R_{on2} = 6$ Ω.

8.1 Efficiency and Input Impedance

The efficiency and input impedance of the DC-DC converter were measured using the methods described in Section 7.3.1 and Section 7.3.2.1. Figure 8.1 shows the measured efficiency and input impedance (defined as $R_{IN} = V_{IN} / I_{IN}$) of the DC-DC converter for input voltages from ±0.5 mV to ±50 mV. Efficiency and impedance are insensitive to input voltage polarity. The impedance is insensitive to V_{IN} for most of the range, decreasing as $|V_{IN}|$ approaches 50 mV due to transformer saturation—effectively clamping $|V_{IN}|$ at 50 mV. The 0% efficiency points were measured to be at $V_{IN} = 0.487$ mV and −0.493 mV, with a measurement accuracy of ±4 μV. The

efficiency at V_{IN} = 1 mV is 63.0% ± 0.4%, and the peak efficiency is 83.9% ± 0.3% at V_{IN} = 6.25 mV. Measurements were taken at a room temperature between 17°C and 21°C. V_{IN} was driven with a source resistance of 1 Ω to mimic that of a matched TEG. Hibernation is disabled but the input voltage detection circuitry remains enabled for representative power consumption.

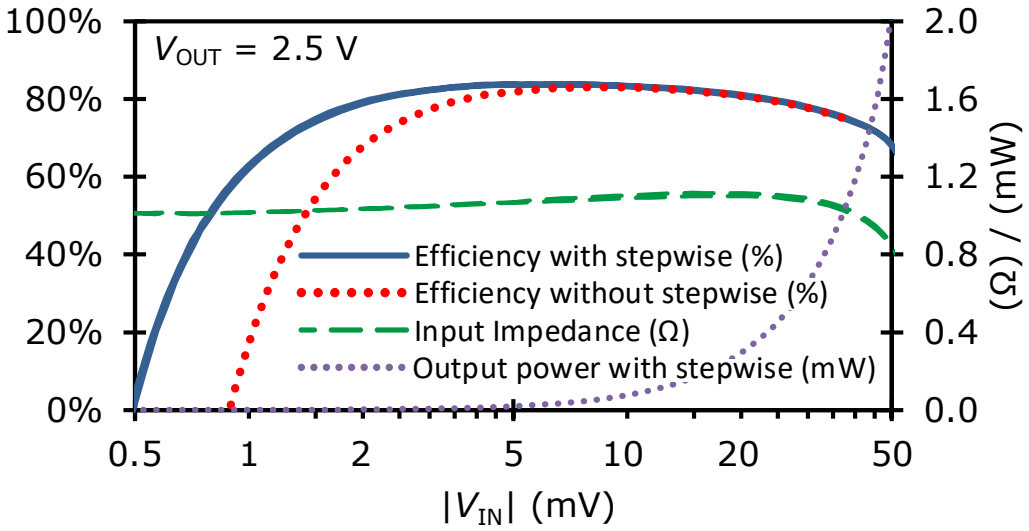

Figure 8.1. DC-DC converter efficiency with and without stepwise gate drive and input impedance from −50 mV to +50 mV input voltage. V_{OUT} = 2.5 V, *Frequency set* = 0 (350 Hz), and hibernation is disabled.

Figure 8.1 also includes what the efficiency would be without stepwise gate-drive. This is calculated by subtracting the simulated power savings due to stepwise gate-drive from the total output power and adding the power consumed by the stepwise driver control circuitry and the transition losses due to the slower gate edge rates of stepwise charging (details are provided in Section 8.2). The calculated 0% efficiency point without stepwise gate-drive is at V_{IN} = 0.883 mV while the measured efficiency at this voltage with stepwise gate-drive is 56.9%. All other plots are with stepwise gate-drive enabled. The benefits of stepwise gate-drive diminish for higher $|V_{IN}|$ as the output power eclipses the gate-drive losses.

Figure 8.2 provides the DC-DC converter efficiency and output power versus V_{IN} for various output voltages, showing that the DC-DC converter maintains reasonable efficiency from V_{OUT} = 1.5 V up to 2.7 V.

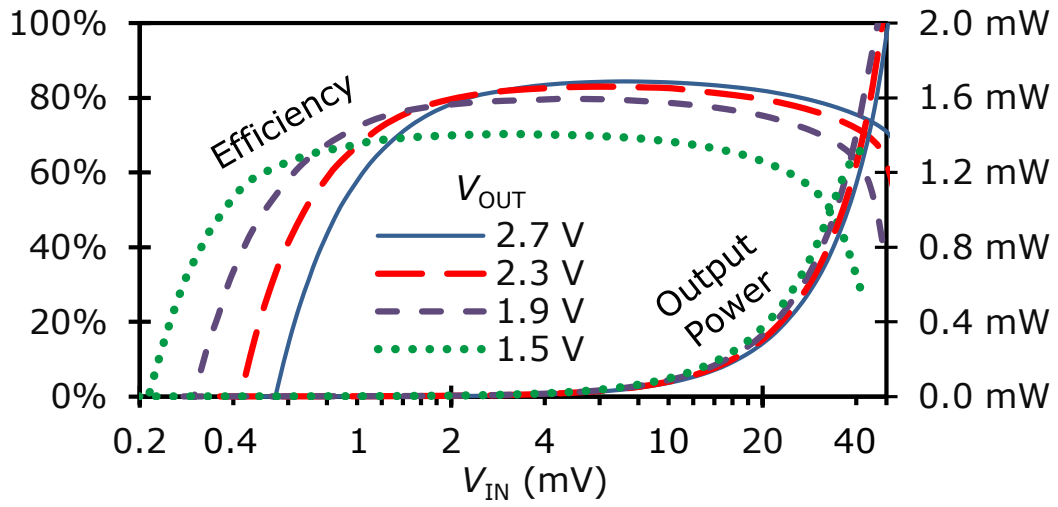

Figure 8.2. Efficiency for V_{IN} ranging from +0.2 mV to +50 mV at various output voltages. *Frequency set* = 0 and hibernation is disabled. © 2023 IEEE

Figure 8.3 shows how the input impedance changes with V_{OUT} and how the minimum input voltage (V_{IN} where the efficiency = 0%) aligns with the threshold at which the DC-DC converter enters hibernation, $V_{IN,Th}$. At V_{OUT} = 1.5 V, the minimum V_{IN} is 0.223 mV. Ideally the hibernation threshold voltage would equal the minimum V_{IN} for all V_{OUT}, but delay line sensitivity to V_{OUT} causes them to diverge. Improvements in the bias generator in Figure 3.9 could reduce the hibernation threshold divergence and the input impedance sensitivity to V_{OUT}; however, since V_{OUT} is normally between 2.5 V and 2.7 V, these sensitivities are not very problematic. The reason why the minimum V_{IN} is lower for lower V_{OUT} is because the capacitive CV^2 losses within the circuit all reduce with the square of V_{OUT}, so efficiency that the lowest V_{IN} improves. T_{rise} also increases for lower V_{OUT} due to the properties of the bias gen. in the slow delay line. This gives the inductance of the primary coil in the flyback transformer more time to build up energy per cycle.

The longer T_{rise} also means that I^2R losses due to i_1 increase for lower V_{OUT}, but those losses are only significant for higher V_{IN}.

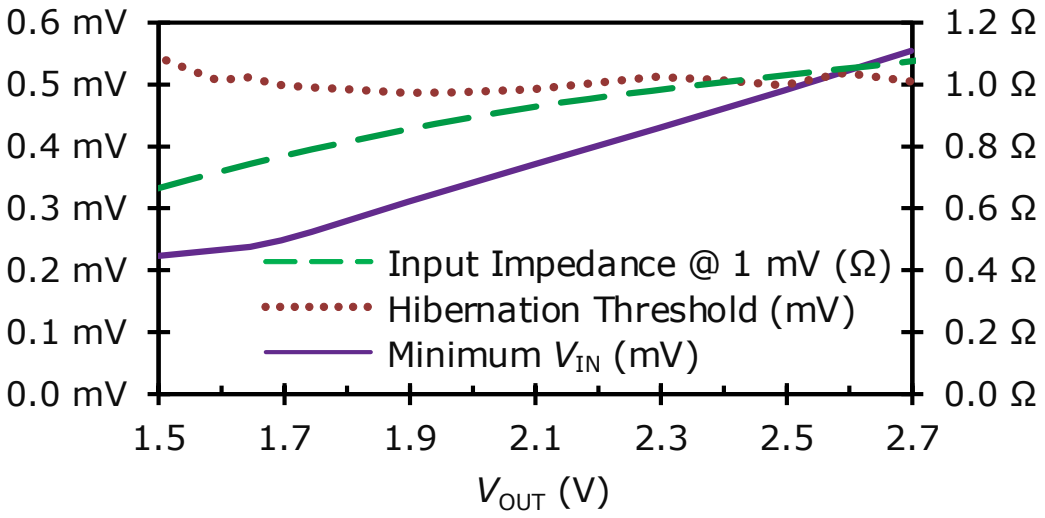

Figure 8.3. Minimum V_{IN} (V_{IN} at efficiency = 0%; hibernation disabled), hibernation threshold ($V_{IN,Th}$), and input impedance vs. output voltage. © 2023 IEEE

Figure 8.4 shows how the switching period of the DC-DC converter is programmable from 2.8 ms to 1.2 s through the 6-bit input *frequency set*. This allows the input impedance to be programmable from 1 Ω to 600 Ω, also shown in Figure 8.4. The DC-DC converter efficiency reduces with longer switching period as C_{OUT} leakage and the slow delay line consume more energy per cycle. The efficiency is still greater than 40% at the maximum setting of 600 Ω. This means that the DC-DC converter is still functional with input power levels below 2 nW.

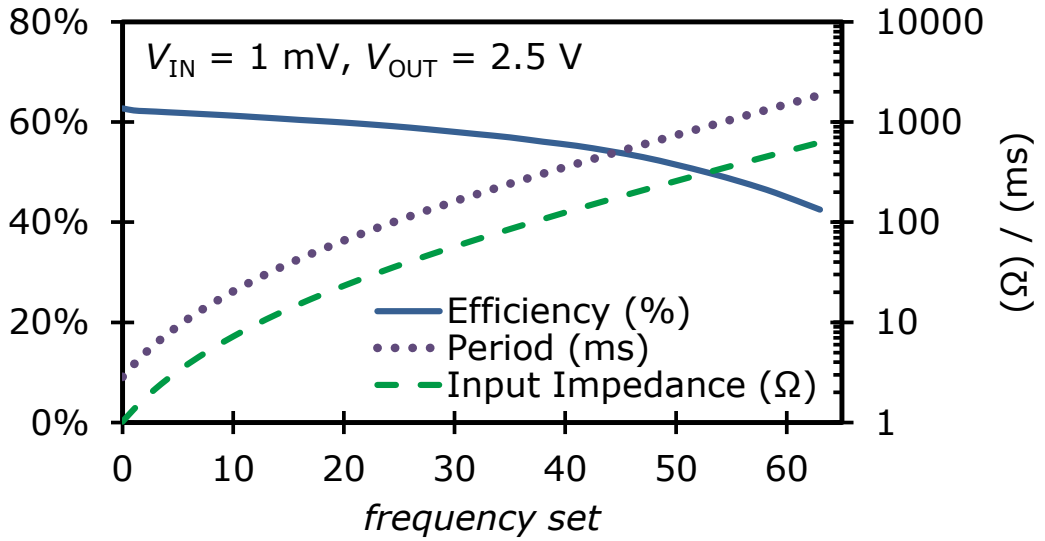

Figure 8.4. The 6-bit input *frequency set* controls the switching period of the DC-DC converter. This sets Input impedance from 1 Ω to 600 Ω. © 2023 IEEE

8.2 Sources of Energy Losses

Simulations were run to estimate the energy losses in the various portions of the of the DC-DC converter circuit. Certain circuit parameters were updated in the simulation with measurement from the hardware, such as: M_1 on-time, M_1 on-resistance, transformer inductance, and transformer winding resistance. This is to make simulation match the hardware as close as possible. Parasitic capacitance on the v_{D2P}/v_{D2N} nodes was estimated to be 2 pF each—which is meant to include the circuit board parasitic trace capacitance and the parasitic capacitance between the turns of the transformer secondary windings. C_{IN} capacitance and ESR (equivalent series resistance) were modeled based on nominal datasheet values. The resistance of M_1, R_{on1}, was measured to be 34 mΩ per the method described in Section 7.4.1.

Table 8.1 provides the sources of (simulated) energy losses within the DC-DC converter per cycle at V_{IN} = 1 mV. The table also includes what the losses would be without stepwise gate-drive. The power consumption of the slow delay line and the fast delay line are included in the "without

stepwise gate-drive" column because these circuits are still needed to generate the switching frequency and on-time for M_1 and the reference delays for the input voltage detection and output voltage monitor. With *frequency set* = 0, the slow delay line utilizes 78 *dly* stages and consumes 45 pJ per cycle. The stepwise gate driver losses ($E_{\text{Gate-Drive}}$) of 222 pJ are calculated from the total charge that flows through switch S_{R9} per cycle (i_{SR9} in Figure 3.8). This energy would be 1550 pJ without stepwise gate-drive. The ideal gate-drive energy consumption from (3.1) is 172 pJ. Of this 50 pJ difference, 30 pJ were found to be due to the C_{Tank} / C_{Gate} ratio (simulating with C_{Tank} 6× larger reduces the stepwise gate driver energy to 202 pJ). The remaining 20 pJ difference between simulated and ideal energy consumption is unaccounted for. Increasing settling time for each step, eliminating the Miller effect [39] by setting V_{IN} = 0 mV, and increasing deadtime for switches S_{R} and S_{F} (break-before-make) all had a negligible effect on the simulated energy consumption. The author did find that the 20 pJ of unaccounted-for losses only appear when parasitic on-chip routing capacitance is included in the simulation, suggesting that those losses could be reduced with more efficient routing.

Table 8.1. Simulated energy losses per switching cycle.

V_{IN} = 1 mV, V_{OUT} = 2.5 V, *frequency set* = 0	**With stepwise gate-drive**		**Without stepwise gate-drive**	
Source of losses	**Energy losses**	**% of total losses**	**Energy losses**	**% of total losses**
Stepwise gate driver for M_1	222 pJ	26.5%	1550 pJ	73.8%
Stepwise switch drivers	57 pJ	6.8%	0 pJ	0.0%
M_1 conduction losses	231 pJ	27.6%	231 pJ	11.0%
M_1 transition losses	10 pJ	1.2%	0 pJ	0.0%
M_1 drain capacitance losses	2 pJ	0.3%	2 pJ	0.1%
Gate driver for M_2	11 pJ	1.3%	11 pJ	0.5%
M_2 control & V_{IN} detect	30 pJ	3.6%	30 pJ	1.4%
M_2 conduction losses	40 pJ	4.8%	40 pJ	1.9%
M_2 drain capacitance losses	63 pJ	7.5%	63 pJ	3.0%
Primary coil cond. losses	34 pJ	4.1%	34 pJ	1.6%
Leakage inductance losses	6 pJ	0.7%	6 pJ	0.3%
Secondary coil cond. losses	1 pJ	0.2%	1 pJ	0.1%
Slow delay line	45 pJ	5.4%	45 pJ	2.1%
Fast delay line	45 pJ	5.3%	45 pJ	2.1%
Voltage monitor	29 pJ	3.5%	29 pJ	1.4%
Total input energy (E_{IN})	2575 pJ		2575 pJ	
Total output energy (E_{OUT})	1738 pJ		476 pJ	
Total losses ($E_{IN} - E_{OUT}$)	837 pJ		2099 pJ	
Simulated efficiency	67.5%		18.5%	

The transition losses due to the slower edge rates for v_{G1} ($E_{Tran\text{-}Loss}$) are calculated to be 10 pJ and the stepwise switch drivers ($E_{Switch\text{-}Drive}$) consume 57 pJ combined, showing that stepwise gate-drive saves a total of 1261 pJ: 49% of the total input energy E_{IN}. Total gate-drive energy is reduced by 82%. Even if the delay line circuits were included in the calculation, the net energy savings would be 1171 pJ: 45% of E_{IN}.

$E_{Gate\text{-}Drive}$, $E_{Switch\text{-}Drive}$, and $E_{C,D1}$ (M_1 drain capacitance losses) consume 281 pJ combined. The target was to balance these losses with the M_1 conduction losses of 231 pJ (at V_{IN} = 1 mV) per (5.5), but the voltage doubler in the stepwise switch driver ended up consuming more energy than planned.

M_2 conduction losses of 40 pJ are dominated by the voltage drop of the body diode during the short period of time that M_2 is conducting but v_{G2} is low, depicted in Figure 4.1. The M_2 on-resistance contributes less than 1 pJ toward conduction losses. M_2 drain capacitance losses include all parasitic capacitance on nodes v_{D2P} and v_{D2N} including circuit board capacitance.

8.3 Circuit Waveforms

The DC-DC converter circuit waveforms were captured using the methods described in Section 7.4.

8.3.1 *DC-DC switching waveforms*

Figure 8.5 and Figure 8.6 show the captured switching waveforms of the fabricated circuit, including the captured stepwise gate voltage v_{G1} for V_{IN} = 1 mV and V_{IN} = 50 mV, respectively. The rising-edge transition time for v_{G1} is T_R = 90 μs, while the falling-edge transition time is T_F = 1.3 μs. The non-linear slope of i_1 when V_{IN} = 50 mV is due to transformer saturation (see Section 2.2).

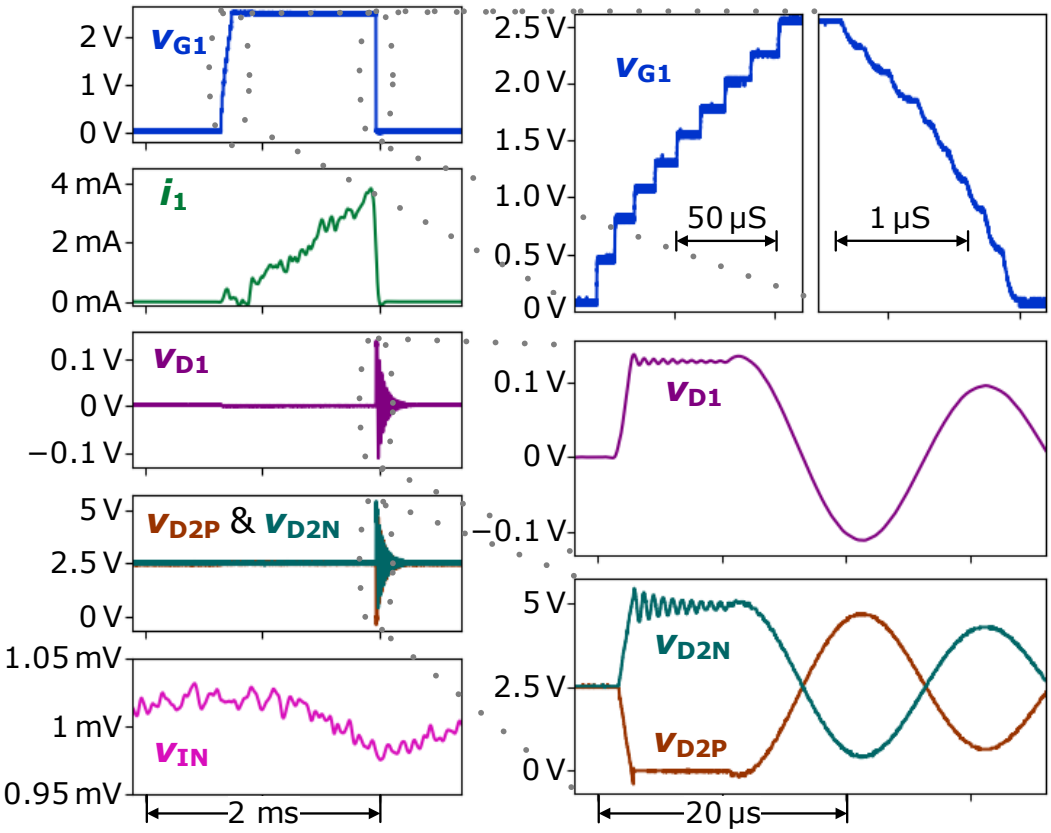

Figure 8.5. Captured DC-DC converter circuit waveforms for V_{IN} = 1 mV and V_{OUT} = 2.5 V. *Frequency set* = 0. © 2023 IEEE

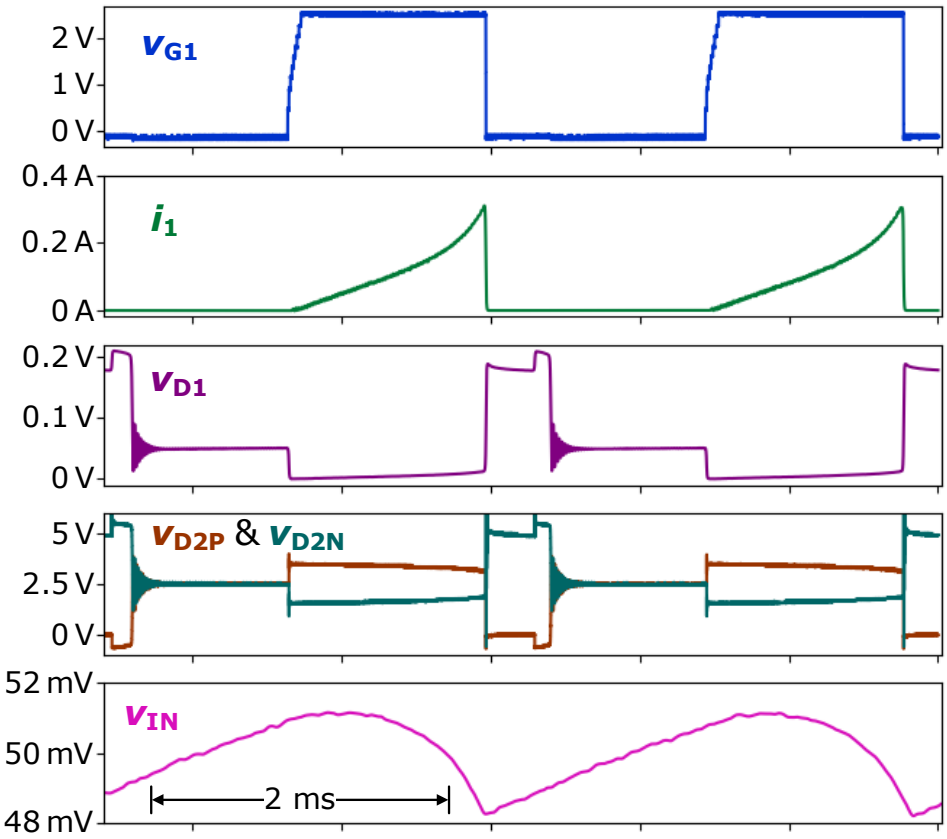

Figure 8.6. Captured DC-DC converter circuit waveforms for V_{IN} = 50 mV and V_{OUT} = 2.5 V. *Frequency set* = 0. © 2023 IEEE

8.3.2 *Long discharge and power good*

When V_{IN} = 0 mV and V_{OUT} = 2.5 V, the quiescent power that the converter draws from its output is 255 pW ± 5 pW (including the leakage of C_{OUT}). The low power consumption keeps V_{OUT} above the minimum required voltage of 1.5 V for 12 weeks, meaning that after initial startup the DC-DC converter would only need to be revived if there was no input power for a 12-week duration. To demonstrate this behavior, Figure 8.7 shows the slow discharge of the output voltage during hibernation. V_{OUT} was pre-charged to 2.5 V and V_{IN} was forced to 0 mV for a 12-week duration. After 12 weeks, when V_{OUT} has discharged below 1.5 V, V_{IN} was increased from 0 mV to 1 mV. With input power now available, V_{OUT} charges to 2.7 V. At that time, the voltage monitor

activates the *power good* signal and the increased load current causes V_{OUT} to discharge to 2.5 V, at which point the load current disables and V_{OUT} once again charges back to 2.7 V.

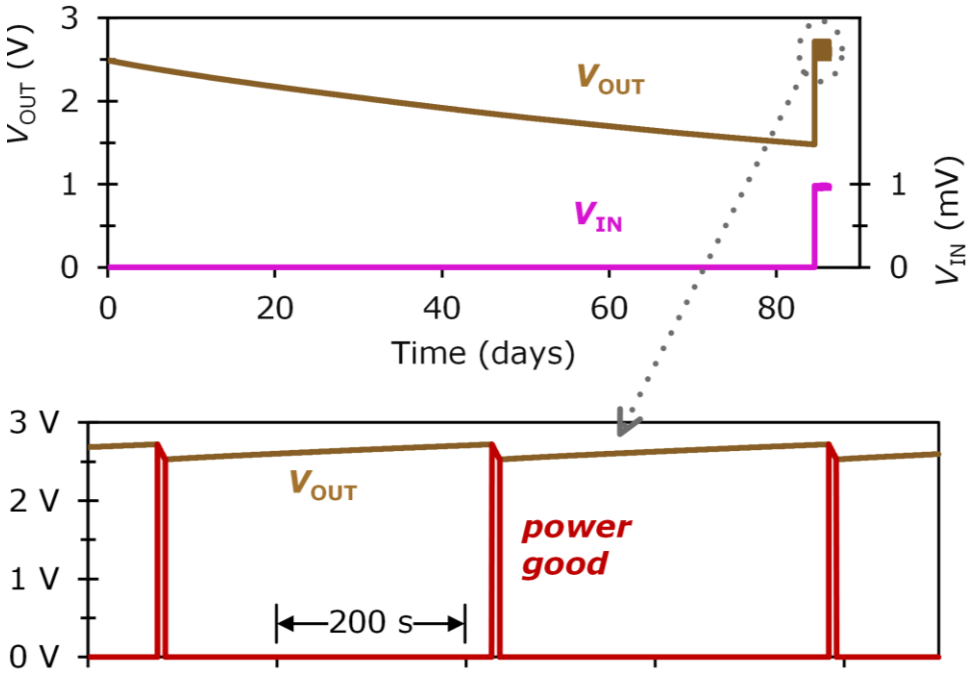

Figure 8.7. The DC-DC converter recovers after 84 days of zero input voltage (top). When 1 mV is applied to the input the output charges up to 2.7 V, enabling the *power good* signal (bottom) until V_{OUT} drops below 2.5 V, after which the output charges back to 2.7 V to complete the cycle. © 2023 IEEE

8.4 Comparison with Other Work

Table 8.2 compares performance with other work. The minimum V_{IN} of ±0.5 mV is 20× lower than the bipolar converter in [19] and 7× lower than the unipolar converter in [6]. The lower minimum V_{IN} of this work can be attributed to the use of stepwise gate-drive and a large transformer inductance. The quiescent power of 255 pW (achieved with the use of the novel delay line and a low-leakage 600-nm CMOS process) is surpassed only by [37], which has a minimum V_{IN} of 250 mV, much higher than the ±0.5 mV of this work. The lower quiescent power consumption can be attributed to the use of a low-leakage 600-nm CMOS process coupled with

using stepwise gate-drive to keep the gate-drive power consumption of the 600-nm power FET low. The low quiescent power consumption can also be attributed to the use of the novel slow delay line circuit, which efficiently increases the switching period to 5 seconds when V_{IN} = 0 V. This very long switching period minimizes the switching losses when no input power is available.

The die area is much larger than other works mostly due to the large C_{Tank} capacitance for the stepwise gate driver. This is a necessary tradeoff for stepwise gate-drive. Although circuit board area is mostly unreported in other works, they are likely much smaller than the 50 cm^2 in this work. The area is dominated by connectors, C_{IN}, and C_{OUT}. As explained in Section 2.3, C_{IN} could be reduced significantly before efficiency is significantly impacted. As explained in Section 2.4, C_{OUT} is sized based on load circuit requirements and maximum input voltage, so could be reduced depending on those requirements. The 20 mm × 8 mm transformer is necessary to achieve the presented performance, but it would need to be much larger without stepwise gate-drive to achieve the same efficiency performance because the transformer core would have to store more energy per cycle to offset the gate-drive losses. Input voltage ripple would also be about 4× larger so to keep the input voltage ripple the same without stepwise gate-drive there would need to be 4× more input capacitance.

Table 8.2. DC-DC converter performance comparison with other work

	[6]	[7]	[19]	[25]	[26]	[27]	[37]	[89]	**This Work**
Input voltage range	3.5 mV – 100 mV	±20 mV – ±50 mV	±10 mV – ±400 mV	±13 mV – ±500 mV	±25 mV – ±300 mV	5 mV – 200 mV	250 mV – 650 mV	20 mV – 72 mV	±0.5 mV – ±50 mV
Bipolar input?	No	Yes	Yes	Yes	Yes	No	No	No	Yes
Output voltage	1.2 V	1.2 V	0.9 – 1.5 V	3 – 5 V	1 V	2.0 – 4.2 V	4.0 V	1.1 V	2.5 V
Quiescent power	240 nW	N/R	110 nW	N/R	N/R	N/R	15 pW	544 pW	255 pW
Self-start voltage	50 mV	None	140 mV	13 mV	129 mV	5 mV	250 mV	None	None
Chip die area	1.0 mm^2*	0.09 mm^2*	3.2 mm^2	< 2.5 mm^2	1.6 mm^2	< 4 mm^2	2.7 mm^2	1.5 mm^2	10.4 mm^2
Circuit board area	N/R	N/R	N/R	N/R	N/R	N/R	Die only	0.5 cm^2	50 cm^2
R_{IN} or R_{TEG}	5 Ω	7 Ω	200 Ω	4 Ω	210 Ω	Uncontrolled	N/A	0.4 MΩ – 1.3 MΩ	1 Ω – 600 Ω
Max output power	1.5 mW	250 μW	720 μW	47 mW	90 μW	20 mW	4 μW	4 nW	2.0 mW
Peak efficiency @ Input voltage, Output power	82% @ 50 mV, 400 μW	70% @ 50 mV, 36 μW	90% @, 300 mV, 400 μW	85% @ 300 mV, 20 mW	84% @ 270 mV, 83 μW	61% @, 16 mV, 110 μW	60% @ 0.5 mV, 8 nW	55% @ 70 mV, 1.2 nW	84% @ 6 mV, 320 μW[§]
Magnetic component	Inductor, 100 μH	Inductor, 47 μH	Inductor, 220 μH	Tr, 1:100, 7.5 μH[†]	Tr, 1:1, 82 μH[†]	Tr, 1:100, 7.5 μH[†]	None[#]	Inductor, 47 μH	Tr, 1:20:20, 300 μH[†]
CMOS process	180 nm	65 nm	130 nm	N/R	180 nm	N/R	180 nm	180 nm	600 nm

N/R: Not reported, Tr: Transformer, *Not including pads or test circuitry, [§]At R_{IN} = 1 Ω, [†]Inductance at primary coil, [#]switched-capacitor topology

Chapter 9.

DEPLOYMENT: HARVESTING ENERGY FROM ROOM TEMPERATURE FLUCTUATIONS

To demonstrate the utility of the DC-DC converter, a thermoelectric harvesting system was constructed to harvest the energy generated by indoor temperature fluctuations. Even though the temperature of human-occupied buildings is generally regulated by the heating cooling and ventilation (HVAC) system, there is still some fluctuation in air temperature as the HVAC system cycles or as outdoor temperatures fluctuate. A photograph of the fabricated energy harvesting unit is shown in Figure 9.1. The unit consists of an insulated thermal storage element, a TEG, a heat sink to exchange heat with the ambient air, and the DC-DC converter.

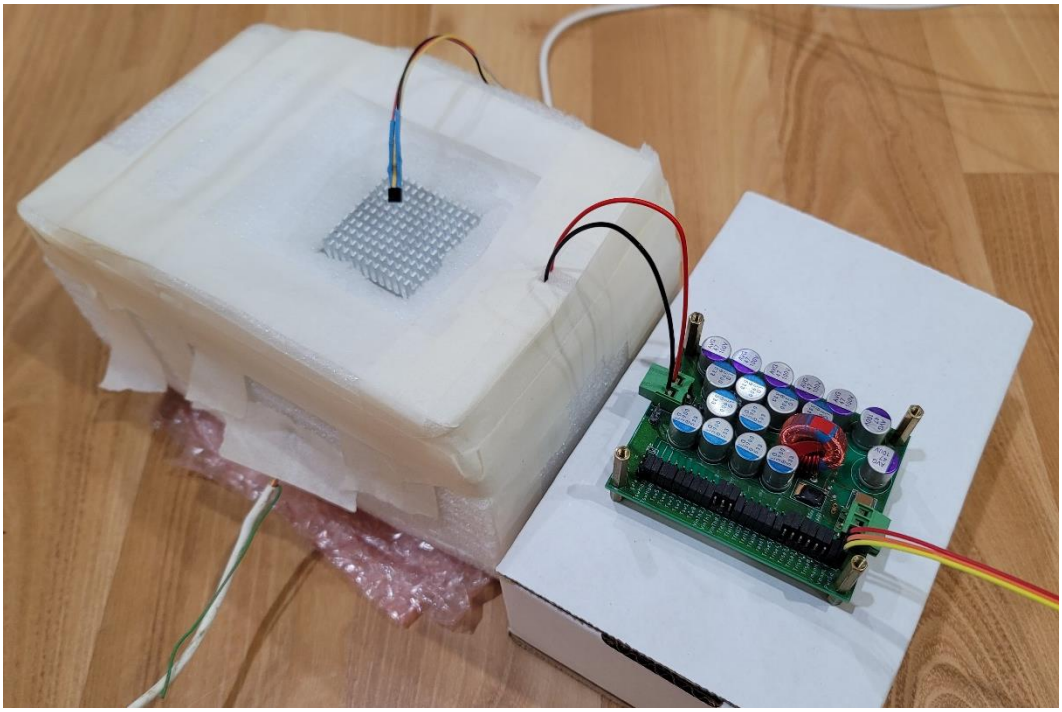

Figure 9.1. Photograph of unit for harvesting energy from indoor temperature fluctuations.

9.1 TEG SELECTION

The TEG is the core of the thermal energy harvesting system, as it is what converts the thermal energy into electrical energy. There are many options to choose from for a TEG, of varying sizes and electrical properties. Since this application is to harvest energy from small indoor temperature differences, a TEG with a large Seebeck coefficient (which determines the open-circuit output voltage for a given temperature difference between the faces of the TEG [17]) is desirable. Since energy must be conserved, a large Seebeck coefficient typically coincides with a large internal series resistance, which the DC-DC converter must match to. The chosen TEG for this demonstration was a TEG2-126LDT [90], which is 40 mm square and has a specified Seebeck coefficient of 53 mV/°C and an internal series resistance of 4 Ω at 30°C.

9.2 THERMAL STORAGE

In order to harvest energy from heat, there must be a temperature difference across the faces of the TEG. To achieve this, a thermal storage element is used. One face of the TEG is thermally coupled to the thermal storage element with thermal paste and the other face of the TEG is thermally coupled to an aluminum heat sink that exchanges heat with the ambient air.

Kiziroglou [17] uses a sealed aluminum container filled with water as the thermal storage element. This work uses a solid aluminum block instead for easier fabrication. The aluminum is insulated on all sides except the area that is coupled to the TEG. The insulation reduces heat loss to the ambient air. This way, as the ambient air temperature fluctuates, the thermal storage element maintains a more consistent temperature and the TEG experiences a temperature difference between its faces.

9.3 Measuring Thermal Harvester Output Impedance

In order to maximize the amount of power harvested from the thermal energy harvester, the input impedance of the DC-DC converter must be programmed to match that of the thermal energy harvester. To do this, the impedance of the TEG must be known. The TEG manufacturer specifies the TEG impedance to be 4 Ω at 30°C. However, this assumes good thermal coupling between the faces of the TEG and the environment. There is substantial thermal resistance between the heat sink and the air. As such, the effective output impedance of the thermal energy harvester is more than what the TEG manufacturer specifies. A description of the method that was used to approximate this impedance follows.

The thermal harvester is continuously producing voltage due to the temperature difference between the air and the aluminum block. The TEG output impedance can be calculated by measuring the TEG open-circuit voltage and then the voltage when the TEG is loaded with a resistor (an appropriate resistor value would be close to the expected output impedance). However, there are two complexities that complicate this measurement. One is that it takes time for the TEG output voltage to settle as the temperatures need time to reach steady-state after the loading on the TEG changes. The other is that the air temperature is dynamic and actively changing during the experiment. To address the settling time issue, the TEG voltage was given 5 minutes to settle each time after the loading was changed. The required settling time was approximated by periodically changing the loading on the TEG and watching the TEG output voltage settle. To filter out the effects of continuous air temperature fluctuations, the TEG was switched between loaded and unloaded periodically for 5-minute intervals many times to obtain many measurements throughout time, then averaging the results. The output impedance was ultimately measured to be approximately 9 Ω.

9.4 MEASURING TEMPERATURE

When demonstrating the performance of a thermal energy harvesting system, it is important to include the temperatures that are being used to generate the power. As such, the temperatures of the ambient air and of the thermal storage element (aluminum block) were monitored. A temperature sensor (LM35A [91]) was placed directly above the heat sink to measure the temperature of the ambient air. A hole was drilled into the center of the aluminum block and second temperature sensor was placed in the hole to monitor the temperature of the thermal storage element. The hole was filled with lithium grease to improve thermal conductivity (while being electrically insulating).

The absolute temperature is not nearly as important as knowing the temperature difference between the air and the aluminum block for this experiment. The specified accuracy of the LM35A temperature sensor is only ±0.5°C, which is insufficient for an accurate temperature difference measurement. To address this, the two sensors were calibrated by putting them at equal temperatures and reading the measured temperatures simultaneously. The difference of the result was then the correction factor for the temperature measurements of the experiment. The sensors were forced to equal temperatures by placing them side-by-side and wrapping them in insulation.

9.5 RESULTS

Figure 9.2 shows measured results of the thermal energy harvesting system over a 48-hour duration. Because most of the time the input voltage V_{IN} to the DC-DC converter is below 1 mV, the DC-DC converter input impedance was programmed to 13 Ω, 44% higher than the output impedance of the thermal harvester. This is to keep V_{IN} above the minimum operating voltage longer and gives a better overall efficiency as explained in [6]. The room temperature is fluctuating

by approximately ±1°C and the temperature of the aluminum block lags that of the ambient air creating a small temperature difference. The ΔT across the TEG itself was not measured but is expected to be much less than the difference between the aluminum block and the ambient air. The average V_{IN} per air-to-block temperature difference is 2.6 mV/°C (excluding time in hibernation), which is much less than the 53 mV/°C (unloaded) Seebeck coefficient specified for the TEG itself. This difference is attributed the inefficiency of the thermal coupling between air and heat sink.

V_{OUT} is visibly charging for $|V_{IN}|$ as low as 0.6 mV, for both polarities. The *power good* pin was loaded with a 1 kΩ resistor in this demonstration. Each time V_{OUT} charges above 2.7 V the output is partially discharged into the 1 kΩ load resistor through the *power good* pin. The average output power can be approximated by multiplying the energy discharged from the output capacitors per *power good* pulse (see Figure 8.7) by the number of charging cycles and dividing by the total measurement duration:

$$P_{\mathrm{OUT}} = \frac{E_{\mathrm{Pulse}} N_{\mathrm{Pulses}}}{T_{\mathrm{Measurement}}}, \tag{9.1}$$

$$E_{\mathrm{Pulse}} = \frac{1}{2} C_{\mathrm{OUT}} \left(V_{\mathrm{OUT,high}}^2 - V_{\mathrm{OUT,low}}^2 \right) N_{\mathrm{Pulses}}. \tag{9.2}$$

With C_{OUT} = 330 μF, $V_{OUT,high}$ = 2.72 V, $V_{OUT,low}$ = 2.53 V, N_{Pulses} = 23, and $T_{Measurement}$ = 48 hours, the average output power was calculated to be 22 nW.

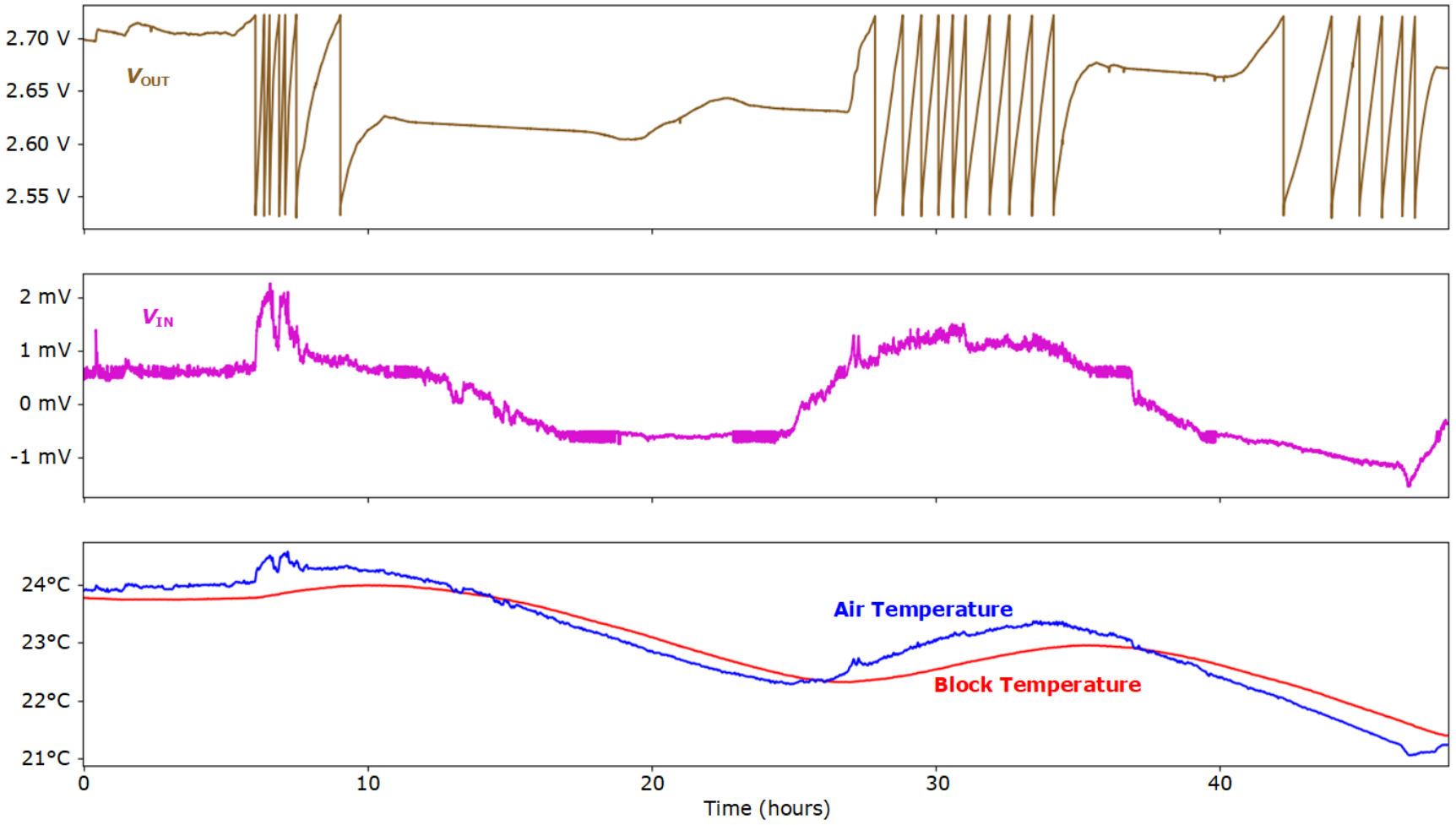

Figure 9.2. Voltage and temperature waveforms of the thermal energy harvesting system. © 2023 IEEE

Chapter 10.
CONCLUSION AND FUTURE WORK

A step-up DC-DC converter that leverages an adiabatic stepwise gate driver to achieve an unprecedented minimum input voltage of ±0.5 mV in a low-leakage 600-nm CMOS process was presented. A low-power delay line circuit efficiently provides the timing signals needed by the stepwise gate driver while also providing timing for on-time, switching frequency, and input voltage detection. The converter hibernates when V_{IN} is too low for efficient operation—reducing quiescent power to just 255 pW. An extra winding on the flyback transformer enables bipolar operation for harvesting energy from both positive and negative temperature differentials. A closed-form analytical model of stepwise gate-drive energy for efficiency optimization was presented. The DC-DC converter was deployed in an energy harvesting system that harvests thermoelectric energy from air temperature fluctuations less than 1°C.

This dissertation leaves several opportunities for future work. Although the DC-DC converter presented in this work was implemented in a 600-nm CMOS process, many CMOS processes support both high-performance short channel-length devices along with longer channel-length low-leakage devices on the same die. Power FET M_1 could be implemented as a shorter channel-length device (say, 180-nm) while the rest of the control circuitry is implemented as low-leakage devices. This would greatly decrease the on-resistance of M_1 for a given gate-drive energy, which would in-turn allow the DC-DC converter to operate at input voltages even lower than 0.5 mV. Short channel-length devices have higher drain leakage current and gate leakage current than the 600-nm devices used here, but M_1 is more tolerant of leakage currents than the rest of the DC-DC converter circuitry. This is because, while most of the circuitry is exposed to the full V_{OUT} voltage

even while in hibernation, the drain of M_1 is never exposed to voltages higher than 300 mV and is equal to V_{IN} most of the time. The gate voltage of M_1 is 0 V in hibernation. The lower voltages on the drain and gate limit the losses due to leakage. Therefore, M_1 could be implemented as a shorter channel-length device without impacting quiescent power consumption. However, there is still a real limit to how short the channel length of M_1 can be because for shorter channel-length CMOS processes the gate leakage will become significant enough that it dominates the gate-drive losses, exceeding the capacitive losses and reducing efficiency in normal operation. A useful study would be to find the CMOS process that gives the optimum tradeoff between capacitive losses and gate-leakage losses for M_1 while including the benefits of stepwise gate-drive.

This leads to the question of how low of an input voltage can you go? What would a circuit designed to work down to 50 μV or even 1 μV look like? There are additional options for improving low-V_{IN} efficiency besides adiabatic gate-drive. Bose [6] describes a method for improving low-V_{IN} efficiency by adjusting M_1 on-time and period as a function of V_{IN} to rebalance switching losses and conduction losses. If M_1 was implemented in a CMOS process that gives the optimal tradeoff between gate leakage and gate capacitance while being driven with stepwise gate-drive and the adaptive timing in [6], how much lower could the minimum input voltage go?

In this work stepwise gate-drive is applied to a unique application: harvesting energy from extremely low-voltage power sources. At this point in time stepwise gate-drive has not been applied to more traditional DC-DC converter applications. Would stepwise gate-drive be beneficial for higher voltage higher frequency applications? Or would the slower edge-rates and transition losses negate the power savings of stepwise gate-drive in those applications?

There is also the question of startup. Many of the works referenced in this dissertation have self-startup techniques, while this work uses a more unique approach of avoiding the need for

startup by hibernating the circuit when no power is available to keep the output voltage from discharging. However, the charge does not last forever and this does not protect against external factors that might cause an unexpected discharge of the output voltage. While many of the cold-start circuits in referenced works are inherent to the DC-DC converter topology and therefore would impact overall performance, the 11-mV cold-start circuit in [61] appears to work independently of the DC-DC converter. It would be interesting to know whether the DC-DC converter in this work could be paired with the cold-starter in [61] to provide a backup revival circuit in the unexpected case of V_{OUT} discharge.

BIBLIOGRAPHY

[1] L. L. Baranowski, G. J. Snyder and E. S. Toberer, “Effective thermal conductivity in thermoelectric materials,” *J. Appl. Phys.*, vol. 113, no. 20, pp. 105–114, May 2013.

[2] K. Zhu, B. Deng, P. Zhang, H. S. Kim, P. Jiang, and W. Liu. “System efficiency and power: the bridge between the device and system of a thermoelectric power generator.” *Energy & Environmental Science*, vol. 13, no. 10, pp. 3514–3526, 2020.

[3] E. J. Carlson, K. Strunz and B. P. Otis, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.

[4] E. J. Carlson, K. Strunz and B. P. Otis, "Erratum to “A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting” [Apr 10 741-750]," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 324-324, Jan. 2021.

[5] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV Startup Voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333-341, Jan. 2011.

[6] S. Bose, T. Anand and M. L. Johnston, "A 3.5-mV input single-inductor self-starting boost converter with loss-aware MPPT for efficient autonomous body-heat energy harvesting," *IEEE J. Solid-State Circuits*, vol. 56, no 6, pp. 1837–1848, June 2021.

[7] M. Alhawari, B. Mohammad, H. Saleh and M. Ismail, "An efficient polarity detection technique for thermoelectric harvester in L-based converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 3, pp. 705–716, Mar. 2017.

[8] C. Souza, et al., “On harvesting energy from tree trunks for environmental monitoring,” *Int. J. of Distributed Sensor Networks*, June 2016.

[9] Y. An, M. Hockman, O. Baiocchi and S. Teng, "Computational model for temperature in tree trunk for energy harvesting," in *IEEE International IOT, Electronics and Mechatronics Conference (IEMTRONICS)*, Vancouver, BC, Canada, 2020, pp. 1-6.

[10] C. T. Hsu, et al., “Experiments and simulations on low-temperature waste heat harvesting system by Thermoelectric Power Generators.” *Applied Energy*, vol. 88, no. 4, pp. 1291–1297, Apr. 2011.

[11] J. Haidar and J. Ghojel, “Waste heat recovery from the exhaust of low-power diesel engine using thermoelectric generators,” in *Proceedings of the International conf. of thermal electrics*, Beijing, China, p. 413, 2001.

[12] A. Moser, *et al.*, “Thermoelectric energy harvesting from transient ambient temperature gradients,” *J. Electron. Mater.*, vol. 41, pp 1653–1661, Feb. 2012.

[13] L. Sigrist, N. Stricker, D. Bernath, J. Beutel and L. Thiele, “Thermoelectric energy harvesting from gradients in the Earth surface,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9460–9470, Nov. 2020.

[14] S. A. Whalen and R. C. Dykhuizen, “Thermoelectric energy harvesting from diurnal heat flow in the upper soil layer,” *Energy Conversion and Management*, vol. 64, pp. 397–402, Dec. 2012.

[15] E. E. Lawrence and G. J. Snyder, “A study of heat sink performance in air and soil for use in a thermoelectric energy harvesting device,” in *21st Int. Conf. on Thermoelectrics*, 2002, pp. 446–449.

[16] S. Pullwitt, U. Kulau, R. Hartung and L. Wolf, “A feasibility study on energy harvesting from soil temperature differences,” in *7th Int. Workshop on Real-World Embedded Wireless Systems and Networks*, 2018, pp 1–6.

[17] M. E. Kiziroglou, *et al.*, “Design and fabrication of heat storage thermoelectric harvesting devices,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 302–309, Jan. 2014.

[18] G. Verma and V. Sharma, “A novel thermoelectric energy harvester for wireless sensor network application,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3530–3538, May 2019.

[19] Q. Kuai, H. -Y. Leung, Q. Wan and P. K. T. Mok, "A high-efficiency dual-polarity thermoelectric energy-harvesting interface circuit with cold startup and fast-searching ZCD," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1899-1912, Jun. 2022.

[20] E. J. Carlson and J. R. Smith, "A ± 0.5-mV-minimum-input DC-DC converter with stepwise adiabatic gate-drive and efficient timing control for thermoelectric energy harvesting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 2, pp. 977–990, Feb. 2023.

[21] A. Dancy, “Power supplies for ultra low power applications,” M.S. Thesis, Dept. of Electrical Eng. and Comp. Sci., MIT, Boston, MA, 1996.

[22] J. M. Damaschke, "Design of a low-input-voltage converter for thermoelectric generator," *IEEE Transactions on Industry Applications*, vol. 33, no. 5, pp. 1203–1207, Sep 1997.

[23] P. S. Weng, H. Y. Tang, P. C. Ku and L. H. Lu, "50 mV-Input batteryless boost converter for thermal energy harvesting," IEEE Journal of Solid-State Circuits, vol. 48, no. 4, pp. 1031–1041, April 2013.

[24] E. J. Carlson, “An ultra-low-voltage Low-power Boost Converter IC for Energy Harvesting Applications,” M.S. Thesis, Dept. of Electrical Eng., University of Washington, Seattle, WA, 2008.

[25] H. Dillersberger, B. Deutschmann and D. Tham, “A bipolar ±13 mV self-starting and 85% peak efficiency DC/DC converter for thermoelectric energy harvesting.” *Energies*, vol. 13, no. 20, Oct. 2020.

[26] P. Cao, *et al.*, “A bipolar-input thermoelectric energy-harvesting interface with boost/flyback hybrid converter and on-chip cold starter,” *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3362–3374, Dec. 2019.

[27] EM Microelectronic, “Ultra-low voltage DCDC boost converter for thermal electrical generators,” *EM8900 datasheet*, Mar. 2017. https://www.emmicroelectronic.com/sites/default/files/products/datasheets/8900-ds.pdf (accessed Jan. 2023).

[28] S. Siouane, S. Jovanovic, and P. Poure, “Equivalent electrical circuits of thermoelectric generators under different operating conditions,” *Energies*, vol. 10, no. 3, p. 386, Mar. 2017.

[29] K. Zhu, B. Deng, P. Zhang, H.S. Kim, P. Jiang, and W. Liu, “System efficiency and power: the bridge between the device and system of a thermoelectric power generator,” *Energy and Environmental Science*, vol. 13, no. 10, 2020, pp. 3514–3526.

[30] C. Goupil, H. Ouerdane, K. Zabrocki, W. Seifert, N. F. Hinsche, and E. Müller, “Thermodynamics and thermoelectricity,” in *Continuum Theory and Modeling of Thermoelectric Elements*”, John Wiley & Sons, Ltd., 2016, pp 1–74.

[31] N. T. Purcell, J. D. Stevens, E. Carlson, G. Boyer and O. R. Baiocchi, "Harvesting energy from tree trunks," *2019 International Energy and Sustainability Conference (IESC)*, 2019, pp. 1–12.

[32] B. R. Helliker and S. L. Richter. "Subtropical to boreal convergence of tree-leaf temperatures." *Nature*, vol 454, no. 7203, pp. 511–514, Jul. 2008.

[33] M. Markiewicz et al., “Software controlled low cost thermoelectric energy harvester for ultra-low power wireless sensor nodes,” *IEEE Access*, vol. 8, pp. 38920–38930, Mar. 2020.

[34] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics*, 2nd ed. John Whiley, 1995.

[35] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, “Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOS circuits,” in *Proc. Of the IEEE*, vol. 9, no. 2, pp. 305–327, Feb. 2003.

[36] Analog Devices, “Auto-polarity, ultralow voltage step-up converter and power manager,” *LTC3109 datasheet*, Wilmington, MA, USA, 2010. https://www.analog.com/media/en/technical-documentation/data-sheets/3109fb.pdf (accessed Jan. 2023).

[37] X. Wu, et al., "A 20-pW Discontinuous switched-capacitor energy harvester for smart sensor applications," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 972–984, Apr. 2017.

[38] C. Chiang and C. Chen, “Zero-voltage-switching control for a PWM buck converter under DCM/CCM boundary,” in *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2120–2126, Sep. 2009.

[39] L. Balogh, “Design and application guide for high speed MOSFET gate drive circuits,” in *Power Supply Design Seminar (SEM 1400)*, 2001.

[40] J. N. Park and T. R. Zaloum, "A dual mode forward/flyback converter," *IEEE Power Electronics Specialists conf.*, 1982, pp. 3–13.

[41] TDK, “Ferrites and accessories,” *B64290L0632X038 datasheet*, Tokyo, Japan, Oct. 2022. https://www.tdk-electronics.tdk.com/inf/80/db/fer/r_20_0_10_0_7_0.pdf (accessed, Jan. 2023).

[42] W. Hurley, “Inductor Design,” in *Transformers and Inductors for Power Electronics: Theory, Design and Applications*. John Wiley & Sons, Incorporated, 2013, pp. 55–83.

[43] TDK, “Ferrites and accessories,” *SIFERRIT material T38 datasheet*, Tokyo Japan, May 2017. https://www.tdk-electronics.tdk.com/download/528868/a1b2c78870f91bc39bb4d281dba6b50c/pdf-t38.pdf (accessed Jan. 2023).

[44] Nichicon, “Conductive polymer aluminum solid electrolytic capacitors,” *PLG datasheet*, Kyoto, Japan. https://www.nichicon.co.jp/english/products/pdfs/e-plg.pdf (accessed Jan. 2023).

[45] Cornell Dubilier Electronics, “Aluminum polymer capacitors, high temperature,” *AVG datasheet*, Liberty SC. https://www.cde.com/resources/catalogs/AVG.pdf (accessed Jan. 2023).

[46] Wurth Electronik, “WCAP-PTHR aluminum polymer capacitors,” *PTEF125470M100DSPA9B000 datasheet*, Niedernhall, Baden-Wurttemberg, Germany. https://www.we-online.com/components/products/datasheet/870055975004.pdf (accessed Jan. 2023).

[47] H. Fujita, “A resonant gate-drive circuit capable of high-frequency and high-efficiency operation,” *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 962–969, Apr. 2010.

[48] E. J. Carlson and J. R. Smith, “An analytical model for stepwise adiabatic driver energy consumption,” 2022, arXiv:2210.16680 [eess.SY].

[49] L. J. Svensson and J. G. Koller, “Driving a capacitive load without dissipating fCV^2,” in *IEEE Symp. Low Power Electronics*, Oct. 1994, pp. 100–101.

[50] L. J. Svensson and J. G. Koller, “Adiabatic charging without inductors,” USC/ISI technical report ACMOS-TR-3a, Feb. 1994.

[51] M. van Elzakker, et al., "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1007– 1015, May 2010.

[52] A. Khorami and M. Sharifkhani, "General characterization method and a fast load-charge-preserving switching procedure for the stepwise adiabatic circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 1, pp. 80–90, Jan. 2016.

[53] M. Arsalan and M. Shams, "Charge-recovery power clock generators for adiabatic logic circuits," 18th Int, Conf. VLSI Design, 2005, pp. 171–174.

[54] J. Park, et al., "A mutual capacitance touch readout IC with 64% reduced-power adiabatic driving over heavily coupled touch screen," IEEE J. Solid-State Circuits, vol. 54, no. 6, pp. 1694–1704, Jun. 2019.

[55] F.Veirano, P. C. Lisboa, P. Perez-Nicoli, L. Naviner, F. Silveira, “Analysis of stepwise charging limits and its implementation for efficiency improvement in switch capacitor DC-DC converters,” *Analog Integr Circ Sig Process*, vol. 109, pp. 271–282, Nov. 2021.

[56] A. Khorami, R. Saeidi, “Energy consumption analysis of the stepwise adiabatic circuits,” *Microelectronics Journal*, vol. 104, Oct. 2020.

[57] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[58] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 599–606, May 1999.

[59] J. Rabaey, A. Chandrakasan and B. Nikolić, “The devices,” in *Digital Integrated Circuits: A Design Perspective,* 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2003, pp. 99–100.

[60] T. Paing, J. Shin, R. Zane, and Z. Popovic, “Resistor emulation approach to low-power RF energy harvesting,” *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1494–1501, May 2008.

[61] R. L. Radin, M. Sawan, C. Galup-Montoro and M. C. Schneider, "A 7.5- mV-input boost converter for thermal energy harvesting with 11-mV self-startup," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 67, no. 8, pp. 1379–1383, Aug. 2020.

[62] Z. Luo, L. Zeng, B. Lau, Y. Lian and C. Heng, "A sub-10 mV power converter with fully integrated self-start, MPPT, and ZCS control for thermoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1744–1757, May 2018.

[63] G. Chowdary and S. Chatterjee, "A 300-nW Sensitive, 50-nA DC-DC converter for energy harvesting applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 11, pp. 2674–2684, Nov. 2015.

[64] N. Femia, G. Petrone, G. Spagnuolo and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," in IEEE Transactions on Power Electronics, vol. 20, no. 4, pp. 963–973, July 2005.

[65] B. Acker, C. R. Sullivan and S. R. Sanders, “Synchronous rectification with adaptive timing control,” in *26th Annual IEEE Power Electronics Specialists Conf. Record, PESC’95*, Jun. 18–22, 1995, vol. 1, pp. 88.

[66] R. L. Radin, M. Sawan and M. C. Schneider, "An accurate zero-current-switching circuit for ultra-low-voltage boost converters," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 68, no. 6, pp. 1773–1777, Jun. 2021.

[67] N. V. Desai, Y. K. Ramadass and A. P. Chandrakasan, “A bipolar ±40 mV self-starting boost converter with transformer reuse for thermoelectric energy harvesting,” in *IEEE/ACM Int. Symp. Low on Power Electronics and Design (ISLPED)*, 2014, pp. 221–226.

[68] T. Williams, “Passive Components,” in *The Circuit Designer’s Companion*, 2nd ed. Elsevier, 2005, ch. 3, pp. 70–79.

[69] *Low-level measurement handbook*, 7th ed., Keithley Instruments, Cleveland, OH. https://download.tek.com/document/LowLevelHandbook_7Ed.pdf (accessed Jan. 2023).

[70] G. Harman, *Wire Bonding in Microelectronics*, 3rd ed. New York: McGraw-Hill, 2010.

[71] Keithley Instruments, “Sub-femptoamp remote sourcemeter SMU instrument,” *6430 datasheet*, Cleveland, OH. https://download.tek.com/datasheet/6430.pdf (accessed Jan. 2023).

[72] *Model 6430 Sub-Femptoamp Remote SourceMeter Instruction Manual*, Keithley Instruments, Cleveland, OH, 1999.

[73] S. Sung, S. Whan, J. Lee, and I. Lee, *Process Identification and PID Control.* John Wiley, 2009.

[74] Analog Devices, “Precision low power single-supply JFET amplifier,” *AD8627 datasheet*, Wilmington, MA, USA, 2013. https://www.analog.com/media/en/technical-documentation/data-sheets/ad8625_8626_8627.pdf (accessed Jan. 2023).

[75] Keysight Technologies, “USB modular digital multimeter,” *U2741A datasheet*, Santa Rosa, CA. https://www.keysight.com/us/en/assets/7018-03382/data-sheets/5991-0042.pdf (accessed Jan. 2023).

[76] S. Franco, “Dynamic Op Amp Limitations,” in *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed. McGraw-Hill, 2002, ch. 5, pp. 210–249.

[77] Analog Devices, “Op-amp noise,” *MT-047 Tutorial*, Wilmington, MA, 2009. https://www.analog.com/media/en/training-seminars/tutorials/MT-047.pdf (accessed Jan. 2023).

[78] LabJack, “Affordable multifunction DAQ with USB, *U3 datasheet*, Lakewood, CO, 2020. https://files.labjack.com/datasheets/LabJack-U3-Datasheet.pdf.

[79] I. Ike, I. Sigalas, and S. Iyuke, “Understanding performance limitation and suppression of leakage current or self-discharge in-electrochemical capacitors: a review.” *Physical Chemistry Chemical Physics*, vol. 18, no. 2, pp. 661–680, 2016.

[80] Keysight Technologies, “Digital Multimeter,” *34401A datasheet*, Santa Rosa, CA. https://www.keysight.com/us/en/assets/7018-06774/data-sheets/5968-0162.pdf (accessed Jan. 2023).

[81] Linear Technology, “Precision refence,” *LT1019 datasheet*, Milpitas, CA, 1993. https://www.analog.com/media/en/technical-documentation/data-sheets/1019fd.pdf.

[82] Riedon, “Precision shunt resistors,” *FPR 2-T218 datasheet*, Alhambra, CA, 2019. https://riedon.com/media/pdf/FPR2T218.pdf (accessed Jan. 2023).

[83] Maxim Integrated, “36V low-noise, precision, single/quad/dual op amps,”, *MAX 44241 datasheet*, San Jose, CA, 2015. https://www.analog.com/media/en/technical-documentation/data-sheets/max44241-max44246.pdf.

[84] ON Semiconductor, “N-channel enhancement mode field effect transistor,” *2N7000 datasheet*, Phoenix, AZ. https://www.onsemi.com/pdf/datasheet/nds7002a-d.pdf (accessed Jan. 2023).

[85] Rigol, “DS1000Z series digital oscilloscope,” *DS1054Z datasheet*, Suzhou, China. https://beyondmeasure.rigoltech.com/acton/attachment/1579/f-0504/1/-/-/-/-/MSO1000Z_Datasheet.pdf (accessed Jan. 2023).

[86] Central Semiconductor, “Surface mount silicon NPN transistor,” *CZT2222A datasheet*. https://my.centralsemi.com/datasheets/CZT2222A.PDF (accessed Jan. 2023).

[87] ON Semiconductor, “JFET – VHF/UHF amplifier transistor, N-channel,” Phoenix, AZ, Oct. 2016. https://www.onsemi.com/pdf/datasheet/mmbfj309lt1-d.pdf.

[88] R. Jaeger, “Field-Effect Transistors,” in *Microelectronic Circuit Design*, McGraw-Hill, 1997, ch. 4, pp. 148–155.

[89] S. Bandyopadhyay, et al., “A 1.1 nW energy-harvesting system with 544 pW quiescent power for next-generation implants,” *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2812–2824, Dec. 2014.

[90] TEC, “Wearables/harvesting module,” *TEG2-126LDT datasheet*, Aurora, ON, Canada, Oct. 2017. https://tecteg.com/wp-content/uploads/2015/11/TEG2-126LDT-Spec.-sheet.1.-REV..pdf (accessed Jan. 2023).

[91] Texas Instruments, “Precision Centigrade Temperature Sensors,” *LM35 datasheet*, Dallas, Texas, Aug. 1999. https://www.ti.com/lit/ds/symlink/lm35.pdf (accessed Jan. 2023).

VITA

Eric J. Carlson earned his Ph.D. degree in Electrical and Computer Engineering at the University of Washington in June, 2023. He received his M.S. degree and B.S. degree in Electrical Engineering from the University of Washington in December, 2008 and June, 2006, respectively. Eric started academic research under Professor Kai Strunz in 2004 working on circuit simulators for power electronics. In 2007 he joined the Wireless Sensing Lab under Professor Brian Otis designing a low-input-voltage DC-DC converter for energy harvesting and wireless sensing applications and was co-advised by Professors Brian Otis and Kai Strunz. Eric produced several well-renowned publications from this work, where he demonstrated powering circuits thermoelectrically from body heat and also demonstrated the first regulated power supply utilizing energy harvested from the electrochemical potentials within trees. In 2015, Eric returned to the University of Washington to complete his Ph.D. under Professor Joshua Smith and the Sensor Systems Lab, where he completed the work described in this dissertation and published a paper on stepwise adiabatic gate-drive and low-voltage thermoelectric energy harvesting.

Eric joined Texas Instruments (formerly National Semiconductor) as an analog design intern in 2007 and became a full-time employee in 2009, where he is still employed. During his tenure at Texas Instruments, he has worked in the Mobile Devices Power, FPD-Link, and Clock and Timing Solutions product lines.

Eric was the recipient of the Granger Foundation Fellowship and the Robert Rushmer fellowship. He was also awarded a grant from the DOE for his work on harvesting energy from the electrochemical potentials within trees. At Texas Instruments he was a finalist in the Mobility Design Challenge competition for proposing an innovative battery management solution.