# High-Speed Optical Modulators and Data Communication Systems in Silicon Photonics

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**Abstract**

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Silicon photonics provides a promising platform for developing densely integrated, highly scalable and potentially very low cost solutions for various applications in the field of optical data communications. This thesis focuses on the technical challenges in silicon photonics on both the component and system levels.

One of the most important components in optical transmitters is the electro-optic modulator. However, building high-speed efficient modulators in silicon remains to be one of the key challenges of silicon photonics. To achieve more efficient modulators, the first approach presented here is to incorporate new materials into the silicon platform with new device geometries. With highly efficient electro-optical polymers and low-loss silicon striploaded slot waveguide, we demonstrated the first silicon-polymer hybrid modulator operating with GHz bandwidth as well as the first sub-1 $V_\pi$ device at RF frequency. The second approach is innovative RF design, through which we demonstrated 40 Gb/s power-efficient silicon pn-junction traveling-wave Mach-Zehnder modulators showing compelling performance compared to commercial Lithium Niobate modulators.

At the time of writing, system level designs in silicon photonics are far from mature. A critical barrier toward system design is the lack of established stable fabrication processes and process design kits (PDKs). I participated in and lead the testing effort of the early development of an monolithic silicon photonics platform (OpSIS-IME). High-speed (50 Gb/s) modulators and detectors as well as high-performance passive components co-exist in the

same process with consistent performance and high yield. This opens up tremendous opportunities for systems. Upon this platform, we demonstrated various kinds of high-speed high-performance transmitters and receivers using different topologies and device approaches, showing a level of integration beyond the state-of-the-art.

For a power-efficient and high-performance photonics system, electronics and in particular the high-speed analog front-end that directly interfaces with the photonic devices is an integral part and to a great extent determines system-level performance. Furthermore, close-integration and co-design offer potentially significant improvement to the overall system performance. Among several other high-speed analog circuits results, we have demonstrated on both the optical transmitter and the receiver sides, that ultra-high data rate (100 Gb/s non-return-to-zero) is plausible in existing silicon-based photonics and electronics technology.

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## ACKNOWLEDGMENTS

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# Chapter 1

# INTRODUCTION

## *1.1 Background: recent progress in silicon photonics*

The field of silicon photonics has been an active research area and has expanded substantially in recent years. Its diverse applications range from biosensing [1] to RF-over-fiber [2] to hyperspectral imaging [3]. One of the most promising application areas where silicon photonics based devices and systems can be widely deployed is data transmission. Optical data links offer superior performance over their electrical counterparts, mainly due to their low loss, immunity to interference and ultra-high bandwidth. As the cost of optical links falls and its performance improves, the application area has moved from long-haul telecom to shorter reach datacom. Recently there have been proposals to construct optical links to break the chip-to-chip electrical I/O bottleneck (so-called computer-com applications). With mature CMOS fabrication, silicon-based photonics, when compared to III/V systems, can offer high-density, highly scalable and low-cost solutions.

Silicon photonics devices can be fabricated with advanced CMOS photolithography and other standard processing tools. This method offers tight dimension control and therefore has successfully produced low-loss waveguides [4], grating couplers [5] and various other passive components [6]. The main platform is a silicon-on-insulator (SOI) substrate, where the insulator layer offers a buffer layer that prevents light from leaking away. However, silicon is not a good material for active photonic components, i.e. lasers, photodetectors and modulators. First, silicon is an indirect bandgap material so constructing lasers in silicon is extremely challenging. Second, since waveguides made in silicon are used for routing light at 1.55 $\mu$m, silicon is transparent at this wavelength so another material with a smaller bandgap must be incorporated to achieve photodetection. Third, the symmetry of the silicon lattice makes the second-order nonlinear optical coefficient zero in un-strained silicon, therefore electro-optic modulation in silicon seemed impossible initially.

Despite the challenges of building active photonic devices on silicon, remarkable progress has been made in this area. Raman lasers were achieved in pure silicon [7] and InP based hybrid integration schemes [8] are becoming increasingly adept at bringing lasers to silicon. Carrier plasma dispersion effect [9] as well as other novel mechanisms [10] are employed toward building efficient modulators in silicon and remain to be an active area of research. Germanium growth is achieved at a low temperature that is compatible with CMOS back-end processes, which enabled monolithically integrating Ge-on-Si detectors with other silicon photonics components [11]. Fig. 1.1 shows an SOI silicon photonics platform, where silicon waveguides, modulators and Ge-based detectors are monolithically integrated.

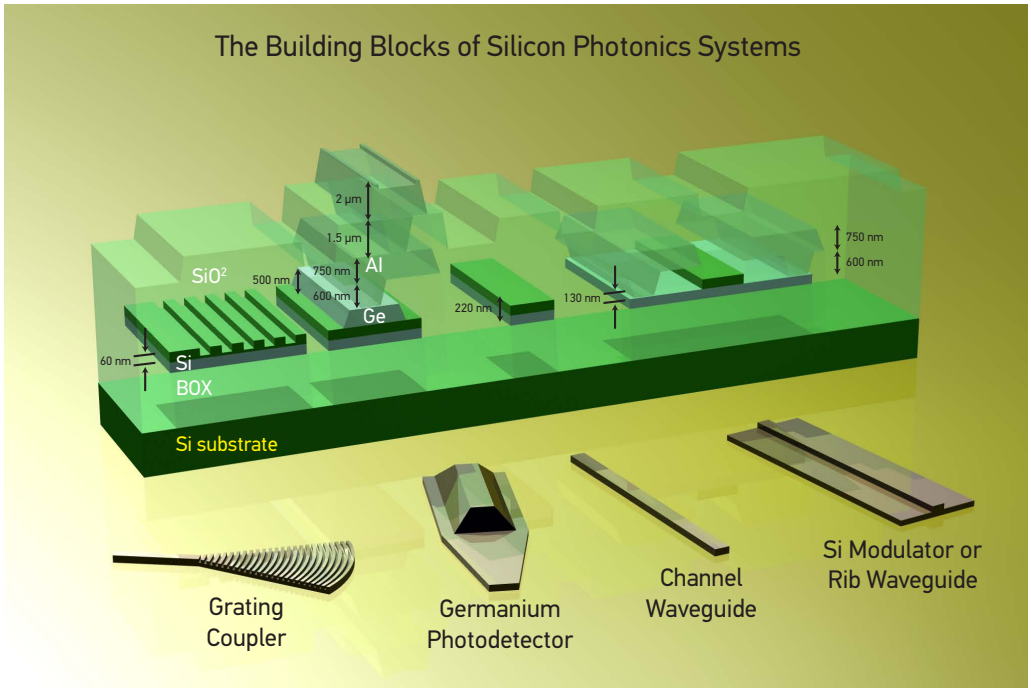



Figure 1.1: (From [12]) 3D rendering of an SOI photonics platform, showing key building components: grating couplers, waveguides and Ge-on-Si photodetectors. More details are discussed in Chapter 4.

### *1.2 Organization of this work*

The contents of this thesis arise from results that were published or currently under consideration at journals and conferences. These papers are listed in Section 1.3 and are referenced below to associate them with respective chapters and sections. The work described in this thesis is organized into three areas: (1) photonics device innovation, (2) photonics platform development and system design, and (3) high-speed electronics and electronics-photonics co-design.

At the device level, my main focus is building high-performance modulators at high-speed, which remains to be one of the key challenges of silicon photonics. Chapter 2 discusses my work in silicon-polymer modulators, focusing on how incorporating new materials into the silicon platform and utilizing new device geometries achieve more efficient modulators compared to conventional approaches. With highly efficient electro-optical nonlinear polymers and low-loss silicon striploaded slot waveguide [13,11], we demonstrated the world's first silicon-polymer hybrid modulator operating with GHz bandwidth [14] as well as the first sub-1 $V_\pi$ device at RF frequency [12].

Chapter 3 describes my work in all-silicon modulator using plasma dispersion effect, with a key focus on traveling-wave design and characterization [10,8,6,5]. A particularly interesting design is slow-wave electrode traveling-wave Mach-Zehnder [3], which offer a promising way to drive highly capacitive pn junctions at 50 Ω. We experimented with periodical phase matching and showed that the EO 3-dB bandwidth closely tracked RF 6.4-dB bandwidth, indicating the RF and optical velocities overall are well matched despite their strong intrinsic mismatch within each individual section. The design also addresses several long-standing problems in prior art, such as RF multi-mode and intra-device cross-talk. At 40 Gb/s, under similar modulator depth, the silicon device showed comparable performance to that of a commercial 40 Gb/s Lithium Niobate modulator in terms of bit-error-rate versus optical-signal-to-noise-ratio.

At the time of writing, system level design in silicon photonics is far from mature due to the lack of established stable fabrication processes and process design kits (PDKs). Chapter 4 first describes a silicon photonics platform that I helped develop in the OpSIS project. In this

platform, passive optics components, high-speed modulators and detectors are monolithically integrated and a relatively complete photonics device library is made available to the research community in the form of a maintained PDK (similar to what has been done in electronics) to finally enable system-level designs. This is the first silicon platform that offers a complete 25 Gb/s (then 50 Gb/s) capability and at wavelengths of both 1550 nm and 1310 nm [9,7]. The second part of Chapter 4 discusses and showcases several systems [4] built on this platform.

For a power-efficient and high-performance photonics system, electronics and in particular the high-speed analog front-end that directly interfaces with the photonic devices is an integral part and to a great degree determines system-level performance. Chapter 5 describes my work in high-speed analog circuit design as well as explorations in co-designing electronics circuits with photonics devices to enhance the overall performance. For energy-efficient ultra-high-speed optical receivers, we demonstrated a 86 GHz broadband transimpedance amplifier in a 130-nm SiGe BiCMOS process, with the highest GBW/$P_{dc}$ efficiency figure, the smallest area, low GDV and low noise [1]. On the transmitter side, we explored electronics-photonics co-design of a 100 Gb/s modulator driver, showing that such data rate is plausible with today's existing silicon-based electronics and photonics technology [2].

### *1.3 Papers related to this work*

This section lists the papers directly related to this work. A full publication list is in Appendix A and is also available at Google Scholar.

1. **R. Ding**, Z. Xuan, P. Yao, D. Prather, M. Hochberg, and T. Baehr-Jones "Power-efficient low-noise 86 GHz broadband amplifier in 130-nm SiGe BiCMOS," submitted to Electronics Letters.

2. **R. Ding**, Z. Xuan, P. Yao, T. Baehr-Jones, D. Prather and M. Hochberg, "100-Gb/s NRZ Optical Transceiver Analog Front-End in 130-nm SiGe BiCMOS," submitted to Optical Interconnect 2014.

3. **R. Ding**, Y. Liu, Y. Ma, Y. Yang, Q. Li, A. E.-J. Lim, G.-Q. Lo, K. Bergman, T. Baehr-Jones and M. Hochberg, "High-speed silicon modulator with slow-wave transmission line electrodes and fully-independent differential drive," submitted to Journal of Lightwave Technology.

4. Y. Liu*, **R. Ding***, Q. Li, X. Zhe, Y. Li, Y. Yang, A. E. Lim, P. G.-Q. Lo, K. Bergman, T. Baehr-Jones and M. Hochberg, "Ultra-compact 320 Gb/s and 160 Gb/s WDM transmitters based on silicon microrings", to appear at OFC 2014 as paper Th4G.6. [*Equal contribution authors]

5. **R. Ding**, Y. Liu, Q. Li, Y. Yang, Y. Ma, K. Padmaraju, A. E.-J. Lim, G.-Q. Lo, K. Bergman, T. Baehr-Jones, and M. Hochberg, "Design and characterization of a 30-GHz bandwidth low-power silicon traveling-wave modulator,", Optics Communications, 321, 124–133 (2014).

6. M. Streshinsky, **R. Ding**, Y. Liu, A. Novack, Y. Yang, Y. Ma, X. Tu, E. Chee, A. Lim, P. Lo, T. Baehr-Jones, and M. Hochberg, "Low power 50 Gb/s silicon traveling wave Mach-Zehnder modulator near 1300 nm," Optics Express, 21, 30350-30357 (2013).

7. Y. Liu, **R. Ding**, M. Gould, T. Baehr-Jones, Y. Yang, Y. Ma, Y. Zhang, A. E.-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, M. Hochberg, "30 GHz Silicon Platform for Photonics System", (**invited**),Optical Interconnects 2013

8. **R. Ding**, T. Baehr-Jones, Y. Liu, A. Ayazi, T. Pinguet, N. Harris, M. Streshinsky, P. Lee, Y. Zhang, A. E-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, and M. Hochberg, "A 25 Gb/s 400 fJ/bit Silicon Traveling-Wave Modulator", (upgraded to **invited** paper at Optical Interconnects 2012).

9. **R. Ding**, T. Baehr-Jones, T. Pinguet, J. Li, N. C. Harris, M. Streshinsky, L. He, A. Novack, A. E-J. Lim, T-Y. Liow, S. H-G. Teo, G-Q. Lo and M. Hochberg, "A Silicon Platform for High-Speed Photonics Systems", (upgraded to **invited** paper at OFC/NFOEC 2012).

10. T. Baehr-Jones, **R. Ding**, Y. Liu, A. Ayazi, T. Pinguet, N. Harris, M. Streshinsky, P. Lee, Y. Zhang, A. E-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, and M. Hochberg, "Ultralow drive voltage silicon traveling-wave modulator", Optics Express, 20, 12014-12020 (2012).

11. **R. Ding**, T. Baehr-Jones, W-J. Kim, B. Boyko, R. Bojko, A. Spott, A. Pomerene, C. Hill, W. Reinhardt, and M. Hochberg, "Low-loss Asymmetric Strip-loaded Slot Waveguides in Silicon-on-Insulator", Applied Physics Letters, 98, 233303 (2011).

12. **R. Ding**, T. Baehr-Jones, W-J. Kim, A. Spott, M. Fournier, J-M. Fedeli, S. Huang, J. Luo, A. K-Y. Jen, L. Dalton, M. Hochberg, "Sub-Volt Silicon-Organic Electro-optic Modulator With 500 MHz Bandwidth", Journal of Lightwave Technology, 29 (8), 1112-1117 (2011).

13. **R. Ding**, T. Baehr-Jones, W-J. Kim, X. Xiong, R. Bojko, J-M. Fedeli, M. Fournier, and M. Hochberg, "Low-loss strip-loaded slot waveguides in Silicon-on-Insulator", Optics Express, 18, 25061-25067 (2010).

14. **R. Ding**, T. Baehr-Jones, Y. Liu, R. Bojko, J. Witzens, S. Huang, J. Luo, S. Benight, P. Sullivan, J-M. Fedeli, M. Fournier, L. Dalton, A. Jen, and M. Hochberg, "Demonstration of a low V$\pi$L modulator with GHz bandwidth based on electro-optic polymer-clad silicon slot waveguides", Optics Express, 18, 15618-15623 (2010).

Chapter 2

# SILICON SLOT-WAVEGUIDES AND SILICON-POLYMER MODULATORS

In this chapter, I discuss my work in silicon-polymer modulators. A remedy to silicon's lack of EO coefficient is to incorporate new materials into the silicon platform and to utilize new device geometries [10]. In particular, slot waveguide geometries [13] can be used to enhance the optical field and to drive the electrical field inside the slot that is filled with low-index polymer material. These highly active electro-optic polymers have been developed and are commercially available. With slot enhancement and engineered high polymer EO coefficients, modulator performance can be significantly improved compared to other approaches.

## *2.1 Slot and strip-loaded slot waveguides*

A slot waveguide consists of two ridges of high index material, such as silicon, narrowly separated from each other by a fully-etched trench that is to be filled with a lower index material. The fundamental TE optical mode tends to be highly concentrated in the void region between the two ridges due to the dielectric discontinuity [13]. Both the narrow spacing of the dielectric arms and the high field concentration provide fundamental advantages for building electro-optic modulators based on slot waveguide geometries [14].

The strip-loaded silicon slot waveguide consists of two silicon arms (un-etched silicon) each with a wide strip-loading region (partially etched silicon), as shown in Fig.2.1. Electrical contact can then be made once the silicon strip-loading is doped by putting metal electrodes on top of the strip-loading region allowing a clearance from the waveguide.

We chose a thickness for un-etched silicon of 220 nm. Making the silicon too thin makes the strip-loading design difficult, while making it too thick makes the waveguide multimode; a 220 nm thickness is a good intermediate value that is both single-mode, and thick enough to support strip-loading thicknesses of reasonable height. In addition to the thickness of

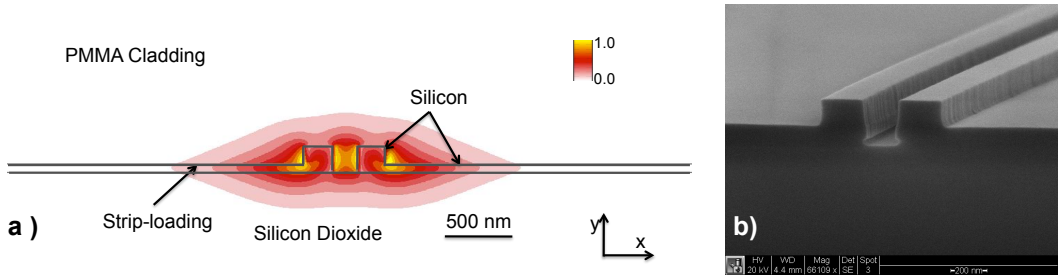



Figure 2.1: (a) Geometry of a strip-loaded slot waveguide. The waveguide has a 200-nm wide slot and a 230-nm wide arm; the silicon height is 220 nm while the strip-loading thickness is 60 nm. The mode is calculated with cladding material refractive index $n_{cladding}$=1.5, and the $E_x$ component of the $TE_0$ mode is shown overlaying the geometry (b) SEM micrograph shows the cross-section of a fabricated waveguide.

the un-etched silicon layer, there are a number of parameters that define each waveguide. Probably the most important parameter is the width of the slot; narrower slots lead to lower drive voltages [15], but are harder to fabricate.

The fabrication of the slot waveguides was done on Silicon-On-Insulator (SOI) wafers with two self-aligned photolithography steps on a 193 nm stepper and two Si dry etching steps. The SOI wafers have a 220 nm thick silicon layer, and a 2 $\mu$m thick buried oxide layer. The process started with a hardmask of 80 nm High Temperature Oxide (HTO) layer on top of the silicon layer (Fig. 2.2a). First, the waveguide arms/slot were patterned (Fig. 2.2b). In this photolithography step, we varied the exposure doses to account for etch bias of the slot. After that, an RIE silica etch with C4F8 was used to remove the hardmask. The quality of the edges is given by the resist roughness and by the recipe of the hard mask etching. The silicon exposed was then partially etched with HBr gases and the remaining thickness of silicon was measured by ellipsometry. As an example, Fig. 2.2c) shows that a 70 nm silicon is left in the etched area, which will finally lead to ≈60nm strip-loading.

In the second lithography step, the remaining hardmask served as a self-alignment, so that the resist to slot overlay became non-critical (Fig. 2.2d). Then a full silicon etch removed the remaining silicon inside the slot and cut the strip-loading so that each waveguide is

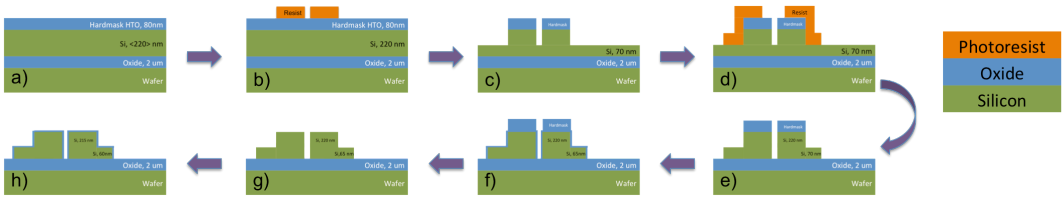



Figure 2.2: Process flow: (a) start with 80 nm HTO on top of SOI; (b) 1st photolithography patterns the waveguide arms; (c) 1st dry etching etches through the hardmask and partially remove silicon, ellipsometry measurement after this step; (d) 2nd photolithography patterns the strip-loading; (e) 2nd dry etching removes silicon inside the slot and cut strip-loading; (f) thermal oxide smoothes the sidewall; (g) strip the remaining hardmask and the thermal oxide, CDSEM after this step; (h) final oxidation serves as passivation. The final step of the PMMA spin-coating is not shown.

electrically and optically isolated (Fig. 2.2e). A 10 nm thin thermal oxide, consuming 4.4 nm silicon [17], was then employed to smooth the waveguide sidewalls (Fig. 2.2f). The remaining hardmask and the thin oxide were removed by a 30 nm SiO2 chemical etch (Fig. 2.2g). After the thin oxide was removed, CDSEM measurements were taken at various sites to determine the actual dimensions of the slots and arms for three different exposure doses in the 1st photolithography step, which were 17.8 mJ/cm$^2$, 19.0 mJ/cm$^2$ and 20.2 mJ/cm$^2$. Finally, another thermal oxidation was done for the purpose of passivation (Fig. 2.2h) which should yield 10 nm oxide and consume another 4.4 nm silicon. The final strip-loading would therefore be 60 nm. With this process, we actually fabricated waveguide with 40nm, 60nm and 70nm strip-loading.

Finally, in order to closely match the expected eventual index of the electro-optic polymers that will be used for actual modulators, we coated the chips in polymethyl methacrylate (PMMA) (MicroChem 950PMMA A 11% solids in Anisole), which has index close to 1.49 and low optical losses on the order of 0.2 dB/cm. A spin-coating was used, typically with spin speed 2000 rpm for 45 seconds, and a bake time of 90 seconds at 180 degree Celcius, which should have resulted in a film thickness of the PMMA of 3 $\mu$m.

To study the waveguide loss, we put five waveguide runouts with lengths ranging from $\sim$1

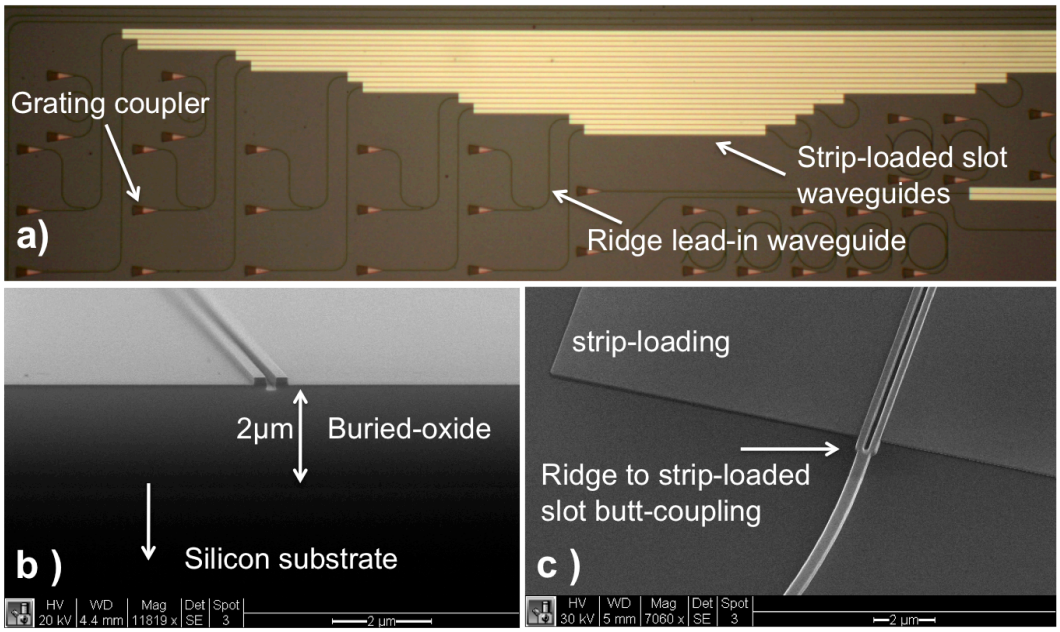



Figure 2.3: (a) Optical micrograph showing the layout of a group of strip-loaded slot waveguide runouts of different lengths; (b) SEM micrograph showing the stack of waveguide, buried-oxide layer and silicon subsrate; (c) SEM micrograph of the ridge waveguide to strip-loaded slot waveguide transition region.

mm to ∼8 mm. on each chip. A diagram of the runout structure geometry is shown in Fig. 2.3(a). Coupling onto the chip is achieved by a series of grating couplers [5], which had typical 3 dB bandwidths of 35 nm, and a typical insertion loss of 9 dB per coupler. A short section of single-mode ridge waveguide was used to lead the light to the strip-loaded slot waveguide; the coupling between ridge and the strip-loaded slot was achieved with butt-coupler, with losses predicted by FDTD of 3 dB. A y-junction is present to allow on-chip mixing for an unrelated experiment. According to FDTD simulations, the y-junction introduces 3.6 dB insertion losses to the runouts. Because each runout structure is identical in all respects, except for the length of the slot waveguide, the losses due to the grating couplers, butt-couplers and y-junctions should not affect our measurements of slot waveguide loss. In order to get similar performances for the grating couplers, these waveguide runouts are compactly laid out, so that they take up only a small fraction of the chip and thereby minimize a

possible fabrication non-uniformity.

Devices were measured with a fiber-coupled Agilent 81980A laser and 81636B detector. Spectra were taken using the built-in sweeping ability of the laser. The laser power used was 6 dBm except as noted elsewhere. Typical fiber-to-fiber insertion losses for the entire testing system, including all fiber wiring, the fiber array, and the integrated optical devices under test were around 35 to 45 dB, which gave us a signal-to-noise ratio of at least 20 dB. On each chip, we tested the five waveguide runouts and fit the spectrum to a quadratic function using the data points near the peak transmission wavelength (the interval was a 40 nm region centered where the wavelength where the optical output signal is at its maximum). Then a regression is employed to fit the peak transmission value extracted from the fitted quadratic function against the waveguide lengths, where we can get waveguide loss in dB per length from the slope of the linear fitting. The linear regression and associated uncertainties in the fitted parameters were computed using standard statistical techniques.

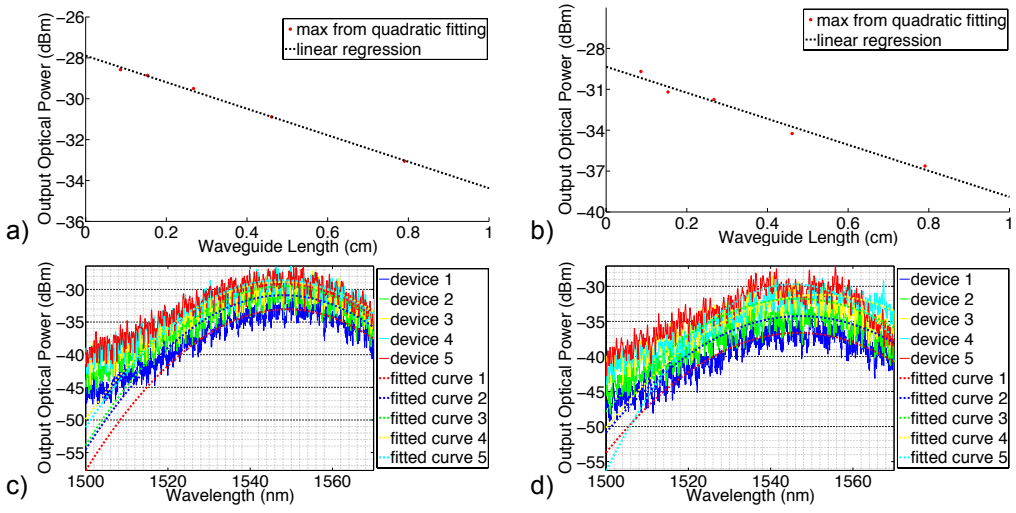



Figure 2.4: Linear regression of peak output optical power vs. waveguide length for (a) chip 1 and )b) chip 4. Spectrum and quadratic function fitting for (c) chip1 and (d) chip4 (the fitting only used data from a section of the spectrum that centers at the peak response wavelength and spans 40 nm). The cladding materials refractive index is $\approx 1.5$.

Fig.2.4 shows example fittings of the spectra and linear regressions for the two chips we tested. We attribute the slight fluctuations seen on the transmission spectra to the back-reflections from the grating couplers, the y-junction and the ridge to slot-waveguide butt-coupler. The low uncertainty of our results indicates that these fluctuations do not impair our ability to measure the waveguide loss of the strip-loaded slot waveguides.

Table 2.1: Summary of waveguide loss and sample information

| **Chip ID** | **Final Strip-loading thickness (nm)** | **Exposure dose in 1st photolithography ($mJ/cm^2$)** | **Final Slot width (nm)** | **Measured loss (dB/cm)** |
|---|---|---|---|---|
| 1 | 39.2 | 19 | 186.4 | 6.5 ± 0.2 |
| 2 | 39.2 | 19.9 | 193.4 | 7.0 ± 0.6 |
| 3 | 58.2 | 19 | 186.4 | 8.8 ± 0.2 |
| 4 | 58.2 | 19.9 | 193.4 | 9.5 ± 0.9 |
| 5 | 67.2 | 20.5 | 198.0 | 8.4 ± 1.0 |
| 6 | 69.2 | 20.5 | 198.0 | 8.0 ± 1.0 |

Data from chips with strip-loading regions of about 40 nm, 60 nm and 70 nm thicknesses are listed in Table 1. It is striking to note that, even when the optical doses are identical, the 40 nm thick strip-loaded waveguides show waveguide losses that are statistically significantly lower than those of waveguides with thicker strip-loading. We believe that thinner strip-loading may cause a more confined optical mode; since there is less overlap with the partially etched silicon, lower losses are observed.

Thus we have experimentally demonstrated low loss strip-loaded slot waveguides with photolithography in SOI. The waveguides that we present data for have not been doped or contacted. With low-optical losses, and a relatively thick silicon strip-loading, high bandwidth slot-waveguide electro-optic polymer modulators can be built. We believe this is an

important step towards realizing practical slot-waveguide polymer devices. We have also found that making a thinner strip-loading section appears to lead to lower losses. Future slot-waveguide modulator designs will likely need to trade optical loss against electrical performance to determine the optimal strip-loading thickness and doping concentrations.

### *2.2 Asymmetric strip-loaded slot waveguide*

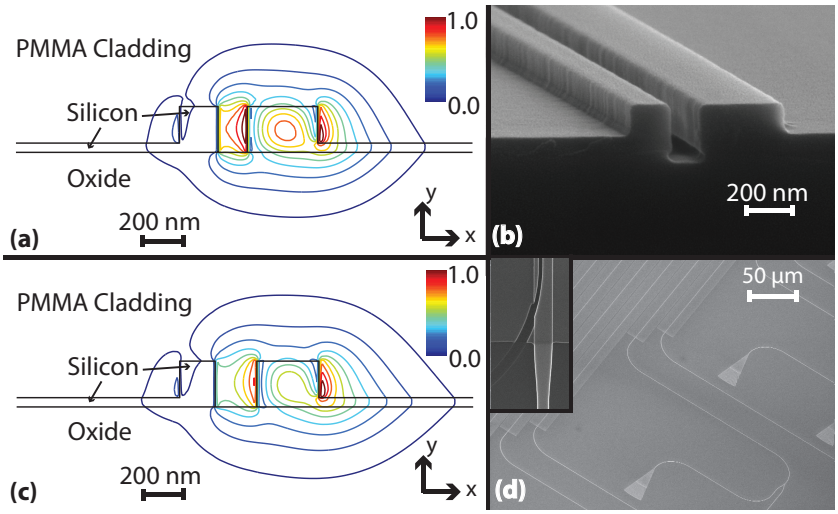



Figure 2.5: (a) $|E_x|$ of $TE_0$ mode of waveguide design 1 (b) SEM micrograph of the cross-section of a fabricated design 1 waveguide (c) $|E_x|$ of $TE_0$ mode of waveguide design 2 (d) SEM micrograph of the waveguide runouts group layout, the inset shows the curve-coupler between the routing ridge waveguide and the asymmetric strip-loaded slot waveguide

An asymmetric strip-loaded SWG is similar to a symmetric strip-loaded SWG discussed in the previous section, but its slot is offset to one side by a modest amount. One of the waveguide designs discussed in this work (design 1) is shown in Fig. 2.5(a) with the fabricated waveguide shown in Fig. 2.5(b). Critical-dimension scanning electron microscopy (CDSEM) and ellipsometry measurements show that typical fabricated samples had around a 200 nm full silicon thickness, a 40 nm strip-loading thickness, a 130 nm slot width, and 170 nm and 310 nm arm widths.

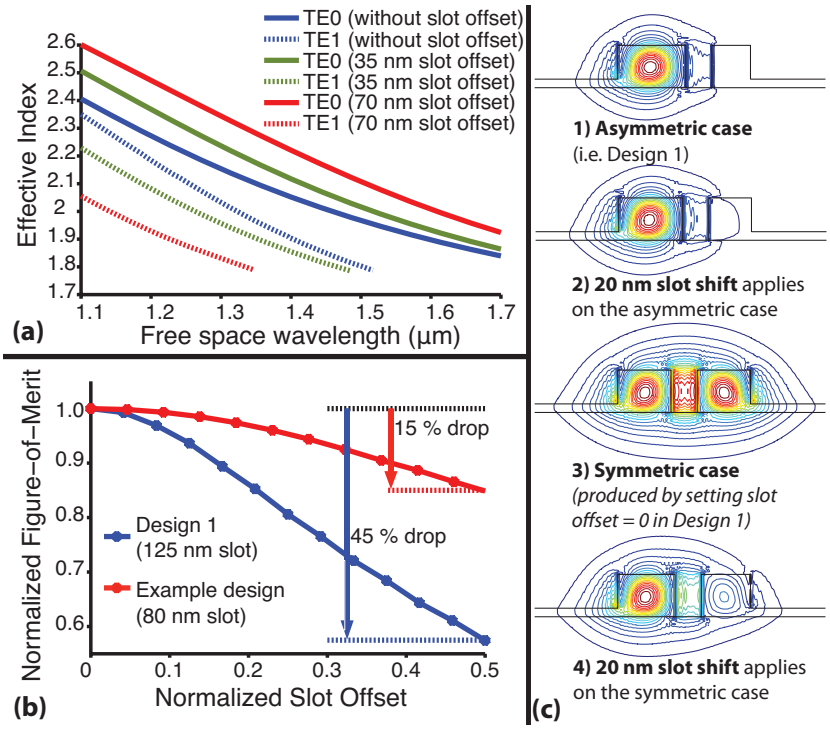



Figure 2.6: (a) Dispersion curves of the $TE_0$ and $TE_1$ mode of design 1 with different slot offsets. (b) Figure-of-merit value $\gamma$ vs. slot offset for design 1 as well as an example design that uses an 80 nm wide slot. The $\gamma$ values are normalized to their maximum value $\gamma_0$ that occurs at zero slot offset. The slot offset is normalized against slot width (c) Sensitivity of modal pattern to variations in slot offset. The magnitude of the Poynting vector is shown.

Single-mode operation in a waveguide requires that higher order modes ($TE_1$ and above) be cut off in the wavelength range of interest. Asymmetric waveguides offer an advantage here. Making the waveguide more and more asymmetric by offsetting the slot to one side while maintaining the total width of the waveguide leads to the $TE_1$ mode being cut off at much shorter wavelengths (Fig. 2.6(a)). This offers a much wider range for single-mode operation, and this in turn leads to better design robustness against process variations. Another useful feature of an asymmetric strip-loaded SWG is that the modal pattern is much less sensitive to slot offset variations. This principle is illustrated in Fig. 2.6(c). This feature suggests that devices based on asymmetric designs will probably be less impacted

by certain fabrication errors such as misalignment.

We measured the transmission spectra of waveguides with various lengths to extract the propagation loss. The groups of waveguides were compactly laid out (Fig. 2.5(c)) to minimize variations caused by possible processing non-uniformity. The average results are presented in the waveguide loss histogram in Fig. 2.7(a). Typical waveguide loss was 2 dB/cm for design 1 and 3 dB/cm for another design with a wider slot (design 2) as suggested by Fig. 2.7(b).

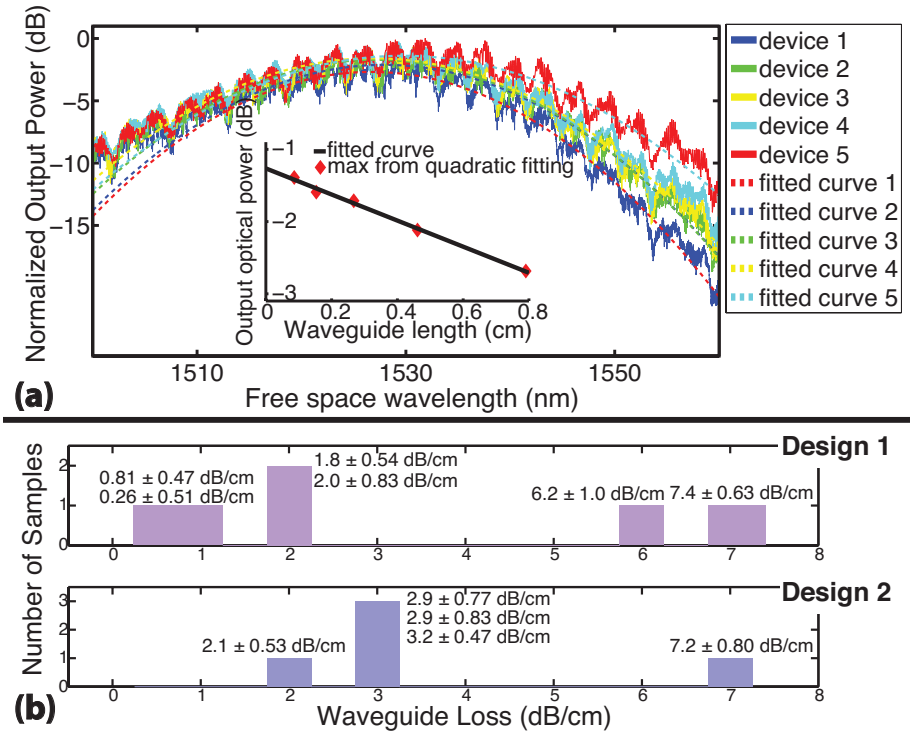



Figure 2.7: (a) Typical device spectra and linear regression of waveguide loss. The spectra of a group of five waveguide runouts of one sample obtained in one test. Quadratic fits are overlaid. The inset shows the linear regression of the peak optical output power extracted from the quadractic fits versus waveguide length. 1.8 ± 0.59 dB/cm was measured. (b) Histogram of waveguide losses for the two designs.

The $V_\pi L$ product of a polymer MZ modulator under push-pull operation is:

$$V_\pi L = \frac{\lambda_0}{4} \frac{1}{\gamma n_p^4 r_{33}} \tag{2.1}$$

where $\lambda_0$ is the wavelength in vacuum, $n_p$ is the polymer refractive index, and $r_{33}$ is electro-optic coefficient of interest. The geometric contribution due to the SWG is captured by the parameter $\gamma$. It therefore indicates how effective a strip-loaded SWG would be as part of an EO modulator. A symmetric strip-loaded SWG with a slot width of 140 nm typically has a $\gamma$ around 0.5–0.6 $\mu m^{-1}$. This value does decrease for the asymmetric design, and this drop is due to a decrease in modal overlap between the optical mode and the slot region. Fortunately, using narrower slots, as shown in Fig. 2.6(b), can significantly mitigate this effect. In any case, design 1 is predicted to exhibit a $\gamma$ value of 0.38 $\mu m^{-1}$.

Strip-loaded SWGs are geometrically compatible with the high-bandwidth traveling-wave Mach-Zehnder modulators proposed by Witzens et al. [16]. However, an important consideration is if a low series resistance from the electrodes to the slot can be achieved with a low optical loss [16]. Intuitively, better tradeoff between optical loss and series resistance of the waveguide implies better tradeoff between device speed, optical insertion loss (IL), and $V_\pi$. To show this for traveling-wave designs, we consider an IL-constrained design scenario. Assuming close RF and optical velocity match, we find that the EO response drops by 3 dB when $\alpha_{rf}(f_{3dB})L_{device} = 0.74$ Neper (i.e 6.4 dB), where the RF loss can be expressed as $\alpha_{rf} = 8\pi^2 f^2 C_{swg}^2 Z_0 G_{swg}^{-1}$. Here, $Z_0$ is the impedance of one driving transmission line loaded with one SWG, $C_{swg}$ is the slot capacitance per unit length, and $G_{swg}$ is the series conductance from both electrodes to the slot arms per unit slot length. Therefore

$$IL = \frac{0.4}{\pi^2 f_{-3dB}^2 C_{swg}^2 Z_0} G_{swg} \times loss(G_{swg}) \tag{2.2}$$

gives the appropriate choice of $G_{swg}$ for desired bandwidths and IL levels. The $loss(G_{swg}$ in the above equation can be optimized given certain flexibility in the doping profile, in that, for a given desired $G_{swg}$ the loss is minimized. Fig. 2.8 shows such optimization results for design 1 and its symmetric counterpart. Due to its compact mode as depicted in Fig. 2.6(c), asymmetric design exhibits substantially lower loss for a given $G_{swg}$. It is straightforward to show that a figure-$V_\pi$f-merit exists between modulation bandwidth and $V_\pi$ that depends

not on the device length but only on the cross-sectional design

$$FOM_{bandwidth-to-V_\pi} = \frac{f_{-3dB}^2}{V_{\pi,f=f_{3dB},push-pull}} = \frac{0.8}{\pi^2\lambda_0}\frac{n_p^4 r_{33}}{\epsilon_{p,rf}^2}\frac{w_{slot}^2\gamma}{h_{slot}^2\eta^2}\frac{G_{swg}}{Z_0} \tag{2.3}$$

where $\epsilon_{p,rf}$ is the permittivity of polymer in RF frequency, $n_p$ is the refractive index of the polymer at wavelength $\lambda_0$, and $w_{slot}$ and $h_{slot}$ are the width and height of the slot, respectively. $C_{swg} = \frac{\epsilon_{p,rf}h_{slot}}{w_{slot}}$ is used to account for the fact that $C_{swg}$ is not an ideal parallel capacitor. Since $G_{swg}$ appears in the numerator on the right-hand-side, the advantage in IL-to-$G_{swg}$ tradeoff directly translates into an improved bandwidth-to-$V_\pi$ figure-of-merit.

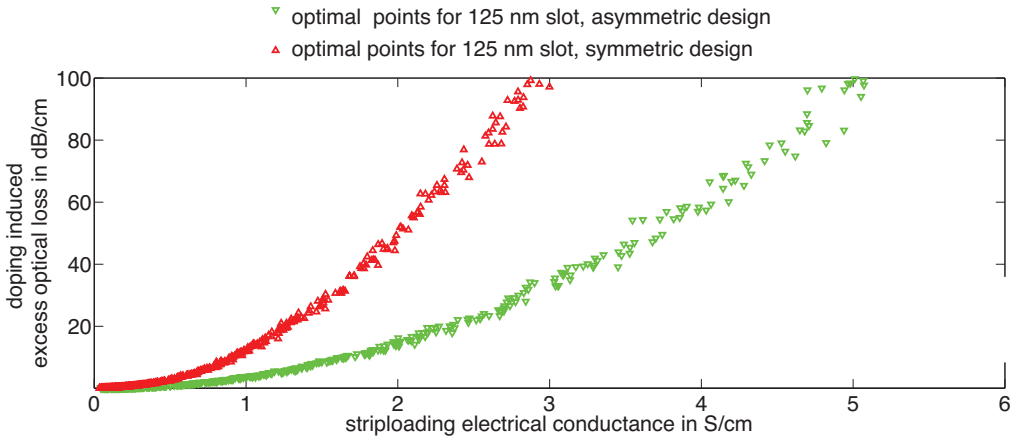



Figure 2.8: Numerical optimization of doping profile to achieve best IL vs. $G_{swg}$ tradeoff: three implant layers are assumed available with n-type doping levels ranging from $10^{16}$ $cm^{-3}$ to $10^{20}$ $cm^{-3}$. Metal to waveguide clearance is 2 $\mu m$.

In conclusion, the very low propagation losses and other benefits of the asymmetric strip-loaded SWGs suggest that they may play an important role in future low-loss, high-bandwidth and low-$V_\pi$ silicon-polymer hybrid EO modulators.

### *2.3 Silicon-polymer modulator at RF speed*

The silicon-polymer hybrid platform [10] offers great potential for a number of applications, including building low drive-voltage modulators and high-speed all-optical switches. Re-

cently, a slot-waveguide based silicon waveguide clad in an electro-optic polymer has been used to build a modulator with a $V_\pi$ of 0.25 V [14], approximately a 20-fold factor lower than that of a typical commercial modulator. However, the results have been obtained for slow speeds on the order of 1 kHz.

The configuration and SEM micrograph of the strip-loaded slot waveguide used in the device were shown in Fig. 2.9. A thin silicon strip, called a "strip-loading" region, is used to make electrical contact between the metal pad and each arm of the slot waveguide. In this specific device, the waveguide dimensions are 200 nm in silicon thickness, 300 nm in arm width, and 200 nm in slot width; and the modal pattern is near 1550 nm as shown in Fig. 2.9(a). A very conservative 10 $\mu$m metal-to-waveguide clearance was used to allow for fabrication error and to avoid excess optical loss. Using this waveguide geometry, we built the Mach-Zehnder modulator shown in Fig. 2.9(b).

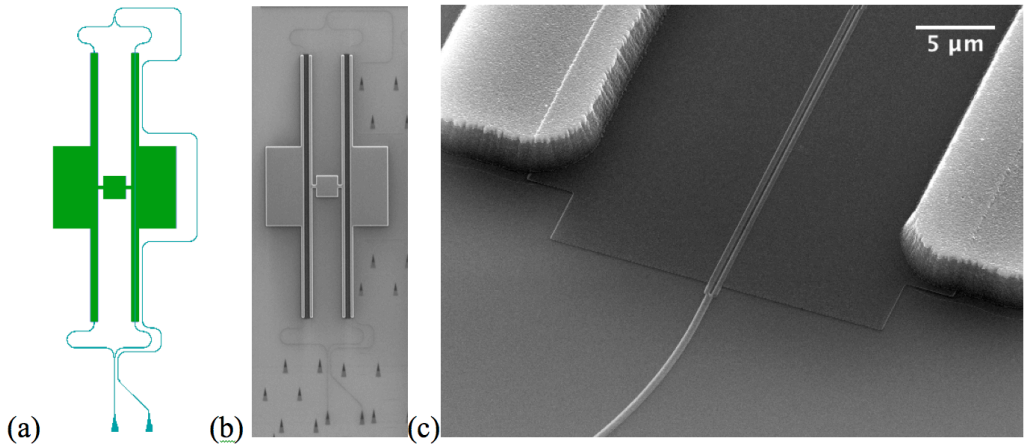



Figure 2.9: (a) Mach-Zehnder modulator layout; (b) SEM micrograph shows the fabricated device; (c) SEM micrograph of the layout of one arm shows the region where the ridge waveguide couples into the strip-loaded slot waveguide and metal pads sitting on strip-loading.

The AJSP-series electro-optic polymers are newly developed high-efficiency nonlinear optical materials, and their $r_{33}$ values range from 50 to 200 pm/V at telecommunication wavelengths [17]. AJSP100 exhibits relatively large electro-optic activity ($r_{33}$ value of 65

pm/V at 1550 nm), low optical loss (∼1 dB/cm), and good temporal and photochemical stability, and it is suitable for a broad spectrum of photonic applications. The electro-optic polymer cladding was prepared by doping AJSP100 into PMMA host. The resulting refractive index of the polymer was 1.54 at 1550 nm. A poling field of 100 V/$\mu$m and a poling temperature of 103 °C were used. During poling, the center pad was set to 0 V, the left pad was set to $+V_{pole}$ and the right pad was set to $-V_{pole}$, where $V_{pole} = 20$ V to achieve the poling field across a 200 nm slot. During modulation, the center pad was set to signal while the left and right pads were held at ground, so that the modulator was operated in a push-pull fashion.

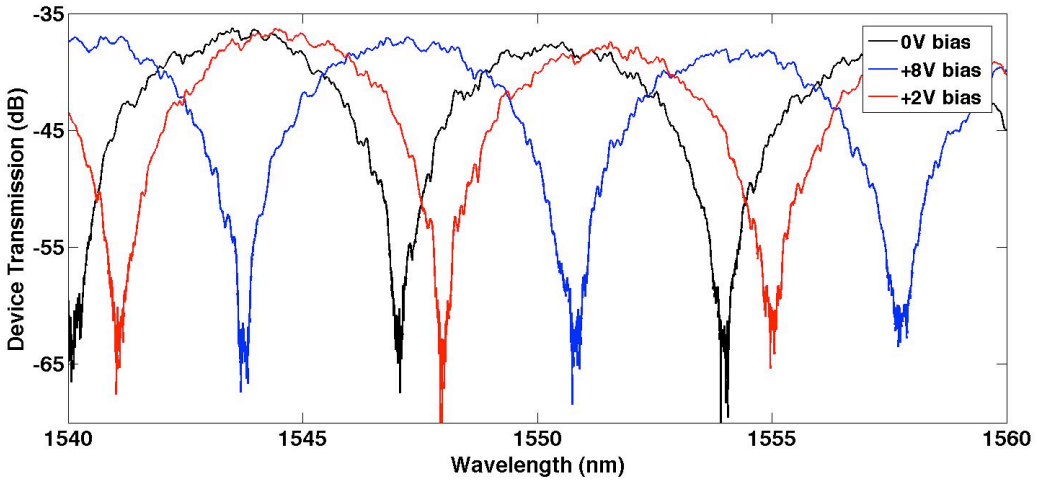



Figure 2.10: Transmission through the Mach-Zehnder device as a function of wavelength for various modulator drive voltages. As can be seen, a 2 V bias suggested the direction of spectrum shift, and an 8 V bias was slightly above $V_\pi$ voltage.

Fig. 2.10 shows the device transmission spectra for various DC drive voltages that were applied to the center pad of the device while the side pads were being held at ground. From the plots, the half-wave voltage $V_\pi$ can be roughly estimated at 8 V, a value that corresponds to a $V_\pi L$ of 0.8 V-cm. This suggests that an in-device poled $r_{33}$ of 40 pm/V was achieved.

The unbalanced Mach-Zehnder design allows us to bias the modulator at a $\pi/2$ bias point (that corresponds to 3 dB of extinction and a maximum response to a driving voltage) by

setting the signal wavelength to the appropriate value. The frequency response of the device was characterized from 200 Hz to 2 GHz. The results are shown in Fig. 2.11 as normalized S21. The corresponding normalized S21 of 8 $V_\pi$ is also plotted on the same axes. To allow direct comparisons across different measurements, the S21 measurement from each detector was also renormalized for the detector gain and the laser power level. Typical noise floors were at least 10 dB beneath the measurement, and were often substantially lower. The noise floor during the measurement with the high-speed detector is plotted in Fig. 2.11.

The spectrum of S21 showed a flatness that extended from DC to the gigahertz range, and an absolute value for S21 that corresponded very well with the value implied by 8 V $V_\pi$. The 6 dB rolloff point occurred at around 3 GHz. We note that our 6 dB rolloff in S21 corresponds to a 3 dB in the optical response that is typically defined to characterize modulator bandwidth as used by Liu et al [18].

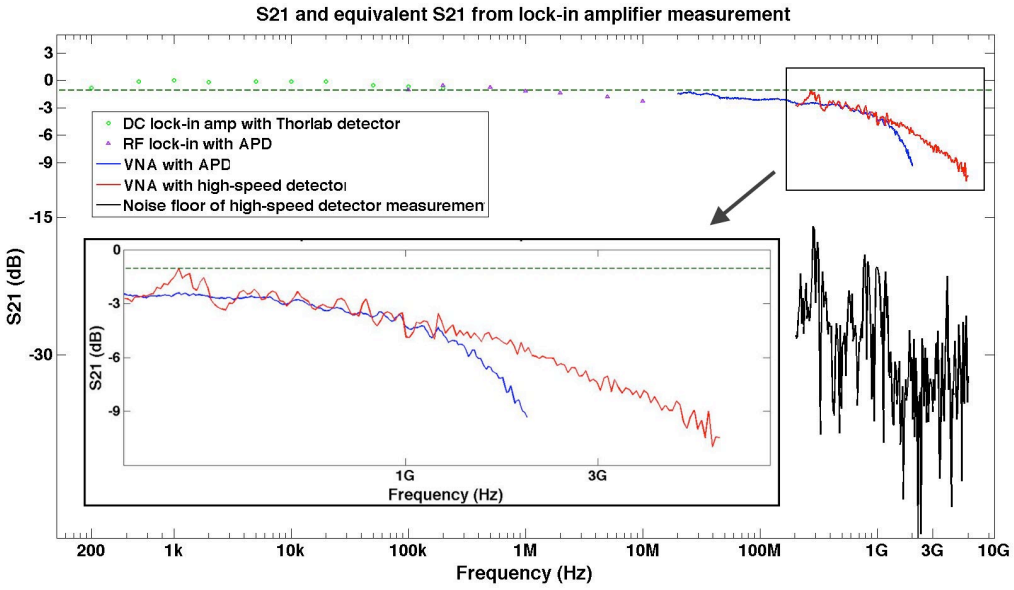



Figure 2.11: The frequency dependence of the device: 6 dB rolloff in S21 occurred around 3 GHz. The corresponding normalized S21 of 8 $V_\pi$ is plotted on the same axis. The inset graph shows the response from 200 MHz to 6 GHz, and the -6 dB rolloff appearing around 3 GHz.

If we assume the polymer has a RF dielectric constant of 4, then the capacitance of each arm can be estimated at 80 pF/m. Combining this with the arm resistance, which is roughly 70 Ω from each pad to the waveguide arm (assuming fully-charged surface states, and thus a 10nm silicon depletion region at this doping), one would expect to see a device bandwidth on the order of 15 GHz. However, our observed bandwidth was significantly lower than this predicted value. One possible source of this limitation could be a higher than expected resistance in the strip-loading section. Another possible source of the rolloff could be RF coupling to the substrate since the pads are large and the silicon substrate beneath the buried-oxide layer is not highly resistive.

### *2.4 Sub-volt Mach-Zehnder modulator*

The first silicon MZI modulator was based on carrier-depletion in a p-n structure, with a bandwidth around 1 GHz and a modulation figure of merit of 8 V-cm [18]. Improvements in design have led to silicon MZI modulators that exhibit modulation figures of merit of 4 V-cm at 30 GHz [19], and, more recently, of 1.4 V-cm at 12 GHz [20]. In the latter case, however, the authors identify a fundamental tradeoff between carrier concentration and modulator performance; their figure of merit can only be obtained with around 19 dB/cm of intrinsic absorption loss. Thus, it may not be possible to build a practical MZI modulator in silicon based on carrier depletion that has a halfwave voltage under 1 Volt. A similar limitation has been encountered with Lithium Niobate based modulators. At speeds near 20 GHz, halfwave voltages are typically near 2.7 V or higher. Even at speeds as low as 1 GHz, halfwave voltages are still over 1.2 V. Typical Lithium Niobate device lengths for these halfwave voltages are 5 cm or longer.

Here we demonstrate, for the first time, a silicon-organic modulator with a low absolute drive voltage at RF speeds. A 9 mm MZI modulator results in a halfwave voltage of 0.69 V with a bandwidth of 500 MHz; this corresponds to a modulator figure of merit of 0.62 V-cm. Fig. 2.12 and Fig. 2.13 show the geometry and mode pattern of this contacted strip-loaded slot waveguide.

We used a path length difference of 80 $\mu$m for the two MZI arms. This allowed the phase shift to be measured by device transmission, as shown in Section 3.1, and it enabled us to set

the MZI bias point by tuning the wavelength. The device dimensions were approximately 9 mm *times* 200 $\mu$m excluding contact pads, resulting in a total area of 1.8 $mm^2$. The device layout was driven by the need to manually probe between the waveguides, so we needed large pads. Considering only the metal leads and silicon waveguide and excluding the probe pads, the total area was 0.8 $mm^2$.

To characterize modulator performance at low speeds, we gathered optical transmission spectra at several different DC bias voltages. They showed a fringe spacing of around 6.9 nm due to the arm length imbalance. A balanced MZI could maximize the optical bandwidth and make the device athermal, however an unbalanced device made it possible to measure the $V_\pi$ by observing the transmission spectrum shift. Fig. 2.14 shows the device transmission spectra under two different bias voltages, as well as the phase shift deduced from the location of one of the peaks.

To measure the halfwave voltage with device transmission, we used the following methodology. To a constant factor, the transmission through an unbalanced MZI can be expressed as a function of wavelength as

$$\frac{1}{2}(1 + cos(\frac{2\pi}{\lambda}n(\lambda)\Delta L \pm \frac{\pi V}{V_\pi})) \tag{2.4}$$

where $\lambda$ is the wavelength, $n(\lambda)$ is the effective index which is generally a function of wavelength, $\Delta L$ is the length difference between the arms, V is the bias voltage, and $V_\pi$ is the halfwave voltage. The sign in front of the bias term is determined by the polarity of the device poling in combination with the sign of the $\chi^2_{xxx}$ tensor component, where $x$ in this case is the direction perpendicular to the direction of propagation, and parallel to the waveguide substrate. The argument to the cosine in Eq. 2.4 expands to first order in $\lambda$ as

$$\frac{2\pi\Delta L n(\lambda_0)}{\lambda_0} - \frac{2\pi(\lambda - \lambda_0}{\lambda_0}n_g\frac{\Delta L}{\lambda_0} \pm \frac{\pi V}{V_\pi} \tag{2.5}$$

where $\lambda_0$ for convenience is chosen to be a wavelength where, for no bias, the device has a minimum in transmission, and $n_g$ is the group index of the optical mode in the waveguide. This amounts to neglecting, among other things, group velocity dispersion. The minimum in the transmission spectra lies where Eq. 2.4 is equal to $\pi$ radians. Thus it is immediately clear that the shift in the location of a transmission minimum will have a linear relationship

with both the bias voltage and the induced phase shift. The phase shift can be expressed most conveniently in terms of the fringe-to-fringe spacing.

$$\pm\frac{\pi V}{V_\pi} = \Delta\phi = \frac{2\pi(\lambda-\lambda_0}{\lambda_0} n_g \frac{\Delta L}{\lambda_0} = \frac{2\pi}{\Delta\lambda}(\lambda-\lambda_0) \tag{2.6}$$

To determine the location of a minimum in the transmission spectra, we selected the very lowest power level in a given region, and then averaged all points within 3 dB of this level. The variance of this distribution was then used as an uncertainty in the measurement. A halfwave voltage of 0.69 ± 0.04V was derived as the average of the two measurement sets. Combining this voltage value with a modulation figure of merit $\gamma$ (defined in [15]) for the waveguide of 0.21 $\mu m^{-1}$ suggests an $r_{33}$ value for the poled polymer of around 54 pm/V. This is slightly lower than the peak performance found in material of 65 pm/V, a relationship that we confirmed by measuring a single layer film on ITO.

To characterize the device at RF speeds, we connected the output from the device to a New Focus 1647 avalanche photodetector with 1 GHz bandwidth. S-parameters S21 and S11 were taken with an Agilent E8361C network analyzer. The wavelength was chosen to bias the device at the 3 dB point. Fig. 2.15 shows the predicted S21 value for the DC halfwave voltage and the measured S21 values. The modulation bandwidth, typically defined as the 6 dB point for an RF S21 [18], is around 500 MHz. It was measured with -10 dBm RF power to ensure that the modulator remained in the linear regime.

The observed bandwidth limitation is almost certainly not due to the electro-optic polymer since similar polymers have shown bandwidths of 165 GHz [21]. The limitation is also not caused by carrier transit times since silicon acts only as a transparent conductor. Instead, it is due to RF parasitics. The equivalent circuit for both arms of the device is shown in Fig. 2.15(c). The resistance due to the strip-loaded arms, $R_{sl}$, should be around 8 Ω. A finite element simulation predicts a $C_{sl}$ of approximately 1.8 pF. $C_s$ should be 3.1 pF, while $R_s$ can be calculated as 6 Ω.

Here, there are four effects that can limit device bandwidth. First, at sufficiently high frequencies, 9 mm will no longer be a small fraction of the wavelength, so distributed effects will likely be a limitation. However, at 1 GHz, 9 mm is still under 1/20 of the wavelength, even in a dielectric material, so this is less likely to be an issue here. Second, the capacitive

loading itself could become a limitation. At 1 GHz, the absolute value of the impedance of the two $C_{sl}$ capacitors is around 44 Ω, so even at 500 MHz, this effect is likely a limitation. Third, if $R_{sl}$ were sufficiently large, then an RC time constant between $R_{sl}$ and $C_{sl}$ would limit the bandwidth. And finally, $R_s$ has the potential to short circuit the modulator as the impedance across Cs drops at higher speeds.

We believe that the three latter effects all play a role. Using the previously calculated values for the components in Fig. 2.15(c), a 6dB rolloff in S21 should be at 780 MHz. However the S11 would only be -0.8 dB in this case (Fig. 2.15(b). It is most likely that $R_{sl}$ is larger than anticipated. At 75 Ω, a 6dB rolloff at around 500 MHz is predicted with an S11 value of -3 dB, in agreement with the experimental data.

In conclusion, we have demonstrated a MZI modulator with a sub-1V halfwave voltage at the RF bandwidth. To our knowledge, this is the lowest halfwave voltage shown for any silicon-based MZI, and it appears to be the lowest halfwave voltage shown in any material system for an RF electro-optic MZI modulator. Moreover, we have revealed a clear path towards improved performance from the standpoints of both better RF design and more active polymers. With polymers that have been demonstrated with $r_{33}$ values of 300 pm/V could be used in our device to give a halfwave voltage of 120 mV. We believe that slot-waveguide polymer modulators will play an important role in future silicon photonic systems.

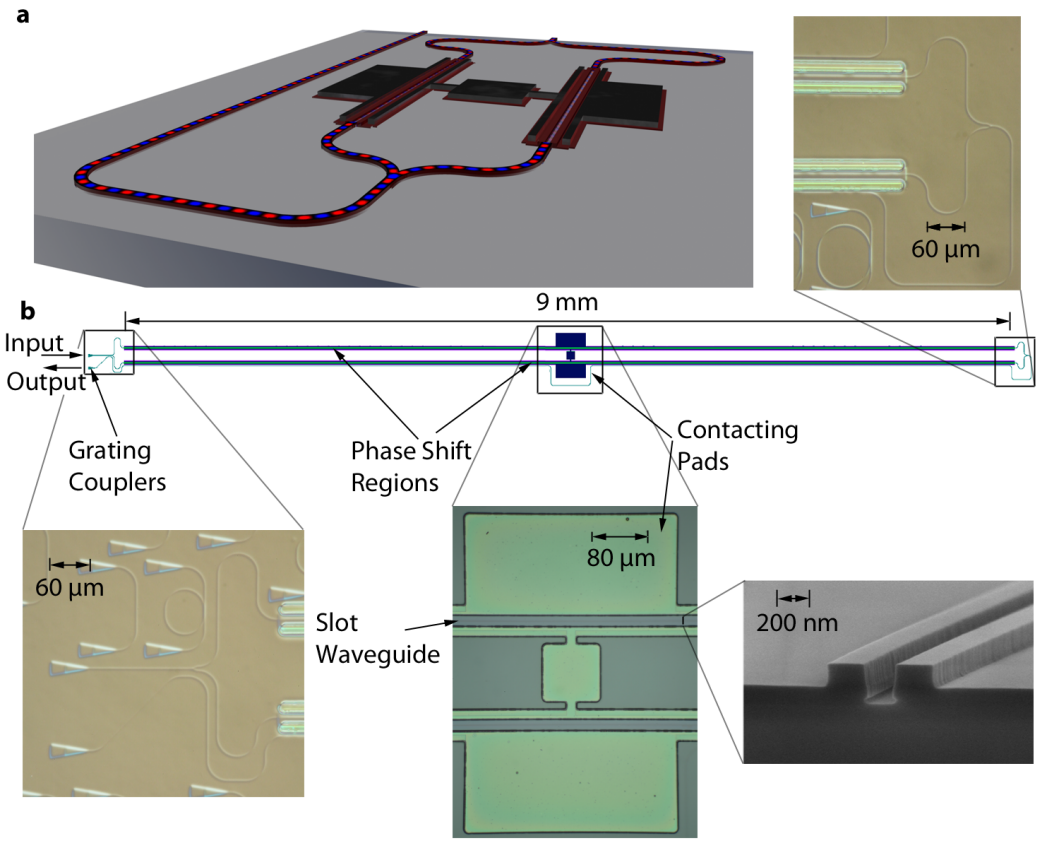



Figure 2.12: Device Layout: (a) A rendering of a portion of the MZI illustrates the optical path. (b) The layout of the device is shown. Note that, after traveling through the MZI, the optical signal returns back to the side of the MZI in a ridge waveguide. Optical micrographs and an SEM micrograph of key features are also displayed. We note that in two of the optical micrographs, portions of adjacent, unrelated devices are also apparent.

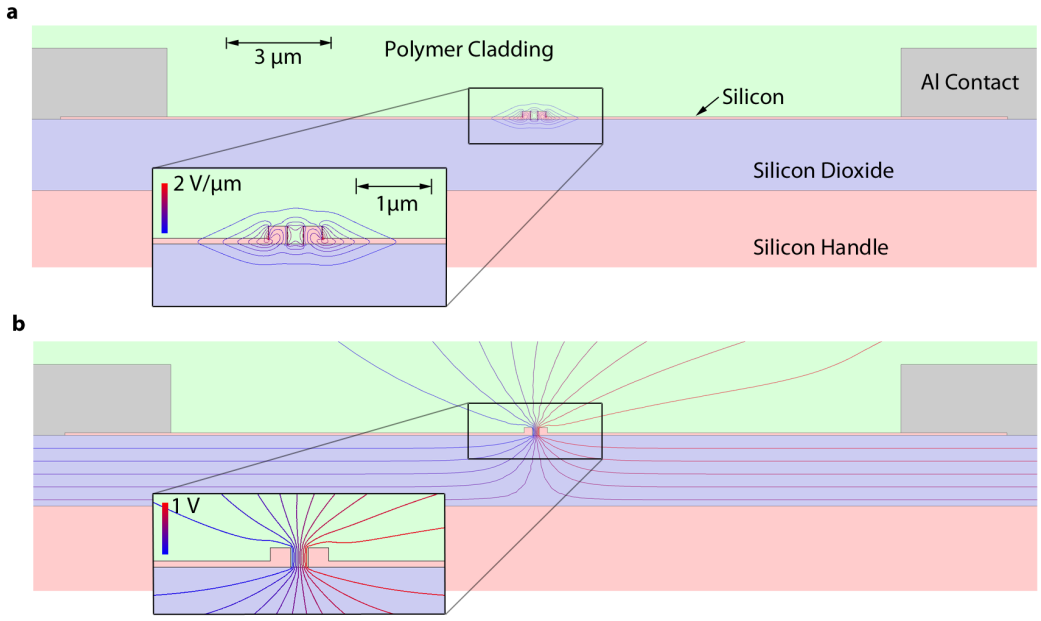



Figure 2.13: Device Cross-section Layout and Modal Structure: (a) The contacted strip-loaded slot structure and the optical mode are illustrated. A contour plot of $|E_x|$ is shown, normalized for 1 mW of propagating power. (b) The RF mode is shown, with a contour plot of the voltage that would be seen at high frequencies, but below the bandwidth limit.

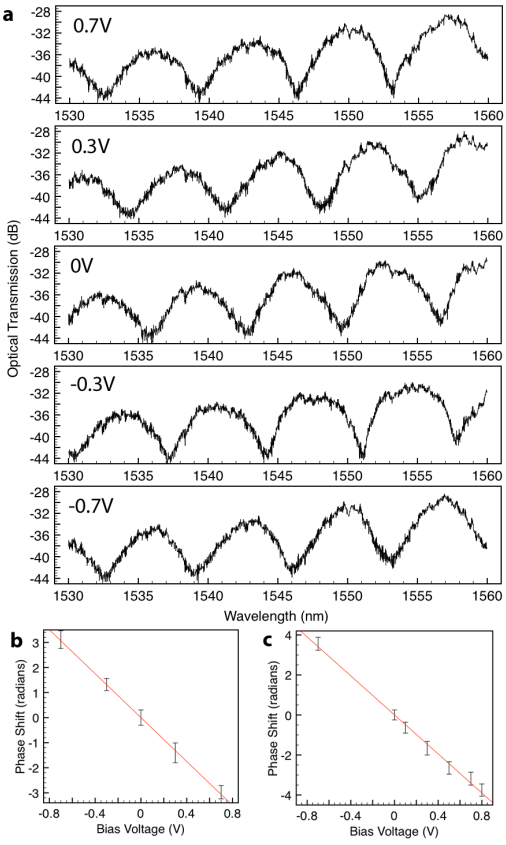



Figure 2.14: DC device performance: (a) Device transmission spectra excluding off-chip coupling losses as a function of wavelength is shown for several bias voltages. (b) and (c), Plots of phase shift (in radians) as a function of bias voltage for two different measurement sets, determined by the migration of the minimum near 1550 nm as a function of bias voltage. The slopes indicate halfwave voltages of 0.72 $\pm$ 0.06 V and 0.65 $\pm$ 0.03 V, respectively. The device transmission plots correspond to the data points of the first measurement set.

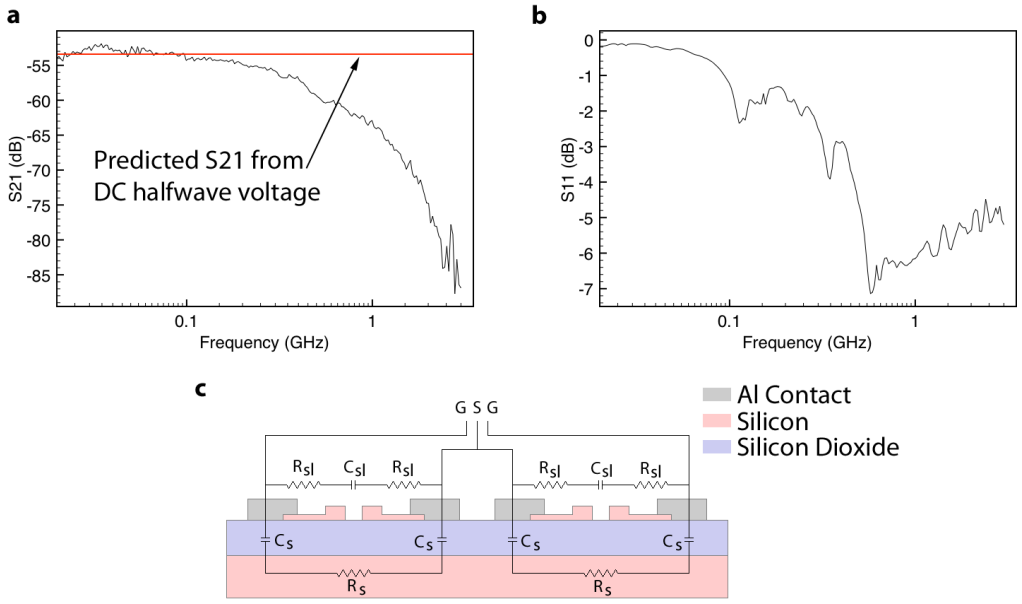



Figure 2.15: RF performance and source of bandwidth limit. (a) The measured S21 parameter is shown as a function of frequency, along with the predicted value from the DC results that is based on the known losses of the system and the photodetector conversion gain. (b) The S11 parameter is shown, with a 3 dB rolloff at around 500 MHz. (c) A rendering of the equivalent circuit of the device.

# Chapter 3

# SILICON PN-JUNCTION MODULATORS

This presents my work in all-silicon modulator using plasma dispersion effect. With this effect, the change of carrier concentration in silicon alters the refractive index of silicon. If this index change occurs in an optical waveguide, light can be modulated. The typical device configuration is thus a lateral or vertical pn junction overlapped with an optical waveguide. However, plasma dispersion here is still a relatively weak effect. Modulation voltage at high speed is usually much higher than what would be compatible with advanced CMOS core transistors [22]. To lower the drive voltage and build practical modulator device two approaches are taken. One is to take advantages of resonance structures (such as ring resonators), where small phase-shift translates into large optical modulation amplitude. But this is usually at the cost of the device being sensitive to temperature and fabrication variations. The other approach is to incorporate traveling-wave design so that long (several millimeters) Mach-Zehnder devices can work properly at high speed. Both of these approaches will be discussed in this chapter, with several related results presented.

## *3.1 Operation principles of pn junction modulators in silicon*

Near-infrared wavelength range plasma dispersion effect in silicon was originally studied by Richard Soref [9] and remains the main mechanism people use to build silicon modulators. In this effect, the carrier concentration change in silicon result in the change of both real and imaginary part of the refractive index. The relationship at wavelength of 1550nm is can be fitted to a dual log curve based on Soref's data. The widely accepted formula is:

$$\begin{aligned} \Delta n = \Delta n_e + \Delta n_h = -8.8 \times 10^{-22} \times \Delta N_e - 8.5 \times 10^{-18} \times (\Delta N_h)^{0.8} \\ \Delta \alpha = \Delta \alpha_e + \Delta \alpha_h = 8.5 \times 10^{-18} \times \Delta N_e + 6.0 \times 10^{-18} \times \Delta N_h \end{aligned} \tag{3.1}$$

The phase velocity of an optical mode is characterized by effective index. The above equation directly links carrier concentration to index change of the material, but one also needs

another equation that shows how the material index change translates into the perturbation of the effective index of an optical mode.

A propagation mode can always be expressed as:

$$\begin{pmatrix} E \\ H \end{pmatrix} = \begin{pmatrix} E_m^*(x,y,\omega) \\ H_m^*(x,y,\omega \end{pmatrix} \exp(-in_{eff}(\omega)\frac{\omega}{c}z - i\omega t) \tag{3.2}$$

Plugging this into Maxwell's equations we can get:

$$\begin{aligned} &\begin{pmatrix} i\omega\epsilon_0\epsilon(x,y) & 0 & 0 & 0 & 0 & \partial_y \\ 0 & i\omega\epsilon_0\epsilon(x,y) & 0 & 0 & 0 & -\partial_x \\ 0 & 0 & i\omega\epsilon_0\epsilon(x,y) & -\partial_y & \partial_x & 0 \\ 0 & 0 & -\partial_y & i\omega\mu_0 & 0 & 0 \\ 0 & 0 & \partial_x & 0 & i\omega\mu_0 & 0 \\ \partial_y & -\partial_x & 0 & 0 & 0 & i\omega\mu_0 \end{pmatrix} \begin{pmatrix} E_x \\ E_y \\ E_x \\ H_x \\ H_y \\ H_z \end{pmatrix} \\ &= i\beta \begin{pmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} E_x \\ E_y \\ E_x \\ H_x \\ H_y \\ H_z \end{pmatrix} \end{aligned} \tag{3.3}$$

or, in short:

$$H\psi = i\beta A\psi \tag{3.4}$$

This takes the form of generalized eigen-value problem, for which we have:

$$\beta = \frac{1}{i}\frac{\Psi^t H \Psi}{\Psi^t A \Psi} \tag{3.5}$$

Consider the perturbation in $\epsilon$ as $\Delta\epsilon$, so that $H$ becomes $H = H + \Delta H$, where

$$\Delta H = \begin{pmatrix} i\omega\epsilon_0\Delta\epsilon(x,y) & 0 & 0 & 0 & 0 & 0 \\ 0 & i\omega\epsilon_0\Delta\epsilon(x,y) & 0 & 0 & 0 & 0 \\ 0 & 0 & i\omega\epsilon_0\Delta\epsilon(x,y) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \tag{3.6}$$

Thus we have

$$\beta + \Delta\beta = \frac{1}{i}\frac{(\Psi + \Delta\Psi)^t(H + \Delta H)(\Psi + \Delta\Psi)}{(\Psi + \Delta\Psi)^t A(\Psi + \Delta\Psi)} \tag{3.7}$$

Assume that $\Delta\Psi = a\Psi + b\Psi_\perp$, where a and b are small numbers, it follows

$$\begin{aligned} \Delta\beta &\approx \frac{1}{i}\frac{\Psi^t\Delta H\Psi}{(1+2a)\Psi^t A\Psi} \\ &\approx \frac{\Psi^t\Delta H\Psi}{\Psi^t A\Psi} \end{aligned} \tag{3.8}$$

i.e.

$$\begin{aligned} \delta n_{eff} &\approx \delta\beta\frac{c_0}{\omega} \\ &\approx \frac{1}{i}\frac{\Psi^t\Delta H\Psi}{\Psi^t A\Psi} \end{aligned} \tag{3.9}$$

The last equation is of particular importance, because it shows given the modal profile ($\Psi$) and index change ($\Delta H$), we can calculate the effective index change by the generalized Rayleigh quotient, which we call optical modal overlap integral. To make is explicit, we have:

$$\begin{aligned} \frac{\delta n_{eff}}{n_{eff}} &= 2n_{si}\frac{\mathrm{d}n_{eff}}{\mathrm{d}\epsilon_{eff}} \\ &= \frac{2n_{si}\oint_{R1}|E|^2\,\mathrm{d}S}{\sqrt{\frac{\mu_0}{\epsilon_0}}\oint_{R2}(E_xH_y^* - E_yH_x^* + E_x^*H_y - E_y^*H_x)\,\mathrm{d}S} \\ &= \frac{2n_{si}}{Z_0}\frac{\oint_{R1}|E|^2\,\mathrm{d}S}{2\oint_{R2}\mathrm{Re}[E_x^*H_y - E_y^*H_x]\,\mathrm{d}S} \end{aligned} \tag{3.10}$$

R1 is the region of where the change of permittivity occurs. R2 is the full domain of the optical mode. Therefore

$$\Delta n_{eff} = \frac{2n_{si}}{Z_0} \frac{\oint_{R2} |E|^2 \Delta \mathrm{n_{si}}(x,y)\,\mathrm{d}S}{2\oint_{R2} \mathrm{Re}[E_x^* H_y - E_y^* H_x]\,\mathrm{d}S} \tag{3.11}$$

is thus calculated from carrier density. $E_x$, $E_y$, $H_x$, $H_y$ should be the complex field from a mode solver.

Given that the carrier concentration can change the effective index of an optical mode, the next question is how to create a situation in optical waveguide that the carrier concentration can be changed by an electrical signal, such as voltage, so that electro-optic modulation can be achieved.

Several difference configurations are possible. The first multi-Gb/s silicon modulator [18] uses MOS capacitor working in accumulation mode and achieve high-speed because the carrier is supplied by the source and drain reservoir rather than thermally generated which would be limited by slow lifetime. However, this device configuration suffers from high optical loss due to the use of poly silicon gate contact, which is heavily doped. Also, MOS capacitor is a relatively complicated device to fabricate on to a waveguide.

Currently, the most popular device configuration is pn junction. Because in addition in the process layers necessary to create a waveguide, only a few implant mask layers are needed to create pn junctions in the waveguide. Semiconductor process and device simulation can accurately simulate the doping concentration versus voltage given the implant recipe and annealing conditions. Then the modal overlap procedure discussed in the previous section can be executed numerically to determine the modulation efficiency, insertion loss and other important properties of the junction and device. Below is a graph from Sentaurus semiconductor simulation environment, showing a simulated waveguide with pn junction built.

The junction is operated in revers-biased mode, because forward biased junctions suffer from slow carrier lifetime that prevents them from achieving high-speed modulation. The modulation efficiency is quantified as $V_\pi L$, usually in V-cm. In silicon, the best achieved number is 1.2 V-cm, meaning in order to achieve a full $\pi$ shift on a 1-cm long waveguide,

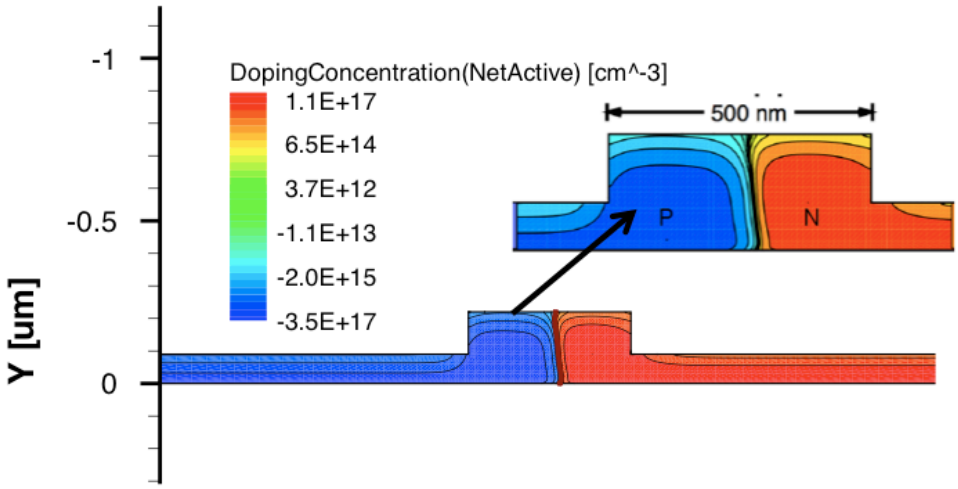



Figure 3.1: Sentaurus simulation of the dopant concentration in a typical waveguide pn junction shifter

one need to apply 1.2 V voltage, for a 1-mm long device, 12 V is required! For high frequency operation, the maximum device is limited by the RF wavelength in addition to device footprint limitations. So, one need to either use compact device in order for it to be considered as a lumped element at high frequency, but this makes the modulation voltage high. Alternatively, one could utilize traveling-wave design, such that although it is an electrically large device, the bandwidth is not limited by device size.

### *3.2 Traveling-wave Mach-Zehnder modulators RF design*

Silicon optical modulator [22] has been one of the centerpieces in silicon photonics, especially for data communication related applications [6, 23–25]. Over the past decade, significant progress has been made in this area, but achieving efficient high-speed modulation in silicon still proves to be challenging, mainly due to the weak electro-optic (EO) effects available in this material [9].

The fundamental and key modulator device metrics include insertion loss, device bandwidth, and EO modulation efficiency (for Mach-Zehnder modulators the efficiency is char-

acterized by $V_\pi$). In addition, optical bandwidth, device footprint, temperature sensitivity, fabrication error tolerance and CMOS compatibility are also of great importance for practical designs, design scalability and possibility of CMOS monolithic integration [26, 27].

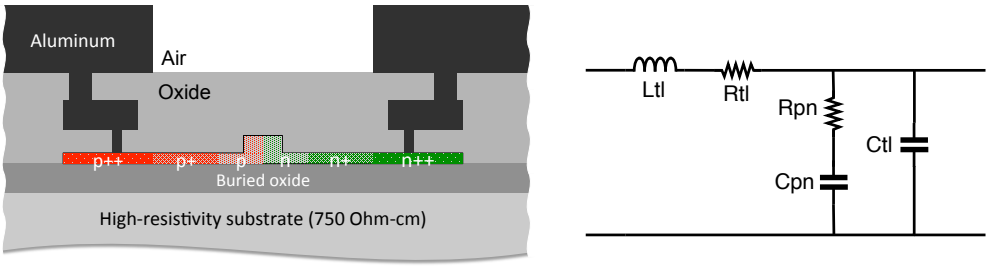
A majority of the high-speed demonstrations so far were based on reverse-biased silicon pn junctions. Among these results, high-speed resonator modulators are promising in achieving ultra-low modulation power consumption and compact device footprint. Recently, Li et al demonstrated a 40-Gb/s 1V-drive ring modulator [19], although issues such as limited optical bandwidth, and consequently necessary thermal drift stabilization, as well as operating wavelength alignment between devices remain to be fully addressed.

The other main category of carrier-depletion pn junction modulators is traveling-wave Mach-Zehnder (TWMZ) modulators. Although in academic demonstrations imbalanced Mach-Zehnder (MZ) modulators are often used (mostly for the convenience of testing), balanced MZ modulators are the true practical devices and have the key advantage of being temperature insensitive, thus do not require active thermal stabilization. Traveling-wave design enables the driving of a long phase-shifter at high speed, therefore can yield low voltage modulators.

In this section, I present a 3-mm long, 30-GHz bandwidth differential-drive silicon TWMZ modulator based on a lateral pn junction with low reverse bias. The phase shifter $V_\pi L_\pi$ is 2.7 V-cm (a small-signal $V_\pi$ of 9 V) and the insertion loss on the phase shifter is only 3.6 dB.

### *3.2.1 Fabrication process*

The device presented in this work was fabricated at the Institute of Microelectronics (IME) in Singapore [11] through an OpSIS Multi-Project Wafer (MPW) run. The fabrication process was very similar to that in [28] with the main difference being that in this work we employed six implant layers instead of four in silicon, and they were: lightly doped P and N for forming the junction in the waveguide core, intermediate density P+ and N+ for reducing series resistance without inducing excessive optical loss, and heavily doped P++ and N++ implant for low resistance silicon far away from the waveguide and for forming




(a) Cross-section diagram (b) Equivalent circuit model

Figure 3.2: Typical cross-section of a traveling-wave pn junction phase shifter

low resistance metal-to-silicon contact - no silicidation was used in the fabrication process, the contact was formed directly between aluminum heavily doped silicon. The traveling-wave phase shifter cross-section is illustrated in Fig. 3.2(a) and the microscope photo of the fabricated device is shown in Fig. 3.3(b). The wafer was an 8-inch Silicon-on-Insulator (SOI) from SOITEC with 220 nm top silicon, 2 $\mu$m buried oxide layer and 750 Ω-cm high resistive silicon substrate. The silicon slab thickness was 90nm and ridge waveguide width was 500 nm. The top metal Aluminum was used for the traveling-wave electrodes, and it was 2 $\mu$m thick, mostly situated above dielectric materials in the back-end stack. Other metal and dielectric material properties and thicknesses as well as fabrication steps were identical as they were in [28].

### *3.2.2 Overall device design considerations*

The cross-section of the TWMZ shown in Fig. 3.2(a) is considered as a pn junction loaded transmission line and its equivalent circuit model is schematized in Fig. 3.2(b). $R_{tl}(f)$ is the frequency-dependent metal skin resistance in Ω/m, and has a $\sqrt{f}$ dependence in principle, $C_{tl}$ and $L_{tl}$ are the capacitance and inductance between the metal traces in the units of F/m and H/m respectively. $C_{pn}$ is the pn junction capacitance (in F/m); the total amount of silicon series resistance from the electrodes to the edges of the junction depletion region is captured in $R_{pn}$ (in Ω-m). We further define the junction intrinsic RC bandwidth as

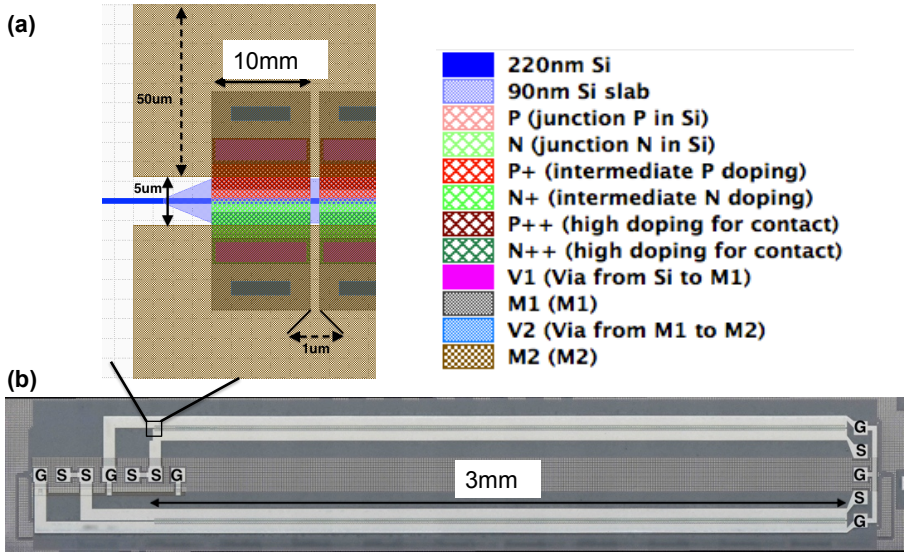



Figure 3.3: (a) RF layout dimensions (b) Device microscope photograph

$f_{rc} = \frac{1}{2\pi RC}$ and approximate the device impedance with $Z_{dev} = \sqrt{\frac{L_{tl}}{C_{tl}+C_{pn}}}$ which is accurate when the frequency is well below the intrinsic RC bandwidth, i.e. $(f/f_{rc}) \ll 1$. It is worth nothing that, due to the use the high-resistivity substrate, the substrate conductance due to transverse current flow can be neglected in the frequency range of interest.

The bandwidth of a TWMZ modulator is mostly determined by the RF loss due to $R_{pn}$, if RF and optical velocities are closely matched. To make this clear we can look at the overall RF field loss coefficient (in the unit of Neper/m), which can be expressed as [29]:

$$\begin{aligned} \alpha &= \alpha_{metal} + \alpha_{silicon} \\ &\approx \frac{1}{2}\frac{R_{tl}(f)}{Z_{dev}} + \frac{2\pi^2 f^2 R_{pn} C_{pn}^2 Z_{dev}}{1+\left(\frac{f}{f_{rc}}\right)^2} \\ &= \frac{1}{2}\frac{R_{tl}(f)}{Z_{dev}} + \frac{\pi f^2 C_{pn} Z_{dev}}{f_{rc}\left(1+\left(\frac{f}{f_{rc}}\right)^2\right)} \end{aligned} \tag{3.12}$$

where $\alpha_{metal}$ and $\alpha_{silicon}$ are the loss due to metal series resistance and lateral silicon resistance respectively. Let us refer to the first term as $R_{tl}$ loss and the second term as $R_{pn}$ loss. At high frequencies, the second term usually dominates because of its $f^2$ dependence,

whereas $R_{tl}(f)$ has a $\sqrt{f}$ dependence. Incidentally, this can be seen clearly in Fig. 3.4(g), a simulation plot of the actual device under discussion.

For the moment, let us assume perfect velocity match and neglect other non-ideal RF effects (such as reflection, multi-modal behavior and etc.), a straightforward relation between EO 3dB bandwidth $f_{EO,3dB}$ and achievable device length $L_{dev}$ can be derived as [30]:

$$\begin{aligned} \frac{1-\exp\left(-\alpha\left(f_{EO,3dB}\right)L_{dev}\right)}{\alpha\left(f_{EO,3dB}\right)L_{dev}} &= \frac{1}{\sqrt{2}} \\ \Rightarrow \alpha\left(f_{EO,3dB}\right)L_{dev} &\approx 0.74\,\text{Neper} = 6.4\,\text{dB} \end{aligned} \tag{3.13}$$

This is the "6-dB" rule-of-thumb frequently referred to in publications about TWMZ, i.e. the RF 6-dB bandwidth (more accurately 6.4-dB) is close to the EO response 3-dB bandwidth.

For the sake of simplicity let us further assume the desired bandwidth $f_{EO,3dB}$ is sufficiently low compared to the intrinsic RC bandwidth of the junction so that $(f/f_{rc}) \ll 1$. Usually the TWMZ design is in the "low loss" regime of the transmission line model where this assumption naturally stands. Inserting Eq. 3.12 into Eq. 3.13, and we get

$$\begin{aligned} L_{dev} &= \frac{0.74}{\frac{1}{2}\frac{R_{metal}(f_{EO,3dB})}{Z_{dev}} + 2\pi^2 f_{EO,3dB}^2 R_{pn} C_{pn}^2 Z_{dev}} \\ &\approx \frac{0.74}{2\pi^2 f_{EO,3dB}^2 Z_{dev}} \frac{1}{R_{pn}C_{pn}^2} \\ &= \frac{0.74}{\pi f_{EO,3dB}^2 Z_{dev}} \frac{f_{rc}}{C_{pn}} \end{aligned} \tag{3.14}$$

The approximation before arriving at Eq. 3.14 is based on that $R_{pn}$ loss is much larger than $R_{tl}$ loss at frequencies near $f_{EO,3dB}$.

A few scaling trends can be derived from Eq. 3.14, which quantify the tradeoffs in the seemingly complicated design space:

(I) It becomes apparent that getting low $V_\pi$ at high frequency is increasingly difficult, since $L_{dev} \propto \frac{1}{f_{EO,3dB}^2}$, consequently $V_\pi \approx (V_\pi L_\pi)/L_{dev} \propto f_{EO,3dB}^2$.

(II) In general, to design for certain impedance and bandwidth the achievable device length $L_{dev}$ and $V_\pi$ have the following scaling trends with respect to pn junction parameters:

$$L_{dev} \propto \frac{1}{R_{pn}C_{pn}^2},\ V_\pi \propto (V_\pi L_\pi) R_{pn} C_{pn}^2 \tag{3.15}$$

Obviously, a reduction in $R_{pn}$ is directly reflected in a reduction in $V_\pi$ (for certain bandwidth design target). Highlighted in Eq. 3.15 is another key point. In an attempt to improve junction modulation efficiency (reducing $V_\pi L_\pi$) the factor $(V_\pi L_\pi) R_{pn} C_{pn}^2$ should be evaluated. A reduction in $V_\pi L_\pi$ is likely to come at the cost of increased $C_{pn}$. An increase in $(V_\pi L_\pi) R_{pn} C_{pn}^2$ implies that the reduction in $V_\pi L_\pi$ does not ultimately lead to the reduction of the device . Therefore, a low doped, low capacitance density junction could be a more advantageous for traveling-wave design, which is the case of the design reported in this paper.

(III) Designing at lower device impedance is advantageous, because $L_{dev} \propto \frac{1}{Z_{dev}}$, $V_\pi \propto Z_{dev}$, holding junction parameters constant. Note that the impedance $Z_{dev}$ is not the termination impedance but the RF impedance of device itself. The effect of termination impedance on device performance will be addressed in later sections. Assuming the device is in fact terminated with $Z_{dev}$, we can then conveniently evaluate the drawback of using low impedance design, which is mainly some loss of the incoming drive voltage, if the driver is at impedance $Z_0$ that is higher than $Z_{dev}$. The ratio of voltage dropped on the device ($V_{dev}$) versus the driver output voltage ($V_0$) is $\frac{V_{dev}}{V_0} = \frac{2Z_{dev}}{Z_{dev}+Z_0}$. For example, this voltage-intake factor is 67 % for a 25 Ω device terminated with 25 Ω driven by a 50 Ω driver. However, the achievable device length at 25 Ω is approximately twice as it would be for a 50 Ω design based on Eq. 3.14, therefore overall the 25 Ω design would be more advantageous. The device length doubling is of course a rough estimate, due to the omission of metal loss, which could be significant if target impedance is extremely low.

### *3.2.3 PN junction design*

The waveguide pn junction phase shifter is the core component of an MZ modulator; its metrics largely determine the achievable overall device performance, as shown in Eq. 3.14 and Eq. 3.15. In addition to providing a low factor, the pn junction design also needs to achieve low optical insertion loss.

We chose lightly doped P and N to form the junction in the waveguide with the P side average doping concentration being around 5e17/cm3 and N side being close to 3e17/cm3.

The junction line was designed to be at the center of the waveguide, with no intentionally added intrinsic region width. This low-doped pn junction is in favor of the efficiency versus loss tradeoff, characterized by the figure-of-merit FdB-V (in dB*V) as defined in [22,23]. Also, it helped achieve a low by maintaining a low and competitive .

To achieve a low $L_{dev} \propto \frac{1}{Z_{dev}}$, $V_\pi \propto Z_{dev}$ with low loss, we employed a 3-level side-doping configuration as illustrated in Fig. 3.2, with carefully chosen doping density and doping profile. We selected P+ and N+ doping density of 2e18 $cm^{-3}$ and 3e18 $cm^{-3}$ respectively and optimized the doping profile. The onset of doping to the edge of the waveguide is defined as "clearance". The clearance of P+ and N+ doping were 120 nm and 140 nm respectively. The P++ and N++ doping were on the level of 1e20 $cm^{-3}$ and their clearance were both 950 nm and the doped region extended laterally until they reached the electrode contact regions that were 3.95 $\mu$m away from the edge of the waveguide. A breakdown of optical loss and resistance of the various regions is presented in table below.

Table 3.1: Simulated optical loss and resistance breakdown

| N & P doped wg core | | N & P doped slab region | | N+ doped slab region | |
|---|---|---|---|---|---|
| R | IL | R | IL | R | IL |
| 1.5 | 6.8 | 1.6 | NA | 1.1 | 0.97 |
| P+ doped slab region | | N++ & P++ doped region | | Total | |
| R | IL | R | IL | R | IL |
| 2.5 | 0.53 | 0.49 | 0.01 | 7.2 | 8.3 |

Notes: "R" denotes resistance in Ω-mm, "IL" denotes insertion loss in dB/cm. The IL reported for waveguide core includes the loss of N and P doped slab region due to simulation setting. IL numbers only include free carrier absorption loss at 0 V bias, and do not include intrinsic waveguide loss.

Based on implantation process modeling and device simulation, $C_{pn}$ was 280 pF/m at 0 V and 220 pF/m at -1 V bias, thus $f_{rc}$ at -1V bias reached 100 GHz. The simulated

small-signal $V_\pi L_\pi$ was 1.7 V-cm at -1 V bias.

### *3.2.4 Traveling-wave electrode design*

In light of the observation (III) discussed previously, we continued to use a 33–37 Ω impedance design similar to [28] instead of designing at 50 Ω. This is also a convenient impedance to design with our junction capacitance $C_{pn}$ while achieving velocity matching condition and low RF loss. Another consideration was that if the device were properly terminated with matching impedance, this device would still provide an acceptable S11 (< -10 dB), when tested in 50 Ω environment or integrated with 50 Ω drivers.

However, we do not deem it a fundamental requirement to comply with 50 Ω standard RF interfaces, because eventually and especially for on-chip applications the TWMZ devices are likely be closely integrated with custom drivers, in which cases the short length (or even zero length) electrical connection as well as the availability of custom designed low impedance drivers would make it possible to freely choose any impedance as long as it advances the overall device and system performance. For example, numerous laser drivers have been designed at very low impedances [31] for efficient driving.

The device layout and microscopic photograph is shown in Fig. 3.3. We used a Ground-Signal (GS) coplanar transmission line electrode to drive each arm. The GS lines have 50 $\mu$m trace width and 5 $\mu$m gap. The length of the phase shifter is 3 mm. The separation between the two arms is 400 $\mu$m center-to-center. The traces used the 2 $\mu$m thick aluminum layer (M2) in the process. The layout of the via-stack from M2 down to silicon was mainly determined by design rules and considerations to achieve sufficiently low resistances for vias and metal-to-silicon contacts. The detailed pn junction and side doping configurations were described in the previous section. It is worth noting that the phase shifter in the actual TWMZ only has ∼90% of its length loaded with pn junction, due to striation as illustrated in Fig. 3.3(b). The striation in doping was to ensure the current flows in the metal traces toward the wave propagation direction, as opposed to flowing in the silicon.

At the driving end (the right side in Fig. 3.3(b)), a GSGSG pad set was used to deliver differential driving signal to the device. A transition was made on chip from GSG to GS.

At the termination end (the left side in Fig. 3.3(b)), a GSSGSSG pad set was used, offering four 50 Ω ports. Each device arm was associated with two 50 Ω ports in parallel, allowing 25 Ω termination through a GSSGSSG RF probe and off-chip resistors. Other values of termination impedance would be less convenient, but is possible to implement by bonding the photonics chip to a high-speed printed circuit board (PCB) via short-length bond wires, and using surface-mount low parasitic resistors on the PCB. On the other hand, the GSSGSSG pad set allowed us to take the RF S-parameter as discussed in detail in next section.

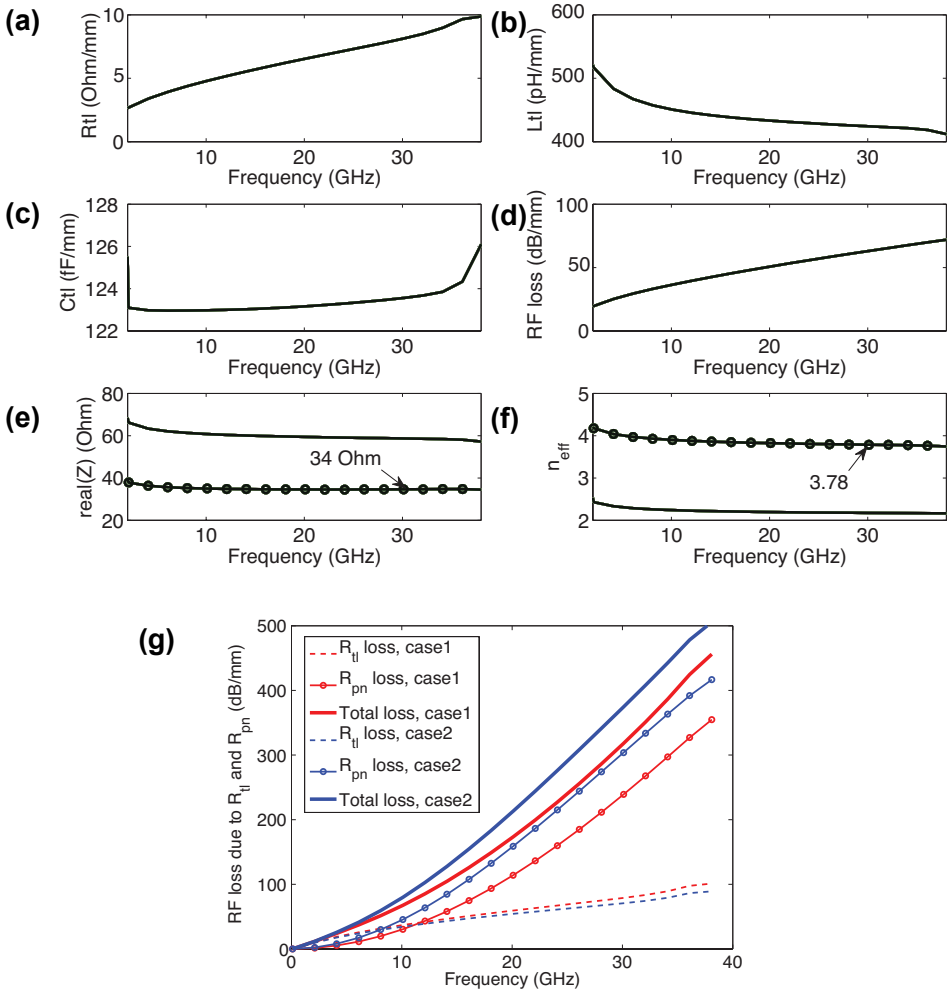



Figure 3.4: (a-f) Simulated unloaded TL (solid line) and junction-loaded TL with 0 V bias (solid line with dots), the frequency axis range is set to 2GHz 38GHz to eliminate artificial simulation data processing errors (g) Simulated RF loss of the device under investigation, Case1 is based on simulated $C_{pn}$ and $R_{pn}$ and Case2 is based on measurement-corrected $C_{pn}$ and $R_{pn}$

Simulated RF characteristics of the transmission line electrodes with and without pn junction loading is presented in Fig. 3.4 (a)-(f). First, the metal traces were simulated in Ansoft HFSS, and then loaded line characteristics were calculated based on the circuit model in Fig. 3.2 (b). The presented curves that involve pn junction, i.e. the dotted traces in Fig. 3.4 (e) and (f) and the entire plot of Fig. 3.4 (g), were calculated at 0 V bias condition and with the 90% junction loading factor taken into account. Near 30G Hz, $R_{tl}$ is 8.1 k $\Omega$/m, $L_{tl}$ is 420 nH/m, and $C_{tl}$ is 120 nF/m. Loaded with pn junction, the impedance is 34 $\Omega$ and RF index is 3.78 at 30 GHz. The RF loss is presented in Fig. 3.4 (g) with the total loss, and loss due to $R_{pn}$ and $R_{tl}$ plotted separately and it is clear that loss is the dominating source of RF loss at high frequencies. In this plot Case 1 trace was obtained with simulated $R_{pn}$ and $C_{pn}$, i.e. 7.2 $\Omega$-mm, and 280 pF/m, whereas Case 2 was using 15 $\Omega$-mm and 230 pF/m to approximate the measured device. The increase in $R_{pn}$ in fabricated device is mainly attributed to the higher sheet resistance in the light P and N doping as well as higher contact resistance from metal to P++ doped silicon, which will be discussed in the measurement section.

### *3.2.5 DC $V_\pi L_\pi$ and insertion loss*

We first measured the optical transmission and DC performance of the device. The optical test setup used an Agilent 81980A tunable laser and an 81636B detector to record the device transmission spectra. The intentional imbalance of the device was 100$\mu$m and the free spectral range was about 5.7 nm. We tracked the null in the spectrum to generate phase shift versus applied voltage on one arm, from which $V_\pi L_\pi$ was calculated. The results are shown in Fig. 3.5. Incidentally, there are some ambiguity and discrepancy about the definition of $V_\pi L_\pi$ in the literature. One way to report $V_\pi L_\pi$ is based on an actual $\pi$ phase shift [20, 32]. This test protocol require devices of various lengths to get a $V_\pi L_\pi$ versus $V_\pi$ (or $L_\pi$) curve and could be difficult for short devices (high voltages). Here we adopted an alternative approach: the $V_\pi L_\pi$ versus applied voltage relation is generated by the measurement of the phase shift $\Delta\phi$ versus applied voltage $V_{applied}$ on one phase shifter of certain length $L_{dut}$, and simply $V_\pi L_\pi = \frac{\pi}{\Delta\phi} V_{applied} L_{dut}$. The curve $V_\pi L_\pi$ versus $V_{applied}$ is basically $V_\pi L_\pi$ versus

$V_\pi$. This approach was widely used in publications on silicon modulators, including several in the references list [33–37].

At -1 V bias the measured phase shifter $V_\pi L_\pi$ was 2.7 V-cm. Further measurements over 5 different chips showed a good uniformity. Taking into account the 90% loading factor, the $V_\pi L_\pi$ of a fully doped waveguide phase shifter would be 2.43 V-cm, higher than the simulated 1.7 V-cm. The measured $C_{pn}$ was 230 pF/m at 0 V and 190 pF/m at -1 V bias for a fully doped waveguide phase shifter, lower than the simulated value 280 pF/m at 0V and 220 pF/m at -1 V. We further measured silicon resistors with various doping types, doping concentrations and silicon thicknesses, and revealed that P++ or N++ doped silicon resistance agreed with simulation within 5%. However, P+ or N+ doped silicon showed ≈30% higher resistance than simulation, and P or N doped resistance showed ≈50% higher resistance than simulation. Combining the higher $V_\pi L_\pi$, lower $C_{pn}$ and higher resistance of P or N doped silicon resistance, we suspect the discrepancies could be due to: physically applied implantation dose being smaller than simulated, and possible incomplete ionization of the dopant. Other fabrication inaccuracies are harder to be verified or excluded.

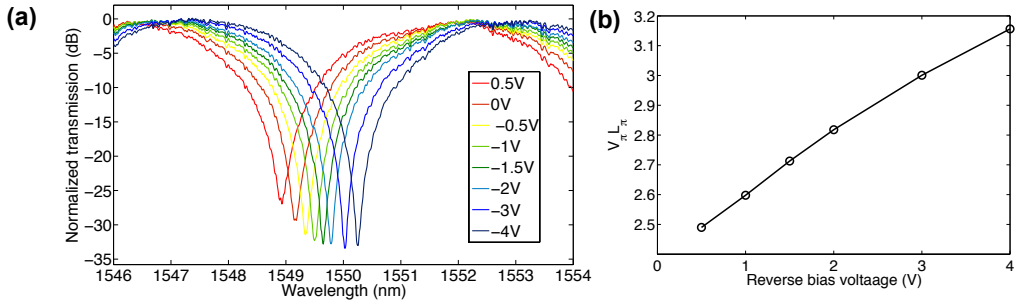



Figure 3.5: (a) Optical spectra versus applied voltage (b) $V_\pi L_\pi$ versus applied voltage

The on and off chip coupling were through grating couplers. The device insertion loss was obtained by comparing the maximum transmission of the MZ spectrum to a grating coupler loop to de-embed the coupler insertion loss. Then the routing waveguide loss was subtracted, and we arrive at the device insertion loss of 6.2 dB that consist of two simple Y-junctions and the phase shifter. We note that the Y-junction in this particular device was

not carefully designed and has a high insertion loss of 1.3 dB each. Therefore the loss due to the phase shifter was only 3.6 dB (averaged from multiple chips with a standard deviation of 0.37 dB). The reduction of the loss in Y-junction would be straightforward, because recently a 0.3 dB insertion loss optimized Y-junction with uniform yield was demonstrated and was fabricated in the same batch of wafers [38].

The 3.6 dB ± 0.37 dB phase shifter insertion loss can be broken down as follows. The waveguide intrinsic loss was measured to be 1.98 ± 0.29 dB/cm from 5 samples on the same wafer, i.e. a ≈ 0.6 dB contribution to the phase shifter loss. Therefore the various dopants (junction and side doping) introduced 3.0 dB ± 0.38 dB loss. Considering the 90% loading coefficient, we can back calculate the free carrier absorption loss was 11.1 ± 1.5 dB/cm, whereas the simulated value is 8.3 dB/cm. The discrepancy could be excess loss due to P+ and N+ misalignment error (the $3\sigma$ of the overlay accuracy was a large fraction of the doping clearance) or a slight change in waveguide dimensions inducing change in optical mode overlap with P+ and N+ dopants. Incidentally, we measured pn junction doped waveguides that are without the side doping P+, N+, P++ and N++. The measured free carrier loss was 6.3 dB/cm on average, which was very close to the simulated 6.8 dB/cm. This made it more likely the extra loss seen in the TWMZ phase shifters was due to P+, N+ doping and etc.

### *3.2.6 Small-signal bandwidth measurement*

The EO frequency response of the TWMZ was characterized using an Agilent 67 GHz Vector Network Analyzer (VNA), and an U2T XPDV3120R-VF-VP 70GHz bandwidth photodetector. The EO S21 is presented in Fig. 3.6. This measurement was done through on-wafer probing with a 40 GHz rated Cascade ACP GSGSG driving probe and a 20 GHz rated Cascade Unity GSSGSSG probe with off-chip resistors for 25 Ω termination. The VNA drove only one device arm at a time; the unused arm was properly terminated at both the driving and termination end with 50 Ω and 25 Ω respectively. This "full-termination" scheme closely resembles the actual operating condition of a differential drive modulator. The probes were not de-embedded from the frequency response and the RF S21 roll-off of the GSGSG probe

was 0.5 dB near the device bandwidth. Reverse bias was applied through the bias-tee in the VNA.

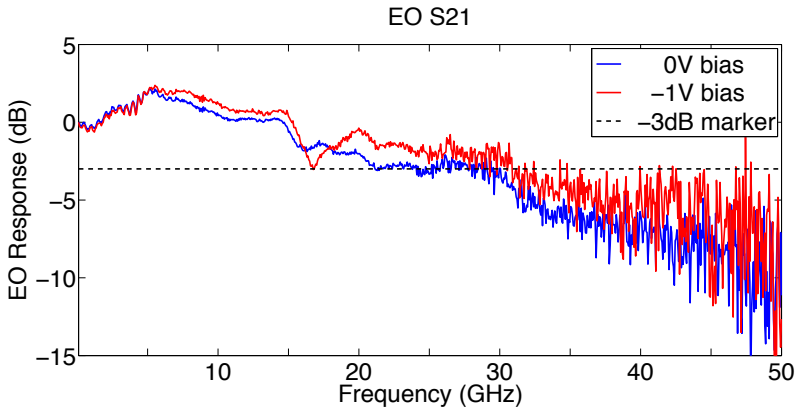



Figure 3.6: EO S21 at 0 V and -1 V bias

30GHz bandwidth was achieved for both arms at 1 V reverse bias. The same bandwidth was almost reached with 0 V bias (a long plateau in the EO S21 coincided with the -3 dB line between 23 GHz and 30 GHz). We observed two distinctive features of the EO S21: the peaking near 5 GHz and the notch near 17 GHz. These two features were consistently observed across many devices on both arms. We will explain them based on RF measurements.

The RF S-parameter measurements were done with the 40 GHz GSGSG probe at the driving side with one GSG port connected to VNA Port 1 and the other GSG port attached to 50Ω to terminate the unused arm. At the termination end, a 40 GHz GSSG probe was used with one GS port connected to VNA Port 2 and one GS port attached to 50 Ω. It presents 25 Ω to the modulator arm under test and receives RF through signal. We had to left the termination end of the untested arm open due to the lack of a high speed GSSGSSG probe. The RF calibration included the cabling but could not include the probes, due to the lack of a GSG-to-GS calibration substrate. The uncalibrated probes were responsible for the fine-pitch ripples on the S-parameters traces, most visible on S11 due to their low magnitude. The measurement results are shown in Fig. 3.7 (a).

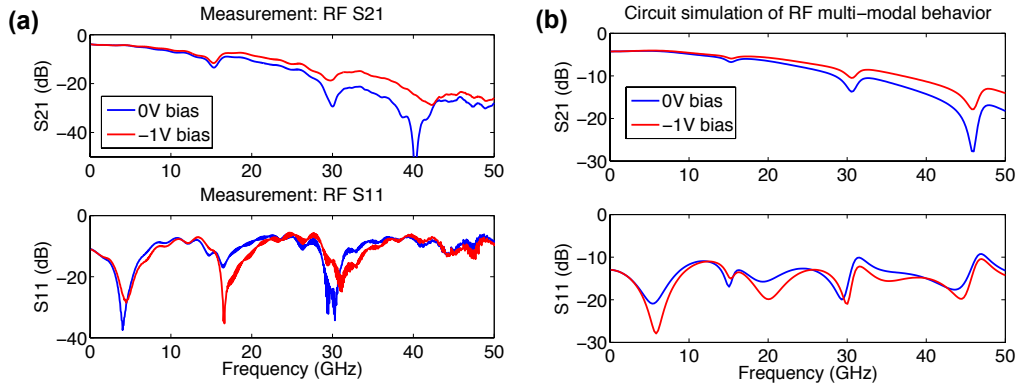



Figure 3.7: a) RF S-parameters measurement (b) circuit simulation to verify hypothesis of RF multi-modal behavior

First of all, we can use RF S11 and S21 to back calculate the RF index and RF loss. The RF index can be obtained by $n_{rf} = \frac{c}{2L_{eff}\Delta f}$, where $c$ is the speed of light in vacuum, $L_{eff}$ is the effective RF length taking into account of the input and termination (estimated to be 3.3mm based on simulation), and $\Delta f$ is the spacing of S11 null locations (measured to be 12 GHz). Therefore RF index was calculated to be 3.8, and is close to the optical group index 3.9.

To calculate RF loss and RF 6.4 dB bandwidth, we should note that the measured RF S21 starts at -3.9 dB rather than close to 0 dB. This was due to the 50 Ω driving, 25 Ω termination testing configuration, which results in a 67% voltage-intake at low frequencies. In principle it should be -3.5 dB, the slightly lower value in measurement was likely due to the series resistance on the long metal traces and probe contact resistance. The RF S21 6.4 dB bandwidth was 20 GHz and 23 GHz for 0 V and -1 V bias, respectively. As mentioned earlier we observed higher resistance in various dopants doped silicon. In addition, we measured the contact resistance between metal and P++ doped silicon to be significantly higher than anticipated and equivalently contributes to 5Ω-mm to $R_{pn}$. We therefore calculated that in the fabricated device $R_{pn}$ is 15Ω-mm instead of the simulated 7.2 Ω-mm. This measurement-corrected resistance in combination with the measured allowed us to re-simulate the RF loss based on measurements, as shown in Fig. 3.4(g) (Case2). It suggests a RF 6.4 dB bandwidth

of 20 GHz at 0V, in excellent agreement with measurement.

The difference between RF 6.4dB bandwidth and EO S21 3dB bandwidth is due to the mismatch between device impedance and termination impedance. This assessment can be evaluated analytically by expressing the RF voltage amplitude on the transmission line as forward and reverse propagating waves due to reflection then an overlap integral with the forward propagating optical wave would generate the EO response [39]. For the 33Ω impedance device we simulated three different termination scenarios and they are shown in Fig. 3.8.

In these simulations, we chose an approximate $f^2$ dependent RF loss function to have RF 6.4 dB bandwidth of 23 GHz to emulate measured performance at -1V bias. In the case where the termination was exactly matched to device impedance (i.e. $Z_{term} = 33\Omega$), as expected the EO 3 dB bandwidth was almost exactly at the RF 6.4 dB bandwidth. For high impedance termination case (i.e. $Z_{term} = 50\Omega$), the device bandwidth was very limited and the crossing of the -3 dB line was only at 13 GHz, this is caused by the reflected wave with an undesired phase shift. On the other hand, for the low impedance termination case (i.e. $Z_{term} = 25\Omega$), which is close to the measurement condition, the reflected wave enhanced the EO response. Near 5 GHz we observed peaking of similar magnitude as that in the measurement, the peaking effect is most pronounced at low frequency S11 nulls primarily due to less phase mismatch (and secondarily due to less RF loss). The device showed close to 29 GHz bandwidth. This is a close match to measurement results, validating our theory. This indicates an advantage of using termination impedance that is lower than the device impedance. As we discussed earlier, at low frequencies the voltage on the device can be evaluated by $\frac{V_t erm}{V_0} = \frac{2Z_{term}}{Z_0+Z_{term}}$ and a voltage-intake factor of 67% is obtained for 25 Ω termination versus 50 Ω termination. Considering a bandwidth extension ratio of 2.2 (29 GHz / versus 13 GHz), the 25 Ω termination case appeared to be more advantageous overall.

Finally, we address the other distinctive signature in the EO S21: the notches in the spectrum. Due to its low magnitude, the notch in the EO S21 would not noticeably degrade eye-diagrams, as was suggested by our eye-diagram simulation comparisons between artificially smoothened EO S21 and measured EO S21. However, the notches are certainly detrimental features and could lead to serious problems in certain designs if we do not de-

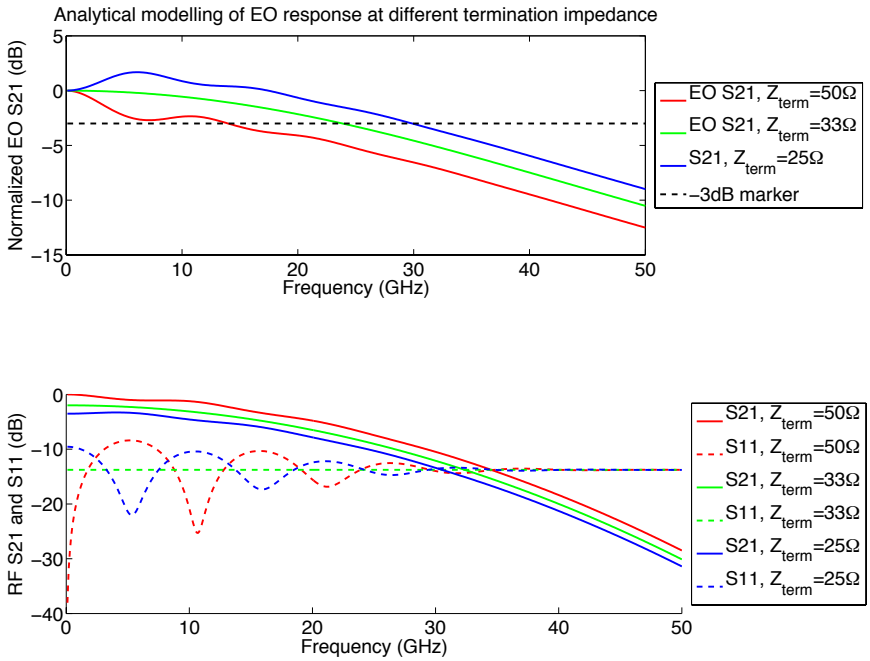



Figure 3.8: Analytical modeling of EO response with respect to termination impedance

velop a good understanding of its root cause. Observing the RF S21, it is evident the notches and steps in EO S21 occur at similar locations as the notches in RF S21. The most visible ones on EO S21 are near 17GHz and 30 GHz. The magnitude of the RF S21 notch at 17 GHz was 3–4dB, which could mostly explain the corresponding notch in the EO S21. To explain the notches in RF S21, we propose a hypothesis that the GS-SG structure is multi-modal. In more detail, when we were testing one device arm, i.e. driving one GS transmission line, we were effectively driving a GS-G structure. The G trace far away has a non-negligible RF interaction with the S trace. This GS-G structure supports two modes due to asymmetry (structure, dielectrics distribution and pn junction loading). A full structure HFSS simulation was challenging due to the large computation domain (long device length and large lateral span), but an analytical analysis could be formulated based on [40]. As a simplification for weakly coupled lines we assume the GS-G supports the 33–37 Ω mode ("main"

mode) we originally designed between the S and the nearby G trace, and the GS-G also supports a stray mode that is mostly between the S and the far away G trace. We model the two modes as two independently propagating modes only connected at the beginning and end of the line. The combined line was driven by a 50Ω source and terminated by 25 Ω. We used the TWMZ parameters described earlier for the main mode, and estimated the capacitance between the S trace and the far away G trace is $C_{stray} = \approx 20$pF/m, using two-wire transmission line equations [29]. To avoid complicated circuit models, we picked reasonable constant metal skin resistance as opposed to a frequency-dependent multi-resistor-inductor network (which is responsible for the large simulation errors in S21 notch amplitude and S11 amplitude and null location). But, our simple model appeared to be sufficient as a qualitative validation. Using a circuit simulator, we obtained the traces in Fig. 3.4(b) with stray inductance between S and side G as $L_{stray}$=4.2 $\mu$H/m. Qualitatively, Fig. 3.4(b) agrees well with Fig. 3.4(a), and validates our multi-modal hypothesis.

In light of this observation we further comment that, notches in RF S21 were observed in previous demonstrations of TWMZ modulators that were based on a GSG layout (or a GSGSG layout by combing two GSG arms), where the pn junction was loaded only in one of the two GS slots. Examples include Fig. 5 in [33], Fig. 9 in [41], Fig. 4 in [35] and likely Fig. 4 in [42]. Many demonstrations did not present EO or RF S21, therefore it is difficult to have a more complete summary. But, according to our simulations in HFSS of a few relatively compact GSG modulator structures, notches were usually present in RF S21. It is very likely that the notches in these demonstrations are due to multi-modal RF behavior as well: the one-side junction loading makes the GSG structure highly asymmetric in a similar fashion as the GS-G structure we discussed above and this RF multi-modal property is expected to exhibit detrimental effect given that the device is sufficiently long and/or the testing frequency is sufficiently high.

A simple remedy to both the GSG structure and GS-G structure is that one needs to periodically tie together the ground planes that are on both sides of the S trace, so that effectively there is only one large ground plane interacting with the S trace, ensuring only one RF mode is supported between S and G. The spacial period of the "G-tie" should be much smaller than the beat length of the lowest two eigenmodes of the originally multi-mode

structure.

### *3.2.7 Conclusions*

To summarize this section, we address the design and characterization of a high performance silicon PN junction traveling-wave Mach-Zehnder modulator. The key underlying design tradeoffs are identified and incorporated into the device design. A device is then presented with significant performance improvement compared to the state of the art.

A PN junction design should maintain a low $(V_\pi L_\pi)\, R_{pn} C_{pn}^2$ factor to enable low $V_\pi$ with high device bandwidth. Modulation efficiency needs to trade effectively with optical loss, indicated by the $F_{dB-V}$ figure-of-merit. For both considerations we chose lightly doped PN junction with optimized 3-level side doping.

We have shown that lower device impedance is advantageous for overall device performance, and a 33–37Ω device impedance was chosen for the TWMZ design. Having termination impedance lower than the device impedance has benefit in terms of bandwidth extension while only incurring modest voltage loss. A bandwidth extension factor of 2.2 was achieved while the voltage-intake factor was maintained at a reasonable 67%. Multi-modal RF behavior is proposed and qualitatively verified to be the possible cause for the S21 notches observed in our device as well as several recent GSG modulator demonstrations. A remedy is suggested to combat this. Therefore, performance enhancement and impairment are both possible with respect to the RF design aspect of a TWMZ device, and 6.4 dB RF bandwidth is not always a good indicator of 3 dB EO response bandwidth.

## *3.3 40-Gb/s TWMZ with slow-wave transmission line electrode*

### *3.3.1 Introduction*

High-speed modulators are key building blocks in silicon photonics [22]. Traveling-wave Mach-Zehnder (TWMZ) modulators are often deployed in practical systems [43] because they offer several key properties, such as thermal insensitivity and high robustness against fabrication variations. Proper RF design is critical to achieve good performance on TWMZ devices. With typical silicon pn junctions and waveguide geometries of the phase shifter, 50

Ω device impedance is usually challenging to achieve due to the high junction capacitance per unit length; instead, TWMZ is often implemented at lower impedances (near 30 Ω for instance) [28, 32, 33, 44]. In addition to creating reflections to driving circuitries, low device impedance incurs bandwidth penalty when terminated with standard 50 Ω impedance [39,45]. This design difficulty is worsened when the modulator designs employ more advanced pn junctions that offer improved $V_\pi L$ but often at the cost of high capacitance [46, 47]. Another key aspect of the RF design is the RF cross-talk effect in multi-conductor TWMZ devices due to the excitation and coupling of multiple RF modes, as has been discussed by [28] and [48] in particular. It is indeed a bandwidth-limiting effect as evidenced by the dips in the EO or RF S21 in several results [28, 33, 35, 41, 44, 49].

In this paper we demonstrate a differential-drive TWMZ modulator using slow-wave electrodes. The slow-wave electrode design significantly increases the achievable inductance per unit length, thus effectively raise the device impedance. The core aspect of a slow-wave TWMZ design is pulling the current paths farther apart laterally from each other in order to raise the transmission line inductance. This raises device impedance, but can potentially raise ohmic losses as well as expanding the size of the RF mode. In particular, the expanded RF mode then more readily exhibits long-range interference, and directional coupling between the two arms, leading to potentially destructive cross-talk within the modulator.

Slow-wave electrode designs have been used in III-V compound modulators [50, 51], though in these cases were used primarily to achieve velocity matching between RF and optical wave. In the silicon system, this type of design has only been explored by Chen et al. [52] and Merget et al. [48]. In [52], the modulator uses a single-drive push-pull configuration. The back-to-back pn junction configuration reduces capacitance loading in half but also reduces the voltage dropped on each arm by the same factor, therefore this configuration incurs higher drive voltage compared to differential-drive. In [48], the GSSG structure supports three RF modes. The authors addressed the cross-talk challenge by utilizing a RF common-mode drive configuration in which only one RF mode was selectively excited.

Our device operates with a GSGSG configuration. The design ensures true single-RF mode operation by laterally connecting ground traces together using lower level metal layer (Metal1), and the single-RF mode operation is verified experimentally by differential mode

and single-ended mode S-parameter measurement. The RF loss associated with slow-wave electrode is maintained to be a small portion compared to the overall RF loss of the device and therefore is not a limiting factor of device bandwidth. A large G patch in the center of the device enables isolation between the two arms to be achieved, which allows for completely independent drive of both arms. This is compatible with commonly used differential signaling scheme and is potentially useful for advanced modulation formats such as quadrature-phase-shift-keying (QPSK).

Due to the combination of large inductance and capacitance per unit length, the RF effective index is 6–7 in the device we report. It is significantly larger than in a typical coplanar strip transmission line designs, where the loaded device RF index is close to the optical group index (3.5–4). We analyze the effect of using periodical phase matching and experimentally demonstrate that using this technique the achieved bandwidth is within a few percent of a continuously velocity-matched modulator.

The 3.5-mm device we report shows an EO 3-dB bandwidth of 21.5 GHz at 0 V bias and 27 GHz at -1 V bias. Both numbers match closely to RF S21 6.4-dB bandwidths, suggesting little RF reflection, cross-talk or other detrimental RF effects are occurring [30]. The RF reflection (S11) is better than -18 dB within the 3-dB bandwidth under both bias voltages. 5.5 V voltage on each arm differentially achieves a $\pi$ phase shift (i.e. full extinction). Between -1 V and 0 V the small-signal $V_\pi$ is 7.8 V, which is useful metric to estimate phase shift and extinction at low drive voltages. 40 Gb/s error-free operation is demonstrated with a power-efficient 1.6 $V_{pp}$ differential-drive. When driving the device with 4.8 $V_{pp}$ differential-drive, the bit-error-rate (BER) versus optical signal-to-noise ratio (OSNR) performance is comparable to that of a commercial 40-Gb/s Lithium Niobate modulator (single-drive) with similar driving voltage amplitude. This establishes that the level of nonlinear distortion found within our silicon TWMZ is minimal and should not be an issue for utilization in communications systems.

### *3.3.2 Slow-wave transmission line electrode*

Slow-wave transmission line electrode [50, 51] refers to ground-signal (GS) or ground-signal-ground (GSG) coplanar strip transmission lines loaded with periodic segmented lateral electrodes (Fig. 3.9(a)–3.9(b)). The segmented lateral electrodes in slow-wave transmission line restrict RF currents to flow only in the continuous G and S strips that have much larger separation ($D$) thus providing higher inductance per unit length ($L_{tl}$). To build a traveling-wave modulator, sections of capacitive pn junction phase shifters are loaded in the gap $d$ (Fig. 3.9(d)). Fig. 3.9(c) shows the distributed circuit model [53]: $L_{tl}$, $R_{tl}$ and $C_{tl}$ are the unit length inductance, resistance and capacitance respectively of the metal transmission line. $C_{pn}$ and $R_{pn}$ are the pn junction capacitance and series resistance (from the G and S traces to the pn junction) respectively.

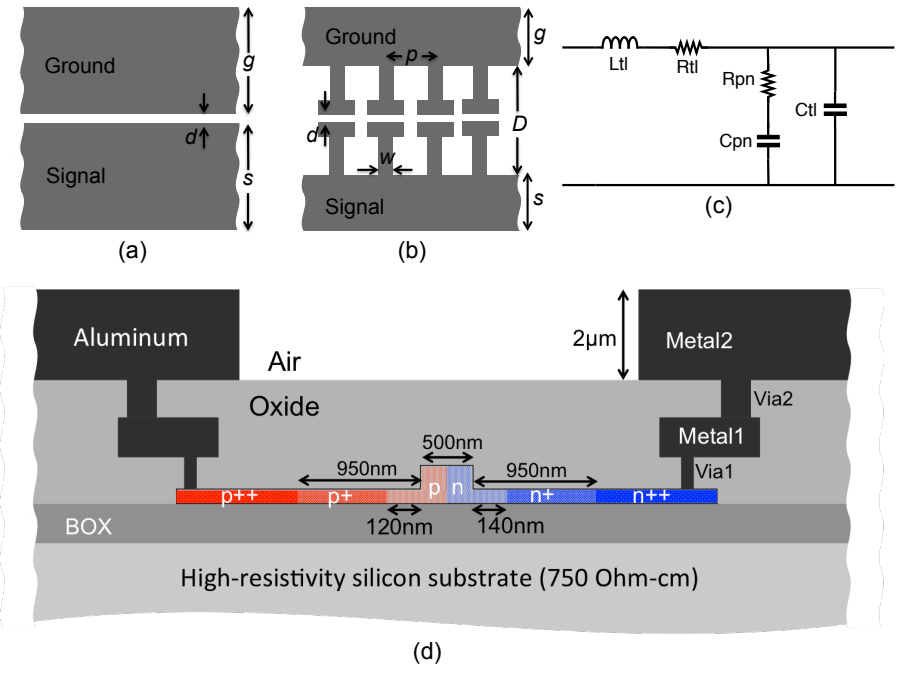



Figure 3.9: (a) Coplanar strip transmission line (b) slow-wave transmission line (c) simplified equivalent circuit model of pn junction loaded transmission line electrode (d) simplified cross sectional diagram of the phase shifter, not to scale

Fig. 3.9(d) illustrates the cross-section of the pn junction phase shifter used in our device with key dimensions annotated. The device fabrication was at the Institute of Microelectronics (IME), A*STAR, Singapore, through an OpSIS multi-project-wafer run [54]. The fabrication process is similar to that of [28] and [44]. The phase shifter uses striploaded ridge waveguide with a slab thickness of 90 nm and ridge height of 220 nm. The pn junction is formed at the center of the waveguide by $5 \times 10^{17}/\text{cm}^3$ p-dopants and $3 \times 10^{17}/\text{cm}^3$ n-dopants. The intermediate p+ and n+ dopants are on the level of $2 \times 10^{18}/\text{cm}^3$. They significantly decrease the series resistance $R_{pn}$ while maintaining low optical loss [44]. The junction capacitance $C_{pn}$ is approximately 250 fF/mm at 0 V bias and the series resistance $R_{pn}$ is 0.7 Ω-cm. We use the top metal layer Metal2 for the G and S traces as well as the segmented lateral electrode. This metal layer is thicker and mostly above the dielectric thus offers a lower resistance and lower capacitance. The lower level metal Metal1 is used for local connections to silicon.

### *3.3.3 Comparison to coplanar strip transmission line*

To illustrate the key differences in RF characteristics between coplanar strip transmission lines and slow-wave transmission lines, we show the numerical analysis of a design case of each. Coplanar strip transmission lines have been frequently used to build traveling-wave modulators in silicon. We analyze the RF design used in [44], with ground trace width $g = 50\mu$m, signal trace width $s = 50\mu$m and GS gap $d = 5\mu$m.

For slow-wave transmission line, we analyze the RF design used in the modulator that we report here. Its geometric parameters are labeled in Fig. 3.9(b): ground trace width $g = 30\mu$m, signal trace width $s = 10\mu$m, GS gap $d = 6\mu$m, GS trace separation $D = 100\mu$m, lateral electrode period $p = 14\mu$m, and lateral electrode width $w = 5\mu$m. In addition to the structure shown in Fig. 3.9(b), the actual modulator device has an additional center G patch to isolate the two device arms (see Fig. 3.11), this G patch is included in the simulation.

We used Ansoft HFSS for 3D electromagnetism simulation and extracted the RF line parameters ($R_{tl}$, $L_{tl}$ and $C_{tl}$) as shown in Fig. 3.10. We further combine them with the junction parameters $C_{pn}$ and $R_{pn}$ to calculate the loaded line RF effective index $n_{eff}$ and

impedance $Z$, also shown in Fig. 3.10. As it is evident from Fig. 3.10, compared to the coplanar strip transmission line with similar GS gap $d$, the slow-wave transmission line offers much higher (2.5×) inductance per unit length while only have 25% more capacitance, therefore effectively raises the device RF impedance.

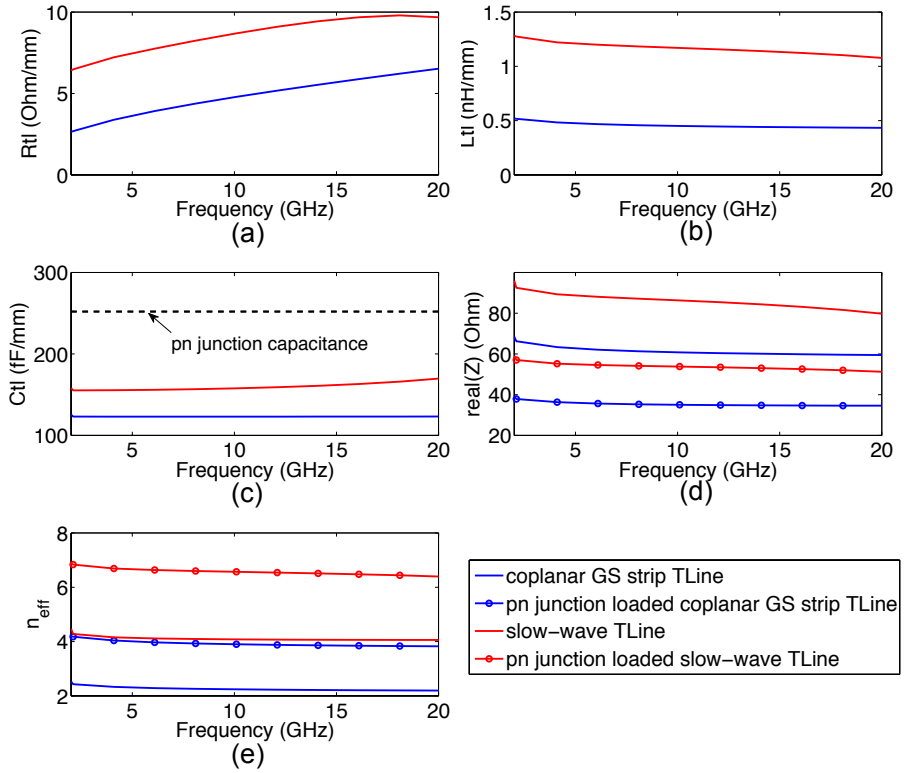



Figure 3.10: Comparison of simulated transmission line parameters. Coplanar GS strip line parameters: $g = 50\mu m$, $s = 50\mu m$, and $d = 5\mu m$. Slow-wave transmission line parameters: $g = 30\mu m$, $s = 10\mu m$, $d = 6\mu m$, $w = 5\mu m$, $p = 14\mu m$ and $D = 100\mu m$.

### *3.3.4 Device configuration and design considerations*

The fabricated Mach-Zehnder modulator with slow-wave electrode is shown in Fig. 3.11. We include a wide center ground patch to isolate the two device arms. Both signal traces are connected to the cathode of the pn junction on each arm of the modulator, thus differential

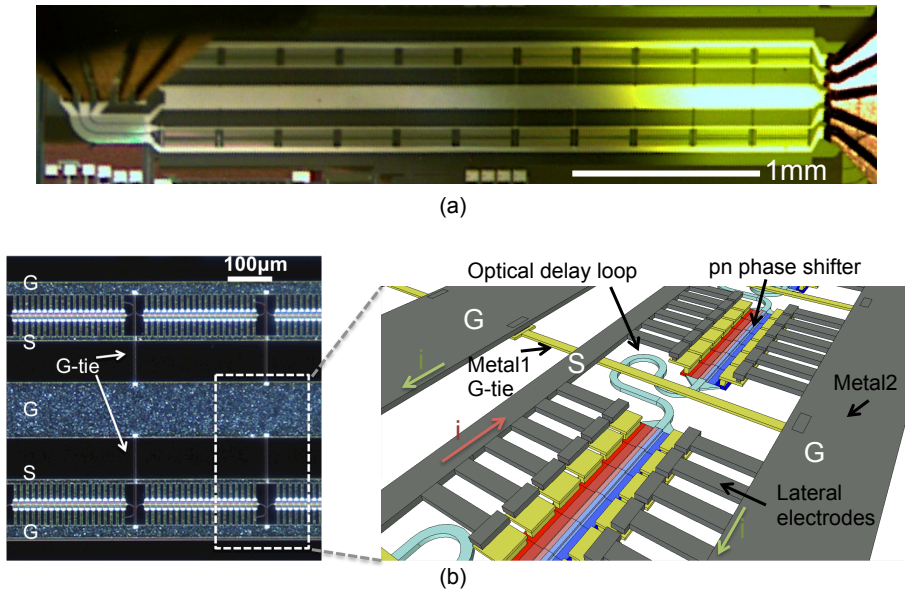



Figure 3.11: (a) Fabricated device under probed testing: GSGSG probe on the right is for driving, and GSGSG probe on the left is for providing 50Ω termination to each device arm (b) microphotograph of a section of the device, mainly top metal (Metal2) is visible. Inset (not-to-scale): details near a ground-plane lateral connection (G-tie) and the optical delay loop for re-aligning optical and RF phase

electrical signaling generates differential phase on the device arms. GSGSG probes, visible in the micrograph, were used for driving and providing 50 Ω termination to the device in high-speed testing. In such a multi-conductor structure, in addition to the desirable RF mode exists between the S and G traces directly connected to the pn junction phase shifter, the center G patch and the S traces also support so-called "slot-line" mode. One way of suppressing cross-talk to and excitation of such unwanted modes is through wire bond air bridges [55]. In our device, we implemented such lateral ground connections (namely G-tie) in lower level metal (Metal1), as illustrated in Fig. 3.11(b). We chose a device length of 3.5 mm, of which 3-mm length is loaded with pn junction phase shifters. The overall device width is 620 $\mu$m. Simulation result suggests that at 0 V bias on the pn junction the device RF loss reaches 6.4 dB near 24 GHz, indicating the EO bandwidth could reach this number.

The periodicity of G-tie is approximately 300 $\mu$m. The device in total has 12 G-tie regions.

In the previous section we compared the RF characteristics of a coplanar strip transmission line and a slow-wave transmission line. Besides the desirable increase in inductance and achievable device impedance, there are two aspects in slow-wave transmission line that are worth careful considerations.

The first one is the higher $R_{tl}$. Fortunately, the RF loss originates from the metal conductor resistance $R_{tl}$ scales with respect to $\sqrt{f}$, whereas the RF loss due to the silicon resistance $R_{pn}$ scales with respect to $f^2$ [53]. Using the RF parameters from HFSS simulation and equation (6) in [53], we show that in our device near the 3-dB bandwidth $R_{tl}$ loss is only 30% of the total RF loss, as presented in Fig. 3.12(a). Therefore, even though the slow-wave transmission line exhibits higher $R_{tl}$ induced RF loss, it is still far from a limiting factor for device EO bandwidth – RF loss due to $R_{pn}$ remains to be the dominating loss mechanism at high frequency.

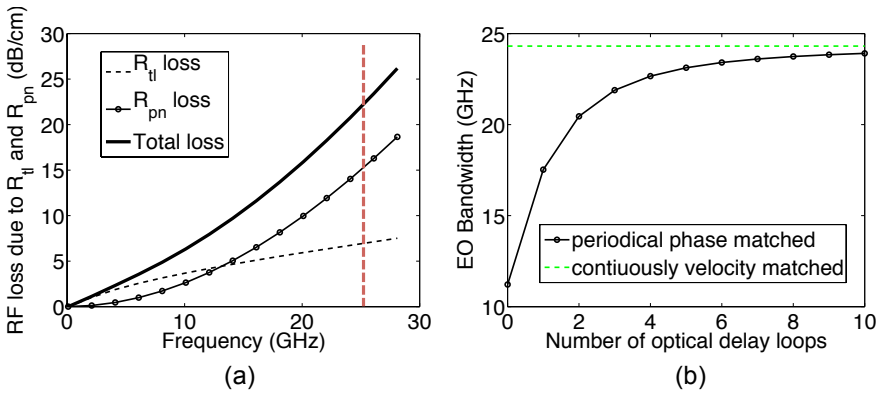



Figure 3.12: (a) Simulated RF loss due to pn junction series resistance $R_{pn}$ and transmission line metal resistance $R_{tl}$, red dashed line marks the 3-dB bandwidth location (b) Simulated EO bandwidth versus numbers of optical delay loops, the green dashed line marks the 3-dB bandwidth of a continuously velocity matched modulator that has the same RF loss

The other consideration is that $n_{eff}$ in the slow-wave electrode device is close to 6.5 (see Fig. 2), which is substantially higher than the optical group index [56] in the silicon waveguide (approximately 3.8). To address the strong velocity mismatch between RF and

optical waves, we break down the whole device into sections and include an optical delay loop after each section to compensate for the faster optical wave, fully realigning its phase to the RF wavefront. To calculate the device bandwidth with respect to different numbers of optical delay loops (i.e. numbers of sections) while maintaining the total device length constant, we use the RF loss in Fig. 3.12(a) and the RF and optical indices mentioned above to carried numerical simulations. We further assume RF reflection is negligible and each optical delay loop correctly compensates the phase walk-off in the section of traveling-wave phase-shifter precedes it. According to the simulation result shown in Fig. 3.12(b), we divided the device into 11 sections and implemented 10 optical delay loops such that the device bandwidth is within 2% of a continuously perfectly velocity match modulator. The optical delay loops are implemented in the G-tie regions that do not have pn junction loading to reuse space, as illustrated in Fig. 3.11(b).

### *3.3.5 Optical spectra and DC $V_\pi$ measurement*

The device uses grating couplers to couple light on and off the chip. Routing waveguide of a few millimeter length is used to connect the device input and output to the grating couplers. To extract the device insertion loss we measured the optical spectra of the device and a reference grating coupler loop near the device, as shown Fig. 3.13(a). The fringes in the device spectrum are due to 100$\mu$m intentional imbalance of the Mach-Zehnder arm lengths. This allows convenient change of the modulator phase bias by tuning the wavelength.

The total on-chip insertion loss of the device is measured to be 8.0 dB. According to further measurements of each component, this insertion loss includes the following: 0.3 dB due to routing waveguide between the device and the input / output grating couplers, 0.9 dB due to the two Y-junctions, 3.6 dB due to the 3-mm active phase shifter, the remaining 3.2 dB is due to two layout issues in the G-tie regions: (1) the Metal1 G-tie accidentally overlapped with a long section of waveguide and (2) too abrupt waveguide tapers were used between the optical delay loops and the striploaded phase shifters. This 3.2 dB loss can be substantially reduced by (1) switching to Metal2 for the part of G-tie that covers the waveguide and (2) using striploaded waveguide in the optical delay loops thus avoid tapers

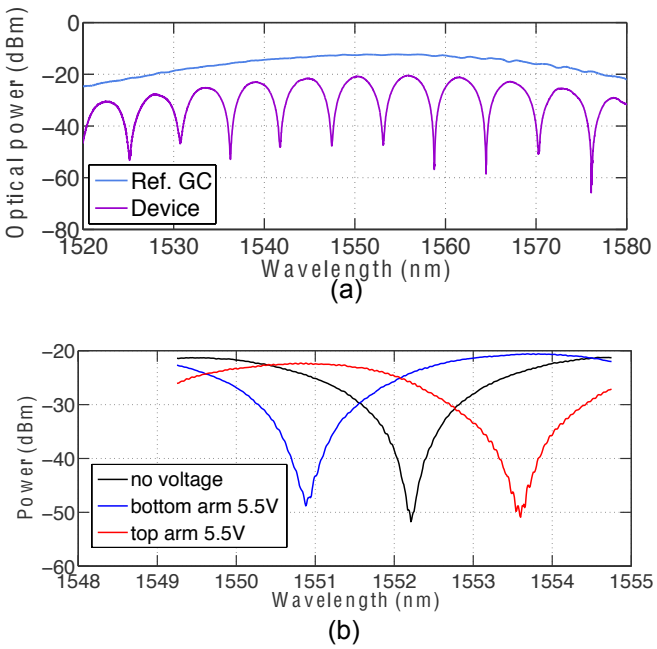



Figure 3.13: (a) Optical spectra: device vs. reference grating coupler (GC) (b) $\pi$ phase shift under 5.5V voltage on each arm

all together. We then measured phase shift versus voltage on both arms. Between -1 V and 0 V the small-signal $V_\pi$ is on average 7.8 V. A full $\pi$ phase shift is achieved with 5.5 V voltage differential drive, as shown in Fig. 3.13(b).

### *3.3.6 Small-signal EO bandwidth*

We then characterized the small-signal EO bandwidth of the device through S-parameter measurements using a vector-network-analyzer (VNA) and a 70-GHz bandwidth photodetector from u2t. The measurements were carried out using the probing configuration shown in Fig. 3.11(a), where a GSGSG probe was used for driving and another GSGSG probe (with termination resistors connected) was used for providing 50 Ω termination to each device arm.

First, "single-ended" EO S-parameter measurement was carried out using an Agilent E8361C 2-port VNA. In this experiment one arm was driven and the unused arm was

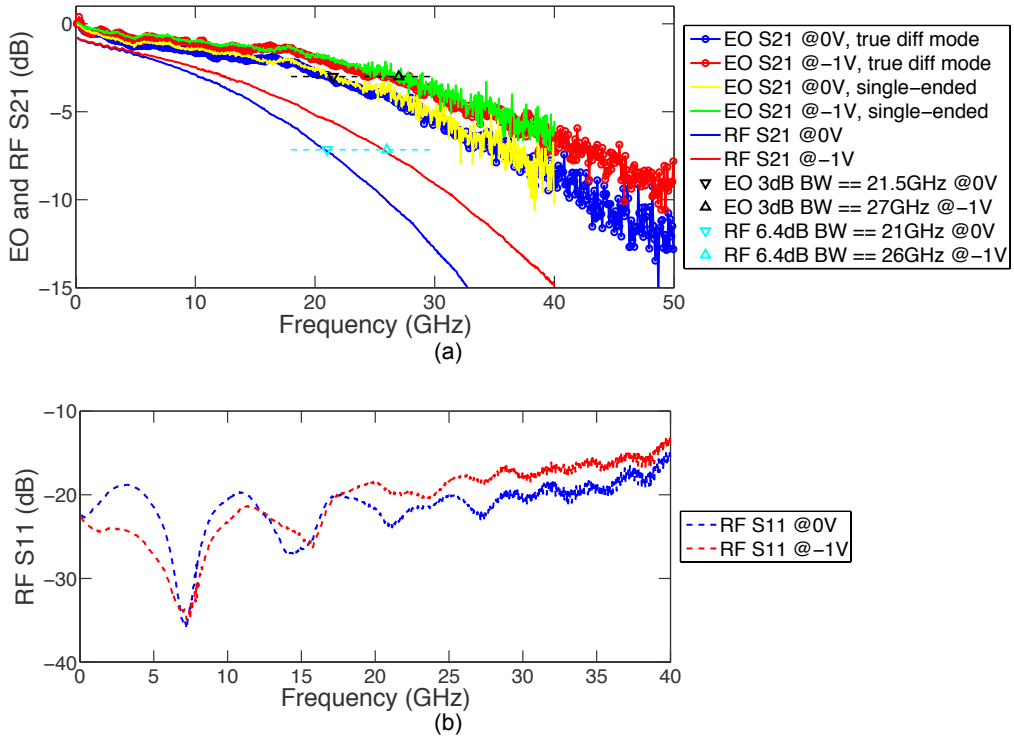



Figure 3.14: EO and RF S-parameters at 0 V and -1 V bias (a) EO and RF S21 (b) RF S11

terminated with 50 Ω at both ends. The result is shown in Fig. 3.14(a) in yellow and green, for 0 V and -1 V bias respectively. Secondly, we repeated the EO S-parameter measurement using true differential-mode excitation with an Agilent N5227A 4-port VNA, in which the two device arms were driven by the VNA differentially. The corresponding result is shown in Fig. 3.14(a) in blue and red dotted lines that almost completely overlap with the single-ended measurements. These two sets of EO bandwidth measurements suggest that the device bandwidth is 21.5 GHz at 0 V bias and 27 GHz at -1 V bias. The smoothness of the EO S21 and the similarity between single-ended and differential-mode S21 suggest that G-tie is effective in suppressing RF cross-talk and multi-mode effects, and the two device arms are fully independent. This enables the device to be compatible with single-ended and differential driving scheme, which are the most commonly used in driving circuitries. Having two fully-independent arms is also potentially useful for advanced modulation format such

as QPSK, where the two device arms carry uncorrelated data patterns.

We further carried out calibrated RF S-parameter measurement, in which the termination probe was connected to a VNA port to receive the RF "through" signal at the end of the device. This experiment was taken on each individual arm, with the unused arm terminated by 50 Ω. The measured RF S21 and S11 are shown in Fig. 3.14 for a direct comparison to the EO S21. We observed a 6.4-dB bandwidth of 21 GHz at 0 V bias and 26 GHz at -1 V bias. The importance of RF 6.4-dB bandwidth is that if device EO bandwidth is only limited by RF attenuation, EO 3-dB bandwidth should coincide with RF 6.4-dB bandwidth [30,39].This is indeed the case as suggested by the EO S21. Thus overall RF and optical velocities are indeed closely matched and other detrimental RF effects such as strong RF reflections or RF cross-talk effects do not exist in the device. The extracted RF index of the loaded slow-wave electrode is 6.1 near 25 GHz at 0 V bias, only a small deviation from the simulated value 6.5. We note that the measured RF 6.4-dB bandwidth at 0 V bias is 21 GHz, slightly lower than the simulated value 24 GHz (see Section 3.3.4). This is attributed to the high metal-to-silicon contact resistance on p++ silicon, which was measured in separate test structures to be 5–10 k$\Omega/\mu$m$^2$ depending on via sizes. This corresponds to a 0.1–0.2 Ω-cm increase in $R_{pn}$ that explains this slight bandwidth degradation.

### *3.3.7 Data transmission measurements*

EO S-parameters characterize device bandwidth in small-signal regime and provide useful information validating device design and modeling accuracy. The large-signal dynamic performance of the device in actual high-speed data transmission was evaluated by bit-error-rate (BER) versus optical signal-to-noise ratio (OSNR) measurement described in this section. The experiment setup is shown in Fig. 3.15(a). Non-return-to-zero (NRZ) pseudo-random-bit-stream (PRBS) with $2^{31} - 1$ pattern at 10 Gb/s was generated by an Anritsu pulse pattern generator (PPG) and then 4-way split and delayed before being multiplexed into a 40 Gb/s using an SHF 24210A module. The differential 40 Gb/s output was amplified by a pair of Centellax OA4MVM3 driver amplifiers, then attenuated to the desired amplitude by passive attenuators. The pair of driving signal was applied to the device through a pair

of high-speed bias-tee and a 65 GHz GSGSG probe. The device probing and termination configuration were the same as in the S-parameter measurements. A tunable laser was used as the input light to the device and its wavelength was chosen to set the device near quadrature (-3 dB point). The modulated light was combined with tunable ASE noise loading that varied the OSNR in the experiments and then passed through an erbium-doped fiber amplifier (EDFA). The output optical signal was split into two branches and fed into an optical spectrum analyzer (OSA) for OSNR monitoring and a u2t DPRV 2022A receiver (AC coupled, -10 dBm sensitivity) with differential outputs. During the experiments the optical modulation amplitude (OMA) into the receiver wa maintained to be near 0 dBm, well above its sensitivity. One of the receiver output was connected to an Agilent 86100B digital communication analyzer (DCA) for eye-diagram viewing. The other output was connected to an SHF 34210A 1:4 demultiplexer followed by an SHF 58210A selector. The demultiplexed and selected tributary was sent to an Anritsu MU181040A error-detector for BER test. The reported BER is an average from all 4 tributaries.

We carried out the BER versus OSNR measurement on the silicon TWMZ modulator and a commercial Lithium Niobate 40-Gb/s modulator that has 5.9 $V_\pi$ for comparison. The Lithium Niobate modulator is a single-drive component and is driven with 5.4 $V_{pp}$, which was the maximal available drive voltage from the driver amplifier due to limited output voltage from the multiplexer. The silicon TWMZ modulator was tested with two different driving configurations: 4.8 $V_{pp}$ drive on each arm with 3 V reverse bias and 1.6 $V_{pp}$ drive on each arm with 1.5 V reverse bias. Because the receiver is AC coupled, an extinction ratio (ER) measurement was not readily available on the DCA. We measured the conversion gain of the receiver under various power levels and recorded the average power into the receiver in the each experiment. Based on these measurements, we calculated that ER is 6–7 dB in the measurement of Lithium Niobate modulator and in the measurement of silicon TWMZ modulator with 4.8 $V_{pp}$ drive. The low ER (6–7 dB) is likely caused by the gain compression of the EDFA and photo-receiver used in the experiments (Fig. 3.17). A separate measurement using a DC-coupled optical module in the DCA and without the EDFA yielded approximately 10 dB extinction ratio at 40 Gb/s. The ER is approximately 4 dB in the measurement of silicon TWMZ modulator with 1.6 $V_{pp}$ drive. As the results in Fig. 3.15(b)

suggest, the silicon TWMZ shows negligible OSNR penalty compared to Lithium Niobate modulator when driven with 4.8 $V_{pp}$. This establishes that the level of nonlinear distortion found within our silicon TWMZ is minimal and should not be an issue for utilization in communications systems. The silicon TWMZ shows approximately 2 dB OSNR-penalty when driven with 1.6 $V_{pp}$. compared to the 4.8 $V_{pp}$ drive and Lithium Niobate. Error-free (BER $<$ 1e-12) eye diagrams of the Lithium Niobate modulator and the silicon TWMZ modulator under different driving voltages are shown in Fig. 3.16.

### *3.3.8 Conclusion*

We demonstrate slow-wave electrode based design as a viable approach for realizing high-speed silicon traveling-wave modulators. As more advanced low $V_{\pi}L$ junctions are employed in silicon modulators, slow-wave electrodes offer a promising way to drive such highly capacitive junctions at 50 Ω. We experimented with periodical phase matching and showed that the EO 3-dB bandwidth closely tracked RF 6.4-dB bandwidth, indicating the RF and optical velocities overall are well matched despite their strong intrinsic mismatch within each individual section. RF cross-talk issue is addressed in our design. Single-RF-mode operation is achieved and the two device arms are fully independent, making the device compatible with differential signaling and uncorrelated signaling on the two device arms typically used in advanced modulation formats, such as QPSK. The device achieves full extinction with 5.5 V voltage on each arm and shows an EO bandwidth of 27 GHz under 1 V reverse bias. At 40 Gb/s, when driving the device with 4.8 $V_{pp}$ on each arm, the BER versus OSNR performance of the device is comparable to that of a commercial 40 Gb/s Lithium Niobate modulator with 5.4 $V_{pp}$ single-drive.

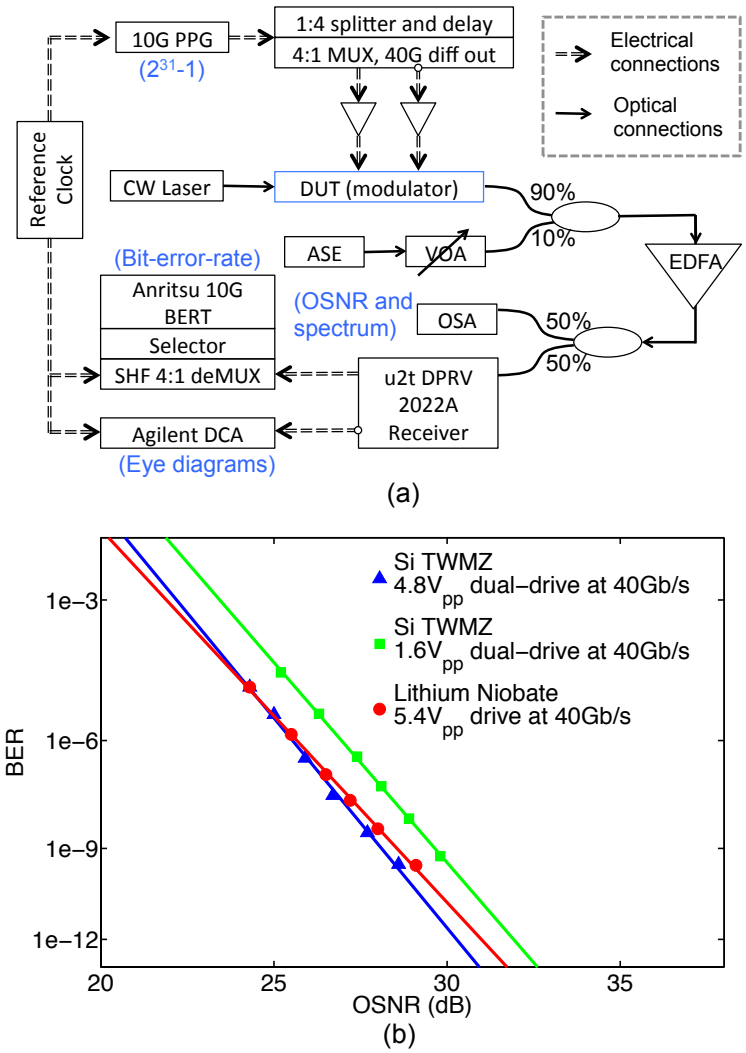
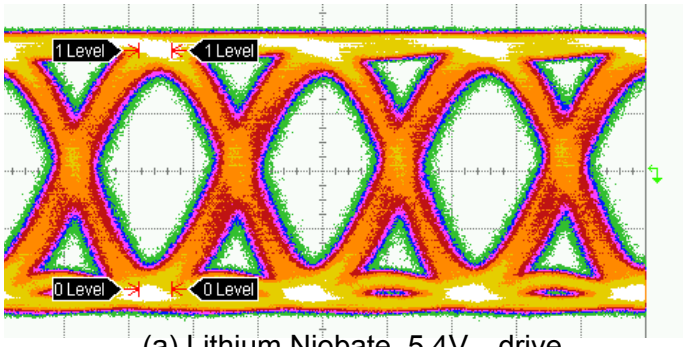
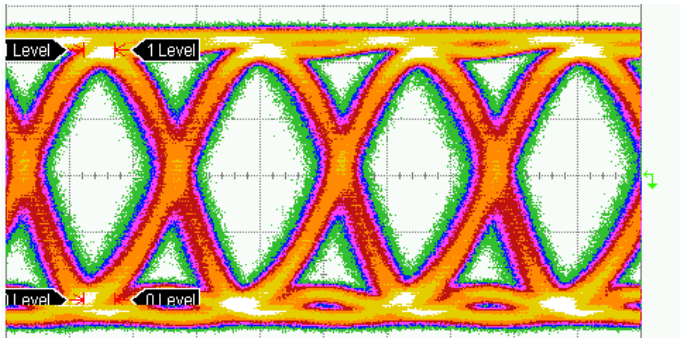


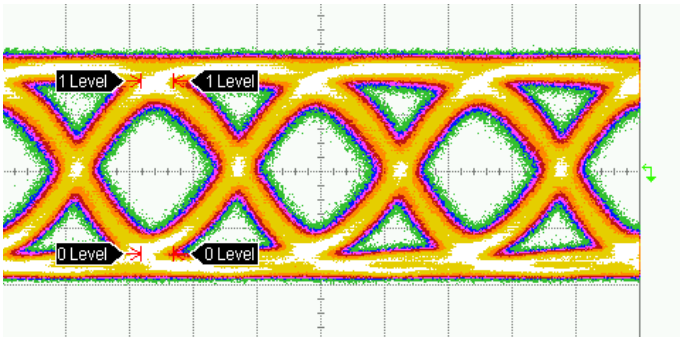

Figure 3.15: (a) Experiment setup for BER and eye-diagram measurements (PPG: pulse pattern generator, OSA: optical spectrum analyzer, VOA: variable optical attenuator, ASE: amplified spontaneous emission). (b) BER versus OSNR.




(a) Lithium Niobate, 5.4$V_{pp}$ drive




(b) Si TWMZ, 4.8$V_{pp}$ dual drive




(c) Si TWMZ, 1.6$V_{pp}$ dual drive

Figure 3.16: Error-free (BER < 1e-12) 40 Gb/s eye diagrams taken during the BER measurement: (a)Lithium Niobate modulator under 5.4 $V_{pp}$ drive (b) Si TWMZ modulator under 4.8 $V_{pp}$ differential drive (c) Si TWMZ modulator under 1.6 $V_{pp}$ differential drive

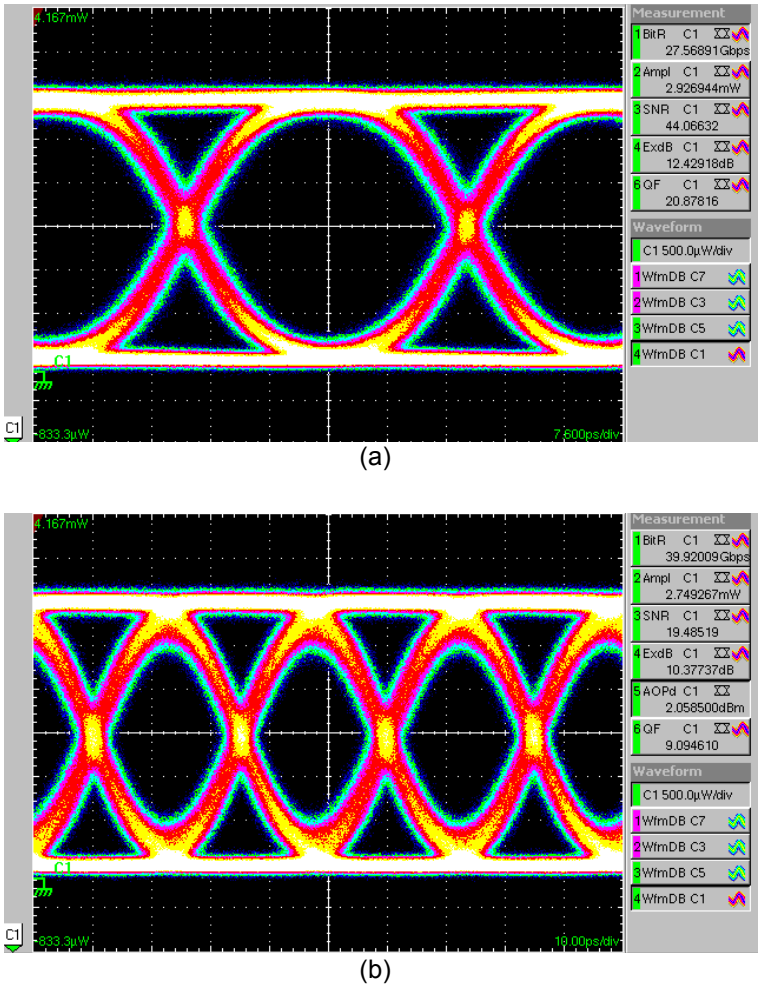



Figure 3.17: Si TWMZ extinction measurement using DC-coupled optical module (a) 12.4 dB extinction at 28 Gb/s and 10 dB extinction at 40 Gb/s

### *3.4 High-speed ring modulators at 1310 nm wavelength*

The 1310 nm wavelength band is of particular interest to data communications, owing to its capability of working beyond the dispersion limit at high bit-rate over considerably long distance. One of the critical components in this data communication is the modulator. Very recently, National University of Singapore reported a 50 Gb/s traveling wave Mach-Zehnder (TWMZ) modulator near 1300 nm [44].

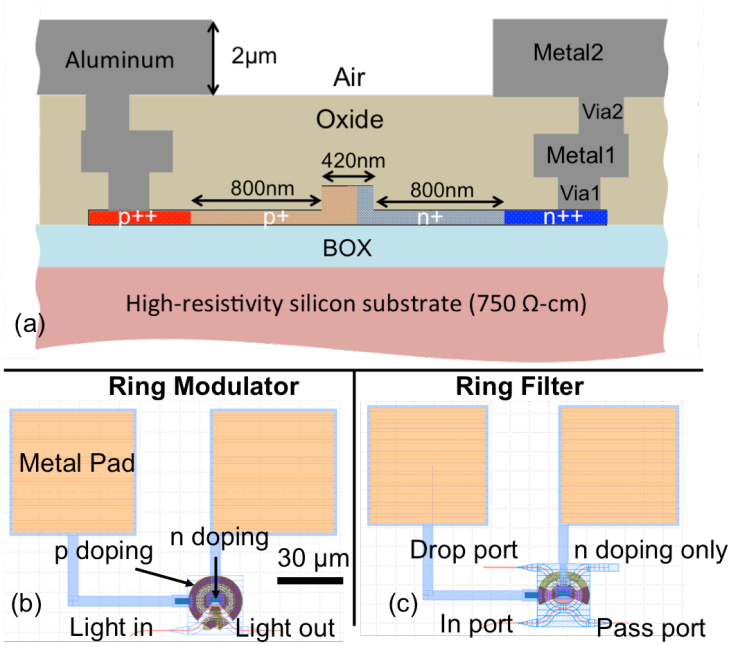



Figure 3.18: (a) Schematic cross sectional diagram of ring modulator, not to scale. (b) Micrograph of ring modulator.

Ring-resonator-based devices have become a powerful tool for a variety of applications in silicon photonics links, such as signal modulation, switching and filtering. Much progress has been made in the past 10 years in silicon ring resonator modulators and filters [57–60]. Compared to TWMZ modulators, ring resonator based silicon modulators produce much better performance in low power consumption, high modulation efficiency, small footprint and high speed due its small capacitance and compact size. However, to the best of our

knowledge, all the ring resonator modulators that have been reported are working near 1550 nm band.

In this section, we report a high-speed silicon microring modulator near 1310 nm with 3 dB bandwidth of 40 GHz. A highly efficient (253 pm/mW) ring filter near 1300nm is also present here to serve as tunable filter for wavelength division multiplexing (WDM) transmitter designs.

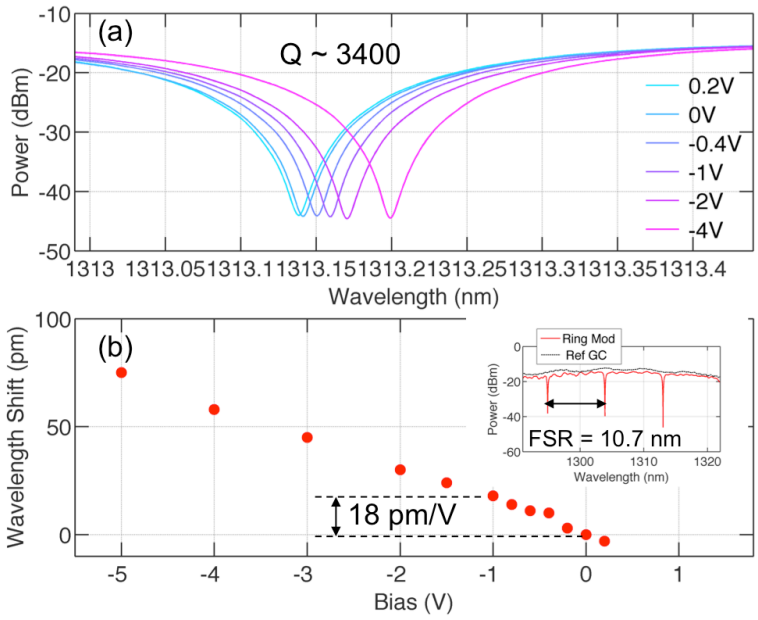



Figure 3.19: pn-junction tunability measurement of ring modulator. Inset shows the FSR and insertion loss with respect to a reference grating coupler.

Fig. 3.18(a) illustrates the cross-section of the pn junction design with key dimensions noted. The device fabrication was at the Institute of Microelectronics (IME), A*STAR, Singapore, through an OpSIS-multi-project-wafer run. The fabrication process was similar to that of [44]. The junction formed on striploaded ridge waveguide with a slab thickness of 90 nm and ridge height of 220nm. The width of the ridge is 420nm. The pn junction is slightly shifted from the center of waveguide to achieve higher efficiency. Fig. 3.18(b)

shows the schematic of the ring modulator design with n-doping at the center, surround by p-doping. In Fig. 3.18(c), filter is only filled with n-doping to form a thermal tuning resistor.

To achieve high modulation bandwidth and efficiency, Quality (Q-) factor and extinction ratio (ER) are two check-and-balance parameters. High photon lifetime-limited bandwidth requires low Q-factor at the cost of reducing modulation efficiency. In our design, we use a symmetric directional coupler to couple light in/out of ring resonators with 2 $\mu$m coupling length and 0.25 $\mu$m coupling separation. As shown in Fig. 3.19(a), the Q-factor was measured to ~3400 while the ER remains >30 dB. The photon lifetime-limited bandwidth is thus as high as 67 GHz.

The ring modulator's resonance shift was investigated with tuning DC bias voltages varying from 0.2V to -5V. The pn-junction tenability is 18 pm/V at small bias voltage, as seen in Fig. 3.19(b). The radius of ring resonator is 6.83 $\mu$m, resulting a free spectrum range (FSR) of 10.7 nm. The insertion loss of the device after doping is  1dB, characterized by measuring a reference grating coupling pair spectrum nearby, as seen in inset of Fig. 3.19(b).

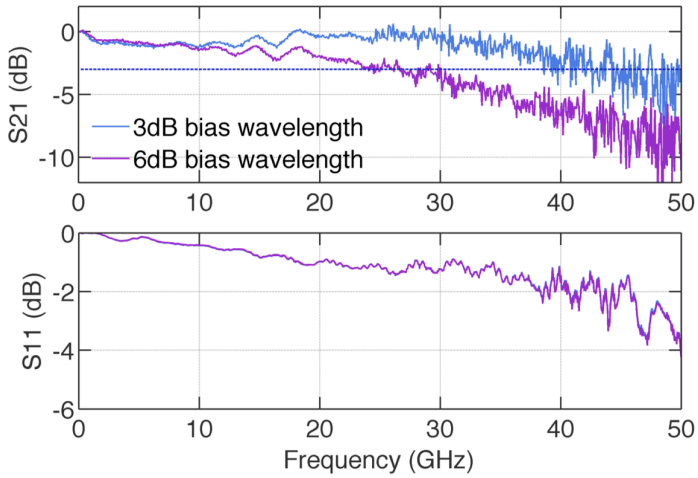



Figure 3.20: EO S-parameter measurement.

The electro-optical (EO) modulation bandwidth was characterized by S-parameter measurement, calibrated from 100MHz to 50 GHz (Fig. 3.20). Since photons with wavelength closer to the resonance will be trapped in the ring resonator longer, the EO bandwidth of

microring is highly dependent on the operation bandwidth [61]. A single EO bandwidth without reporting which operation wavelength is of no important value in estimating data transmission speed. The operation wavelength can be defined in terms of power drop-off with respect the off-resonance power. For example, 3dB wavelength means the power at this operation wavelength is 3dB smaller than the off-resonance power.

Here we present in Fig. 3.20(a) the measured EO S21 at -1V DC bias. The 3-dB bandwidth was measured to be 40 GHz when operating at 3dB wavelength and 28 GHz at 6-dB wavelength. The device is estimated to be workable at 40 Gbps and higher.

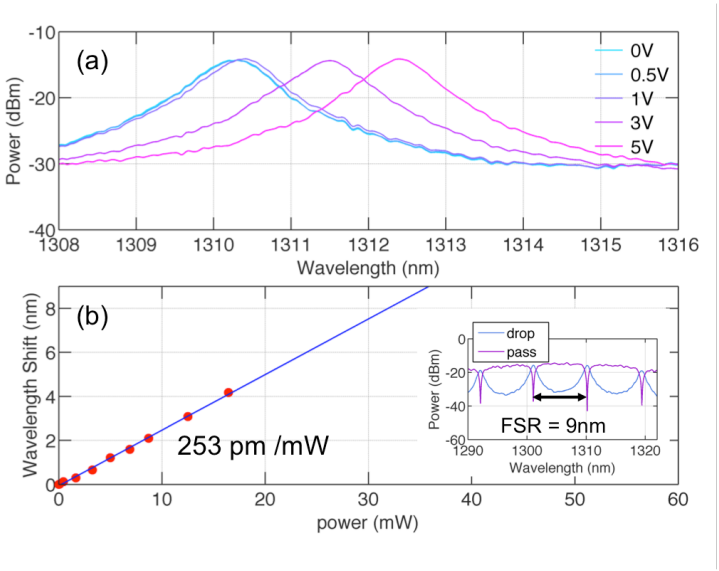



Figure 3.21: Thermal tunability measurement of ring filter. Inset shows FSR and filter spectra of drop port and pass port.

The ring resonator can act as filter when the drop port is utilized to pick out the demanded signal at a certain wavelength. We use similar ring resonator structures but with only n+ doping to form a high efficient thermal tuner. Spectra of drop port were shown in Fig. 3.21(a) when tuned from 0V to 5V. The fitted thermal tenability is 253 pm/mW in Fig. 3.21(b). Only 38 mW is need to tune a full FSR of 9 nm. As seen in inset of Fig. 3.21(b), the drop port shows almost no loss at resonance. Q-factor of the pass port is ∼1300.

We demonstrated, to the best of our knowledge, the first high-speed silicon microring modulators near 1310 nm. The device shows 40 GHz and 28 GHz EO bandwidth at 3-dB and 6-dB operation wavelengths, respectively. Combined with a high efficient ring filter that is also presented in this paper, our design can be used to build ultra-compact on-chip silicon photonic WDM transmitters for O-band telecommunications.

### *3.5 Modulator comparison in mid-reach fiber transmission*

The scaling of modern data centers calls for an economic and generic solution for both short-reach ($<$ 300m) and mid-reach ($\sim$2 km) optical interconnects. While the short-reach links remain to be bulk of the optical interconnect opportunity in the data center, modern data centers have grown to the point where $\sim$2 km reach is necessary to enable new data-center inter-link architectures and applications. The mid-reach requirement is unlikely to be met with existing technologies using VCSELs and multi-mode fibers, especially when the channel data rate scales towards 40 Gb/s [62–64]. The goal of this work is to demonstrate that silicon photonic modulators can be used at data rates up to 40G – even in the higher-dispersion C-band – over multi kilometer links with minimal penalty. At 1310 nm, the link performance will only improve, due to the lack of dispersion in the fiber.

Both the slow wave traveling Wave Mach-Zehnder (TWMZ) and microring modulator discussed here are fabricated at the Institute of Microelectronics (IME)/ASTAR via OpSIS multi-project-wafer run.

The traveling-wave Mach-Zehnder modulator under study (Fig. 3.22) is designed with slow-wave electrode to achieve 50-$\Omega$ impedance with low RF loss. Periodical velocity matching is implemented to ensure overall phase matching between RF and optical wave. Center ground shield and lateral ground connections are implemented to ensure RF single-mode operation and minimal RF crosstalk between device arms. The 3.5-mm device we report shows an EO 3-dB bandwidth of 27 GHz at -1 V bias, sufficient for 40 Gb/s operation. 5.5 V voltage on each arm differentially achieves a $\pi$ phase shift (i.e. full extinction). Between -1 V and 0 V the small-signal V$\pi$ is 7.8 V, which is a useful metric to estimate phase shift and extinction at low drive voltages.

The microring modulators (Fig. 3.23) were built with stirploaded waveguides with 500

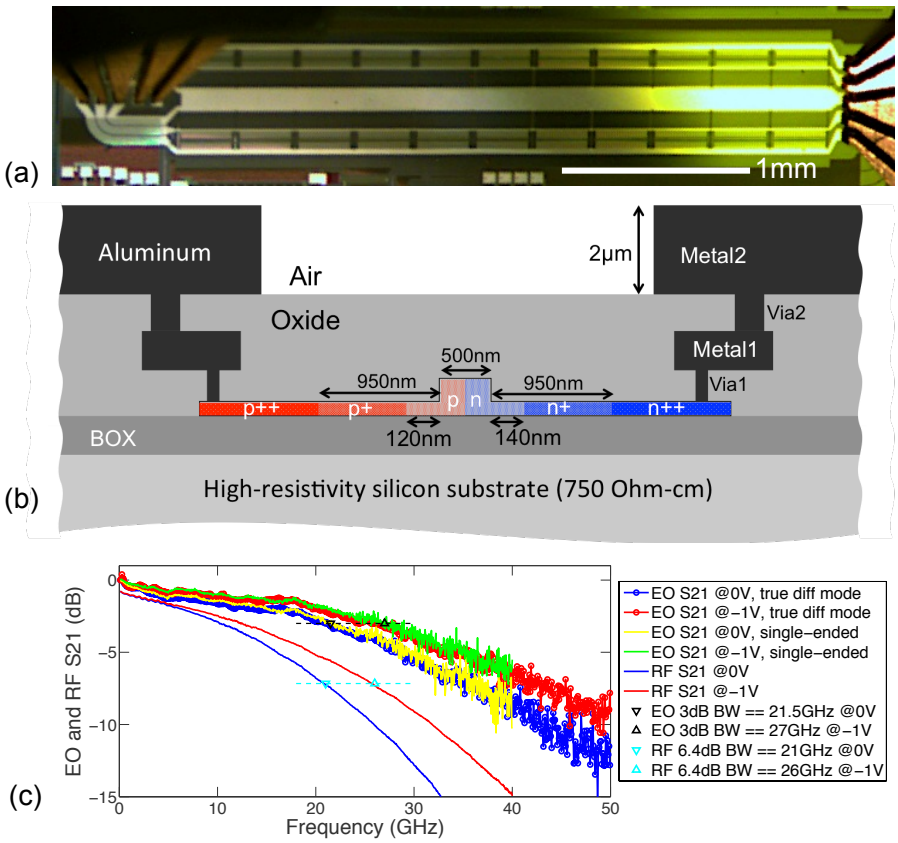



Figure 3.22: (a) Fabricated TWMZ under probed testing: GSGSG probe on the right is for driving, and GSGSG probe on the left is for providing 50Ω termination to each device arm (b) simplified cross sectional diagram of the phase shifter, not to scale (c) EO and RF S21 at 0 V and -1 V bias.

nm core width and 90 nm slab height. A small radius of 8 um was used to enable a relatively large FSR of 12 nm, which is more favorable for WDM applications, and at the same time a minimal capacitance estimated to be 25 fF. A lateral pn junction with $2 \times 10^{18}$ doping level loaded approximately 75% of the ring perimeter, enabling a high tunability of 22 pm/V. 20% of the ring circumference is only n typed doped to form an integrated heater. EO 3-dB bandwidth of the microring modulator was measured to be 25GHz when the operation point has 6-dB bias loss with respect to the maximum transmission.

The data transmission performance of silicon TWMZ and microring modulators was

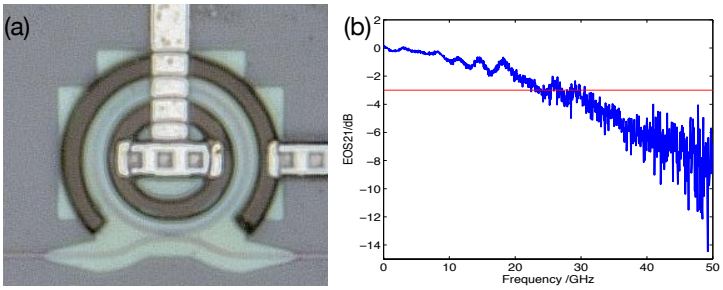



Figure 3.23: (a) Fabricated microring modulator: (b) EO and RF S21 at 6dB bias loss.

characterized using a setup shown in Fig. 3.24(a). A CW tunable laser was coupled onto silicon chip, modulated by TWMZ/microring modulator, and mixed with an amplified spontaneous emission (ASE) source with tunable power. The mixed optical signal passed through a standard SM28 fiber and amplified by an Erbium doped fiber amplifier followed by an optical band pass filter with 5nm bandwidth. Part of the optical signal is connected to an optical spectrum analyzer (OSA) for optical signal to noise ratio (OSNR) monitoring and the other part is directed to a u2t DPRV 2022A receiver with differential outputs, enabling simultaneous recording of eye diagram and BER.

The 40 Gb/s NRZ PRBS $2^{31}$-1 data stream we used to drive the modulators were obtained by electrically multiplexing 4 copies of de-correlated 10 Gb/s NRZ PRBS steams. The signal was then amplified and attenuated to desired amplitude, before launched to silicon modulators via RF probes. For TWMZ, we used a differential signal with 1.6 Vpp and 1.5 V reverse bias to drive both arms of the modulator, while the far end of the modulator was terminated with 50 Ω resistor. For microring modulators, a RF driving signal with 2.7 Vpp and 1.1V reverse bias was launched via a GS probe with inline 50 Ω termination, in order to reduce the RF reflection.

Fig. 3.24(b) and (c) shows the typical eye diagram and BER curve for back-to-back, 2km, and 5km SM fiber propagation on TWMZ and microring modulators. With the driving condition described above, 3dB extinction ratio on microring and 4dB extinction ratio on TWMZ was achieved. We did not observed noticeable single degradation after 2km fiber propagation on both types of silicon modulators (OSNR penalty <1 dB). After propagation

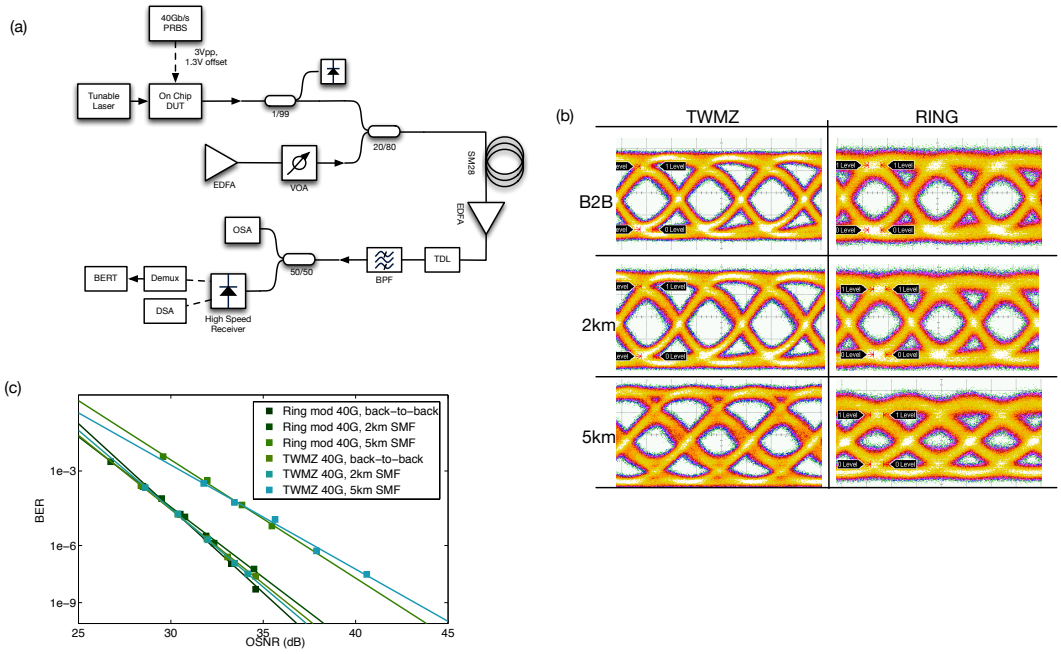



Figure 3.24: (a) Setup for data transmission characterization : (b) Typical eye diagram for back-to-back, 2km and 5km fiber propagation on TWMZ and ring modulator. (c) BER vs OSNR for both types of modulators

through 5km SM fiber, severe distortion was observed on the optical signal, and the OSNR penalty is about 6dB comparing to the back-to-back case.

# Chapter 4

# OPTICAL TRANSCEIVERS IN A SILICON PLATFORM

This chapter first describes a silicon photonics platform that I helped develop in OpSIS project. In this platform, high-performance passive optics components, high-speed modulators and detectors are monolithically integrated and a relatively complete photonics device library is made available to the research community in the form of a maintained PDK (similar to what is been done in electronics) to finally enable system-level designs. The second part of this chapter discusses in detail a 320-Gb/s and a 160-Gb/s wavelength-division multiplexing (WDM) transmitter as well as highlight several other transmitters and receivers and I design and implemented in this platform.

## *4.1 OpSIS-IME monolithic silicon photonics platform development*

### *4.1.1 Monolithic silicon photonics platform for 25 Gb/s*

#### *4.1.1.1 Introduction*

Silicon has attracted attention as an inexpensive and scalable material system for photonic-electronic [9, 65] system-on-chip development. For this, a platform with both photodetectors and modulators working at high speeds, with excellent cross-wafer uniformity, is needed [66–68]. The ideal platform will also be based on optical lithography for wafer-scale fabrication, and demonstrate high speed, low cross-wafer variability and low defectivity rates. Here we report a new wafer-scale silicon photonics platform with integrated modulators and photodetectors demonstrating 15 GHz bandwidths and higher, as well as 25 Gb/s operation. We demonstrate modulation with an ultra-low drive voltage of 1 $V_{pp}$ at 25 Gb/s, the first published example of a 25 Gb/s modulator directly compatible with typical CMOS transistor voltages. We demonstrate attractive cross-wafer uniformity, and provide detailed information about the device geometry. Our platform is available to the community as part of a photonics shuttle service [69].

The first multi-Gb/s capable silicon photonics modulator was reported by Liu et al in 2004 [18]. Since then, silicon photonics has seen an explosion of interest, with low-loss waveguides [70], detectors [71], and grating couplers [72] all separately demonstrated. A challenge has been the development of a platform that supports all of these key components simultaneously with attractive performance, and achieves drive voltages compatible with CMOS processes. Luxtera demonstrated a photonics platform with both integrated modulators and detectors at 10 Gb/s in 2006 [27]. Luxtera has since announced 25 Gb/s capability and recently reported a 4 $\times$ 28G link, though the technical details remain unpublished, and key device geometries and performance characteristics have been kept a trade secret. Kotura has achieved 40 Gb/s for various devices [73], but has not reported a common platform with both high-speed modulators and detectors on the same wafer, at the same time. Intel and IBM have reported individual high-performance devices [74, 75]. Meanwhile, ePIXfab has been providing fabrication services to the photonics community [18], and has published results on modulators and detectors at 40 Gb/s speeds separately [34, 76], though not on results achieved simultaneously as part of an integrated platform. Kim et al have recently demonstrated both modulators and detectors working at speeds of 30 Gb/s [68]; however, the on-chip drive voltage required for the modulator was 2.4 $V_{pp}$, and additionally, a 5 V DC bias was required for 15 GHz+ bandwidths, which will hamper integration with advanced CMOS circuits. Wafer-scale defectivity and performance data was also not provided for any of the devices in question, making it unclear how suitable this platform will be for large scale photonic integration.

Silicon is not the only viable integrated photonics platform. For example, Infinera has been pursuing photonics integration in III-V systems, with 45.6 Gb/s speeds achieved [77]. Devices in III-V systems have traditionally enjoyed performance advantages compared to silicon. Traditional semiconductor light sources are impossible in silicon, while III-V lasers are in wide use, and III-V based modulators enjoy better performance [78] than state-of-the-art silicon devices. This is similar to the electronics industry; typically non-silicon platforms have superior performance. Silicon has become dominant due to low cost and high yield, which have enabled integrated systems of unparalleled complexity to be constructed [79]. To realize these benefits in the photonics community, a high-speed and low-defectivity wafer-

scale platform is necessary.

*4.1.1.2 Fabrication*

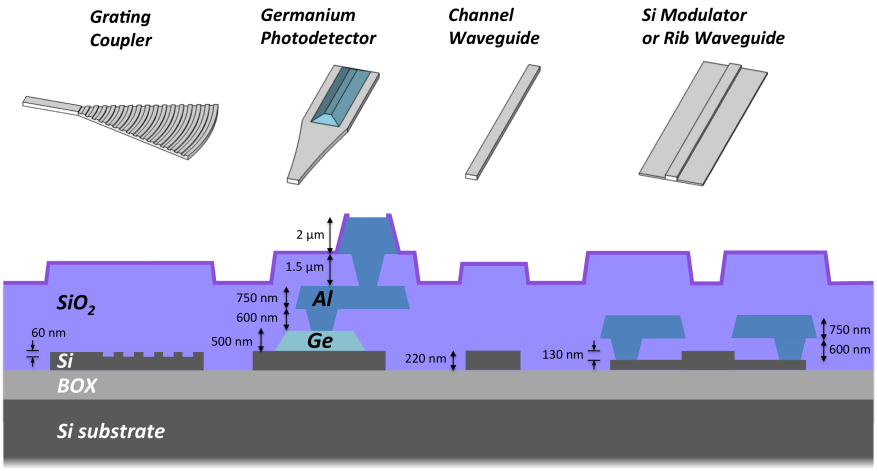



Figure 4.1: Platform geometry. A diagram of the cross-sections of key devices is shown, as well as layer thicknesses. The platform features a 220 nm top silicon layer that has three possible etch depths, an epitaxially grown Ge layer, and two metal layers for electronic routing.

Fabrication for this work occurred at the Institute of Microelectronics (IME) / A*STAR. The starting material was an 8-inch Silicon-on-Insulator (SOI) wafer from SOITEC, with a Boron-doped top silicon layer of around 10 Ω-cm resistivity and 220 nm thickness, a 2 $\mu$m bottom oxide thickness, and a 750 Ω-cm handle silicon wafer, needed for RF performance. A 60 nm anisotropic dry etch was first applied to form the trenches of the grating couplers. Next, the rib and channel waveguides were formed using additional etch steps. In all cases 248 nm photolithography was utilized. The p++, p, n++, and n implants for the Si modulator and the p-type doping for anode formation of the Ge p-i-n photodetectors were performed on the exposed silicon, prior to any oxide fill. This was followed by a rapid thermal anneal at 1030 degree Celsius for 5 s for Si dopant activation. Ge was then selectively grown to a thickness of 500 nm [11] in regions defined by a deposited SiO2 mask layer. Ion implantation

was performed for the Ge regions and annealed at 500 degree Celsius for 5 min, followed by the formation of contact vias and two levels of aluminum interconnects. Chemical-mechanical planarization (CMP) was not utilized. The schematic cross-section is shown in Fig. 4.1. Excluding edge dies, 41 dies of overall size 25 x 16 mm were fabricated per wafer. All results reported are from a single wafer.

Implant recipes were chosen to give peak doping concentrations of approximately $7 \times 10^{17}\,\mathrm{cm}^{-3}$ for the p doping regions, $1.7 \times 10^{20}\,\mathrm{cm}^{-3}$ for the p++ doping region, $5 \times 10^{17}\,\mathrm{cm}^{-3}$ for the n doping concentration, and $5 \times 10^{20}\,\mathrm{cm}^{-3}$ for the n++ doping concentration. The sheet resistances were measured to be $10\,\mathrm{k}\Omega/\square$, $100\,\Omega/\square$, $7\,\mathrm{k}\Omega/\square$, and $58\,\Omega/\square$, respectively. These values are for the resistance in the partially etched silicon regions.

#### *4.1.1.3 Waveguides*

All test results reported here were obtained using a wafer-scale, normal incidence opto-electronic test setup. Fiber-coupling was achieved with grating couplers [72]. The average grating coupler insertion loss across 19 dies was determined to be 4.4 ± 0.2 dB, with a peak wavelength near 1545 nm and a typical 1.5 dB bandwidth of 45 nm. The typical on-chip return loss from the grating couplers was -12.5 dB. The defectivity rate for characterization loops was 5%, out of 657 devices tested. The period and size used for the trenches was 630 nm and 220 nm, respectively. Cross-wafer data is shown in Ω. Waveguide losses of 1.0 ± 0.3 dB/cm were achieved in the best die measured for 0.5 $\mu$m wide rib waveguides with 220 nm thickness, with low cross-wafer variation as shown in Fig. 4.4. The average waveguide loss was 2.2 ± 0.8 dB/cm from 19 dies measured. For channel waveguides with 0.5 $\mu$m dimensions, losses of 2.4 ± 0.3 dB/cm were obtained from these dies. On the worst-performing dies, losses were 3.4 ± 0.2 dB/cm for the rib waveguide, while worst-case losses of 3.1 ± 0.1 dB/cm were seen for the channel waveguide.

#### *4.1.1.4 Traveling-wave Modulators*

Traveling-wave modulators were constructed [28], based on a lateral pn-junction waveguide with coplanar metal strips, with a GS configuration utilized. The device length was 3 mm, while each arm had an independent GS transmission line drive. Each GS line was predicted to have an impedance of around 33 Ω, consistent with the measured S11 values. A lower

impedance assists velocity-matching and lowers RF losses [16]. Termination was achieved with two 50 Ω lines, via a GSSG probe. As will be detailed later, a test pattern of 9 dies was used. Fig. 4.2 shows the device layout. The average cross-wafer modulator insertion loss, excluding known losses from the grating coupler and routing waveguides, was 6.2 ± 0.5 dB. The device was intentionally unbalanced by a waveguide length of 100 $\mu$m, to enable biasing of the modulator by tuning the input wavelength. A slight asymmetry in response was observed between the two arms. We characterize the voltage required for a phase shift of $\pi/2$ radians, due to the well-known nonlinear electrooptic response of reverse-biased pn junctions, as shown in Ω. The cross-wafer average $V_\pi/2$ value for the lower arm was 7.2 ± 1.3 V and 5.3 ± 0.2 V for the upper arm.

Average cross-wafer 3 dB bandwidths at 0 V bias were 15.5 ± 0.2 GHz for the lower arm, and 17.6 ± 0.8 GHz for the upper arm. The cross-wafer variation of some key parameters is shown in Fig. 4.4. Eye-patterns were taken with differential drive at 25 Gb/s, utilizing a pseudo-random bit sequence. An extinction of 4.4 dB was obtained with a 1 $V_{pp}$ signal, as shown in Fig. 4.3. The drive signal was centered at 0 V. We note that even for small forward biases, forward diode current remained minimal due to the built-in voltage of the junction. For this particular Mach-Zehnder device, a lower arm $V_\pi/2$ of 6.8 V and upper arm $V_\pi/2$ of 5.5 V was measured. At 0 V bias, the typical capacitance of the lateral pn junction was found to be 0.3 fF/$\mu$m. For the typical separations of 1.05 $\mu$m between the n++ and p++ doping and the unetched ridge, intrinsic junction bandwidths of 31 GHz should be possible based on measurements of the relevant sheet resistances. Because the modulator had impedance lower than 50 Ω, the true on-chip voltage was in fact slightly lower than 1 $V_{pp}$.

#### *4.1.1.5 Ring Modulators*

Dual-bus ring modulators, with a 30 $\mu$m radius and a lateral PN junction centered in a rib waveguide were tested in an expanded set of 13 dies (see later section on wafer test patterns). The ring FSR was around 3.2 nm, and a typical Q was 7,000. An average cross-wafer tunability of 10.6 ± 1.2 pm/V was determined by measuring resonance shift as bias voltage varied from -200 mV to 200 mV. Ring bandwidth was measured at 0 V dc bias. The

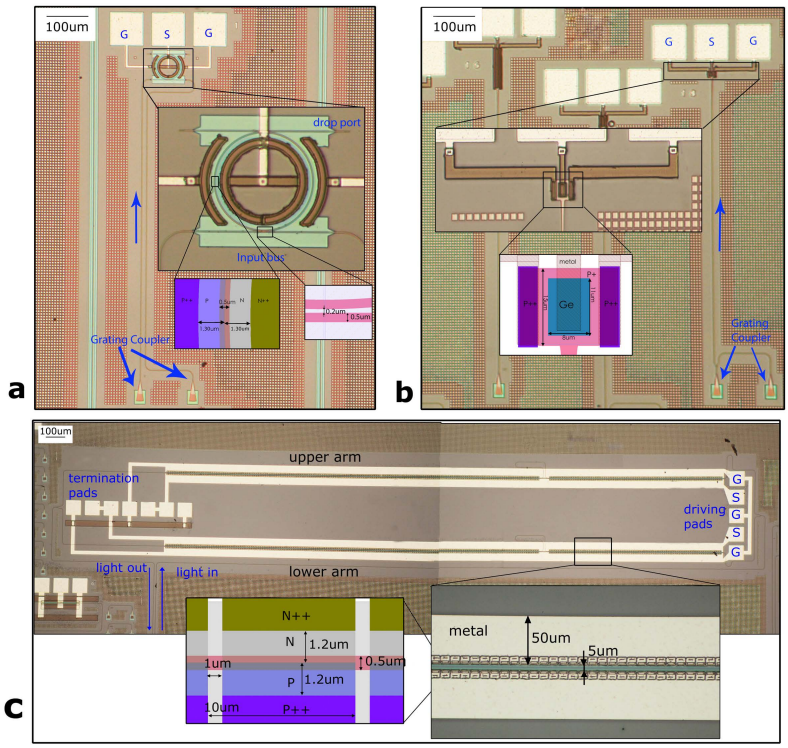



Figure 4.2: Device layout. (a) Optical micrographs of the ring modulator device. Note that the insets with the highest magnification are renderings of the mask layout, instead of micrographs. (b) Optical micrographs of the Ge detector device. Again, the highest magnification insets are renderings of the mask layout. (c) Optical micrographs of the 3 mm traveling-wave Mach-Zehnder modulator.

average bandwidth was 18.7 ± 0.1 GHz, as shown in Fig. 4.4. No defective ring modulators or photodetectors were encountered during test.

#### *4.1.1.6 Photodetectors*

Photodetectors were constructed with vertical Germanium PIN junctions, as shown in Fig. 4.1. Devices were 11 $\mu$m long, 8 $\mu$m wide, as shown in Fig. 4.2. Average on-chip responsivities of 0.54 ± 0.05 A/W with dark currents of 4.8 ± 0.4 $\mu$A were achieved at 4 V reverse-bias. RF testing was also performed, with devices showing average cross-wafer 3 dB bandwidths of

20.2 ± 1.4 GHz, indicated in Fig. 4.4 and Fig. 4.3. The bandwidth was determined from the S21 parameter of a vector-network analyzer driving an external modulator. Several devices were tested at lower reverse-bias voltage as well; one detector exhibited bandwidth of 20 GHz with 2 V reverse-bias, as shown in Fig. 4.3. A dark current of 1.2 $\mu$A and responsivity of 0.46 A/W was measured. One detector was characterized for nonlinearity and the damage threshold, which was 15 mW of on-chip optical power. The detector exhibited a 14% deviation from linear responsivity at 7.8 mW input power. An eye pattern is shown at 25 Gb/s in Fig. 4.3. Typical detector capacitance was measured at 4 V reverse-bias to be 0.5 fF/$\mu$m$^2$, or 44 fF.

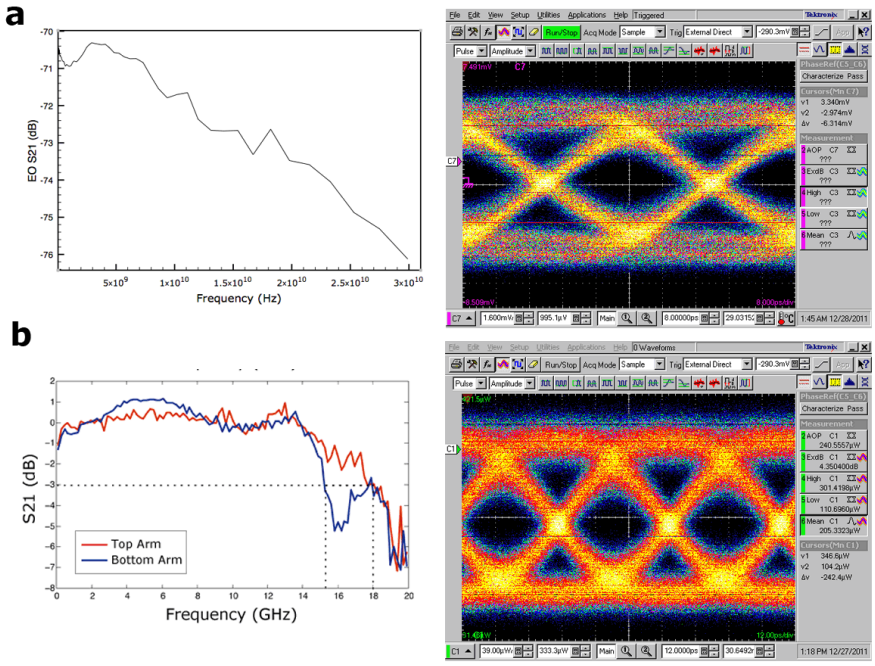



Figure 4.3: Traveling-wave Modulator and Detector Performance. (a) The electrooptic (EO) S21 of a typical photodetector with 2 V reverse-bias, as well as an eye pattern at 25 Gb/s. The 3 dB rolloff is at 20 GHz. (b) The EO S21 traces of a typical traveling-wave Mach-Zehnder device are shown, as well as an eye pattern produced by a differential drive signal of 1 $V_{pp}$ at 25 Gb/s. 4.4 dB of extinction is achieved. 5.5 dB of excess loss in addition to the intrinsic device loss is seen on the modulator for a "1" bit, due to the device bias point.

#### *4.1.1.7 Conclusion*

To conclude, we have demonstrated a wafer-scale silicon photonics platform that achieves 15 GHz bandwidths, and is capable of 25 Gb/s data rates. We provide precise fabrication details and device geometries, which should enable other users of this platform to fully leverage our results in designing integrated photonic-electronic systems-on-chip, and in developing their own fully integrated processes.

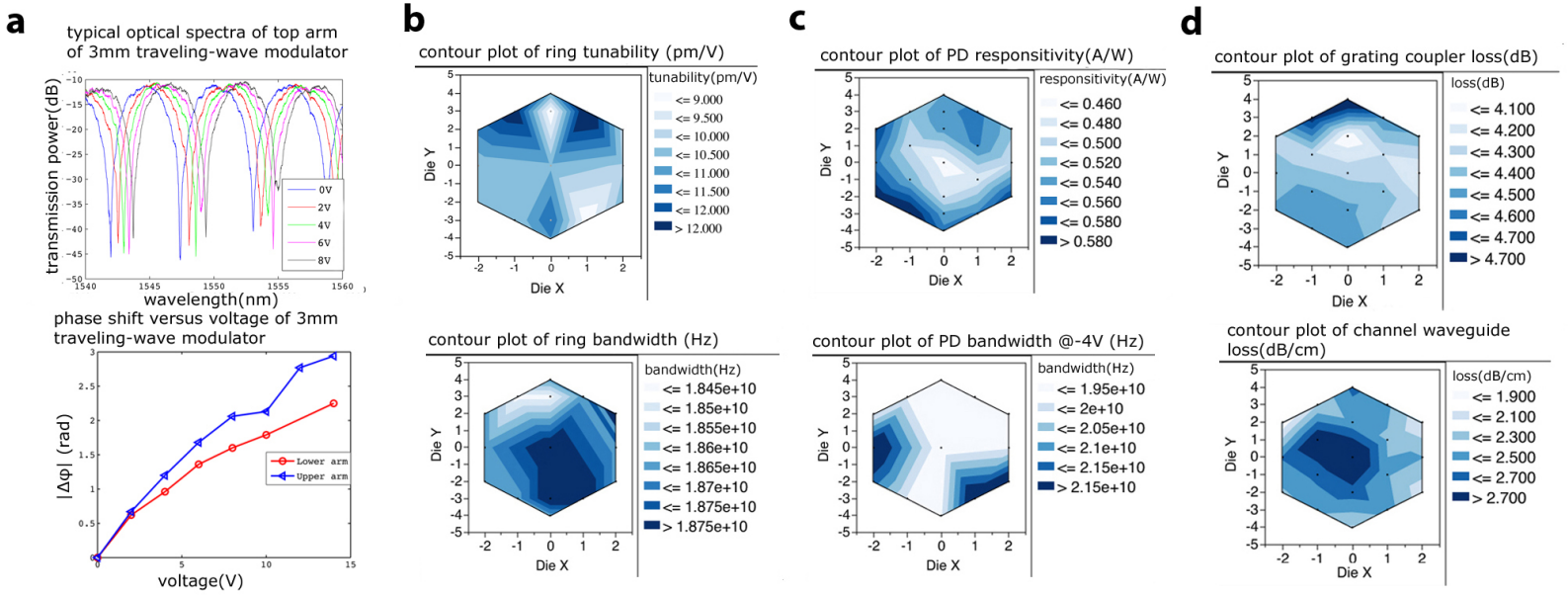



Figure 4.4: Cross-wafer data. (a) The performance of the traveling-wave Mach-Zehnder is shown. Typical specta with varying applied reverse-bias voltage is shown, as well as phase shift as a function of bias voltage. (b) The performance of the ring modulator across the wafer is shown, with both tunability and bandwidth reported. (c) Ge Photodetector responsivity is also shown, as well as bandwidth with a 4 V reverse-bias. (d) Grating coupler performance is shown, as well as the cross-wafer variation in channel waveguide loss

### *4.1.2 Extending platform capability to 40 Gb/s and beyond*

We continue to develop this process and showed 40–50 Gb/s operation in newly developed ring modulators, TWMZ modulators and photodetectors. The high-speed ring and TWMZ modulators are discussed in detail in Chapter 3. In this section these devices are briefly overviewed and highlighted. In the next sections, I will show a few systems with 40 Gb/s channel rate as a result of this exciting new development.

#### *4.1.2.1 58-GHz bandwidth inductive-peaked photodetector*

Photodetectors (PD) were constructed with vertical Germanium p-i-n diodes. A spiral metal inductor in series with the diode was employed to improve the bandwidth. An average responsivity of 0.7 A/W was achieved at 2 V reverse bias, with 5 $\mu$A dark current. To characterize the RF performance of the detector, we used a vector network analyzer (VNA) to drive a high-speed Lithium Niobate (LiNbO3) modulator, and detect the electrical output from the PD. The EO response of the modulator was calibrated by an ultrafast commercial photodetector whose bandwidth was larger than 70 GHz, and was normalized out in our PD measurement. Using this methodology, the 3 dB bandwidth of our PD is measured to be 58 GHz when 2 V reverse bias was applied as shown in Fig. 4.5.

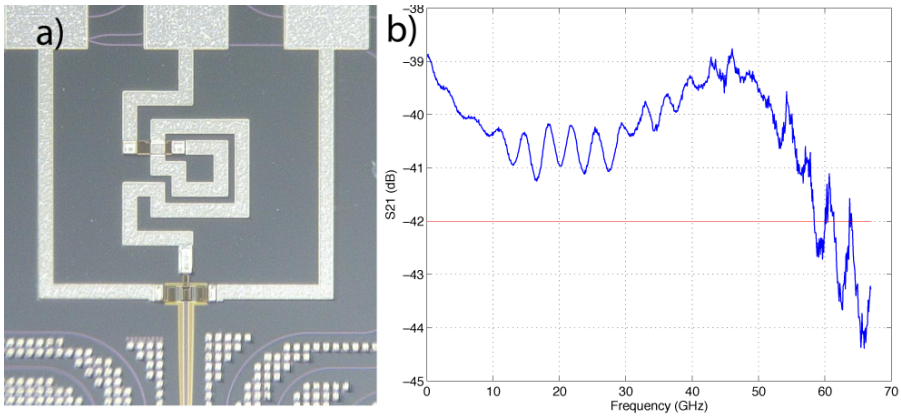



Figure 4.5: Image of inductive peaking PD. b: EO response of inductive peaking PD, 58-GHz bandwidth was achieved

#### *4.1.2.2 30-GHz bandwidth traveling-wave modulator*

Traveling wave Mach-Zehnder modulators with 3 mm active lengths were built based on a lateral PN-junction waveguide phase shifter and metal GS transmission line electrodes with 33 Ω impedance. The p+ and n+ doping in silicon were used to reduce the parasitic resistance from the silicon slab. The on chip insertion loss, excluding known loss from routing waveguide, is measured to be 7 dB. The two arms are intentionally unbalanced by 100 um in order to conveniently set the bias point by choosing the input wavelength. By applying a DC bias voltage and calculating the spectrum shift, the small signal $V_\pi$ on both arms were measured to be 7 V around 0 V bias. The RF performances of the top and bottom arm were characterized individually. During the measurement, the top (or bottom) arm was driven by VNA port and terminated by 25 Ω terminator, while bottom (or top) arm was terminated by 50 Ω in the driving end and 25 Ω in the termination end. By this means, the 3 dB bandwidth of both arms achieved 30 GHz under 1 V DC bias. 50 Gb/s modulation with 5 dB ER can be produced when the modulator was driven differentially from a 50 Ω pattern generator with 2 $V_{pp}$ NRZ signal centered at 1 V, and the "1" bit biased to have 3 dB modulation loss.

#### *4.1.2.3 45-GHz bandwidth ring modulator*

The tunability and bandwidth of a ring modulator with 12 $\mu$m radius was tested. The ring modulator was constructed by rib waveguide with 500-nm width and 90-nm slab thickness. Heavily doped PN junction with $N_a$=$1.8\times10^{18}\,cm^{-3}$ and $N_d$=$2.5\times10^{18}\,cm^{-3}$ was employed to achieve high tuning efficiency. A typical Q of 2,800 and FSR of 7.65 nm were observed. Small signal tunability of 28 pm/V was determined by measuring the spectrum shift as a function of DC bias voltage from -0.5 V to 0.5 V. The 3 dB bandwidth is measured to be 45 GHz under 0 V bias voltage, enabling 50 Gb/s data transmission. We estimated 5 dB ER can be achieved when the device was driven by 2.4 $V_{pp}$, and the "1" bit was biased to have 7 dB modulation loss.

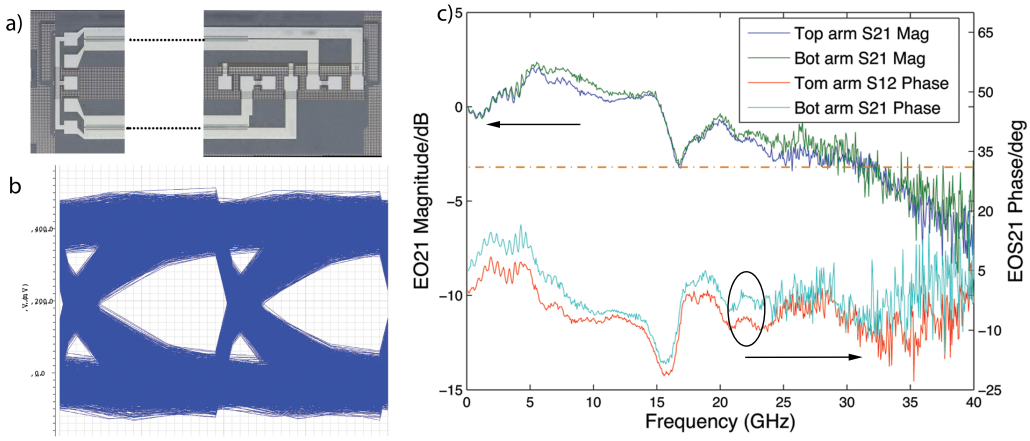



Figure 4.6: Image of the 3 mm TWMZ. b: Simulated eye diagram at 50 Gb/s based on the measured S-parameters. c: RF performance when 1-V reverse bias was applied. 30 GHz bandwidth was achieved on both arms. A slight dip is seen near 18 GHz, likely due to cross-talk between the arms, but the S21 does not drop below the 3-dB line until 30 GHz. From the phase of S21, the group delay variation is less than 4 ps up to 40 GHz.

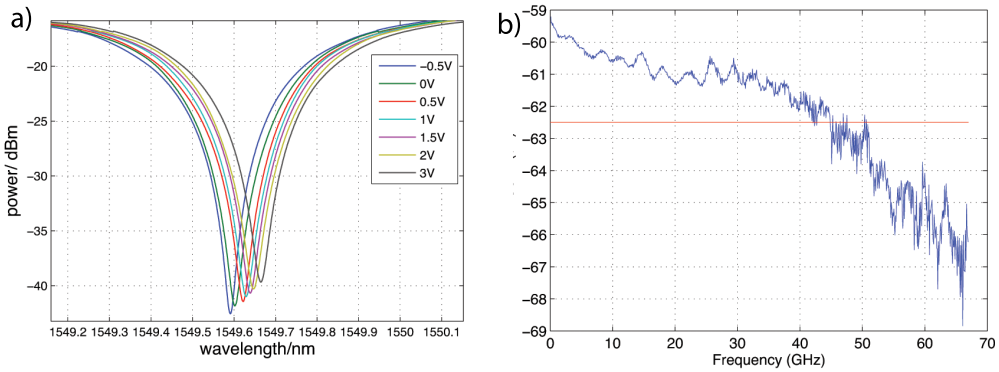



Figure 4.7: a: Shift of resonant wavelength when different bias voltage was applied. B: measured EO frequency response at 0V bias, showing 45-GHz 3-dB bandwidth

## 4.2 Ultra-compact 320-Gb/s and 160-Gb/s WDM transmitters based on silicon microrings

### 4.2.1 Introduction

Wavelength division multiplexing (WDM) system has attracted more and more interests in the past several years, for building ultra-high aggregated data rate optical network and optical interconnects. This topic has taken on more excitement given that interconnection has been considered as the bottleneck for the next-generation computing systems. Microring resonators are one of the most popular devices to form the key building blocks of on-chip network and optical interconnects, owing to small footprint, small capacitance and low power consumption. Much progress has been made in the past decade in design and demonstrating microring-based modulators, filters, switches and lasers, etc.

In this work, we present two WDM transmitters using silicon microring modulators and microring-based add-filters (multiplexers). The first design is a 320-Gb/s 8-channel WDM transmitter based on conventional common-bus architecture, which to the best of our knowledge demonstrates the highest aggregated data rate achieved in silicon transmitters. The second design is a 160-Gb/s 4-channel transmitter prototype to demonstrate the new "Mod-MUX" architecture that we propose. Both designs exhibit 32-fJ/bit modulation power efficiency and consume less than 0.04 $mm^2$ chip area excluding the driving pads.

### 4.2.2 Ring-based WDM transmitter architectures

The commonly used ring-based WDM transmitter architecture is shown in Fig. 4.8(a), where a series of ring modulators share one bus waveguide, referred to as "common-bus" architecture. This configuration does not require each ring modulator to be associated with a specific wavelength in the WDM system; instead it offers the flexibility of assigning rings to the closest wavelength so as to minimize the overall tuning power [25]. However, a comb laser or pre-multiplexed laser sources are required at the common input and cross-modulation may be introduced since the light in the bus waveguide passes through multiple ring resonator modulators [80]. It is also worth noting that automated thermal stabilization is particularly challenging in the common-bus design, due to the fact that multiple wavelengths are always

present at the bus waveguide and interact with each ring modulator but the monitoring photo detector is naturally insensitive to wavelength.

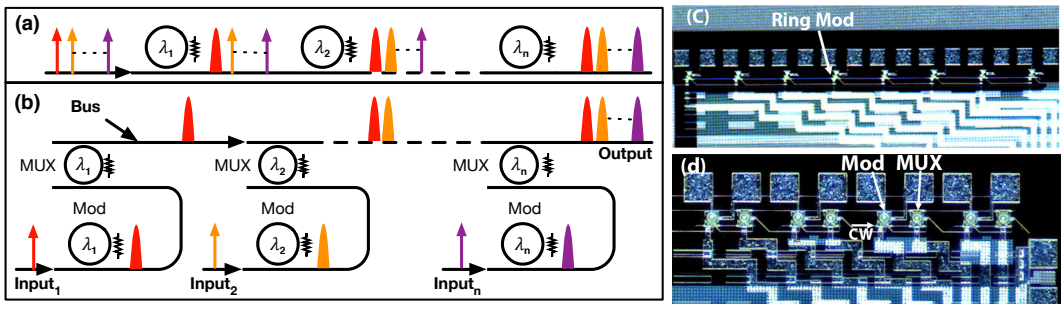



Figure 4.8: (a) schematic diagram of the common bus design, (b) schematic diagram of the Mod-MUX design, (c) photograph of fabricated 8 ring transmitter based on traditional common bus design; (d) photograph of the fabricated Mod-MUX design.

Here we propose a new architecture, referred to as "Mod-MUX" to overcome the weakness of the common-bus design. As shown in Fig. 4.8(b), in the Mod-MUX architecture the laser for each channel is first fed into a ring modulator (Mod) and then the modulated light is multiplexed onto the bus waveguide by a ring add-filter (MUX). This architecture offers several key advantages: (i) removing the requirement of comb sources; (ii) avoiding cross-modulation, due to the fact each laser only pass through one ring modulator; (iii) Mod-MUX offers compatibility to simpler thermal stabilization schemes compared to the common-bus architecture since each Mod-MUX branch operates with only one laser wavelength; (iv) specific design can be made to ring modulators and ring filters respectively to optimize the performance of each element, such as the best tunability with the maximum allowable quality factor (ring modulator) and sufficient bandwidth with low loss and low cross-talk (ring filter).

### *4.2.3 Common-bus WDM transmitter*

Both of the aforementioned designed are fabricated via an OpSIS multi-project-wafer run [54]. The common-bus design is implemented with 8 channels. The ring modulators are

formed by slab waveguide of 500 nm width, 90 nm slab height and 7.5 um radius resulting a free spectral range (FSR) of 12.8 nm. Approximately 75% of the waveguide was doped with pn junction for high-speed modulation and the tunability of the ring modulator is 28 pm/V near 0 V bias. The combination of low capacitance (∼25 fF) and intentionally lowered Q (5,000) enabled an ultra-high EO bandwidth of 35 GHz. An integrated heater with 620 Ω resistance is formed by doping 15% of the ring with n-type dopants. The thermal tunability was measured to be 150 pm/mW. The size of the rings are designed to be slightly different so that the spacing between the resonance peak of two adjacent rings is 1.6 nm, i.e. eighth of the FSR, in order to achieve cyclic operation with minimum tuning power.

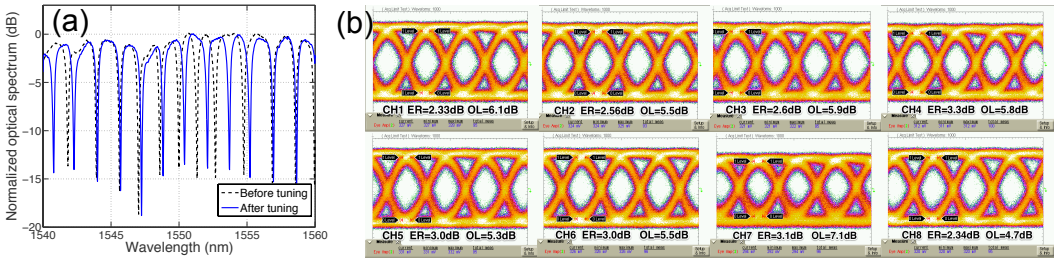



Figure 4.9: (a) 8-ring transmitter bus waveguide spectra before and after thermal tuning (b) 40-Gb/s eye diagrams of 8 channels. ER: extinction ratio. OL: on-state loss

Grating couplers are used to couple laser on and off chip. A fiber array is attached to the silicon chip making the optical coupling more stable during the test. The overall on chip insertion loss is 12 dB, including 0.9 dB from each ring modulator, and 5 dB due to unexpected high loss of 2 mm long routing waveguide covered by metal interconnects. In the test, we first tuned the 8 rings so that their resonance peaks were evenly distributed with 1.6 nm channel spacing. The overall tuning power was 17 mW. To operate each channel, a tunable CW laser was aligned to each of the resonance peaks. The modulated light was boosted by an EDFA, detected by a u2t DPRV2022A receiver module and then connected to an Agilent digital communication analyzer (DCA). A Centellax TG1P4A pattern generator followed by a Centellax modulator driver amplifier, a 6 dB RF attenuator and a 40 GHz bias tee produced a 40-Gb/s $2^{31}$-1 PRBS signal with 2.27 $V_{pp}$ centered at 0.8 V (reverse biasing

the pn junction) to drive the ring modulator. In order to avoid RF reflections, we used a 50 Ω terminated probe to contact the rings. Due to the AC coupling feature of the receiver, the extinction ratio of the eye diagram could not be measured directly by the DCA. Instead, we measured the average optical power of the modulated light, the optical power when the laser wavelength is set to off resonance, and the amplitude of the eye diagrams. The extinction ratio of the optical eye and the on-state loss were calculated off line. Clear eye opening with ∼3 dB extinction ratio and ∼6 dB on-state loss were observed on all 8 channels. The power consumption of each channel is estimated to be 32 fJ/bit.

### *4.2.4 Mod-MUX WDM transmitter*

In the Mod-MUX design, as discussed in Section 4.2.2, each ring modulator is followed by a ring add filter [57] multiplexing the ring modulator output to the bus waveguide. As shown in Fig. 4.8(d), we implemented a 4-channel prototype based on this principle and it is straightforward to scale up to higher channel count. The modulator in this transmitter is similar to those described in Section 4.2.3, except the channel spacing is now 3.2 nm. The filters are sized to align with the modulators. Thermal tuning of the filters is achieved through a 200 Ohm resistor formed by n-type doped striploaded waveguide covering 60% circumference of ring. The thermal tunability was on average 250 pm/mW. The add filter achieved <1 dB insertion loss, 0.8 nm (∼100 GHz) 3 dB bandwidth and better than -20 dB crosstalk when the channels are correctly spaced.

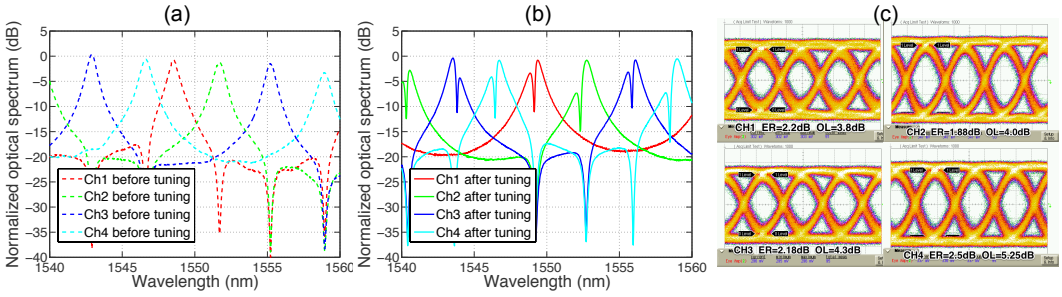



Figure 4.10: Spectra of each channel before (a) and after (b) thermal tuning; (c) 40 Gb/s eye diagrams of 4 channels. ER: extinction ratio. OL: on-state loss

The test setup assembly closely resembles that in Section 4.2.3. During testing, we monitored the optical power at the bus output when sending a tunable CW light into each input as illustrated in Fig. 4.8(b). We first tuned the filters to achieve the target channel spacing, and then tuned the modulator resonances to approximately align with the filter. The before and after tuning spectra for each channel are shown in Fig. 4.10(a) and Fig. 4.10(b) respectively. In principle the laser wavelength should be at the peak of the optical filter to minimize loss and optical filtering of the data stream, the modulator resonance should be slightly off the laser wavelength just as it is in a single ring modulator to generate desired extinction ratio. With similar setup as described in Section 4.2.3, we successfully demonstrated 40 Gb/s eye-diagrams on all 4 channels with 32 fJ/bit modulation power efficiency, as shown in Fig. 4.10(c). We observed  2 dB ER and  4 dB on-state loss with clear eye opening. We note that fine-tuning the alignment of the modulator resonance and laser wavelength was necessary in the measurement due to the drift of modulator resonance caused by RF power dissipation on the ring modulators.

### *4.2.5 Conclusion*

We demonstrated, to the best of our knowledge, silicon transmitters with the highest aggregated data rate. Two types of microring-based WDM transmitter architectures are implemented with 8 channels and 4 channels respectively. While both designs achieved 40-Gb/s/channel data rate with 32 fJ/bit and therefore are suitable for energy-efficient high data rate applications, we note their complementary characteristics: the conventional common-bus design allows flexible wavelength assignment and can be particularly advantageous in minimizing overall thermal tuning power; the proposed new "Mod-MUX" architecture avoids cross-modulation entirely and does not require a comb source, therefore it is an attractive approach to achieve highly dense WDM and allow convenient integration with single wavelength lasers.

### *4.3 Other systems at a glance*

This section briefly highlight several other transceivers that I designed and implemented in the OpSIS-IME photonics platform. A key category of optical transceivers is wavelength-division multiplexing (WDM) transceivers with non-return-to-zero (NRZ) signaling, which strike a good balance between increased data capacity using multiple wavelength and minimal overhead in interfacing with electronics.

A key building block in WDM transceivers is a wavelength multiplexer (MUX) for the transmitter and de-multiplexer (deMUX) for the receiver. Echelle grating and array waveguide grating are the conventional approaches for building wavelength multiplexers. They are widely used in conventional material systems such as silica and silicon nitride, where the index contrast is small and therefore the required fabrication accuracy is rather relaxed. Recently, these types of designs are also demonstrated in high-index-contrast silicon platforms [81, 82]. An alternative approach is to use interleaved Mach-Zehnder interferometer (MZI) to achieve wavelength MUX/deMUX [83]. For low-channel-count (4 to 16) transceiver designs, MZI offers several key advantages:

(1) Design only depends on well-characterized and well-understood basic components: directional couplers and waveguides mostly

(2) Unit-cell based modularized design is possible

(3) Can achieve very low loss for low-channel-count designs due to simplicity in design

(4) Intrinsically cyclic

(5) Most importantly, it is convenient to implement tuning and control feedback knobs

For these reasons, I used MZI-based MUX to build:

(1) A 16-channel MUX with integrated thermal tuner, p-i-n loss tuners and monitor photodetectors (PD) (Fig. 4.11). This MUX design uses 4 similar unit-cells of 4-channel MUX/deMUX. The thermal tuners allows freely tuning the MUX channel locations, while the loss tuner fine compensates for non-perfect 50% directional couplers. Monitor PDs are implemented at each layer of MUX, making it possible to interface with control electronics. This chip is currently being packaged for testing, while preliminary testing results on individual components and 4-channel MUX are close to designed performance.

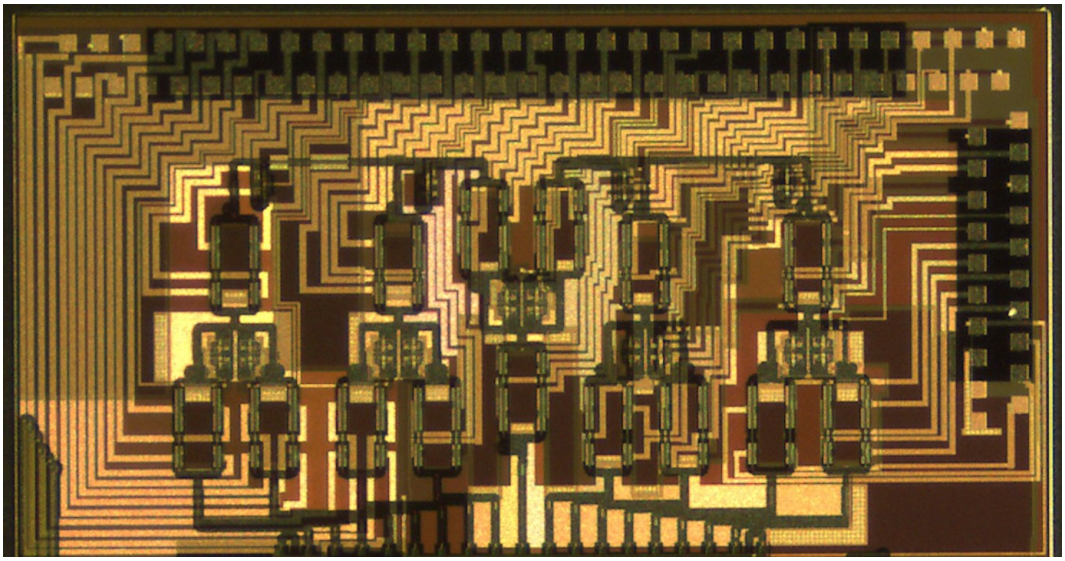


Figure 4.11: 16-channel tunable MUX with integrated optical monitors

(2) Using a newly developed on-chip 0.5-dB loss polarization beam splitter and rotator (PBSR) [84], a 4 × 40 Gb/s polarization-insensitive WDM receiver is implemented according to the schematic shown in Fig. 4.12. The receiver operates near 1550 nm wavelength. Once the light is input to the chip, it is passed through a PBSR and then variable attenuator (optional), followed by a pair of 1-to-4 deMUX. The originally TE and TM light are demultiplexed and joined at the high-speed photodetector that has two inputs.

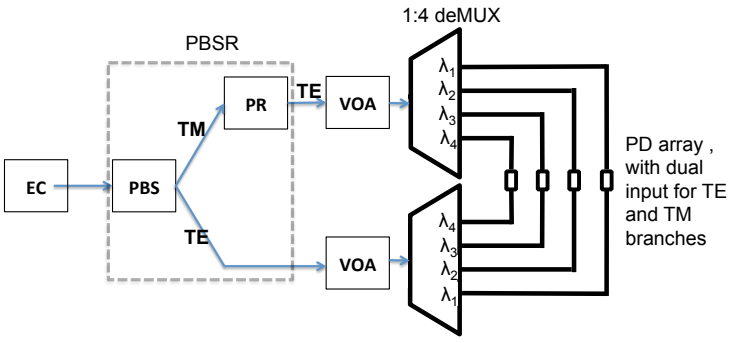



Figure 4.12: 4-channel WDM receiver schematic

The fabricated chip is shown in Fig. 4.13. The input is at the bottom. The PDs are at the top. Tuning pads for the deMUX are near the left and right edge of the chip. Multiple monitor PDs are implemented inside the deMUX as well as after the PBSR to provide sufficient monitor for feedback control loops. The PDs are designed to supposed more than 40 Gb/s data rate with 0.7 A/W responsivity.

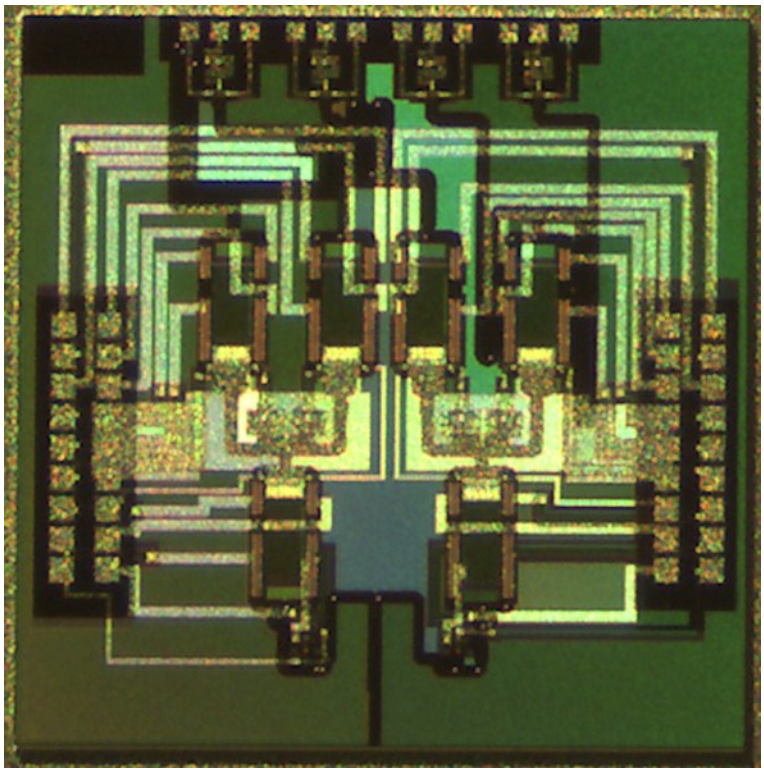
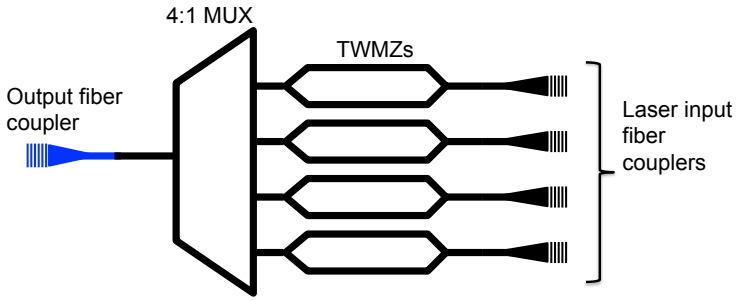
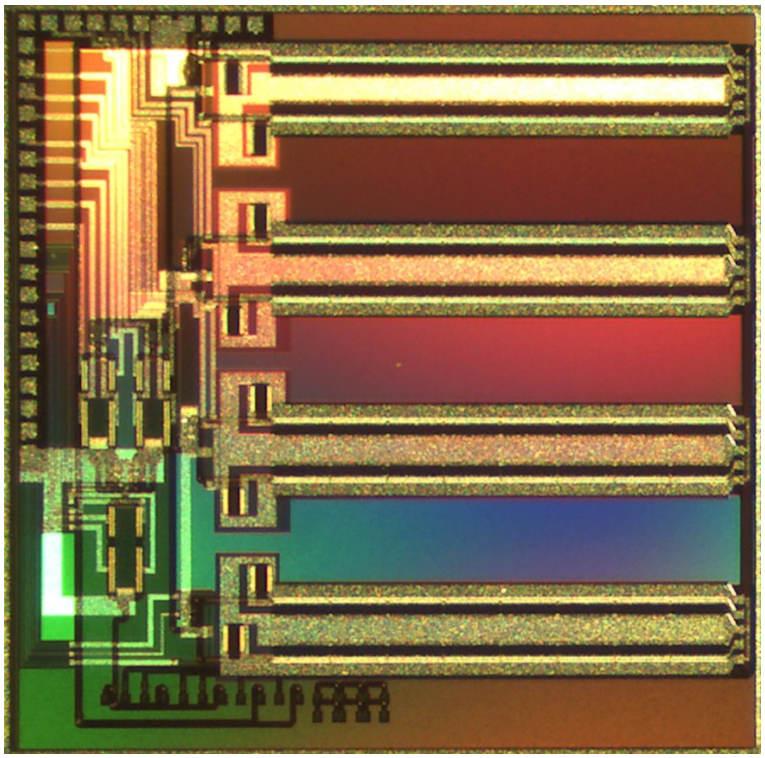


Figure 4.13: 1550nm 4 × 40 Gb/s polarization-insensitive receiver chip photo, chip size is 2.5 mm × 2.5 mm.

(3) A corresponding 4 × 40 Gb/s transmitter is shown in Fig. 4.14. The MUX remain the same as the deMUX in the aforementioned receiver. The modulators are similar to that in Section 3.2, but with a new RF design to remove the cross-talk between device arms. Another key change is the addition of on-chip termination resistor.




(a) 4-channel WDM transmitter schematic



(b) Transmitter chip photo

Figure 4.14: 1550nm 4 × 40 Gb/s TWMZ transmitter schematic and chip photo, chip size is 5 mm × 5 mm.

# Chapter 5

# HIGH-SPEED ANALOG CIRCUIT DESIGN AND ELECTRONICS-PHOTONICS CO-DESIGN

For a power-efficient and high-performance photonics system, electronics and in particular the high-speed analog front-end that directly interfaces with the photonic devices is an integral part and to a great degree determines system-level performance metrics. This chapter describes my work in high-speed analog circuit design as well as explorations in co-designing electronics circuits with photonics devices to enhance the overall performance.

## *5.1 40-GHz bandwidth transimpedance amplifier with adjustable gain-peaking in 65-nm CMOS*

In this section, I present the design and characterization of a broadband transmipedance amplifier (TIA) with adjustable gain-peaking in 65-nm CMOS. The TIA exhibits 40-GHz bandwidth, 20-dB gain and consumes 107 mW power. 50 Gb/s operation is demonstrated electrically as well as in an optical testbed. A low average input-referred-noise current density of 17.5 pA/$\sqrt{Hz}$ is achieved, which in combination with a 1 A/W photodetector implies an average optical power sensitivity of -16 dBm comparable or better than the state-of-the-art in similar fabrication processes. The circuit incorporates a simple yet effective gain-peaking adjustment functionality. With a 14% power consumption overhead, a 12-dB gain peaking can be achieved and is continuously tunable to non-peaked flat frequency response.

### *5.1.1 Circuit Design*

The circuit uses a three-stage cascaded topology with an resistive shunt-feedback as the transimpedance input stage, followed by a common-source gain stage, and then a cascode output stage. The input stage is designed to provide a good tradeoff between input impedance (broadband and sufficiently low), bandwidth, power and noise. Between the three stages as well as inside each stage, custom curled transmission line inductors are implemented to

achieve well-controlled inductive peaking.

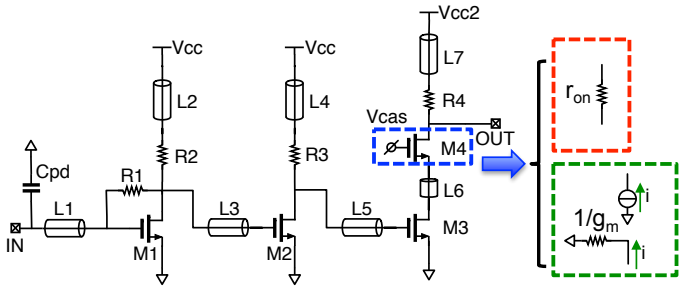



Figure 5.1: Circuit schematic

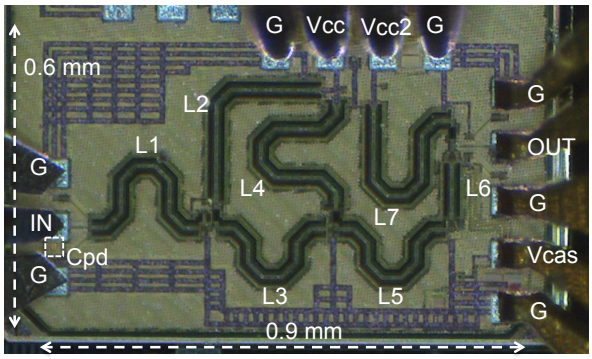



Figure 5.2: Chip photo

The output stage utilizes a cascode topology to minimize Miller capacitance. More importantly, the cascode device M4 in our design is to achieve tunable gain peaking. As illustrated in Fig. 5.1, depending on the bias voltages, mainly Vcas and Vcc2, the cascode device can exhibit two distinctly different behaviors.

When the device M4 is in saturation regime, standard small-signal modal applies: the impedance looking into the source of M4 is $1/g_m$ and the impedance looking into the drain of M4 is very high, the source of M4 is properly isolated from the output, therefore L6 is only connected to $1/g_m$ and not visible to L7 and R4. The value of L6 is rather small compared to $1/g_m$, and not sufficient to create significant peaking. So in this case the amplifier exhibit

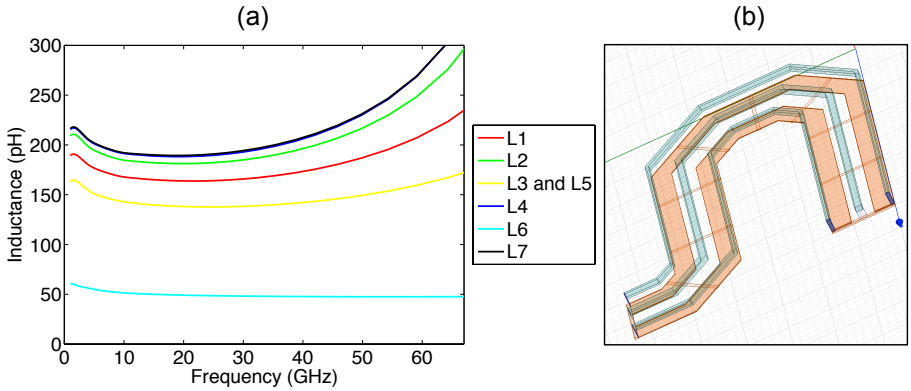



Figure 5.3: Inductor modeling (a) simulated inductance (b) 3-D rendering of one of the shielded-microstrip-transmission-line inductors (L7) used in the circuit

a flat response and the bandwidth is determined by the design of other parts of the circuits.

On the other hand, when the cascode device M4 is in triode mode due to a low bias voltage across gate and source, it behaves as a small resistor on the order of 3 Ω ($r_{on}$), so L6 is almost directly connected to R4 and L7. The additional inductance L6 can creates significant peaking as we will show in the measurement results. The degree of peaking can be continually tuned by adjusting the bias, i.e. essentially adjusting the $r_{on}$, so M4 behaves somewhere in between of the two situations illustrates in the inset of Fig. 5.1.

The fabricated circuits is shown in Fig. 5.2. Most visible are custom designed transmission line inductors. At the circuit input, we also implemented a small capacitor of 40 fF to emulate the capacitance of a photodetector. This is also indicated in Fig. 5.2.

The reason the inductors are implemented as transmission lines are to have the flexibility in layout and also the accuracy in modeling. The simulated inductance values of each inductor are shown Fig. 5.3(a) and an 3D rendering of a inductor model in HFSS is shown in Fig. 5.3(b). The top metal in this process is used for the signal trace and side ground shields. The side shield is to reduce the coupling to other inductors and to the inductor itself when it is curled in the layout. In addition, the lowest two levels of metal are used as a partial shield at the bottom to reduce the field penetration into the conductive substrate (thus reducing loss) while not introducing significant parasitic capacitance to the signal

trace.

### *5.1.2 Measurement and discussion*

On-wafer probed measurement was carried out to characterize the small signal performance of the circuit. The probing arrangement is shown in Fig. 5.2. The measured S-parameters are presented in Fig. 5.4. The solid lines and dash lines represent two different bias conditions, which are summarized in Table 5.1. Under fat-response bias, the circuit shows 20-dB gain, 40-GHz bandwidth and consumes 107-mW DC power. It is worthy nothing that, in this case the circuit only require one 1.6 V supply. By adjusting Vcas to be 1.2 V and Vcc2 to be 2.2 V we can achieve a maximum of 12 dB peaking with the peak centered at 40 GHz. The DC power in this case is 122 mW, a 14% overhead compared to flat-response case.

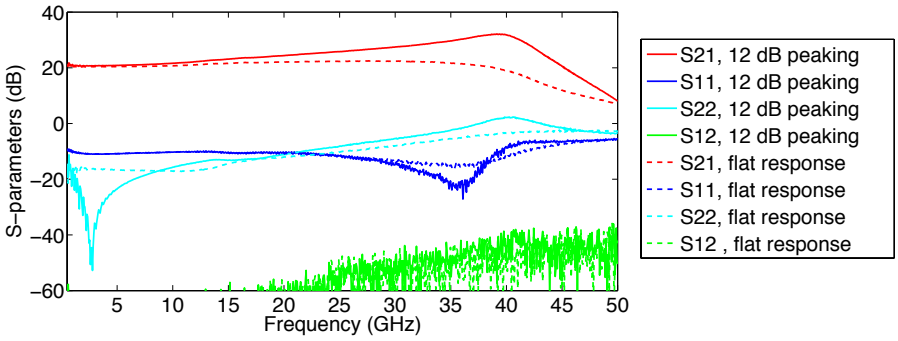



Figure 5.4: Measured S-parameters under two bias conditions: flat-response and 12-dB peaking.

Table 5.1: Bias Conditions for Flat and Peaked Response

| | $V_{cc}$ | $I_{cc}$ | $V_{cc2}$ | $I_{cc2}$ | $V_{cas}$ | $P_{dc}$ |
|---|---|---|---|---|---|---|
| Flat response | 1.6V | 46mA | 1.6V | 21mA | 1.6V | 107mW |
| 12-dB peaking | 1.6V | 46mA | 2.2V | 22mA | 1.2V | 122mW |

From the measured S-parameters we extracted the transmipedance gain to be 55 dBΩ as

shown in Fig. 5.12 inset. Integrated output noise is measured using a Tektronics DSA8200 sampling oscilloscope module with 60 GHz bandwidth and 1.802 $\mathrm{mV_{rms}}$ integrated noise. We have

$$\begin{aligned} I_{n,in,tot} &= \frac{2\sqrt{(2.053\,\mathrm{mV})^2 - (1.802\,\mathrm{mV})^2}}{55\,\mathrm{dB\Omega}} \\ &= 3.5\,\mu\mathrm{A_{rms}} \end{aligned} \tag{5.1}$$

and the average input-referred noise current density is

$$\begin{aligned} I_{n,in,avg} &= I_{n,in,tot}/\sqrt{BW} \\ &= 17.5\,\mathrm{pA}/\sqrt{\mathrm{Hz}} \end{aligned} \tag{5.2}$$

where $BW$ is the bandwidth of the circuit, i.e. 40 GHz. The measured input-referred-noise current density agrees well with simulation, as shown in dashed line in Fig. 5.5, which is below 20 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ up to 50 GHz. The low-noise performance is mainly attributed to the large input device M1 as well as a relatively large feedback resistor $R_1$ of 250 $\Omega$.

We further carried out data transmission measurement at 50 Gb/s characterize the dynamic response of the amplifier. Fig. 5.7(a)–(c) shows the output eyes with various input swing amplitude. Fig. 5.7(d) and (e) compare the eye-diagrams in a bandwidth limited electrical link showing the peaking significantly improved eye-opening in such a case. Finally, Fig. 5.7(f) shows the measurement in an optical testbed as shown in Fig. 5.6.

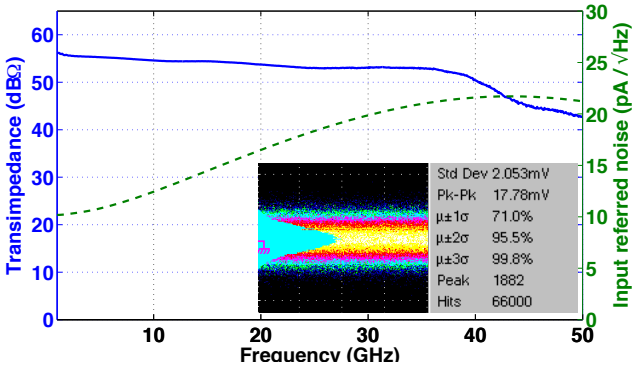



Figure 5.5: Extracted transimpedance and noise performance: Green dashed line showing simulated input-referred noise current density versus frequency; inset shows measured integrated output noise voltage is 2.053 $mV_{rms}$ including 1.802 $mV_{rms}$ due to the oscilloscope itself

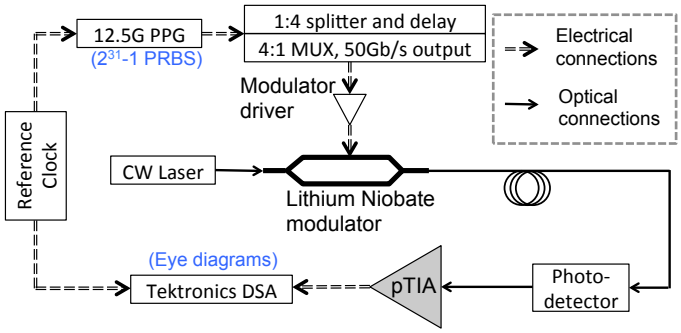



Figure 5.6: Optical testbed. PPG: Anritsu MU181020A pulse pattern generator; MUX: SHF 24210A 4:1 multiplexer; pTIA (peaking-TIA) is the amplifier under test; DSA: Tektronics DSA8200 digital serial analyzer.

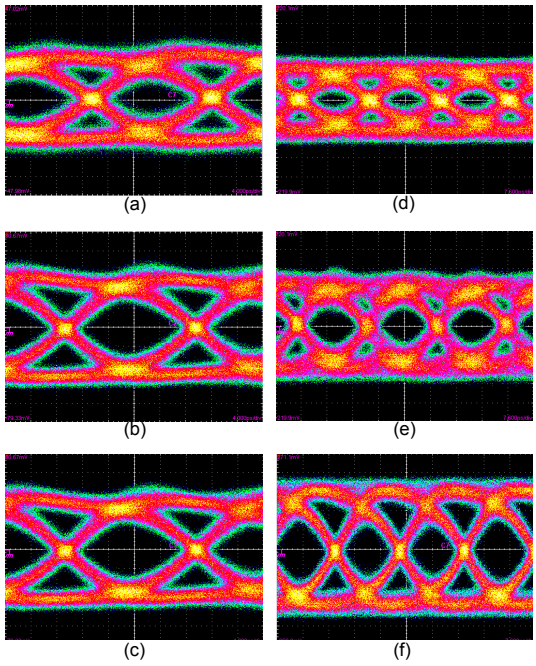



Figure 5.7: Measured output 50 Gb/s eye-diagrams: (a-c) with electrical input of 9 $mV_{pp}$, 18 $mV_{pp}$ and 35 $mV_{pp}$ respectively (d-e) flat-response and 12-dB peaking response in a severely bandwidth-limited cable link (f) measured in the optical testbed described in Fig. 5.6 with 0 dBm average optical power.

## *5.2 Power-efficient low-noise 86 GHz broadband amplifier in 130-nm SiGe BiCMOS*

A power-efficient, low-noise, broadband amplifier with a compact footprint is demonstrated in a 130-nm SiGe BiCMOS process. The amplifier exhibits 20-dB gain, 86-GHz bandwidth and consumes only 89-mW DC power, demonstrating a state-of-the-art gain-bandwidth (GBW) versus DC power efficiency of 9.66 GHz/mW. Intended as a low-noise transimpedance front-end for ultra-high-speed optical receivers, the circuit exhibits a low average input-referred-noise of 20.4 pA/$\sqrt{\text{Hz}}$ as well as low group delay variation of $\pm$5.9 ps up to 100 GHz. The core circuit area is only 0.04 mm$^2$, which includes active devices and transmission-line based peaking inductors.

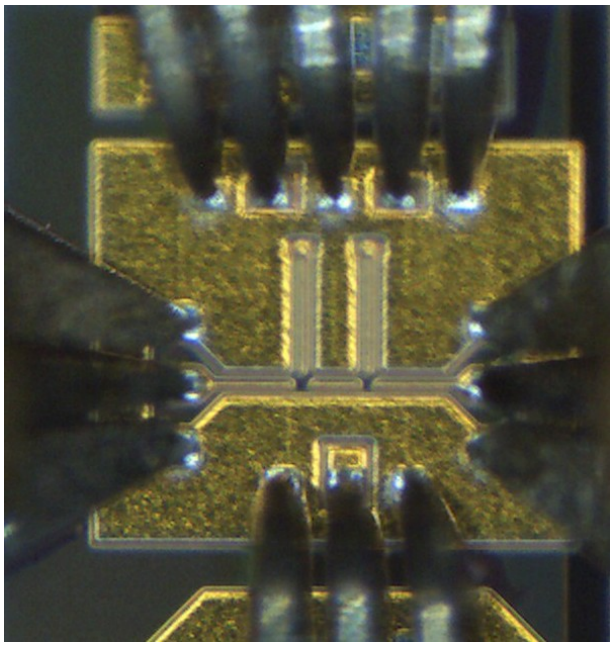


Figure 5.8: SiGe BiCMOS broadband amplifier chip photo

### *5.2.1 Introduction*

Energy-efficient optical interconnect [73] offers promising solutions to data transmission bottlenecks and power density problems in supercomputers, data-centers as well as other applications. Adopting higher channel data rates greatly reduces complexities in optical

communication systems and improves interconnect density [62], however this requires high performance circuitries with excellent power efficiency at high speed in order to improve the overall energy efficiency.

Compared to distributed amplifier topologies a non-distributed (lumped) amplifier design could achieve better tradeoffs between power consumption and key circuit performance metrics. In this letter, we report a broadband SiGe amplifier design based on a lumped amplifier topology. The amplifier exhibits a GBW/$P_{dc}$ of 9.66 GHz/mW with 89-mW DC power, 20-dB gain and 86-GHz bandwidth. The circuit demonstrate the highest figure-of-merit of GBW/$P_{dc}$ (gain-bandwidth-versus-DC-power) compared to the state-of-the-art, while achieving the most compact footprint. In addition, a low group delay variation (GDV) of $\pm$5.9 ps up to 100 GHz and low average input-referred noise of 20.4 A/$\sqrt{\text{Hz}}$ are demonstrated, enabling the amplifier to function as a low-noise transimpedance front-end in ultra-high-speed optical receivers. Data transmission up to 120 Gb/s is possible according to time-domain simulations based on measured S-parameters, while 50 Gb/s operation is experimentally demonstrated, limited by available equipment.

### *5.2.2 Circuit design*

The circuit topology, as shown in Fig. 5.9, can be viewed as three cascaded stages: a shunt-feedback Darlington amplifier as the input trans-impedance stage (TIS) consists of Q1 and Q2; a buffering emitter follower (EF) Q3; and a cascode trans-admittance stage (TAS) output stage, composed by Q4 and Q5. The circuit is implemented in IBM8HP 130-nm SiGe BiCMOS process with a 240 / 200 GHz $f_{max}$ / $f_T$ for the npn HBT devices.

Device Q1, Q2, R1 and R2 constitute a Darlington device to offer a higher effective $f_T$ [85]. The output impedance presented to the following stage (at node A) is 22 $\Omega$. The low impedance in combination with the input impedance of Q3 avoid bandwidth-limiting poles; it also ensures stability (concerning the potential negative resistance emerging from node A). The closed loop gain of the TIS stage is 13 dB. The TAS stage uses cascode to reduce Miller capacitance due to the large device Q4 and to improve output matching. An EF (Q3) is inserted to buffer the large input capacitance of Q4. To the first order, the

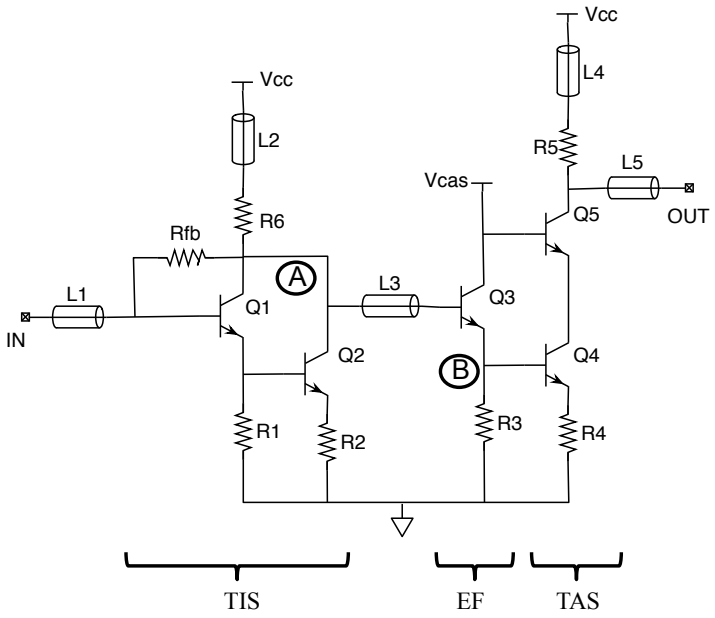



Figure 5.9: Schematic. L1–L5 are transmission line-based inductors; DC bypassing capacitors are omitted. Device sizes (emitter length) are: Q2, Q4, and Q5 is 10 $\mu$m, Q1 is 7 $\mu$m and Q3 is 5 $\mu$m. All devices are using minimum emitter width. The nominal resistance values are: $R_{fb} = 300\,\Omega$, $R_1 = 97\,\Omega$, $R_2, R_4 = 3.8\,\Omega$, $R_3 = 134\,\Omega$, and $R_5, R_6 = 48\,\Omega$.

emitter load impedance is scaled up by $1 + \beta_{Q3}$ if looking into the base of Q3, thus EF effectively reduces capacitive loading to the preceding stage [86]. In addition to impedance transformation (buffering), EF output impedance also has an inductive response, which compensates the input capacitance of Q4. The TAS stage provides a broadband output impedance and roughly 7 dB gain.

The shunt-feedback Darlington TIS stage has a 50 GHz bandwidth before inductive peaking. The inductor L2 and L3 are introduced for shunt-series peaking for the output of the TIS stage, while maintaining a low GDV of $\pm 2$ ps. All inductors were implemented as side-shielded microstrip transmission lines. L2 and L4 are 180 $\mu$m long, providing 90 pH inductance. L3 is 60 $\mu$m long, providing 30 pH inductance. L1 and L5 lead out to input and output pads and do not have a significant effect on the overall device bandwidth.

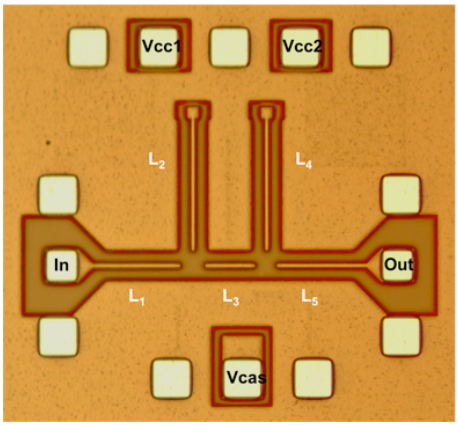



Figure 5.10: Chip photo

### *5.2.3 Result*

The amplifier occupies a total area of 0.28 $mm^2$ (0.52 mm $\times$ 0.54 mm) including pads, as shown in Fig. 5.10. The core area including the active devices as well as the main peaking inductors (L2, L3 and L4) is 0.04 $mm^2$. The amplifier frequency response was measured with an Agilent E8361C Vector Network Analyzer (VNA) and N5260A mm-wave controller. Cascade Infinity 110 GHz GSG probes were used to probe the input and output RF ports. Calibration was done with a standard substrate; therefore the bandwidth measurement included pad capacitance. At the optimal biasing, $V_{cc1}$ was at 2.65 V and supplies the Darlington stage with 17 mA current and $V_{cc2}$ was at 2.75 V and supplies the cascode stage with 10 mA current. $V_{cas}$ biases the cascode device and supplies the EF device; it is at 2.4 V and flows 6.9 mA current. Therefore the amplifier consumes 89 mW DC power. As shown in Fig. 5.11, the amplifier shows 20-dB gain (S21) at low frequency, and a 3-dB bandwidth of 86 GHz. The gain ripple is below $\pm$1 dB. The reverse isolation S12 is better than 35 dB. The measured stability $\mu$-factor is greater than 1, suggesting the amplifier is unconditionally stable. GDV is measured to be $\pm$5.9 ps up to 100 GHz, enabling high-speed data transmission.

From the measured S-parameters we extracted the transmipedance gain to be 55 dB$\Omega$ as shown in Fig. 5.12a. Integrated output noise is measured using Tektronics DSA8300

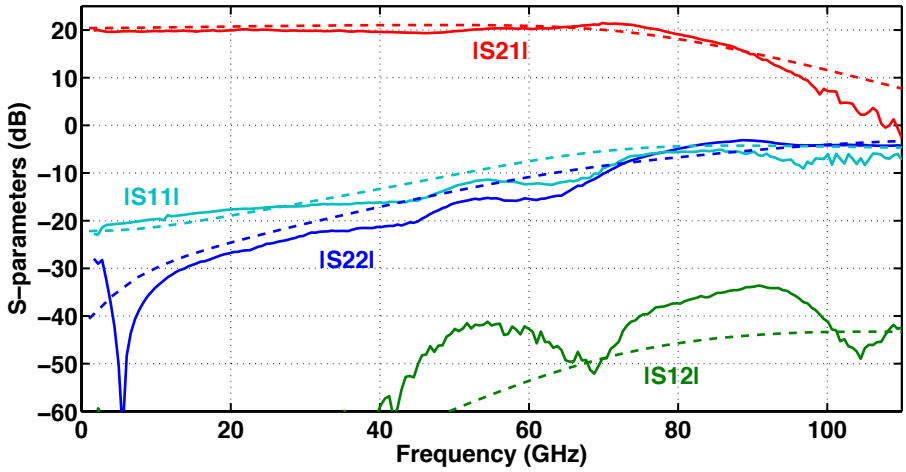



Figure 5.11: Measured (solid) and simulated (dotted) S-parameters

sampling oscilloscope module with 60 GHz filter bandwidth and 0.442 $\mathrm{mV_{rms}}$ noise. We have

$$I_{n,in,tot} = \frac{2\sqrt{(1.491\,\mathrm{mV})^2 - (0.442\,\mathrm{mV})^2}}{55\,\mathrm{dB\Omega}} = 5.0\,\mu\mathrm{A_{rms}} \tag{5.3}$$

and the average input-referred noise current density is

$$I_{n,in,avg} = I_{n,in,tot}/\sqrt{BW_{DSA}} = 20.4\,\mathrm{pA}/\sqrt{\mathrm{Hz}} \tag{5.4}$$

where $BW_{DSA}$ is the oscilloscope module bandwidth 60 GHz. The measured input-referred-noise current density agrees well with simulation, as shown in dashed line in Fig. 5.12a, which is below 24 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ up to 60 GHz. The low-nose performance is mainly attributed to the large input device Q1 and Q2 as well as a relatively large feedback resistor $R_{fb}$ of 300 Ω.

A 50 Gb/s pseudo-random-bit-stream is generated by an SHF 4:1 multiplexer from multiplexing four 12.5 Gb/s $2^{31}-1$ PRBS generated by a pulse pattern generator from Anritsu. The 50 Gb/s PRBS is then attenuated to 17 $\mathrm{mV_{pp}}$ before inputting to the amplifier. The input eyed-diagram before attenuation is measured to have an amplitude of 170 $\mathrm{mV_{pp}}$ and a Q factor of 6.6. The output eye-diagram from the amplifier is shown in Fig. 5.13a with an amplitude of 162 mV and a Q factor of 5.97, only a slight degradation from the input eye.

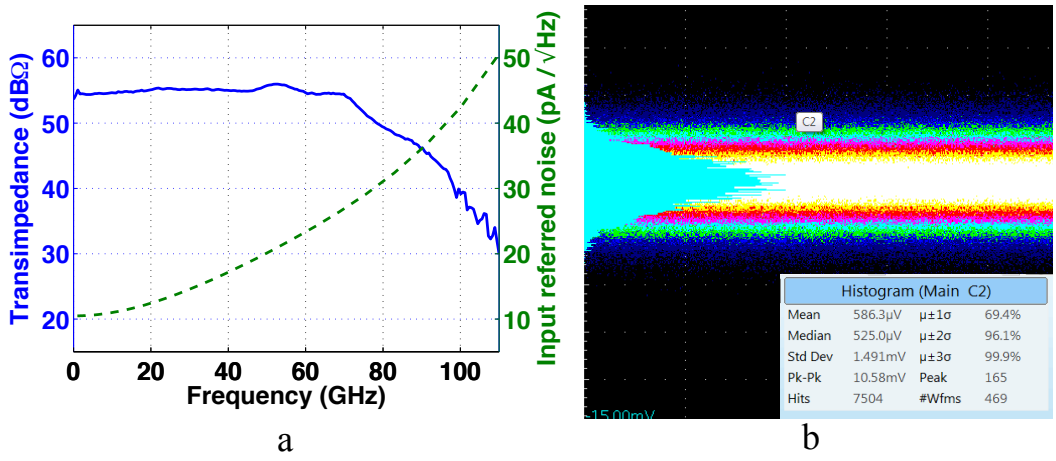



Figure 5.12: Noise measurement

a. Extracted transimpedance and simulated input-referred noise current

b. Measured integrated output noise

It is worth mentioning that the oscilloscope used to capture the eye-diagram has a relatively high level RMS noise of 1.8 $mV_{rms}$ and peak-peak noise of 14 $mV_{pp}$, contributing to such eye quality degradation. PRBS source beyond 50 Gb/s is currently unavailable, therefore we simulated eye-diagrams at 80 Gb/s and 120 Gb/s based on the measured S-parameters. As shown in Fig. 5.13b and 5.13c, the eye-height at 120 Gb/s is similar to 80 Gb/s while the deterministic jitter increases noticeably, since at 120 Gb/s the bit period is comparable to the GDV.

Using Eq. 5.3, and assume a photodetector (PD) responsivity of 1 A/W, following [87] we can estimate the average optical power sensitivity $\overline{P_{sens}}$ would be -14.6 dBm if the PD is closely integrated with the amplifier and the PD assumes similar capacitance (∼40 fF) as the pads that currently exist in the layout. This sensitivity is comparable or better than the state-of-the-art transimpedance amplifier and optical receiver results at much lower data rates [87–89].

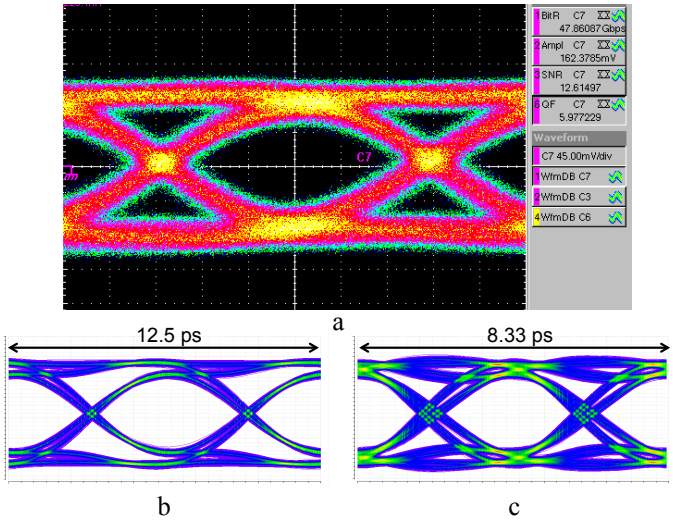



Figure 5.13: Eye-diagrams

a. Measured 50 Gb/s eye-diagram

b. Simulated 80 Gb/s eye-diagram based on measured S-parameters

c. Simulated 120 Gb/s eye-diagram based on measured S-parameters

### *5.2.4 Conclusion*

We demonstrate a broadband amplifier in a 130-nm SiGe BiCMOS process with high gain, low noise, low GDV, low power consumption and miniaturized footprint. Comparisons to other broadband amplifiers in SiGe processes are summarized in Table 1. Considering broadband amplifiers with 40 GHz or higher bandwidth that could support a 50+ Gb/s data rate, the amplifier described in this work achieves the highest GBW/$P_{dc}$ efficiency figure as well as the smallest area. The low GDV and low noise as well as the high GBW/$P_{dc}$ make this amplifier particularly suitable for energy-efficient ultra-high-speed optical receivers.

Table 5.2: Comparison to other broadband (BW > 40 GHz) amplifier results in SiGe processes

| Ref. | Process / $f_T$ | Gain (dB) | BW (GHz) | GBW (GHz) | $V_{cc}$ (V) | $P_{dc}$ (mW) | GBW /$P_{dc}$ | Area ($mm^2$) |
|---|---|---|---|---|---|---|---|---|
| [90] | SiGe / 200 GHz | 16 | 60 | 379 | 5.0 | 770 | 0.49 | 0.30 |
| [91] | SiGe / 100 GHz | 13 | 81 | 362 | 5.5 | 495 | 0.73 | 1.17 |
| [92] | 0.18$\mu$m SiGe / 200 GHz | 20 | 84.6 | 846 | -5.5 | 990 | 0.85 | 0.63 |
| [93] | 0.13$\mu$m SiGe / 200 GHz | 5 | 62 | 110 | 2.5 | 125 | 0.88 | −− |
| [94] | SiGe / 200 GHz | 12 | 50 | 199 | 5.2 | 182 | 1.09 | 0.92 |
| [95] | 0.13$\mu$m SiGe / 200 GHz | 10 | 110 | 347 | 3 | 119 | 2.92 | 2.18 |
| [96] | 0.12$\mu$m SiGe / 200 GHz | 10 | 102 | 323 | 2 | 73 | 4.42 | 0.29 |
| [97] | 0.13$\mu$m SiGe / 200 GHz | 24 | 15-110 | 1500 | 3.3 | 247.5 | 6.06 | 0.65 |
| **This work** | 0.13$\mu$m SiGe / 200 GHz | 20 | 86 | 860 | 2.75 | 89 | **9.66** | **0.28 /0.04(core)** |

### *5.3 100-Gb/s NRZ optical transmitter analog front-end in 130-nm SiGe BiCMOS*

Optical interconnects [73] offer promising solutions to data transmission bottlenecks in supercomputers, data-centers as well as other applications. Adopting higher channel data rates can greatly reduce the complexity in optical communication systems and/or further improve interconnect capacity and density [62]. In this paper we explore the possibility of implementing ultra-high channel rate (100 Gb/s) optical transmitters in silicon-based electronics and photonics technology.

As highlighted in Fig. 5.14a, the analog front-end in a typical optical transceiver includes the modulator driver and the transimpedance amplifier that serve as an interface between the high-speed optical channel and lower speed digital electronics.

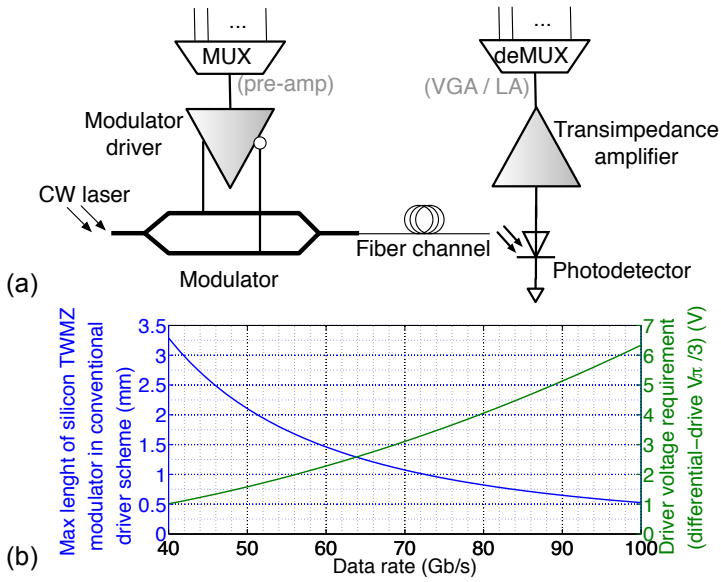



Figure 5.14: (a) Block diagrams of a typical optical transmitter and receiver (b) silicon traveling-wave modulator scaling versus data rate

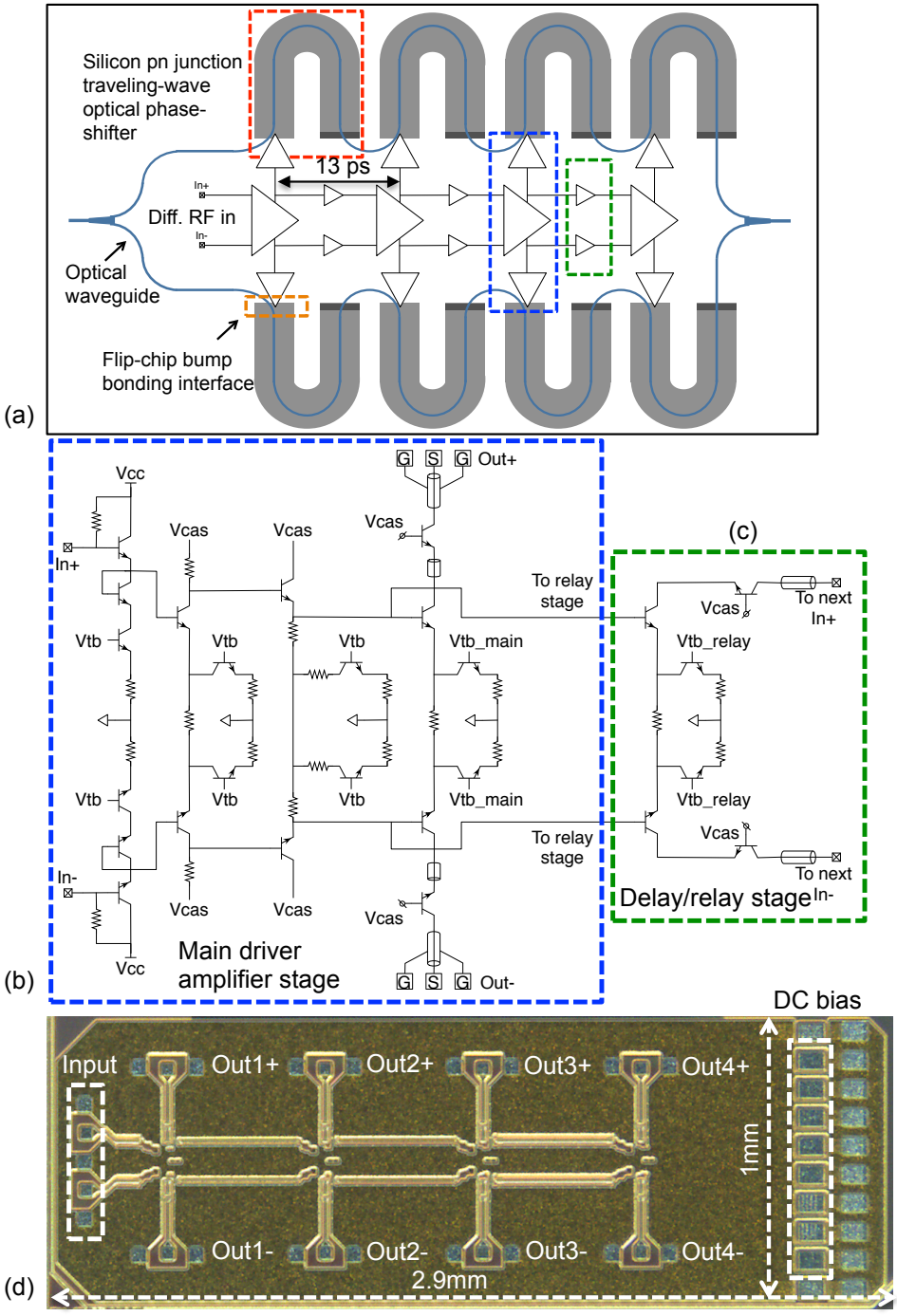



Figure 5.15: Distributed traveling-wave Mach-Zehnder (TWMZ) modulator driver: (a-b) circuit block diagram and schematics (c) chip photo.

The most important requirement on the driver amplifier is the output voltage swing. The state-of-the-art driver amplifier in CMOS/BiCMOS can output 3 $V_{pp}$ at 40 Gb/s, consuming 1.35 W DC power [98]. The output voltage swing is both limited by the low breakdown voltages of high-$f_T$ transistors and by the circuit design tradeoff against operating speed. Therefore, at higher data rates the available drive voltage is challenging to maintain or improve without substantial advance in fabrication process. This trend is at odds with the increasingly higher drive voltage required by modulators at higher speed. Based on the discussions in [99], we project silicon traveling-wave Mach-Zehnder (TWMZ) modulator device length, and consequently drive voltage requirement, versus data rate in Fig. 5.14b. The following assumptions are made: $C_{pn}$ is 230 fF/mm, $R_{pn}$ is 5.5 Ω-mm, $V_\pi L_\pi$ is 2.0 V-cm, device bandwidth is 70% data rate, differential-drive is used, and an equivalent of $V_\pi/3$ swing generates acceptable optical modulation amplitude. As shown in Fig. 5.14b, the drive voltage required at 100 Gb/s is $> 6$ $V_{pp}$ (on each single-end output), far from a practical voltage in existing CMOS/BiCMOS technology. To bridge the gap between the increasingly higher drive-voltage required by modulators and the limited available driver output voltage swing from electronics at higher data rates, we propose and implement a distributed TWMZ driver in 130-nm SiGe BiCMOS process.

As shown in the circuit block diagram in Fig. 5.15a, the driver amplifier takes 400 $mV_{pp}$ at each of the differential inputs, delay and amplify them to four pairs of outputs with 13 ps delay between each output stage. Each output swings 1 $V_{pp}$ single-ended (2 $V_{pp}$ differential) on a 25 Ω impedance. The output is intentionally configured to be open-collector to offer the flexibility to drive both 25 Ω and 50 Ω impedance TWMZ sections (without and with near-end termination, respectively).

The integration interface between silicon TWMZ sections and the driver circuits is expected to be flip-chip bump-bonding and 40 fF parasitic capacitance is assumed for each signal connection. The optical delay of each TWMZ section plus optical waveguide wiring matches the delay between the amplifier stages so that successive modulations add constructively. As an additional step to improve the performance, we incorporated pre-emphasis in the driver output to extend the length of TWMZ sections that can be driven at 100 Gb/s by ∼40%.

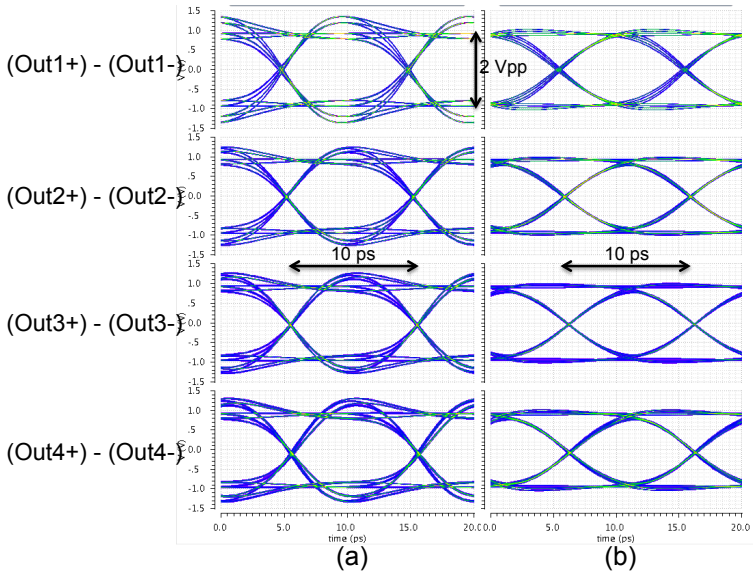



Figure 5.16: Distributed TWMZ driver post-layout simulation 100 Gb/s eye-diagrams: (a) at the driver outputs with pre-emphasis (b) after Si TWMZ. Differential output is 2 $V_{pp}$ at 25 Ω impedance; data is shifted by 13 ps between each output stage.

The circuit overall consumes 1.5 W DC power. The DC bias pins on the right of the chip (Fig. 5.15c) control the on and off of each main driver stage individually – a useful feature for testing before integration. Post-layout simulations at 100 Gb/s is shown in Fig. 5.16. The TWMZ sections are modeled using the equivalent circuit model in [99]. Bump-bonding parasitics are taken into account. Similar electrical eye quality is maintained in each stage output by scaling the transmission lines and device sizes in each stage. The eye-diagrams at the end of the TWMZ (Fig. 5.16b) provides a conservative estimation of the optical eye-diagrams [99].

In such a driving scheme, the overall drive voltage requirement is linearly lowered by accumulating modulation from four sections of TWMZ of 750 $\mu$m, achieving an overall modulator length of 3 mm – similar to what is achievable at 40 Gb/s with conventional driver scheme (Fig. 5.14b), providing a practical solution for 100 Gb/s optical transmitter.

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# Appendix A

# PUBLICATIONS

## *A.1 Recent papers and manuscripts*

1. **R. Ding**, Z. Xuan, T. Baehr-Jones, and M. Hochberg, "60 Gb/s Parasitics-Insensitive Optical Receiver Front-End for Hybrid Integration with Photonics," in preparation.

2. **R. Ding**, Z. Xuan, T. Baehr-Jones, and M. Hochberg, "A 40-GHz Bandwidth Transimpedance Amplifier with Adjustable Gain-Peaking in 65-nm CMOS," in preparation.

3. **R. Ding**, Y. Liu, Q. Li, Z. Xuan,1 Y. Li, Y. Yang, A. E.-J. Lim, G.-Q. Lo, K. Bergman, T. Baehr-Jones, and M. Hochberg, "A compact low-power 320-Gb/s WDM transmitter based on silicon microrings," in preparation.

4. **R. Ding**, Z. Xuan, P. Yao, D. Prather, M. Hochberg, and T. Baehr-Jones "Power-efficient low-noise 86 GHz broadband amplifier in 130-nm SiGe BiCMOS," submitted to Electronics Letters.

5. **R. Ding**, Z. Xuan, P. Yao, T. Baehr-Jones, D. Prather and M. Hochberg, "100-Gb/s NRZ Optical Transceiver Analog Front-End in 130-nm SiGe BiCMOS," submitted to Optical Interconnect 2014.

6. **R. Ding**, Y. Liu, Y. Ma, Y. Yang, Q. Li, A. E.-J. Lim, G.-Q. Lo, K. Bergman, T. Baehr-Jones and M. Hochberg, "High-speed silicon modulator with slow-wave transmission line electrodes and fully-independent differential drive," submitted to Journal of Lightwave Technology.

7. **R. Ding**, Y. Liu, Q. Li, Y. Yang, Y. Ma, K. Padmaraju, A. E.-J. Lim, G.-Q. Lo, K. Bergman, T. Baehr-Jones, and M. Hochberg, "Design and characterization of a 30-GHz bandwidth low-power silicon traveling-wave modulator,", Optics Communications, 321, 124–133 (2014).

8. Y. Liu*, **R. Ding***, Q. Li, X. Zhe, Y. Li, Y. Yang, A. E. Lim, P. G.-Q. Lo, K. Bergman, T. Baehr-Jones and M. Hochberg, "Ultra-compact 320 Gb/s and 160 Gb/s WDM transmitters based on silicon microrings", to appear at OFC2014 as paper Th4G.6. [*Equal contribution authors]

9. Z. Xuan*, **R. Ding***, T. Baehr-Jones, and M. Hochberg, "A 92 mW, 20 dB gain, broadband lumped SiGe amplifier with bandwidth exceeding 67 GHz", to appear in the Proceedings of IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM), paper 7.1, Oct 2013. [*Equal contribution authors]

### *A.2 Journal papers*

10. M. Streshinsky, **R. Ding**, Y. Liu, A. Novack, Y. Yang, Y. Ma, X. Tu, E. Chee, A. Lim, P. Lo, T. Baehr-Jones, and M. Hochberg, "Low power 50 Gb/s silicon traveling wave Mach-Zehnder modulator near 1300 nm," Opt. Express 21, 30350-30357 (2013).

11. Y. Ma, Y. Zhang, S. Yang, A. Novack, **R. Ding**, A. Lim, G. Lo, T. Baehr-Jones, and M. Hochberg, "Ultralow loss single layer submicron silicon waveguide crossing for SOI optical interconnect," Opt. Express 21, 29374-29382 (2013).

12. C. Galland, **R. Ding**, N. C. Harris, T. Baehr-Jones, M. Hochberg, "Broadband on-chip optical non-reciprocity using phase modulators", Opt. Express 21, 14500-14511 (2013).

13. T. Baehr-Jones, **R. Ding**, Y. Liu, A. Ayazi, T. Pinguet, N. Harris, M. Streshinsky, P. Lee, Y. Zhang, A. E-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, and M. Hochberg, "Ultralow drive voltage silicon traveling-wave modulator", Opt. Express 20, 12014-12020 (2012).

14. M. Gould, T. Baehr-Jones, **R. Ding** and M. Hochberg, "Bandwidth Enhancement of Waveguide-Coupled Photodetectors with Inductive Gain Peaking", Opt. Express 20, 7101-7111 (2012).

15. **R. Ding**, T. Baehr-Jones, W-J. Kim, B. Boyko, R. Bojko, A. Spott, A. Pomerene, C. Hill, W. Reinhardt, and M. Hochberg, "Low-loss Asymmetric Strip-loaded Slot Waveguides in Silicon-on-Insulator", Applied Physics Letters, 98, 233303 (2011).

16. A. Spott, T. Baehr-Jones, **R. Ding**, Y. Liu, R. Bojko, T. O'Malley, A. Pomerene, C. Hill, W. Reinhardt, and M. Hochberg, "Photolithographically fabricated low-loss asymmetric silicon slot waveguides", Opt. Express 19, 10950-10958 (2011).

17. **R. Ding**, T. Baehr-Jones, W-J. Kim, A. Spott, M. Fournier, J-M. Fedeli, S. Huang, J. Luo, A. K-Y. Jen, L. Dalton, M. Hochberg, "Sub-Volt Silicon-Organic Electro-optic Modulator With 500 MHz Bandwidth", Journal of Lightwave Technology, 29 (8), 1112-1117 (2011).

18. M. Gould, T. Baehr-Jones, **R. Ding**, S. Huang, J. Luo, A. K-Y. Jen, J-M. Fedeli, M. Fournier, and M. Hochberg, "Silicon-polymer hybrid slot waveguide ring-resonator modulator", Opt. Express 19, 3952-3961 (2011).

19. **R. Ding**, T. Baehr-Jones, W-J. Kim, X. Xiong, R. Bojko, J-M. Fedeli, M. Fournier, and M. Hochberg, "Low-loss strip-loaded slot waveguides in Silicon-on-Insulator", Opt. Express 18, 25061-25067 (2010).

20. **R. Ding**, T. Baehr-Jones, Y. Liu, R. Bojko, J. Witzens, S. Huang, J. Luo, S. Benight, P. Sullivan, J-M. Fedeli, M. Fournier, L. Dalton, A. Jen, and M. Hochberg, "Demonstration of a low V$\pi$L modulator with GHz bandwidth based on electro-optic polymer-clad silicon slot waveguides", Opt. Express 18, 15618-15623 (2010).

### *A.3 Invited talks*

21. Y. Liu, **R. Ding**, M. Gould, T. Baehr-Jones, Y. Yang, Y. Ma, Y. Zhang, A. E.-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, M. Hochberg, "30 GHz Silicon Platform for Photonics System", (invited), Optical Interconnects 2013

22. C. Galland, A. Novack, Y. Liu, **R. Ding**, M. Gould, T. Baehr-Jones, Q. Li, Y. Yang, Y. Ma, Y. Zhang, K. Padmaraju, K. Bergman, A. E.-J. Lim, G.-Q. Lo, M. Hochberg, "A CMOS-compatible silicon photonic platform for high-speed integrated opto-electronics", (invited), Proc. of SPIE Vol. 8767 87670G-1 (2013).

23. **R. Ding**, T. Baehr-Jones, Y. Liu, A. Ayazi, T. Pinguet, N. Harris, M. Streshinsky, P. Lee, Y. Zhang, A. E-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, and M. Hochberg, "A 25 Gb/s 400 fJ/bit Silicon Traveling-Wave Modulator", (upgraded as invited paper at Optical Interconnects 2012).

24. **R. Ding**, T. Baehr-Jones, T. Pinguet, J. Li, N. C. Harris, M. Streshinsky, L. He, A. Novack, A. E-J. Lim, T-Y. Liow, S. H-G. Teo, G-Q. Lo and M. Hochberg, "A Silicon Platform for High-Speed Photonics Systems", (upgraded as invited paper at OFC/NFOEC 2012).

25. T. Baehr-Jones, **R. Ding**, A. Ayazi, T. Pinguet, M. Streshinsky, N. Harris, J. Li, L. He, M. Gould, Y. Zhang, A. E.-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, S. Ocheltree, C. Hill, A. Pomerene, P. D. Dobbelaere, A. Mekis and M. Hochberg, "Shared shuttles for integrated silicon optoelectronics" (invited), Proc. SPIE 8252, 82520G (2012).

26. A. Spott, **R. Ding**, T. Baehr-Jones, W-J. Kim, X. Xiong, R. Bojko, J-M. Fedeli, M. Fournier and M. Hochberg, "Photolithographic fabrication of slot waveguides" (invited), Proc. SPIE 7927, 792704 (2011).

### *A.4 Magazine articles*

27. M. Streshinsky, **R. Ding**, Y. Liu, A. Novack, C. Galland, A. E-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "The Road to Affordable, Large-Scale Silicon Photonics", Optics and Photonics News, OSA, Sept. 2013 (Front cover and featured article)

28. M. Hochberg, N. C Harris, **R. Ding**, Y. Zhang, A. Novack, Z. Xuan, T. Baehr-Jones, "Silicon Photonics: The Next Fabless Semiconductor Industry", Solid-State Circuits Magazine, IEEE, 5 (1), 48-58, 2013.

### *A.5 Other conference proceedings*

29. Q. Li, Y. Liu, K. Padmaraju, **R. Ding**, D. F. Logan, J. J. Ackert, A. P. Knights, T. Baehr-Jones, M. Hochberg and K. Bergman, "10-Gb/s BPSK link using Silicon Microring Resonators for Modulation and Demodulation ", to appear at OFC2014 as paper Tu2E.5.

30. M. Streshinsky, **R. Ding**, A. Novack, Y. Liu, X. Tu, A. E.-J. Lim, E. K. S. Chen, P. G.-Q. Lo, T. Baehr-Jones and M. Hochberg, "50 Gb/s Silicon Traveling Wave Mach-Zehnder Modulator near 1300 nm", to appear at OFC2014 as paper Th2A.5.

31. T. Shiraishi, Q. Li, Y. Liu, X. Zhu, K. Padmaraju, **R. Ding**, M. Hochberg and K. Bergman, "A Reconfigurable and Redundant Optically-Connected Memory System using a Silicon Photonic Switch", to appear at OFC2014 as paper Th2A.10

32. **R. Ding**, Y. Ma, Y. Liu, Y. Yang, A. E. Lim, P. G.-Q. Lo, T. Baehr-Jones and M. Hochberg, "High-speed silicon modulators with slow-wave electrodes", to appear at OFC2014 as paper Th2A.35

33. C. Galland, A. Novack, Y. Liu, **R. Ding**, M. Gould, T. Baehr-Jones, Q. Li, Y. Yang, Y. Ma, Y. Zhang, K. Padmaraju, K. Bergman, A. E.-J. Lim, G.-Q. Lo, M. Hochberg, "A CMOS-compatible silicon photonic platform for high-speed integrated opto-electronics", SPIE Microtechnologies, 2013

34. A. Novack, Y. Liu, **R. Ding**, M. Gould, T. Baehr-Jones, Q. Li, Y. Yang, Y. Ma, Y. Zhang, K. Padmaraju, K. Bergman, A. E.-J. Lim, G.-Q. Lo, M. Hochberg, "A 30 GHz silicon photonic platform", SPIE Optics+ Optoelectronics, 2013

35. Y. Liu, **R. Ding**, M. Gould, T. Baehr-Jones, Y. Yang, Y. Ma, Y. Zhang, A. E.-J. Lim, T.-Y. Liow, S. H.-G. Teo, G.-Q. Lo, M. Hochberg, "30GHz Silicon Platform for Photonics System", Optical Interconnects Conference, 2013 IEEE

36. M. Hochberg, C. Galland, **R. Ding**, Y. Liu, Y, Zhang, N. Harris, T. Baehr Jones, "The Role of a Fabless Silicon Photonics Industry in the Era of Quantum Engineering", Latin America Optics and Photonics Conference, 2012

37. **R. Ding**, T. Baehr-Jones, T. Pinguet, J. Li, N. C. Harris, M. Streshinsky, L. He, A. Novack, A. E-J. Lim, T-Y. Liow, S. H-G. Teo, G-Q. Lo and M. Hochberg, "A High-Speed Silicon Photonics Platform", in Proceedings of IEEE Photonics Conference (PHO), Arlington, Virginia, (2011), Post-deadline Session PD8

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39. A. Ayazi, T. Baehr-Jones, **R. Ding**, M. Gould, W-J. Kim, A. Spott, S. Huang, J. Luo, B. Boyko, R. Bojko, A. K-Y. Jen, L. Dalton, and M. Hochberg, "Towards a low-loss, ultra-low drive voltage silicon-polymer hybrid electro-optic modulator", in Proceedings of IEEE 8th International Conference on Group IV Photonics, London, (2011)

40. **R. Ding**, T. Baehr-Jones, Y. Liu, R. Bojko, J. Witzens, S. Huang, J. Luo, S. Benight, P. Sullivan, J-M. Fedeli, M. Fournier, L. Dalton, A. K-Y. Jen, and M. Hochberg, "A Low V$\pi$L Modulator with GHz Bandwidth Based on an Electro-optic Polymer-Clad Silicon Slot Waveguide", in Proceedings of IEEE 7th International Conference on Group IV Photonics, Beijing, (2010), ThC4