A 1.1μW 2.1μVrms Input Noise Chopper Amplifier for Biomedical Applications

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Abstract

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Electrical Engineering

Micropower amplifiers for neural sensing and other biosignals are becoming increasingly relevant in cutting edge biomedical research. This thesis presents a complete 1.1uW two stage subthreshold low-noise amplifier configured for measuring local field potentials (brain signals used in neuroprosthetics). The first stage chopper amplifier is a 700nW folded cascode topology with three low-impedance node mixers that allow different sections of the amplifier to be chopped at different frequencies for lower noise levels. With a simulated NEF (noise efficiency factor) of 3.28 the first stage amplifier has the potential for incorporating many recording channels on an implanted IC; making efficient use of both silicon area and battery power.

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During two years of graduate studies my advisor Professor Dave Allstot provided the leadership and support to successfully balance this research with other responsibilities. Recognition also goes to Drs. Daibashish Gangopadhyay and Karthik Natarajan for technical guidance.

1.0 Introduction

Micropower amplifiers for sensing biosignals have numerous potential applications in advanced medical technology; particularly with implantable devices. The low frequencies associated with the electrical signals generated by the human body can be measured with very limited bandwidth amplifiers that draw minimum power and take up little silicon area. With these low bias currents also comes decreased signal to noise ratios. This thesis presents a power efficient low-noise chopper amplifier for biomedical applications.

Following the background information in this chapter, Chapter 2 will describe subthreshold CMOS design theory and noise considerations. Chapter 3 gives a functional description of the entire two-stage Bio-LNA for recording neural signals. Chapters 4 and 5 describe the first stage folded cascode chopper amplifier topology. Three low-impedance node mixers modulate the cascode output and folded input differential pair sections of the amplifier at two different frequencies. This technique gives very low noise levels. Chapter 6 presents schematic simulation results and Chapter 7 concludes with extracted results and a test plan.

1.1 Motivation

One of the only inside accounts of DARPA projects is given in [9]. The first chapter, "An Arm and a Leg," discusses efforts to develop prosthetic limbs. Standard "hook" type prosthetic arms are often chosen over the most advanced electromechanical models because of reliability and ease of use issues. Compared to prosthetic legs, the precision range of motion required for prosthetic arms leads to a more difficult engineering task: "Whereas our

legs are ordinarily not much more than our means of getting around, our hands are nothing less than our most versatile tools [9]."

Advances in technology are currently being made and new breakthrough prosthetic devices are under development. Conventional myoelectric arms rely on signals picked up externally from residual muscles at the prosthetic device attachment point. "For an advanced electronic arm to actually offer an improvement to the old-fashioned body-powered hooks, they will have to get better. A lot better … that would ultimately mean nothing less than going right to the source for full control of a full-featured prosthetic arm and hand: the brain [9]."

1.2 Neural Signals

Extracellular neural signals are classified as two types: Neural Spikes and Local Field Potentials (LFPs). Individual neurons produce spikes in the 300Hz – 5KHz range. "Spikes are 'digital' events; neurons produce spikes of nearly identical amplitude and durations, and information is encoded in the timing of spikes [6]." LFPs are the combined effect of many neurons firing in the brain and contain information that can be more easily recorded and analyzed for useful functions. LFPs are typically below 200Hz and have been shown to "correlate with specific arm movement reach parameters such as direction, distance, and speed, and thus may be useful in neuroprosthetic applications [6]." Neural spikes are on the order of 100uV and LFPs 30uV [6]. Some sources specify single digit microvolt levels for LFPs. Surely probe design, proximity, and background noise reduce measurable signal levels making sub-microvolt input noise levels desirable for LFP applications.

2.0 Subthreshold CMOS Circuit Design

MOSFETs are typically operated in the above-threshold region where an inversion layer exists in the channel between the source and drain. Subthreshold circuit design involves smaller currents and is inherently lower power. Devices are biased such that the gate to source voltage is below the threshold voltage. Some characteristics of subthreshold circuit design are [7, Ch. 3]:

- Saturation current is exponential in v_{GS}
- Currents are small
- High noise and offset
- Current flows by diffusion
- Can work on low power supply voltages

Reduced bandwidth is inherent with smaller currents and subthreshold design is usable only in low-frequency applications; however, with the exponential relationship between v_{GS} and i_{DS}, the current amplification per bias current ratio is greater than in above-threshold circuits. Despite the higher noise levels that are present, intelligent design choices can be made to mitigate noise in the circuitry. This allows for essentially the only major tradeoff to be the restriction to low frequencies. The benefits of efficient amplification and extremely small power consumption make subthreshold analog ICs ideal for use in implantable biomedical sensing devices.

2.1 Subthreshold CMOS Device Physics

The current flow characteristics of an nFET or pFET in weak inversion/subthreshold vary substantially from those in strong inversion/above-threshold. Looking at the strong-inversion/above-threshold device current-to-voltage curves that are predominately used in circuit design (Figure 1), it is seen that the transistor is assumed to be turned off when gate-to-source voltage (v_{GS}) is below the threshold voltage (v_{TH}) as no curves exist for these lower voltages. The semi-log plot of Figure 2 shows the weak inversion region that would otherwise be compressed and unreadable in the standard linear plot. Characteristics to note from Figure 2 are that saturation occurs in subthreshold with v_{DS} at around 100mV, v_{DSAT} is independent of v_{GS}, and that i_{DSAT} is exponential with v_{GS}.

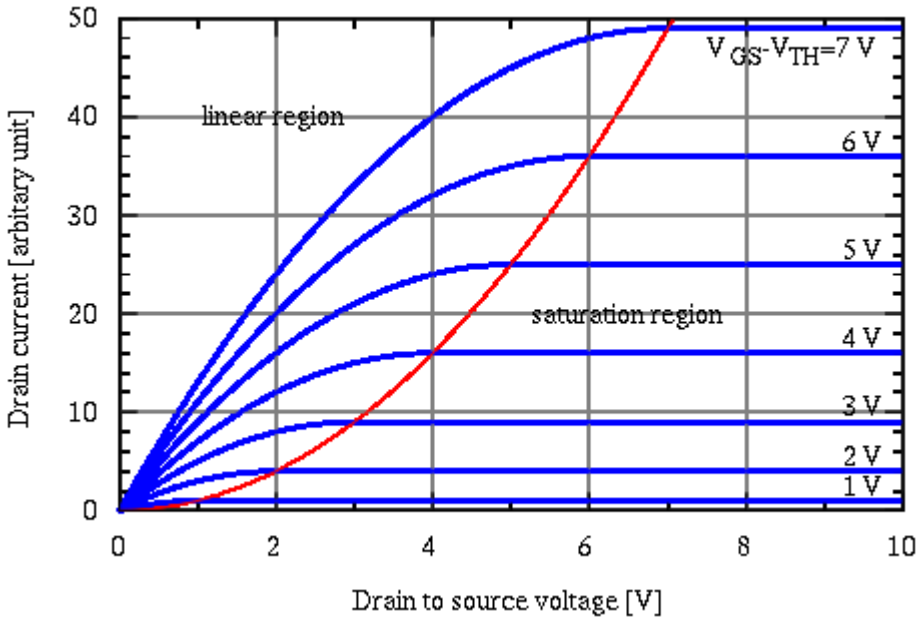

Figure 1 : NFET I-V Curve (Source: Wikipedia)

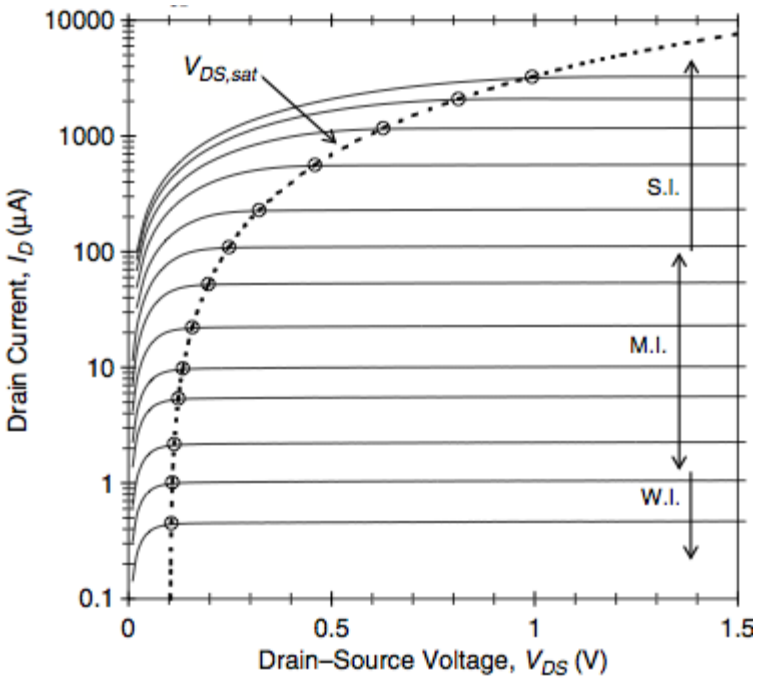

Figure 2: NFET I-V Curve Weak to Strong Inversion (Source: EDA Board)

The exponential I-V relation in subthreshold is due to the fact that current flow is predominately charge carrier diffusion, whereas current flows mostly by drift in above-threshold. Lower subthreshold gate voltages lead to less negative charge in the channel. An inversion layer is not formed because the fixed dopant atoms in the depletion region are sufficient to cancel the charge on the gate. The channel-to-drain and channel-to-source PN junctions are respectively reverse biased and off in subthreshold FETs, thus the surface potential (ψ_S) at the silicon channel to silicon-dioxide insulator interface is set only by the capacitive divider consisting of the oxide and depletion region capacitances [7]. This leads to a constant surface potential across the channel and no drift current as a result.

2.1.1 Saturation I-V Characteristics of MOSFETs

The square-law current to voltage relationship in above-threshold saturated CMOS devices is well known:

$$i_{DSAT} = \frac{\kappa_s \mu C_{ox}}{2} \frac{W}{L} (v_{GS} - V_{TS})^2 \qquad (1)$$

In subthreshold operation the diffusion current is determined by the concentration gradient of charge carriers (electrons in nFET devices) between the source and drain. Saturation in a subthreshold device occurs when the channel-to-drain junction is sufficiently reverse biased so that increasing drain voltages no longer affect carrier concentration in the channel at the drain end. The source end of the channel is a forward biased, but off, diode. Charge concentration in the source end of the channel will vary exponentially with gate to source voltage, leading to exponential changes in drain to source diffusion current [7].

$$i_{DS} = I_{0S} e^{\frac{\kappa_S v_{GS}}{\Phi_t}} (1 - e^{-v_{DS}/\Phi_t}) \qquad (2)$$

$$I_{0S} = \mu C_{ox} \Phi_t^2 \frac{W}{L} \left(\frac{1-\kappa_{sa}}{\kappa_{sa}}\right) e^{-\kappa_s v_{TS}/\Phi_t} \qquad (3)$$

Where κ_s is the subthreshold slope (1/n in some conventions), κ_{sa} is an exact value of κ_s calculated from the surface potential, and Φ_t is the thermal voltage (approx. 26mV at room temp) per [7].

2.1.2 g_m of Subthreshold MOSFET Devices

Taking the derivative of the subthreshold saturation current gives the small signal current gain similar to a BJT:

$$g_m = \frac{\partial i_{DS}}{\partial v_{GS}} = \frac{\kappa_S I_{DS}}{\Phi_t} \qquad (4)$$

Where the current gain of a BJT is the collector current (I_C) divided by the thermal voltage, for the subthreshold MOSFET it is the drain current (I_{DS}) divided by the thermal voltage and multiplied by the extra factor κ.

The subthreshold slope, κ, (or 1/n) is the slope of the I-V curve when current is shown in log scale. Intuitively this can be related to the physical value of κ:

$$\kappa = \frac{C_{ox}}{C_{ox}+C_{dep}} \qquad (5)$$

This capacitive divider ratio gives the surface potential in relation to the gate to bulk voltage (also the gate to source voltage, v_{GS}, when the source is connected to the bulk). When the source voltage changes linearly, the charge concentration changes exponentially and so does the diffusion current.

The subthreshold slope was found to be higher for the nFET devices than pFETs in the IBM process. Detailed test results and discussion are given in Chapter 6.2. The most likely cause for this is different dopant concentrations in n-channel vs. p-channel FETs to set the threshold voltages. The devices are operating in accumulation mode with no inversion layer. Less doping will cause a larger depletion region to form and higher depletion region capacitance in pFETs. Also, the pFETs residing in an n-well will affect depletion region capacitance.

2.2 Noise in Subthreshold CMOS Circuits

Subthreshold circuit design differs significantly from standard above-threshold operation. Useful in certain low-power applications, subthreshold techniques have advantages: higher gain for a given bias current, increased headroom due to the almost constant 100mV v_{DSAT}, and lower power consumption. The different method of current flow in subthreshold devices also leads to a different analysis of noise.

Thermal noise is due to random electron motions in the channel. In subthreshold the thermal noise current is [7]:

$$\overline{\Delta I_{DS}^2} = 2qI_{DSAT}\left(1 + e^{-v_{DS}/\phi_t}\right) \qquad (6)$$

The equation for subthreshold thermal noise current shows that noise is proportional to current and asymptotes at a minimum once saturation is reached (i.e. $v_{DS} = 4\phi_t \approx 100\text{mV}$). One thing to notice is that device size doesn't affect thermal noise—at least in first order calculations. Test results in chapter 6.2 show that there is a small effect from device sizing and channel type in the IBM 130nm process.

Flicker noise is the major concern at low frequencies. The theory behind flicker noise is that there are traps in the gate to channel interface which charge carriers can become trapped in. The energy barrier associated with these traps in pFETs is higher than nFETS and so pFETs have approximately half the 1/f noise power of comparable nFETs. The noise power is proportional to frequency such that every decade has the same amount of flicker noise. There

is as much flicker noise power from 1Hz to 10Hz as there is in the 10KHz to 100KHz band. Much of the theory behind 1/f noise is empirical. It is an observed phenomenon that exists, and there are models, but it is not definitively understood.

Flicker noise is also proportional to g_m^2. This can be explained by one model: "The trapping theory states that electrons move into and out of traps or low-energy states in the gate oxide. This motion modulates Q_0, the fixed charge in the oxide, and consequently varies V_{FB} such that there is a dynamic modulation of the threshold voltage." In saturated above threshold operation this modulates current by the square law. In subthreshold the modulation is exponential.

$$\overline{\Delta I_{DS}^2} = \frac{KI_{ds}^2}{f^{n_1}}\Delta f, \text{ in subthreshold } n_1 \approx 1 \qquad (7)$$

$$= \frac{KI_{ds}}{f^{n_2}}\Delta f, \text{ in above threshold } n_2 \approx 1 \qquad (8)$$

This subchapter shows that thermal noise performance in subthreshold is proportionally better than in above threshold for a given current due to greater amplification. Flicker noise is much more of a problem for the same reason. The larger transconductance helps with thermal noise while it is part of the cause of flicker noise. This background information on noise in subthreshold circuits was presented to show the importance in reducing flicker noise in low-frequency circuitry—especially in subthreshold. It should also give insight into why some design choices were made in the first stage chopper amplifier.

3.0 Bio-LNA System Level Description

A two-stage LNA for recording biological/neural signals was designed in the IBM CMOS 8-metal layer RF process. Variable gain is implemented in both stages with digitally controlled capacitor banks for amplification control in six increments from 30dB to 83dB. The first stage chopper amplifier utilizes high-frequency feedback loops for improved accuracy and noise performance. A low-pass filter, mixer, and coupling capacitor make up a DC offset cancellation loop in the first stage. This chapter will describe the features of these sub-blocks.

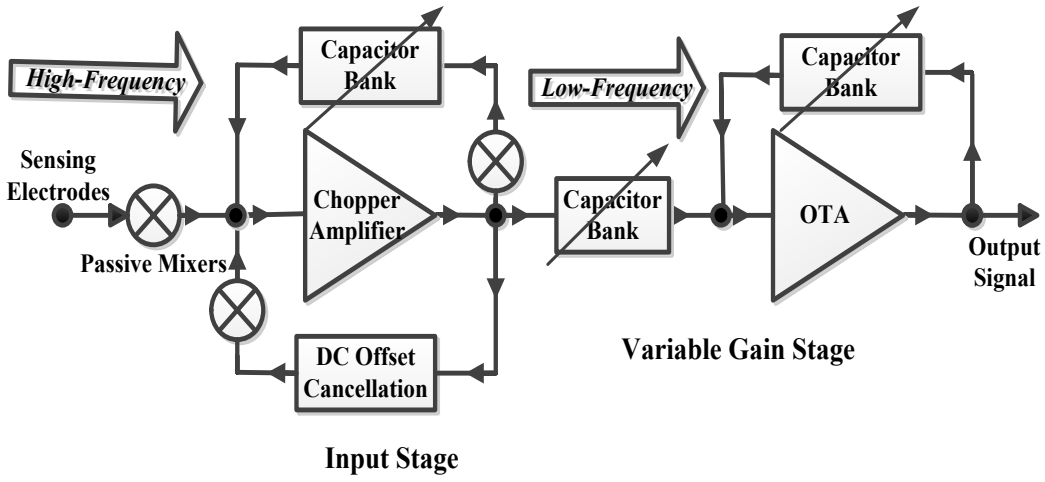

Figure 3: System Level Block Diagram

3.1 First Stage Chopper-Stabilized Amplifier

A link budget noise analysis of the LNA shows that low-input referred noise in the first stage improves noise performance. Chopper modulation was utilized in the first stage to overcome flicker noise which is the major contributor at the low frequencies at which this amplifier is designed for.

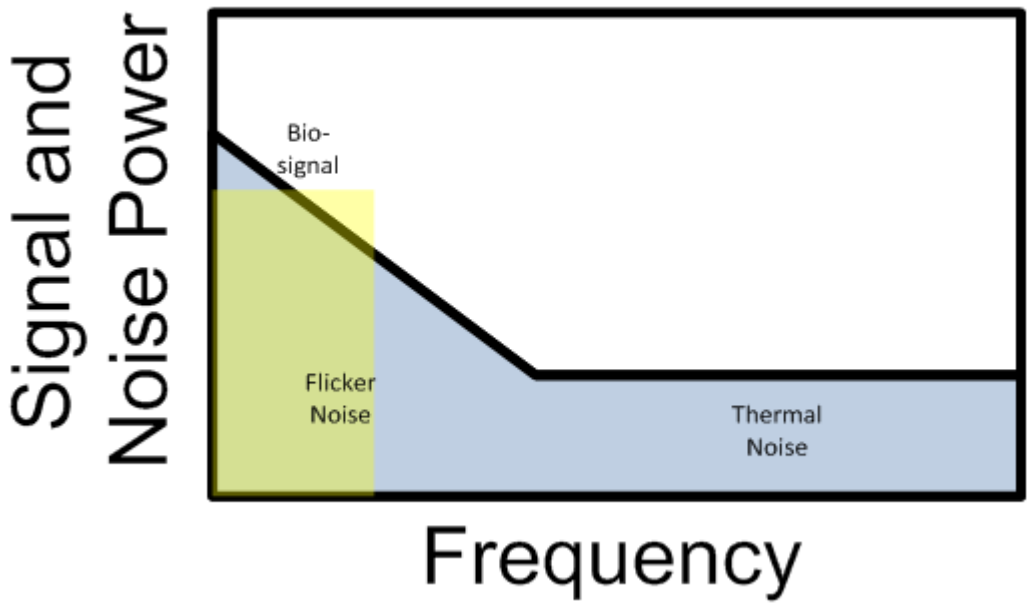

Figure 4: Noise and Signal Spectrum

The differential neural signal is connected directly to CMOS switches and the up-modulated signal is capacitively coupled to the differential input summing nodes of the chopper amplifier via 20pF MIM capacitors. A maximum gain of 43dB is achieved using the smallest (130fF) capacitors in the feedback capacitor banks. Two larger capacitors in series are used instead of a single capacitor for the high-gain setting since this capacitance value is very close to the minimum allowed by the design kit. Using two larger series capacitors should improve matching.

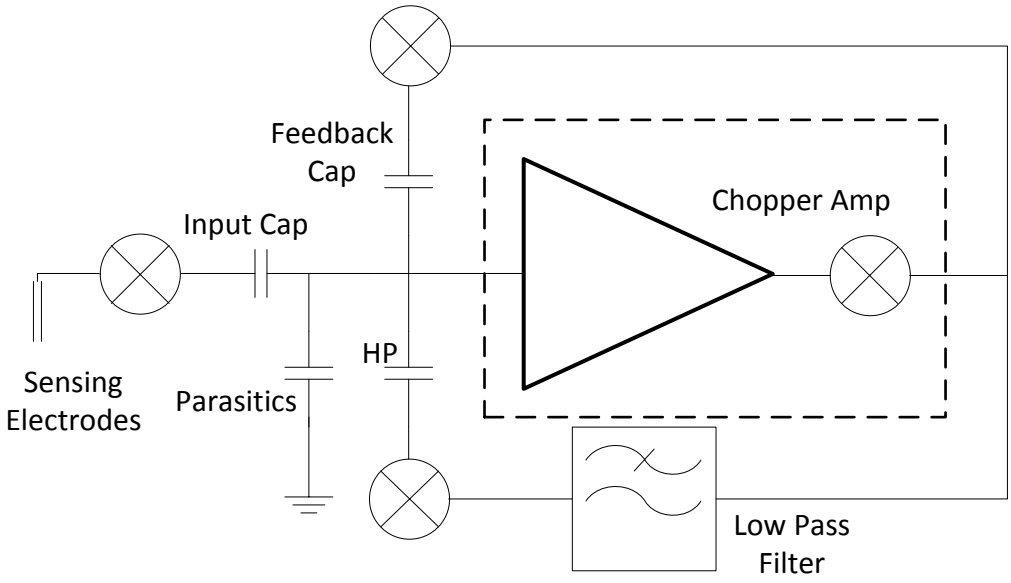

Figure 5: First Stage Amplifier Feedback Network

Demodulation occurs inside the chopper amplifier so the output is at baseband. The gain controlling feedback path consists of the feedback cap banks and CMOS switches to re-modulate the output back up to the chopping frequency prior to the feedback capacitors and application to the high frequency input summing node at the input gates of the differential chopper amplifier. The overall transfer function for the first stage is shown below [2]:

$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{C_{in}}{C_{fb}} \cdot \frac{1}{1+\frac{1}{A_0}\cdot\frac{C_{in}+C_{fb}+C_{hp}+C_p}{C_{fb}}} \cdot \frac{1}{1+\frac{s}{\omega_{lp}}} \cdot \frac{1}{1+\frac{\omega_{hp}}{s}} \qquad (9)$$

There is some additional gain error from charge sharing at the input node involving the input, feedback, and parasitic capacitances. The high-pass and low-pass frequencies are [2]:

$$\omega_{lp} = \omega_t \cdot \frac{C_{fb}}{C_{in}}, \qquad \omega_{hp} = \frac{C_{in}}{C_{fb}} \cdot \frac{C_{hp}}{C_{fb}} \cdot \omega_{lpf} \qquad (10),\ (11)$$

The low pass frequency is set by the gain bandwidth product and the high pass -3dB corner is set mostly by the low pass filter corner frequency in the DC offset cancellation loop in equations 10 and 11. The chopper amplifier topology and more on noise reduction techniques are discussed in Chapter 4.

3.2 Second Stage Variable Gain Amplifier

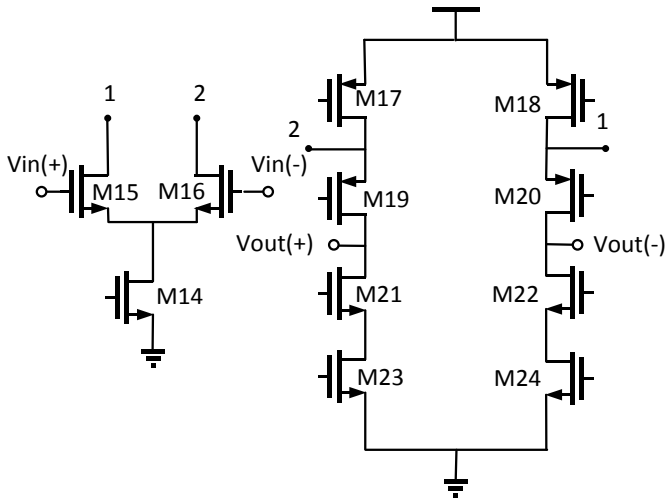

Figure 6: Second Stage OTA

The second stage amplifier is a subthreshold folded cascode topology using 56% of the bias current of the first stage to keep the overall power consumption less than 1.1uW. This amount of biasing is used because the second stage is assumed to be driving an ADC with input capacitance much smaller than the 2pF band-limiting output caps. The second stage gain requirement is lower, and the non-chopped topology requires less current. Another reason for minimizing the second stage bias current is also to limit the bandwidth. In this design chopping is performed at 15 – 60 times the Nyquist rate for the first stage amplifier's

bandwidth. The corner frequency of the second stage amplifier is at double the nyquist rate with a single pole -20dB per decade roll-off. Using a chopping frequency of 10KHz, or greater, ensures at least 20dB attenuation of chopper ripple at the output of the second stage amplifier.

One design choice that could be made to further reduce flicker noise in the second stage is to replace the input pair M15/16 with pFETs. On the other hand, the high gain of the first stage makes second stage noise almost insignificant. There is a power/noise tradeoff by using the greater transconducting nFET input pair. The important characteristics of the second stage amplifier are its variable gain/bandwidth and low power consumption. The next chapter will be focused only on the first stage amplifier design. The second stage amplifier, at the system level, is included for additional (variable) gain and low-pass filtering.

3.3 DC Offset Cancellation Loop

The first stage output is applied to a G_mRC ladder low pass filter with a cutoff frequency of less than two hundred milli-hertz and is fed back to cancel differential DC offset errors. These errors may be from the sensing electrodes themselves or from the amplifier—although chopping will significantly reduce any offsets from device mismatches originating within the amplifier and feedback paths. DC levels that are present at the sensing electrodes are upconverted and then demodulated to saturate the first stage amplifer. An offset cancellation loop is necessary to handle these sensing electrode DC errors that exist in real world sensing applications.

The DC offset cancellation loop utilizes a subthreshold low gain pFET body input current amplifier in conjunction with a two-stage RC ladder network to realize an extremely low corner frequency. The functionality of this DC offset cancellation loop was shown in schematic, with its addition affecting the high pass corner in Quasi-Perioding Steady State simulations in Cadence SPECTRE™. These simulations could not be run on the extracted design and how this performs will need to be actually tested. Due to the small currents involved, the design may be rendered ineffective by leakage currents at the switches. In any event, the worst case is that the DC cancellation feature does not perform as it should and it adds noise in the first stage—noise that would be present in any real world neural sensing application utilizing a DC cancellation loop.

3.4 Conclusion

The two-stage Bio-LNA is an integrated system built around the high performance first stage chopper amplifier to measure small bio-signals. Other important functions are the additional gain and low-pass filtering of the second stage amplifier as well as the active DC offset cancellation feedback loop. The remainder of this thesis will focus on the first stage chopper amplifier design.

4.0 Three Mixer Folded Cascode Chopper Amplifier

The folded cascode chopper amplifier in Figure 7 is a fully differential low-noise instrumentation amplifier for input signals on the order of low single-digit to tens of microvolts; specifically for recording local field potentials (LFPs) in the human brain. Three mixers are placed at low-impedance nodes of the folded cascode amplifier for dynamic component matching, offset elimination, signal modulation, and noise modulation. Due to relatively small RC time constants, the settling time of the low-impedance nodes is small and chopping can be done at frequencies much above the closed loop bandwidth of the subthreshold LNA [3]. For simulated testing purposes in Cadence SPECTRE-RF™ a 40KHz set of non-overlapping clocks for both n and p devices was used to obtain schematic and extracted results. Other frequencies will be used after fabrication and actual test results will give power-to-noise performance data for comparison. The three-mixer design allows the input signal path to be chopped at a different frequency than the cascode output section of the amplifier—providing another control knob for noise optimization. This chapter describes the chopper amplifier operation, topology, and design choices made.

4.1 Chopper Amplifier Schematic and Biasing

Figure 7 shows the chopper amplifier schematic with bias currents. The folded input is separated from the cascode output section at nodes 1 and 2 in the drawing. The chopping signals CLKP, _CLKP, CLKN, and _CLKN are complimentary non-overlapping square waves generated on-chip. Non-overlapping clock generators are supplied a sinusoidal input and generate off-overlap square waves for both NMOS and PMOS devices.

The differential input pair, M1/M2, consists of nFET devices because the input signal is modulated at the chopping frequency (above the 1/f noise corner). Using pFETs would only reduce 1/f noise that is later upconverted to the chopping frequency and filtered out, therefore the higher current gain devices are used. The supply rail is 1.2V and the bias current is proportioned between the input devices and cascode output section for increased gain and lowered output noise. Although more severe current scaling can be used to push performance even more, greater attention is then needed alleviate the effects of process variations [1].

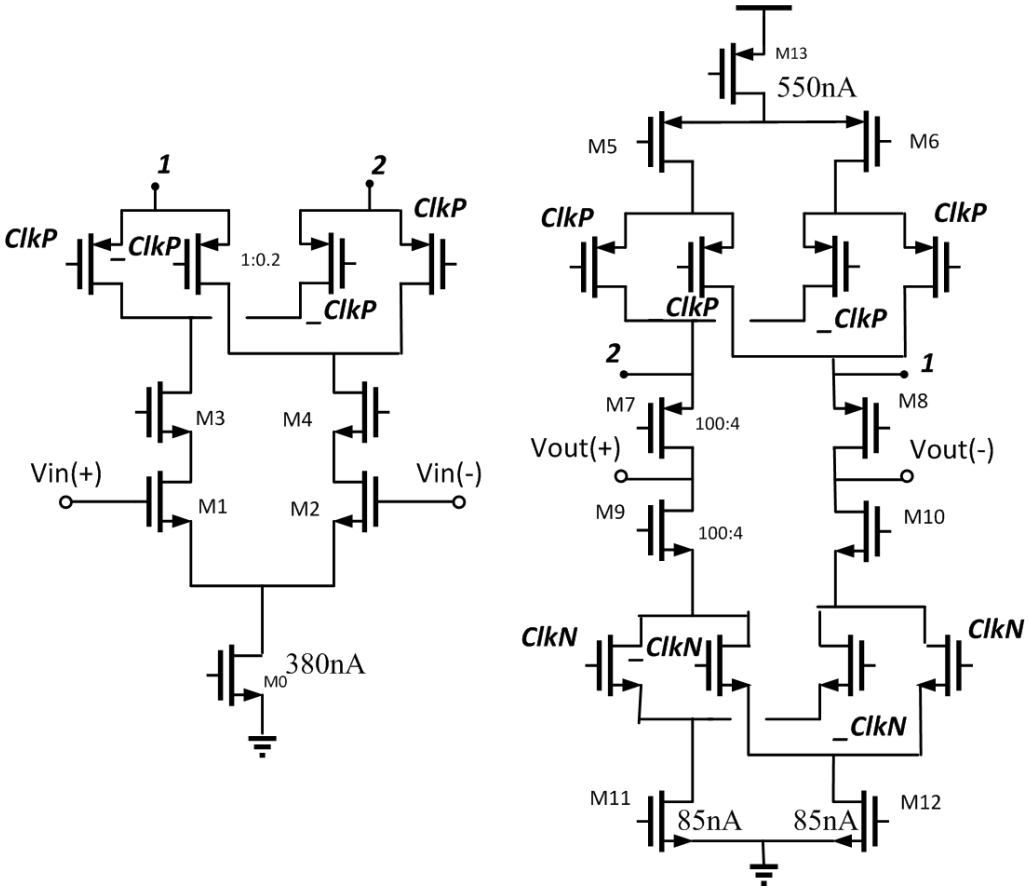

Figure 7: Schematic of Folded Cascode Chopper Amplifier

It was experimentally observed that the cascode output required higher bias current levels to function properly with the addition of low-impedance node choppers. Therefore, the current

ratio of 16:1 used in the non-chopped amplifier of [1] would not be possible in the chopped topology. When the bias current is too small, it requires too much time to adjust charge levels at the various nodes in the circuit; this results in increased chopper ripple as current is reduced. A bias current of 85nA allows the periodic steady state to be restored quickly, i.e. the amplifier re-biases, after switching operations without causing excessive spiking (chopper ripple) at the output. This observed effect can be expected to be worse after fabrication, or even in extracted testing, with increased nodal parasitics and leakage. The current ratio of 2.2:1 keeps a conservative amount of bias current in the cascode output, while still maintaining overall power consumption low and benefitting from an increased current division ratio.

Another benefit of maximizing the current in the input devices is increasing their bandwidth because they're amplifying the signal at the chopping frequency. By adjusting current levels and chopping frequencies in simulation, it was verified that the higher bias current input section is not frequency limited at the 40KHz chopping frequency. Higher chopper frequencies started to show output attenuation with the 380nA of bias current that is being used in the input. Actual results should vary significantly, but extracted testing worked at frequencies above 40KHz. One proven design uses a chopper frequency of 100KHz, however this occurs after the signal is amplified at baseband [5]. This design choice is discussed further in section 4.4. The ability to chop at higher frequencies allows the use of a single pole low-pass filter for chopper ripple and upmodulated noise removal in addition to reduced thermal noise.

4.2 Chopper Amplifier Block Diagram

Figure 8 is a block diagram that shows how modulation is performed inside the chopper amplifier by separating the amplifier into sections that are connected with mixers. The signal to the input transistors M1 and M2 is up-modulated to the chopping frequency by passive voltage-commutating transmission gate mixers. The folded section consisting of the input differential pair (M1 & M2), cascode transistors M3 & M4, and current mirror M0 are represented by the gm triangle in the block diagram. MOSFETs M5, M6, and M13 source all of the conventional flowing current and are referred to as the current source. The bottom nFETs are another set of input transistors and are used to control common-mode output voltage DC level with a continuous time common-mode feedback loop.

The four cascode devices M7, M8, M9, and M10 are the cascode output block. The cascode output is separated from all of the other blocks with current-commutating mixers and is therefore the only baseband circuit block in the chopper amp. Inside the amplifier, only the mixer between the gm block and cascode output is on the actual signal path—and must be at the same frequency as the input mixers connected to the sensing electrodes. The other two mixers may be run at a different frequency to decrease noise.

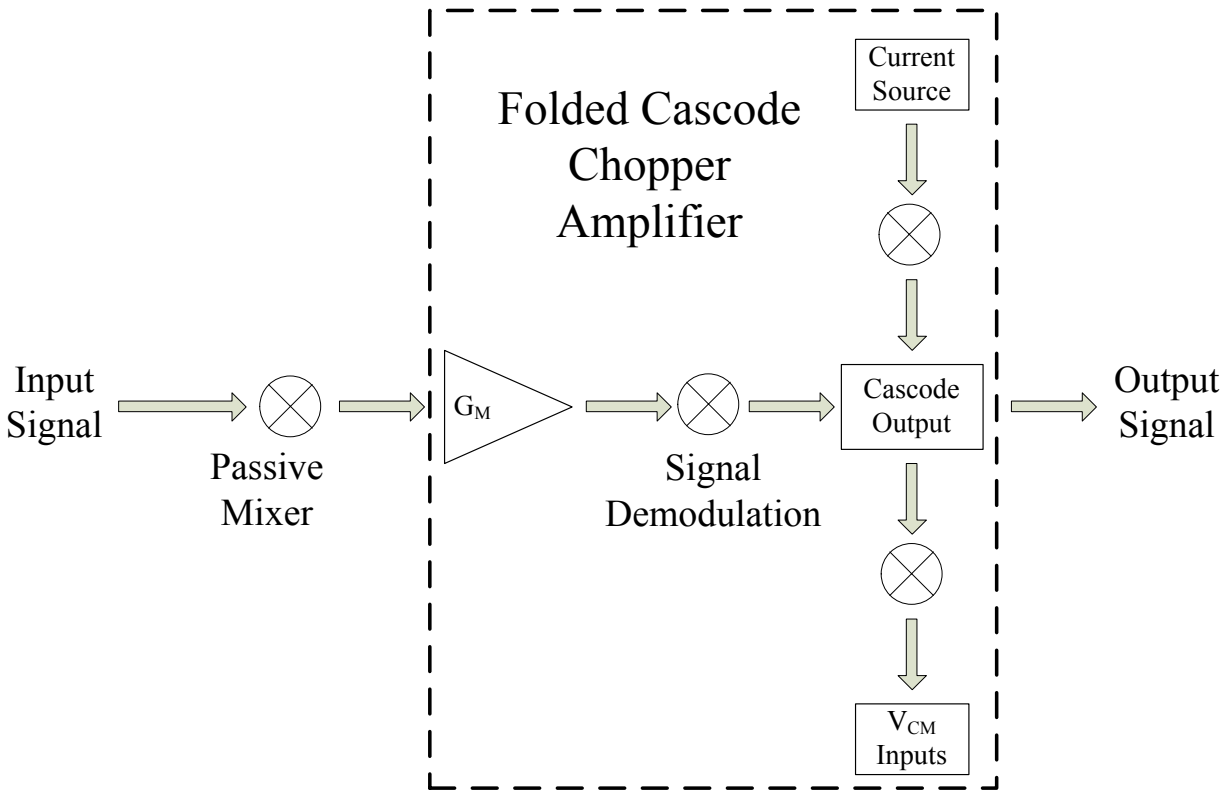

Figure 8: Functional Block Diagram of Chopper Amp

4.3 Common Mode Feedback

Continuous time common mode feedback using a differential pair with diode connected NMOS loads sets the amplifier's common mode output level to VDD/2 or 600mV. Sensing of output common mode voltage levels is done with long-channel PMOS pseudoresistors, a technique that is frequently used throughout this design. A diode connected PNP bipolar transistor is formed by tying the n-well substrate to the source. This transistor conducts very little current and has a high incremental resistance for small differential voltages. The gate is also tied to the drain to diode connect the PMOS so that a high resistance is achieved in both directions for small differential voltages. When measuring LFPs that are 100uV or less, the

chopper amplifier ouput swing will be under 30mV. The resistance of the series pseudo-resistors is in the giga-ohms in this case, which is ideal for common-mode sensing. The large resistance will add noise directly to the input of the second stage amplifier. At this point in the overall amplifier the signal is amplified by 43dB so this effect is minimal when referred back to the input.

The common-mode sensing pseudoresistor noise will also be amplified and added to the noise from the common mode feedback amp. The CMFB amp output noise power is applied to the NMOS devices M11 and M12 (Figure 7), along with the CMFB control voltage, and is further amplified at the output. This noise is upmodulated by the lower NMOS switching devices in the cascode output of the chopper amplifer so that only thermal noise from the CMFB circuit is added in and amplified at the amplifier output in the signal band. Careful design methodology ensures that all flicker noise is upmodulated before amplification at the output.

4.4 Placement of Mixers and Input Caps

Having the passive input mixers first in the signal path, before the 20pF input caps, was a design choice that involved tradeoffs. Another option is to directly couple the input caps to the sensing electrodes in a “capacitor first” design. This is then followed by the mixer and input devices or input devices and then the mixer:

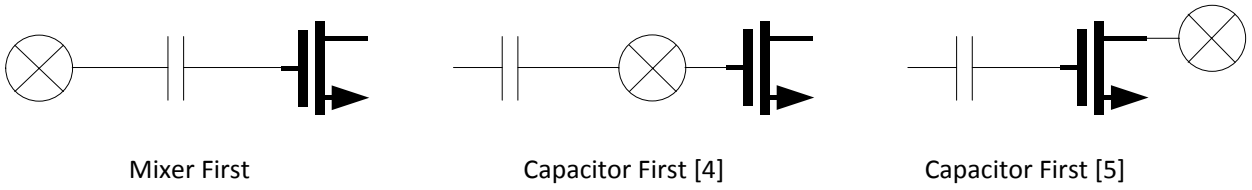

Figure 9: Alternative Input Capacitor and Mixer Ordering

Placing the input caps first has the direct advantage of reducing the DC offset cancellation requirements of the LNA. The input capacitors block the large electrode offsets and the amplifier offset can then be taken care of with resistive feedback. This leads to reduced offset cancellation complexity and higher input impedance. Mixer first topologies, such as the one presented in this thesis, will have a parasitic switched capacitor at the input that lowers the input impedance into the gigohms [4]:

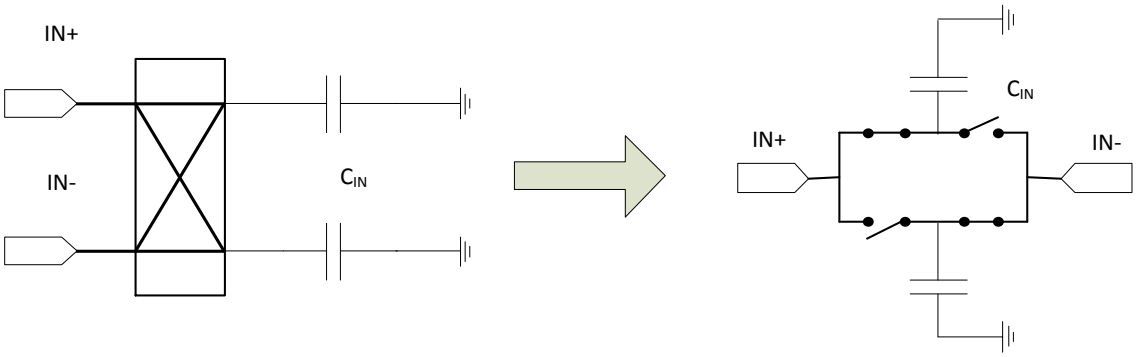

Figure 10: Switched Capacitor Parasitic Resistance at Input Electrodes

The capacitor first topology in [5] has the mixer after the input pair. The input pair is implemented with large area pFETs that are direct 1/f noise contributers in the signal band. Chopping is then possible at a higher frequency of 100KHz because the signal is not applied to the pFET input gates at the chopping frequency. The main reason for the placement of the mixer after the input pair is that the capacitor first topology in [4] has another parasitic switched capacitor at the input device gates. This parasitic resistance to ground results in noise multiplication at the input [5]. The solution involves unreasonably large 100pF input capacitors or else the tradeoff of [5]; placing the mixer after the input FETs. Actual measured output noise voltages are $4uV_{rms}$ integrated from 10Hz to 5KHz and $1.3\ uV_{rms}$ from 0.5 to 100Hz in the designs of [5] and [4] respectively.

The major disadvantage in mixer first designs is that a feedback loop containing an integrator is required to cancel DC offsets because the full electrode offset is upmodulated and passed through the input capacitors. Implementation of this one hundred millihertz low-pass filter has been proven on-chip with switched capacitor integrators [3]. This work is attempting a simplified approach to this that is not practically testable in extracted transient simulations. Real world offset cancellation can take up to 5 seconds to recover from a step input during which time the amplifier is saturated and inoperable [2]. Long transient simulations are too computationally intensive and so actual testing must be conducted. Lower supply voltages also place limits on the theoretical maximum offset that can be cancelled using this approach.

After all design tradeoffs were considered, a mixer first topology was implemented. One important reason is that mismatches in the input capacitors will not convert common mode input variations into offset errors as occurs in capacitor first amplifiers [4]. The magnitude of this problem is unknown, and is probably less significant than the direct DC electrode offset, but still must be cancelled with a low-pass filtered feedback loop [4]. In this case, the major disadvantage of the mixer first topology, the LPF feedback loop, is something that is also required in capacitor first implementations to correct a different problem that arises.

Mixer first topologies inherently have capacitively coupled high-frequency input nodes. This allows feedback to be implemented with precision capacitors [3]. While there is no parasitic switched cap that causes noise at the input, there is one at the electrodes which lowers input impedance. Using the capacitor first topologies implies a choice between two additional noise concerns and the possibility of also requiring a LPF feedback loop. This design is a mixer first topology so that the smallest possible NEF is attained.

5.0 Chopper Amplifier Noise Analysis

The max gain bandwidth of this amplifier is 340Hz and is far below the flicker noise corner in modern submicron CMOS processes. Although careful design methodology and techniques such as those in [1] can significantly reduce 1/f noise in non-chopper amplifiers, and lead to low input referred noise levels, the 1/f noise from the input pair will be present and will depend solely on device sizing. Chopper modulation is explored as a noise reduction technique in this design because the low-frequency signal can be applied to CMOS devices above their flicker noise corners and be amplified such that only thermal noise is added in. The extra power overhead of clock generation is minimized by distribution among multiple chopper amplifiers in many channel sensing arrays and the clocking power per amplifier is typically under ten-percent of each amplifier's total power. For a fractional power increase, noise from the highest noise contributing devices can be greatly reduced.

5.1 Output Noise Reduction via Modulation

The principle of noise modulation via chopping is shown in Figure 11 below:

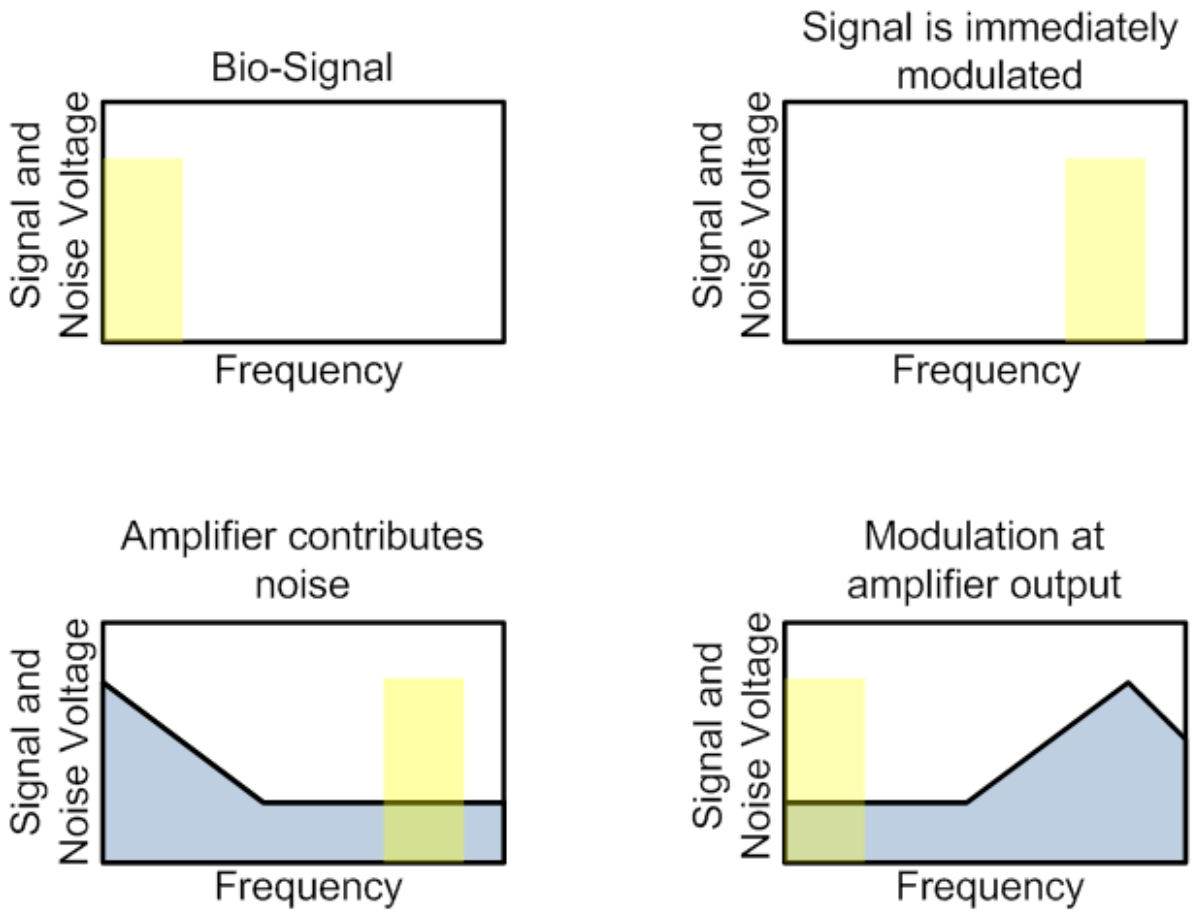

Figure 11: Noise Reduction via Chopping

The passive voltage commutating mixers upmodulate the neural signal and apply it to the input gates of the chopper amplifier at the chopping frequency. The noise floor is assumed to be essentially zero at this point since it is the amplifier device noise that is being analyzed. The signal is amplified and noise is added from the amplifier devices. Only the thermal noise

at the chopping frequency is present in the signal band at the output. Demodulation can be looked at from a small signal perspective. Inside the chopper amplifier, prior to the sources of the cascode devices M7 and M8, the PMOS switches downconvert the signal to DC and signal current flows through the low impedance path to the amplifier output. The 1/f noise is upconverted and is filtered out later along with the "chopper ripple."

5.2 Cascode Device Noise

In the non-chopped cascoded amplifier output shown below, the cascode device noise is attenuated while the input device noise is amplified:

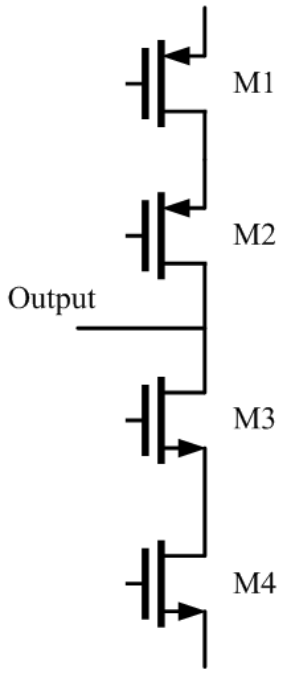

Figure 12: Standard non-chopper Cascoded Output

Source degeneration of M2 and M3 by the drains of M1 and M4 attenuates noise from the cascode devices in equation 12.

$$v_{noise\ M2/3,\ output} = \frac{I_{noise,\ M2/3}}{1+ g_m R_{o,\ M1/4}} R_{output} \qquad (12)$$

Noise currents from M1 and M4 are amplified at the high impedance output in equation 13:

$$v_{noise,\ output\ M1/4} = I_{noise,\ M1/4}\, R_{output} \qquad (13)$$

When choppers are placed at the low impedance nodes between the cascode device sources and input FET drains, noise cancellation still occurs, but with slightly decreased effectiveness.

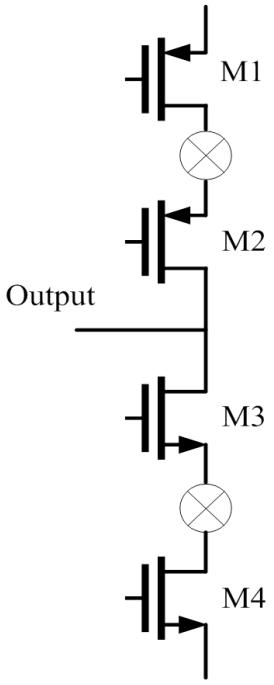

Figure 13: Chopper Amplifier Cascode Output

In the cascoded output with low-impedance node choppers, several different things are taking place. Dynamic component matching is one key reason for utilizing chopping at the output. Any process variations will be averaged out from switching. This allows for much more accurate common-mode feedback and offset elimination. Noise modulation is the other reason to utilize chopping. The 1/f noise from transistors M1 and M4 that would normally be greatly amplified at the output is modulated up to the chopping frequency.

Cascode devices M2 and M3 are on the other side of the mixers at the baseband output node. The cascode devices are the only FETs in this amplifier design that do not have their 1/f noise upconverted and other noise reducing techniques must be relied upon. Fortunately, the cascode device noise is still attenuated to relatively insignificant levels with the mixers placed between the cascode sources and degeneration impedance. Figure 14 shows in the frequency domain how the self-attenuation is occurring with mixers added in:

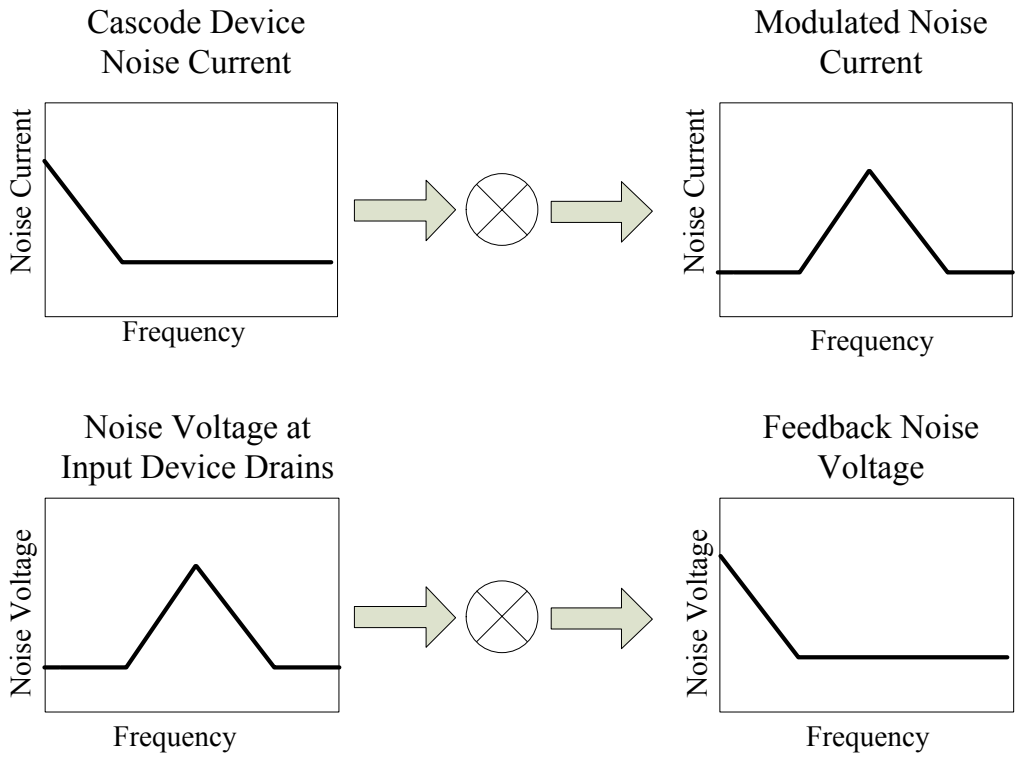

Figure 14: Cascode Device Noise Cancellation in Chopper Amplifier

The noise currents are upmodulated and applied to the degeneration impedances at the chopping frequency. The feedback voltage is then down converted and applied to the cascode device sources where cancellation occurs. Passing the noise current through a mixer twice leads to only slightly less effective noise cancellation per the following equations:

Noise current conversion (-3db):

$$\cos(\omega_{chop})\cos(x) = \tfrac{1}{2}[\cos(\omega_{chop} + x) + \cos(\omega_{chop} - x)] \qquad (14)$$

$$= \tfrac{1}{2}[\cos(\omega_{chop} + x) + \cos(x - \omega_{chop})]$$

Noise voltage conversion (-6dB):

$$\cos(\omega_{chop})*(½[\cos(\omega_{chop}+x)+\cos(x-\omega_{chop})] =$$

$$¼[½\cos(2\omega_{chop}+x)+\cos(x)+½\cos(2\omega_{chop}-x)] \quad (15)$$

Trigonometric identities show the conversion loss associated with passing the noise current through mixers. The amount of negative feedback at the source of the cascode devices is reduced and less effective noise cancellation occurs. Simulated experiments on cascode circuits show that almost all of the output noise is thermal noise from the input nFETs and pFETs downconverted from f_{chop}. Cascode device noise at the output is still kept at a low level with sizing in combination with marginally reduced self-attenuation.

5.3 Chopper Amplifier Noise Analysis Summary

The mixer first topology discussed in 4.5 avoids unnecessary noise contributors at the input in comparison to other options. The three-mixer folded cascode chopper amplifier upmodulates all device 1/f noise from the baseband except for the output cascode FETs. Sizing and self-attenuation of noise currents keeps cascode FET 1/f noise at insignificant levels. The additional mixer on the folded signal path allows the signal current to flow into the low-impedance cascode FET sources at baseband. Separate mixers implement dynamic component matching and noise modulation in the cascode output circuit. The following chapter contains simulated results indicating a competitively low noise efficiency factor (NEF) and the potential for similar actual results after fabrication.

6.0 Cadence™ Simulation Results

Cadence Virtuoso™ was used for schematic and layout design. SPECTRE-RF was the analog simulator used for all transient, AC, noise, PSS, QPSS, PNoise, QPNoise, and QPAC simulations. The first subchapter shows the simulated test results of the entire Bio-LNA along with a discussion of the performance. The next subchapter, 6.2, contains data from simulations that was used as part of the design process.

6.1 Bio-LNA Performance

Running periodic steady state simulations with two chopping frequencies is computationally intensive and difficult to run. Both the signal path and cascode output are chopped at the same 40KHz frequency for most testing so that simulations were able to be successful. Limited QPSS simulations completed when using two different chopping frequencies, and only when they were integer multiples of each other. These results demonstrate improved performance over a single chopping frequency and are included in 6.1.2.

6.1.1 40KHz Chopping Frequencies Schematic Simulations

Figure 15 is an AC gain plot obtained from running a QPAC (Quasi Periodic AC) analysis. Peak gain is 83dB with a 337Hz bandwidth for the two stage Bio-LNA.

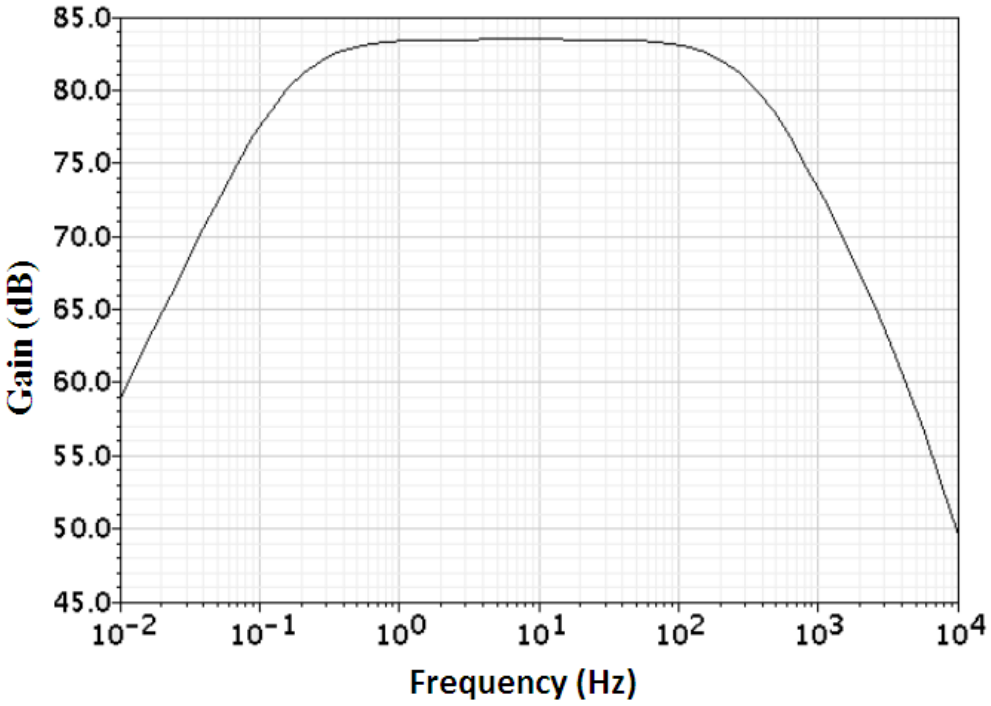

Figure 15: AC Gain

The output noise power spectrum in Figure 16 is also taken from the second stage amplifier output. It shows a 1/f corner close to 1Hz and corresponds to the 340Hz bandwidth of the first stage chopper amplifier.

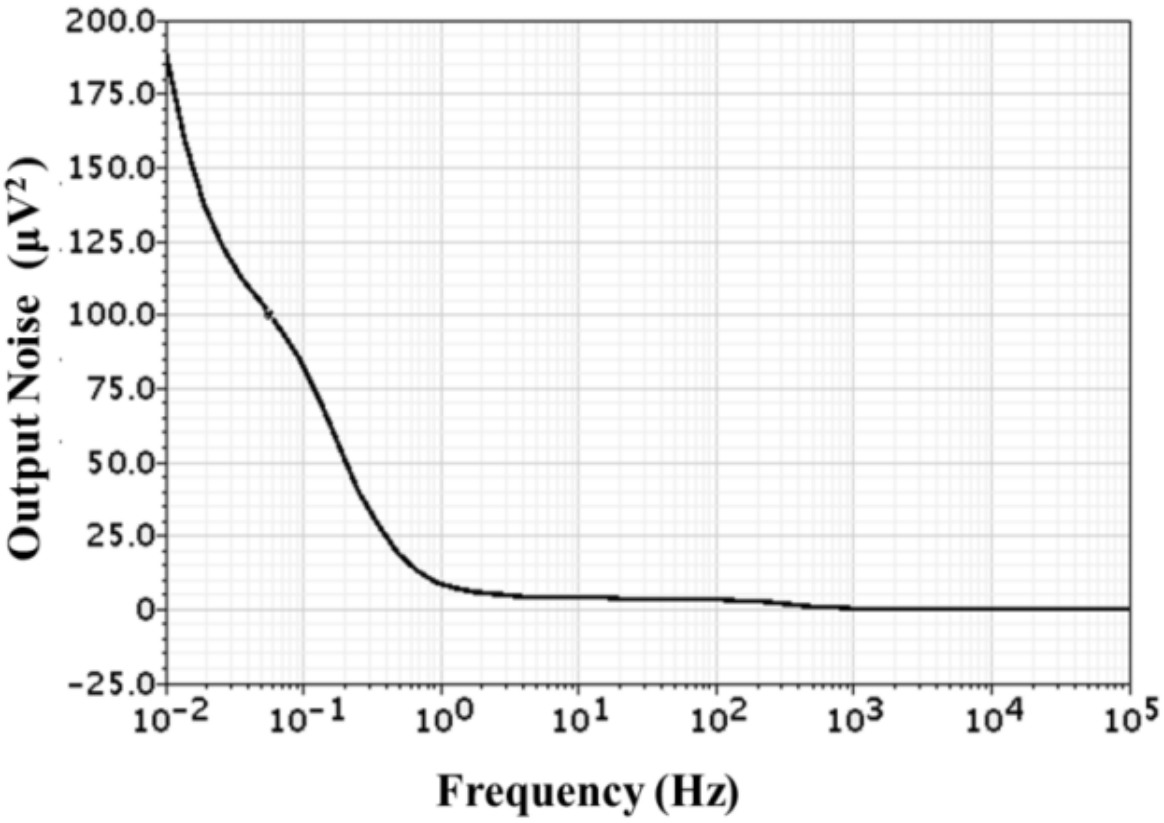

Figure 16: Output Noise Power vs. Frequency

Integrating the output noise from 100mHz to 100KHz gives a value of 1.85 mV^2. Input-referred noise voltage is calculated:

$$V_{ni,rms} = \sqrt{\frac{Total\ Output\ Noise\ power\ (V^2)}{2 \cdot Gain^2}} = 2.06\mu V \qquad (16)$$

The simulations tools also can refer the noise back to the input. Among micro-power neural amplifiers, a noise floor below 100nV/$\sqrt{\text{Hz}}$ is considered good. The simulated input referred noise floor for this amplifier is between 65 – 70 nV/$\sqrt{\text{Hz}}$ with 40KHz chopping frequencies.

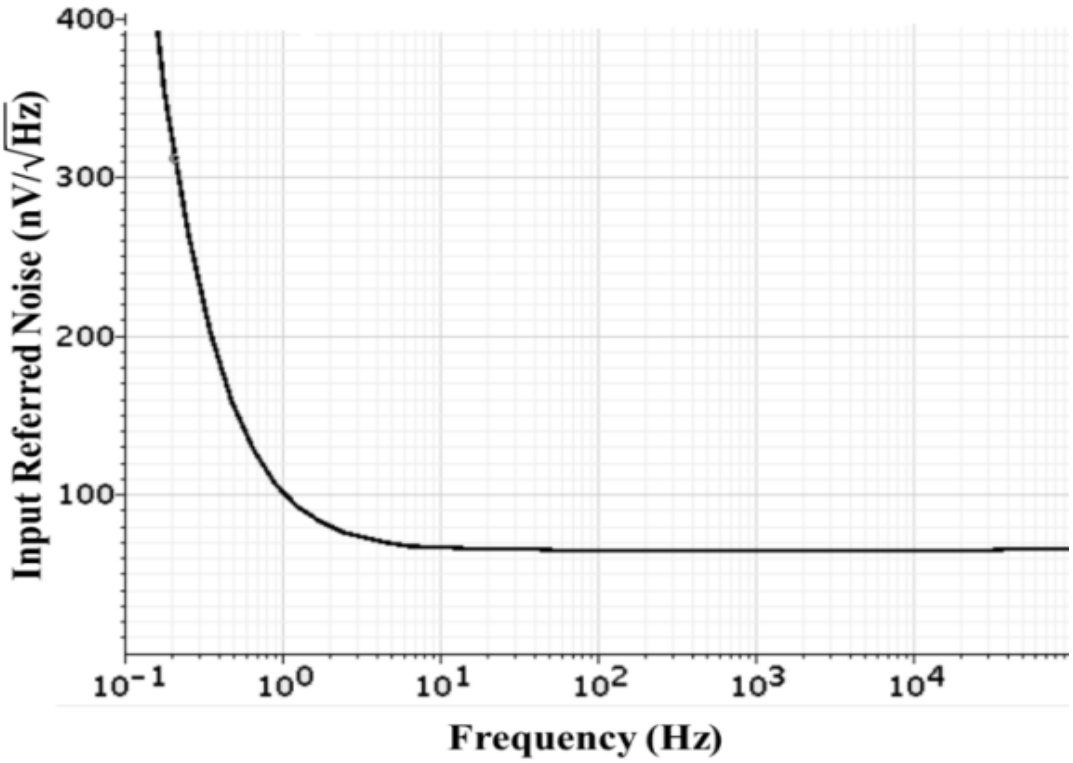

Figure 17: Input Referred Noise Voltage vs. Frequency

QPSS (Quasi-Periodic Steady State) analysis produced the spectrograph in Figure 18. A DC offset is present from the initial startup transient of the second stage amplifier. Measured gain is slightly less than the 83dB that is shown in the QPAC and transient simulations. Harmonic distortion is very low and the 40KHz chopper ripple is significantly attenuated by the second stage amplifier.

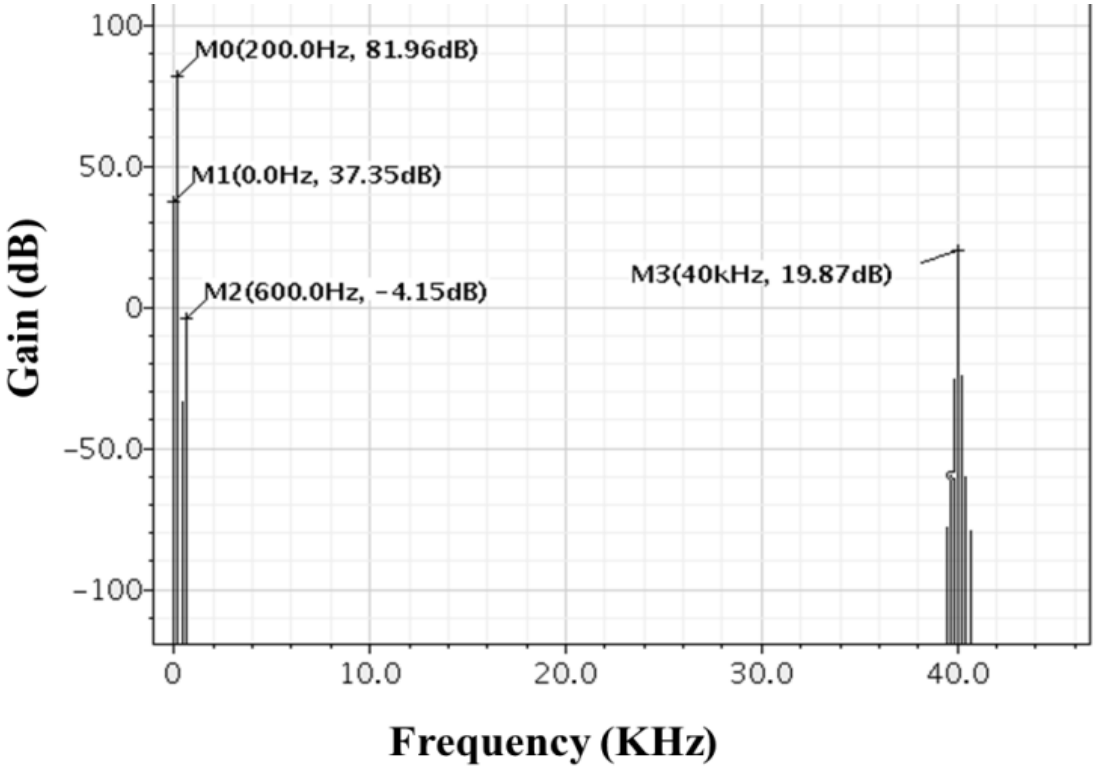

Figure 18: Output Spectrum

These results were obtained with 902nA total bias current for a total power consumption of 1.1uW. The first stage amplifier was biased with 580nA and the second stage with the remaining 322nA.The noise efficiency factor is calculated for the entire two stage amplifier and also for the first stage amplifier by itself—using the same input referred noise as a conservative value and only changing the amount of bias current.

$$\text{NEF} = 2.06\text{uV}_{\text{rms}}\sqrt{\frac{2*902nA}{\pi\cdot V_T\cdot 4\kappa T\cdot 340\text{Hz}}} = 4.1 \qquad (17)$$

$$\text{NEF} = 2.06\text{uV}_{\text{rms}}\sqrt{\frac{2*580nA}{\pi\cdot V_T\cdot 4\kappa T\cdot 340\text{Hz}}} = 3.28 \qquad (18)$$

Noise efficiency factor is a figure of merit that compares the power dissipation to noise tradeoff in biomedical amplifiers. “An amplifier with noise contributed only by the thermal noise of a single ideal bipolar transistor has an NEF =1; all physical circuits have NEF > 1 [6].” When comparing NEFs between designs it is also necessary to look at supply voltage separately to make an accurate comparison: “Note that NEF does not directly account for power dissipation since supply voltage is not present in the expression. However, in modern IC amplifiers, supply voltage only varies by perhaps five (e.g., 1-5V), while supply currents can vary many orders of magnitude (e.g. 1 nA -1 A) [6].” The noise integration bandwidth also directly changes the NEF and there doesn’t seem to be a standard rule for choosing it.

Table 1: Comparison of Amplifiers

Parameter	This Work	[1]	[2]	[3]	[4]	[5]
Technology	0.13	0.5	0.18	0.8	0.18	0.13
Supply Voltage	1.2	2.8	1.5	1.8	1	1.2
Bias Current (nA)	580[a]/902[b]	743	5000	1000	3500	3166
Gain (dB)	43[a]/83[b]	40.9	40.8	41	60	54
Input Referred Noise RMS (µV)	2.06	1.66	1.27	1.3	1.3	4.7
Integrated Noise Bandwidth	100KHz	1KHz	100Hz	4KHz	100HZ	5KHz
High Pass F_{3dB} (Hz)	0.17	0.4	0.5	0.05	?	<1
Low Pass F_{3dB} (Hz)	340	295	100	180	100	5000
NEF	3.28[a]/4.1[b]	3.21	6.1	4.6	9.3	4.4

a. First stage, b. Entire LNA

For comparison purposes, the first stage NEF of 3.28 is used; except to compare to the three stage amplifiers in [2] and [5]. All other amplifiers are single stage.

6.1.2 Dual Chopping Frequency Simulations

QPSS and QPNoise were able to run several times, in schematic, while using different chopping frequencies on the signal path and cascode output sections of the first stage amplifier. The results show that increasing the cascode output chopping frequency will lower output noise levels and that there is an ideal frequency for the input signal to be chopped somewhere between 20 – 40KHz.

Table 2: Dual Chopping Frequency Noise Performance

Chopping Frequency			
Signal Path	Cascode Output	Input Noise (μV_{rms})	NEF
40KHz	40KHz	2.06	3.28
40KHz	20KHz	2.09	3.4
20KHz	40KHz	1.8	3.1
26KHz	52KHz	1.4	2.4

Test results fit the expected theory. Chopping at higher frequencies introduces less thermal noise into the signal band, so the cascode output should be chopped at a higher frequency that maximizes clocking power to noise efficiency. The optimal chopping frequency for the passive mixers and differential nFET input part of the folded amplifier is lower because the signal is at the chopping frequency and there is an upper band limit for the input devices.

6.2 Subthreshold Noise and Transconductance

Many other low-power bio-signal amplifier designs use a pFET input pair. In a standard non-chopped biomedical amplifier this is done because pFETs have less 1/f noise in the signal band. Noise reducing techniques can then greatly reduce the impact of the greater flicker noise from nFETs in the circuit. This section will show the simulation results obtained from the following cascode schematic. Data obtained from the input devices M1 and M4 is used to determine that an nFET input pair should be used in the first stage chopper amplifier where thermal noise is the concern.

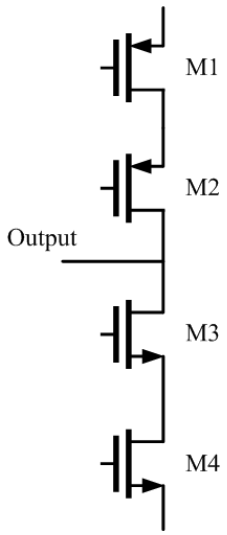

Figure 19: Single Stage Cascode

6.2.1 Cascode Test of Current Gain

The single ended cascode circuit was biased with different levels of subthreshold current. Transconductance was measured with varying device sizes at the different bias current levels. The following tables show these results:

Table 3: Transconductance for 20µM Width Subthreshold FETs

	Channel Length			
	500nM	1uM	500nM	1uM
I_D	nFET		pFET	
50nA	1.79	1.78	1.45	1.44
100nA	3.53	3.51	2.82	2.78
200nA	6.94	6.86	5.45	5.33
500nA	16.84	16.52	12.88	12.49
	g_m (µA/V)			

Table 4: Transconductance for 50µM Width Subthreshold FETs

	Channel Length			
	500nM	1uM	500nM	1uM
I_D	nFET		pFET	
50nA	1.81	1.8	1.49	1.49
100nA	3.59	3.57	2.92	2.9
200nA	7.09	7.05	5.69	5.62
500nA	17.34	17.16	13.62	13.31
	g_m (µA/V)			

Table 5: Transconductance for 100µM Width Subthreshold FETs

	Channel Length			
	1uM	2uM	1uM	2uM
I_D	nFET		pFET	
50nA	1.81	1.8	1.52	1.5
100nA	3.61	3.57	2.98	2.93
200nA	7.15	7.05	5.8	5.67
500nA	17.52	17.18	13.87	13.42
	g_m (µA/V)			

Table 6: Transconductance for 200µM Width Subthreshold FETs

	Channel Length			
	1uM	2uM	1uM	2uM
I_D	nFET		pFET	
50nA	1.82	1.81	1.54	1.43
100nA	3.63	3.59	3.04	3.01
200nA	7.21	7.13	5.96	5.86
500nA	17.8	17.52	14.28	13.99
	g_m (µA/V)			

nFETs have 15-20% higher g_m than same sized pFETs for a given bias current. It should be noted that in subthreshold g_m is linearly proportional to drain current per equation 4 in Chapter 2. Increasing device width has a small boosting effect and increasing length slightly lowers g_m. Essentially the behavior is the same as above-threshold, except changing parameters has a reduced effect.

Using equation 4, the subthreshold slope/κ values can be calculated:

$$\kappa = \frac{g_m \Phi_t}{I_d} \qquad (19)$$

For example: κ is 0.93 and 0.75 for 100:1μM nFETs and pFETs with 200nA of bias current.

6.2.2 Cascode Thermal Noise Test

Output noise of the pFET and nFET devices in the cascode circuit was looked at with SPECTRE™ noise analysis. The following tables contain the measured output noise in micro-volts seen at the high-impedance cascode output. Since the g_m and g_{ds} (output resistance) of the devices are not normalized, the absolute noise can't be compared accurately from test to test. These results show a direct noise comparison between nFETs and pFETs in each individual test, and an overall rough comparison of noise levels for varying device dimensions and bias currents throughout different tests.

Table 7: Cascode Output Noise Levels - 100:2μM

	Bias Current			
	100nA		200nA	
Frequency	nFET	pFET	nFET	pFET
100K	2.1	2.2	2.88	3.04
50K	4.2	4.4	5.76	6.07
40K	5.28	5.53	7.23	7.62
30K	7	7.3	9.55	10
20K	10.5	10.9	14.1	14.9
10K	20	21	25.9	27.3
	Output Noise (μV_{rms})			

Table 8: Cascode Output Noise Levels - 100:1µM

	Bias Current			
	100nA		200nA	
Frequency	nFET	pFET	nFET	pFET
100K	2.18	2.29	3.13	3.17
50K	4.37	4.59	6.25	6.33
40K	5.5	5.78	7.83	7.94
30K	7.29	7.66	10.3	10.5
20K	10.9	11.4	15.2	15.4
10K	20.9	22	27.6	28
	Output Noise (μV_{rms})			

Table 9: Cascode Output Noise Levels - 50:1µM

	Bias Current			
	50nA		100nA	
Frequency	nFET	pFET	nFET	pFET
100K	3.18	3.24	4.28	4.45
50K	6.36	6.49	8.52	8.88
40K	8	8.17	10.7	11.1
30K	10.6	10.8	14.1	14.7
20K	15.9	16.2	20.7	21.6
10K	30.4	31	37.2	38.8
	Output Noise (μV_{rms})			

Table 10: Cascode Output Noise Levels - 20:0.5µM

	Bias Current			
	50nA		100nA	
Frequency	nFET	pFET	nFET	pFET
100K	6.51	6.64	9.71	9.85
50K	12.9	13.2	18.9	19.2
40K	16.2	16.6	23.2	23.6
30K	21.3	21.7	29.6	30
20K	31.1	31.8	39.8	40.4
10K	54.1	55.2	56.1	57
	Output Noise (μV_{rms})			

Two trials on 100µM width transistors were conducted with two different lengths of 2µM and 1µM. The 50µM tests were performed with a single length of 1µM while the 20µM width tests use a 500nM channel length. Another side effect of greater channel lengths is increased output resistances and output noise levels. Changing V_{DS} also affects output resistance in subthreshold, although channel length has a larger effect in these tests. The output noise still sees a net reduction when increasing all four device lengths.

Results show lower noise levels for the two input devices when all four devices are sized with longer channel lengths; indicating that longer channel length and larger width devices produce less thermal noise. Advantageously, increasing the W*L product also decreases 1/f noise. The nFET inputs show slightly better thermal noise performance than same sized pFET inputs under the same bias conditions.

6.2.3 Input Device Discussion

Both the transconductance and noise test results show that nFETs should be used for the input differential pair in chopper amplifiers. Flicker noise is not a concern because of modulatio and nFETs have lower thermal noise levels at the frequencies that were tested (10KHz – 100KHz). Larger device sizes will have lower thermal noise, in addition to 1/f noise, and higher chopping frequencies will modulate less thermal noise back into the signal band. The transconductance testing demonstrates that subthreshold nFETs more efficiently amplify the signal; leading to a higher signal to noise ratio.

7.0. Future Work and Conclusion

The complex non-LTI nature of chopper amplifier and mixer design limited the pre-fabrication analyses that could be run on the extracted design to only DC operating point and transient simulations. Some extracted results are presented and a comparison is made to schematic results. Finally, the chip layout is shown and future testing is discussed to conclude this thesis.

7.1 Extracted vs. Schematic Transient Results

The first figure in this section shows the output of the first stage chopper amplifier in schematic. Very little chopper ripple is present at the output and the magnitude corresponds to a 20uV amplitude input amplified by 43dB.

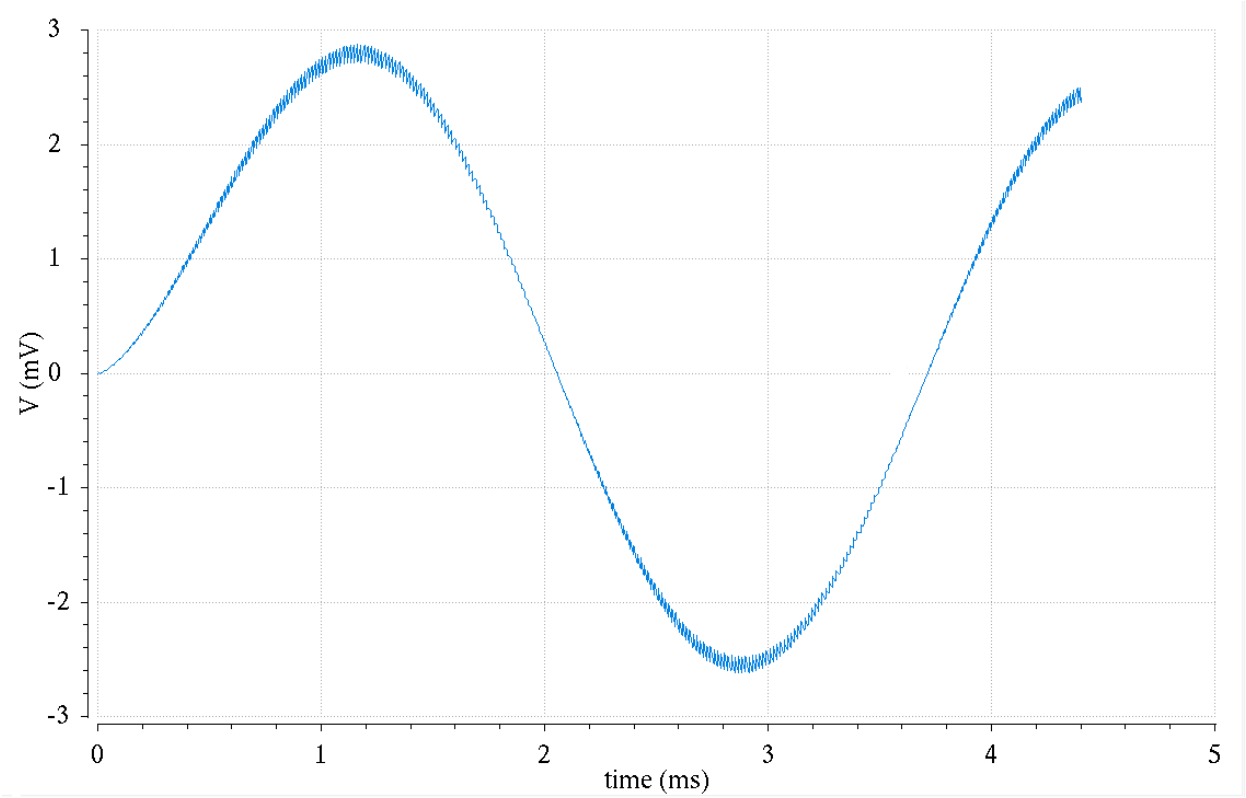

Figure 20: Chopper Amplifier Output (Schematic)

The same 20uV amplitude input signal is applied to the extracted netlist in Figure 21:

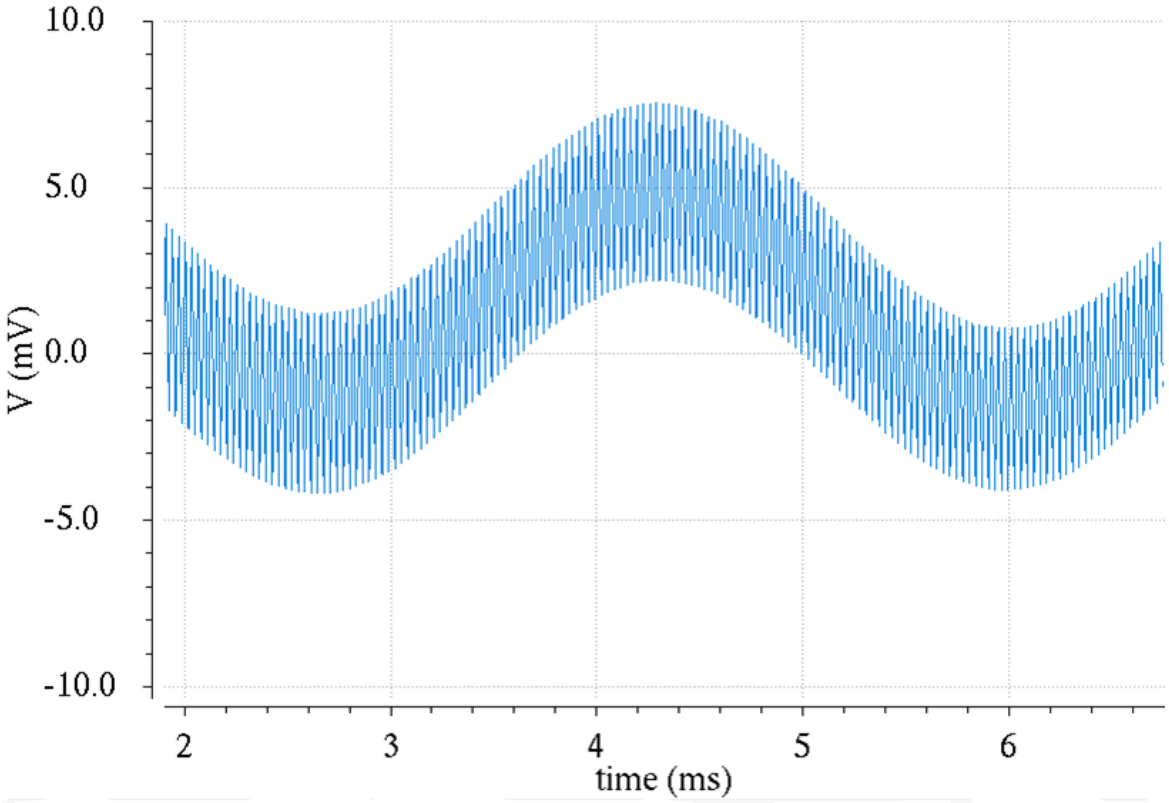

Figure 21: Chopper Amplifier Output (Extracted)

The extracted simulation has a startup time associated with it. Initially there is a DC offset from the first stage that saturates the second stage amplifier. Despite the second stage being capacitively coupled, the initial offset will pass through momentarily until steady state is achieved. There is also significantly more chopper ripple present at the first stage output. Part of this can be attributed to additional parasitics and layout non-symmetries might also have a part. Efforts were taken to match ICW and vias in layout, especially in the first stage. Adding capacitance to nodes in the amplifier is one solution that can be borrowed from RF mixer design, although adding capacitance to subthreshold circuits has the effect of reducing the already low bandwidth. The extracted results from the second stage output show the

effectiveness of the second stage in removing the larger chopper ripple that is to be expected post-fabrication. It is entirely possible that a higher-order lowpass filter will still be required before the data-converter input depending on the application.

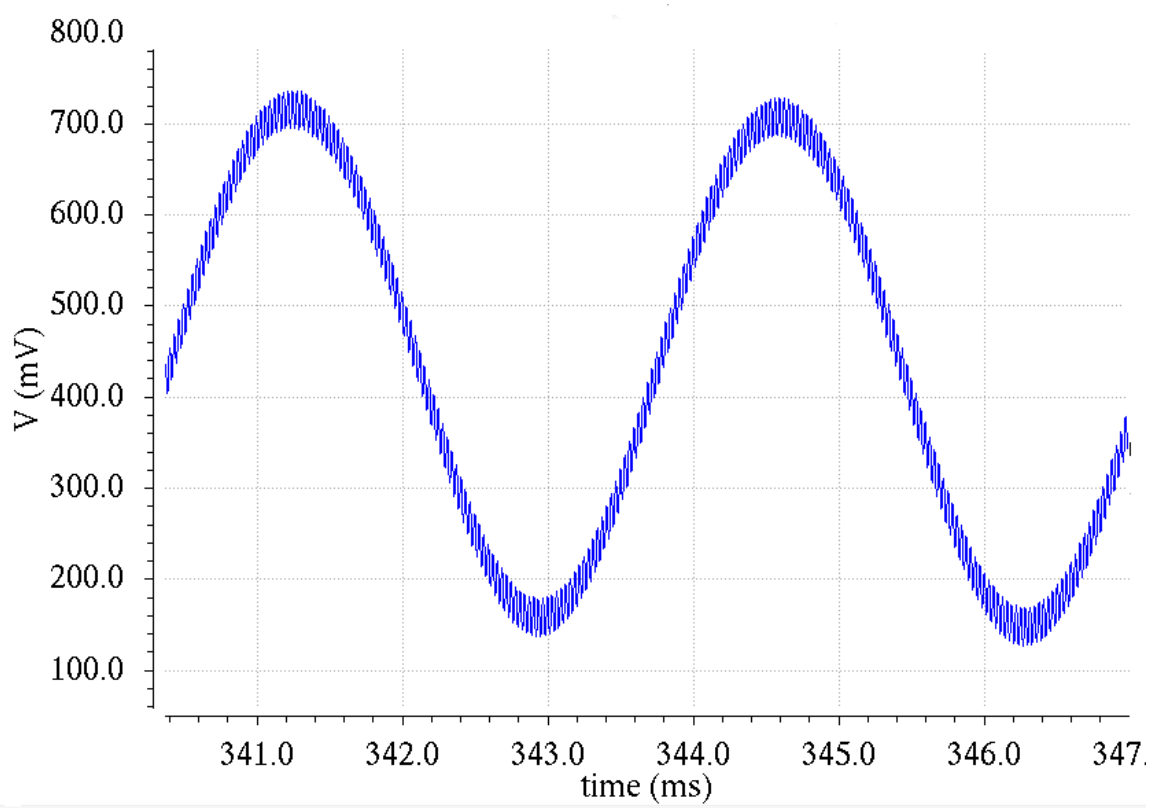

Figure 22: Second Stage Amplifier (Extracted)

The extracted second stage output graph displays 6mS during which time the initial offset is still dissipating. The 20uV signal is amplified by 83dB at the output of the second stage. The chopper ripple at the output of the first stage that is approximately the same amplitude as the signal is now attenuated to 25dB below the signal level.

7.2 Bio-LNA Layout

The chip is awaiting fabrication by MOSIS™.

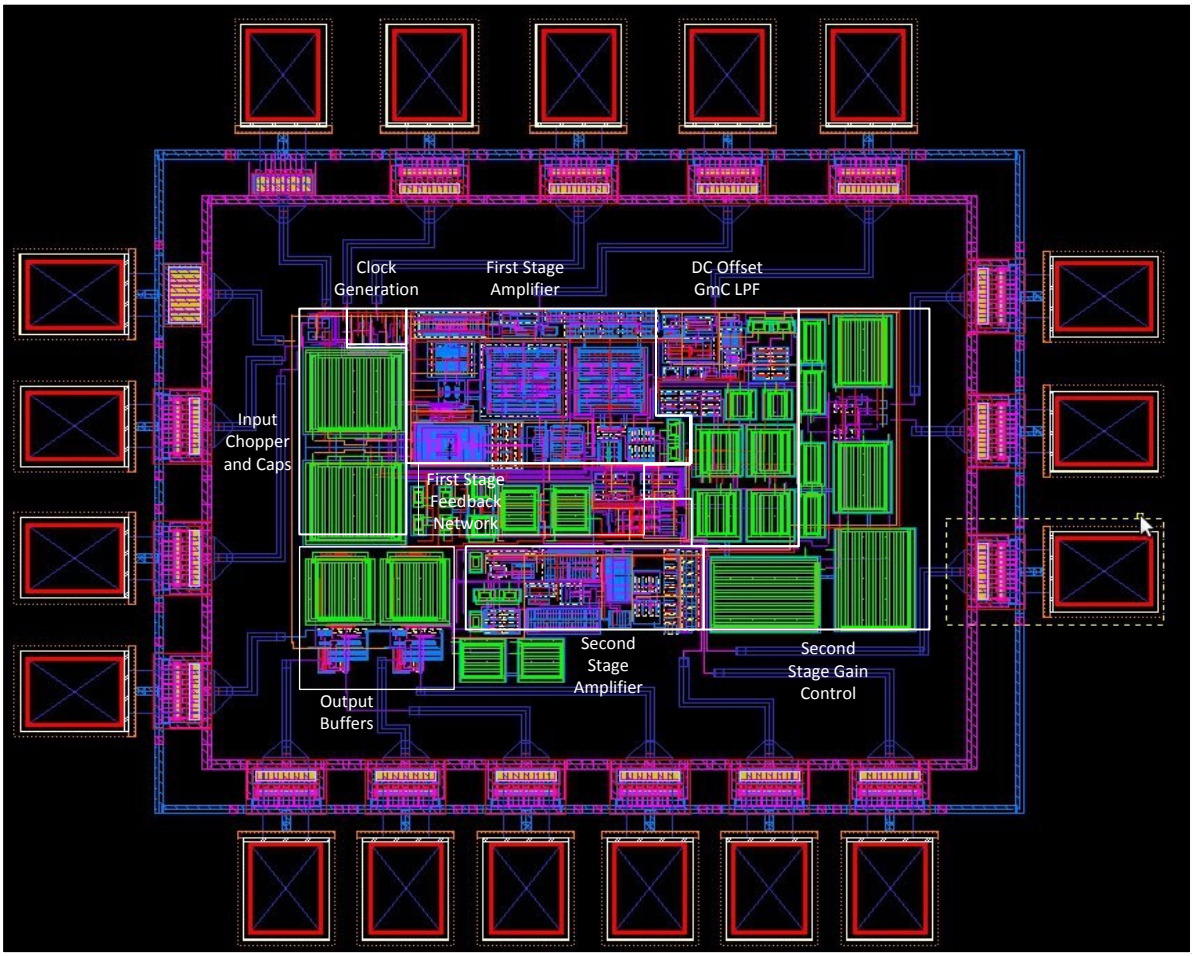

Figure 23: Layout of Bio-LNA

Some notes on the layout: The 20pF dual-layer MIM input caps could be downsized to around 10pF for a relatively small signal to noise ratio decrease. Transistors can be sized smaller in the first stage; depending on the area-to-noise requirements in specific applications. The second stage feedback network uses a lot of area to achieve a high capacitor ratio. A redesigned second stage feedback network is also a possibility. This design leans more towards low-noise than low-area in order to see what noise-to-power efficiency is achievable.

7.3 Future Testing

Testing is highly anticipated and will give much quicker results than software simulations. Changing one or both chopping frequencies will have an immediately visible effect on the noise floor on an FFT display. The same result would take hours, if not days, on a computer.

It is unlikely that an NEF as low as 2.4 from the simulation results in 6.1.2 will be attained, but is not entirely impossible. An NEF of 2.02 is the theoretical minimum thermal noise limit for a MOS differential input [1]. The thermal noise at the first stage chopper amplifier output is mainly from two sources: The cascode output and the folded input pair.

Due to degenerative attenuation, the four cascode FETs contribute less than 2-percent of the total noise in simulations. Actual results should be similar. The rest of the cascode output section of the folded chopper amplifier can be chopped at relatively high frequencies so that minimal thermal noise is passed to the output from the other devices.

The folded input differential pair is on a high frequency signal path between the passive input choppers and the low-impedance node mixer before the first stage cascade output. The input device bandwidth therefore limits the maximum chopping frequency. Theoretically this chopping frequency should be raised until open-loop gain starts to drop; and then backed off. Measured results will prove if this is the case and what the actual output noise levels are for different combinations of chopping frequencies.

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