Signal Integrity of Coplanar Waveguides versus Microstrip Interconnects for Clock Distribution

Austen Clair

A thesis

submitted in partial fulfillment of the

requirements for the degree of

Master of Science

University of Washington

2025

Committee:

Walter Charczenko, Chair

Arnie Berger

Kaibao Nie

Tadesse Ghirmai

Seungkeun Choi

Program Authorized to Offer Degree:

Electrical Engineering

University of Washington

Abstract

Signal Integrity of Coplanar Waveguides versus Microstrip Interconnects for Clock Distribution

Austen R. Clair

Chair of the Supervisory Committee:
Walter Charczenko
Electrical Engineering

This thesis investigates the use of Grounded Coplanar Waveguide (GCPW) interconnects, commonly employed in monolithic millimeter-wave circuits, versus microstrip interconnects for distributing digital clock signals on printed circuit boards (PCBs) with the goal of improving electromagnetic compatibility (EMC) and signal integrity (SI). Two prototype PCBs, one using microstrip traces and the other using GCPW traces, were designed and fabricated using identical materials and layout constraints. Both designs were simulated and measured in the frequency and time domain to evaluate their performance in clock signal splitting and isolation from adjacent transmission lines. Results show that the GCPW-based PCB outperforms the microstrip design in the frequency range from 300kHz to at least 6GHz. The GCPW circuit demonstrated a superior suppression of electromagnetic coupling and crosstalk to adjacent nets, reduced clock skew, lower reflection, and minimized signal attenuation. After propagating through the clock distribution

network, clock signals at the output ports of the GCPW PCB displayed greater signal integrity and a higher isolation between output ports than the microstrip PCB throughout the measured spectrum. Crosstalk measurements taken on a net adjacent to the clock distribution circuit, while clearly quantifiable on the microstrip PCB, were nearly undetectable on the GCPW PCB. This study supports the use of GCPW structures over microstrip for high-performance digital clock distribution to improve EMC and SI.

TABLE OF CONTENTS

List of Figures iii

List of Tables vii

Chapter 1. Introduction 1

Chapter 2. Design of GCPW and Microstrip Circuits for Clock Distribution 10

2.1 Printed Circuit Board Requirements 10

2.2 Clock Distribution Splitter Design 26

2.3 Resistor Selection and Measurement 28

2.4 Clock Delay Line Skew Matching 31

2.5 Intranet Crosstalk Considerations 32

Chapter 3. Time-and-Frequency Domain Simulations For Signal Integrity and Crosstalk 36

3.1 Frequency Domain Analysis (Sonnet Software) 36

3.1.1 Three-Port 1x2 Clock Distribution S-Parameters 39

3.1.2 Two-Port Intranet Crosstalk S-Parameters 49

3.2 Time Domain Analysis (LTSpice) 52

3.2.1 Low-Speed versus High-Speed Clock Signals (10 MHz to 1 GHz) 54

3.2.2 Crosstalk Circuit Model 64

Chapter 4. Measurement of CPW versus Microstrip clock distribution for SI 69

4.1 Frequency Domain Measurements for SI 70

4.2 Time Domain Measurements for SI 81

Chapter 5. Measurement of CPW versus Microstrip for Crosstalk 85

5.1 Frequency Domain Measurements for Crosstalk 85

5.2 Time Domain Measurements for Crosstalk 87

Chapter 6. Findings and Conclusions 91

Bibliography 95

LIST OF FIGURES

Figure 1.1. Clock frequency increasing chronologically in Intel processors [17] 2
Figure 1.2. Signal bandwidth increasing with shorter rise times 3
Figure 2.1. TXLINE calculations for a 50Ω microstrip 12
Figure 2.2. TXLINE calculations for a 50Ω GCPW 13
Figure 2.3. Finite ground coplanar waveguide. Waveguide width (S), center conductor width (W), ground plane width (B) 14
Figure 2.4. Spacing dimensions of shielding vias 16
Figure 2.5. Microstrip Sonnet layout 16
Figure 2.6. GCPW Sonnet layout 17
Figure 2.7. Straight transmission line S-Parameter simulations for GCPW and microstrip. 18
Figure 2.8. Straight transmission line S-Parameter measurements for GCPW and microstrip. 19
Figure 2.9. Proximity of clock distribution circuit to straight transmission line (a) due to narrow gap between ground planes (b) 20
Figure 2.10. Loss for microstrip and GCPW straight transmission line 21
Figure 2.11. Time domain impulse response of straight microstrip transmission line measured and simulated 22
Figure 2.12. Time domain impulse response of straight GCPW transmission line measured and simulated 22
Figure 2.13. Filtered time-domain impulse response of microstrip and GCPW input reflection coefficients (S_{44}) 23
Figure 2.14. Input and output reflection coefficients for microstrip and GCPW transmission lines after applying filtering techniques to impulse response 24
Figure 2.15. Microstrip and GCPW impulse response to 2ns 25
Figure 2.16. Ideal two-port Wilkinson splitter [6] 26
Figure 2.17. Equal-split resistive splitter [6] 27

Figure 2.18. Resistive splitter design: microstrip (a), GCPW (b)..... 28
Figure 2.19. Vishay Dale 50Ω parallel RF SMD resistors (a) and Yageo 16.7Ω SMD resistor (b) 29
Figure 2.20. Asymptotic Bode plot of resistor configurations..... 30
Figure 2.21. Signal traces to ports 2 and 3 (microstrip), designed with identical length but different physical properties..... 32
Figure 2.22. Electric fields between a signal path and a return path and how they might interact with a second net when it is far away (a) and when it is close (b)..... 33
Figure 2.23. Representation of electric fields intercepted by GCPW ground plane..... 34
Figure 2.24. Straight signal trace (port 4 to port 5) adjacent to meandering time delay serpentine on microstrip (a) and GCPW (b)..... 34
Figure 2.25. Fabricated GCPW PCB..... 35
Figure 2.26. Fabricated microstrip PCB..... 35
Figure 3.1. Sonnet PCB layout for microstrip (a) and GCPW (b) with labeled port locations 37
Figure 3.2. A section of curved GCPW transmission line from Sonnet layout..... 38
Figure 3.3. Microstrip simulated S_{21} versus S_{31}..... 40
Figure 3.4. Microstrip simulated output phase at port 2 and port 3..... 41
Figure 3.5. GCPW S_{21} versus S_{31}..... 42
Figure 3.6. GCPW output phase at port 2 (red) and port 3 (blue)..... 43
Figure 3.7. Clock distribution simulated total reflection (S_{11})..... 44
Figure 3.8. Microstrip S_{21}, S_{31}, and S_{23} simulation..... 45
Figure 3.9. GCPW S_{21}, S_{31}, and S_{23} simulation..... 46
Figure 3.10. Microstrip versus GCPW clock distribution total power analysis..... 47
Figure 3.11. Microstrip versus GCPW clock distribution logarithmic power analysis..... 48
Figure 3.12. Simulated results of S_{23} on microstrip and GCPW clock distribution network49
Figure 3.13. Crosstalk simulation signal diagram for GCPW and microstrip PCBs..... 50
Figure 3.14. Far-end cross talk (S_{51}) simulation for GCPW and microstrip..... 51
Figure 3.15. Near-end crosstalk (S_{41}) simulation for GCPW and microstrip..... 52
Figure 3.16. Lumped-element transmission line circuit model..... 53

Figure 3.17. LTSpice resistive splitter model for microstrip (top) and GCPW (bottom). 54
Figure 3.18. LTspice 10MHz clock signal, T_{rise} = 7ns 55
Figure 3.19. LTspice 50MHz clock signal, T_{rise} = 2.5ns 55
Figure 3.20. LTspice 100MHz clock signal, T_{rise} = 0.7ns 56
Figure 3.21. 1 GHz clock signal, T_{rise} = 0.1ns. GCPW attenuation enlarged. 57
Figure 3.22. Enlarged delay and attenuation from LTSplice 1 GHz plot 57
Figure 3.23. MWO microstrip circuit schematic 58
Figure 3.24. MWO GCPW circuit schematic 59
Figure 3.25. MWO 10MHz microstrip clock signal, T_{rise} = 7ns 60
Figure 3.26. MWO 10MHz CPW clock signal, T_{rise} = 7ns 60
Figure 3.27. MWO 100MHz microstrip clock signal, T_{rise} = 0.7ns 61
Figure 3.28. MWO 100MHz CPW clock signal, T_{rise} = 0.7ns 62
Figure 3.29. MWO 1 GHz microstrip clock signal, T_{rise} = 70ps 63
Figure 3.30. MWO 1 GHz CPW clock signal, T_{rise} = 70ps 63
Figure 3.31. Capacitive crosstalk equivalent circuit (50MHz, T_{rise} = 2.5ns) with aggressor net (top) and victim net (bottom) 65
Figure 3.32. 50MHz (T_{rise} = 2.5ns) clock signal on aggressor net (top) and victim net (bottom) 66
Figure 3.33. Enlarged crosstalk waveform 67
Figure 4.1. Microstrip (a) and GCPW (b) clock distribution circuit layouts 69
Figure 4.2. Microstrip S_{21} versus S_{31} measurement 70
Figure 4.3. Difference between S_{21} and S_{31} on the microstrip clock distribution network 71
Figure 4.4. GCPW S_{21} versus S_{31} measurement 72
Figure 4.5. Difference between S_{21} and S_{31} on the GCPW clock distribution network ... 72
Figure 4.6. Microstrip S_{21} versus S_{31} output phase measurement 73
Figure 4.7. GCPW S_{21} versus S_{31} output phase measurement 74
Figure 4.8. Group delay with respect to frequency plot for the microstrip PCB 75
Figure 4.9. Group delay with respect to frequency plot for the GCPW PCB 76
Figure 4.10. Clock skew (|Port 3 – Port 2|) on the microstrip PCB 77
Figure 4.11. Clock skew |Port 3 – Port 2| on the GCPW PCB 77

Figure 4.12. Microstrip versus GCPW S_{23} measurement 78
Figure 4.13. Microstrip S_{11}, S_{22}, and S_{33} measurements 79
Figure 4.14. GCPW S_{11}, S_{22}, and S_{33} measurements 80
Figure 4.15. Total loss measured in microstrip and GCPW clock distribution circuits ... 81
Figure 4.16. 50 MHz clock pulse direct from generator (orange) and on microstrip port 2 (yellow) and port 3 (green) 82
Figure 4.17. 50MHz clock pulse direct from generator (orange) and on microstrip port 2 (yellow) and port 3 (green) enlarged 83
Figure 4.18. 50 MHz clock pulse direct from generator and on GCPW port 2 (yellow) and port 3 (green) 84
Figure 5.1. Crosstalk signal diagram for microstrip (a) and GCPW (b) PCBs 85
Figure 5.2. Microstrip versus GCPW FEXT (S_{51}) crosstalk measurements 86
Figure 5.3. Microstrip versus GCPW NEXT (S_{41}) crosstalk measurements 87
Figure 5.4. Microstrip NEXT measured at port 4 (Ch 2, 0.5mV/div), FEXT measured at port 5 (Ch 1, 0.5mV/div) and input clock pulse (Ch 3, 1V/div) 88
Figure 5.5. GCPW NEXT measured at port 4 (Ch 2, 0.5mV/div), FEXT measured at port 5 (Ch1, 0.5mV/div) and input clock pulse (Ch 3, 1V/div) 89

LIST OF TABLES

Table 1. Findings from Signal Integrity and Crosstalk Measurements 91

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to Professor Walter Charczenko for his invaluable guidance throughout this project. His expertise and mentorship were critical in guiding my research and helping to shape this thesis.

Special thanks to the University of Washington Bothell faculty and staff for an amazing academic experience since 2022.

To my wife Lindsay and my daughter Daniella, your love, support, patience, and resilience made it possible for a working father to realize his dream of becoming an engineer.

To Daniel Glass, whose memory will always inspire me to be better.

Chapter 1. INTRODUCTION

In modern industry, be it commercial, private, defense, or any other technologically dependent sector, it has become crucial that products pass stringent regulatory requirements, enforced by government entities, for said products to reach local and international markets. In decades past, when digital clock rates were regularly 10 MHz or lower, signal integrity (SI) and electromagnetic compatibility (EMC) were not considered when designing digital circuits. With pulse rise times in the past normally bottoming out around 10 nanoseconds, the main concern when prototyping PCBs involved mechanical packaging and layout constraints unrelated to signal integrity issues. This all changed with the emergence of what is commonly referred to as the high-frequency or high-speed regime, where clock frequencies reach 100 MHz or higher, with rise times of 1 ns or less. It is in this regime that SI and EMC must be at the top of the list when considering the best practices for designing circuits involved in the transmission of high-speed digital signals.

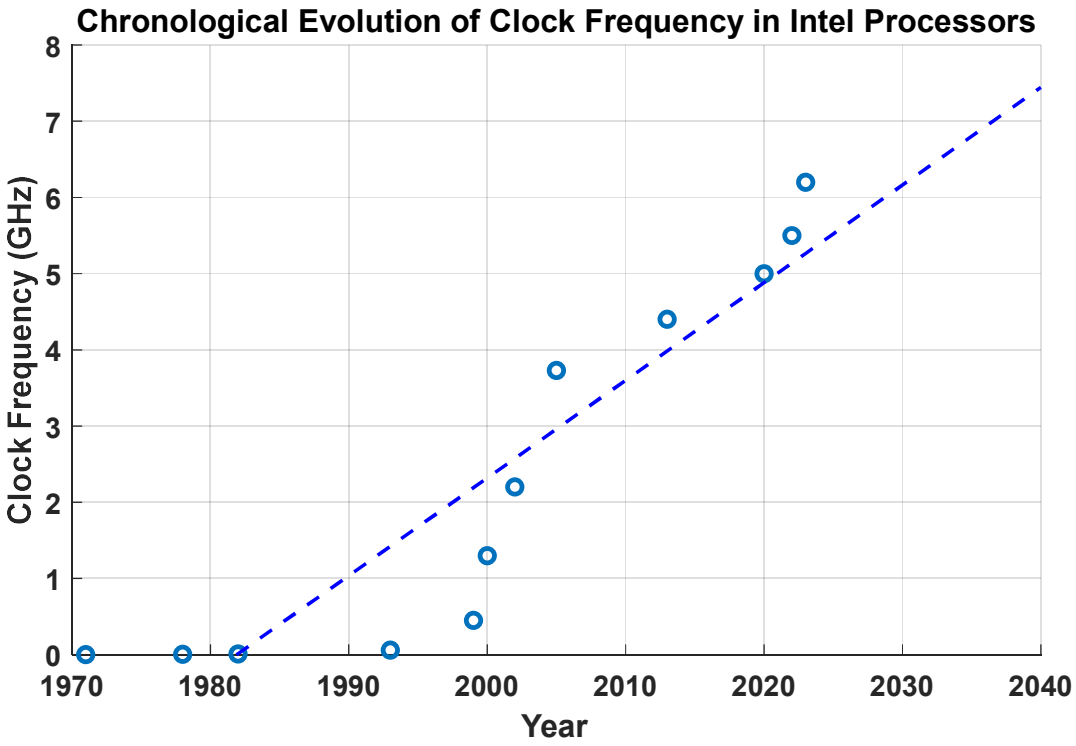

Figure 1.1. Clock frequency increasing chronologically in Intel processors [17]

When discussing SI and EMC, regarding clock and data rates, most problems encountered are inversely proportional to the rise time of individual clock or data pulses. Rise time refers to the time required for a signal pulse transition from a specific lower percentage to a specific higher percentage of its maximum amplitude. Rise times will often be referred to using their specific percentage values, the most common being the '10-90' rise time. This means it takes '*n*' nanoseconds for the pulse to transition from 10% to 90% of its amplitude. It is through the coincidental increase in frequency as rise times decrease that the frequency of signals is even involved. The importance of rise times is due to the frequency components of a digital clock pulse. When decomposed, a digital clock pulse becomes the sum of many sine-wave frequency components, from the 0th to the nth harmonics, which are always odd due to the mathematics involved in their calculations. In simple terms, as rise times get shorter, the frequency of the

signal's components increases. Because of this, the true bandwidth of a digital signal is determined not by the frequency of the signal, but the rise time of the signal's individual pulses. When considering a special case of only some harmonics of a digital signal and fitting a straight-line approximation to the data, an empirical relationship can be approximated with the formula

$$BW = \frac{0.35}{\tau} \quad [1] \ (1.1)$$

where 'τ' represents the 10-90 rise time in nanoseconds, and 'BW' the bandwidth of the signal in Hz that must be considered when designing an appropriate transmission line [2, 3]. In Figure 1.2, a plot of signal bandwidth versus clock rise time is given to show how drastically the bandwidth of a digital signal can increase as its rise time becomes shorter.

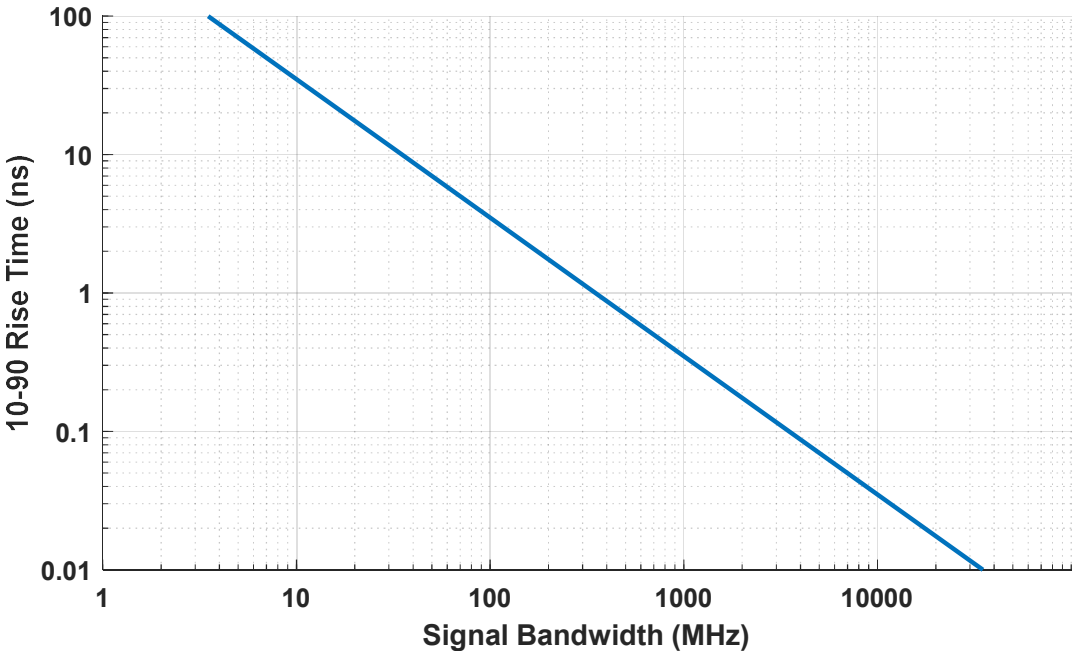

Figure 1.2. Signal bandwidth increasing with shorter rise times

Signal integrity refers to the state of a signal at its terminus compared to its original state at its source. One of a PCB designer's primary responsibilities when designing high-speed digital circuits is to ensure that a signal arrives at its destination having suffered minimal degradation or distortion along its path, mirroring its source state as closely as possible. The ever-shorter rise times in modern digital signals has led to a significant increase in signal integrity issues, and these problems will only increase in frequency as rise times continue to shorten. Some of the main factors that contribute to signal degradation can be attributed directly to the transmission lines that digital signals propagate along, including uncontrolled line impedance, propagation delay, reflective signal distortion from terminations, rise-time degradation due to signal attenuation, ground bounce, rail collapse, and crosstalk noise originating from electromagnetic interference or radiation [1]. To prevent the occurrence of these factors as rise times shorten, transmission line structures that are proven to maintain signal integrity in millimeter-wave and microwave applications can be utilized in digital circuit design. This thesis will compare the efficacy of coplanar waveguide transmission lines and microstrip transmission lines for use with high-frequency digital signals.

Anyone who has encountered transmission line theory when dealing with high-speed signals, be they analog or digital in nature, will be familiar with the necessity of ensuring that transmission lines and terminations maintain a characteristic impedance to reduce reflections of the incident signal. These reflections, if not properly mitigated, will degrade the signal and increase ringing, which takes the form of attenuating interference within the signal pulses. Given that ringing is already a common byproduct of short rise times, aggravating the issue with uncontrolled line impedance will be detrimental to the signal quality at the receiver.

Propagation delay is encountered when two lines that carry identical or inverted signals are not properly matched to the same length. This will lead to signal skew, which cause greater propensity for errors in data detection. While a certain amount of skew is generally acceptable, increasing signal frequencies leaves less room for allowable skew, which when exceeded will increase the risk of sampling errors.

Signal attenuation arises when high-speed signals encounter higher resistance along a transmission line due to skin effect, which is the propensity of a charge to accumulate along the surface of a conductor as frequency increases. This effectively reduces the conductivity of the conductor, thereby increasing the resistance of the line.

Finally, crosstalk refers to the transfer of an unwanted signal from one net to an adjacent net. Crosstalk is commonly encountered when transmission lines carrying unequal signals are routed close together and noise is electromagnetically transferred from one net, referred to as the active net or aggressor net, to the other, known as the quiet net or victim net.

All these problems will be addressed in later chapters. Some of these effects, such as propagation delay and line impedance, can be addressed simply by following best practices in the PCB design phase. Others, such as signal skew and crosstalk, were analyzed and compared on two separate PCBs that utilized different transmission line structures.

Transmission line theory played an important role in the design and testing phases of this thesis. Given the calculation for bandwidth as it relates to rise time (1.1), it becomes clear that a data signal with a short rise time, even when delivered at a manageable frequency of 100MHz, must be treated, when designing a planar transmission line, with as much care as one meant to deliver a radio frequency (RF) or microwave signal. Take, for instance, a 100MHz clock signal with a 10-90 rise time of 0.5 nanoseconds. By utilizing equation 1.1, it is determined that this

would create an operational bandwidth of 700MHz, which requires the use of specific high-speed design practices. Given this criterion and the increasing necessity of SI and EMC in modern circuit design, this thesis focuses on a comparison of two different transmission line structures, routed identically on separate PCBs, and their ability to mitigate signal degradation. One of these PCBs was routed with microstrip transmission lines, the other with grounded coplanar waveguides (GCPWs).

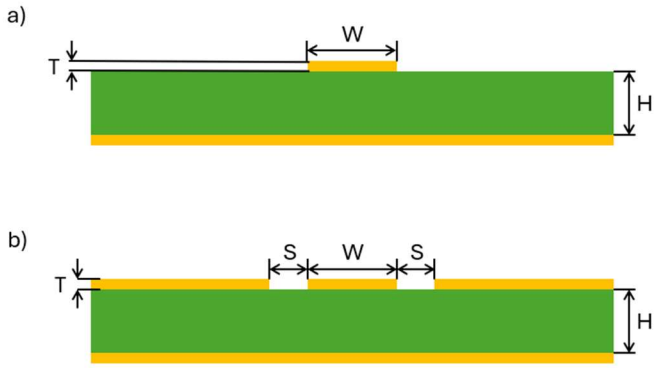

Figure 1.3. Microstrip (a) and grounded coplanar waveguide (b) cross sections.

Figure 1.3 depicts cross sections of both a microstrip transmission line and a GCPW transmission line, where "H" represents the height of the dielectric, "W" the width of the signal conductor, and "T" the thickness of the signal conductor. In the case of the GCPW, "T" would represent the thickness of both the signal conductor and top-ground plane, and "S" represents the waveguide gap between the top-ground planes and the signal conductor. Because of their relatively simple design, fabrication, and integration, microstrip transmission lines are one of the most utilized structures in microwave PCB design. They consist of a simple conducting strip, or trace, separated from a ground plane by a dielectric substrate. Microstrip lines are compact, allowing for

dense circuit integration and facilitating miniaturization, but suffer from certain disadvantages: they commonly exhibit dispersive qualities, where propagation velocity varies with frequency, as well as surface wave excitation, which can result in increased radiative losses. While in many cases these drawbacks can be ignored or managed, they can become critical when designing for signal integrity. Dispersion effectively decreases the circuit's operational bandwidth, which is detrimental when dealing with rise times under 1ns, and increased radiation also increases the likelihood of crosstalk. GCPW transmission lines, used frequently in monolithic microwave integrated circuit (MMIC) design, consist of a central signal trace sandwiched between two ground planes on the same substrate layer. These ground planes are then connected to a bottom ground plane by regularly spaced shielding vias placed along the gaps that separate the signal trace from the top ground planes. These vias serve to provide equal potential between the ground planes at all points along the transmission line. While the impedance of a microstrip line is determined solely by the physical dimensions of the signal trace, the impedance of a GCPW can be manipulated by adjusting the dimensions of both the signal trace and these gaps. While more labor intensive to design and requiring a larger footprint, GCPWs help to mitigate radiation loss and dispersion commonly suffered by microstrip lines due to the shielding nature of the top ground planes and shielding vias. For these reasons, GCPWs tend to be more effective in mitigating crosstalk while also possessing a broader operational bandwidth.

These two transmission line circuits were designed to imitate a common clock tree circuit, utilizing a resistive splitter design to equally divide a digital clock signal and send it to output connectors placed at unequal distances from the input signal source connector. Trace lengths were matched by meandering the trace connected to the closer output, ensuring that both output signals experience minimal phase imbalance upon termination. Both circuits were designed identically

with the exceptions of the width of the signal traces and the addition of the top ground planes and vias required for the GCPWs. The PCBs were designed using Altium Designer software and were simulated with LTSpice, AWR Microwave Office, and Sonnet to analyze their performance in both the frequency and time domains. After all simulated results were analyzed and compared, the PCBs were ordered from a professional board fabricator and subjected to laboratory testing. The PCBs were also subjected to a 50 MHz clock signal with a 10-90 rise time of 2.5ns and analyzed in both the frequency and time domains by utilizing a vector network analyzer (VNA) and digital oscilloscope at the University of Washington Bothell Innovation Capstone lab.

Recent research has been conducted and published regarding some of the topics central to this thesis. GCPW transmission lines are widely known to operate at millimeter-wave frequencies to great effect. In *Wafer Level 3D-Stacked Integration Technology with Coplanar Hot Via MMIC for mm-Wave Low-Profile Applications*, published in *Progress in Electromagnetics Research Letters* in 2024 by Xiaobo Zhu, Yujin Zhou, and Jun Zhou, wafer-scale GCPW technology is demonstrated to produce low insertion loss (within 0.65 dB) and return loss (below -20 dB) at frequencies of up to 40GHz [20]. In *A Compensated Finite-Ground Elevated Coplanar Waveguide Interconnect Strategy for InP Based Integrated Circuits Above 100 GHz*, researchers presented findings at the 19th European Microwave Integrated Circuits Conference in 2024 that show that a finite-ground elevated coplanar waveguide (FG-ECPW) structure can average an insertion loss of only 2.4 dB in the full D-band from 110-170 GHz [21].

Some consideration has also been given to the EMI resilience of microstrip interconnects in high-speed digital circuits. Researchers in Russia, presenting at the 2024 International Ural Conference on Electrical Power Engineering, compared different routing techniques with microstrip transmission lines. They concluded that meandering traces, when compared with inner-

and-outer spiral structures, exhibited the lowest amount of crosstalk at both input and output ports [22].

When searching for references on the performance of GCPW structures with respect to digital signals, however, there seems to be no readily available data. It is inferred, therefore, that the concepts explored in this thesis with regard to the digital signal performance observed on the prototype GCPW PCB are novel in the scope provided by available resources.

Chapter 2. DESIGN OF GCPW AND MICROSTRIP CIRCUITS FOR CLOCK DISTRIBUTION

To accurately compare the performances of both a GCPW and Microstrip PCB, many design considerations must be adhered to. The two PCBs had to be built to nearly identical specifications regarding all physical dimensions, dielectric substrate composition, and conductor height, a notable exception being the composition of the two differing transmission line styles. The designs must also effectively transport and evenly split a high-frequency digital clock signal, while also creating an environment conducive to electromagnetic interference and crosstalk. Given the high frequencies involved in this experiment, it would not suffice to simply split a circuit trace, as will be discussed later in the chapter. Signal integrity was measured using two length-matched traces terminating at different distances from the input, and crosstalk was determined by placing one of these traces near a separate and isolated straight transmission line.

2.1 PRINTED CIRCUIT BOARD REQUIREMENTS

Two prototype PCBs, one routed with microstrip and the other GCPW, were designed using Altium Designer [19], and were made as geometrically identical as possible on the same dielectric substrate. These prototypes, consisting of a clock distribution circuit and an adjacent transmission line, were used to compare the SI performance of microstrip versus GCPW. Some differences in geometry were necessary, as a microstrip of the same characteristic impedance as this GCPW on the same substrate will necessarily have a wider signal conductor, but this is acceptable. The quality and dimensions of the dielectric substrate also required careful selection. In the instance of this experiment, it was necessary to select a low-loss dielectric with consistent thickness and low anisotropy of the medium. For instance, while FR-4 is widely used and

inexpensive, it suffers from a high loss tangent and variable, difficult to predict dielectric constant, which can lead to signal loss and impedance issues. This is due to FR-4's anisotropic properties, which makes it difficult to consistently define a dielectric constant, due to an inability to predict wave propagation within the medium. This, again, could be misconstrued as a design disparity if the dielectric substrate in the two boards react differently to electromagnetic wave stimuli. For this reason, these PCBs were designed using Rogers RO4350B dielectric laminate [8]. This material is isotropic, maintaining tight control of the dielectric constant while reducing dielectric loss. The dielectric layer of these boards will also react more efficiently if it is reduced in thickness, such as in this experiment with 20 mil laminate. This is because a thin dielectric will mitigate unwanted modes and allow for a narrow transmission line.

The other design aspect to be considered in high-speed PCB manufacture is the controlled impedance transmission line. To effectively reduce reflection and loss, the characteristic impedance of the transmission line must be constant and equal to the characteristic impedance of the input and output ports. As 1 ounce copper (approximately 1.4 mil thick) conductor was used throughout both PCBs, characteristic impedance was determined by the width of the signal trace as it pertains to the style of the transmission line. As 50Ω is the characteristic impedance in single-ended industry applications, including the SMA connectors used in this experiment, this is what the transmission lines were designed to. To accomplish this, the AWR TXLINE calculator was used to design the 50Ω transmission line cross-section geometries [7]. Observing Figs. 2.1 and 2.2, the dielectric is set to Gallium Arsenide (GaAs), as TXLINE does not include an option for RO4350B. This can be overcome by simply inserting the appropriate dielectric constant (3.66) and loss tangent (0.0037), which can be derived from the RO4350B datasheet [8].

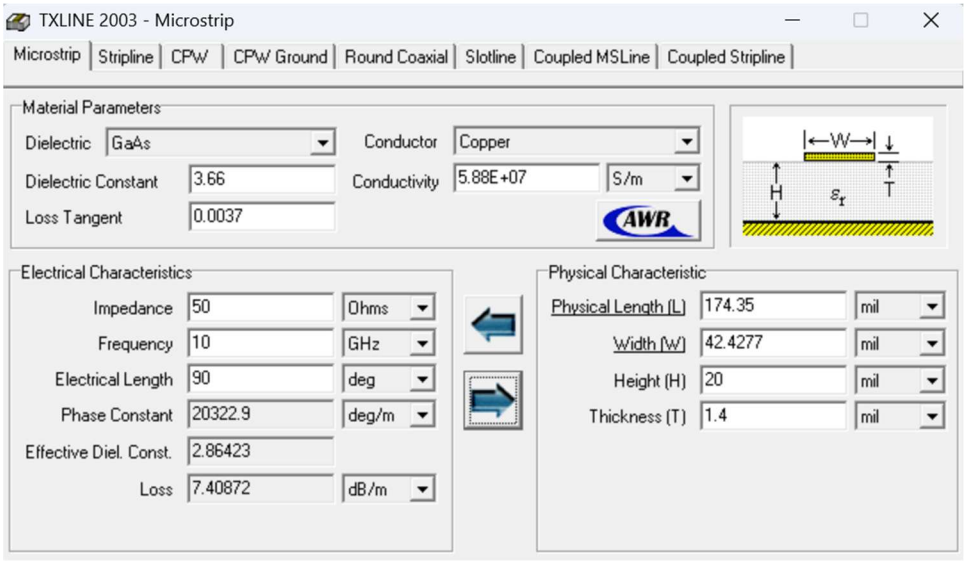

Figure 2.1. TXLINE calculations for a 50Ω microstrip

Appropriate dimensions for constructing a 50Ω microstrip transmission line have been calculated as having a width of 42.43 mil (rounded to 42 mil) when the height of the dielectric is 20 mil, with a conductor thickness of 1.4 mil when using copper, which has a conductivity of $5.88x10^7$ S/m. Besides the width of the conductor, the other calculated parameter of note is the effective dielectric constant of the substrate (2.86 for microstrip, 2.29 for GCPW), which will be required for later calculations. Given the isolated nature of the PCBs used in this experiment, the physical length, electrical length, and phase constant are arbitrary.

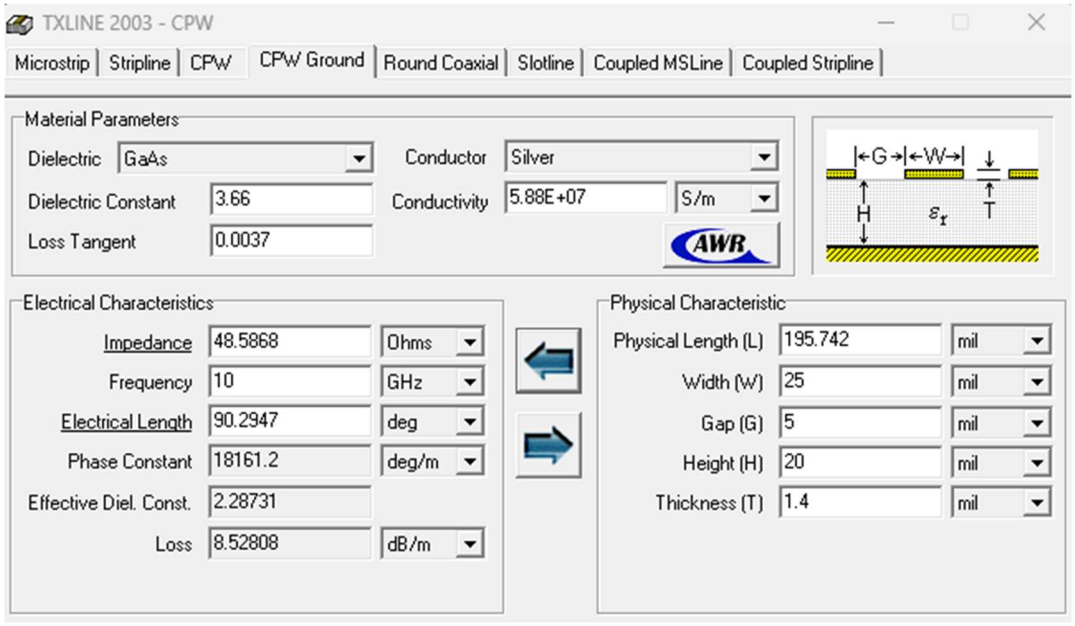

Figure 2.2. TXLINE calculations for a 50Ω GCPW

Dimensions for a 50Ω GCPW transmission line with the same height and thickness show a required conductor width of 25 mil when designed with a waveguide gap of 5 mil, which was chosen to maintain a small footprint while still large enough to be accurately fabricated. The effective dielectric constant is 2.287, which is smaller than the microstrip (2.864), meaning the velocity of propagation in the GCPW is higher. Although dimensions for both PCBs have been calculated and all necessary dimensions for the microstrip line are known, for the GCPW there is still the matter of the ground plane width to consider (Fig. 2.3).

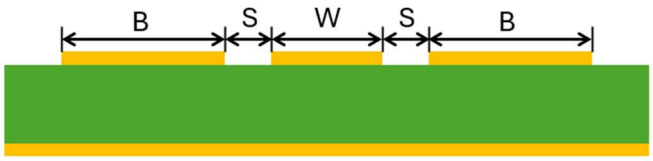

Figure 2.3. Finite ground coplanar waveguide. Waveguide width (S), center conductor width (W), ground plane width (B)

In many cases, it is common practice to multiply the sum of the signal trace and both adjacent waveguide gaps by three to reduce signal attenuation that would be caused by narrow ground planes. Unfortunately, this also raises the question of how much space is available. For this experiment, however, it is important to keep aspects of the footprint as condensed as possible, therefore it has been determined that an alternative design method may be imposed. To paraphrase a report by Dr. George Ponchak, a senior researcher at NASA's Glenn Research Center, to maintain good transverse electromagnetic (TEM) mode characteristics, where the electric and magnetic fields are perpendicular to each other and to the direction of wave propagation, GCPW ground plane width must be less than $\lambda_d/_4$, but greater than twice the width of the center conductor. This is to both counter heightened attenuation and reduce spurious resonances [5]. λ_d represents the wavelength in the dielectric, which can be derived from the equation

$$\lambda_d = \frac{c}{f\sqrt{\varepsilon_{eff}}} \tag{2.1}$$

where $c = 3 \cdot 10^8$ m/s, representing the light speed constant, $f = 10GHz$, which is the maximum frequency in the bandwidth expected for this experiment, and $\varepsilon_{eff} = 2.287$, which is calculated in TXLINE. After calculating for $\lambda_d/_4$ and converting to SI units, it is determined that

the ground plane width must be less than 194.88 mil (0.19488 inches), while still greater than 50 mil, which is twice the width of the center conductor. To maintain a small footprint while leaving a significant margin above the 50-mil minimum, a ground plane width of 70 mil was used for this design.

Another important aspect of the GCPW is the use of shielding vias. These are rows of small, in this case 10 mil diameter, vias that run parallel to the waveguide gaps as well as the edges of the ground plane. While similar via structures have different uses throughout various PCB design applications, for this experiment they serve as a solid connection between the top and bottom ground planes. This works to confine the electromagnetic field produced by the signal trace, reducing the likelihood of interference in the form of electromagnetic coupling between adjacent traces. Common best practice for the design of shielding vias is to space them apart by at least $\lambda_d/_{10,}$ with minimum spacing only determined by the limits of the fabrication process or structural integrity of the PCB. Given the calculation for λ_d (2.1), it can be shown that the maximum spacing required for the bandwidth involved in this experiment is 61.7 mil to effectively block electromagnetic wave propagation. Leaving a margin below the maximum while remaining above the minimum spacing required to maintain the physical durability of the board and meet the minimum spacing requirements of the fabricator, this experiment utilized a spacing of 50 mil between shielding vias, with a separation of 10 mil from both edges of the ground plane.

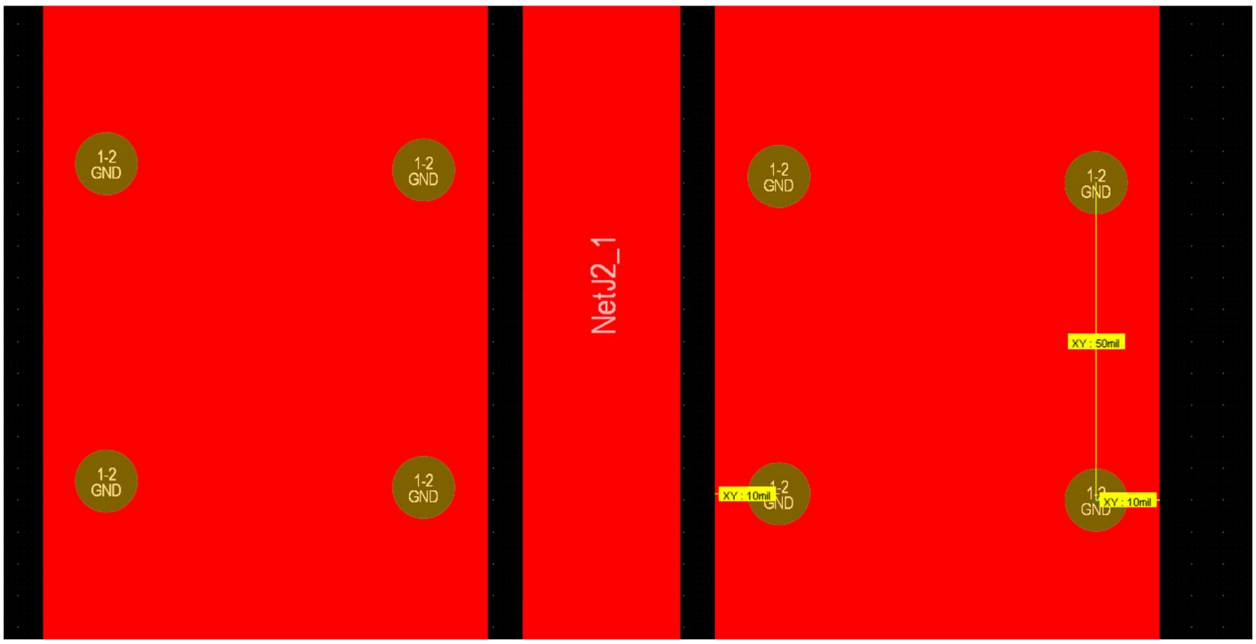

Figure 2.4. Spacing dimensions of shielding vias

As a comparison between the efficiency of GCPW and microstrip lines, the straight transmission lines on each PCB were simulated and measured.

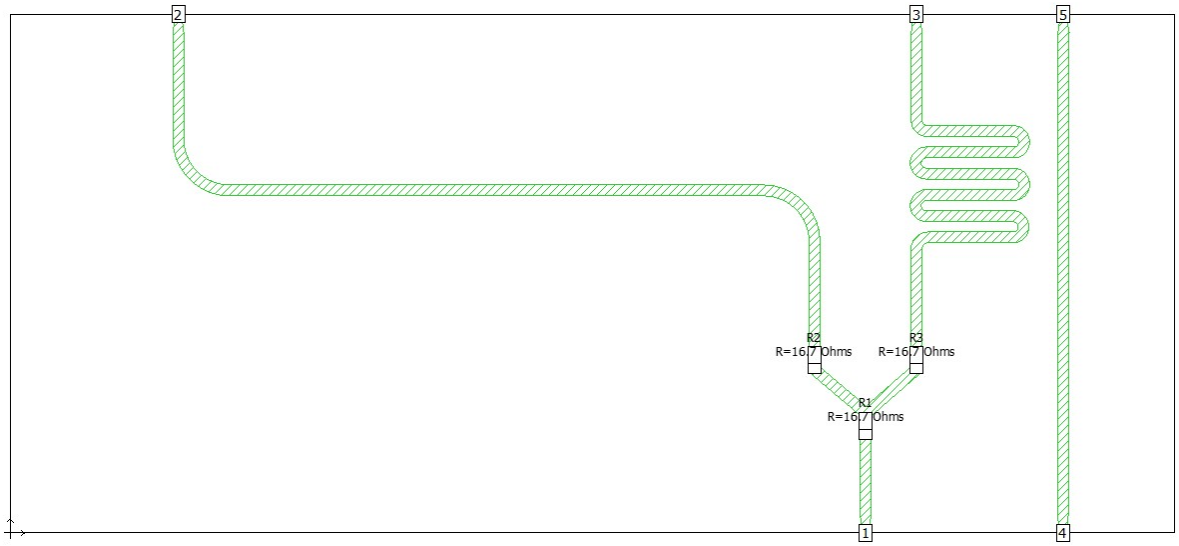

Figure 2.5. Microstrip Sonnet layout

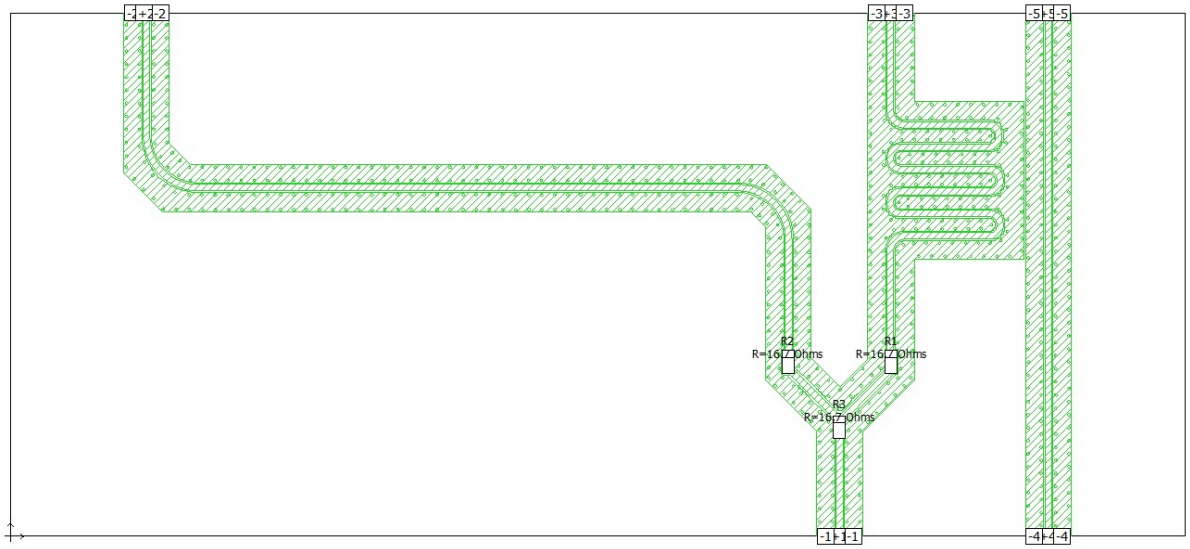

Figure 2.6. GCPW Sonnet layout

Scattering parameters (S-parameters) describe the response of a multi-port network and all associated ports to signals incident to any or all the ports [9]. S-parameter transmission coefficients are labeled alphanumerically in the form of S_{ij}, which would indicate the response of port ‘i’ due to a signal at port ‘j’, or S_{ii}, which represents the reflection coefficient at port ‘i’.

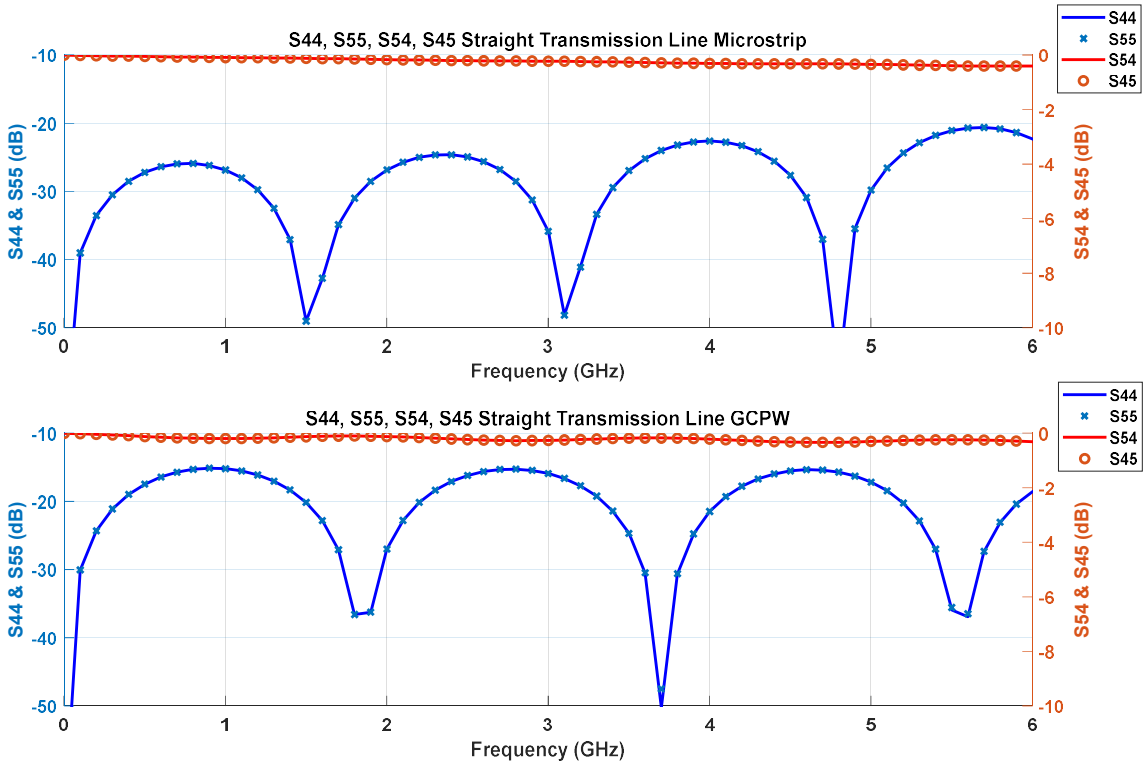

Figure 2.7. Straight transmission line S-Parameter simulations for GCPW and microstrip.

Figure 2.7 shows the expected input and output reflection coefficient equality in S_{44} and S_{55}, which represent the reflection coefficients at ports 4 and 5, as well as port isolation in the matching of S_{45} and S_{54}, which are representative of the transmission coefficients between ports 4 and 5. While the low reflection coefficient and straight S_{45} and S_{54} curves in the microstrip is expected, the GCPW shows about 10 dB more reflection, as well as gently oscillating S_{45} and S_{54} curves, which is indicative of a line that is not impedance matched to the 50Ω ports. In this case, that can be attributed to losses incurred by a lack of proper resolution in the Sonnet layout design. Because the Sonnet simulation for the GCPW was designed with 5 mil cells, and the waveguide gap bracketing the transmission line is also 5 mil wide, there is no error margin in the

simulation, leading to possible impedance mismatches along the transmission line (this will be discussed in more detail in Chapter 3).

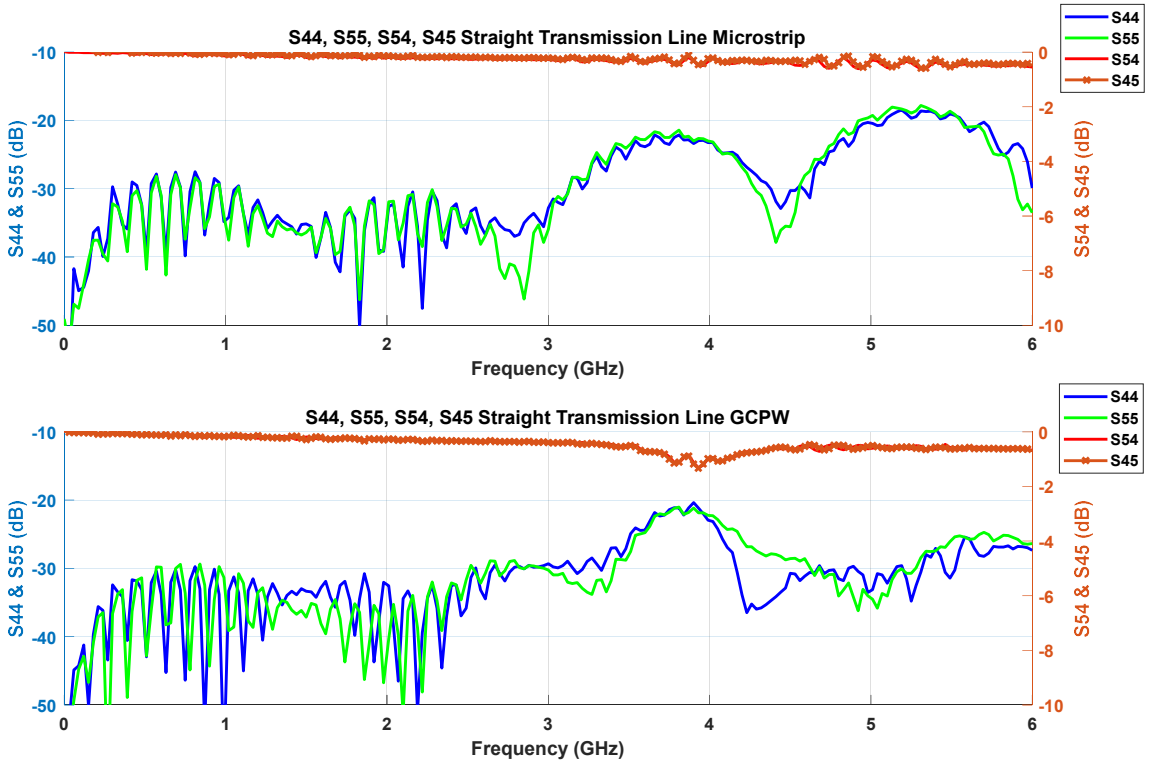

Figure 2.8. Straight transmission line S-Parameter measurements for GCPW and microstrip.

Observing Figure 2.8, the GCPW input and output reflection coefficient's (S_{44} and S_{55}) average magnitude is more in line with expected values for a matched line, remaining under -20 dB for the entirety of the measured spectrum, providing further evidence that the mismatched impedance behavior of the simulated GCPW line is due to the low resolution of the GCPW simulation. There is a discontinuity in the GCPW S_{54}/S_{45} curve, which matches an increase in the reflection coefficient (S_{44}/S_{55}), near 4 GHz. This could be the result of capacitive coupling in the GCPW ground planes between the straight transmission line and clock distribution circuit. Differences in simulated and measured values in Figures 2.7 and 2.8 could be due to unknown

factors in firmware or hardware related to the Tektronix VNAs used in this experiment. The prototype PCBs will need to be tested further on separate equipment to determine the root causes for these discontinuities.

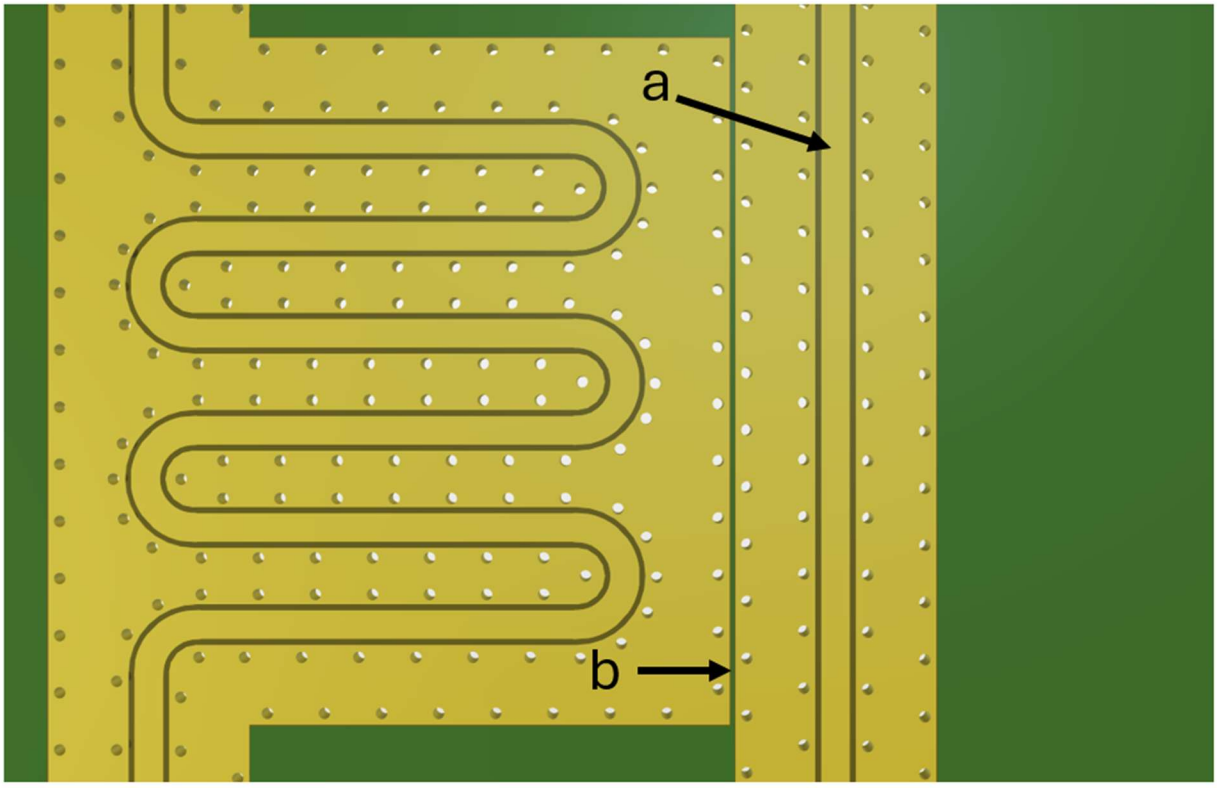

Figure 2.9. Proximity of clock distribution circuit to straight transmission line (a) due to narrow gap between ground planes (b)

It is known that coupled coplanar waveguide structures produce quasi-TEM mode propagation with small losses [13]. This means that, under coupled conditions, there will be some field component in the direction parallel to the transmission line, which is not a desirable effect. It is a primary goal to design transmission lines to operate at a fully TEM mode to reduce loss. Ultimately, this matches the section of the GCPW S_{44}/S_{55} curve in Figure 2.8 at approximately 3.75 to 4 GHz where the line experiences loss that coincides with a slight increase

in input/output port reflection. This added loss can itself be calculated and plotted by using equation 2.1.

$$|S_{44}|^2 + |S_{54}|^2 \quad (2.1)$$

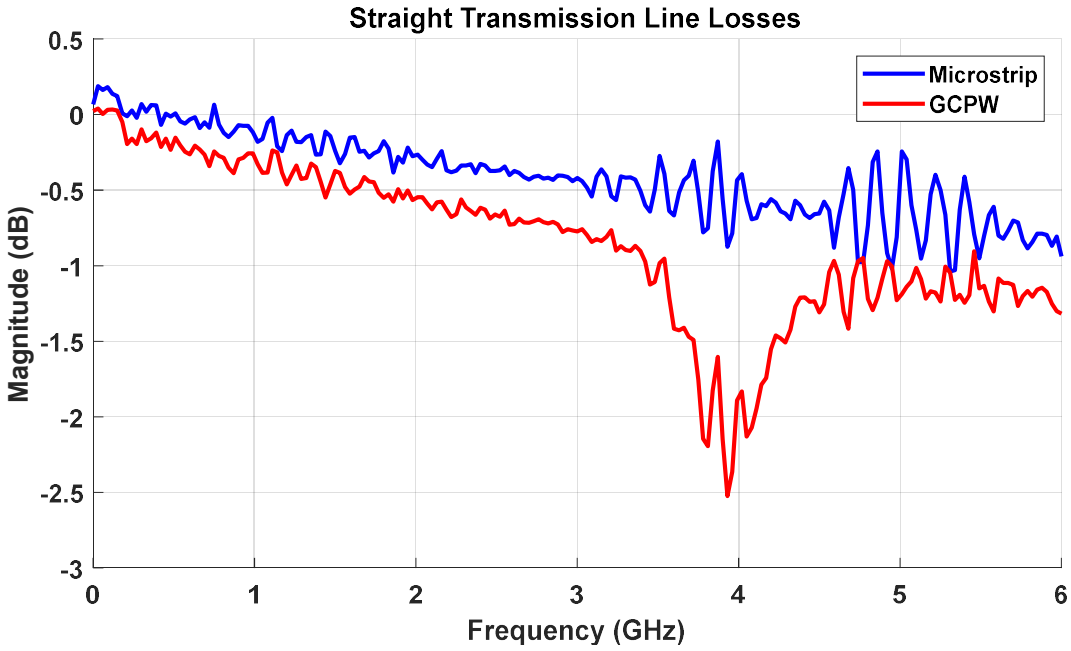

Figure 2.10. Loss for microstrip and GCPW straight transmission line

Figure 2.10 shows that the microstrip transmission line is less lossy than the GCPW by approximately 0.25 dB, with the GCPW exhibiting the same resonance dip at the vicinity of 4 GHz that matches the location of the resonance in the S_{44}/S_{54} data. This could be further evidence of capacitive coupling in the GCPW ground planes.

Present in Figures 2.8 and 2.10 is significant frequency response ripple throughout the measured spectrum. The small change in frequency between each ripple indicates that these are very small reflection coefficients occurring very far apart from each other. To further investigate this phenomenon, the S-parameters from Figure 2.8 were converted to time-domain impulse responses by subjecting S_{44} to an inverse fast-Fourier transform (IFFT).

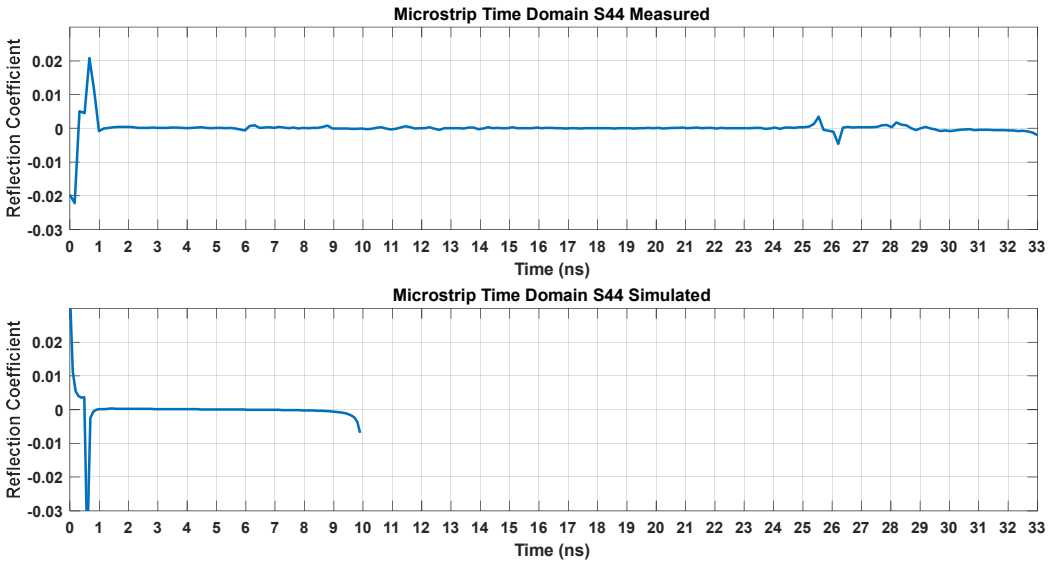

Figure 2.11. Time domain impulse response of straight microstrip transmission line measured and simulated

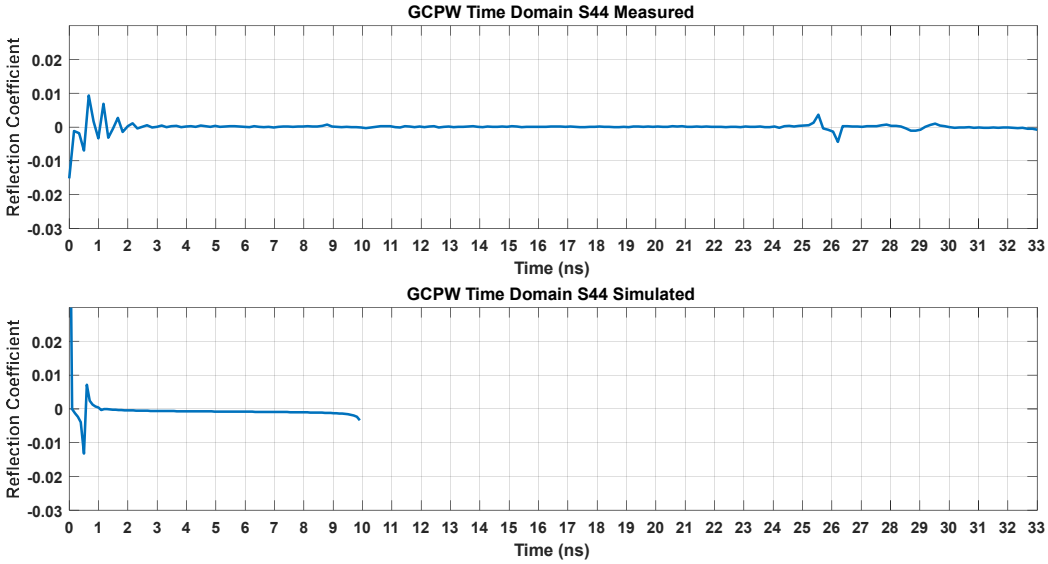

Figure 2.12. Time domain impulse response of straight GCPW transmission line measured and simulated

Because the simulations consist of fewer data points than the measurements, they only provide up to 10 nanoseconds of data. The measurements, however, run all the way to 33 nanoseconds and include a feature between 25 and 27 nanoseconds. Given that a signal only requires 286.6 picoseconds (microstrip) and 256.1 picoseconds (GCPW) for a signal to propagate from one port to the other, the position of the feature is an anomaly that does not conform with the propagation time delay of the transmission line. It is reasonable, therefore, to take steps to remove the feature and observe the resulting S-parameters. This was accomplished by setting all values after 4 ns to zero and converting back to the frequency domain using the fast-Fourier transform (FFT).

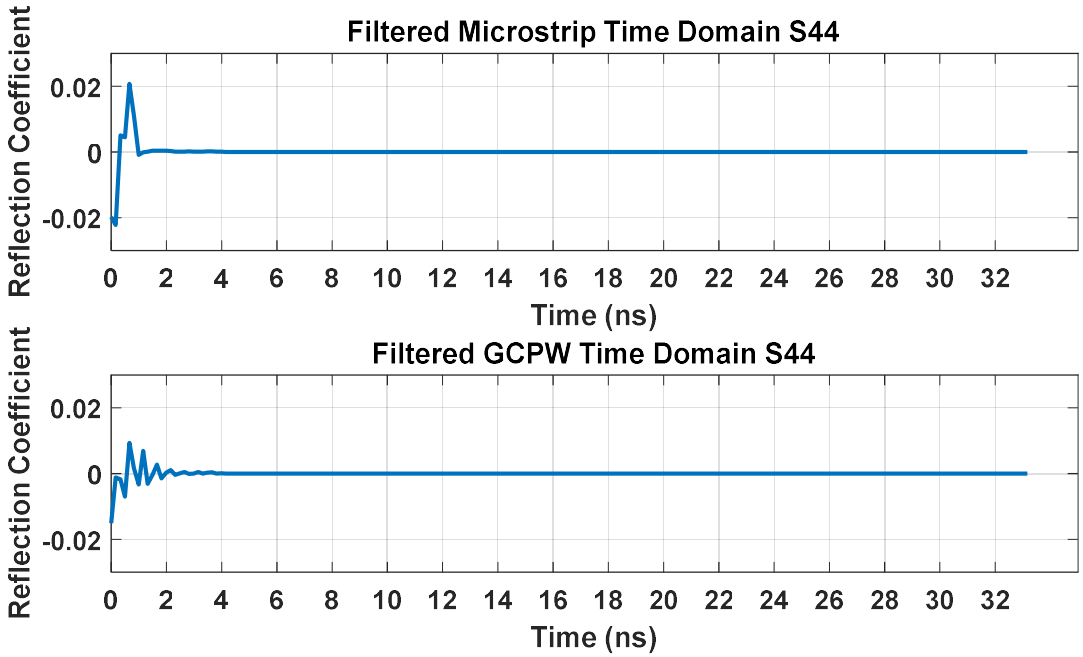

Figure 2.13. Filtered time-domain impulse response of microstrip and GCPW input reflection coefficients (S_{44})

Utilizing the filtered impulse response, the S-parameters can now be re-plotted in the frequency domain to determine if this was the cause of the ripple in the S_{44} and S_{55} curves.

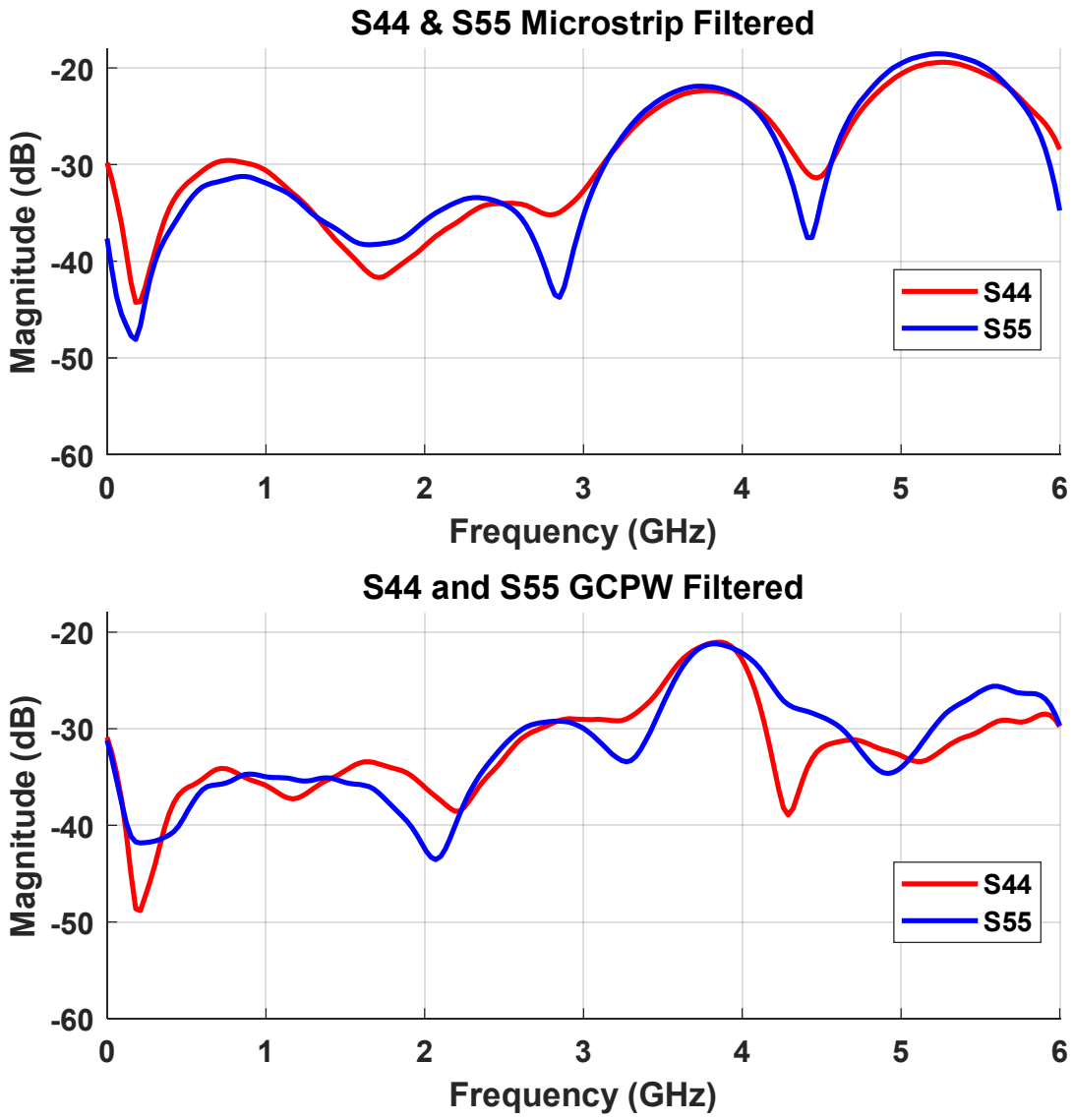

Figure 2.14. Input and output reflection coefficients for microstrip and GCPW transmission lines after applying filtering techniques to impulse response

It is clear when observing Figure 2.14 that the feature at 26 ns on the impulse response graphs of the reflection coefficients of each line is responsible for the frequency response ripple present on the S-parameter measurements and can therefore be discounted.

To observe the data that is most representative to the behavior of the measured reflection coefficients, it is helpful to reduce the timescale of the data to focus only on the first 3 nanoseconds to analyze the initial impulse response on the transmission lines.

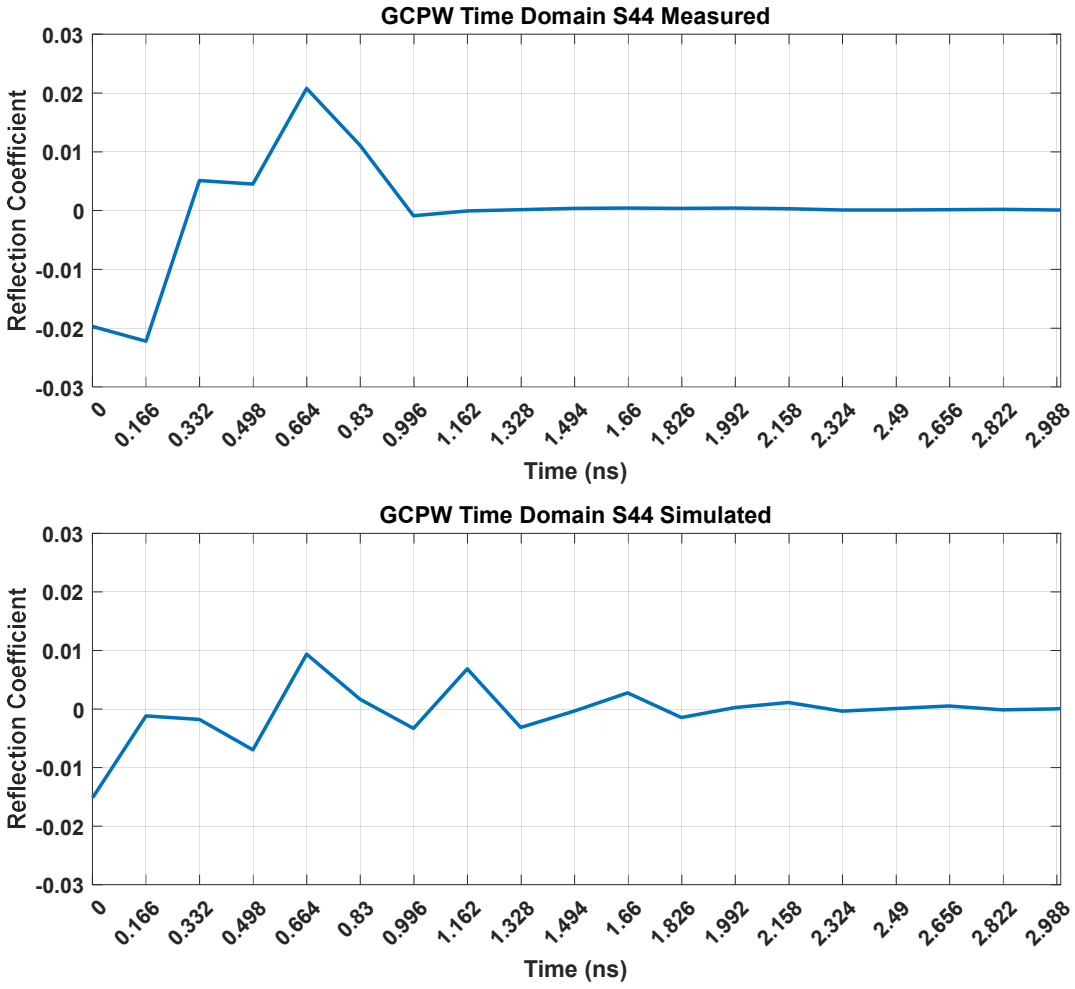

Figure 2.15. Microstrip and GCPW impulse response to 2ns.

In Figure 2.15, individual reflections can be identified as the peaks in the signal following the incident pulse. The microstrip line suffers from one large reflection before stabilizing, while the GCPW signal encounters three successive reflections which are lower in magnitude; that each of these reflections occur at multiples of 166ps is indicative of the sampling rate of the impulse response and is the limit of resolution for the plot given the frequencies measured.

2.2 Clock Distribution Splitter Design

To effectively compare signal integrity maintenance within the two PCBs, it was determined that a highly effective method was to design a clock distribution splitter, which is a method in which one input clock signal is divided into two equal output signals. The equality of these signals, after propagating through two different signal traces, will determine the ability of the PCB to maintain SI. There are several methods utilized in RF engineering to effectively split, or divide, a high frequency signal. A common and effective example is the Wilkinson power splitter in Figure 2.16. This circuit utilizes two quarter-wave transporters and isolation resistor to provide a low loss, fully matched split that isolates both output ports.

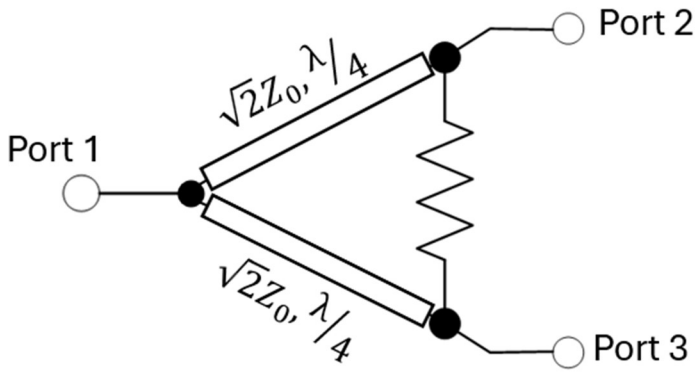

Figure 2.16. Ideal two-port Wilkinson splitter [6]

This approach is perfect for splitting a relatively narrow bandwidth signal while maintaining low losses of input power, as an ideal Wilkinson is 100% efficient. Unfortunately, due to the wide bandwidth of a high-speed digital signal, a Wilkinson is not ideal. Instead, for this experiment, it is acceptable to sacrifice power efficiency in exchange for a wide bandwidth. The resistive splitter (Figure 2.17), while suffering ideally 6.02 dB of net loss, has the benefit of both an extra wide bandwidth and a compact configuration, both of which are advantageous for this experiment.

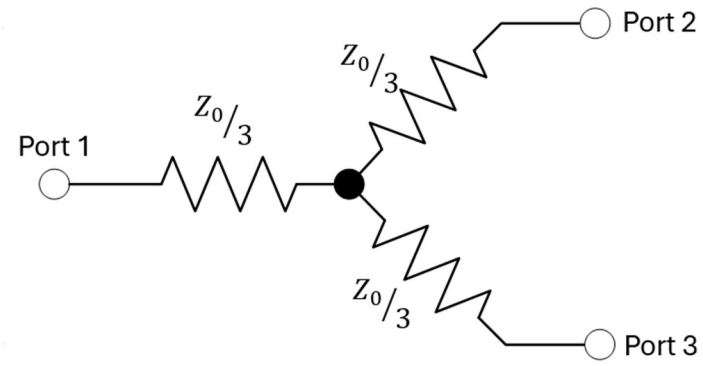

Figure 2.17. Equal-split resistive splitter [6]

Given the 50Ω characteristic impedances of the two PCBs in this investigation, $Z_0/3 =$ 16.7Ω. Designing for two geometrically equal PCBs in GCPW and microstrip, the design of the resistive splitter only varies between boards in the width of the signal trace and the presence of the top ground planes.

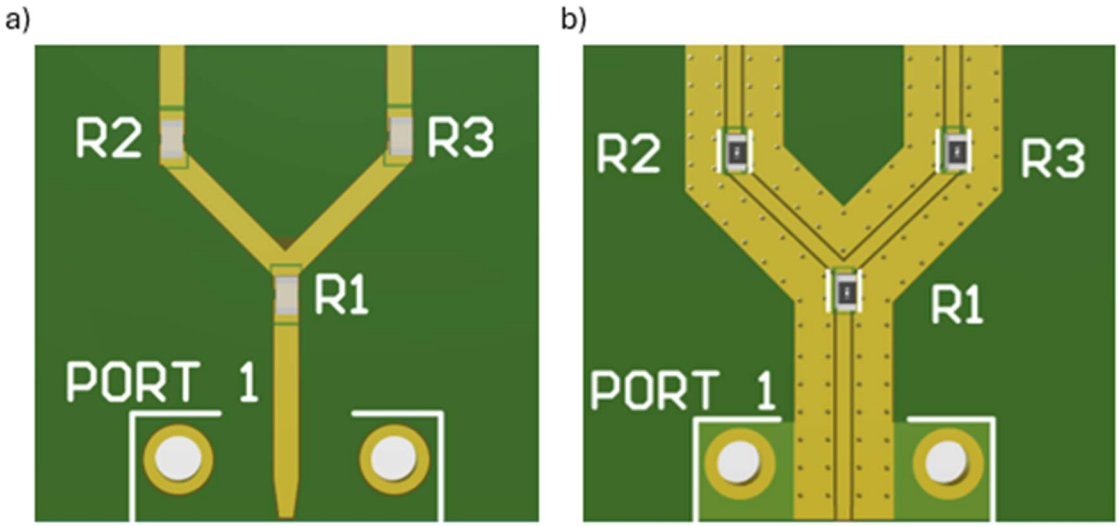

Figure 2.18. Resistive splitter design: microstrip (a), GCPW (b)

2.3 Resistor Selection and Measurement

Given that the characteristic impedance of the transmission lines on both PCBs is 50Ω, the resistive splitter in the clock distribution circuit requires three 16.7Ω resistors. Normally, in any low-frequency circuit, resistance values are constant and unchanging. When dealing with high frequencies, however, a resistor may exhibit purely resistive, inductive, and capacitive behaviors depending on the frequency it is subjected to. For this reason, some companies will fabricate RF-rated surface mount resistors, to extend the operational bandwidth at which a resistor will avoid capacitive or inductive behavior. For this experiment, two resistor configurations were tested to determine if one is more capable than the other at maintaining the 16.7Ω required for the clock distribution circuit.

The first resistor to be considered is a standard Yageo RT0603BRD0716R7L 16.7Ω +/- 0.1% 1/10W 0603 thin-film surface-mount resistor [11]. It is a standard, low-cost resistor of a type widely used for PCB applications involving DC to low-frequency signals. The

second resistor to be considered is a Vishay Dale FC0603E50R0BST1 50Ω +/-0.1% 1/8W 0603 RF/High Frequency 0603 thin-film surface-mount resistor [12]. These resistors are made specifically for high-frequency applications of up to 40 GHz and are designed for low internal reactance. They are expensive and limited in their available resistive values, which is why, rather than using a single 16.7Ω resistor, three have been stacked and soldered together in parallel for the requisite $Z_0/3$ resistance.

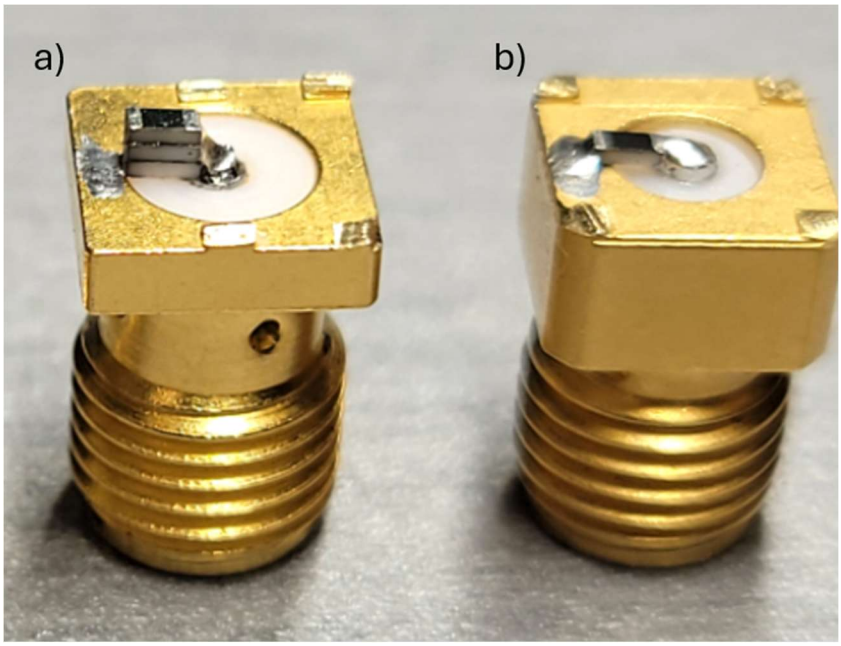

Figure 2.19. Vishay Dale 50Ω parallel RF SMD resistors (a) and Yageo 16.7Ω SMD resistor (b)

To test the frequency response of these configurations prior to gathering data on the resistive splitter circuit as a whole, the resistors were soldered across the signal and return paths of two modified SMA connectors and their RLC behavior was analyzed with a VNA.

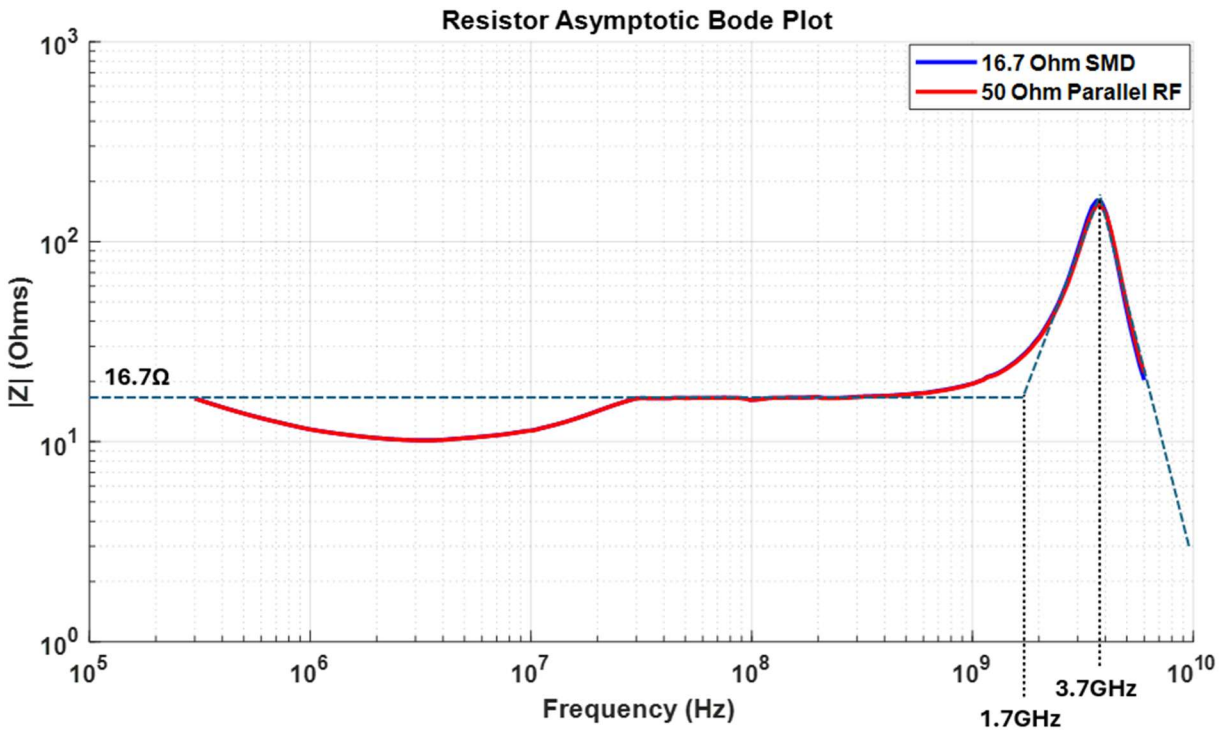

Figure 2.20. Asymptotic Bode plot of resistor configurations

The impedance of each resistor configuration from 300KHz to 6 GHz, which is the bandwidth of the Tektronix TTR506A USB VNA, is shown in Figure 2.20. The results from both configurations are closely related, with a slightly flatter curve from the three parallel RF resistors, which were selected for further experimentation. The flat portion of the plot represents the bandwidth of purely resistive behavior, which only occurs between 300 kHz and 1.7 GHz. This is the operational bandwidth of the resistors, after which they suffer from inductive behavior. The resonance frequency of 3.7 GHz represents the point at which the resistors become capacitive until the end of the measurement at 6 GHz. From this plot, it can be surmised that both resistor configurations only operate as true resistors up to approximately 1.7 GHz. Because of the non-ideal nature of these resistors, they may act as series inductors up to the resonant frequency, and parallel capacitors for the rest of the spectrum. This parasitic capacitance and inductance will

affect the impedance and circuit performance of the resistors when the prototype PCBs are measured in a laboratory environment. The slight dip in the plot from 300kHz to 30MHz is unexpected but could possibly be attributed to a small LC section between the resistor and the end of the calibrated test cable in the form of the modified SMA used to mount the resistors (Fig. 2.19). It will be worth revisiting this problem in the future by extending the calibration plane and observing whether or not this dip is removed.

2.4 Clock Delay Line Skew Matching

To effectively measure the ability of both PCBs to maintain signal integrity, it is beneficial to measure the output of two lines that maintain the same input signal and are of identical lengths but are designed to differing geometric specifications. In the case of this experiment, one line takes a curved 90-degree turn after the signal split, ran straight for approximately two inches, followed by another 90-degree curve to port 2. The adjacent line, however, follows a direct path forward to port 3, and includes a meandering time delay structure to ensure that its length is identical to the trace terminating at port 2. Ideally, ports 2 and 3 will produce an identical signal.

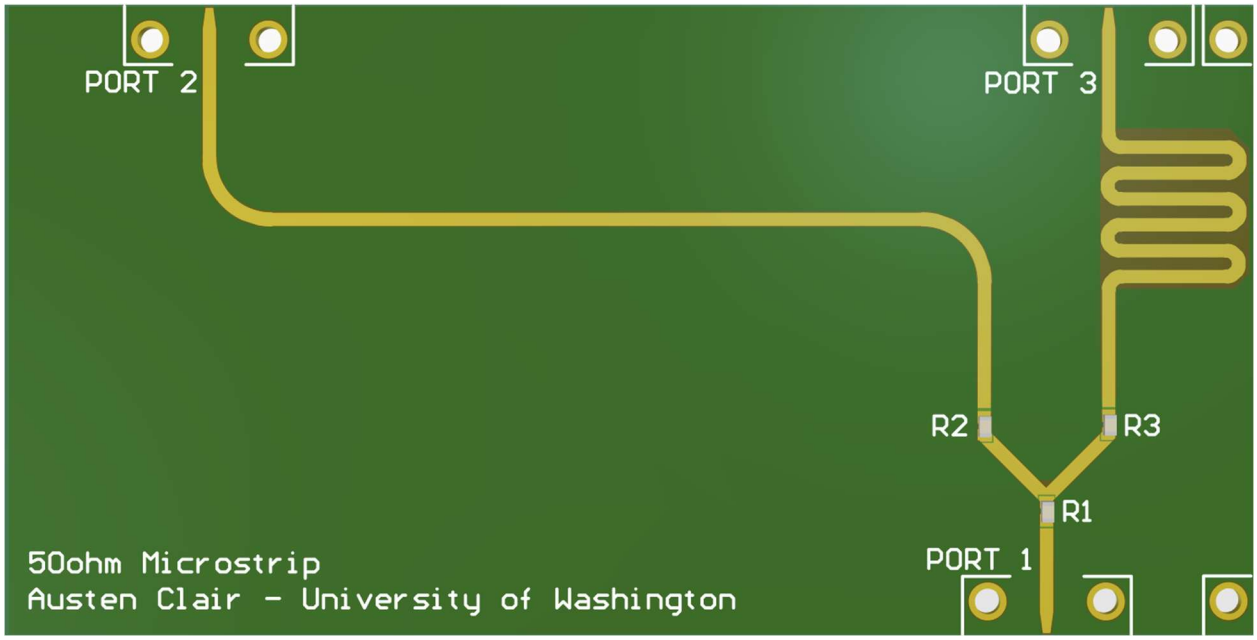

Figure 2.21. Signal traces to ports 2 and 3 (microstrip), designed with identical length but different physical properties

In this model, however, physical aspects such as the curves in the traces and the proximity of the traced paths in the meandering time-delay section are likely to suffer from uneven losses and parasitic effects, which will negatively affect SI.

2.5 Intranet Crosstalk Considerations

Another common problem affecting digital circuits, especially in small form-factor PCBs, is crosstalk; it is defined as "…the transfer of an unwanted signal from one net to an adjacent net, and it occurs between every pair of nets [1]." This is due to coupling between adjacent nets, which is caused by fringe fields; as defined by Dr. Bogatin: "Any time a signal propagates down a transmission line, there are electric field lines between the signal and return paths, and rings of magnetic field lines around the signal-and-return path conductors [1]."

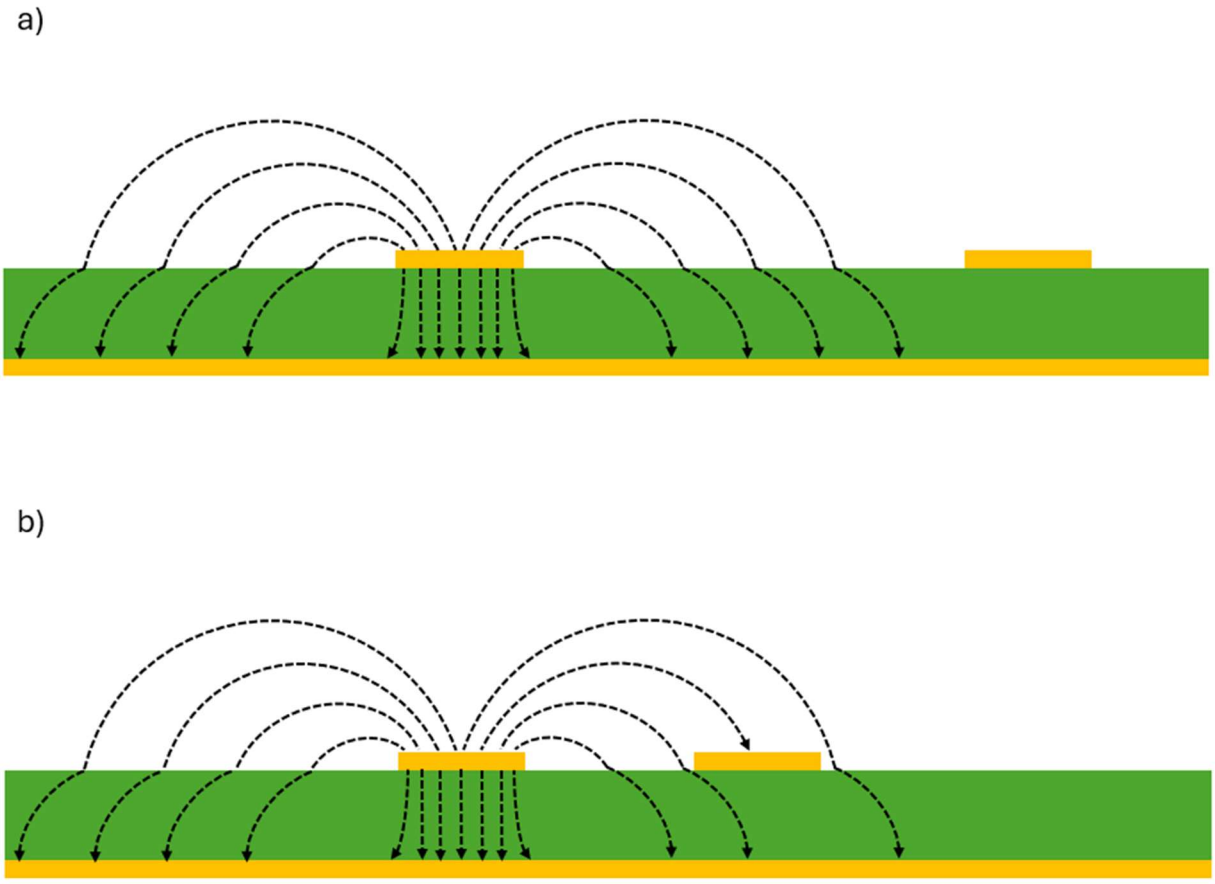

Figure 2.22. Electric fields between a signal path and a return path and how they might interact with a second net when it is far away (a) and when it is close (b)

Figure 2.22 represents the cross-sectional view of a microstrip transmission line and the long paths of electric fields that radiate from the active signal trace. If this same model is made with a GCPW transmission line (Fig. 2.23), it is feasible to consider that the waveguide gaps and top-side ground planes will trap the electric fields and enable a more compact layout with a reduction in crosstalk.

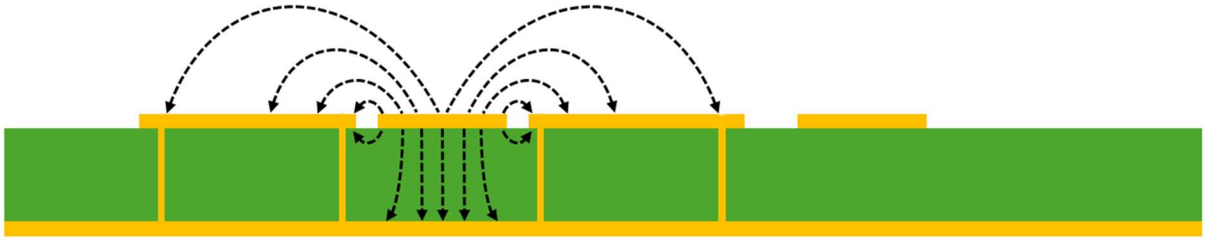

Figure 2.23. Representation of electric fields intercepted by GCPW ground plane

For this experiment, a straight signal trace (ports 4 and 5) was routed as close as possible to the meandering time delay trace. This effectively compares the ability of a GCPW PCB to reduce crosstalk effects with that of a microstrip PCB.

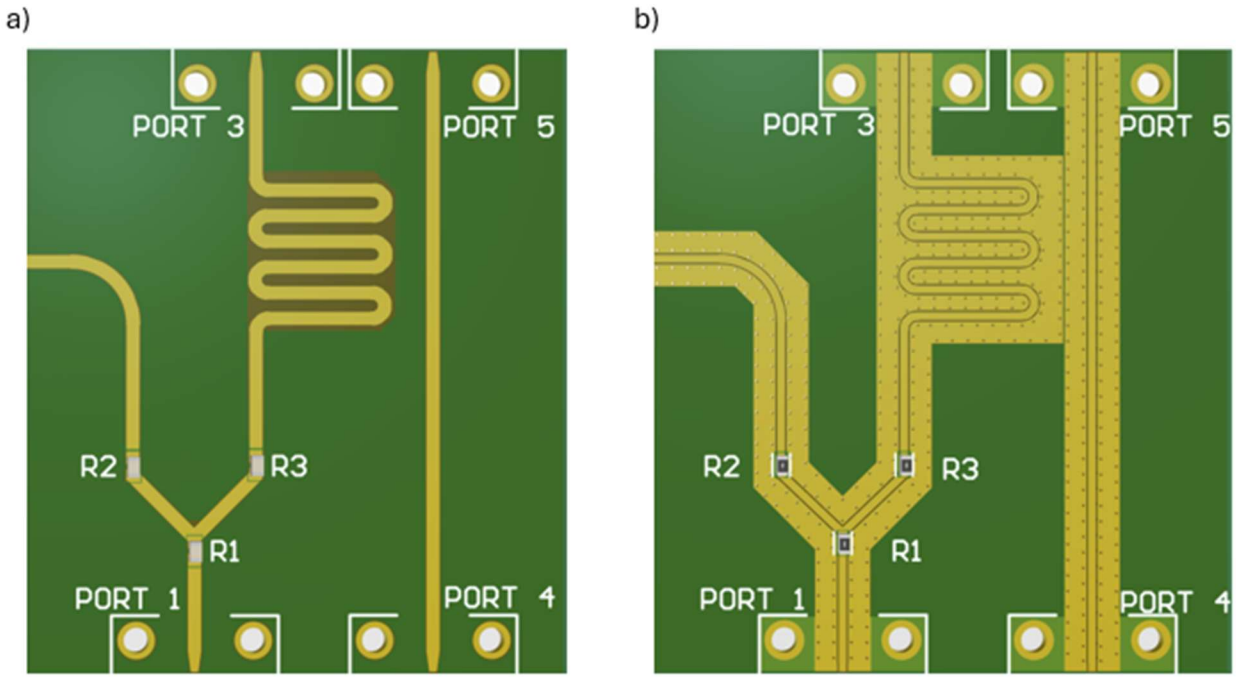

Figure 2.24. Straight signal trace (port 4 to port 5) adjacent to meandering time delay serpentine on microstrip (a) and GCPW (b)

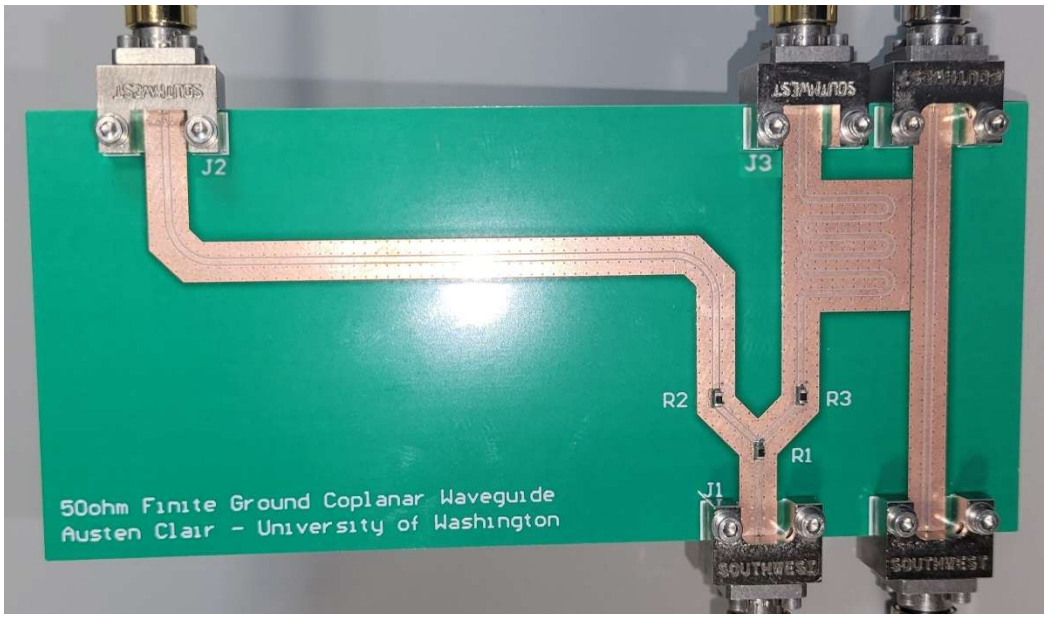

Figure 2.25. Fabricated GCPW PCB

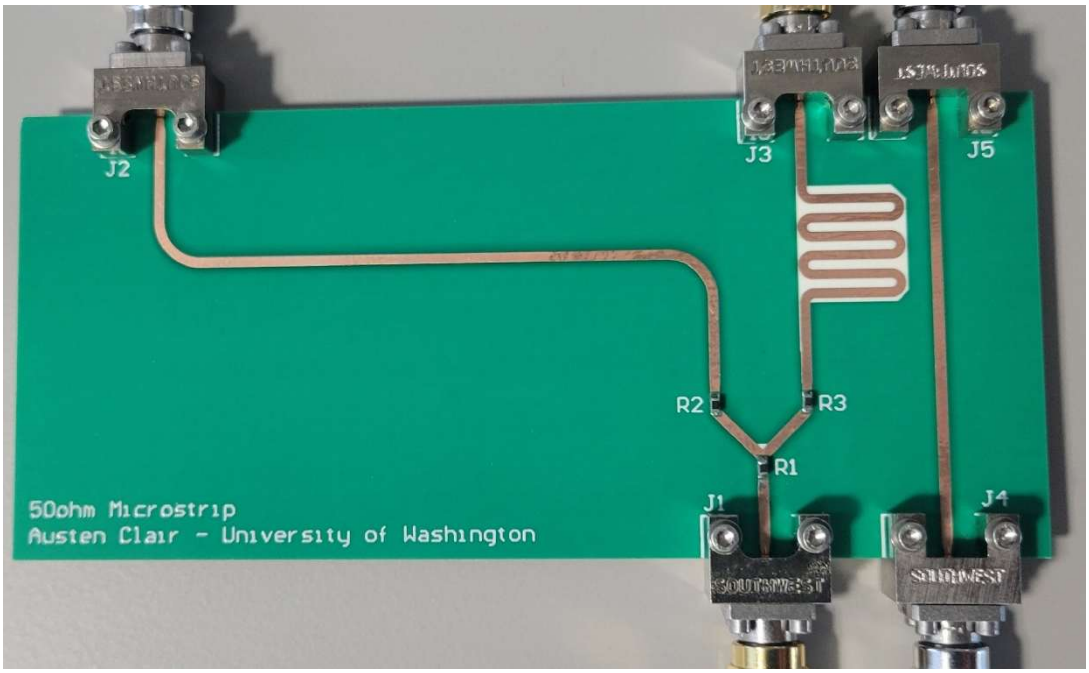

Figure 2.26. Fabricated microstrip PCB

Chapter 3. TIME-AND-FREQUENCY DOMAIN SIMULATIONS FOR SIGNAL INTEGRITY AND CROSSTALK

To prepare a PCB for fabrication after initial design, best practice dictates that comprehensive simulations are performed to maximize design efficacy and efficiency. Afterall, once a PCB has been fabricated, there is very little that can be done to remedy any mistakes or defects, and often a PCB will have to be fixed or revised, then ordered again. This is time consuming, not to mention expensive. For this experiment, the PCBs were simulated in both the frequency and time domains using Sonnet and LTSpice to determine their effectiveness at maintaining signal integrity and reducing intranet crosstalk.

3.1 Frequency Domain Analysis (Sonnet Software)

Sonnet is an electromagnetic simulation tool that is capable of high-accuracy broadband analysis of planar circuits and antennas. By importing .dxf files from the Altium PCB designs, Sonnet builds a model of the PCBs compatible with its analysis environment.

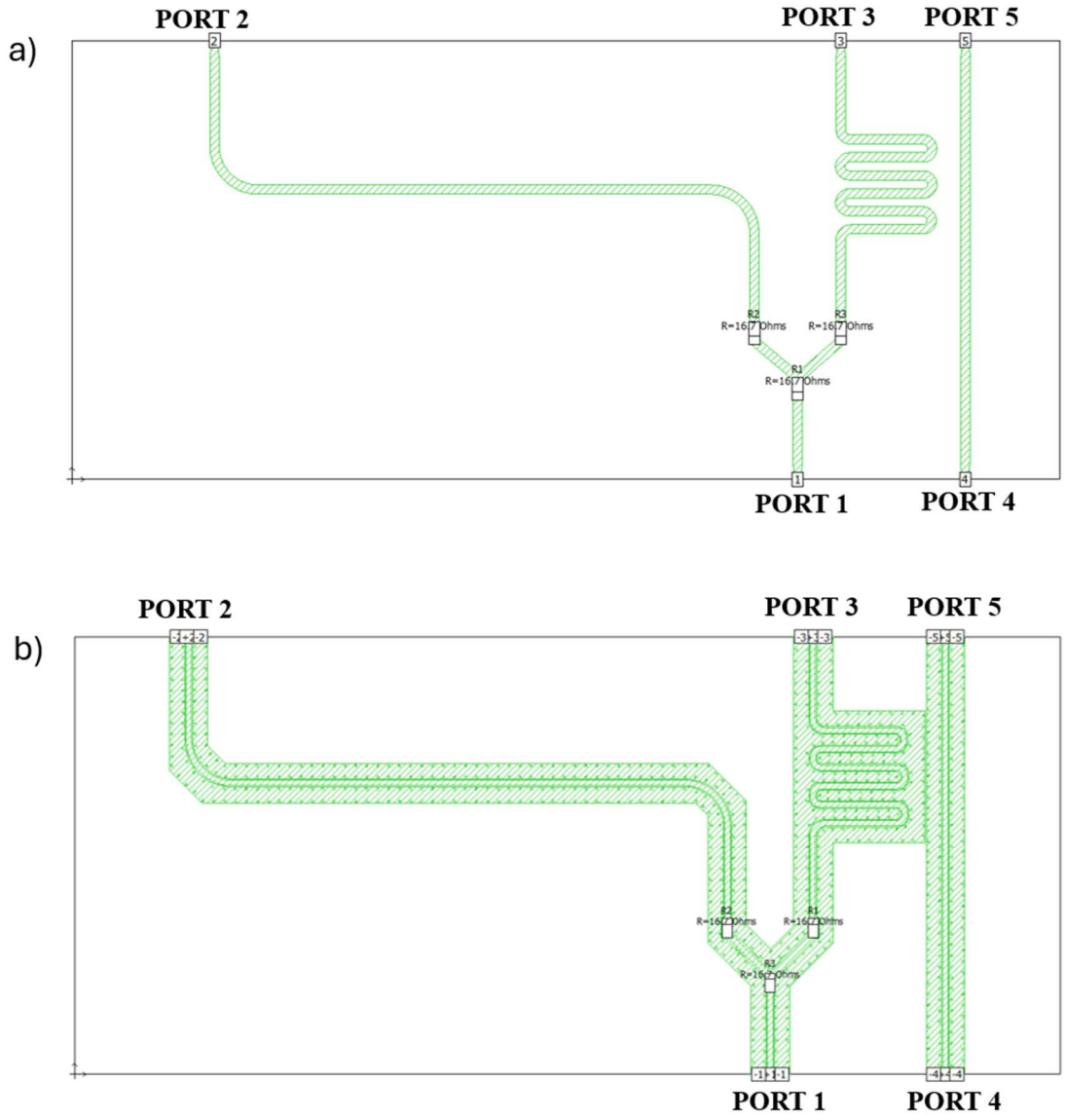

Figure 3.1. Sonnet PCB layout for microstrip (a) and GCPW (b) with labeled port locations

In the case of the circuits in this experiment, measuring S_{21} refers to the response at port 2 due to a signal at port 1, and S_{31} refers to the response at port 3 due to a signal at port 1. This effectively represents the efficiency of the line between the two ports, where less loss is better. S_{11}, however, represents the reflection coefficient of port 1. In this instance it is preferred that the response measured is as low as possible, as this would indicate less power reflected back to port

1. It is also possible to determine intranet crosstalk by measuring S_{51}, which determines the magnitude of the signal at port 1 which is coupled to the straight transmission line and propagated out of port 5. Due to the design of the resistive splitter, it is to be expected that S_{21} and S_{31} will never exceed -6 dB, as this represents the purely resistive loss of the splitter design. In figure 3.1 (b), the copper conductors and ground planes of the GCPW circuit are represented in green. Also present are the rows of shielding vias, as well as the positive and negative aspects of the ports. The design is sub-sectioned into 360,000 individual 5 mil square cells, which are each analyzed over the frequency range of 0 Hz to 10 GHz, incrementing every 100 kHz. Unfortunately, because these circuits were designed to be as compact as possible and the GCPW was designed with 5 mil waveguide gaps as mentioned in Chapter 2, this means there is no margin for error in the simulation.

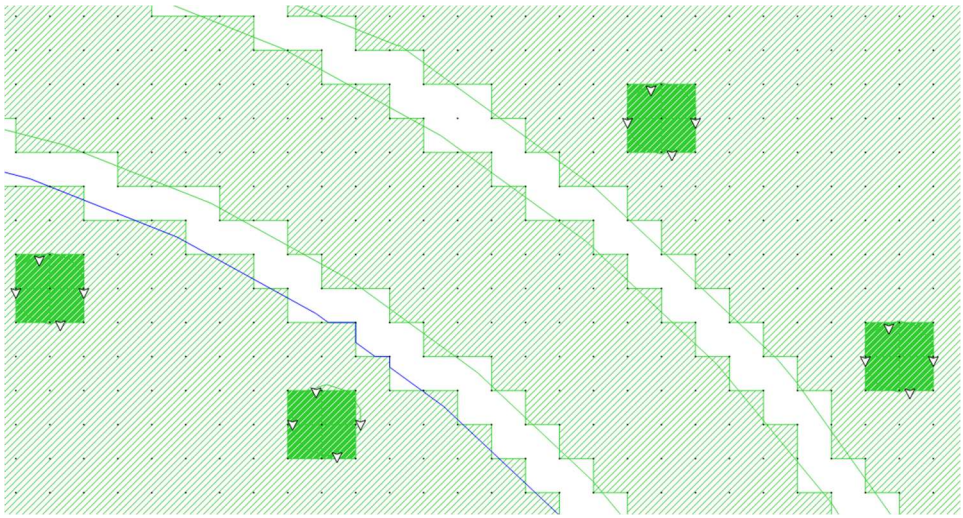

Figure 3.2. A section of curved GCPW transmission line from Sonnet layout

As can be seen in Figure 3.2, the GCPW transmission line is left with a choppy, uneven waveguide gap, which may negatively affect the performance of the simulation. While the GCPW design could theoretically be sub-sectioned into 1 mil squares, Sonnet would require a

CPU with over 300GB of RAM to process the data. Due to the reduced complexity of the microstrip design, as compared to the GCPW, it was possible to sub-section the microstrip circuit into 1 mil square cells. Once simulations are complete, a process that can take up to 10 hours in this case, Sonnet produces any 5-port S-parameter data required.

3.1.1 *Three-Port 1x2 Clock Distribution S-Parameters*

S-parameters, as discussed in Chapter 2, describe the response of a multi-port network to signals at any port in the network. They are derived from a scattering matrix (S-matrix), which is a mathematical means of simplifying and describing the properties of a complex, multi-port network [9].

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{3.1}$$

The S-matrix for a three-port network (3.1) describes the behavior of all possible S-parameter measurements applicable to the 1x2 clock distribution network modeled in this experiment. Considering the resistive splitter in Given that a symmetric resistive splitter is a lossy, matched network, the S-matrix can be simplified as

$$[S] = \begin{bmatrix} 0 & S_{12} = S_{21} & S_{13} = S_{31} \\ S_{21} = S_{12} & 0 & S_{23} = S_{23} \\ S_{31} = S_{13} & S_{32} = S_{23} & 0 \end{bmatrix} \tag{3.2}$$

making it a reciprocal matrix; this is why it is only necessary to measure S_{21}, S_{31}, and S_{23} for losses, as their reciprocal parameters are equal. Because each output port experiences a 6 dB resistive loss, the matrix can be further simplified as:

$$[S] = {}^{1}/_{2}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \tag{3.3}$$

To predict the effectiveness of the three-port clock distribution circuit, S-parameter and phase simulations between ports 1, 2 and 3 are analyzed graphically and compared between PCBs. In an ideal clock distribution circuit, for example, the S_{21} curve would mirror the exact behavior of the S_{31} curve. The signal phase at port 2 would also match the phase at port 3. Therefore, the comparison of these two measurements in the microstrip and GCPW circuits respectively indicates which circuit displays a superior ability to maintain signal integrity.

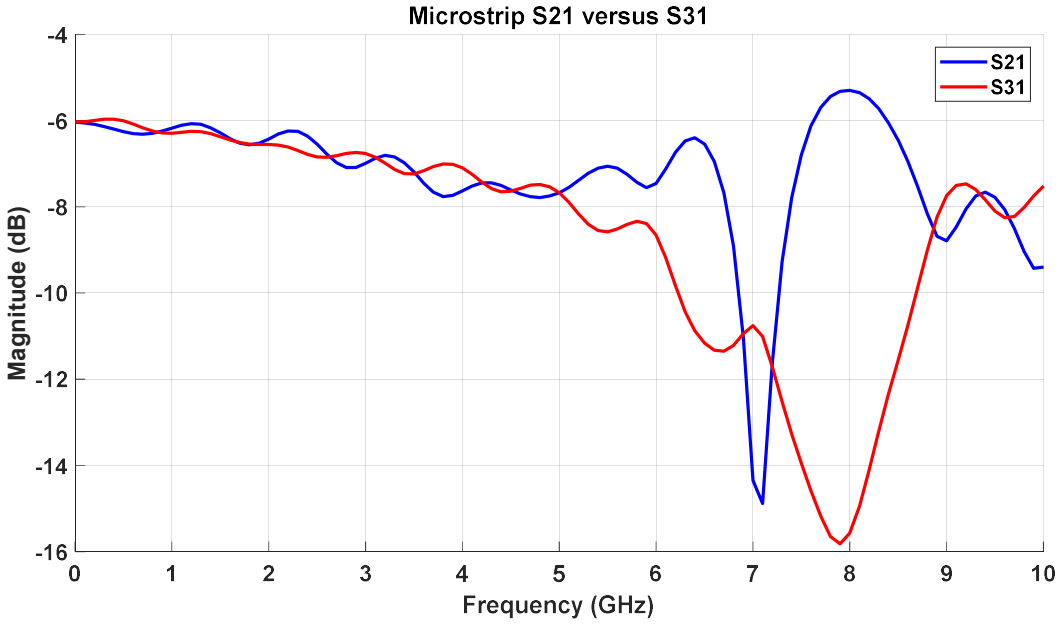

Figure 3.3. Microstrip simulated S_{21} versus S_{31}

Figure 3.4 shows that the two output ports in the microstrip maintain an acceptable relationship until 5 GHz, where S_{21} and S_{31} begin to diverge. By 7-to-8 GHz, the two ports diverge completely, with S_{21} showing a sharp resonance and S_{31} resonating over a broad

bandwidth. This does not predict promising behavior in regard to maintaining signal integrity over a wide range of frequencies.

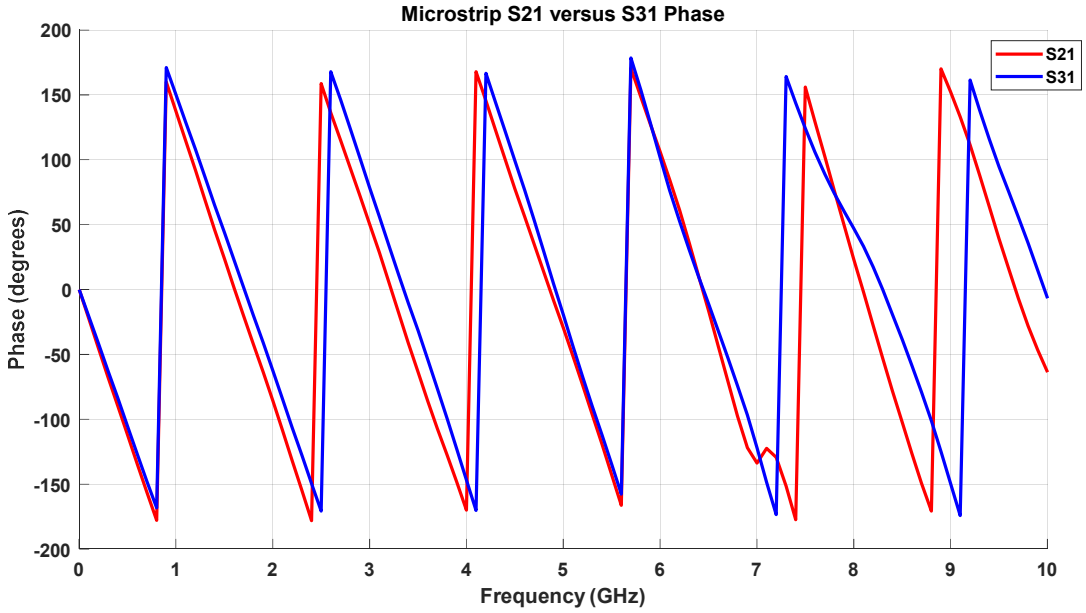

Figure 3.4. Microstrip simulated output phase at port 2 and port 3

The phase relationship between port 2 and port 3 of the microstrip clock distribution circuit indicates that the input signal at port 1 becomes desynchronized as it passes through the resistive splitter and propagates down two geometrically dissimilar transmission lines, even though they are of identical lengths. This is indicative of a significant level of clock skew at the output ports if observed in the time domain.

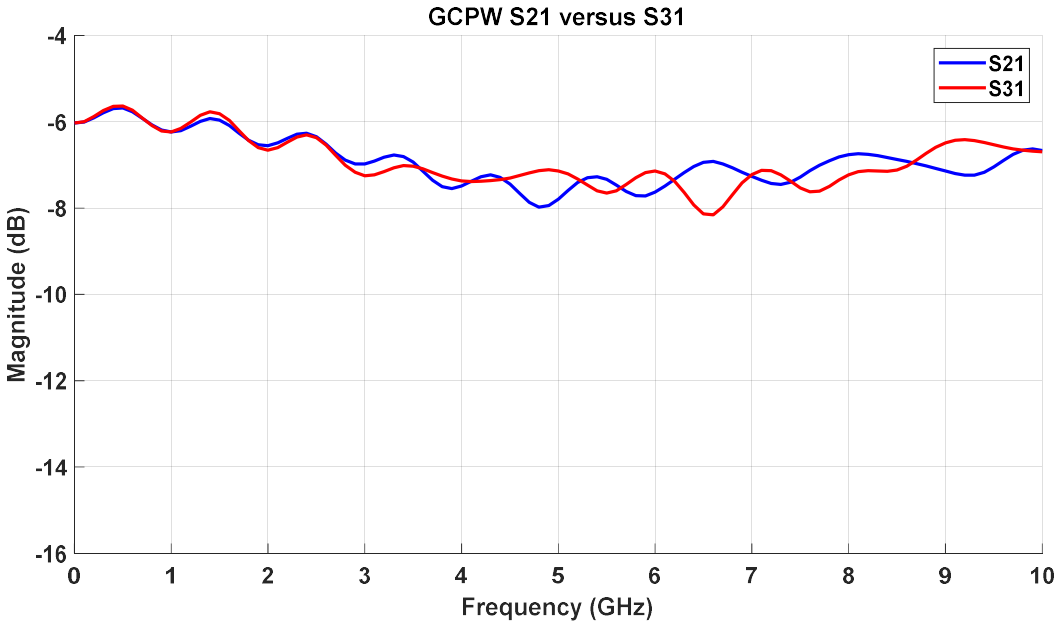

Figure 3.5. GCPW S_{21} versus S_{31}

In Figure 3.5, the GCPW maintains exceptional synchronicity between S_{21} and S_{31} until nearly 3 GHz, where the signals begin to diverge. Unlike the microstrip line, however, S_{21} and S_{31} on the GCPW still retain the same overall trend across the spectrum, never diverging more than 6 dB.

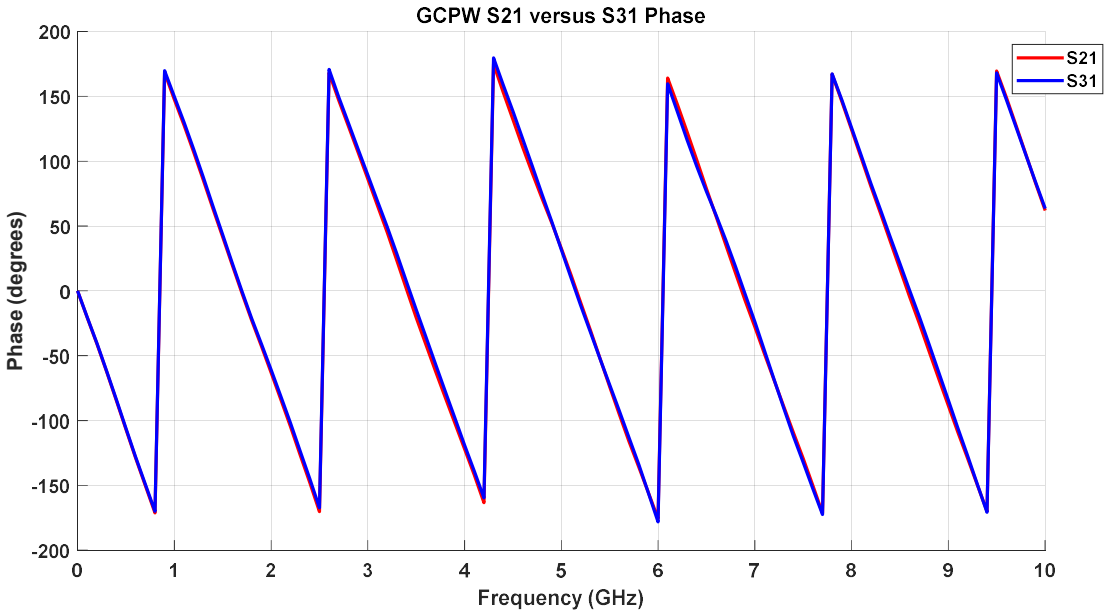

Figure 3.6. GCPW output phase at port 2 (red) and port 3 (blue)

The GCPW phase relationship in Figure 3.7 presents a nearly identical signal pattern between ports 2 and 3, suggesting that the GCPW will maintain signal integrity throughout the experimental bandwidth. One could expect, therefore, to observe matching clock signals emerging from ports 2 and 3, with minimal skew.

As in Chapter 2 when discussing the straight transmission line parameters, it is important here to discuss total reflection in the clock divider circuit, represented as S_{11}.

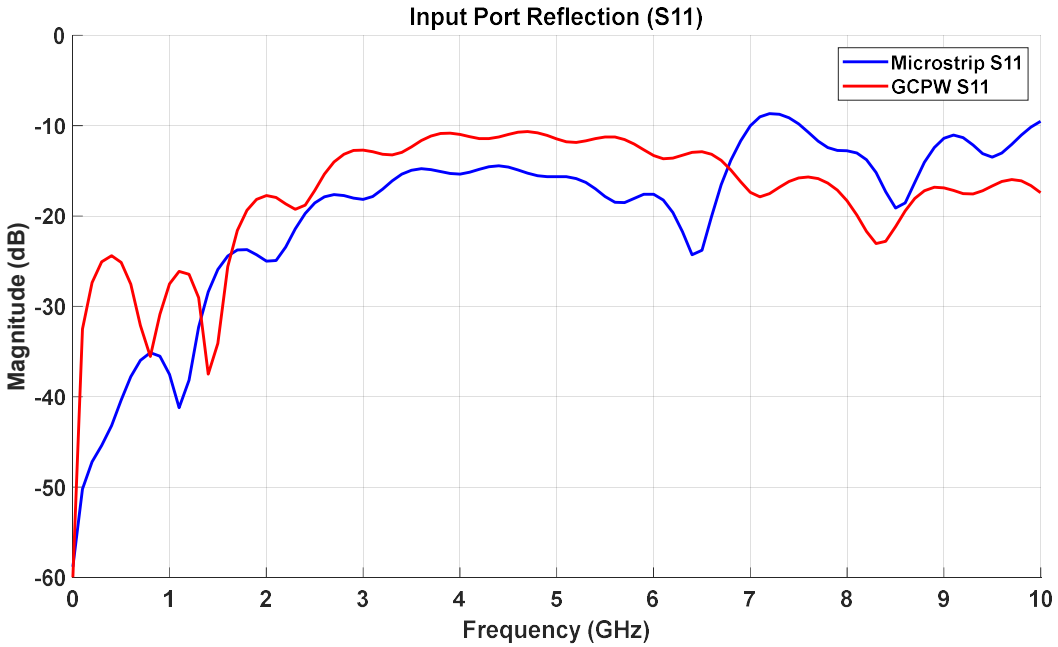

Figure 3.7. Clock distribution simulated total reflection (S_{11})

Analyzing Figure 3.7, both circuits suffer from minimal reflection (< -20 dB) initially, with an increase beginning at 2 GHz. The microstrip suffers less reflection through most of the spectrum, until approximately 6.5 GHz, where it experiences a sharp increase. The GCPW, on the other hand, reduces reflection before leveling out as the frequency nears 10 GHz. This is an indicator that the GCPW could operate effectively to an even higher frequency.

The final simulated measurement to consider when evaluating the clock distribution network is S_{23}. As outlined by Dr. Pozar in *Microwave Engineering* [10] and equations 3.1 through 3.3, theoretically $S_{21} = S_{31} = S_{23}$, so it would be expected that these three S-parameter curves would also follow the same approximate trajectory, varying only with geometric and material effects. The prototype PCBs in this case, however, form more of a modified splitter, where R2 and R3 are separated from R1 by a short length of transmission line, as can be seen in Figure 2.17. Because of this, the resistive splitter in this experiment varies from the traditional

resistive splitter, so it will be beneficial to plot S_{21}, S_{31}, and S_{23} together to observe how this modification affects the results.

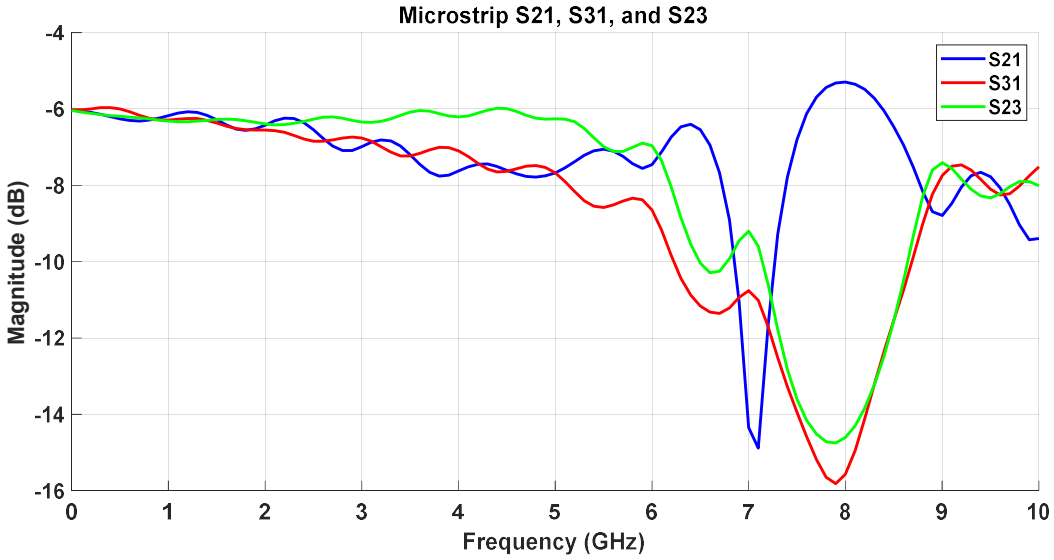

Figure 3.8. Microstrip S_{21}, S_{31}, and S_{23} simulation

Observing Figure 3.8, the S_{23} curve begins at the expected -6 dB produced by the splitter but maintains approximately 1 dB less loss than the other two curves until encountering a wide resonance between 6 and 9 GHz. The S_{23} curve mirrors S_{31} closely while experiencing slightly less loss until converging at the resonance dip. Because S_{31} represents the transmission line with the time delay serpentine structure, it is reasonable to conclude that the large dip that occurs on both curves is due to reflections caused by the serpentine.

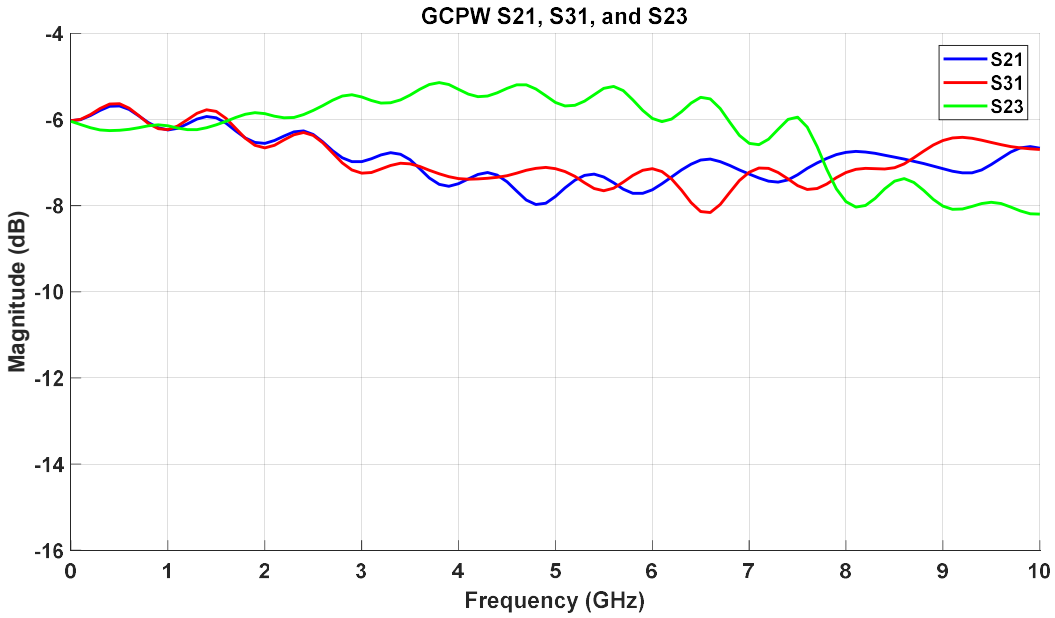

Figure 3.9. GCPW S_{21}, S_{31}, and S_{23} simulation

Figure 3.9, representing the GCPW, shows no indication of the wide resonance present in the microstrip simulation, indicative of an ability to minimize reflection on the time delay serpentine structure.

As with the straight transmission line analysis in chapter 2, it is worth examining the total power leaving all ports when power is injected into port 1. Expected loss for an ideal resistive splitter is -6 dB, with all other losses due to resistive and conductive effects. Equation 3.4 is used to calculate a summation of signal out of all three ports.

$$|S_{21}|^2 + |S_{31}|^2 + |S_{11}|^2 \tag{3.4}$$

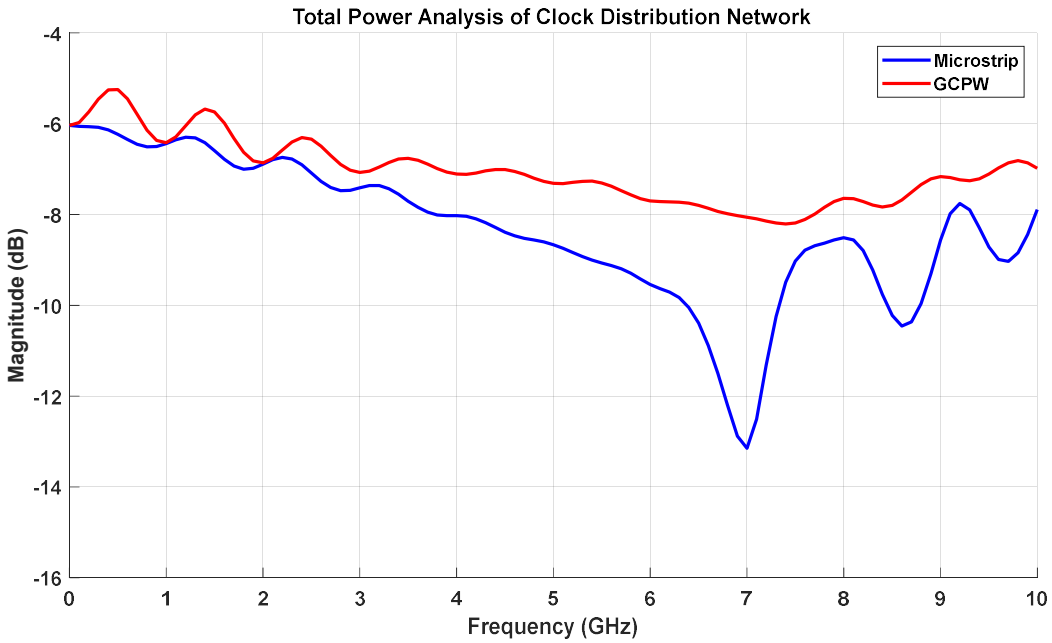

Figure 3.10. Microstrip versus GCPW clock distribution total power analysis

As with previous plots, the microstrip encounters a broad resonance between 6 and 9 GHz, while losses suffered by the GCPW are significantly lower and more linear.

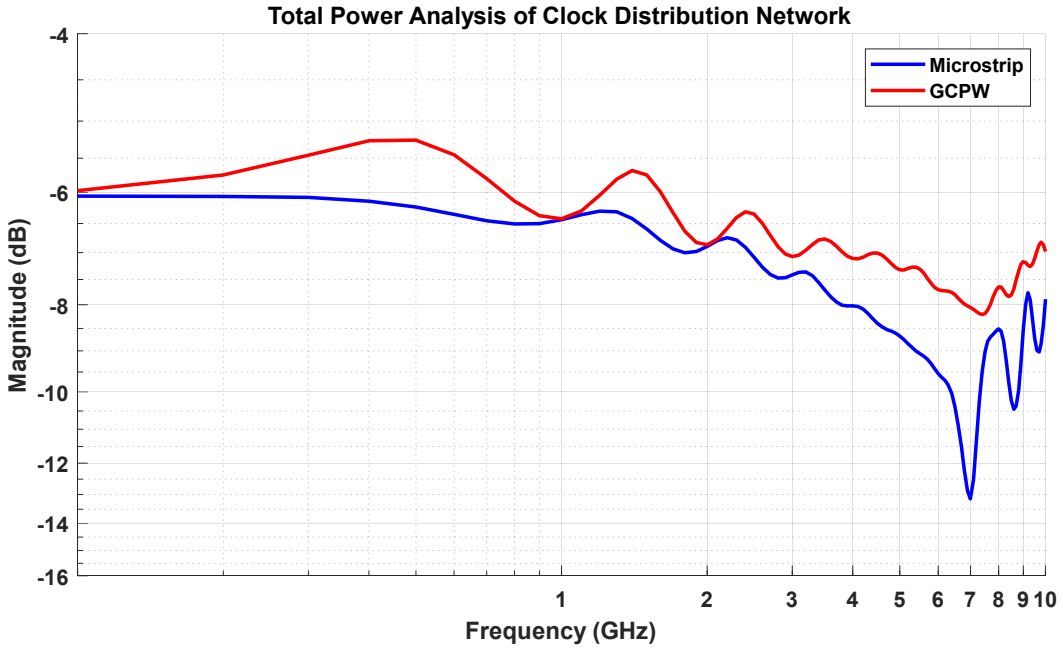

Figure 3.11. Microstrip versus GCPW clock distribution logarithmic power analysis

When examining this plot logarithmically, the lack of an asymptotic decrease at higher frequencies indicates that the losses suffered by the 3-port network are parasitic and resistive in nature, but not conductive.

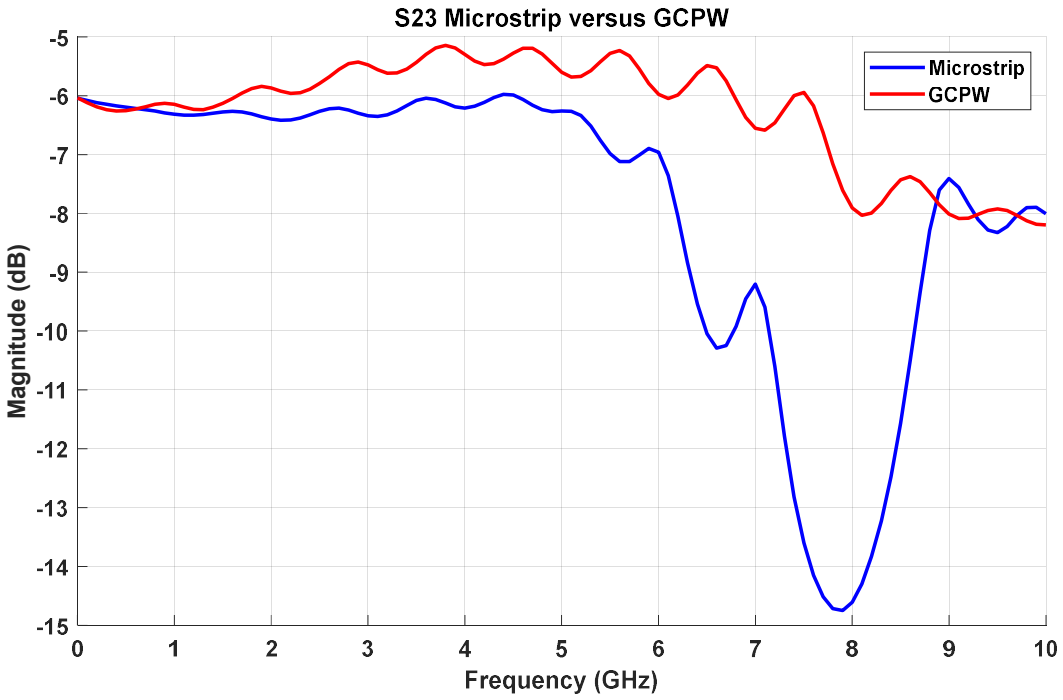

Figure 3.12. Simulated results of S_{23} on microstrip and GCPW clock distribution network

Figure 3.12 provides a comparison of output port isolation S_{23} on the GCPW and microstrip circuits. While the GCPW PCB outperforms the microstrip by 0.5 dB in terms of less net loss, the microstrip remains closer to the expected -6 dB magnitude until the sharp dip that begins at 5 GHz. This indicates that the three ports of the microstrip resistive splitter may be more equally matched at lower frequencies than the GCPW but suffer greatly due to the reflections caused by the time delay serpentine.

3.1.2 *Two-Port Intranet Crosstalk S-Parameters*

Crosstalk between signal traces on PCBs refers to a situation where the source of the electromagnetic emission and the receptor of this emission are within the same system [2]. In the case of the two prototype PCBs in this experiment, the straight transmission line measured in

Chapter 2 was intentionally placed close to the serpentine time delay line terminating at port 3. This is to collect any near-field radiated emissions generated by the serpentine, which has been illustrated in Figures 2.21 and 2.22, to determine which PCB is more effective at mitigating crosstalk. Simulating S_{51}, which represents the magnitude of the signal at port 1 which is radiated to the straight transmission line and propagated out of port 5, will provide a clear representation of which PCB is more effective at mitigating crosstalk. It is important to note that, as with the 1x2 clock distribution network, crosstalk S-parameters are reciprocal, meaning $S_{ij} = S_{ji}$.

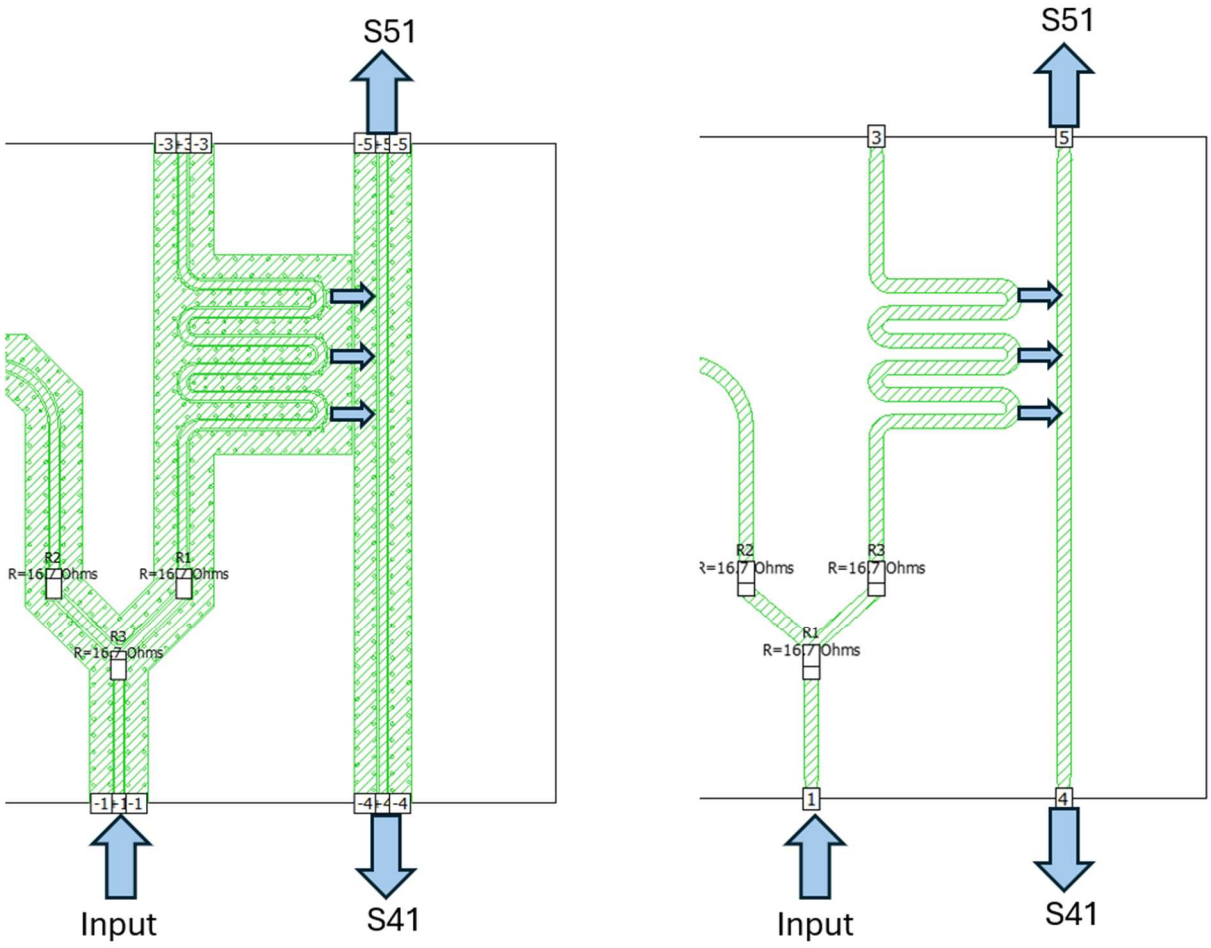

Figure 3.13. Crosstalk simulation signal diagram for GCPW and microstrip PCBs

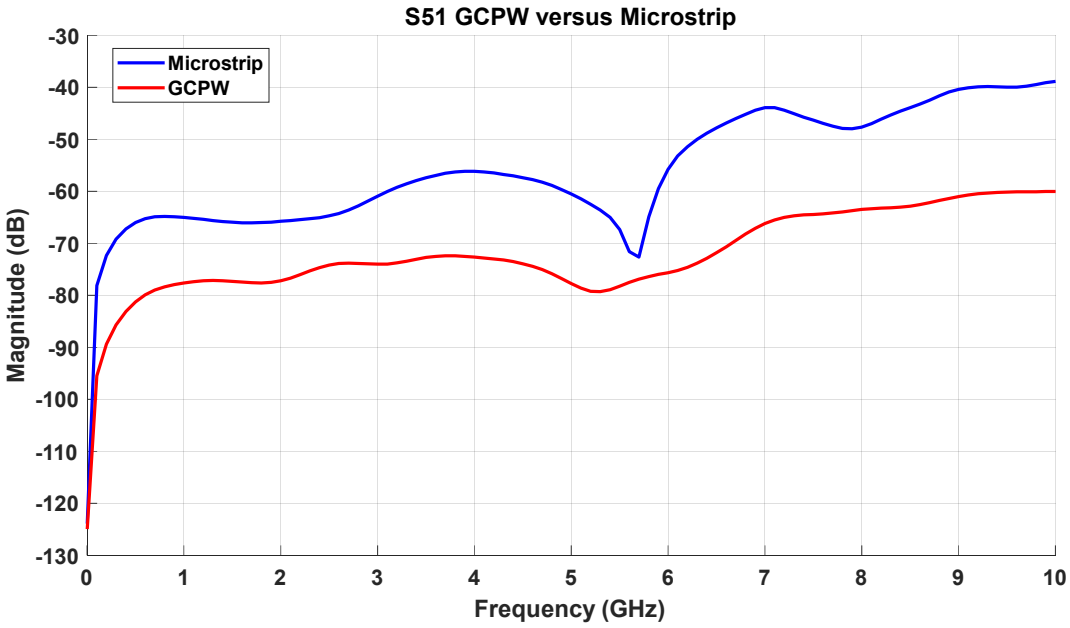

Figure 3.14. Far-end cross talk (S_{51}) simulation for GCPW and microstrip

Far-end crosstalk (FEXT) represents the crosstalk present at the output port of the victim net. In Figure 3.8, it can be concluded that the GCPW generates between 10 dB and 20 dB less FEXT than the microstrip. While both curves represent low magnitudes, the disparity is significant in determining which line is superior in mitigating intranet EMI. This is because, while the GCPW utilizes waveguides to redirect and trap electric fields, the microstrip freely radiates until such time as the electric fields refract through the dielectric and intercept the sole ground plane in the structure, resulting in a broad field pattern around the trace.

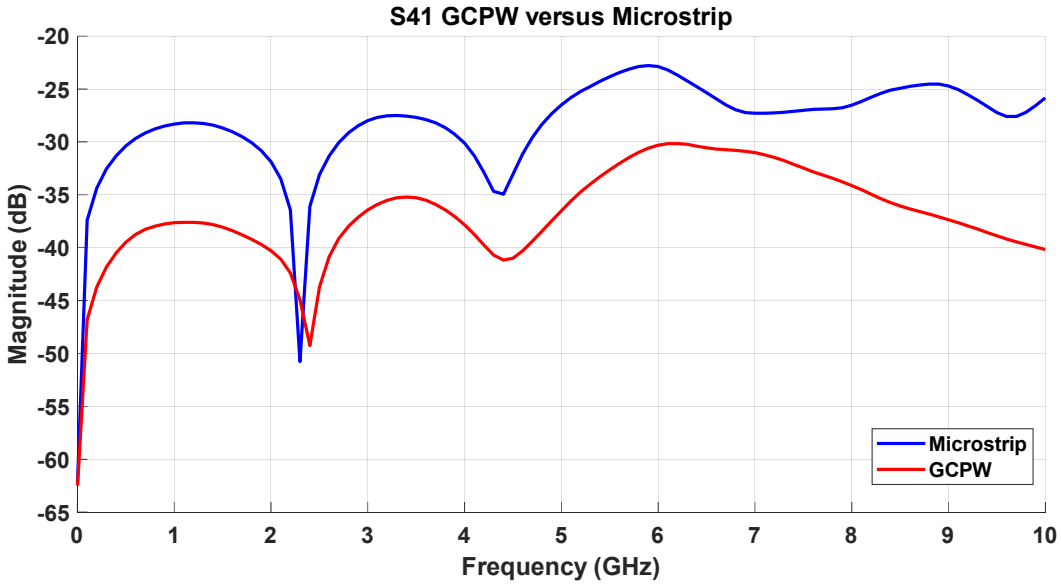

Figure 3.15. Near-end crosstalk (S_{41}) simulation for GCPW and microstrip

The S_{41} simulation in Figure 3.14 represents near-end crosstalk (NEXT) measured at the straight transmission line input port. NEXT, because of its proximity to the signal input of the aggressor net, is higher in magnitude, and indicates that the GCPW outperforms the microstrip structure in mitigating intranet crosstalk at both ends of the transmission line. In this form, crosstalk is more pronounced in both PCBs, with the microstrip curve reaching as high as -22 dB at 6 GHz. Still, the GCPW outperforms the microstrip across nearly all frequencies, except for a sharp drop in microstrip NEXT at 2.3 GHz.

3.2 Time Domain Analysis (LTSpice)

At frequencies involved in this experiment, time domain simulations must include transmission line analysis. A circuit that starts as a simple schematic with only six components (Fig. 2.10), quickly gains complexity as transmission line theory comes into play. The generalized lumped-element model of the lossy transmission line considers material and

geometric properties of the conductor and dielectric substrate and provides a per-unit-length approximation of signal behaviors. This is necessary when dealing with high frequencies as transmission lines may be a considerable fraction of a wavelength, or many wavelengths in size, unlike circuit analysis, which assumes conductor lengths are much smaller than electrical wavelengths [10].

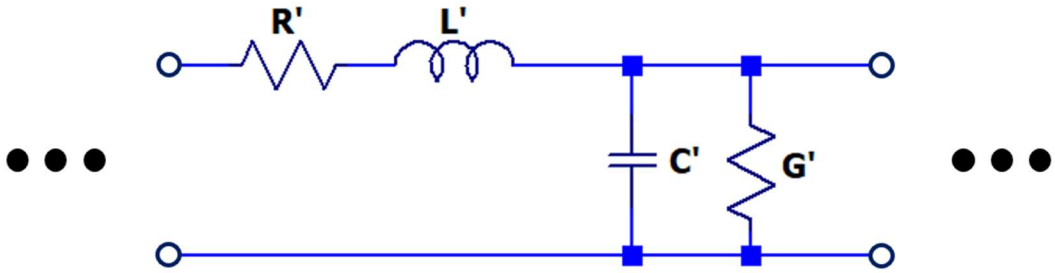

Figure 3.16. Lumped-element transmission line circuit model

A distributed model in Figure 3.16 includes values dependent on the per-unit length properties of the transmission line. R' and L', the per-unit length series resistance and per-unit length series inductance, measured in Ohms-per-meter (Ω/m) and Henrys-per-meter (H/m), are dependent upon the physical and electrical characteristics of the conductor. C' and G', the per-unit length shunt capacitance and per-unit length shunt conductance, measured in Farads-per-meter (F/m) and Siemens-per-meter (S/m), are dependent upon the physical and electrical characteristics of the dielectric. For the sake of the simulated model, shunt conductance is modeled as the inverse in Ω-m, enabling the use of a resistor. This model will be used automatically via software for all time domain simulations.

3.2.1 *Low-Speed versus High-Speed Clock Signals (10 MHz to 1 GHz)*

The LTSpice model of the resistive splitter circuit for signal integrity utilizes the lossy transmission line model with spice directives modified using the per-unit length characteristics (L', R', and C') calculated for the microstrip and GCPW transmission lines. G' is not present as it is not available in the lossy transmission line model in LTSpice and can acceptably be omitted from this model due to the results from Figure 3.11 and the extremely low shunt conductance of the RO4350B laminate used in the prototype PCBs.

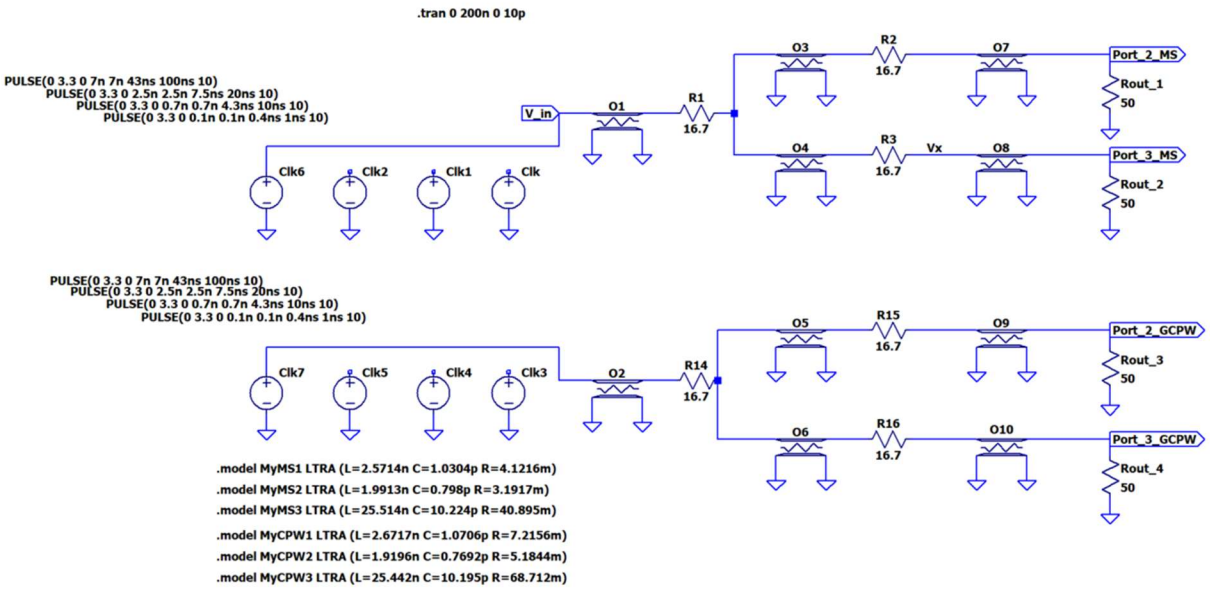

Figure 3.17. LTSpice resistive splitter model for microstrip (top) and GCPW (bottom)

In Figure 3.16, both resistive splitter designs are modeled adjacently with the clock signal feeding both simultaneously. Inductance and capacitance only vary slightly between the GCPW and microstrip transmission lines, with the main difference being the series resistance, which is slightly higher than the microstrip.

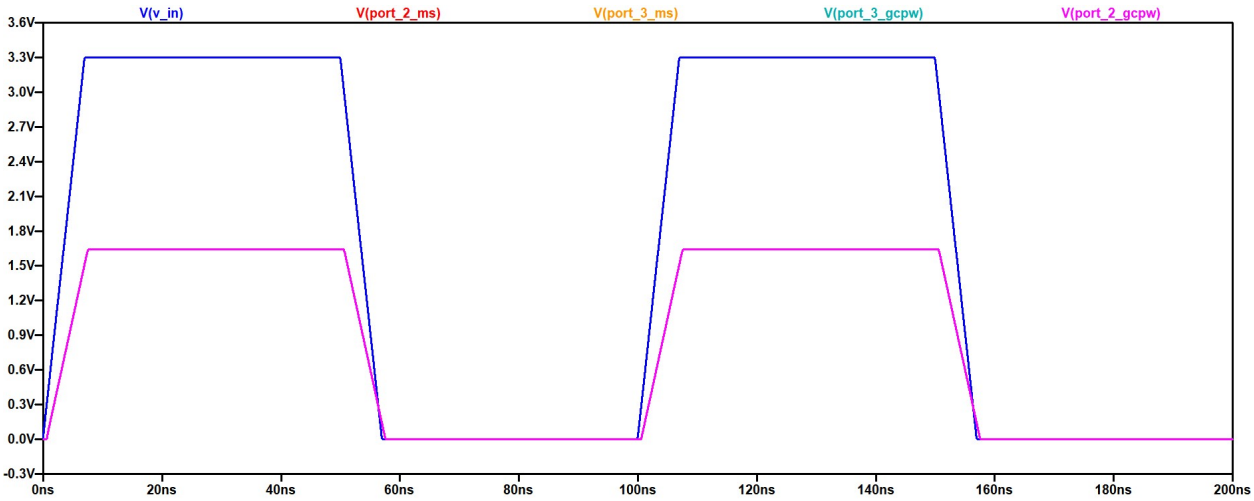

Figure 3.18. LTspice 10MHz clock signal, T_{rise} = 7ns

At 10MHz (Fig. 3.18), there is no discernible difference between any output port on the GCPW or microstrip. The expected 6 dB net loss is present, and there is a slight delay due to the time the signals take to propagate through the circuits.

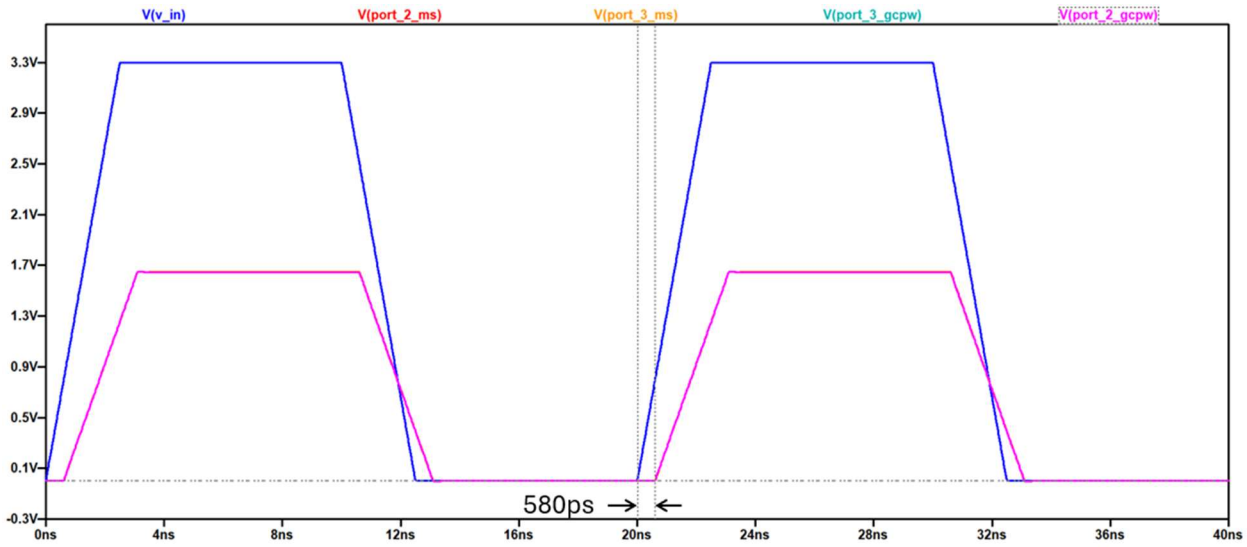

Figure 3.19. LTspice 50MHz clock signal, T_{rise} = 2.5ns

When observing the 50MHz signal, clearly visible is the expected 580ps (GCPW) to 600ps (microstrip) delay, which is the time it takes for a signal to propagate through the clock distribution network to either port 2 or port 3 when not taking parasitic effects into account.

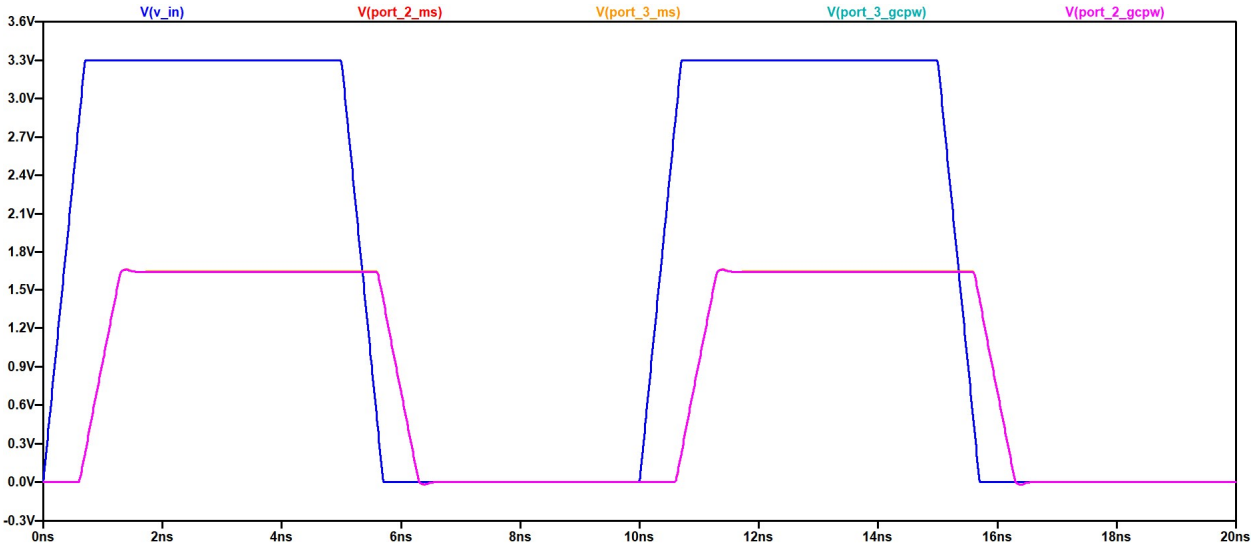

Figure 3.20. LTspice 100MHz clock signal, T_{rise} = 0.7ns

At 100MHz (Fig. 3.20), the delay resolves to 600ps as the clock pulse propagates through the transmission lines. All four output values are identical, and there is evidence of ringing at the rise and fall edges of the output waveforms.

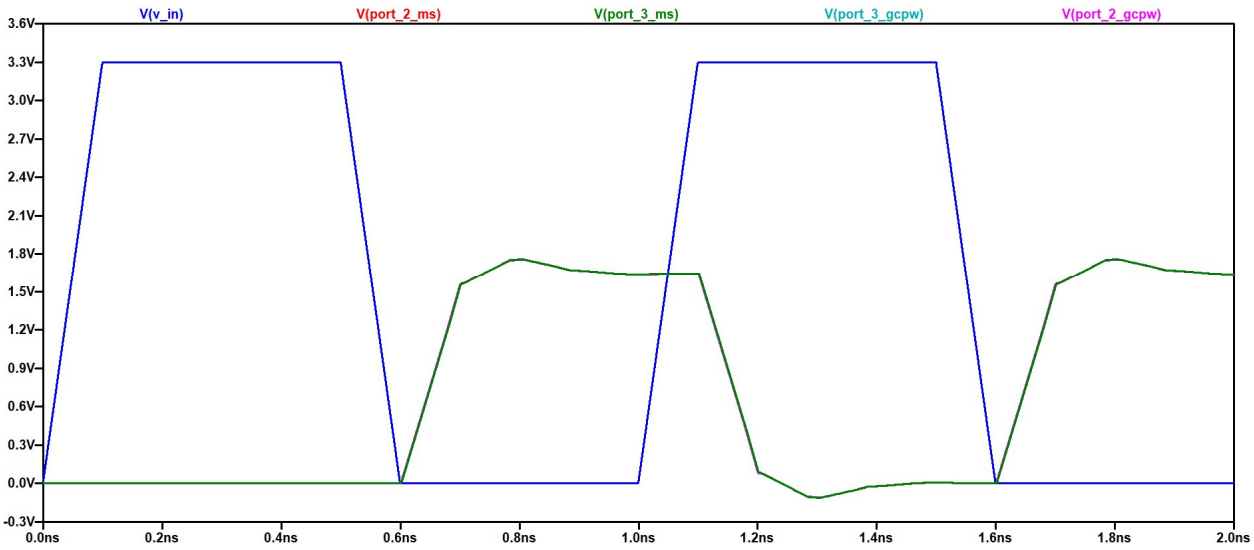

Figure 3.21. 1 GHz clock signal, T_{rise} = 0.1ns. GCPW attenuation enlarged.

At 1 GHz the LTSpice simulation output signals, while still largely synchronized, show a slight attenuation on the part of the GCPW due to it being more lossy than the microstrip. There is also a very minor delay on the microstrip pulse when compared to the GCPW.

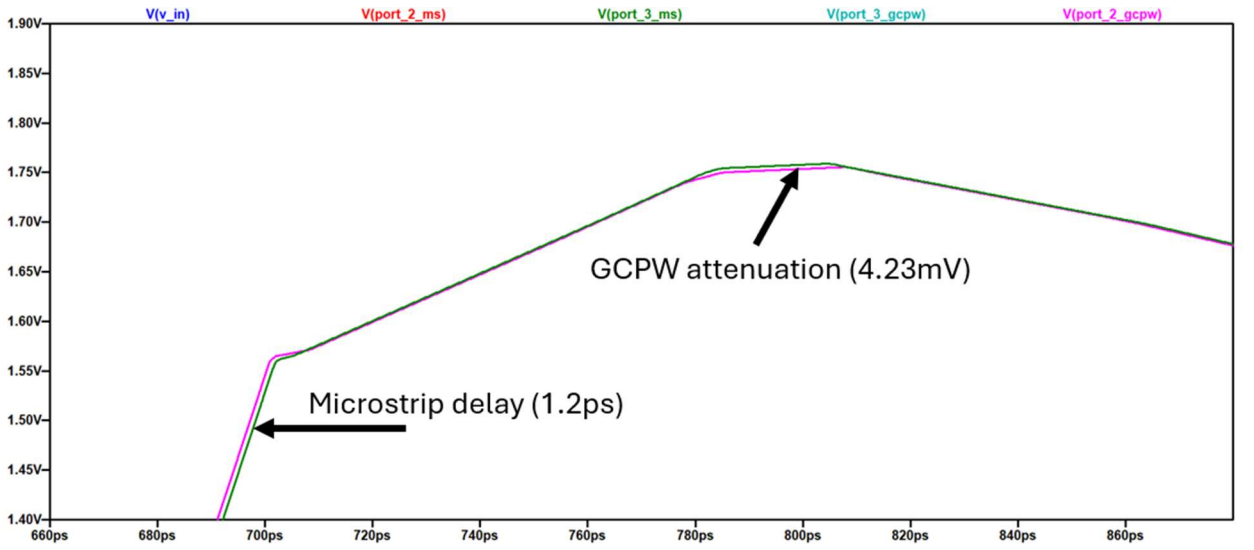

Figure 3.22. Enlarged delay and attenuation from LTSplice 1 GHz plot

Because the LTSpice model does not account for any of the curvature found on the prototype PCBs, the only parameter that differs between the two simulated circuits is the greater resistive loss of the GCPW. This accounts for the symmetry between the two plots at every frequency, with the only noticeable variation occurring at 1 GHz. Because of this, a tool more suited to simulating these differences is the AWR Design Environment's Microwave Office (MWO). MWO provides the ability to model all transmission line sections and curves, enabling the simulation to predict the behavior of the signal as it propagates along the bends and meandering tracks of the clock distribution circuit.

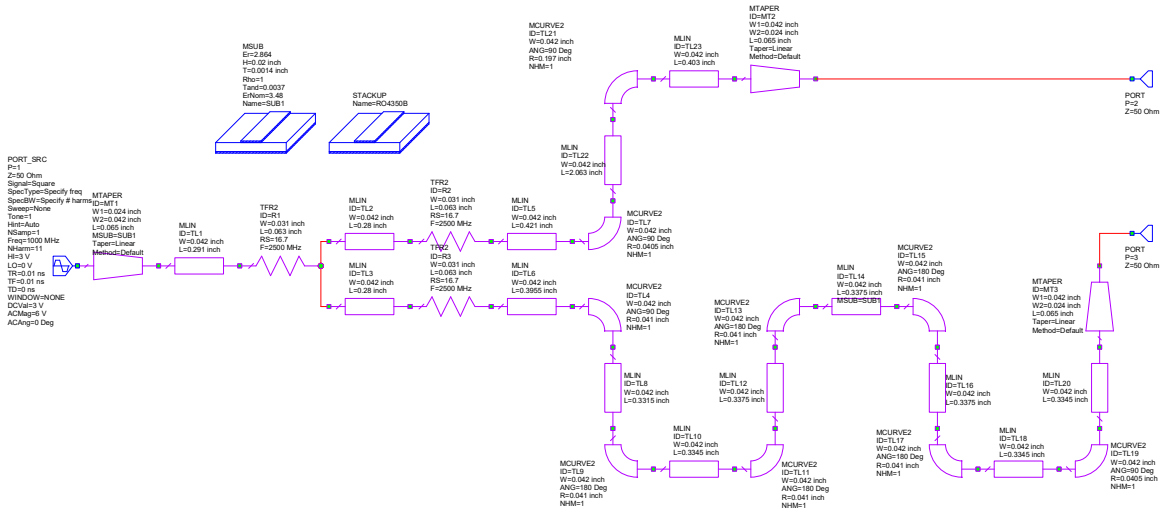

Figure 3.23. MWO microstrip circuit schematic

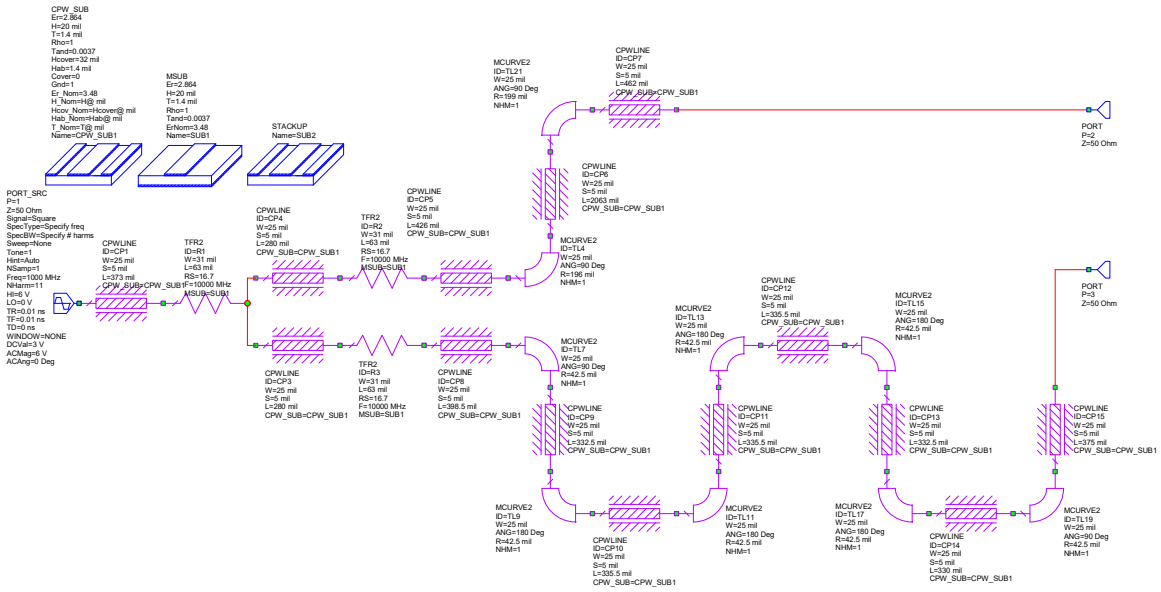

Figure 3.24. MWO GCPW circuit schematic

MWO can model several different types of transmission line, including the coplanar waveguide. Unfortunately, while it is equipped with a model of a CPW right-angle turn, it cannot simulate a curved GCPW. In this case, the curved portions of the line remain as microstrip, while the straight-line sections are CPW. This will not provide a completely accurate representation of the GCPW circuit, but it should provide a passable comparison of the benefits and drawbacks of the two designs.

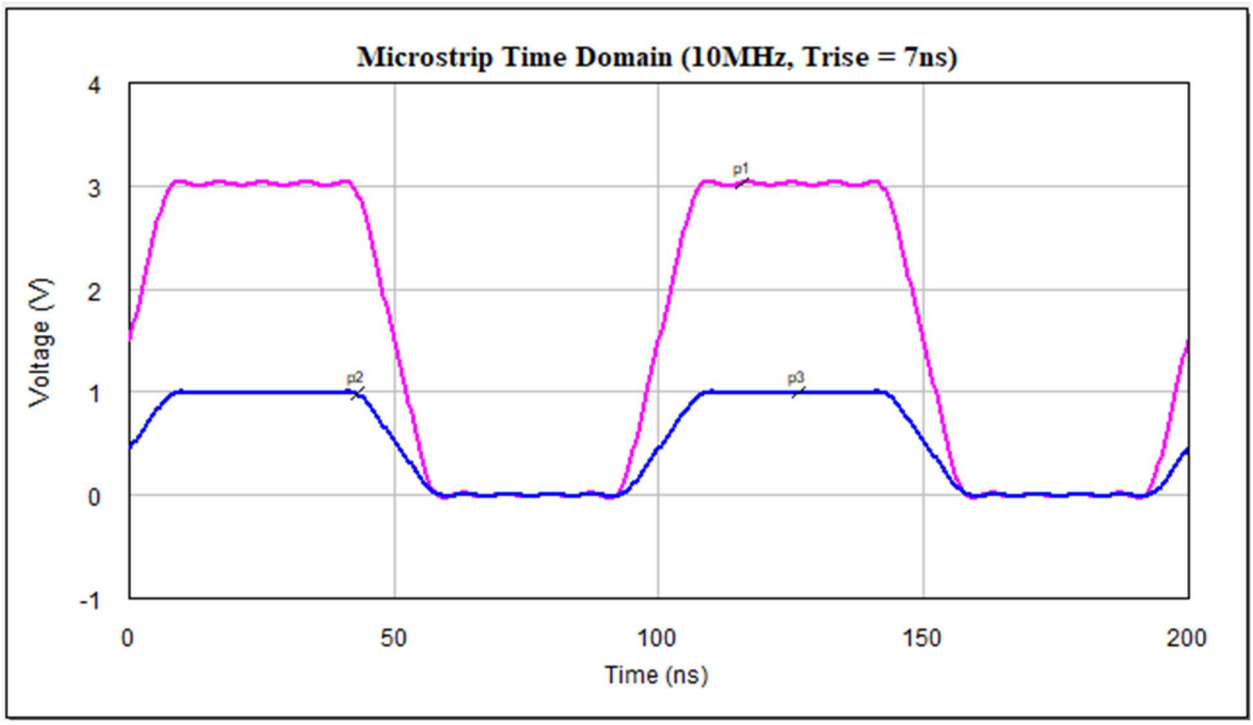

Figure 3.25. MWO 10MHz microstrip clock signal, T_{rise} = 7ns

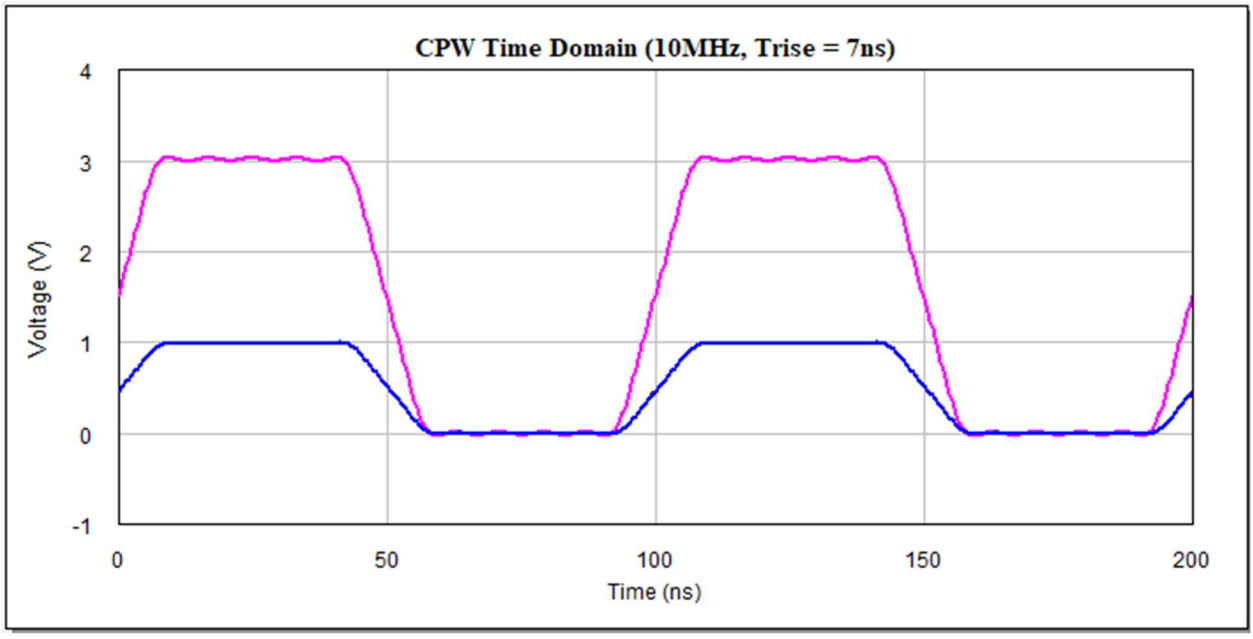

Figure 3.26. MWO 10MHz CPW clock signal, T_{rise} = 7ns

At 10MHz, the microstrip and GCPW react identically, with very little delay and no disparity between output signals.

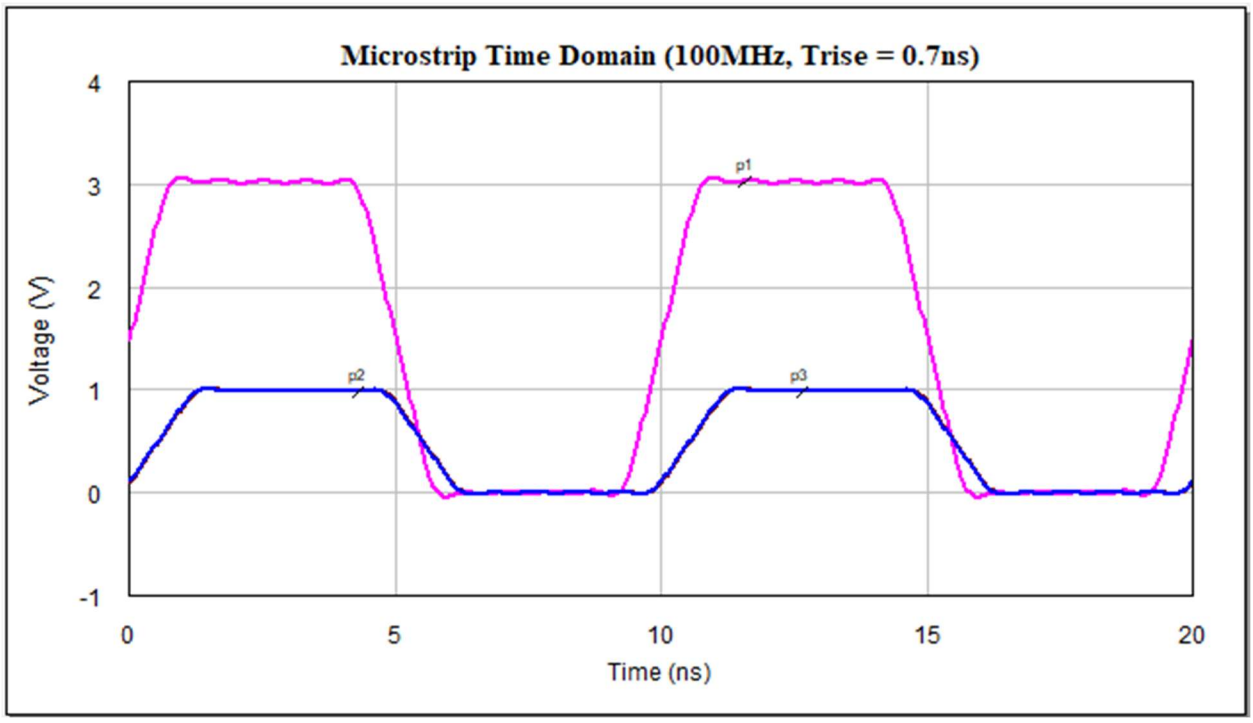

Figure 3.27. MWO 100MHz microstrip clock signal, T_{rise} = 0.7ns

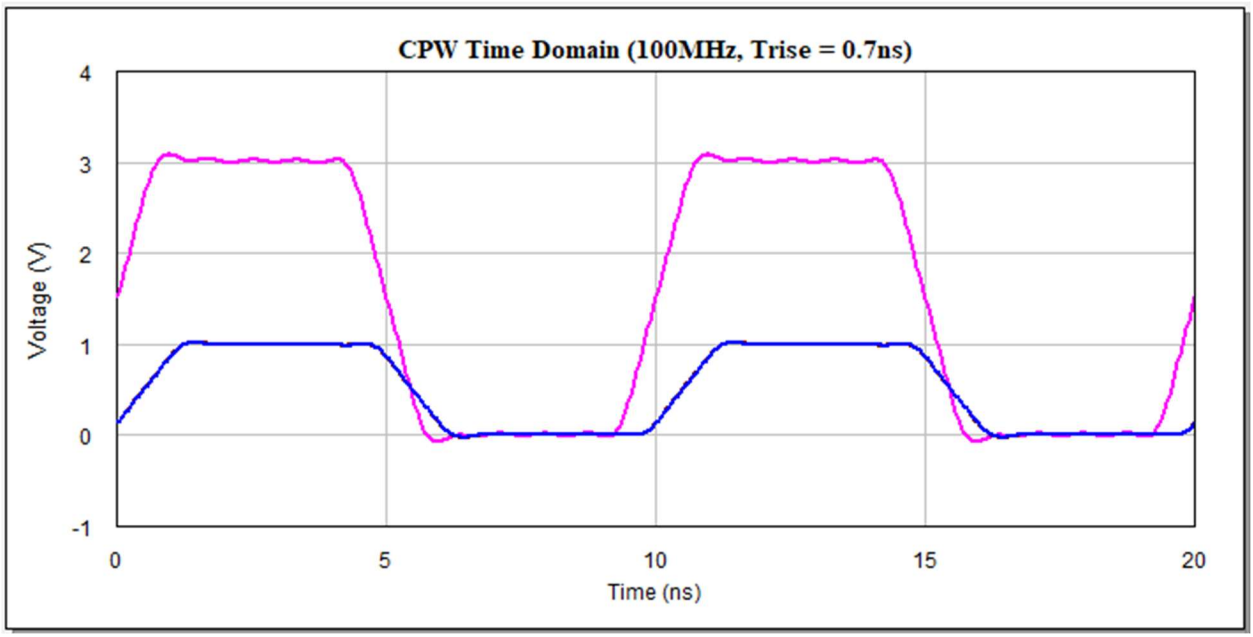

Figure 3.28. MWO 100MHz CPW clock signal, T_{rise} = 0.7ns

As with the 10MHz simulation, at 100MHz both the microstrip and GCPW show no disparity between the two output ports. The 580ps delay is now clearly visible, as is some slight ringing on the edges of the signal.

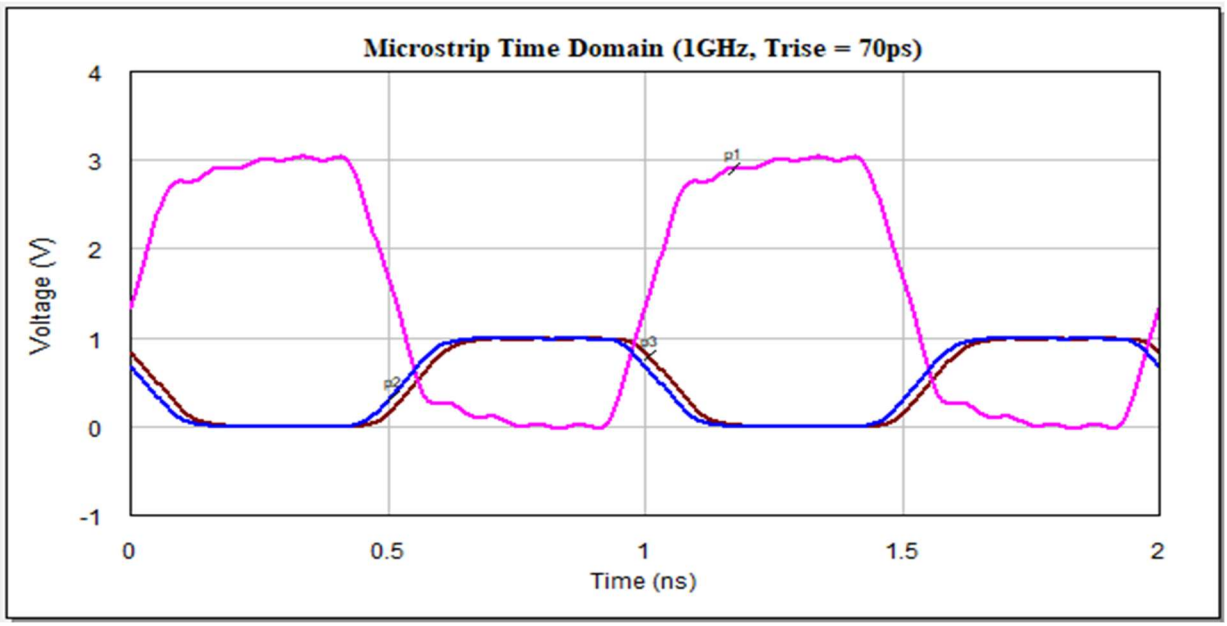

Figure 3.29. MWO 1 GHz microstrip clock signal, T_{rise} = 70ps

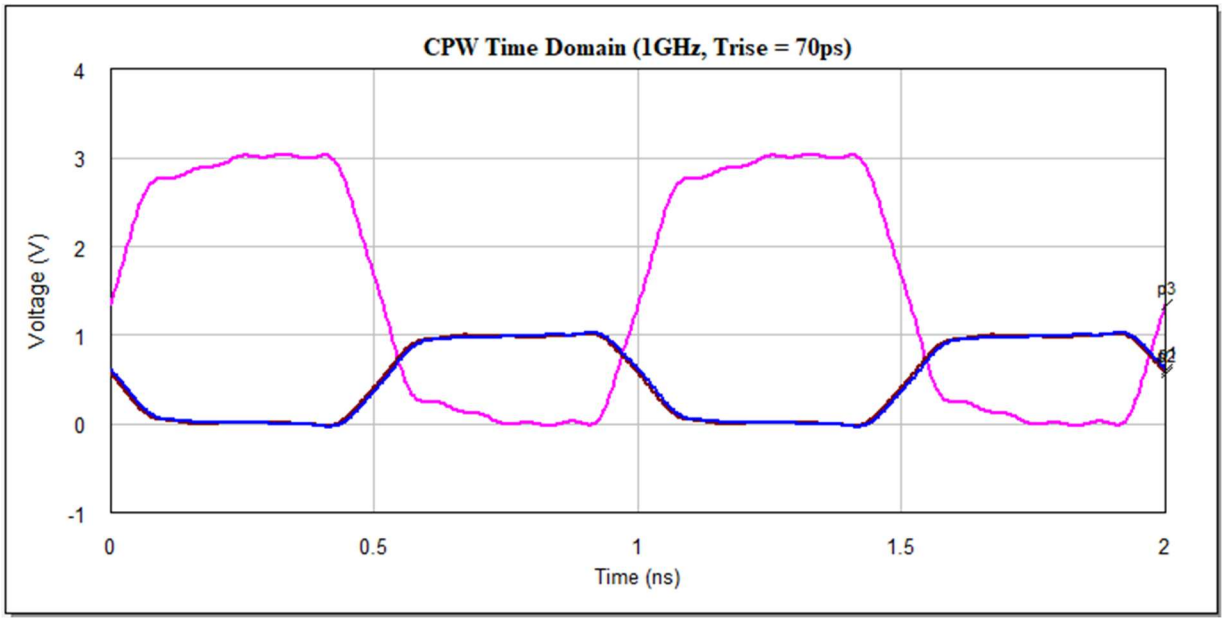

Figure 3.30. MWO 1 GHz CPW clock signal, T_{rise} = 70ps

It is at 1 GHz that the two designs begin to diverge in their ability to maintain SI. While both graphs are similar in signal attenuation and delay, the microstrip shows signs of a phase disparity

at the output ports. This is consistent with the findings in the frequency domain simulations in 3.1, where the microstrip saw a significant loss of phase synchronization in higher frequencies. There are, however, some significant differences between the MWO and LTSpice simulations:

- The MWO inclusion of bends in the transmission line gives output signals a greater degree of ringing at 100 MHz with a 700ps rise time.
- MWO shows greater delay on the microstrip line at port 3 than the GCPW.

3.2.2 *Crosstalk Circuit Model*

A significant source of intrasystem crosstalk is found in the form of near field coupling between two parallel signal paths. Near field coupling consists of rings magnetic field lines around the aggressor net conductor, creating mutual inductance, and electric field lines between the signal and return paths, which create mutual capacitance [1]. This is modeled using the LTSpice circuit model of the microstrip clock distribution circuit (Fig. 3.16) coupled to a victim net consisting of a lossy transmission line segment that simulates a portion of the straight transmission line on the prototype PCBs.

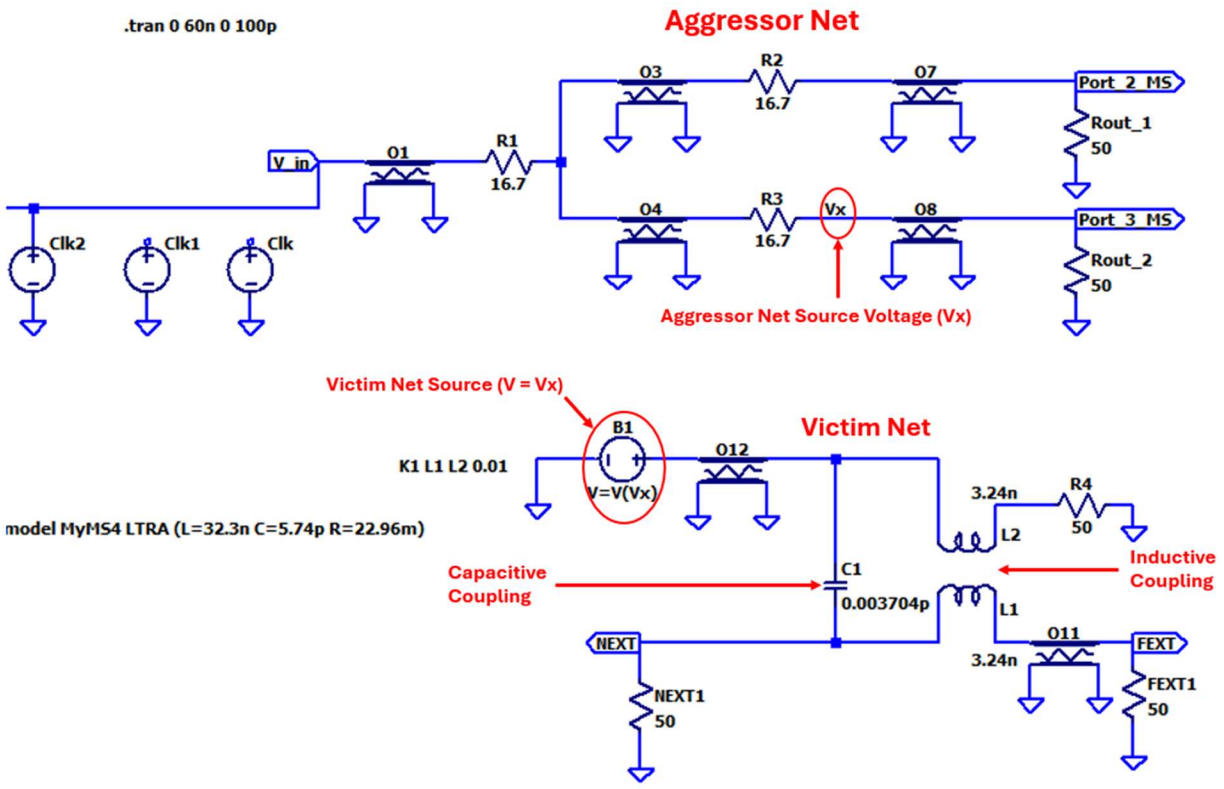

Figure 3.31. Capacitive crosstalk equivalent circuit (50MHz, T_{rise} = 2.5ns) with aggressor net (top) and victim net (bottom)

Shown in Figure 3.29 is an approximate circuit model of the crosstalk that may arise from the time delay serpentine trace on the microstrip prototype PCB shown in Figure 2.26. The LTSpice microstrip clock distribution circuit was used to simulate the aggressor net, while the victim net was coupled capacitively and inductively to simulate electric and magnetic crosstalk. The source voltage for the victim net (V = Vx) is supplied by the aggressor net at a point that represents the meandering transmission line on the clock distribution network between R3 and port 3 (Vx). The C1 capacitor value was calculated using formula for parallel plate capacitance [18] with the addition of the effective permittivity (ε_{eff}) of the prototype PCBs

$$C = \frac{\varepsilon_0 \varepsilon_{eff} A}{d} \tag{3.5}$$

calculating for capacitance (C) in Farads, where $\varepsilon_0$is the permittivity of free space, A is the area of the parallel conductor face, and d is the distance between conductors.

The values of the coupled inductors L1 and L2 are consistent with the series inductance of a section of 42 mil wide microstrip of the same length as the trace immediately adjacent to the time delay serpentine. The coupling coefficient was set at 1% of the magnetic field generated by the adjacent transmission lines due to their significant separation of 110 mil. This model does not consider the geometry of the serpentine itself, instead treating it as an adjacent straight transmission line. When the aggressor net is energized, the signal crosstalk can be measured on the output ports of the victim net (V(next) and V(fext)).

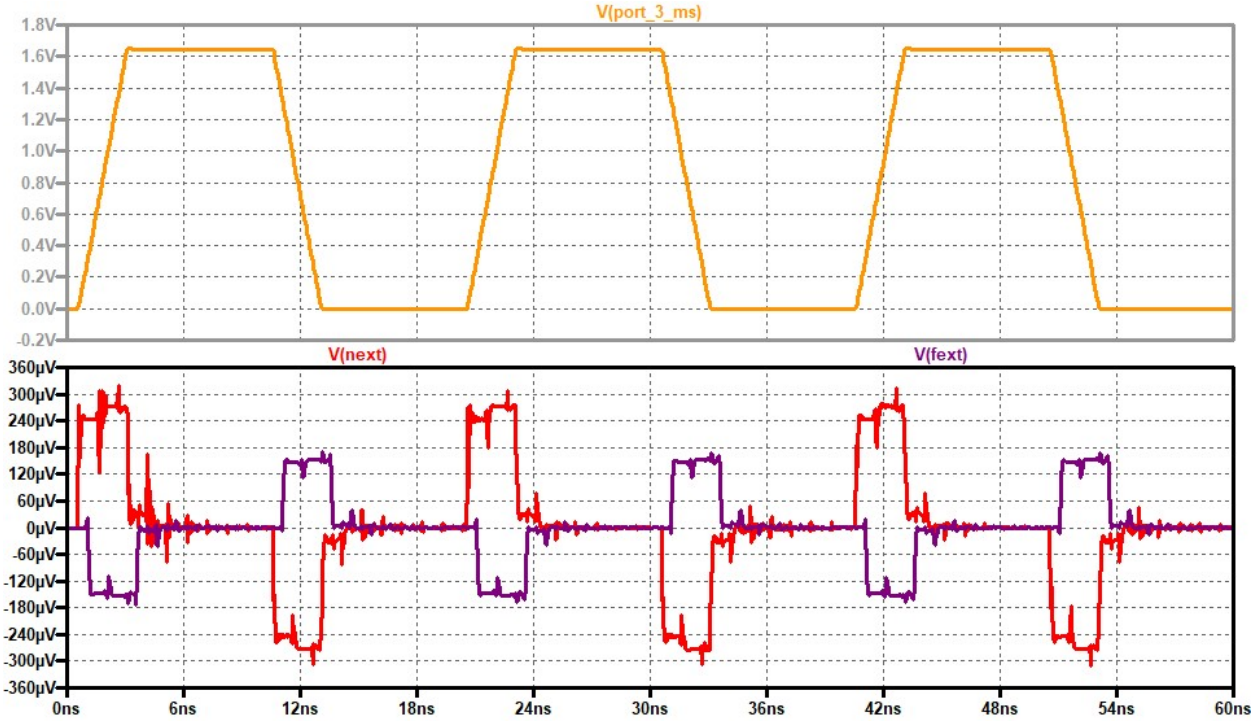

Figure 3.32. 50MHz (T_{rise} = 2.5ns) clock signal on aggressor net (top) and victim net (bottom)

In Figure 3.32, the crosstalk on the victim net with an amplitude of 0.28 mV on the near end of the victim net (NEXT), which is in the opposite direction of signal propagation, and 0.14 mV on the far end of the victim net (FEXT), which is in the direction of signal propagation. There is also a time delay from the rise edge of the NEXT signal to the rise edge of the FEXT signal of approximately 450ps, which is 78% of the overall propagation delay of the victim net transmission line. This makes sense, as the coupling region lies roughly three-quarters of the way down the victim net transmission line as viewed from port 4.

Figure 3.33. Enlarged crosstalk waveform

NEXT relates to the net coupled current on the near end terminating resistor of the victim net circuit [1], with the constant voltage of the NEXT signal representative of a saturated net. When the rising edge of a signal on the aggressor net enters the coupling region of a system, it begins to

generate near-end noise, and the amplitude of the NEXT signal will increase for a time equal to the rise time of the aggressor signal. Once the rising edge fully enters the coupling region, the amplitude of the NEXT signal will have reached its maximum value and will level out into a constant value, having become saturated. As the rising edge leaves the coupling region, the current flowing from the aggressor net to the victim net will begin to decrease, until the rising edge leaves the coupling region [1]. Because the rise time of the aggressor signal is 2.5ns, and the propagation delay of the victim net is only 580ps, this should not be possible. Because the amplitude of the FEXT signal scales to the coupling length [1], it is reasonable to infer that the lower amplitude of the FEXT signal in this simulation is due to the short coupling length along the edge of the meandering trace, which is the area at which the coupled transmission lines are in closest proximity to each other. The fact that the two coupled transmission lines on the prototype PCBs used in this project do not maintain an equivalent separation throughout the circuit, as well as the meandering nature of the aggressor net, make this a very complex system that will require further calculations to more accurately model.

Chapter 4. MEASUREMENT OF CPW VERSUS MICROSTRIP CLOCK DISTRIBUTION FOR SI

The primary objective of the clock distribution network on the two prototype PCBs is to determine whether a GCPW structure is more effective than a microstrip at maintaining signal integrity under unequal conditions. In the case of the PCBs used for this experiment, the two transmission lines immediately following the resistive splitter are of equal length (3550 mil) and characteristic impedance (50Ω) but differ in their physical layout.

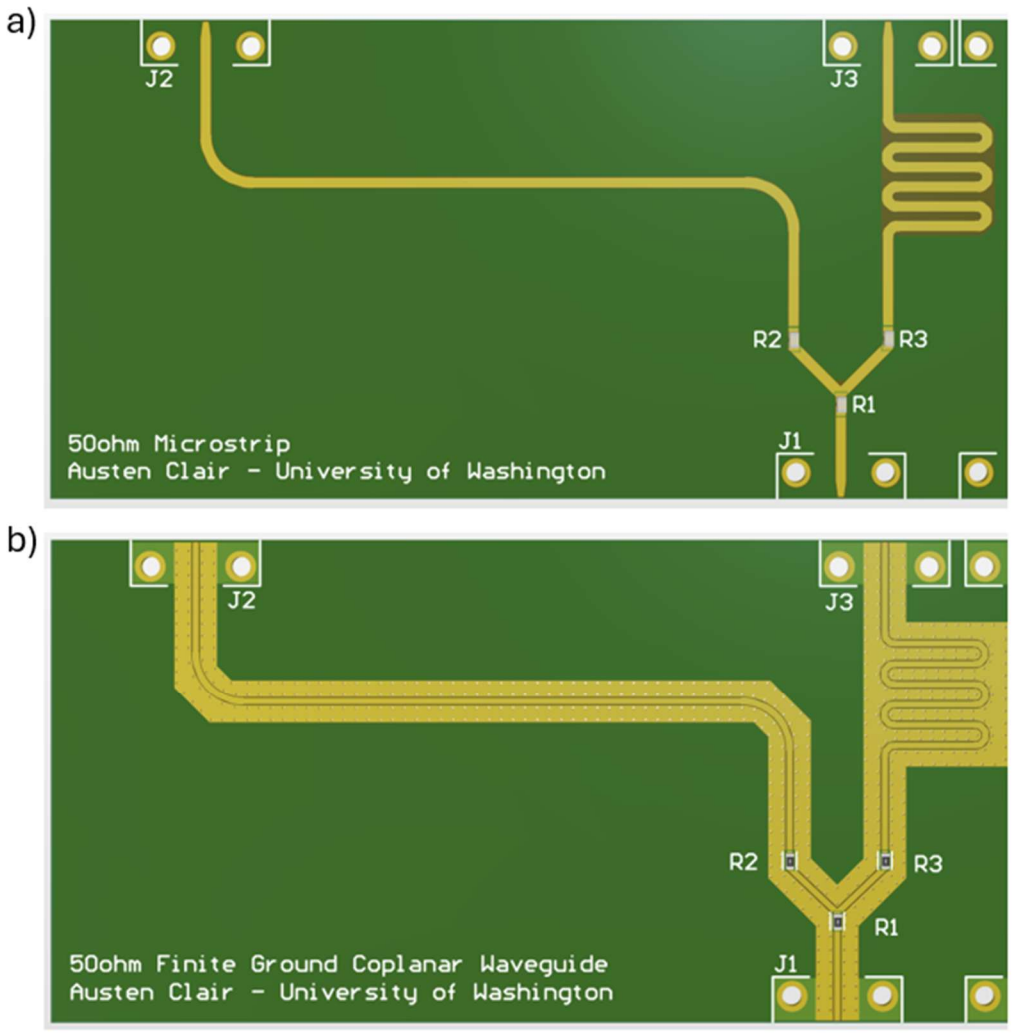

Figure 4.1. Microstrip (a) and GCPW (b) clock distribution circuit layouts

Theoretically, two transmission lines with equal delay times that share an input signal should produce an equal response at their respective output ports. This chapter will measure frequency and time domain results of this circuit and determine which transmission line structure is superior in maintaining SI.

4.1 Frequency Domain Measurements for SI

Frequency domain measurements were taken from 300 KHz to 6 GHz using a 2-port Tektronix TTR506A USB vector network analyzer (VNA). To effectively measure the prototype PCBs, which each have five ports, multiple measurement sets were taken with 50Ω RF terminators on each unused port.

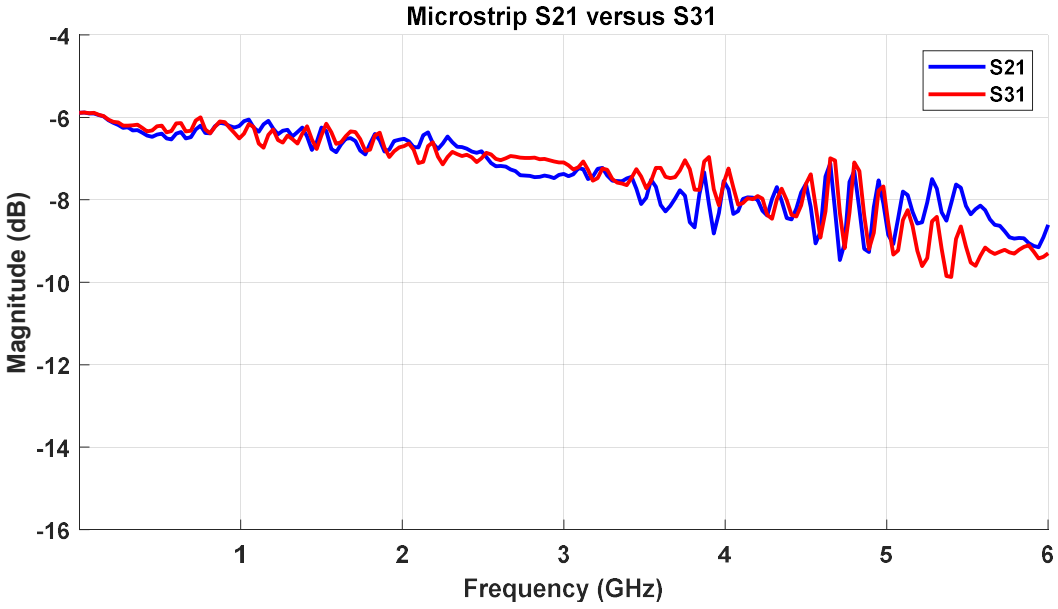

Figure 4.2. Microstrip S_{21} versus S_{31} measurement

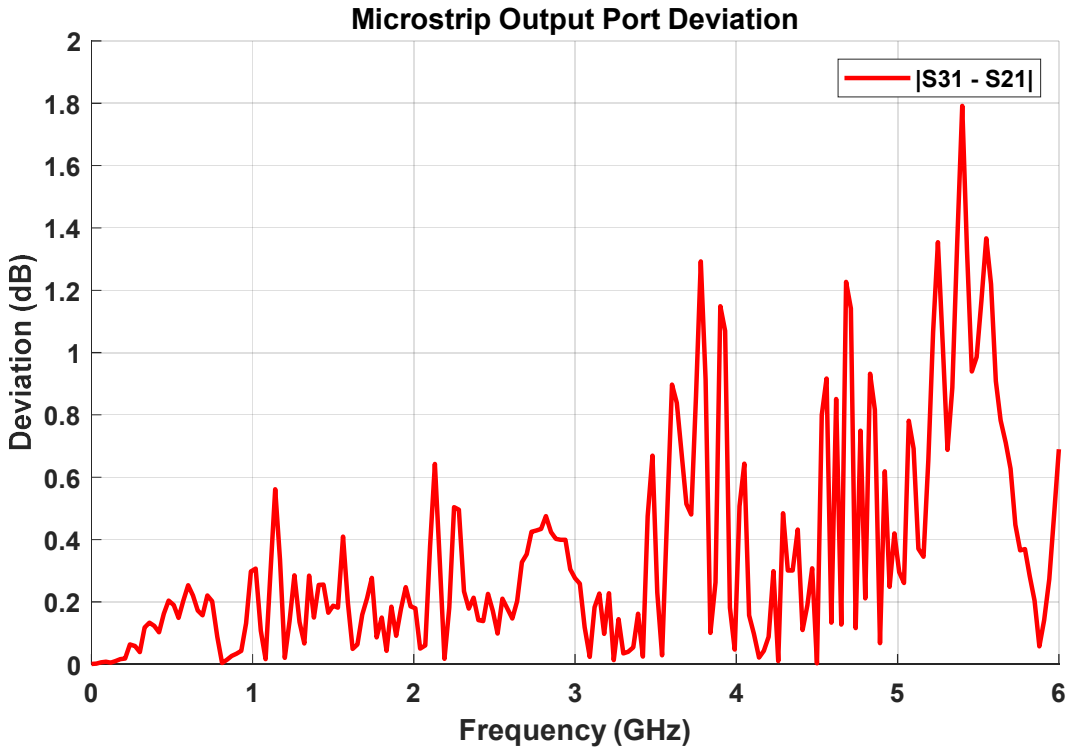

Figure 4.3. Difference between S_{21} and S_{31} on the microstrip clock distribution network

Figure 4.2 represents the S-parameter behavior of the known stimulus signal after propagating through the clock distribution circuit, while Figure 4.3 plots the deviation $|S_{31}-S_{21}|$ between the two output ports. The two signals, while theoretically equal, deviate up to 1.8 dB from each other, and rarely synchronize.

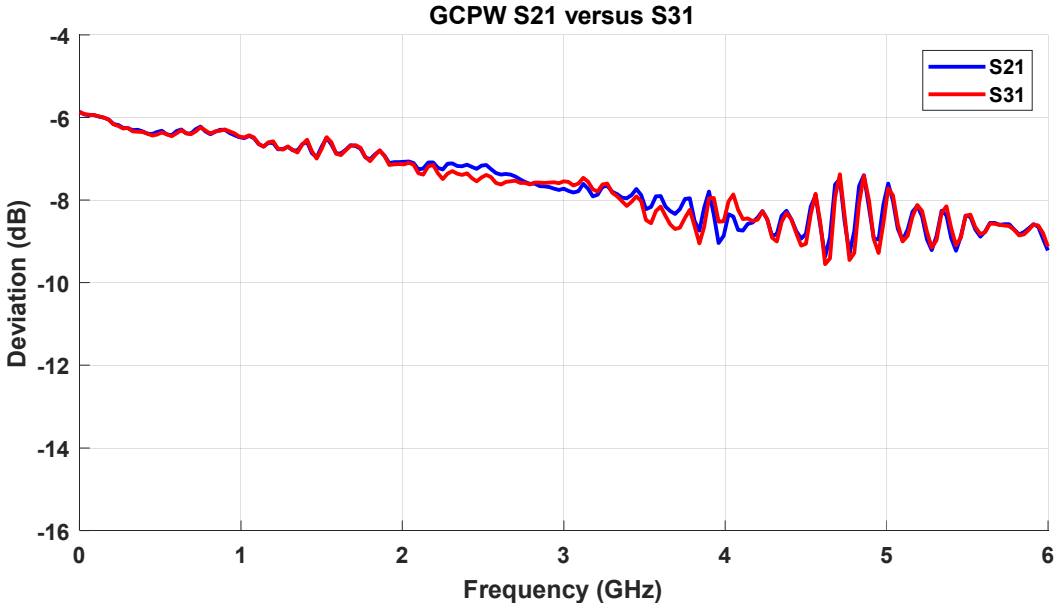

Figure 4.4. GCPW S_{21} versus S_{31} measurement

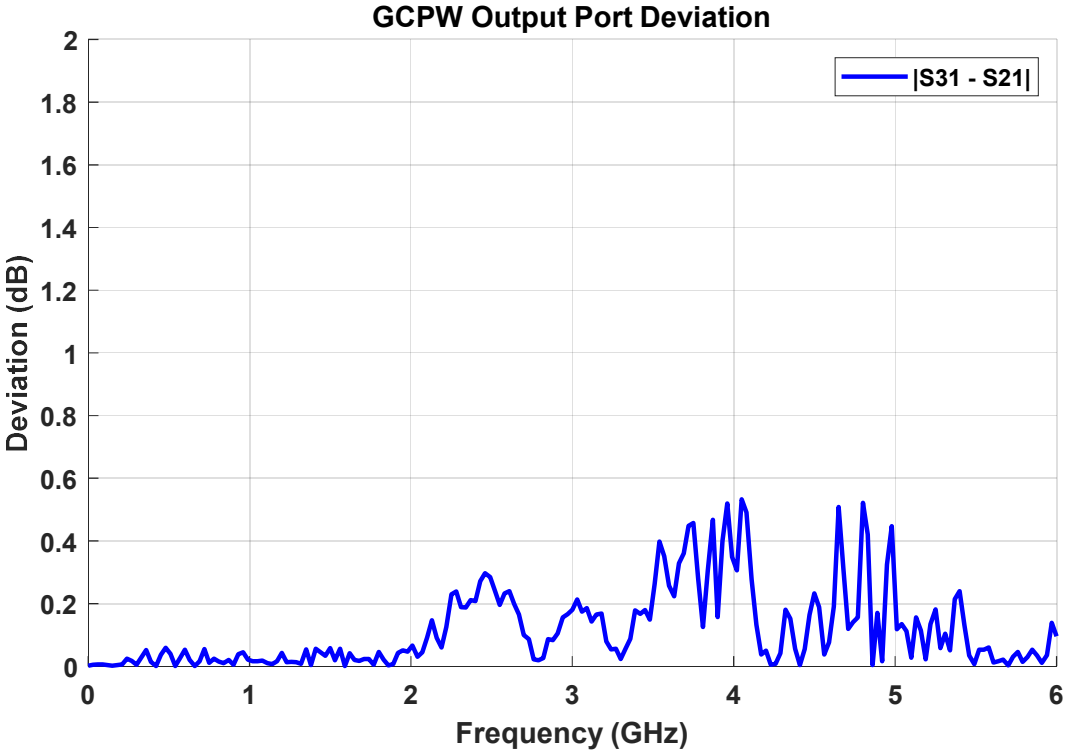

Figure 4.5. Difference between S_{21} and S_{31} on the GCPW clock distribution network

The S_{21} versus S_{31} properties for the GCPW (Fig. 4.4) display similar curves regarding loss, however they differ in that the two signals maintain a much greater degree of continuity, as seen in Figure 4.5. The greatest degree of deviation between ports 2 and 3 on the GCPW circuit occurs between 2 and 5 GHz, where it still only reaches 0.53 dB.

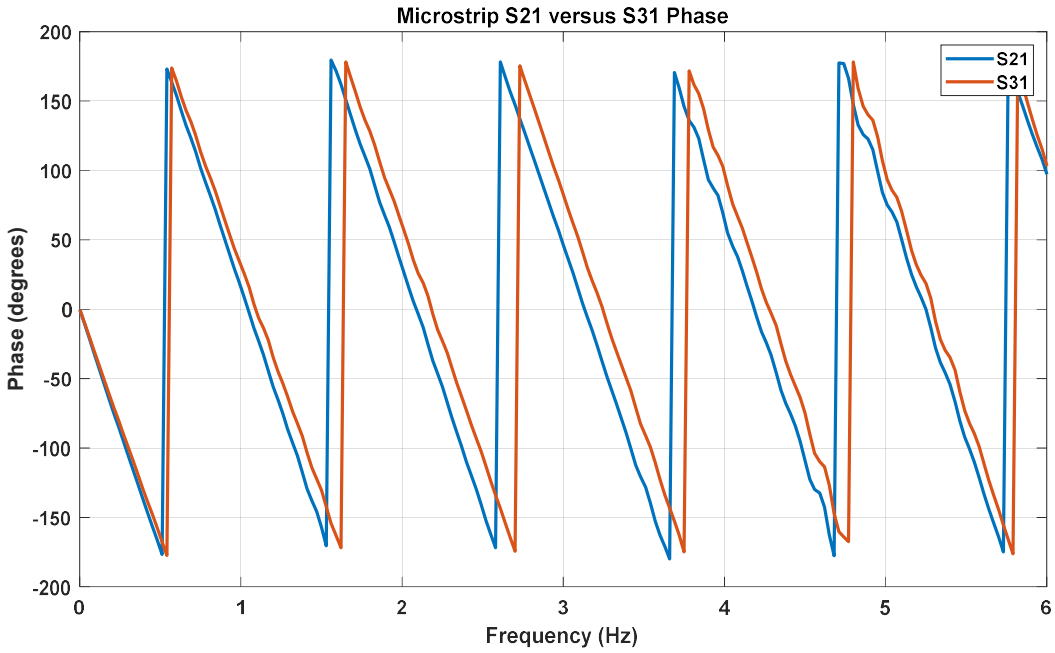

Figure 4.6. Microstrip S_{21} versus S_{31} output phase measurement

The microstrip output phase relationship in Figure 4.3 is mostly consistent with the simulated response, albeit cleaner and more uniform. The output phase at ports 2 and 3 starts off matched, but almost immediately diverges and remains disparate throughout the entire bandwidth, only beginning to reconverge near 6 GHz. This divergence, commonly known as dispersion, will result in individual frequency components losing their original phase relationships as they propagate along the transmission line, causing signal distortion [10].

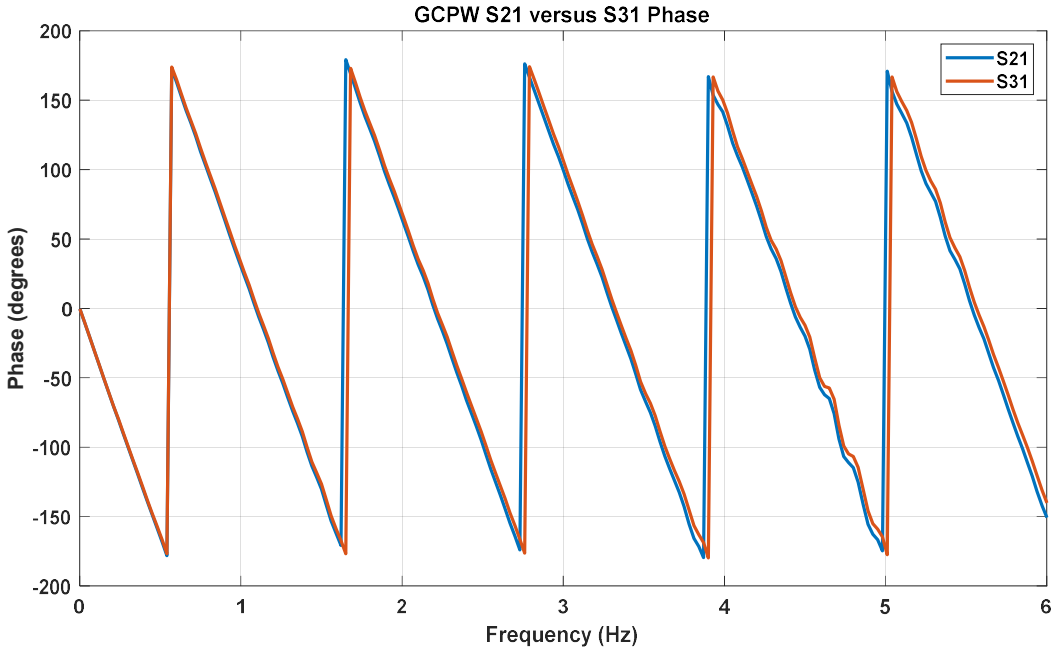

Figure 4.7. GCPW S_{21} versus S_{31} output phase measurement

Consistent with the simulation from 3.1.1, the GCPW output phase relationship between ports 2 and 3 maintains a much lower level of dispersion throughout the spectrum, deviating slightly around 1.6 GHz and remaining consistent through 6 GHz. This is indicative of a higher degree of SI than the data provided by microstrip measurements.

When considering the phase delay present on both PCBs, it is helpful to convert to group delay to determine the difference in time it takes for the signal to propagate. Group delay is defined as "...the rate of change of transmission phase angle with respect to frequency" [16] and pertains to the envelope of a modulated signal as it propagates through the system; in this case, the envelope in question is the spectrum from 0 to 6 GHz. Group delay is represented by the equation:

$$Group\ Delay\ (s) = -\frac{\Delta\Phi\ (rad)}{\Delta\omega\ (rad/s)} \tag{3.5}$$

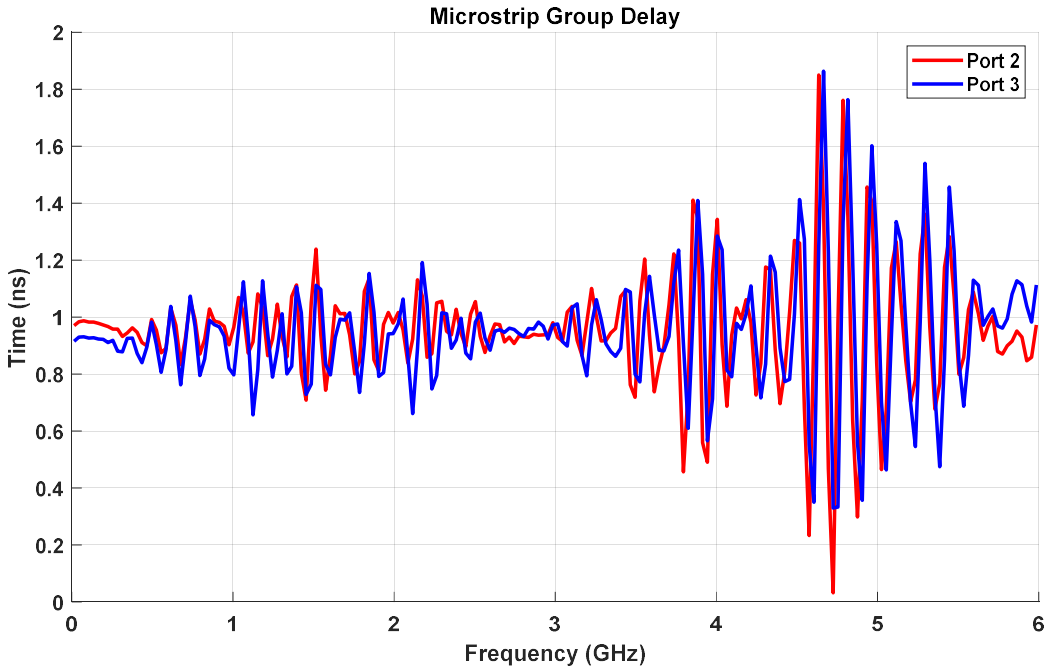

Figure 4.8. Group delay with respect to frequency plot for the microstrip PCB

As can be seen in Figure 4.6, it is very seldom that ports 2 and 3 on the microstrip PCB experience the same group delay with respect to frequency, which is suggestive of a constant state of dispersion between the ports; this is evident wherever the red of port 2 is visible outside of the blue Port 3 overlay.

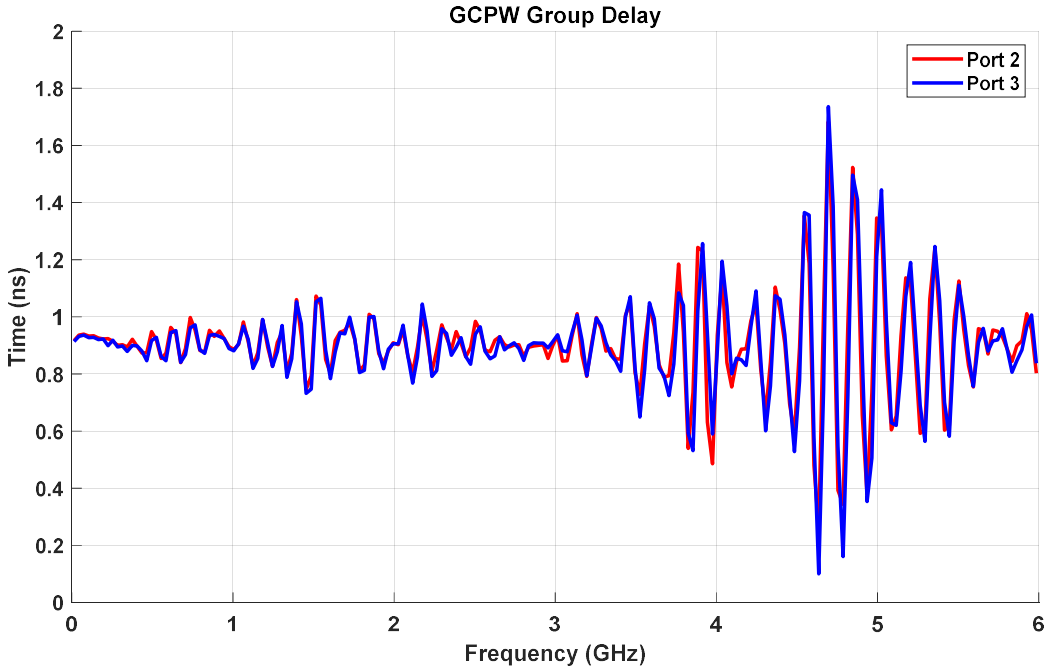

Figure 4.9. Group delay with respect to frequency plot for the GCPW PCB

When compared to Figure 4.6, the GCPW group delay plot in Figure 4.7 shows very little evidence of dispersion. These findings are consistent with the phase relationships explored in Figures 4.4 and 4.5, which provide evidence of a higher degree of SI maintained in the GCPW clock distribution circuit. To plot and compare the level of skew with respect to frequency, the plots in Figures 4.6 and 4.7 will be subjected to a function that will plot the difference in group delay with a superimposed threshold. As a rule of thumb, clock skew should be less than 10% of the clock period [15], therefore $0.1T$ will be chosen as the threshold to provide a reference for comparison between the microstrip and GCPW PCBs.

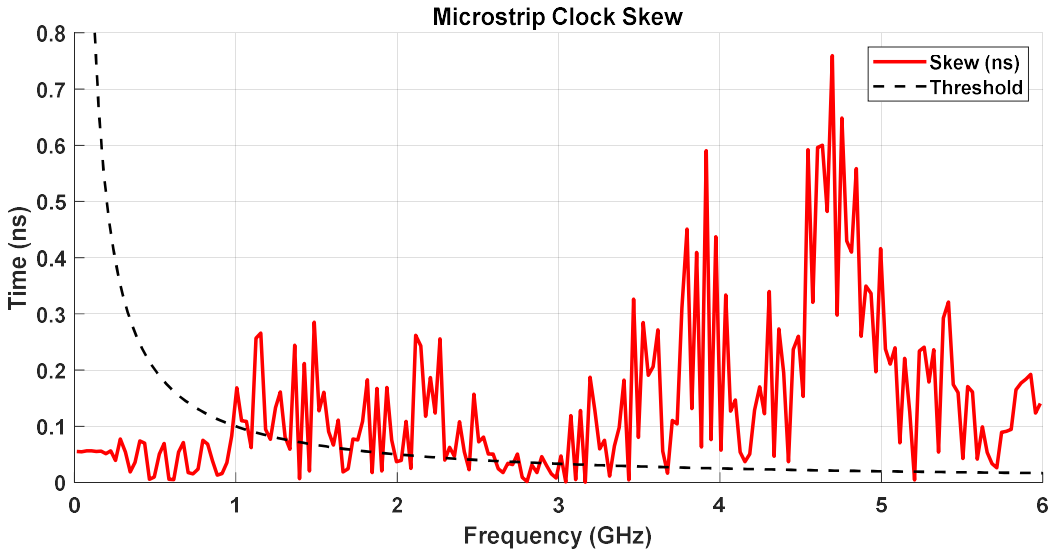

Figure 4.10. Clock skew (|Port 3 – Port 2|) on the microstrip PCB

Given the imposed threshold of $0.1T$, the microstrip PCB only operates effectively until approximately 1 GHz, after which skew consistently surpasses the 0.1T threshold.

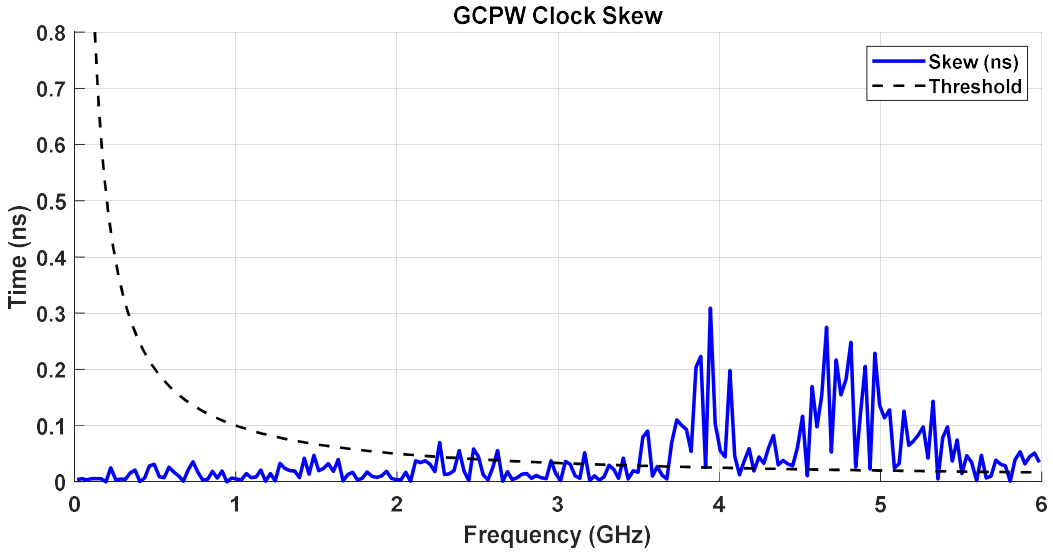

Figure 4.11. Clock skew |Port 3 – Port 2| on the GCPW PCB

The GCPW PCB displays significantly less skew, operating below the $0.1T$ threshold for half of the measured spectrum aside from some intermittent peaks in skew that pass above the threshold.

The GCPW only encounters significant skew around 3.5 GHz, with a maximum skew of only 0.3ns. With further modification after a comprehensive design review, it is not unreasonable to expect that an improved GCPW design will be able to keep skew below $0.1T$ up to, and possibly exceeding, 6 GHz. The plots in Figures 4.10 and 4.11 are consistent with the output port deviation plots in Figures 4.3 and 4.5 in providing proof of the greater ability of the GCPW PCB in maintaining SI.

As in Chapter 3, output port isolation (S_{23}) was measured on the VNA by taking a two-port measurement at ports 2 and 3 and terminating all other ports with 50Ω RF terminators.

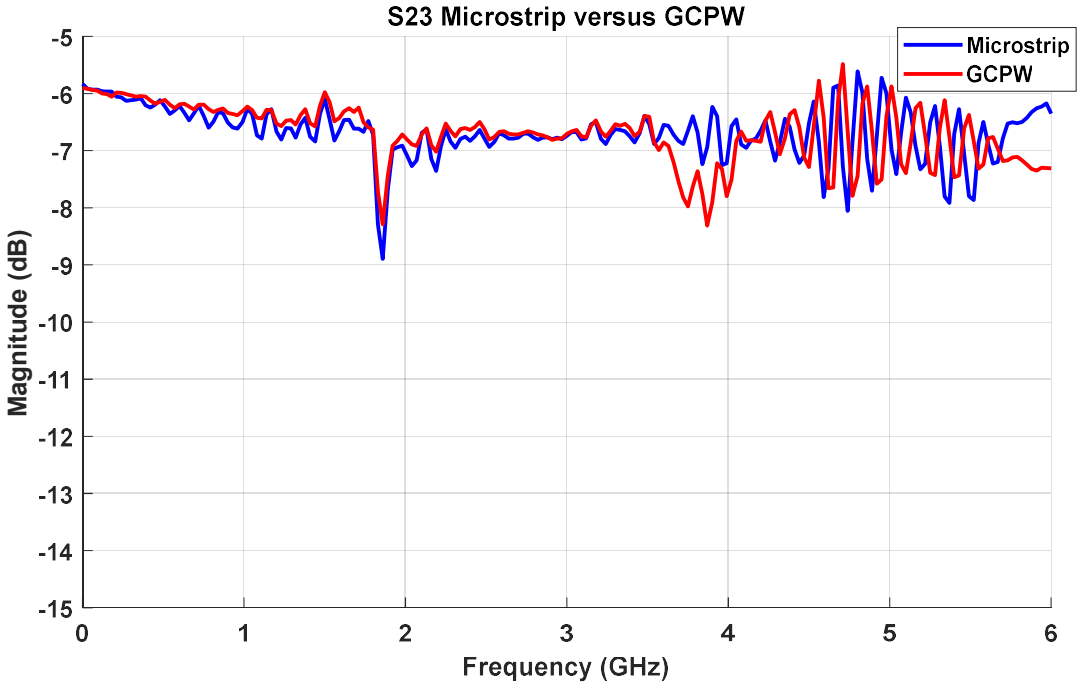

Figure 4.12. Microstrip versus GCPW S_{23} measurement

When observing the S_{23} measurements, the two PCBs exhibit similar behavior throughout much of the spectrum, with the GCPW maintaining slightly less loss than the microstrip. Because of the reciprocal nature of the divider circuit, a 6 dB net loss like that seen in Figure 4.12 is

expected. It is worth also plotting the full three-port parameter measurements for both PCBs to observe how output port isolation correlates with S_{21} and S_{31}.

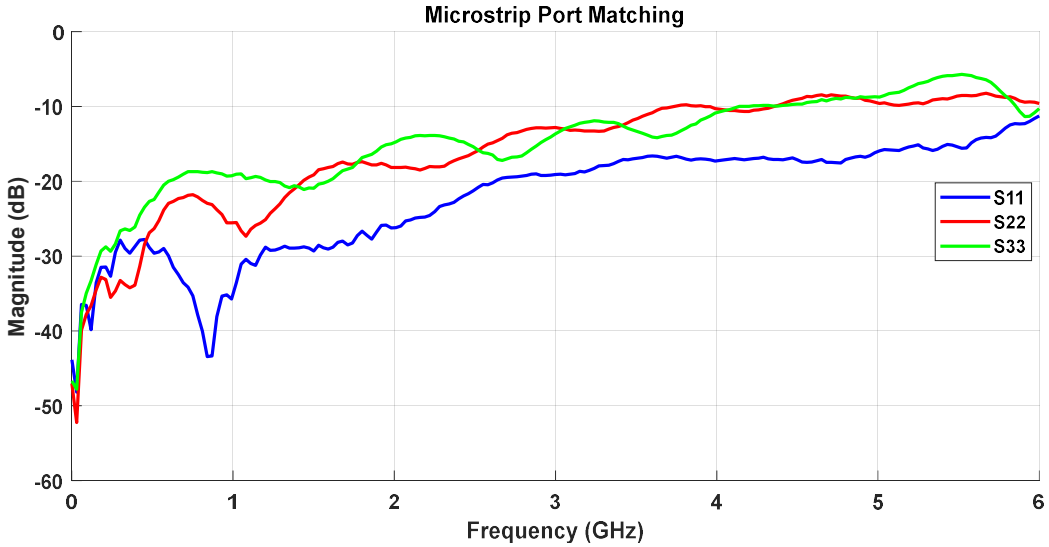

Figure 4.13. Microstrip S_{11}, S_{22}, and S_{33} measurements

The three port microstrip circuit, while maintaining a similar curve between all three ports in Figure 4.11, is clearly not matched. While S_{22} and S_{33} follow a similar curve, they are continually deviating, and S_{11} displays significantly more loss throughout the spectrum. Theoretically, as shown in equation 3.3 and outlined by Dr. Pozar in *Microwave Engineering* [10], $S_{11} = S_{22} = S_{33}$ in an ideal resistive splitter circuit. In these prototype PCBs, however, the lossy effects of the transmission lines, the modified design of the resistive divider, and the non-ideal resistors must also be considered. It is important to note that there is no instance that will allow a single divider to be lossless, matched, and reciprocal [10]. A reciprocal network is one in which a change in the conditions at one port affects the other two ports; a network is matched when the characteristic impedance at all three ports is the same as their respective port impedance; and though no network is truly 'lossless,' one can be classified as lossless when all of the power of a wave at any one port is equal to the sum of the power exiting the other two ports [14]. The resistive

splitter is defined as a matched, reciprocal network; all transmission lines carry a characteristic impedance of 50Ω and terminate at 50Ω ports, and the scattering matrix shows reciprocity (3.2) in that $S_{21} = S_{12}$, $S_{31} = S_{13}$, and $S_{21} = S_{32}$. It is not, of course, lossless, due to the resistors included in the circuit.

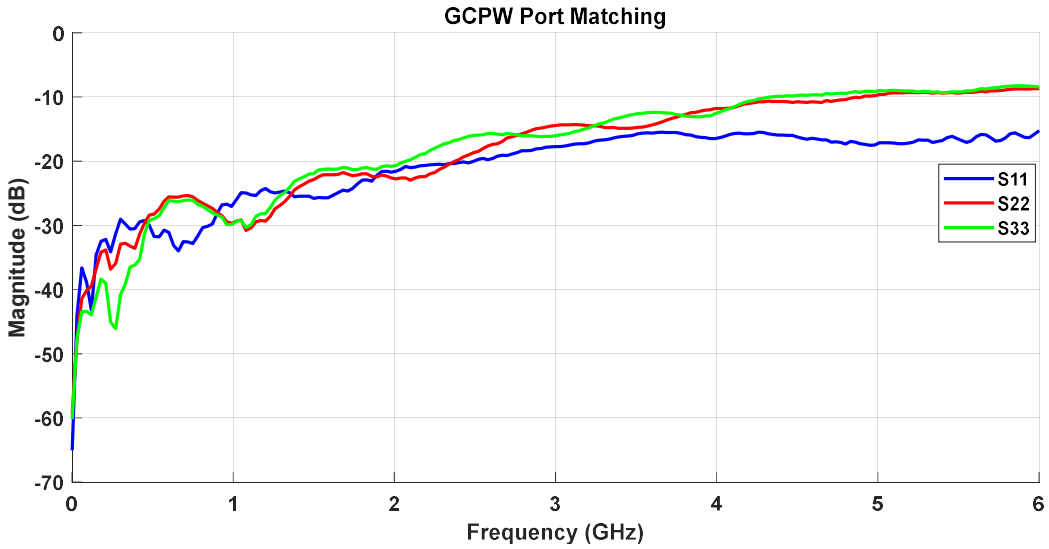

Figure 4.14. GCPW S_{11}, S_{22}, and S_{33} measurements

Unlike the microstrip, the GCPW ports are significantly more matched until approximately 4 GHz, where port 1 begins to experience more reflection. The similarities between the two plots confirm that there are factors that do not reflect on the transmission line structures, such as the initial resonance dip at 1 GHz. There is a high likelihood that similarities such as this between the two PCBs are the result of elements present in both circuits, such as the resistors or the geometric structure of the resistive splitter. More insight into these properties can be gained by plotting the net loss of each clock distribution circuit by utilizing equation 3.4 with the measured S-parameters of each PCB.

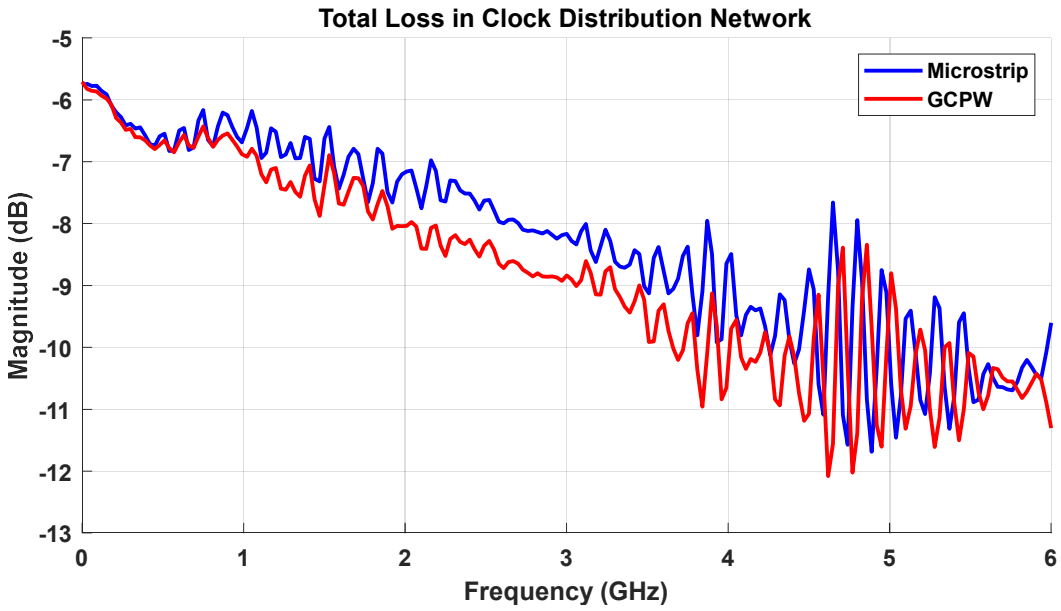

Figure 4.15. Total loss measured in microstrip and GCPW clock distribution circuits

The total loss curve comparison in Figure 4.11 confirms two things; the GCPW transmission line structure, as observed while testing the straight transmission line losses in Chapter 2 (Fig. 2.10), is more lossy than the microstrip, and both curves, while differing in magnitude, follow a very similar trend regarding frequency response ripple and slope. The latter fact is further evidence that much of the loss suffered is due to shared characteristics, and the source of the ripple is external to the PCBs.

4.2 Time Domain Measurements for SI

The GCPW and microstrip clock distribution circuits were energized by a 3.3V 50MHz clock pulse with a 50% duty cycle and a rise time of 2.5 nanoseconds using a Tektronix AFG3252 arbitrary function generator. Measurements were then taken with a Rohde and

Schwartz RTE 1054 oscilloscope. Because the function generator was only able to produce an acceptable clock pulse at 50MHz, further testing at higher frequencies will have to be conducted once more advanced equipment becomes available.

Figure 4.16. 50 MHz clock pulse direct from generator (orange) and on microstrip port 2 (yellow) and port 3 (green)

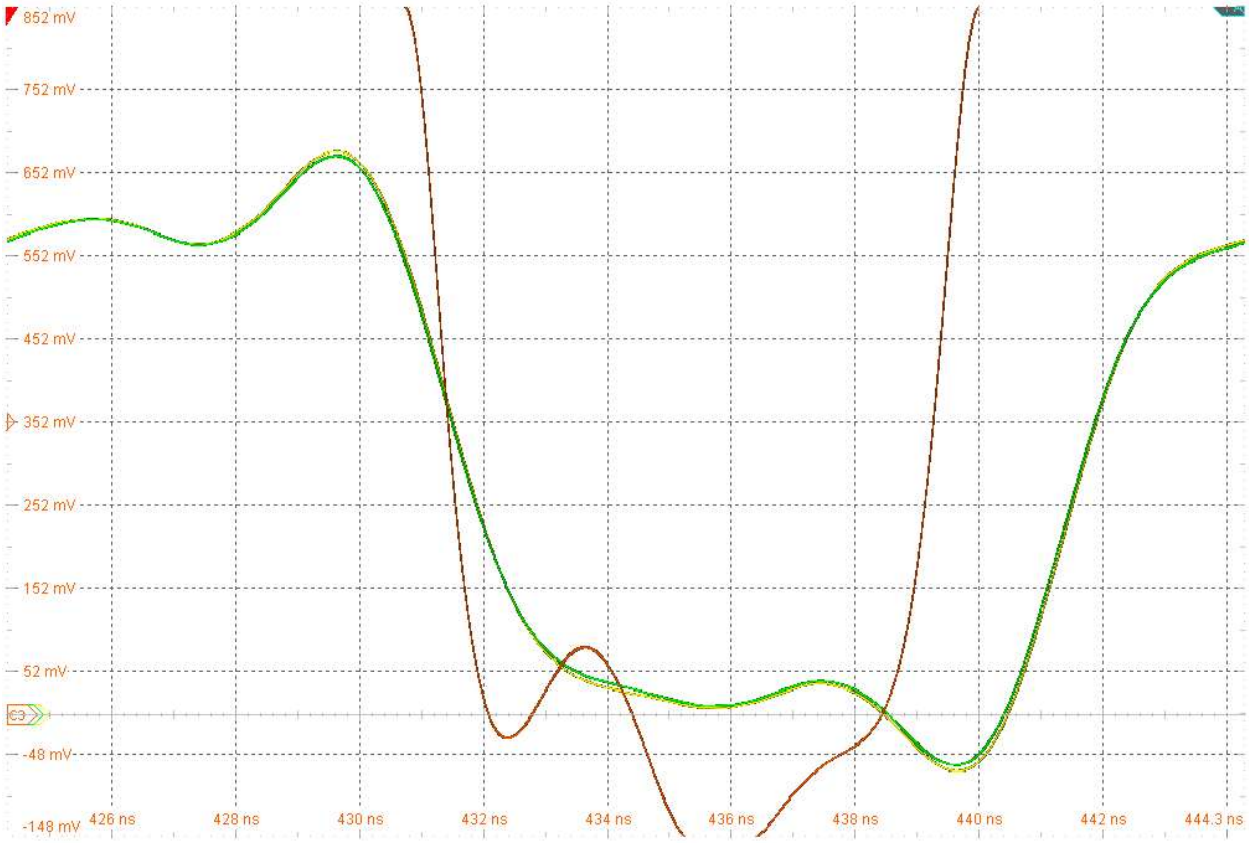

Figure 4.17. 50MHz clock pulse direct from generator (orange) and on microstrip port 2 (yellow) and port 3 (green) enlarged

At 50MHz, the microstrip PCB suffers from noticeable attenuation on port 3 and a slight phase delay on the rise-edge of the signal. These disparities are small enough that they are not obvious (Fig. 4.16) until the plot is magnified (Fig. 4.17). While small, however, this is still an effective representation of a loss of signal integrity even at relatively low frequencies, and SI will only degrade further as frequency increases. These plots differ from the LTSpice 50MHz simulation in that the slight attenuation and delay between output ports, while not present in the simulation until 1 GHz, is already visible at 50 MHz when measured.

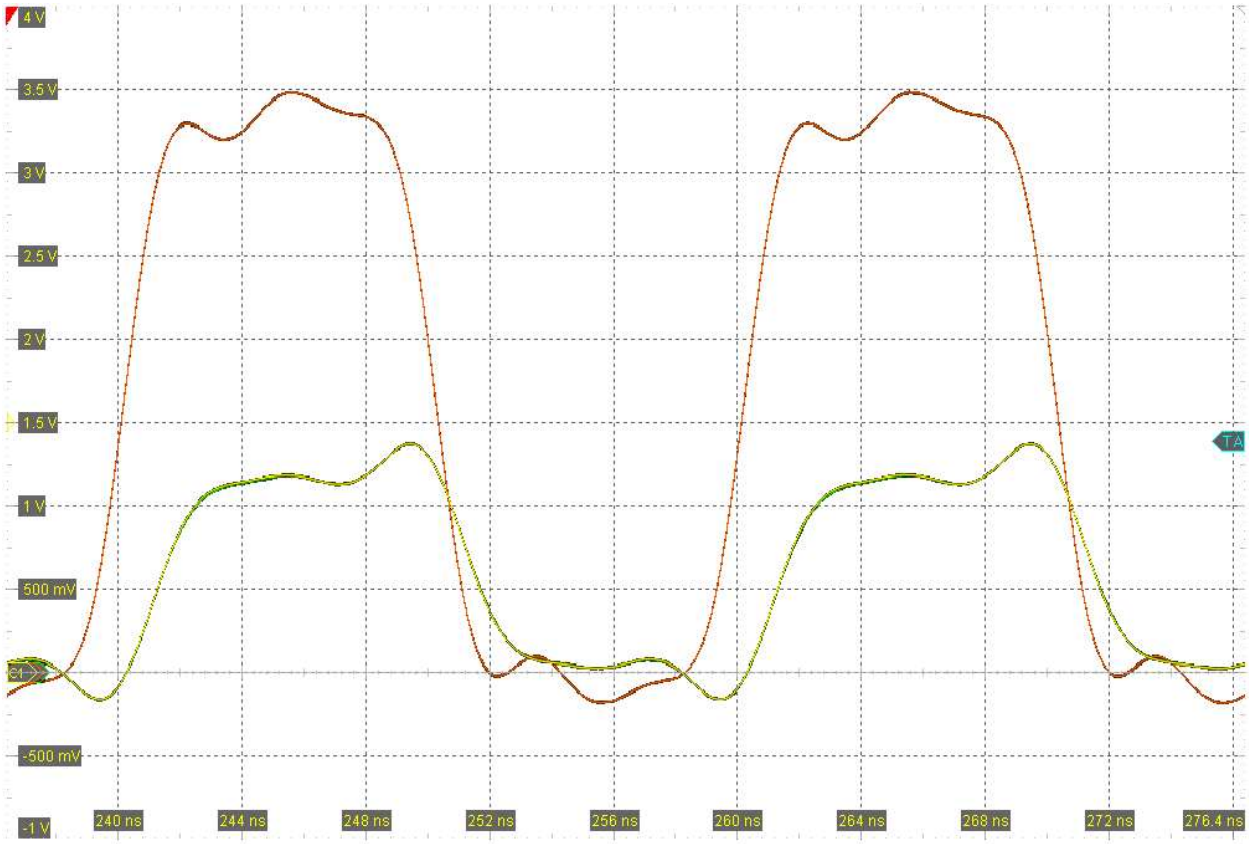

Figure 4.18. 50 MHz clock pulse direct from generator and on GCPW port 2 (yellow) and port 3 (green)

Observing Figure 4.13, the attenuation present when measuring the microstrip PCB is absent when measured on the GCPW PCB. Further testing with more advanced equipment in the future will determine how effective the GCPW structure is at maintaining SI at frequencies more commonly present in modern digital circuits. It will be beneficial to continue time domain testing on both prototype PCBs at higher frequencies beyond the scope of this project.

Chapter 5. MEASUREMENT OF CPW VERSUS MICROSTRIP FOR CROSSTALK

Intranet crosstalk was measured by observing signals at ports 4 and 5 of the straight transmission lines of both prototype PCBs by energizing their respective clock distribution networks. Any signal magnitude or waveforms present represent near-field and far-field electromagnetic crosstalk transferring from the clock distribution network to the straight transmission line.

5.1 Frequency Domain Measurements for Crosstalk

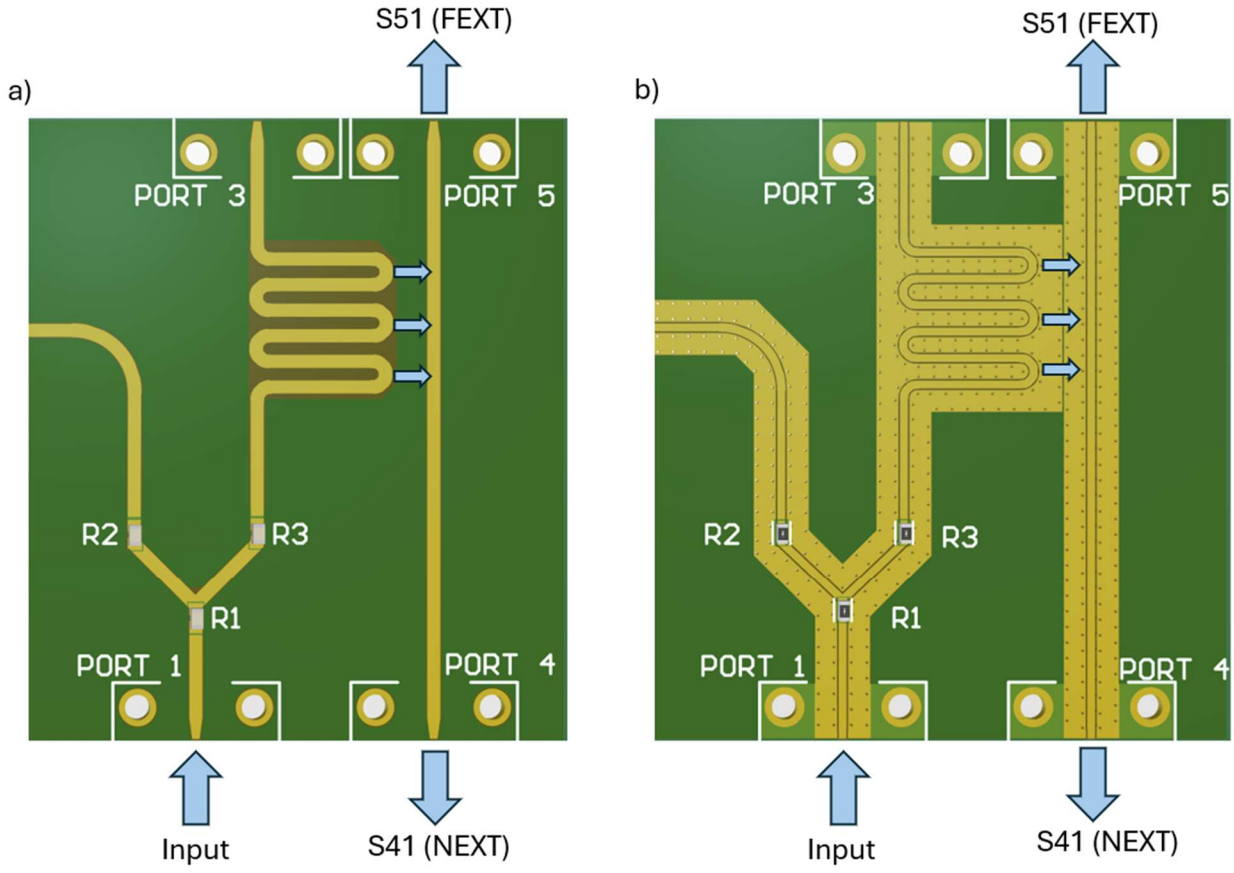

Figure 5.1. Crosstalk signal diagram for microstrip (a) and GCPW (b) PCBs

Frequency domain NEXT (S_{41}) and FEXT (S_{51}) measurements were taken using the Tektronix TTR506A VNA by terminating all unused ports with 50Ω RF SMA terminators. Signals are applied to port 1 to propagate through the clock distribution network to Ports 2 and 3. Measurements of any electromagnetic NEXT and FEXT coupling from the network will be measured at the input (port 4) and output (port 5) ports of the straight transmission line.

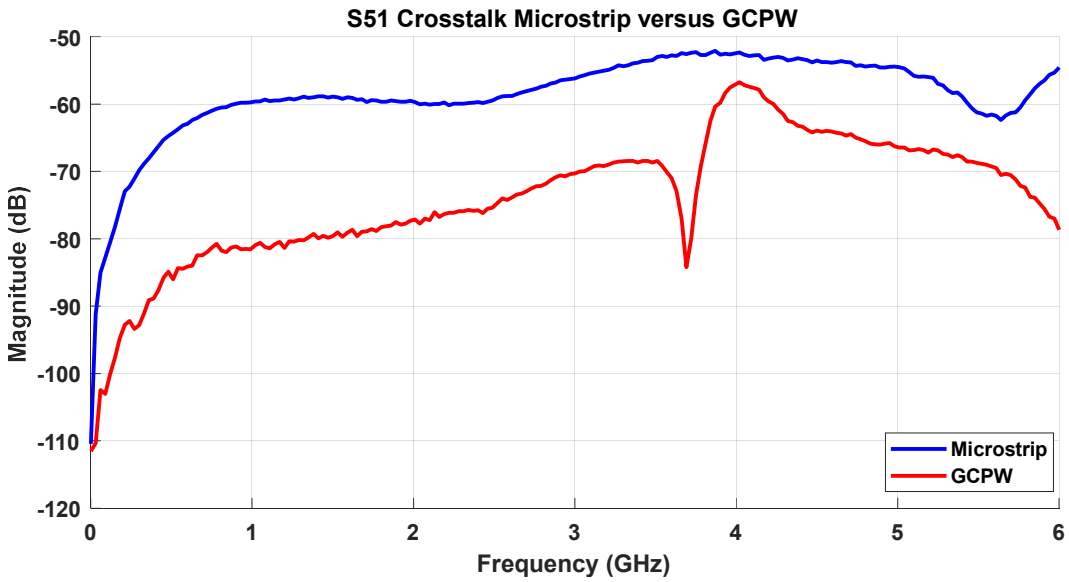

Figure 5.2. Microstrip versus GCPW FEXT (S_{51}) crosstalk measurements

The results in Figure 5.2 show that, much as in the S_{51} simulation, the GCPW PCB outperforms the microstrip PCB at reducing crosstalk from 5 dB to more than 20 dB across the entire spectrum.

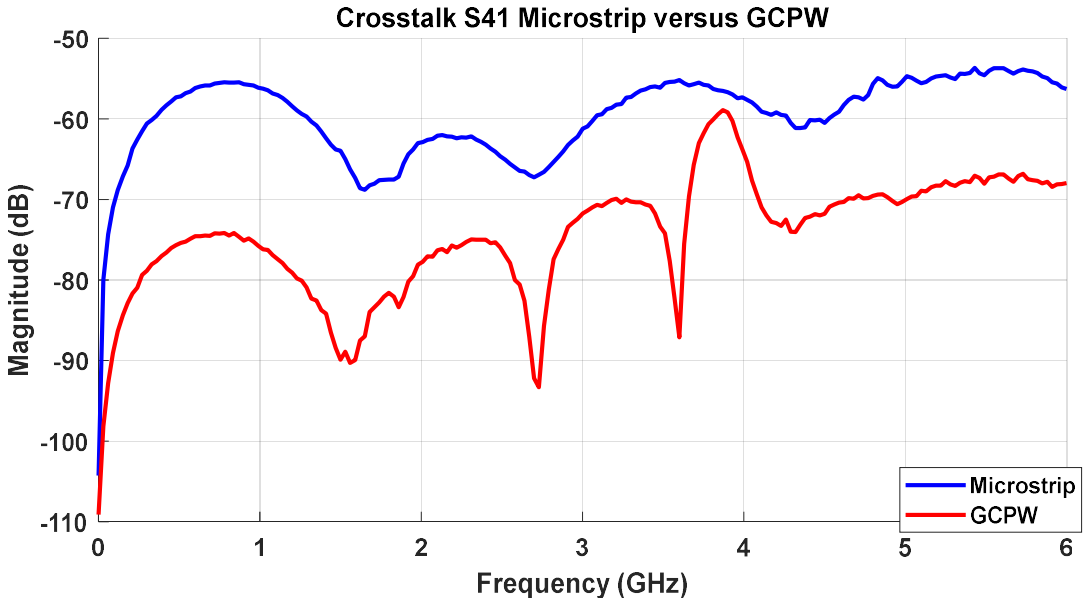

Figure 5.3. Microstrip versus GCPW NEXT (S_{41}) crosstalk measurements

As expected, the GCPW again outperforms the microstrip in reducing crosstalk, be it NEXT or FEXT. Magnitude averages remain relatively constant between the two plots, with NEXT displaying more frequency resonances than FEXT.

5.2 Time Domain Measurements for Crosstalk

NEXT and FEXT were measured in the time domain using the same Tektronix AFG3252 arbitrary function generator and Rohde and Schwartz RTE 1054 oscilloscope that were utilized for SI testing in Chapter 4. The GCPW and microstrip clock distribution circuits were again energized at port 1 by a 3.3V 50MHz clock pulse with a 50% duty cycle and a rise time of 2.5 nanoseconds, and ports 2 and 3 were terminated with 50Ω RF terminators to effectively simulate a loaded through-circuit. Output measurements were taken from port 4 to measure NEXT, and port 5 to measure FEXT.

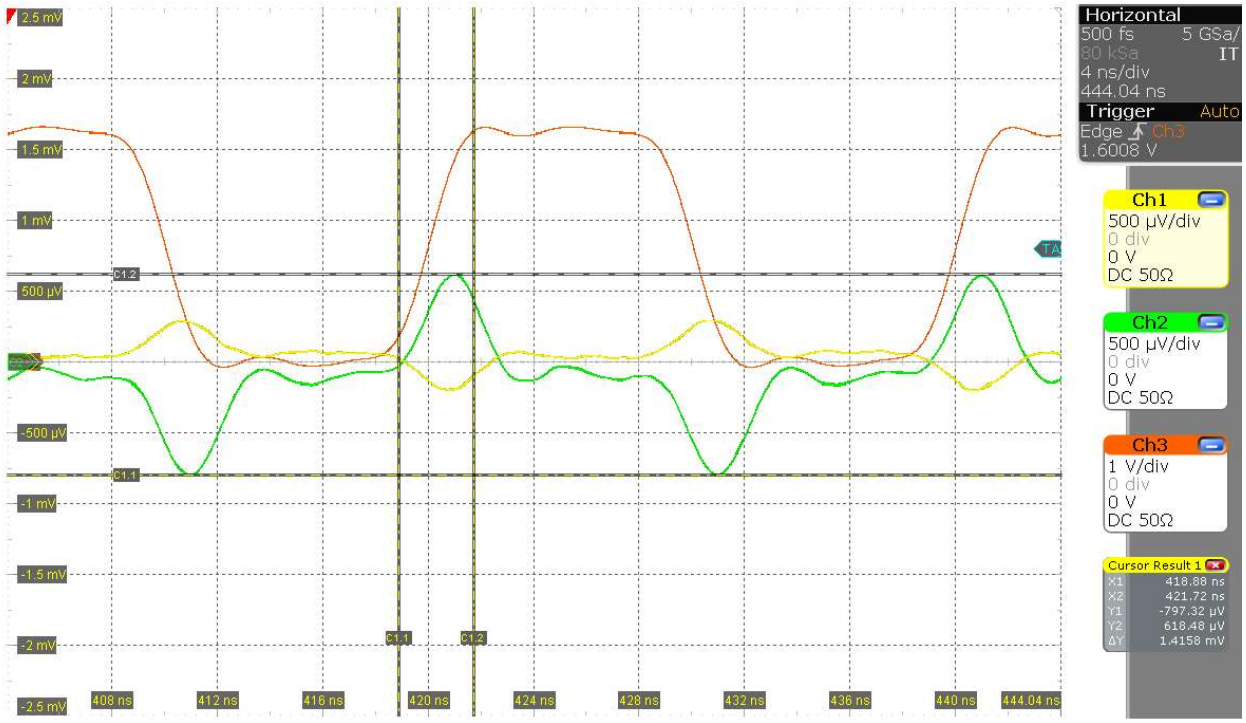

Figure 5.4. Microstrip NEXT measured at port 4 (Ch 2, 0.5mV/div), FEXT measured at port 5 (Ch 1, 0.5mV/div) and input clock pulse (Ch 3, 1V/div)

When NEXT is measured on port 4 of the microstrip straight transmission line, there is a clearly discernable waveform with an amplitude of 1.4158mV created by the electromagnetic coupling between the clock distribution circuit and the straight transmission line. FEXT, as in the LTSpice crosstalk simulation (Figs. 3.32 and 3.33), is of lower amplitude than NEXT, with a 180-degree phase shift. Both waveforms have a period of 20 ns, and each pulse in the crosstalk signal coincide with the rise and fall edges of the clock pulse. An aspect that differs from the LTSpice simulation is the saturation of the NEXT signal. Because the NEXT waveform in Figure 5.4 never reaches a constant value, it did not saturate, meaning that the 2.5ns rising edge of the aggressor net signal doesn't fully enter the coupling region before it emerges from the other side. Because it takes a

signal 496ps to propagate from resistor R3 to port 3, with less than 400ps of that time spent in the time delay serpentine, NEXT never saturates, reaching only a fraction of its maximum value. This explains the rise and fall of the NEXT waveform without reaching a constant maximum, with the fall edge of the NEXT waveform coinciding with the end of the clock pulse rise edge. Also of note is that there is a slight delay with the NEXT signal as opposed to the FEXT signal. In the traditional case of two straight coupled transmission lines, there will be a time delay from when the NEXT signal appears to when the FEXT signal appears, as FEXT must first travel the length of the victim net transmission line. Because the coupling region of the prototype PCBs begins at 1100 mil from port 1, which is 100 mil further than halfway down the line from the input port, the two crosstalk signals are arriving at almost the same time.

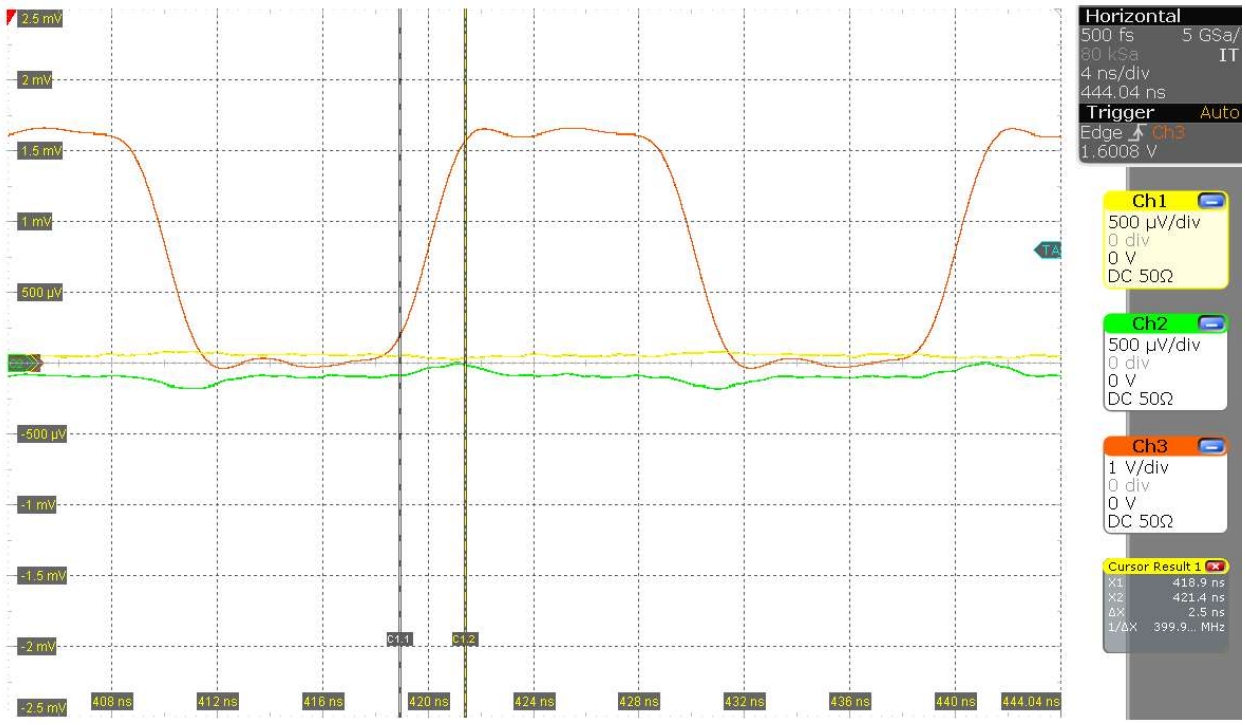

Figure 5.5. GCPW NEXT measured at port 4 (Ch 2, 0.5mV/div), FEXT measured at port 5 (Ch1, 0.5mV/div) and input clock pulse (Ch 3, 1V/div)

The GCPW crosstalk measurements in Figure 5.5 display a much greater ability to mitigate both near-end and far-end crosstalk. NEXT measures approximately 100μV in amplitude, while FEXT is not present in any quantifiable value. This is notable, as FEXT is dependent on the far-end coupling coefficient K_f, defined by

$$K_f = \frac{1}{2v_p}\left(\frac{C_{mL}}{C_L} - \frac{L_{mL}}{L_L}\right) \tag{5.1}$$

where C_{mL} is the mutual capacitance per length, C_L is capacitance per length of the signal trace, L_{mL} is the mutual inductance per length, and L_L is the inductance per length of the signal trace [1]. This is relevant because, in a homogeneous, uniform medium, such as that found in a stripline or embedded microstrip, the effective dielectric constant (ε_{eff}) is independent of any voltage pattern due to the equal values of even-and-odd mode signals. Because of this, $\frac{C_{mL}}{C_L}$ and $\frac{L_{mL}}{L_L}$ are equal, meaning that the far-end coupling coefficient is zero, resulting in no FEXT, and would behave similarly to the GCPW in Figure 5.5. It is unrealistic to expect this behavior at higher frequencies, however, as the GCPW PCB is not homogenous; therefore, further testing with more advanced equipment will be needed to determine at precisely what frequency the GCPW becomes susceptible to harmful levels of crosstalk.

Chapter 6. FINDINGS AND CONCLUSIONS

Measurement	Parameter	Microstrip	GCPW
Signal Integrity	Magnitude Deviation |Port 3 – Port 2|	0.2 dB to 1.8 dB (0.5 to 6 GHz) Max: 1.8 dB	< 0.05 dB (0 to 2 GHz) < 0.6 dB (2 to 6 GHz) Max: 0.55dB
	Phase Mismatch |Port 3 – Port 2|	> 10° from 0.5 to 5.8 GHz Max: 38.1° (2.7 GHz)	> 10° at 3.9GHz, 4.9GHz, 5GHz Max: 12.9° (3.9 GHz)
	Clock Skew	> 0.1T Threshold from 1 to 6 GHz Max: 0.76ns Time domain skew at 1 GHz	< 0.1T Threshold from 0 to 3.5 GHz Max: 0.31ns No time domain skew
Crosstalk	FEXT Freq. Domain	Avg: -65 dB Max: -52 dB	Avg: -75 dB Max: -57 dB
	NEXT Freq. Domain	Avg: -60 dB Max: -54 dB	Avg: -70 dB Max: -59 dB
	FEXT Time Domain (50MHz)	0.6 mVp-p	N/A
	NEXT Time Domain (50MHz)	1.4 mVp-p	0.3 mVp-p

Table 1. Findings from Signal Integrity and Crosstalk Measurements

A GCPW circuit, when properly designed on a low-loss, isotropic dielectric substrate, will outperform a microstrip circuit of the same relative parameters in maintaining signal integrity and reducing crosstalk. The experiments in this report focused on two prototype PCBs of the same general geometric layout on a low loss isotropic laminate. They were designed to

compare the performance of a microstrip structure with that of a GCPW in their ability to transmit and equally split a high-frequency clock signal. This signal would propagate through a resistive divider and travel down two adjacent and geometrically different transmission lines of equal length. The PCBs were then evaluated on their ability to maintain signal integrity by minimizing clock skew at the output ports, as well as crosstalk to an adjacent transmission line.

Upon initial measurements of the straight transmission lines present on both prototype PCBs, input port S-parameter results displayed similar trends, but resulted in some frequency response ripple between across the spectrum. After converting these S-Parameters to a time-domain representation of the impulse response and applying a smoothing filter to the measured data after 4 nanoseconds, it was determined that the ripple of the frequency domain S-parameters is likely due to very small reflection coefficients occurring over long distances and can therefore be discounted. When designing the 1x2 resistive splitter, two resistor configurations were considered and tested. The first configuration was a set of three 16.7Ω SMD resistors which are widely used and inexpensive. They were measured against the second configuration, which consisted of three sets of three 50Ω high-frequency resistors, which were stacked and soldered in parallel to meet the required resistance. After measuring the magnitude of the impedance of both configurations and comparing on the asymptotic bode plot in Figure 2.20, it was concluded that both show nearly identical behavior and are only truly resistive up to approximately 1.7GHz. Further testing and experimentation will be needed to optimize this portion of the design for higher frequencies.

Frequency domain measurements and simulations examining the output phase of S-parameters prove that, while higher in loss, the GCPW clock distribution circuit reduces clock skew across the entire measured bandwidth by as much as 45 nanoseconds. It also maintains a

higher degree of matched behavior between all three ports, making it more effective at distributing input power. The significance of this while propagating down a meandering serpentine signal trace is important because, at high frequencies, tight curves and traces in close proximity can distort signals and increase loss. This is why, while the GCPW is naturally more lossy than microstrip, much of the loss is negated by the ability of a GCPW to tightly contain electromagnetic fields within the gaps adjacent to the center conductor. When examining the time domain response of the two prototype PCBs, some visible skew and attenuation is present on the microstrip circuit even at the relatively low frequency of 50 MHz. This is indicative of significant issues maintaining good SI at higher frequencies. The GCPW, however, shows no sign of clock skew or attenuation.

Intranet crosstalk on the GCPW PCB, when observed in the frequency domain, measures consistently lower, over all measured frequencies, than on the microstrip, with as much as 20 dB of separation. This result is so consistent it can be concluded that special shielding or increased separation between nets would be required to reduce crosstalk on the microstrip PCB to levels seen on the GCPW. When observed in the time domain, there is a significant level of measurable crosstalk on the microstrip PCB, both at the near end (1.4 mVp-p) and the far end (0.3 mVp-p), even at 50 MHz. Because the NEXT signal on the microstrip PCB reaches such a significant amplitude without full saturation, it is safe to predict that, given a larger coupling region or a shorter rise time, NEXT will reach a higher amplitude. When the same signal is propagated through the GCPW, NEXT is present, but in significantly less magnitude than the microstrip PCB, and FEXT on the GCPW is nonexistent. This is conclusive evidence that a GCPW structure excels at mitigating electromagnetic field coupling effects that can seriously hamper a PCBs ability to maintain SI.

From the findings present in this thesis, it can be definitively concluded that GCPW structures are superior at maintaining SI in high performance digital clock distribution circuits. Future investigative efforts should show that, while both circuits can be optimized to improve performance at higher frequencies, the GCPW will consistently outperform the microstrip as clock rates continue to increase.

BIBLIOGRAPHY

[1] E. Bogatin, Signal and Power Integrity Simplified, 3rd edition, Prentice-Hall, 2018.

[2] C.R. Paul, Introduction to Electromagnetic Compatibility, 2nd edition, John Wiley & Sons, 2006.

[3] H. Johnson and M. Graham, High-Speed Signal Propagation, Prentice-Hall, 2003.

[4] Microwaves101 | Transmission Lines

[5] Dr. George E., Ponchak. "Finite Ground Coplanar (FGC) Waveguide: Characteristics and Advantages Evaluated for Radiofrequency and Wireless Communication Circuits." NASA Technical Reports Servers, 1999.

[6] Microwaves101 | Couplers and Splitters

[7] AWR | TXLine Calculator | Cadence

[8] https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-electronics-solutions/english/data-sheets/ro4000-laminates-ro4003c-and-ro4350b---data-sheet.pdf

[9] Microwaves101 | S-parameters

[10] D. M. Pozar, Microwave Engineering, 4th edition, John Wiley & Sons, 2012.

[11] pyu-rt_1-to-0.01_rohs_l.pdf (Yageo 16.7Ω 0603 resistor datasheet)

[12] fcseries.pdf (Vishay Dale 50Ω 0603 RF resistor datasheet)

[13] Wolff, Ingo. Coplanar Microwave Integrated Circuits, John Wiley & Sons, 2006.

[14] Microwaves101 | Basic network theory

[15] Mustafa, K. (n.d.). Defining Skew, Propagation-Delay, Phase Offset (Phase Error) [Review of *Defining Skew, Propagation-Delay, Phase Offset (Phase Error)*]. In *TI.com* (p. 7). Texas Instruments. https://www.ti.com/lit/an/scaa055/scaa055.pdf

[16] Microwaves101 | Group Delay

[17] Cumins, N. (2024, Aug 8). *Intel Processors Over the Years*. Business News Daily; businessnewsdaily.com. https://www.businessnewsdaily.com/10817-slideshow-intel-processors-over-the-years.html

[18] Young, H. D., & Freedman, R. A. (2015). *University physics with modern physics.* Addison-Wesley.

[19] PCB Design Software & Tools | Altium

[20] Zhu, X., Zhou, Y., & Zhou, J. (2024). Wafer Level 3D-stacked Integration Technology with Coplanar Hot via MMIC for mm-Wave Low-profile Applications. *Progress in Electromagnetics Research Letters*, *117*, 27–32. https://doi.org/10.2528/pierl23113002

[21] T. K. Johansen, R. Hersent, V. Nodjiadjim, M. Riet, C. Mismer and B. Ardouin, "A Compensated Finite-Ground Elevated Coplanar Waveguide Interconnect Strategy for InP Based Integrated Circuits Above 100 GHz," *2024 19th European Microwave Integrated Circuits Conference (EuMIC)*, Paris, France, 2024, pp. 98-101

[22] Murmansky, M. S., Kuzmin, N. O., & Zabolotsky, A. M. (2024). Impact of Routing on EMI Resilience in High-Speed Digital PCBs: A Time-Domain Analysis. *2021 International Ural Conference on Electrical Power Engineering (UralCon)*, 735–739. https://doi.org/10.1109/uralcon62137.2024.10718974