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Highly Integrated CMOS Interface Circuits for SiPM Based PET Imaging Systems

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Abstract

**Highly Integrated CMOS Interface Electronics
For SiPM based PET Imaging Systems**

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Recent developments in the area of Positron Emission Tomography (PET) detectors using Silicon Photomultipliers (SiPMs) have demonstrated the feasibility of higher resolution PET scanners due to a significant reduction in the detector form factor. However, reduced size implies a corresponding increase in the detector density, resulting in a proportional rise in the number of channels interfacing a SiPM array with the digital backend. This thesis explores a row-column-diagonal decoding architecture to simplify and reduce the required channels between the individual elements in the SiPM array, and the backend digital electronics. The front-end interface is designed using a current amplifier with a very low input impedance. Accumulation of noise presents itself as a challenge to the row-column summation architecture. This may lead to an increased chance of false triggering as compared to a more traditional approach using dedicated single-channel readout for each individual SiPM device. This work uses a current comparator topology to act as a thresholding circuit to minimize the accumulation of ‘dark noise’ and reduce the possibility of a

false triggering event. A separate high-speed timing channel is designed to acquire the timing information across all the channels. Line drivers are used to interface this chip to a wide variety of impedances, allowing a general purpose interface to the digital backend. The proposed readout electronics has been realized in STMicroelectronics 130 nm CMOS process.

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1. Introduction

Physics has revolutionized virtually all aspects of human society from mechanics to life sciences. One of its most rewarding applications has been that of Medical Physics in the form of various Imaging Technologies. It started with the discovery of X-rays in 1895 by Wilhelm Rontgen, a German professor of physics. He discovered that the radiation from the X-rays is absorbed differently by different tissues in the body, depending on their density and composition. This very property is used to map the different tissue densities within the body on a photographic film. Then came the use of pharmaceutical contrast agents between 1906 and 1912. Administered orally or using vascular injection, they were the first one to help visualize blood vessels, digestive and gastro-intestinal systems, bile ducts and gall bladder. This paved the way for angiography by the 1960's. In angiography, a radio-opaque contrast agent injected into the blood vessel is used to visualize the inside of blood vessels and organs of the body, with specific interest in arteries, veins and the heart chambers.

The advent of Nuclear Physics in medical imaging was made possible in the early 1950s when Geiger Muller counters were used to measure counting rates from iodine-131 in the thyroid gland from point to point over the neck. As years went by, nuclear physicists made considerable improvements with inventions like gamma camera [1] and emission tomography system. The early part of 1950's also saw the rise of Positron Emission Tomography (PET), thanks to the work of Gordon Brownell, Charles Burnham and their associates at the Massachusetts General Hospital [2]. Later on, pioneering work by Michel Ter-Pogossian at the Washington University of St. Louis revolutionized the field of PET [3]. In the 1960's, the principals of sonar in the form of ultrasound were applied to the field

of diagnostic imaging. Since then, it has become a very popular imaging technique due to the lack of any adverse bio-effects. Computed Tomography (CT) scan, introduced in the 1970's, uses computer processed X-rays to produce tomographic slices of specific areas of the body, letting us gain a better insight into the pathogenesis of the body. The motivation behind Magnetic Resonance Imaging (MRI) was the discovery of the fact that the magnetic relaxation times of tissues and tumors differed, and this was shown by Raymond Damadian in 1971. The next 20 years saw vast improvements in the field of MRI due to the contributions of different scientists. Radio waves stronger than the magnetic field of the earth are used to form a strong magnetic field around the area to be imaged. This causes the alignment of protons (hydrogen atoms) in tissues containing water molecules. The excited protons emit a radio frequency signal which is picked up the scanner and transformed into an image by the computer.

PET and SPECT are radioactive tracer imaging techniques. A radioactive tracer compound is a chemical compound in which one or more atoms have been replaced by radioisotope, in this case by positron-emitting radionuclides. When injected into the human body, these tracer compounds can then be used to track the mechanism of various biochemical and physiological processes in vivo by virtue of their radioactive decay. The system detects the pair of gamma rays emitted as a result of this decay, and 3D images of tracer concentration within the body are then created by image reconstruction algorithms.

Our ASIC development is primarily targeted for use in PET scanners. Existence of positron-emitting isotopes of elements such as carbon, nitrogen, oxygen and fluorine makes PET detection an important tool in medical research and practice, because these compounds can be processed to create tracer compounds similar to naturally occurring

substances in the body. Some of the most common radiotracer compounds used clinically are carbon-11 (^{11}C), nitrogen-13 (^{13}N), oxygen-15 (^{15}O) and fluorine-18 (^{18}F). They have been used to identify and diagnose cancers, epilepsy and other movement disorders, and heart and cardiovascular problems.

A PET scanner consists of three main systems: the photodetectors, the data acquisition (DAQ) and pulse processing electronics, followed by the image reconstruction systems in the back-end. This thesis will concentrate on the data acquisition portion of the scanner, specifically the front end readout electronics. The scope of the DAQ system depends on the application, but in general, it starts from front end electronics which receive the signals from the detector modules and ends with the data transmission network circuits which are used to send the processed data from the photon events, to the image reconstruction PC. The front end electronics need to properly acquire the signals from all the channels, where the number of channels can be on the order of few hundreds or thousands. Without multiplexing, the number of channels interfaced to the back end Analog-to-Digital Converters (ADCs) would increase, and the power dissipation would scale accordingly. There are examples of existing multiplexing schemes in the optical [4-5] and electrical domains [6-13]. Most of the works in the electrical domain are based on discrete board level implementations, even though the emerging solid state photodetector technologies are based on CMOS technologies. Therefore, the research paradigm for DAQ systems has shifted towards CMOS implementations because there is a potential for the integration of the data acquisition and pulse processing electronics on the same substrate as the detector modules [14-19]. The focus of this thesis is to implement a multiplexing scheme using CMOS circuits. It is organized as follows:

Chapter 2: Positron Emission Tomography introduces the main building blocks of PET imaging systems including the tracer chemistry, the scanner hardware including the detector modules and the DAQ, the back end image reconstruction algorithms and the uses of PET.

Chapter 3: System Design covers the impact of analog non-idealities associated with front end electronics on PET imaging systems and the motivation behind the architecture used in this implementation.

Chapter 4: Circuit Design discusses the circuit level implementation of different blocks in the system, as well as of the interfacing of the blocks on the system level.

Chapter 5: Measurements presents the test results of the chip in various test setups.

Chapter 6: Conclusions and Future Work summarizes the contributions of the thesis and some possible future works.

2. Positron Emission Topography

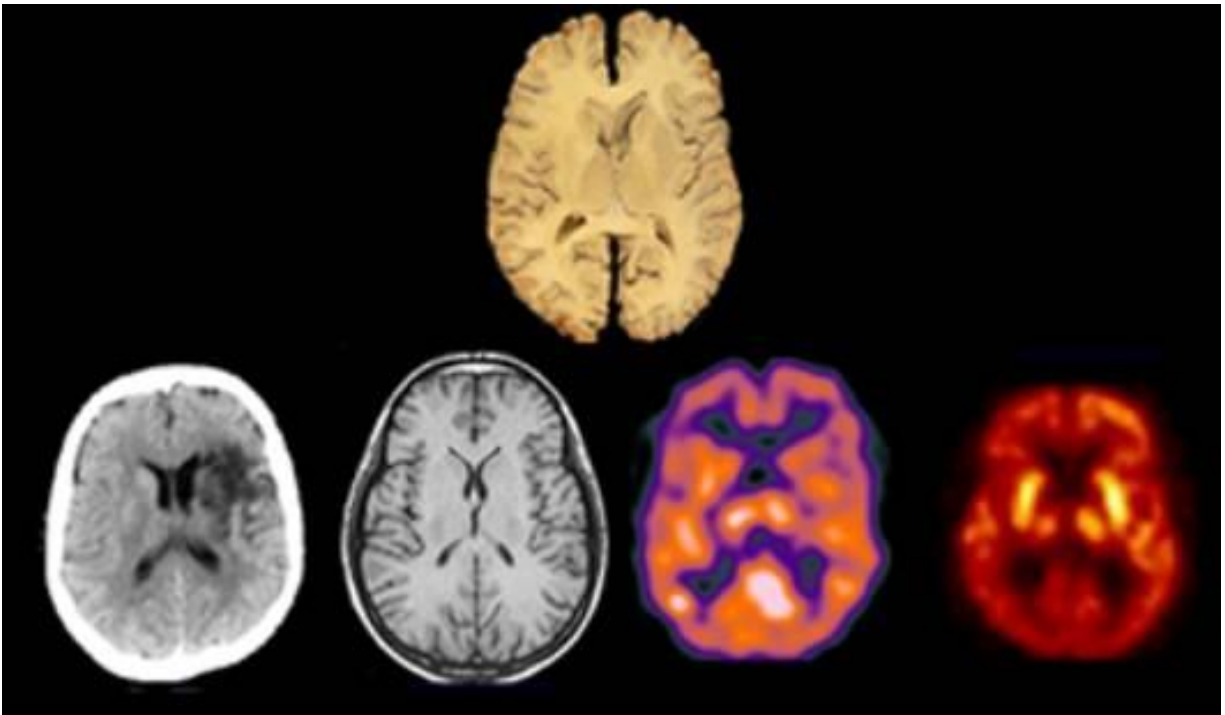


Fig. 1: Transaxial slice of the human brain (top) acquired with different imaging modalities (bottom) from left to right: X-ray CT, MRI, SPECT and PET [20]

Medical imaging techniques can be broadly classified into two different categories – structural and bio-chemical. Ultrasound, X-rays, CT (Computed Tomography) and MRI (Magnetic Resonance Imaging) belong to the first kind, as they produce image of the body anatomy. Biochemical imaging modalities, on the other hand, map the different chemical processes inside the body, like blood flow and metabolism. Positron emission tomography (PET) and single-photon emission computed tomography (SPECT) are well-established examples of biochemical imaging modalities, which provide physicians with information about the body's chemistry not available through any other procedure. Figure 1 shows a transaxial slice through the human brain (top row)

acquired with X-Ray CT, MRI, SPECT and PET (bottom row) giving different information about the brain function and anatomy.

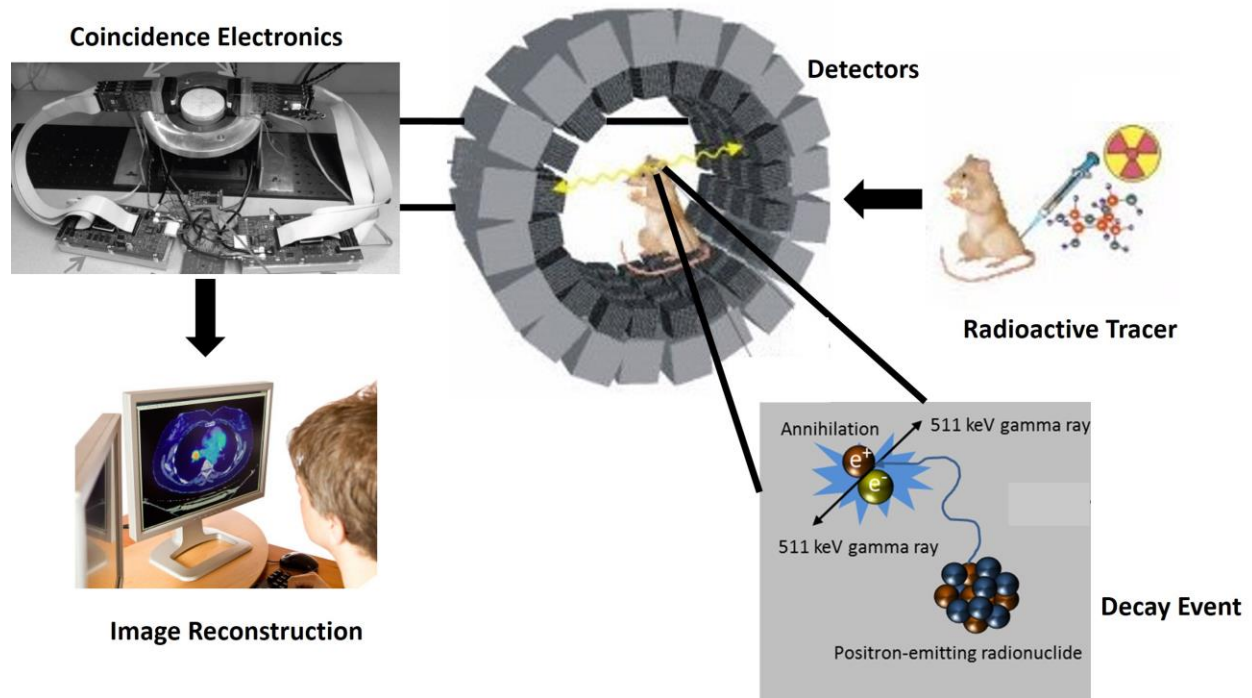


Fig. 2: PET Scanner Ring and the associated electronics [21]

The main components of the PET imaging system have been shown in Figure 2. The first step is to generate and administer the radioactive tracer, composed of a radioactive isotope and a metabolically active molecule. These tracers are injected into the body of the patient to be scanned. After enough time has elapsed for the tracer to distribute and concentrate in certain tissues, the subject is placed inside the scanner. The radioactive decay events for tracers used in PET studies give off two 511KeV antiparallel photons. The scanner hardware is designed to efficiently and accurately capture these photons. The scanner, the second component of PET, consists of a ring of sensors attached to electronics. The sensors are made up of scintillator crystals attached to a

photodetector. The scintillator converts the 511KeV photon into many visible light photons, while the photodetector generates an electrical pulse in response to the burst of visible light. These pulses are processed by the front-end digital acquisition electronics to determine the parameters of each pulse (i.e. energy, timing). Finally, the data is sent to a host computer that performs the tomography to turn the data into a 3-D image.

2.1 Radiopharmaceutical

Before the start of the actual PET scan, the first step is to synthesize the radiopharmaceutical (or tracer). This is done by replacing one or more atoms of a metabolically active molecule by the radioisotope. To conduct the scan, the tracer is injected into the body of the subject. In most applications, imaging is begun after the radiopharmaceutical has distributed in the tissues, but for some applications, imaging begins with injection so that the dynamics of tissue uptake can be measured. Most of the radioisotopes have a short half-life, thereby ensuring large portion of the decay will occur during the scanning period. This helps to gather maximum information for a given dose of radiation. However, due to the short half-lives of most positron-emitting radioisotopes, the radiotracer has to be produced in close proximity to the PET imaging facility. At present, the most commonly used radiotracer in clinical PET scanning is fluorodeoxyglucose (also called FDG or fludeoxyglucose), an analogue of glucose that is labeled with fluorine-18. This makes up a large majority of radiotracer (>95%) used in clinical PET and PET/CT scanning, with extensive uses in oncology as well as neurology.

2.2 Decay Event

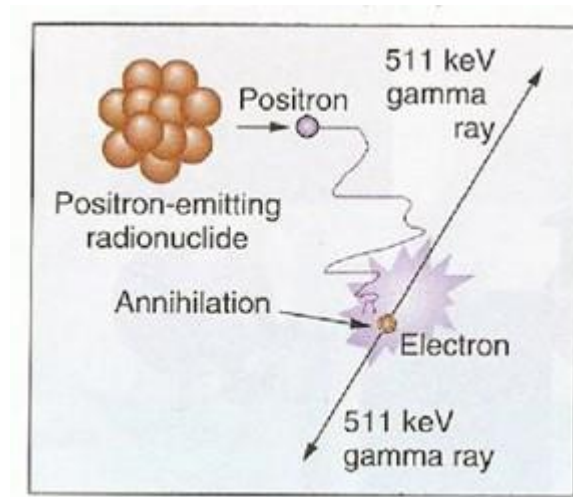


Fig. 3: Basic Physics of Positron Emission Tomography [22]

After being absorbed by the tissue of interest, the radioisotope inside the tracer undergoes positron emission decay. A positron is an antiparticle of the electron with opposite charge. As shown in Figure 3, the emitted positron travels in tissue for a short distance (typically less than 1 mm, depending on the isotope), and then interacts with an electron. The encounter leads to the annihilation of both the positron and the electron, producing a pair of 511 KeV gamma photons, which travel away at an angle of 180° with one another. This makes it possible to localize their source along a straight line of coincidence (also called the line of response, or LOR). The coincidence events are then detected from these simultaneously emitted photons. In practice, the LOR has a finite width as the emitted photons are not exactly 180 degrees apart.

2.3 Photon Scintillation

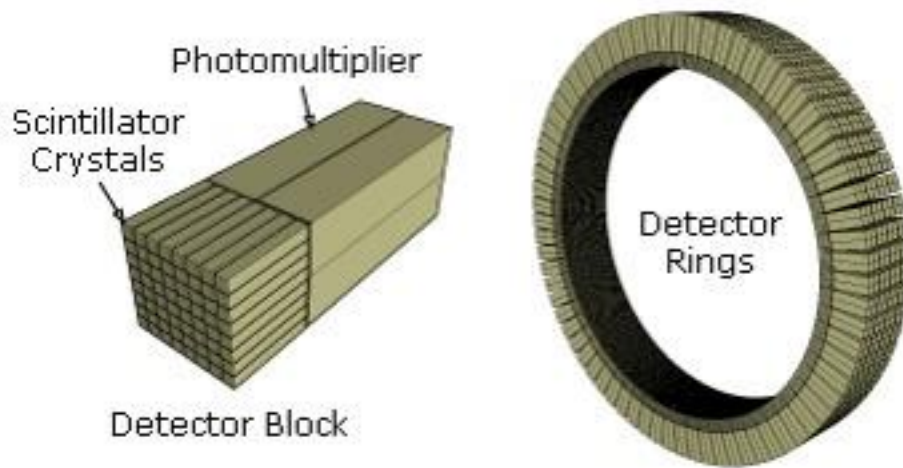


Fig. 4: Detector Rings Arrangement [2]

The amount of energy possessed by a 511KeV makes it easy for it to pass through many materials, including body tissue. Though it helps in observing the photon outside the body, but still it has to be stopped before the actual detection can take place. This is the job of the scintillator. A typical arrangement of detector rings is shown in Figure 4. The scintillation process is the transformation of high-energy photons into visible light through interaction with a scintillating material, and consists of the following steps [23]:

- 1) A photon incident on the scintillator creates an energetic electron, either by Compton scatter [24] or by photoelectric absorption.
- 2) As the electron passes through the scintillator, it loses energy and excites other electrons in the process.
- 3) These excited electrons decay back to their ground state, giving off light as in the process.

Scintillators can have different density, wavelength of maximum emission and timing characteristics depending on the materials they are composed of, including plastics, organic crystals, inorganic crystals and organic liquids. One common scintillator crystal used in modern scanners is $\text{Lu}_2\text{SiO}_5(\text{Ce})$, or LSO, which is an organic crystal.

2.4 Photodetectors

The visible light photons need to be converted to electronic pulses, in order to be processed. This is the job of the photodetectors, which follow the scintillators in the system. In the past, most of the photodetectors were photomultiplier tubes (PMT), which consist of a vacuum tube with a photocathode, several dynodes (series of electrodes within the PMT), and an anode that has high gains to allow very low levels of light to be detected. The emerging photodetector technologies, based on solid-state detectors, are considered the most promising candidates to replace the PMT because of their features – high quantum efficiency, high gain, operation at low bias voltages, and insensitivity to magnetic fields, excellent time resolution, robustness and compactness. In addition to their operating features, the ability to fabricate them with CMOS technology has created potential for the integration of the data acquisition and pulse processing electronics on the same substrate [25-26]. This helps to eliminate issues related to parasitic capacitance associated with interconnect and the large addition of noise from unwanted board-level signals coupling into the supply and/or bias circuitry. Solid state detectors are known by different names, like single photon avalanche diodes (SPADs), silicon photomultipliers (SiPMs) or multi-pixel photon counters (MPPC), but they are based on the same technology. They are reverse biased p-n junction diodes, with the bias voltage higher than the breakdown voltage. As a result, the electric field developed in the depletion region is higher than 3×10^5 V/cm. In this bias condition, a single carrier injected

into the depletion region can trigger a self-sustaining avalanche. This mode of operation is known as Geiger-mode Avalanche (GM), differentiating it from normal avalanche mode where the bias voltage is less than the breakdown voltage of the semiconductor. In PET detection systems, the incident photon initiates the avalanche breakdown. In the SiPM, each diode is segmented into tiny micro-cells (each working in GM) connected in parallel to a single output, as shown in the Figure 5(a) [27]. When activated by an incident photon, the current response is similar for all the microcells, making the output signal proportional to the number of cells hit by a photon. The number of micro-cells limits the dynamic range of the SiPM. Also, depending on the size of the micro-cell, 2 or more photons can hit the same microcell, reducing the dynamic range further.

There are mainly two equivalent circuits for the SiPM available in literature. The difference between the two circuits is the way the firing micro-cells are represented. Corsi et al. [28] employ a current source, while Seifert et al. [29] and Claudio Piemonte [27] modeled the avalanche following a breakdown event using a voltage source, V_{br} , in series with a resistor, R_S , and a switch, Sw , as shown in Figure 5(b). Here V_{br} is the breakdown voltage and V_{bias} is the operating voltage. Initially the diode capacitance, C_D , is charged to $V_{bias} > V_{br}$ through the quenching resistance R_Q . When an avalanche discharge is initiated due to the incoming photon, the switch is closed, C_D discharges to V_{br} through the resistor, R_S . As the voltage on C_D decreases, the current flowing in the quenching resistor, R_Q , tends to the asymptotic value of $(V_{bias} - V_{br})/(R_Q + R_S)$. R_Q being of the order of few hundreds of $k\Omega$, this diode current is so low that a statistical fluctuation brings the instantaneous number of carriers flowing through the high-field region to zero, quenching the avalanche. The switch is again open and the circuit is in its initial configuration. The diode capacitance gets recharged back to V_{bias} , so that the diode is ready to detect the arrival of a new photon. The table below shows the values for the different elements in

the model for a Hamamatsu SiPM device [29]. A common arrangement of SiPM is an 8x8 array of about 3 mm x 3 mm cells. Each cell has a density of about 10^3 diodes per mm^2 .

	MPPC-S10362-11-25u- Hamamatsu[2] N= 1600
V_{br}(V)	68.8±1.5
C_D (fF)	15.0±1.2
C_q (fF)	4.3±1.2
R_q (kΩ)	179±1
C_g (fF)	7.5±1.9
R_D (kΩ)	1

The equivalent circuit simulating the discharge of N_f cells in a SiPM which consists of a total number of N_{tot} microcells is illustrated in the Figure 6. [27]. The dashed lines separate the circuit into an active part (left), representing a number of N_f fired microcells in parallel; a passive component (middle), representing the remaining $N_p = N_{tot} - N_f$ unfired microcells; and a parasitic capacitance C_g (right), which equals the sum of the parasitic capacitances of the N_{tot} cells connected in parallel. The resistor and capacitor values in the active and passive part of the circuit are given by,

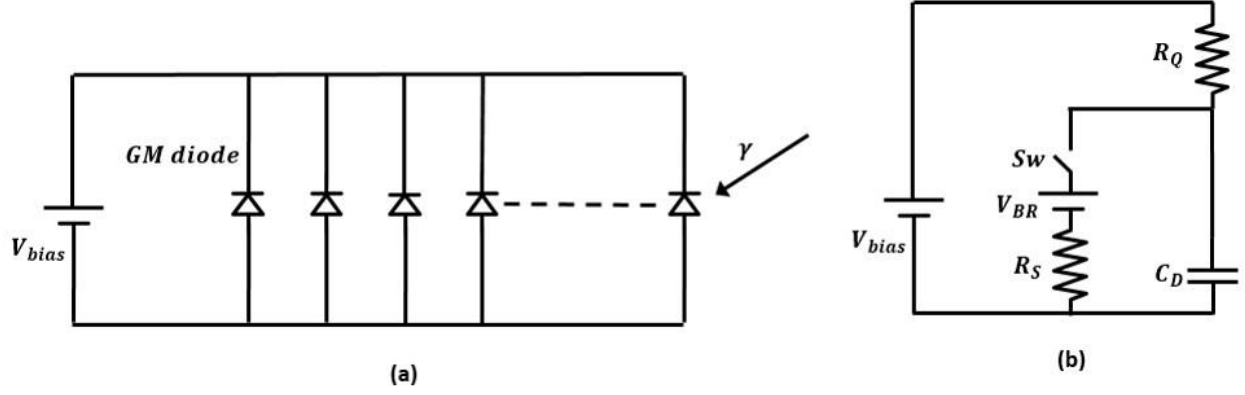


Fig. 5: Equivalent Circuits of (a) a single SiPM and of (b) a single GM-APD [27]

$$C_{D,N_f} = C_D \cdot N_f, \quad R_{q,N_f} = \frac{R_q}{N_f}, \quad C_{q,N_f} = C_q \cdot N_f,$$

$$C_{D,N_p} = C_D \cdot N_p, \quad R_{q,N_p} = \frac{R_q}{N_p}, \quad C_{q,N_p} = C_q \cdot N_p, \quad R_{q,N_f} = \frac{R_q}{N_f},$$

Where the capacitance of the reverse-biased diode is C_D , R_D is the series resistance of the microplasma in the avalanche, R_q is the quench resistor and C_q is its associated stray capacitance, all for an individual microcell.

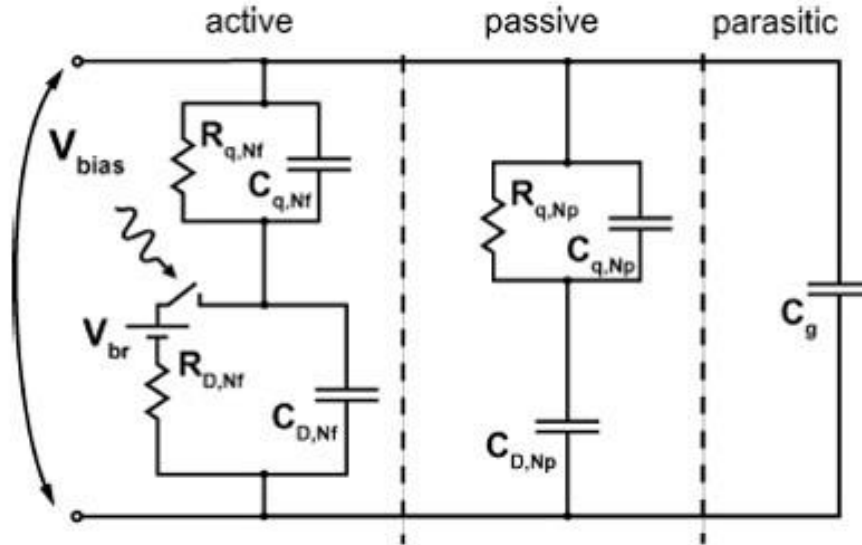


Fig. 6: Equivalent circuit for the discharge of N_f microcells in a SiPM [29]

2.5 Data Acquisition System

Most of the information needed to create a PET image is contained in the photodetector pulses, such as the spatial information (location) of the photon event and the time of interaction with the scanner. The next step is the processing of the pulses to extract this information. This is done with the data-acquisition system (DAQ). The roles of a DAQ system in PET are (1) to collect single photon events, (2) to identify coincidence events, and (3) to send the coincidence events to the image reconstruction PC. As explained before, coincidence events are detected when there are simultaneously photons emitted. The coincidence events are identified using a parameter called the coincidence timing window. The choice of the timing window depends on the timing resolution of the system and the reduction of random coincidences.

The design of the data paths of a DAQ system can be categorized into four parts - multiplexing, event generation, DAQ board interconnection to detect coincidences, and transmission to image reconstruction PC. For a PET imaging modality, the number of channels

required varies depending on the application. For example, 400-600 channels are present in a small animal PET system, while that for a brain PET is ~4500[30]. Specifically, the reduced size of the SiPM devices compared to PMTs implies an increase in the detector density, resulting in a proportional rise in the number of read out channels which interface to the digital backend. With the advent of 3D positioning architectures, X, Y, and Z components of an event can be captured, improving both spatial and image resolution. However, 3D positioning architectures lead to further increase in the array density, and hence the number of read channels also grows proportionally, requiring significantly more amplifiers and Analog-to-Digital Converters. With such a large number of channels, multiplexing is necessary to significantly reduce the number of connectors between the front end electronics and the backend DAQ boards, and also reduce the number of DAQ boards required. But, multiplexing can lead to degradation of energy resolution as well as timing resolution. The energy resolution can be degraded if the noise added in the multiplexing circuit is similar or larger than the original scintillation crystal. Pulse pile-up can also be an issue with large multiplexing ratios as more signals get merged together. All of these factors should be considered together before designing a multiplexing circuit. There are examples of existing multiplexing schemes in both optical and electrical domains- light sharing Anger logic[4] (optical), cross-strip[5] (optical), position encoding/decoding scheme[10-11] (electrical) and compressed sensing scheme [12-13] (electrical). In this work, a row-column summing architecture (RCA) has been used in the front end readout electronics to reduce the number of readout channels for highly dense SiPM arrays. This approach is analogous to decoding methods used in digital memory systems. This effectively reduces the number of channels from N^2 to $2N$, for an N by N SiPM array. The row and column channels convey information about the position of a detected event. In addition, a single high-speed channel is used to extract timing information for all elements in the

SiPM array. This reduces the number of high-speed ADCs from N^2 to a single channel which captures the timing information.

The signals from the front end electronics are a stream of analog signals. After digitization in the back end ADC, the DAQ system is responsible for identifying a single event and extracting the timing and energy information of the event. Once the information of the event is acquired, it is stored in the form of an event packet and can be sent to other DAQ boards or stored into a local memory. The next step is identification of the coincidence events from the event packets generated from all the DAQ boards. The last data path in the DAQ design is the network connection to the image reconstruction PC. The network speed of the connection should be high enough to ensure no data loss. The required speed will be minimized if the DAQ system does all of the data processing. A possible alternative to replace the network connection is to provide a low power high frequency radio to provide bi-directional control and transfer between the DAQ and the image reconstruction PC. A separate radio will be needed on the image reconstruction PC to act as a receiver for this channel.

2.6 Image Reconstruction

Image reconstruction begins after the collection of all the coincidence events in the host computer. Each coincidence event represents the line of response (LOR) for a particular positron emission event. Most commonly, coincidence events are grouped into projection images, depending on the angle of each view and tilt (for 3D images). These projection images are known as sinograms. Back projection algorithms are then used to reconstruct images from these projections. But before that, in filtered backprojection, pre-processing of the data is required-

correction for random coincidences, estimation and subtraction of scattered photons, detector dead-time correction and detector-sensitivity correction. On the other hand, if iterative reconstruction technique is used, then all those corrections are often done with the reconstruction iterations. An example of a PET scan image is shown in the Figure 7. As the computing power of PCs is improving rapidly with the help of multi-core CPU and GPU processor technologies, some of the DAQ event processing can be off-loaded or post-processed in the image reconstruction PC. In the PC, events can be processed with more flexibility with high computing power and large memory size. In order to post-process events at the PC, more information needs to be transmitted to the PC.

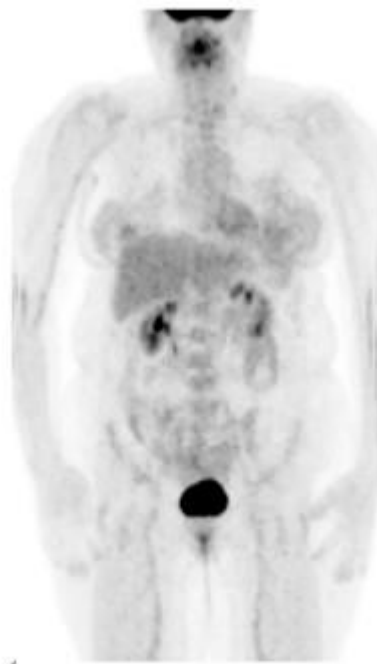


Fig. 7: Whole body PET scan image using [F-18] FDG, with notable spots for glucose utilization highlighted (the abdomen, the bladder near the bottom of the image and the brain)[31].

2.7 Some examples of the uses of PET

Oncology – Fluorine-18 (F-18) fluorodeoxyglucose (FDG) is a radioactive tracer analogous to glucose. As a result, it is taken up by glucose-using cells and trapped there, until it decays. In clinical oncology, PET scanning with FDG is used in radiolabeling of tissues with high glucose uptake, such as the brain, the liver and most cancers. FDG-PET can be used for the diagnosis and treatment of patients with Hodgkin's lymphoma, non-Hodgkin lymphoma, and lung cancer.

Neuroimaging – Blood flow in different parts of the brain is believed to be correlated with the areas of high radioactivity in the brain. This has been measured using the tracer oxygen-15. However because of its short half-life (2 minutes), it is difficult to use in practical systems. But since the brain pathologies like Alzheimer's disease can reduce the brain metabolism of both glucose and oxygen to a large extent, FDG-PET can be used successfully for early diagnosis of Alzheimer's disease. In addition, it can be used for localization of seizure focus.

3. System Design

SiPM devices have been implemented in CMOS technology in recent years, thus potentially enabling integration of a significant portion of the interface electronics on the same substrate with the detectors, which would reduce interconnect parasitics, and lower power consumption. With respect to readout channels for SiPM detectors in PET applications, a majority of the circuits have been derived from previous discrete or integrated implementations developed for PMTs [32-34]. In contrast, recent efforts have attempted to integrate the readout electronics on a single die with dedicated designs for use with SiPM detectors [35-37]. However, a number of challenges exist for highly integrated front-end detectors. As mentioned in the previous chapter, the miniaturization of detectors due to reduced form factors of SiPM devices has led to a proportional increase in the number of channels interfacing to the backend. In an effort to reduce the number of channels for high-element arrays, multiplexing techniques have been utilized. When multiplexing a large number of elements, there are several key considerations with respect to analog IC impairments. First, the impact of circuit non-linearity on timing and energy resolution needs to be understood. While analog circuits can be approximated by a linear model for small-signal operation, nonlinearities often lead to spectral regrowth and distortion in the time domain that are not predicted by a linear small-signal model. Second, the impact of electronic noise needs to be understood. Electronic noise from thermal, flicker and shot noise often limit the lower end of the dynamic range, thus limiting the minimum detectable signal. Third, channel bandwidth plays a critical role in determining the high-frequency behavior of the interface electronics as often times the sharp rising and falling edge of a SiPM pulse contains high-frequency information useful for timing and energy resolution. Further, the input impedance of the front end electronics together with the impedance of the microcells not undergoing any breakdown will change the loading of

the readout electronics and alter its high frequency response. To date, relatively little modeling has been done to understand the impact of analog non-idealities on SiPM-based PET systems. This chapter explores the impact of analog performance on the mixed-signal interface between SiPM devices and the digital electronics. The objective is to provide sufficient understanding of the effect of analog non-idealities on PET imaging systems, to be used as a part of a design methodology for the interface electronics. As a test bench to evaluate the relationship between analog performance and the overall image quality, the impact of additive Gaussian noise, linearity with respect to harmonic and intermodulation distortion, and channel bandwidth has been modelled using MATLAB simulations. The interface between an 8x8 Silicon Photomultiplier (SiPM) array and the Phase II MiCES FPGA boards [38] is used as a test bench to understand the impact of analog circuit performance on the achievable energy resolution using the commonly accepted metric of Full Width at Half Maximum (FWHM). The MATLAB simulation model for the front end electronics is illustrated in Figure 8. The blocks inside the dashed lines are used to emulate various analog impairments associated with the interface electronics including non-linearity, circuit noise and channel bandwidth. As a starting point, the MATLAB model uses a set of measured SiPM pulses. 2000 SiPM pulses were taken from a Zecotek Photonics MAPD-3N1 using a 511 keV Ge-68 radiation source as an input. Section 3.1 describes the impact of linearity using Intermodulation Intercept Points (IIPs). In section 3.2, additive white Gaussian noise has been used to model the impact of electronic noise on the system. Section 3.3 derives the impact of channel bandwidth on the system performance.

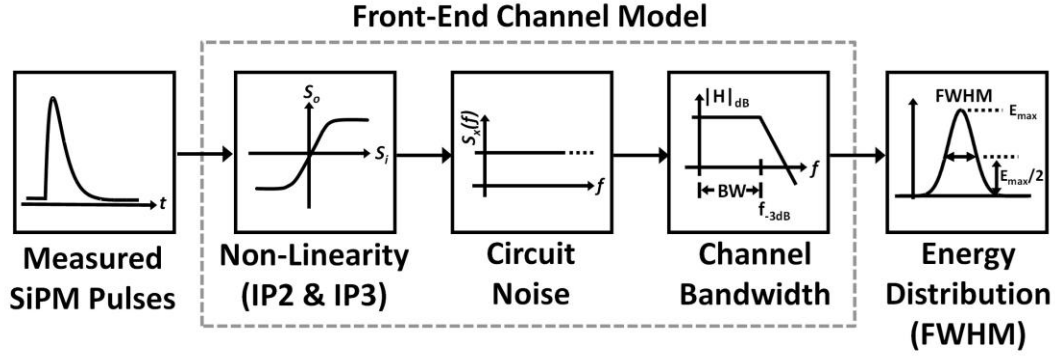


Fig. 8. MATLAB Simulation Model

3.1 Linearity

The nonlinear behavior of a circuit can be viewed as variation of the small-signal gain with the input level. To model the nonlinearities of the channel, the circuit was assumed to be broad banded relative to the desired signal bandwidth. Stated differently, only resistive affects were considered and the circuit is assumed to be memoryless. This allows an approximation of the circuit nonlinearities in the channel using a Taylor Series expansion [39] as follows

$$y(t) = a_1x(t) + a_2x^2(t) + a_3x^3(t) \dots \quad (1)$$

For small x , $y(t) \approx a_1x$ indicating that a_1 is the small-signal gain in the vicinity of $x \approx 0$. The gain of the higher order terms can be related to common metrics of analog linearity performance in terms of the Input 2nd and 3rd order Intermodulation Intercept Point (IP2 and IP3) with the below expressions.

$$a_2 = \frac{a_1}{IIP2} \quad a_3 = \frac{4a_1}{3IIP3}$$

The measured SiPM pulses were then applied to a Matlab model where the amplifier input referred linearity was defined using the above two expressions. The output of the amplifier blocks

was then collected and energy resolution plots were constructed to help determine the FWHM as a function of linearity. The process was repeated with the IP2 and IP3 values swept from -30dBV to 0dBV. Figure 9 shows plots of FWHM as a function of the amplifier IP2 and IP3, respectively. IP3 is seen to have negligible impact on the FWHM of the pulses. In large part, this is intuitively pleasing as the effect of circuit nonlinearities is to generate new spectrum, this is commonly referred to as spectral regrowth in power amplifier used in communication applications.

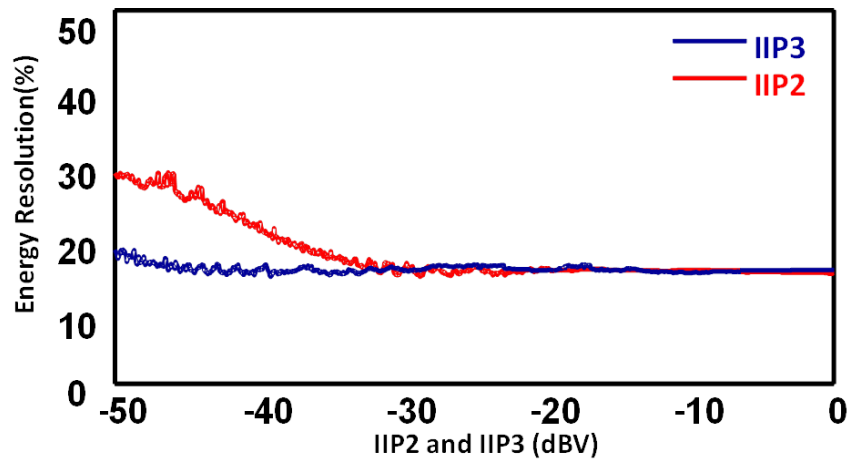


Fig. 9: Energy Resolution vs Input Intercept Point

Although nonlinearities will create new spectrum, the total energy associated with the analog signal is preserved, thus having minimal impact on the FWHM performance of the analog portion of the SiPM channel. This suggests that digitization of signals early in the interface chain is possible in future architectures. However, 2nd order nonlinearities are seen to have an impact on the FWHM. This effect is still under evaluation but believed to be from DC components generated by the 2nd order.

3.2 Noise

Assuming CMOS technologies are used to realize the SiPM interface electronics, there are a number of noise processes which may interfere with a detection pulse including thermal channel noise and flicker noise. Electronic noise corrupts the signal level, thus changing the energy associated with the signal. Another challenge associated with the row-column summation approach used in [40] is the potential accumulation of dark noise produced by each of the detectors connected on a row, column, or diagonal line, in addition to the thermal noise generated by the associated interference electronics. For the purposes of these simulations, additive white Gaussian noise was assumed to be dominant. Scaling the noise floor in Matlab relative to the pulse amplitude was accomplished by estimating the signal power through simulation, then using the Signal-to-Noise Ratio (SNR) as a means to determine the variance of a noise source. Figure 10 shows the energy resolution as a function of the SNR (dB) scaled relative to the magnitude of the SiPM pulses. The energy resolution begins to degrade for SNRs < 5 dB suggesting a relatively modest noise performance required of the front-end electronics.

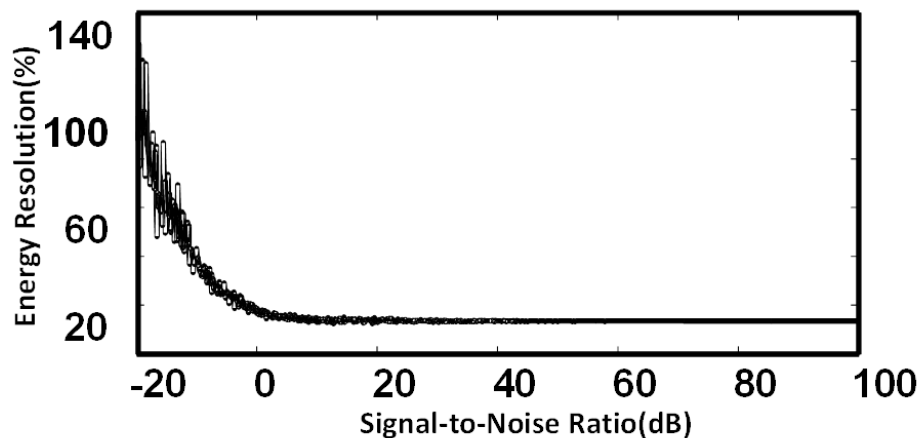


Fig. 10: Energy Resolution vs Signal-to-Noise ratio

3.3 Channel Bandwidth

Although achieving constant open-loop amplifier gain up to several GHz is possible using modern silicon processes, realizing similar bandwidths using closed-loop amplifiers becomes challenging above several hundred MHzs. Moreover, understanding the required signal bandwidth becomes crucial from the perspective of optimizing overall power consumption of the front-end interface channel. The rise time of the SiPM pulses can be as fast as 2 ns. To understand the impact on energy resolution versus channel bandwidth, a 10th order Butterworth filter was used in the Matlab simulation test bench. The channel bandwidth was swept and the impact on the energy resolution was recorded. Figure 11 shows that there is degradation in the energy resolution for cutoff frequency below 20 MHz. Although the bandwidth is relaxed for detecting the energy resolution, higher bandwidths are required to detect the timing information for the proposed ASIC architecture [40]. This is because the anodes of all the SiPM devices in the array are shorted to a common node. This common anode signal is used to derive the time of arrival information for each SiPM pulse. However, it is worth mentioning that only one common timing channel is required for the entire array.

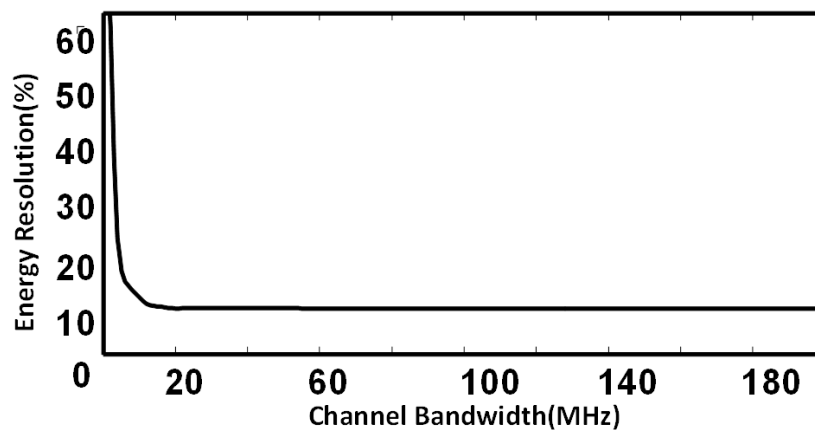


Fig. 11: Energy Resolution vs Channel bandwidth

3.4 Row Column Summing Architecture (RCA)

Conventional readout electronics will dedicate an individual channel for each SiPM device in the array. Each channel consists of a SiPM detector which feeds either a current or transimpedance amplifier, after which the signal is driven off chip into a cable connected between the readout electronics and the ADC at the backend where digital signal processing takes place. For an N by N array, the channels are replicated N^2 times.

In the RCA approach, shown in Figure 12, each SiPM detector output feeds a low-input impedance, programmable gain current amplifier. The amplifier interface is the only component of the readout electronics which is unique to each SiPM detector. The current amplifier has three output stages which feed a row output line, column output line and common pickoff line.

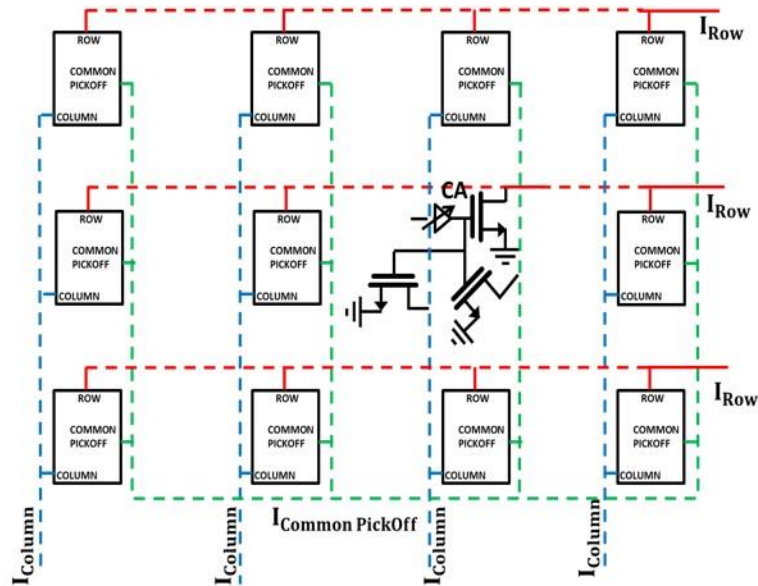


Fig. 12: Row Column Architecture (RCA)

The row and column channels provide spatial information of a detected event. The common pickoff channel, used as the timing channel, sums the output of all the array elements. This allows better timing information with respect to any individual SiPM event in the array, since it reflects

the total current drawn by the array when multiple elements are fired. As all SiPM elements share this channel and the intent is to optimize timing, this particular channel needs significantly higher bandwidth as compared to the individual row and column readout (spatial positioning) channels. If there is a SiPM current at the input of any array element, there will be outputs across the corresponding row and column channels, as well as the common pickoff channel.

Each array element is implemented with a high speed current amplifier interfaced to the off chip SiPM device. The use of current amplifiers is motivated by the need to present low impedance from the perspective of the SiPM output, which reduces the current division between the amplifier input and the remaining SiPM cells. In addition, current mode circuits have significantly higher bandwidth compared to their voltage mode counterparts, thus facilitating wideband implementations. The use of a single amplifier to interface the SiPM device has the additional benefit of reducing cross talk between the SiPM devices in the array. In addition, because a single amplifier (rather than three) is used to supply a row, column, and pickoff signal, the capacitive loading on the SiPM's cathode is minimized, further increasing the bandwidth of the detector-channel interface.

4. Circuit Design

At present, our front-end readout electronics are situated in close proximity to the SiPM array. A differential interface then runs from the output of the front-end amplifiers to the input of a set of ADCs and the subsequent digital signal processing chip. Some of the proposed electronics between SiPM and line driver are shown in Figure 13. A low input impedance, high-output impedance current amplifier interfaces the SiPM device and produces a current which is shared with other SiPM devices along a row, column, or diagonal line. The current amplifier is designed to produce the lowest input impedance possible to improve the bandwidth at the SiPM-Current Amplifier interface. Each amplifier has an additional high-speed current output that supplies a common timing signal.

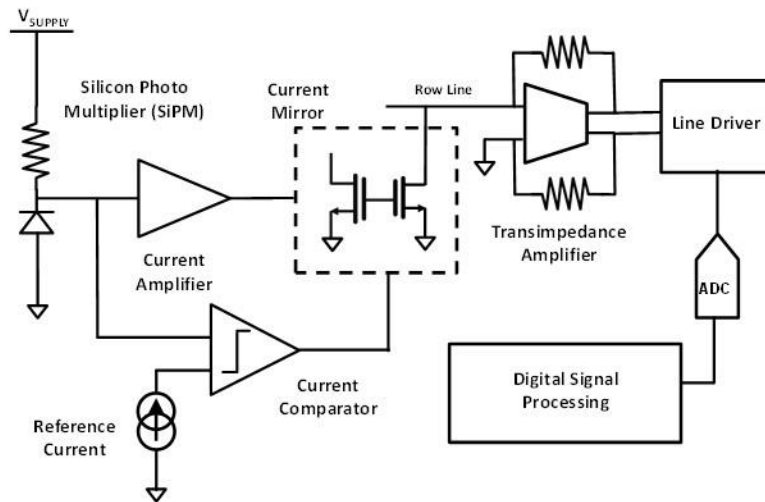


Fig. 13: Channel Architecture

Compared to a single-channel readout of an individual SiPM device, the accumulated noise associated with combining numerous detectors on a single row line, for example, can increase the possibility of detecting a false event. In order to minimize the accumulation of “dark current “ produced by the SiPM devices, a current comparator is used in parallel with the main signal path and either enables or disables the output of the current amplifier. This comparator output goes high, and enables the current amplifier when the SiPM output reaches a predetermined threshold. A transimpedance amplifier acts as the interface between the summing lines and the off-chip ADC and FPGA by converting the single-ended current signal to a differential voltage. Analog line drivers are used to tune the channel output impedance over a range of loading conditions (50Ω - 200Ω) presented by a variation in the Firewire lengths, shape, etc., all of which influence the load impedance presented to the ASIC output.

4.1 Current Amplifier

The use of current amplifiers at the SiPM interface is motivated by the need to present low input impedance to the SiPM current output, and to extend the bandwidth at the SiPM-amplifier interface. The regulated cascade (RGC) architecture [41] has been used. Figure 14 represents the RGC architecture with the transistors M1-M5.

According to the small-signal analysis, the gain of the amplifier is given by

$$\frac{\partial I_{OUT}}{\partial I_{IN}} = - \frac{g_{m3}(1 + g_{m4}R_1)r_{ds2}r_{ds3}}{\frac{1}{g_{m5}} + r_{ds3} + g_{m3}(1 + g_{m4}R_1)r_{ds2}r_{ds3}}$$

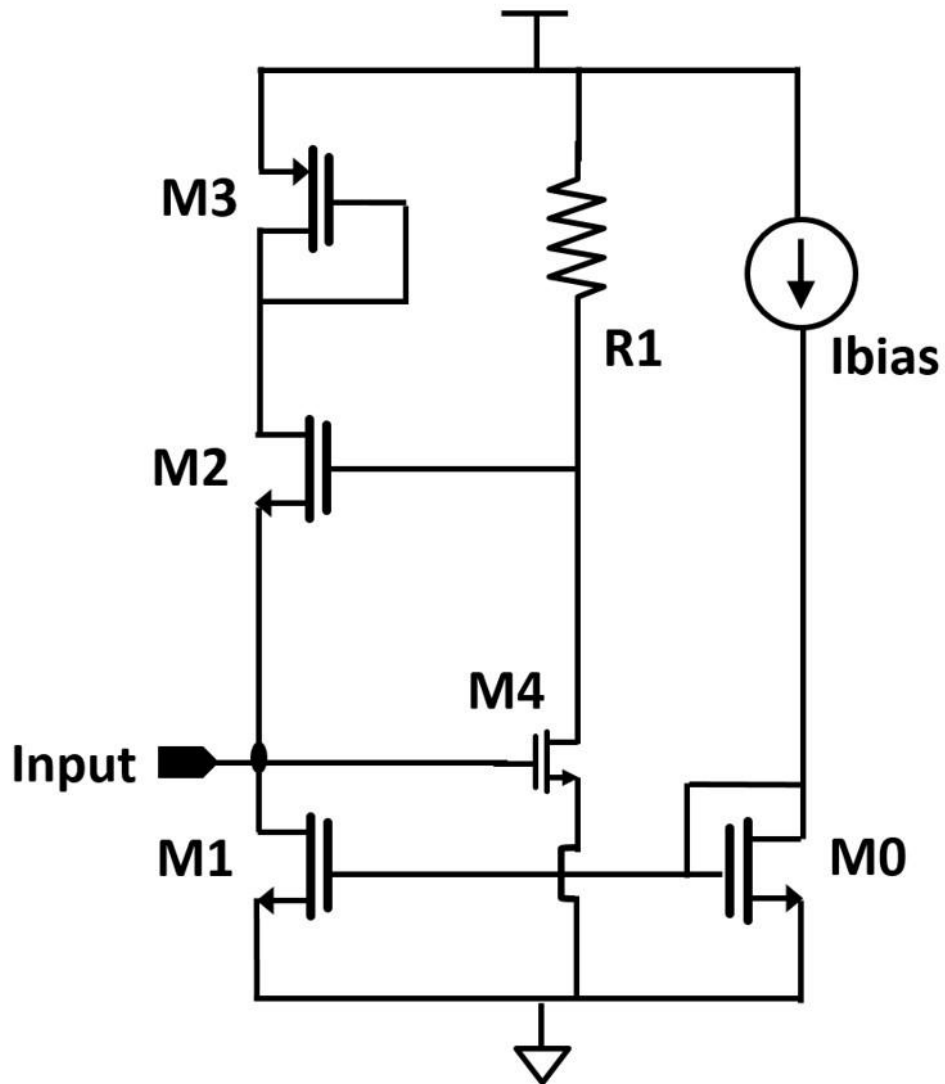


Fig. 14: Regulated Cascade Architecture

Evident from the expression is the fact that the gain of the amplifier is less than unity, and hence needs a variable gain stage for gain enhancement. The feedback loop comprised of the transistors [M3-M4] keeps the input impedance low because of the shunt feedback. The value of the input impedance is given as

$$Z_{in} = \frac{1}{g_{m3}(1 + g_{m4}R_1)}$$

The bandwidth of the amplifier is given by the input impedance and the capacitance of the SiPM device. The input referred noise current due to M1, M2 and M3 is given by

$$I_{n,in}^2 = 4kT \frac{2}{3} (g_{m1} + g_{m3})$$

The input referred noise current due to M4 and R1 is given by

$$I_{n,in}^2 = 4kT \left(\frac{2}{3g_{m4}} + \frac{1}{g_{m4}^2 R1} \right) (C_{in}\omega)^2$$

From the equations, it is clear that one has to increase g_{m4} and R1 to decrease the input impedance and the input referred noise current. But in order to increase g_{m4} we need to decrease R1. Thus, there is a tradeoff between the noise performance and the input impedance, and hence the bandwidth. In our circuit, a current source is used as an active load with the common source stage, as shown in Figure 15. The output impedance and the minimum required v_{dsat} of M7 are less strongly coupled than the value and the voltage drop of a resistor. As a result, the gain obtained can be increased by increasing r_{ds7} while maintaining the same overdrive voltage across the transistor. The common source stage is cascaded with a common gate stage composed of transistors M4 and M5, to further increase the gain obtained from the feedback loop and decrease the capacitive loading at the input of the amplifier. The input impedance of the common gate stage is relatively high compared to the input impedance of M2, because the load impedance connected to the drain is relatively high. Hence, the current sharing between the transistors M2 and M5 is minimized. The penalty associated with this circuit is the presence of two poles within the feedback loop. R1 and C1 are used to compensate the frequency response of the loop for maintaining the stability of the loop.

transistors M81-M84 operating as switches. The cascode transistors M41-M45 increase the output impedance of the current mirror branches and ensure better matching.

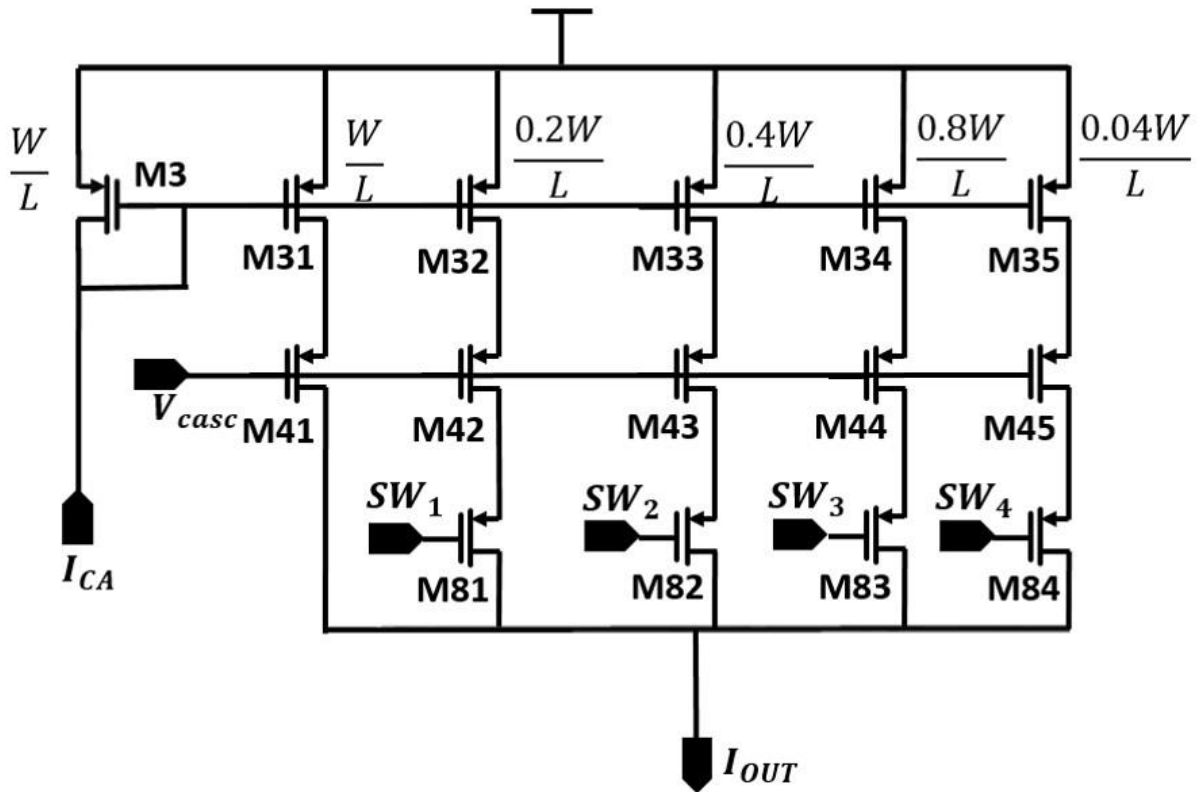


Fig. 16: Variable Gain Stage

4.3 Current Comparator

One challenge associated with the row-column summation approach is the potential accumulation of noise down a single line. This problem is exacerbated by combining the output of multiple SiPM devices along a row or column. The situation is illustrated in Figure 17, where the dark current generated in an individual SiPM device is shown to accumulate with other detectors, sharing a row or column output line. When the noise is added at the output, there is an increased

chance of false triggering as compared to a single-channel readout of individual SiPMs, as the accumulated noise from the row or column output, is likely to be comparable to a desired signal.

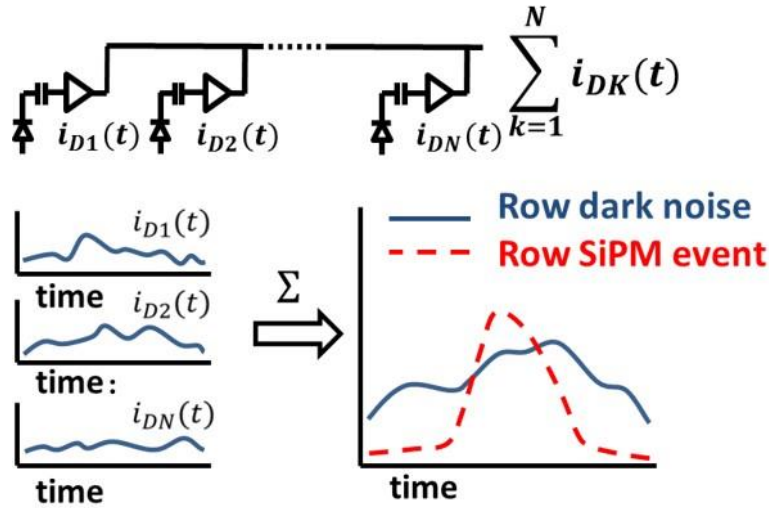


Fig. 17: Dark Noise Accumulation across a single row

In the Row Column Architecture (RCA), threshold detection is used to decrease the noise contribution on the summation lines. The input SiPM current is compared with a programmable threshold current, and if the current of the input signal falls below a threshold which would signify a detected gamma event, the output stage of the current amplifier is disconnected from the summation lines using the switches, as shown in Figure 18. Threshold detection becomes challenging for a continuous-time amplifier where the delay associated with the main amplifier and the threshold detection circuitry becomes critical. In short, any mismatch in the delay between these two paths will clip the rising edge of the SiPM pulse. Thus, the speed of the threshold detection circuitry becomes paramount to minimize any loss of information on a real detection event.

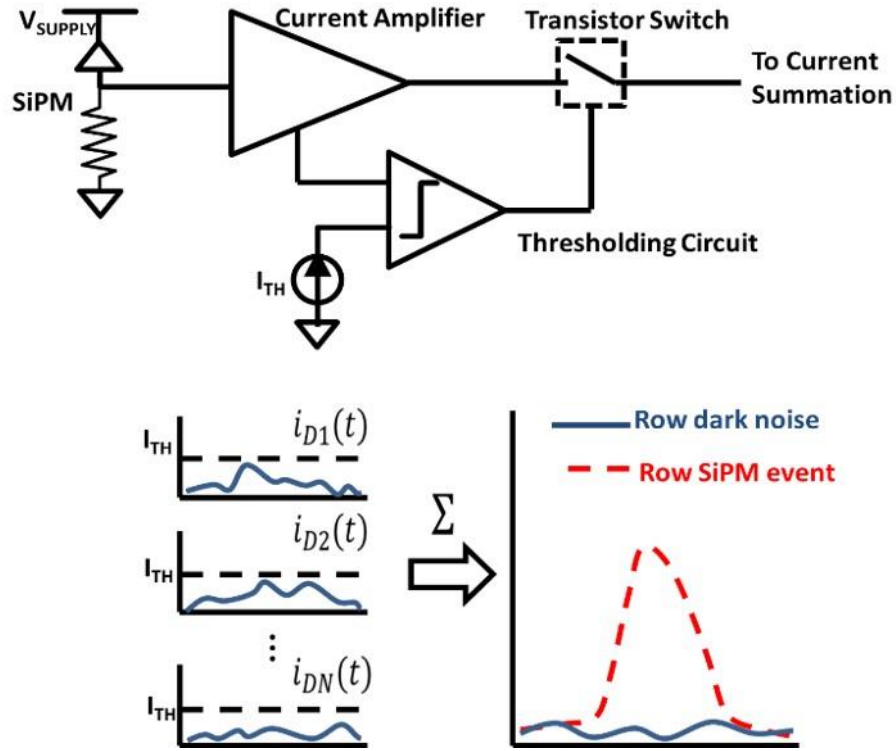


Fig. 18: Threshold Detection Circuit

The signal is run current mode from the SiPM output to the row and column lines. As such, a current comparator is utilized to realize the threshold detection circuitry. Because current-mode signals are used, the input impedance of the comparator needs to be low to improve the bandwidth and minimize loading of the previous stage. In addition, to ensure all devices in the comparator remain in saturation, an input bias voltage is established at half the supply voltage. In the proposed current comparator, Figure 19, the input stage utilizes a regulated cascode (transistors M1 – M5) to lower the input impedance of the circuit and reduce the propagation delay at high frequencies. An inverter chain at the output of the comparator amplifies the threshold detection signal, forcing the output to run rail-to-rail. The inverter with resistive feedback (M6-M7) allows the transistors to operate in the saturation region, thus having a very high voltage gain. A replica bias circuit is implemented to force the DC bias voltage at the input of the CMOS inverters to $V_{DD}/2$. This further improves the propagation delay by holding the inverter input bias voltage to the tripping

point of the comparator. The replica bias circuit also provides a resistive load which is better controlled over process, voltage and temperature (PVT) variations.

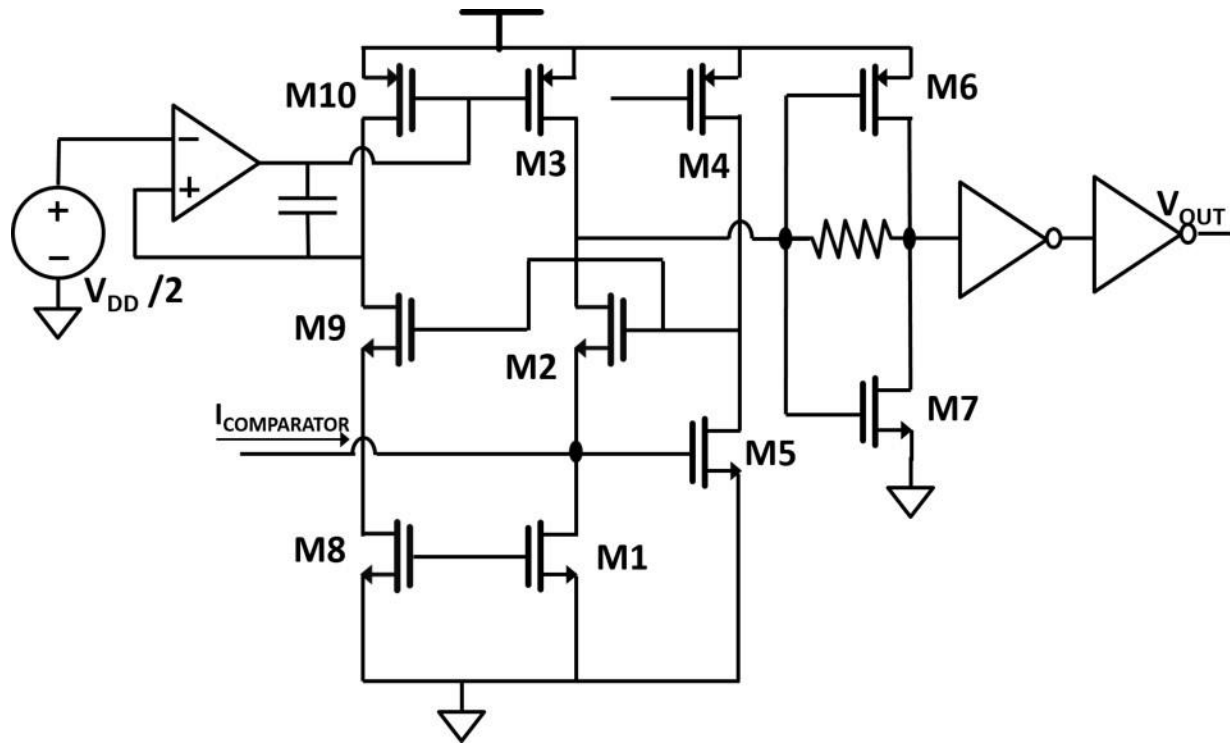


Fig. 19: Current Comparator

4.4 Current Mode Signal Path

The signal path consists of current mode switches controlled by the comparator output, as shown in Figure 20. To minimize the propagation delay introduced by the threshold detection technique, a current-mode switching circuit is used which is analogous to high-speed current commutating mixers. The output stage of the current amplifier in the main signal path is either routed to the transimpedance amplifier through the common row-column line, or to the supply when sitting idle. This is done by using switches arranged in complementary fashion, as shown in the figure, similar to that of a charge pump PLL to prevent charge sharing between intermediate nodes. If an event is detected which is above the threshold current setting, the detection circuitry

will current commute the amplifier's output stage into the common row-column line. This ensures that a constant bias current flows through the amplifier output stage, to allow for fast switching. The voltage along the row column line is held constant by the input stage of the transimpedance amplifier.

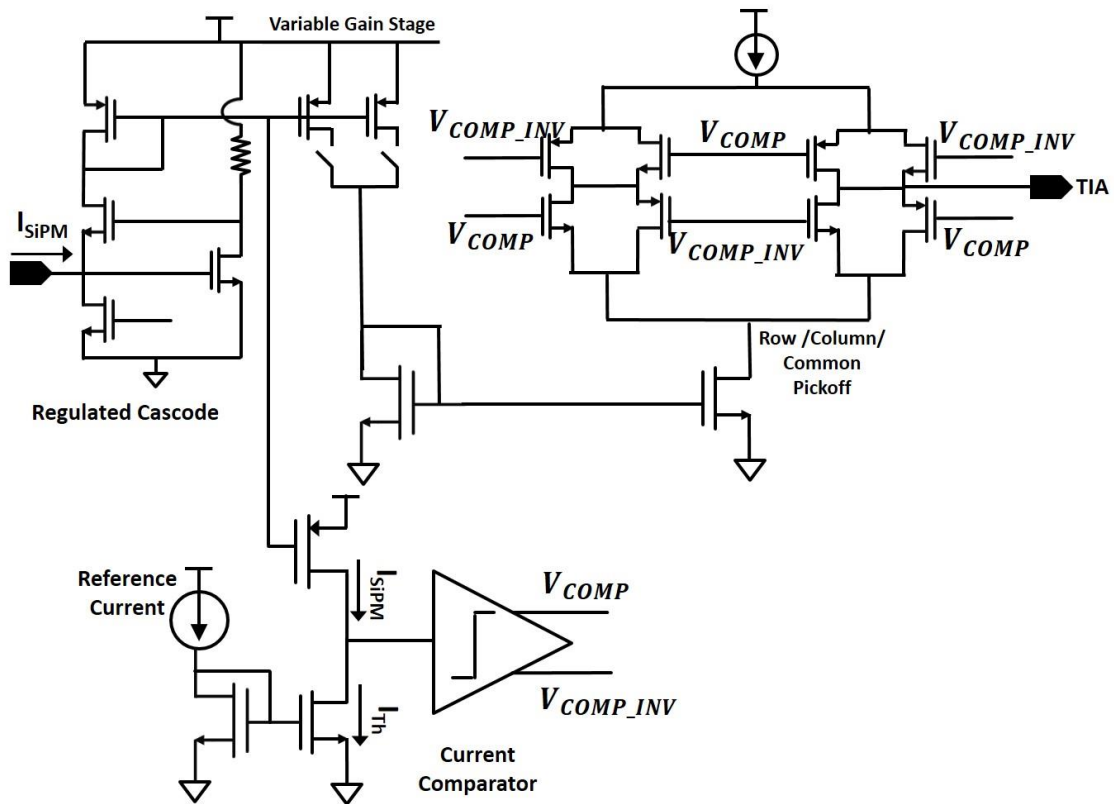


Fig. 20: Current Mode Signal Path

In order to reduce current mismatch between the upper and the lower current sources, a voltage controlled current source is used in the upper current branch. This ensures that the devices in the front end of the transimpedance amplifier are not pushed out of the high gain region. The details of this scheme are described in the next section.

4.5 Transimpedance Amplifier

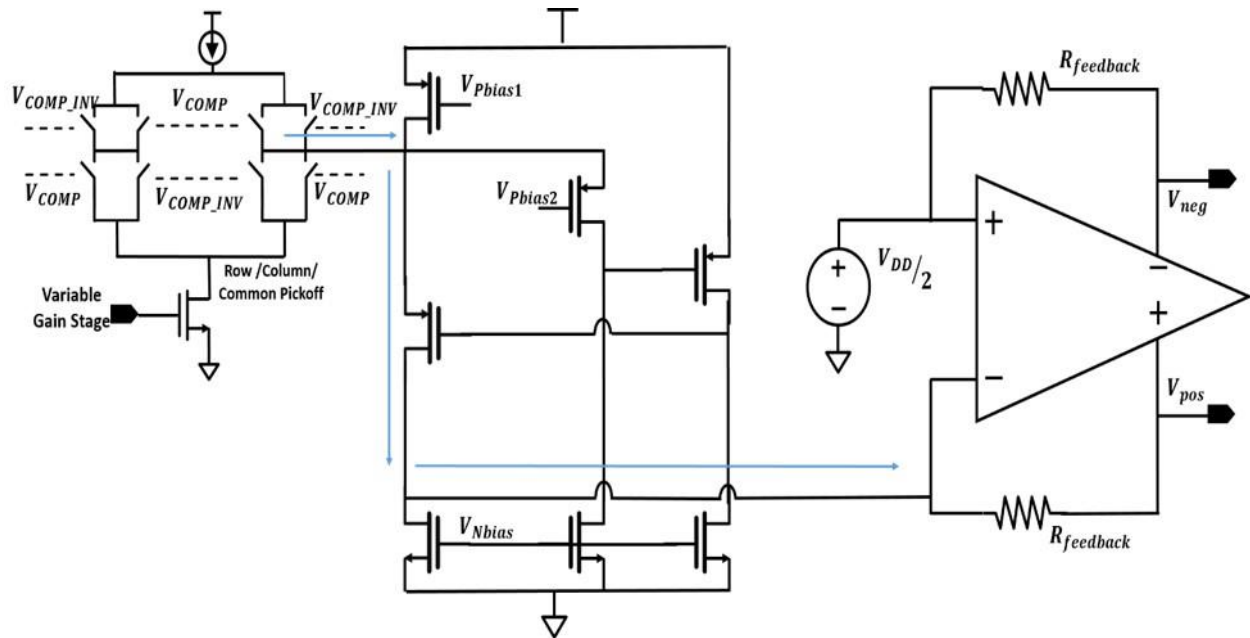


Fig. 21: Input Stage of Transimpedance Amplifier – Regulated Cascode

The output at the end of the summing channels is single ended, but the input to the ADCs in the back end is differential. A transimpedance amplifier is necessary to convert the single-ended current into the differential-ended voltage. The input stage consists of a regulated cascode stage to keep the input impedance to a minimum. This was done to prevent any current division at the summing node at the end of the signal path, as shown in Figure 21. The capacitive loading at the input of the transimpedance amplifier is relatively high because it is shared by all the elements across a particular row or column, and in the case of the common pickoff channel, by all the 64 elements. The low impedance at that node because of the shunt feedback in the regulated cascode stage ensures that the pole introduced by that node is at higher frequencies, and doesn't reduce the bandwidth of the channel. The signal path is highlighted in the figure 22. The differential and

common mode feedback inside the transimpedance amplifier ensures that there is no DC voltage difference across the feedback resistors. But any mismatch of DC current in the up and down current sources would result in either current being supplied to or absorbed from the input branch of the regulated cascode. This would create a DC voltage difference across the feedback resistors, thus compromising the linearity of the circuit.

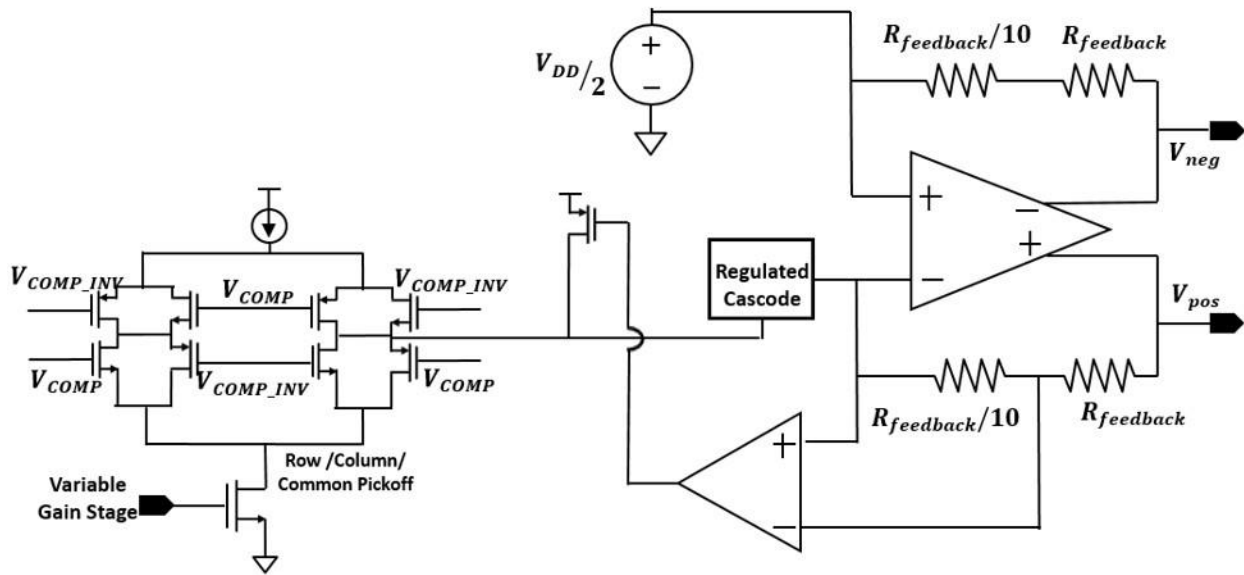


Fig. 22: Low Bandwidth Feedback Circuit to reduce dc current mismatch

As explained in the last section, there is a voltage controlled current source in the signal path to ensure there is no DC current mismatch between the two current sources. The scheme utilizes the voltage difference across the feedback resistor in the input current branch to control a current source supplying or absorbing the extra current from the current summation node, as shown in Figure 22. The bandwidth of the feedback loop needs to be low enough so that it doesn't compromise the circuit operation in the signal bandwidth (> 10 MHz). The dominant pole in the feedback loop was brought down to lower frequencies by using a high compensation capacitor (50 pF). To reduce the area, MOS capacitors are used due to their higher density compared to MOM

caps. Also, the loop gain is reduced by sensing the voltage difference across $R_{fb}/10$, reducing the bandwidth further.

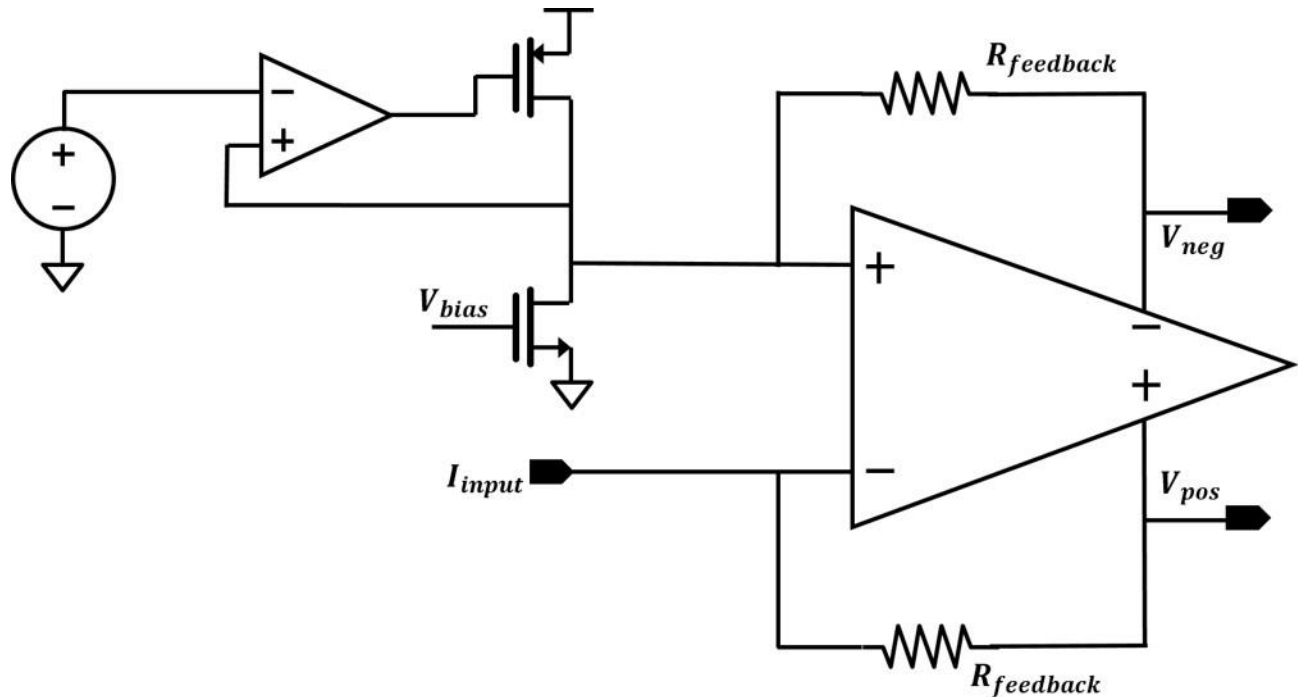


Fig. 23: Single-ended to Differential Scheme

The amplifier is a two stage operational amplifier with the 2nd stage cascoded. To get a fully differential system from the single-ended current, the virtual ground at the input of the amplifier should always hold; in other words, the inputs need to be fixed to the common mode voltage value. As a result, the performance of this scheme depends on how accurately the DC input voltage of the op amp is maintained at the common mode voltage. For this, a circuit that detects the difference between the positive input and the common mode value, is needed. Also, it should provide a DC path for the current to flow in the feedback resistor, because the operational amplifier virtual ground being the gate of a MOS transistor can neither supply nor absorb any current. The circuit is realized by a voltage controlled current source which checks the difference between the voltage values, and generates a current, as shown in Figure 23. The differential feedback of the

amplifier ensures that the two inputs are held at mid rail, while the common mode feedback inside the amplifier maintains the common mode output voltage at mid-rail.

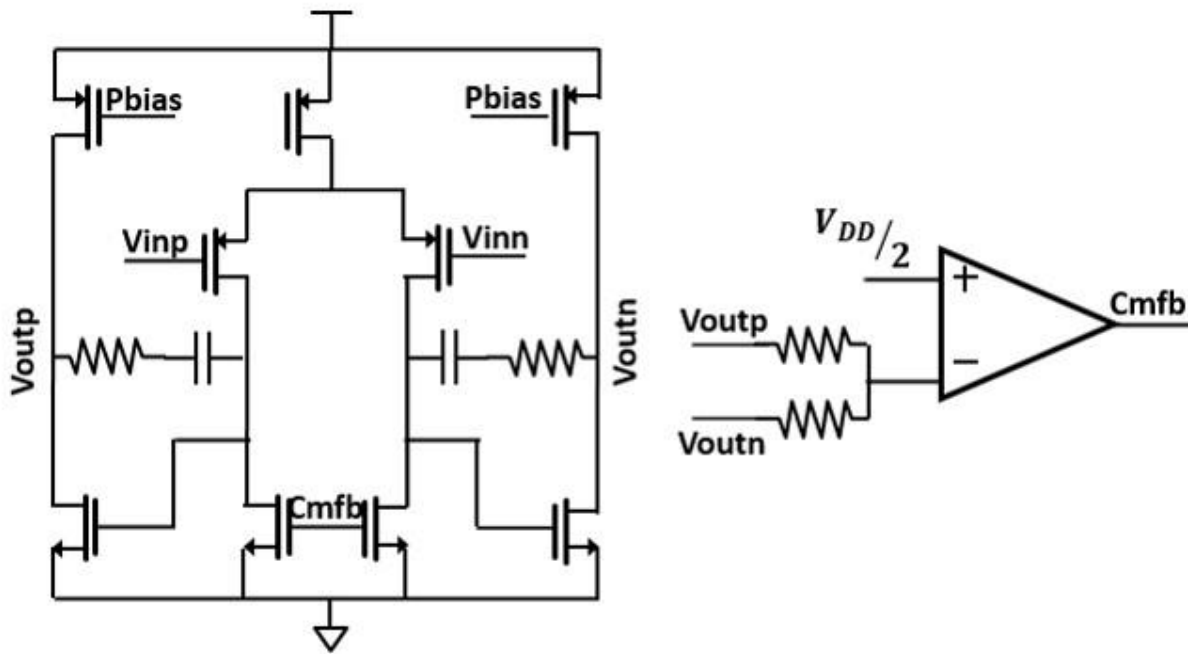


Fig. 24: Transimpedance Amplifier

The operational amplifier is a two stage amplifier, where the second stage produces the differential output voltage. The amplifier uses a fully differential scheme to increase noise immunity, increase output swing and improve linearity. The resistive gain of the transimpedance amplifier was fixed at 500 ohms. The transimpedance amplifier is a two stage differential amplifier, as shown in Figure 24. The dynamic range required is 1V peak-to-peak for a 1 mA input current signal from the summing node. To meet the specification, the PMOS devices in the output stage are made wider ($900 \mu\text{m}/0.4 \mu\text{m}$) so that they have a v_{dsat} less than 100 mV. The resistors for the resistor divider used to detect the common mode output voltage are made larger ($5 \text{ k}\Omega$)

compared to feedback resistors to minimize any loading effects on the output of the amplifier. The common mode feedback loop is composed of a single stage differential amplifier and the NMOS active load devices in the first stage of the transimpedance amplifier. This is done to decrease the number of nodes in the feedback loop.

4.6 Line Driver

Co-axial cables act as the interface between the ASIC and the backend ADC. Like transmission lines, the source and load impedance of the cable needs to be equal to the characteristic impedance of the cable to reduce reflections. However, cable to cable characteristic impedance variation makes this job difficult. For coaxial cables, this variation can be $\pm 2\%$, while for twisted pair cables this variation can be as high as $\pm 15\%$. This cable variation combined with process variations can cause the transmit signal to vary significantly. To address these issues, analog line driver circuits are realized which can adapt their output impedance to a value equal to the applied load, minimizing reflections. The design of an efficient line driver is a challenging one in modern low supply voltage CMOS processes. The approach used here builds upon the architecture used in [42]. This is shown conceptually in the Figure 25.

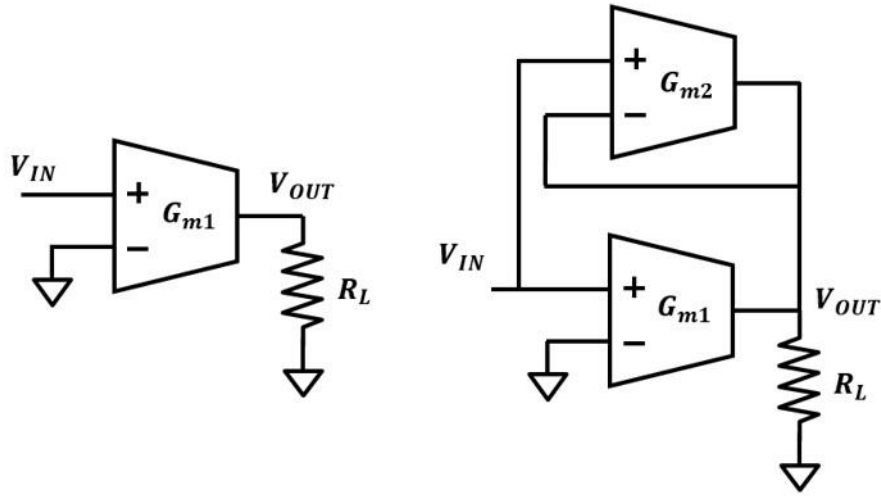


Fig. 25. Theory of Operation of Line Driver [42]

In Figure 25, a linear transconductance cell, G_{m1} , is used to drive a signal line, modelled by the resistive load R_L to obtain a voltage gain and output impedance given by

$$\frac{V_{OUT}}{V_{IN}} = R_L G_{m1} \quad Z_{OUT} = \infty$$

If a second ideal transconductance cell, G_{m2} , is added in the feedback loop as shown in the Figure, then

$$\frac{V_{OUT}}{V_{IN}} = \frac{(G_{m1} + G_{m2})R_L}{1 + R_L G_{m2}} \quad Z_{OUT} = \frac{1}{G_{m2}}$$

If G_{m1} and G_{m2} are set to $G_{m1} = G_{m2} = 1/R_L$, then

$$\frac{V_{OUT}}{V_{IN}} = 1 \quad Z_{OUT} = R_L$$

With a voltage gain of unity, the differential input voltage to G_{m2} is ideally zero. Thus, it produces no output signal current, and hence a tunable output impedance is achieved without incurring any loss.

In the chip, the transconductor G_{m1} is implemented as shown in Figure 26 [43]. The input voltage is copied across R_1 using an operational amplifier and the transistor M_1 . The resulting current is amplified by a factor of N because of the sizing of the transistor M_2 , and produced at the output. Making $R_1 = NR_L$ results in a transconductance of $N/R_1 = 1/R_L$ [43]. N is chosen to be large enough so that most of the power is consumed in the output branch consisting of M_2 and the load, while minimizing the power consumption in the operational amplifier and the branch consisting of M_1 and R_1 . G_{m2} is implemented by placing R_2 as shown in the figure. In the ideal case, the output impedance is given by

$$Z_{OUT} = \frac{R_2}{N+1}$$

So, the final design values of R_1 and R_2 are chosen to be

$$R_1 = NR_{Lnom} \quad R_2 = (N + 1)R_{Lnom},$$

where R_{Lnom} is the nominal value of R_L [ref].

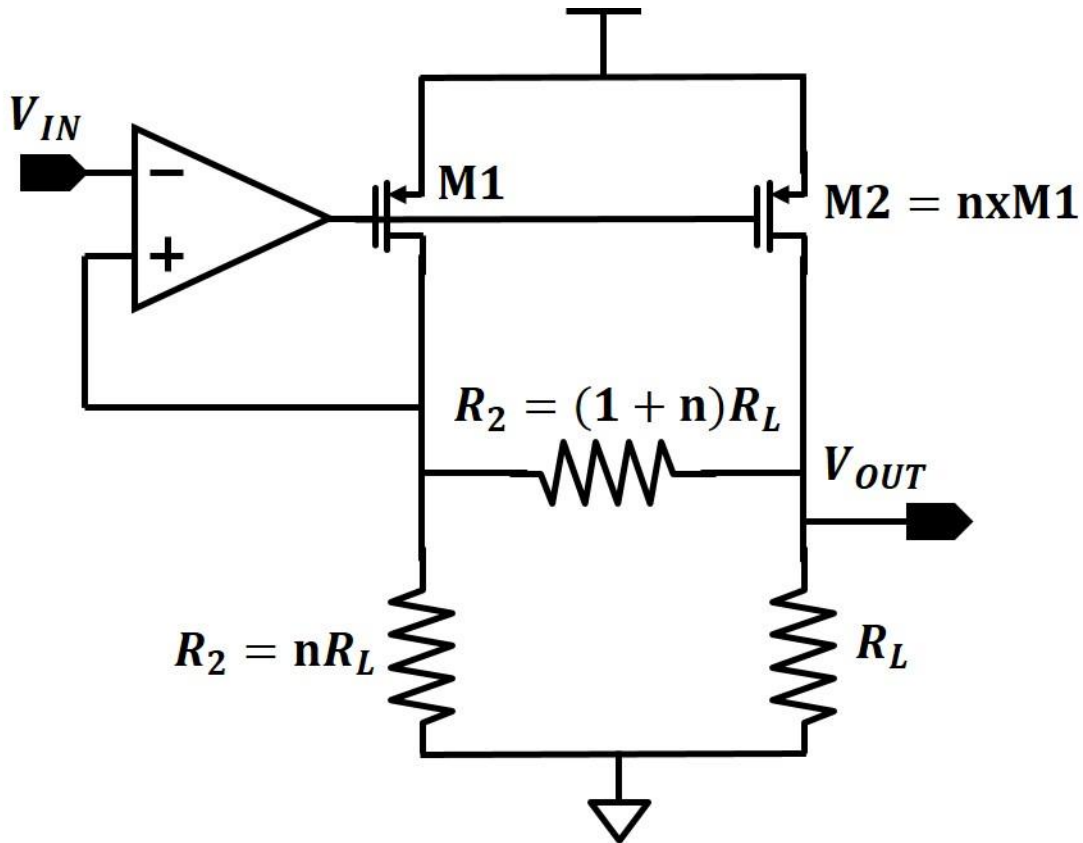


Fig. 26: Line Driver Circuit Implementation (PMOS driver stage) [41]

The output from the transimpedance amplifier is differential, so complementary structures were followed for the line drivers for each of the channels, as shown in the figure 27. The value of N was chosen to be 10 for the NMOS line driver and 18 for the PMOS line driver. The co-axial cables used by the PET imaging systems used in this work have characteristic impedances in the range of 50 – 200 ohms. The tuning range for the output impedance was chosen accordingly with steps of 10 ohms. Resistor banks for all these values were created for both R_1 and R_2 , and they were controlled using MOS switches. Sizing of the MOS switches was critical for getting the required bandwidth from the circuit and maintaining the stability of the loop.

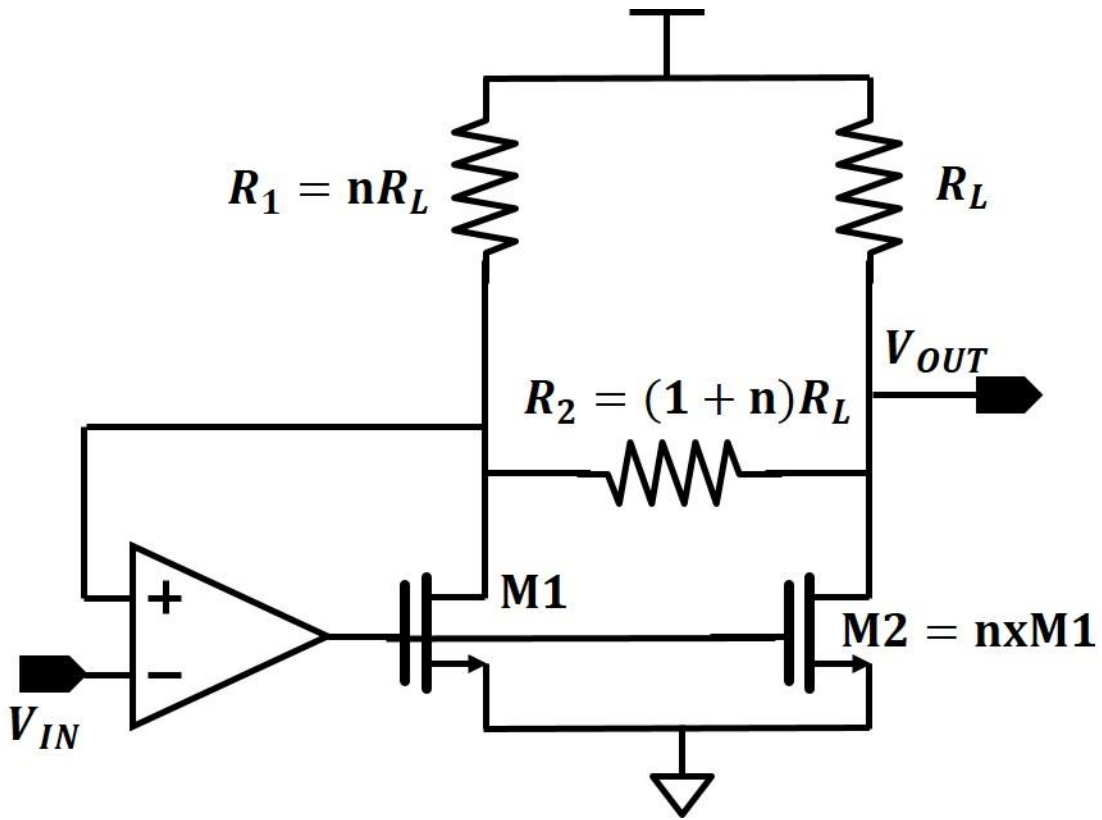


Fig. 27: Line Driver Circuit Implementation (NMOS driver stage) [41]

5. Measurements

In this chapter, measurement results for the ASIC are presented. The ASIC was designed and laid out in a 130 nm STMicroelectronics HCMOS9GP process using a 6-layer metal stack.

5.1 Die Photo

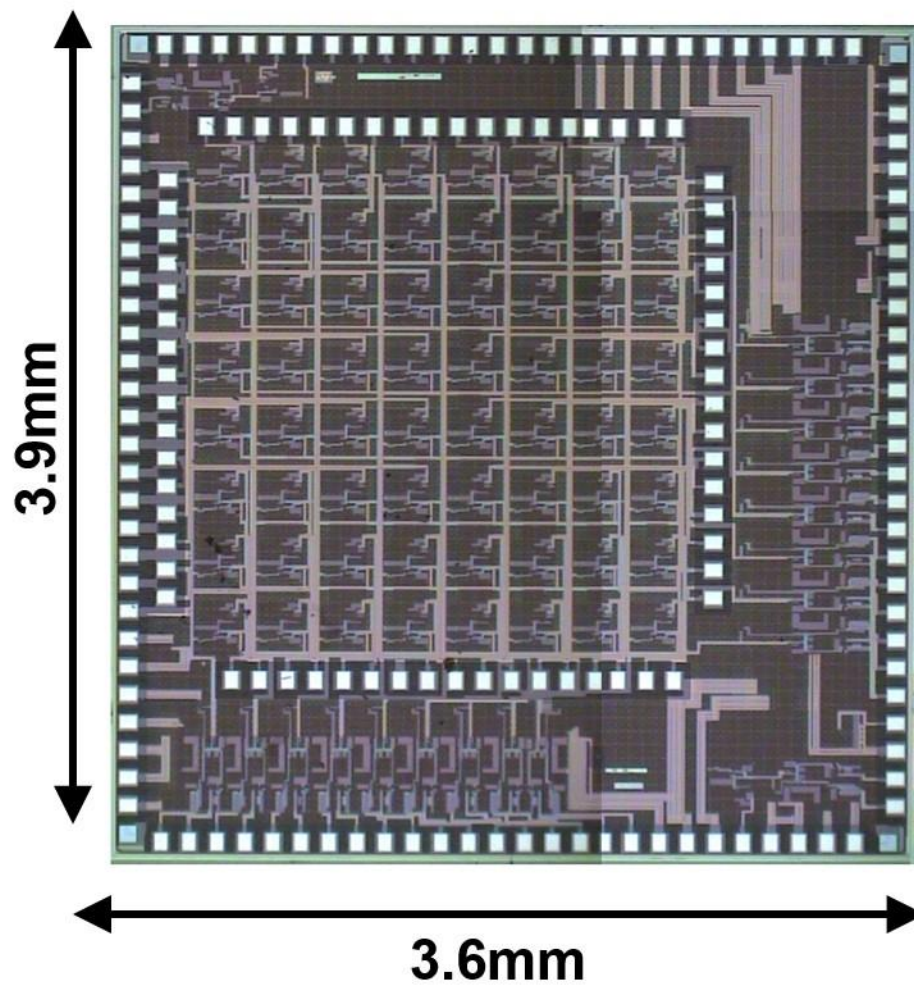


Fig. 28: Die Photo

Figure 28 shows the die photo of the entire chip. The chip dimension is 3.9mm x 3.6mm. The total number of pads is 173, which are arranged in two rings. The inner ring of pads is for the input to the current amplifiers, to ensure the input impedance is kept to a minimum. The outer ring of pads is used for the power supply pads, channel outputs, bias current input, and the on-chip shift register inputs and output.

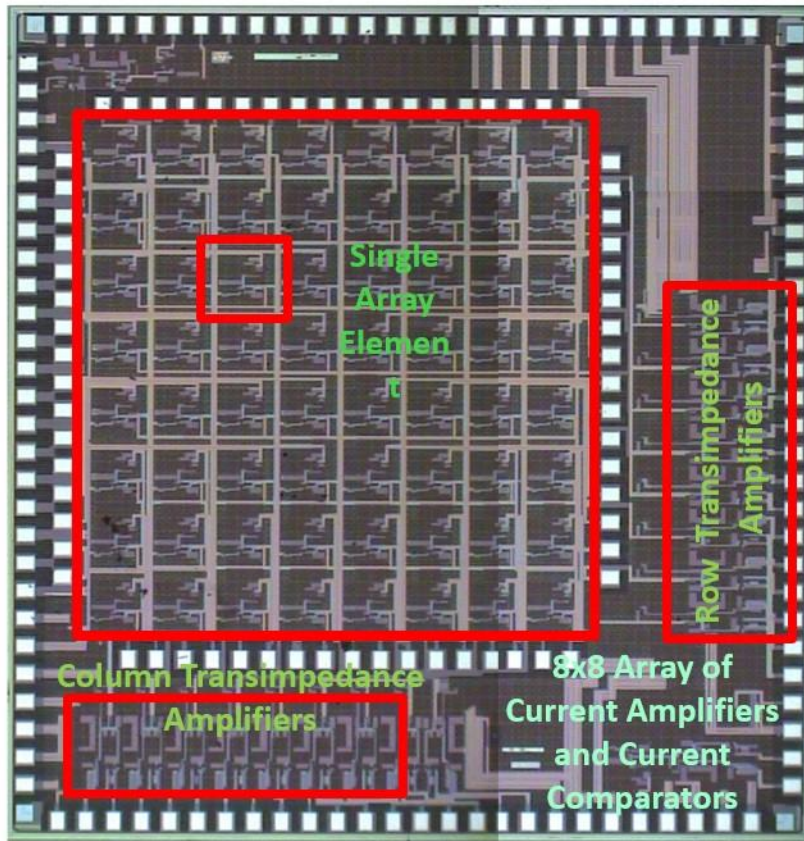


Fig. 29: Die Photo showing different blocks of the system

Figure 29 shows the 8x8 array of current amplifiers and current comparators in the center. The transimpedance amplifier blocks have been highlighted, with the column amplifiers in the bottom left and the row amplifiers in the left of the chip. Figure 30 shows the test channels and the 1000 bit on chip shift register for feeding in the digital bits for controlling various blocks. In order

to ensure there is no racing condition in the shift register, buffers have been placed between each stage of the shift register. There are two test channels, Test Channel SR and Test Channel NSR. SR is controlled by the on chip shift register, while NSR is controlled by off-chip digital bits.

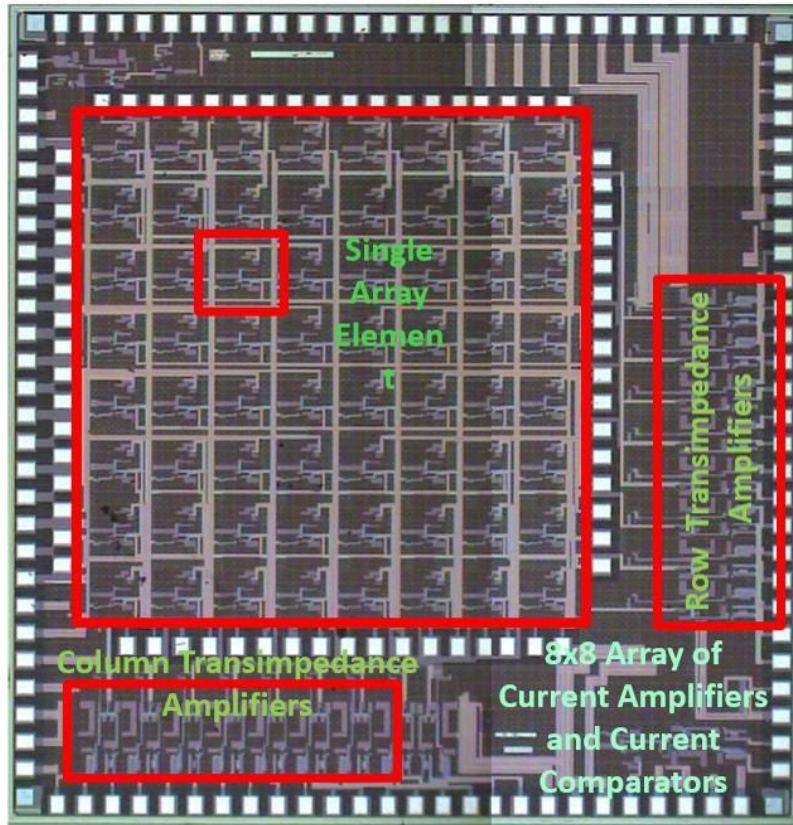


Fig. 30: Test Channels, Bias Circuitry and Shift Register

5.2 Test Setup

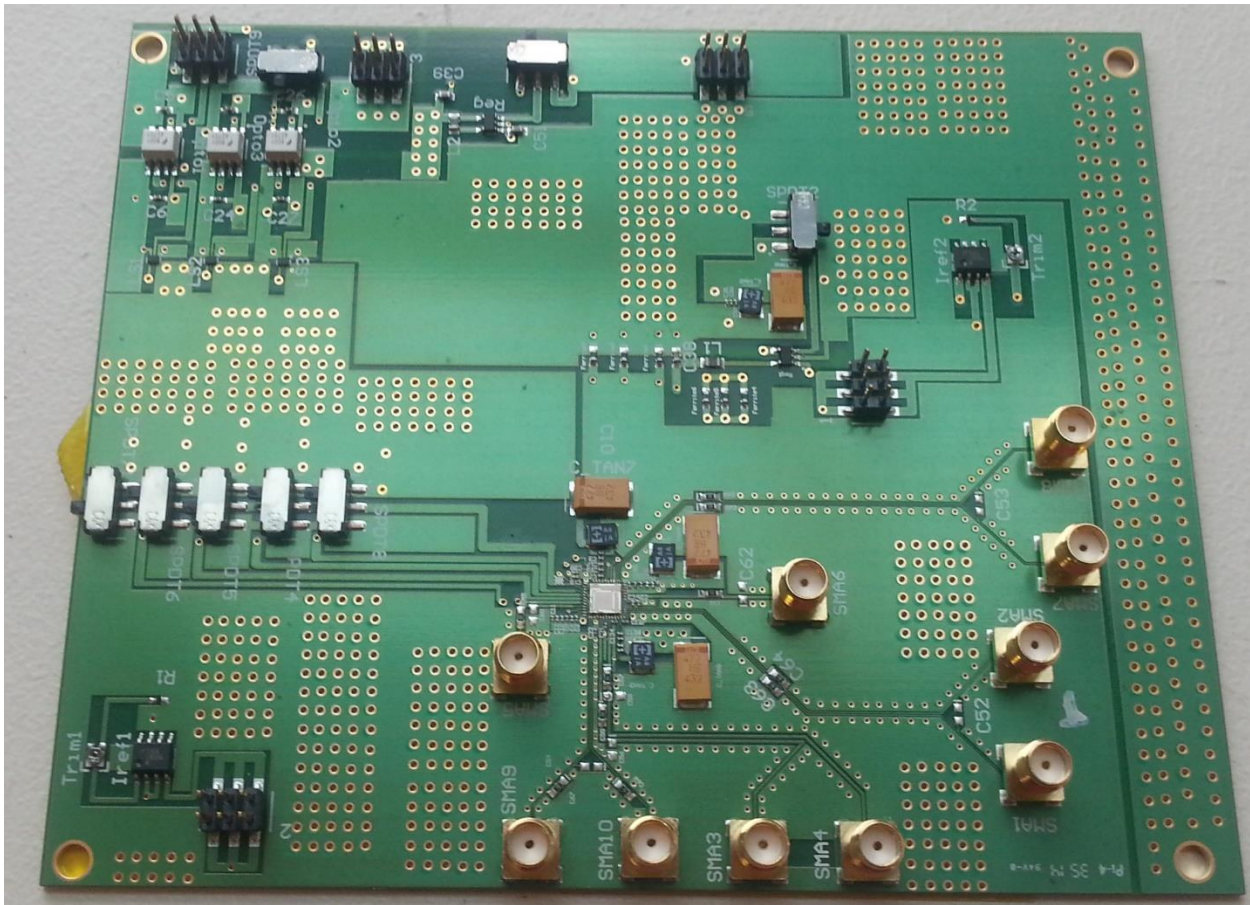


Fig. 31: Test Board (Chip-on-Board Assembly)

The first version of the test board has a “chip-on-board” assembly, as shown in the figure 31. All the pads were not utilized in this version of the board, because the goal was to test the basic functional of the individual channels, and an individual column-combined channel on the chip. As a result, the test channels were measured in this setup, along with a column channel. The current bond pad structure leads to difficulties with chip-on-board packaging, because two rings of pads make the length of the bond wires quite long. For the final testing, we are packaging the ASIC in a wire bond ball grid array chip (BGA) standard adapter board from Amkor Corporation. Figure

32 shows one of the ten ASICs we had packaged and the new adapter board to connect it to the SiPM array. The ASIC is glued to the center of the open die and then wire bonded to the surrounding pads. After electrical checks by Amkor to assure the wire bonds are connected properly, the package was sealed. The package size is no more than 12x12mm.

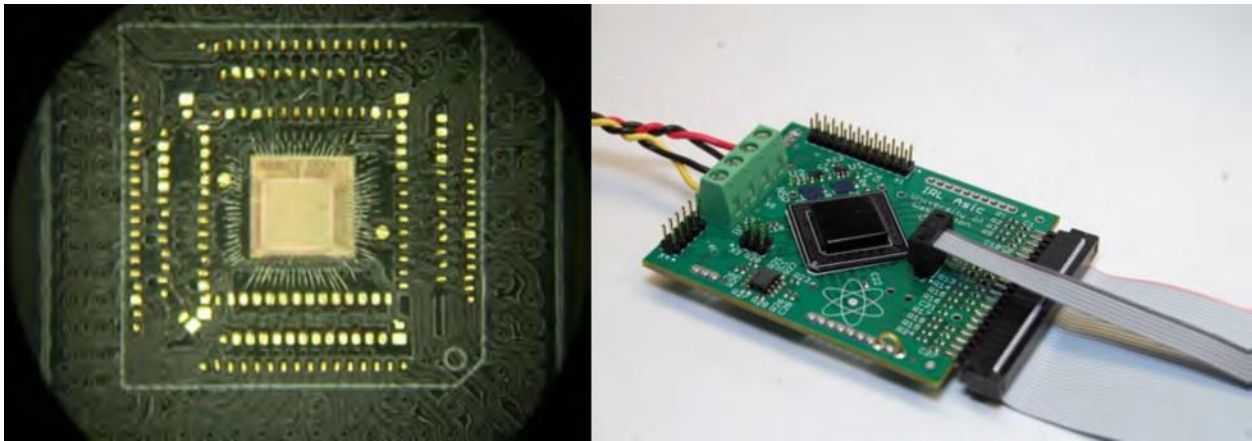


Fig. 32: BGA Package – (Left) Die in the middle of the package before encapsulation and (Right) the package mounted on new test board

5.3 Variable Pulse Generator

To simulate the timing characteristics of SiPM pulses, a variable pulse generator was used. The pulses had a rise time of 30 ns and fall time of 100ns with varying amplitudes. The plots below show the output response of the column channel under different supply voltages and bias currents. The input pulses are shown in the bottom, and the channel output in the top. As can be seen in the figures, the channel output is not distorted with respect to the input, and hence maintains the timing information of the input pulse.

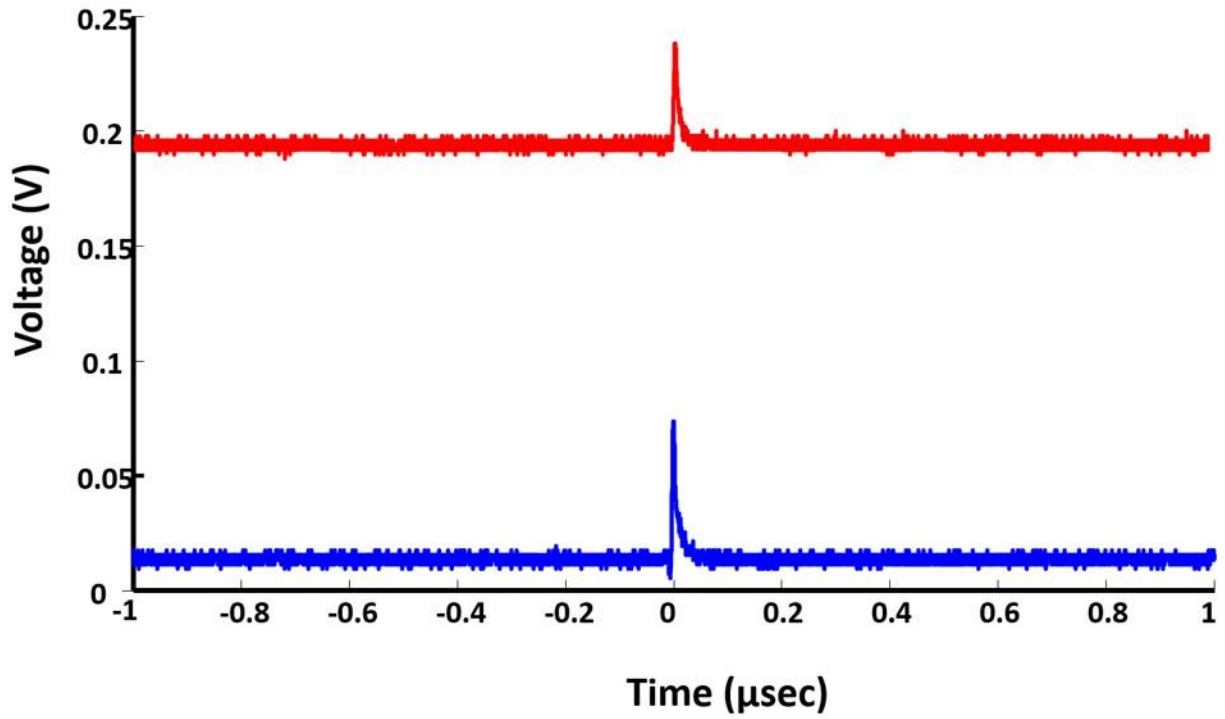


Figure 33 $V_{dd} = 1.2V$, $I_{bias} = 10 \mu A$

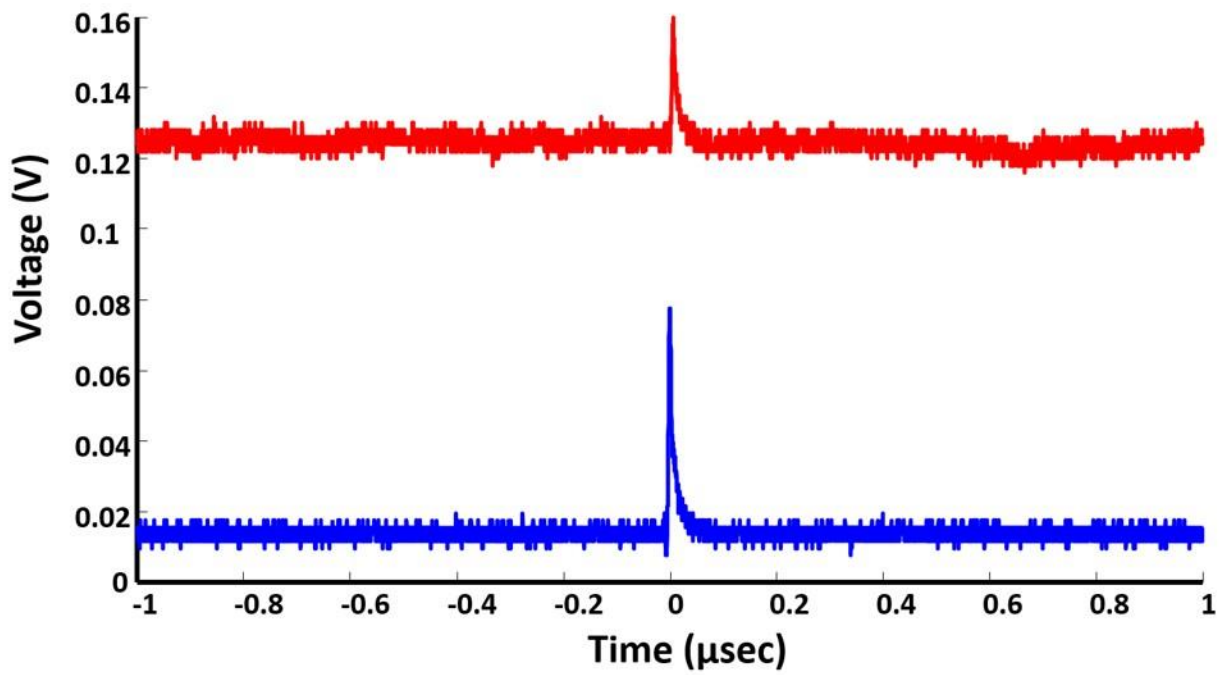


Figure 34 – $V_{dd} = 0.9V$, $I_{bias} = 10 \mu A$

5.4 Threshold Detection Circuit

To illustrate the working of the threshold detection circuit, the pulse generator was used to feed a SiPM current pulse into the channel, while changing the threshold current level of the current comparator circuit. The reference current is changed in binary weights from 0.1mA to 1.5 mA. Below are some of the measured responses with different reference current levels. The bottom waveform is the input to the channel, while the waveform at the top is the output to the channel. When the threshold current is zero, the output of the channel maintains the energy as well as the timing information of the input pulse (Figure 35). But as the threshold current level is increased to 1.2 mA and 1.5mA, the channel output is disabled (Figure 36-37), thus validating the working of the current comparator circuit.

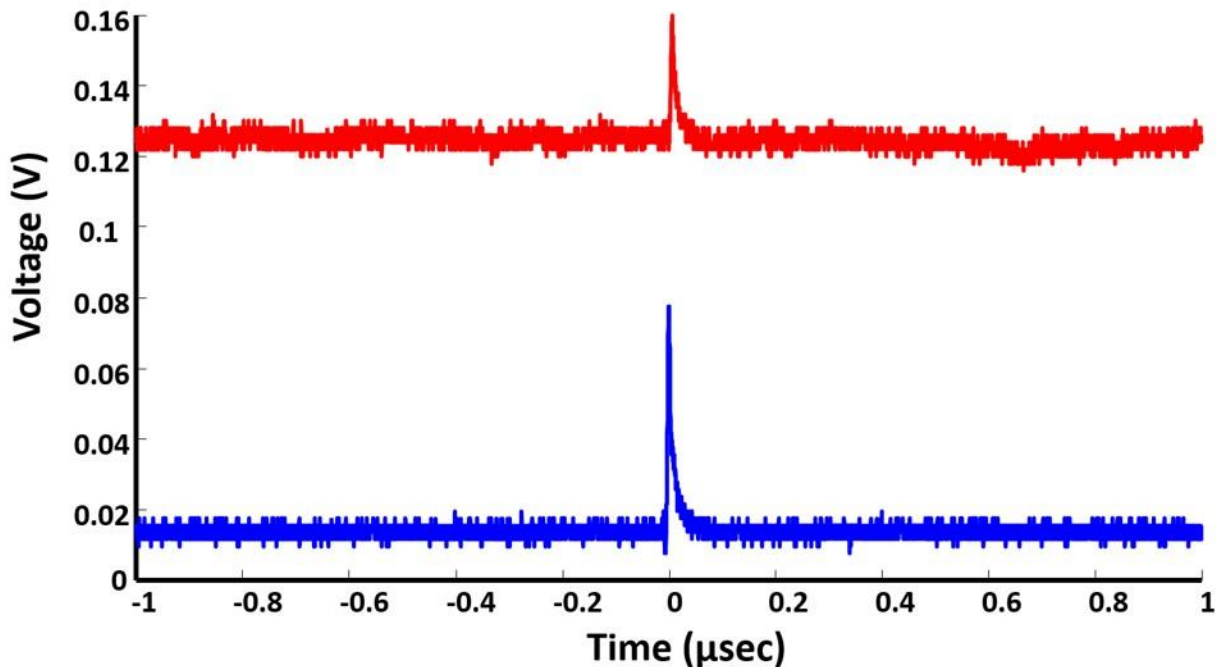


Fig. 35: Threshold Current 0 mA

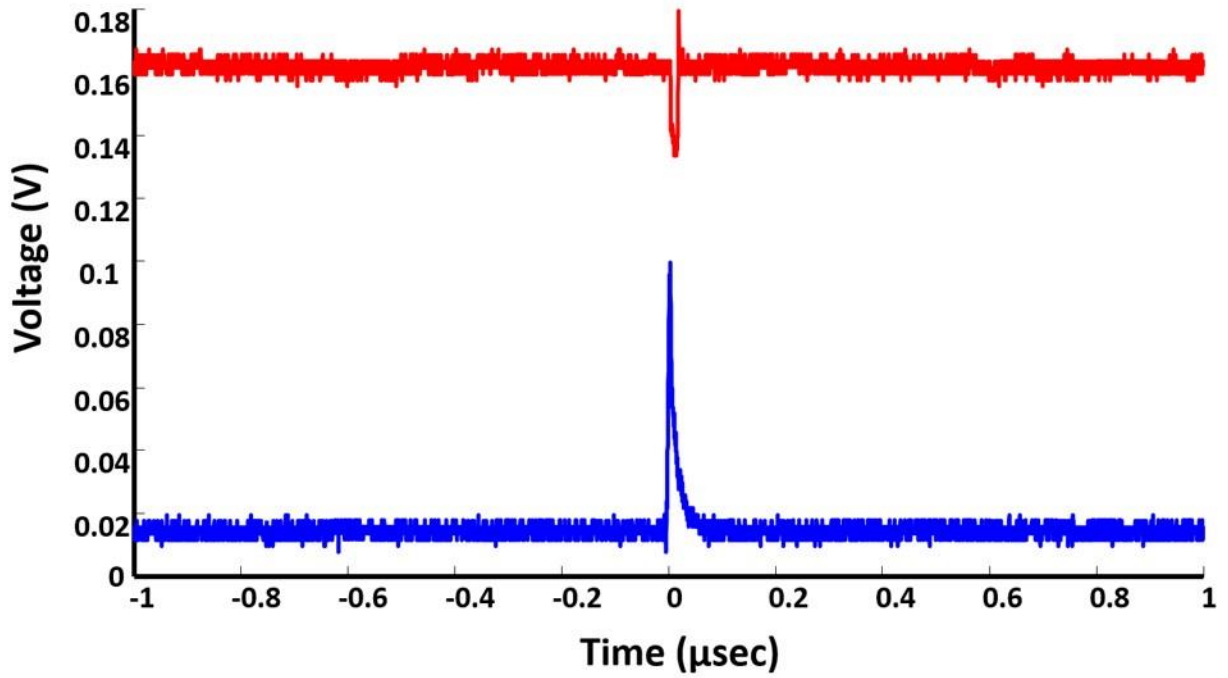


Fig. 36: Threshold Current 1.2 mA

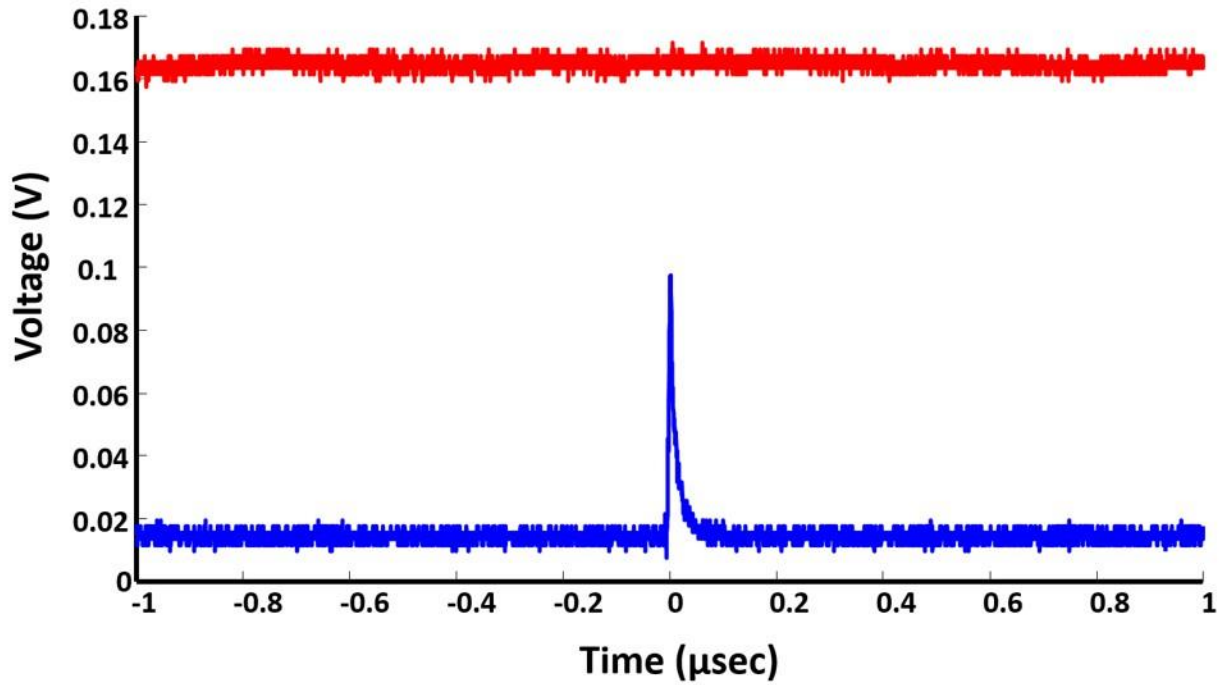


Fig. 37: Threshold Current 1.5 mA

5.5 SiPM Array

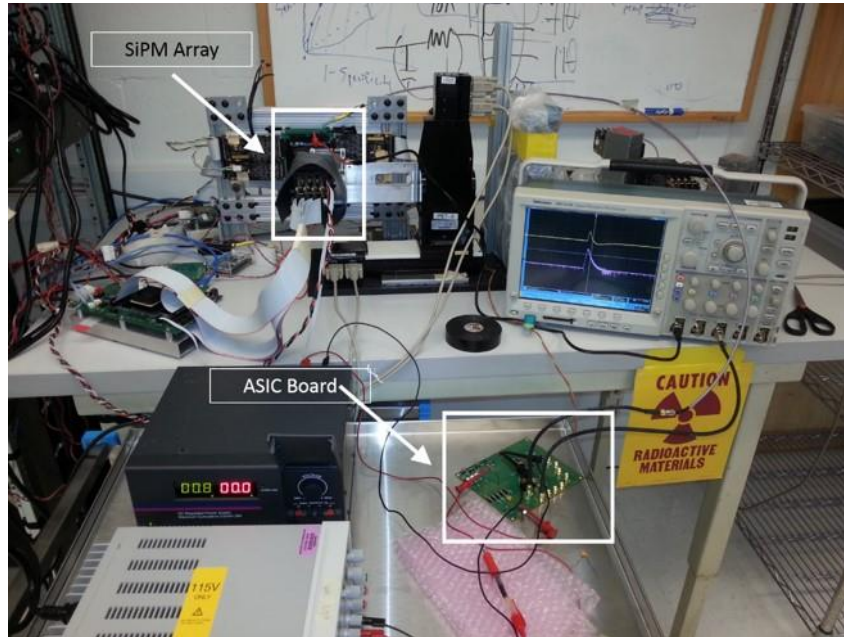


Fig. 38: Test board mounted on a detector test bench

After validating the working of the chip with a pulse generator, the board was tested with a SiPM array and mounted on one of the detector test bench (Figure 38). The signal lead lengths were not minimized for this phase of the testing. Figure 39 shows data from one such test. The top waveform (yellow) is the output of one of the channels in the SiPM array. The bottom waveform is the output of the ASIC. As is evident from the figure, the input and the output appear to be sufficiently noisy. The pulse generator input was used to help determine if the ASIC was injecting significant noise into the signal path. The input and output pulse generator signals (Figure 40) show essentially no noise injection by the ASIC amplifiers and summing circuits. The comparison of a summed column channel (8 SiPM elements) compared to one SiPM channel in a neighboring row also supports other data we have that the noise on the output of the summing channels is coming from the SiPM array, not the ASIC.

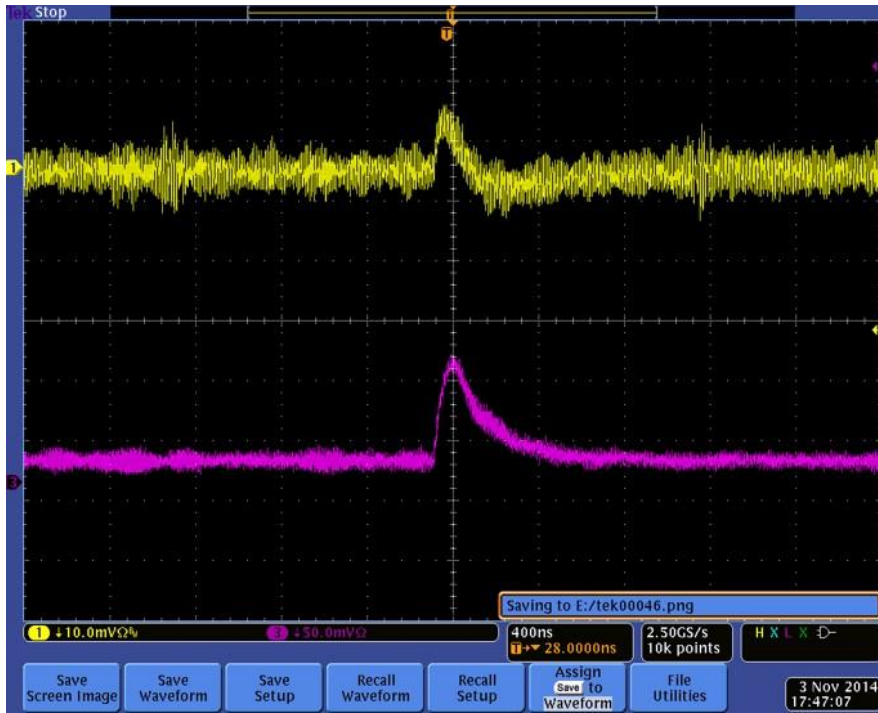


Fig. 39: SiPM signal

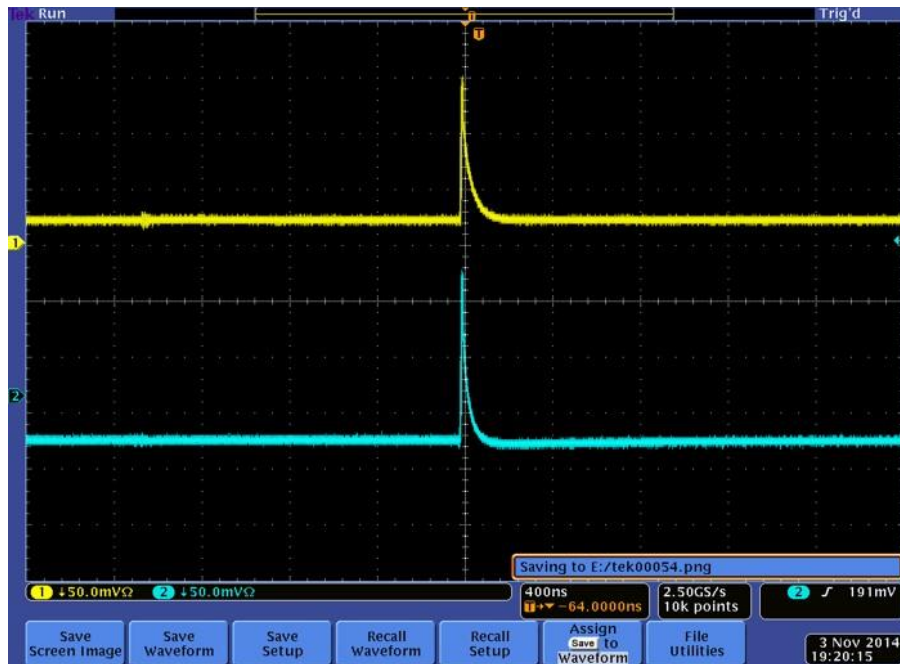


Fig. 40: Pulse Generator

6. Conclusions and Future Work

This work presents the design of a new front-end readout ASIC dedicated to PET imaging systems which facilitates the integration of the SiPM with the front end electronics. The Row Column architecture (RCA) reduces the number of channels between the SiPM array and the backend digital signal processing. A low input impedance high bandwidth current amplifier interfaces with the photo diodes in the front end. The variable gain stage tunes the individual gain of the current buffer, thus helping to calibrate each element of the SiPM array with respect to another. The current comparator minimizes the accumulated noise across a particular row or column using threshold detection. The transimpedance amplifier acts as the interface between the row and column summing lines and the off-chip ADC and FPGA by converting the single-ended current signal to a differential voltage. Analog line drivers are used to tune the channel output impedance over a range of loading conditions (50Ω - 200Ω) presented by a variation in the Firewire lengths, shape, etc., all of which influence the load impedance presented to the ASIC output. At present, the ASIC is being measured in the lab in a full PET imaging system. In addition, data acquisition boards are being designed which interface the CMOS front-end chip with the ADCs and the Phase II FPGA [38]. The ASICs have been packaged for these boards in order to use all the pads on the chip. Future versions of the ASIC would seek to eventually integrate the RCA design with on chip digitizing of the signals and a compact package to allow it to be tightly coupled to SiPM array elements with techniques such as bump bonding. Also, time-to-digital converters would be explored to improve the resolution of the timing paths. The amount of data produced in modern PET scanners continues to grow as detectors are integrated in silicon both reducing the size while increasing the speed. As a result of the miniaturized detectors and the increased density of the detector arrays, the amount of data, and the number of channels coming from the detection array

continues to scale upward. This leads to corresponding increase in the number of cables connected to the back end PC, where the image reconstruction is being performed. A possible solution can be to remove these cables completely and instead, transmit the data wirelessly from the ASIC to the back end image reconstruction hardware. Our program plans to realize this vision eventually providing seamless high-data rate wireless connectivity between the detection array and the digital backend where signal progress will take place. This could have the potential to transform PET Imaging Systems as we know them.

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