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A Robust Power-Scalable Transmitter Architecture for Wireless Body Area Networks

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Abstract

A Robust Power-Scalable Transmitter Architecture for Wireless Body Area Networks

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Chair of the Supervisory Committee:
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In this dissertation, an RF transmitter is presented that uses closed-loop PLL- based BFSK modulation and is reconfigurable for both the MedRadio and 433 MHz ISM bands. A power efficient class-C amplifier is utilized and the design methodologies for designing a highly efficient and low-power amplifier are discussed in detail. The mediocre PVT performance of the classical implementation of the class-C power amplifiers is a major cause of concern that inhibits widespread usage of these types of amplifiers. An open-loop ultra-low power calibration loop is designed to deal with process, temperature and voltage drifts. Also introducing for the first time, a digitally tunable power amplifier core with a single reconfigurable matching network is able to vary the output power level from -12 dBm to -2dBm while maintaining similar efficiency numbers. A completely integrated PLL is used in the frequency synthesis. BFSK modulation is performed by switching the divide ratio of a dual modulo divider and a low-power NMOS delay-based ring-VCO acts as the oscillator. Several performance records are achieved: (1) The PA realizes a peak efficiency of 47% in the high-

power (ISM) (-2 dBm) mode and 43% (33%) in the MedRadio -12 dBm (-16 dBm backoff) modes. (2) The PLL dissipates only 72 μW with a phase noise of -111 dBc/Hz @ 1 MHz, and (3) the overall transmit efficiencies are 29% and 17% for the -12 dBm and -16 dBm backoff levels for the MedRadio band and 44% for the ISM (433 MHz) bands.

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Life is a journey shaped by people who you come in contact and I believe every single person paves the path. Thanks to all who have done so during my Ph.D life and in general!

Dedication

To my mom, Shanti Natarajan

1. Introduction

Ultra low power sensors are required and used everywhere. Medical sensors enable wireless monitoring of patient's vital signs such as ECG, EEG, ECog etc. The key challenge in integrating radios on the sensor platform is power efficiency of transmit and receive circuits, in particular the power-amplifier (PA) [1]. This efficiency of the power amplifier is further reduced at low output powers with the best-in-class PAs having a maximum efficiency of 30% @ -16dBm [3][4][5] . Further the ability to reconfigure the output power according to the wireless standard is critical for hardware adaptability in this dynamic market. FCC defined MICS and US-WMTS are two examples of wireless standard specifically for medical purposes and define maximum EIRPs of -16dBm and 5dBm respectively [2]. Apart from the medical areas where the low power sensing is prevalent, the broad classification is shown in Figure 1-4 and is classified into medical, environmental and vehicular.

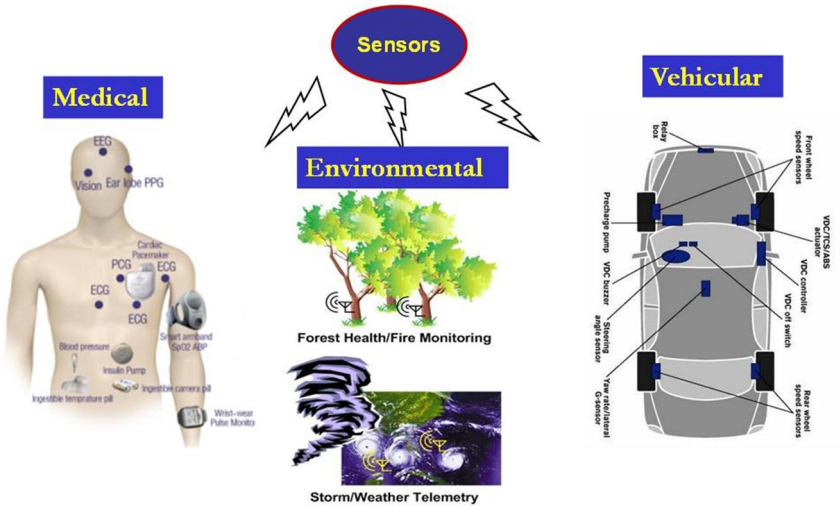


Figure 1-1: Sensors Application Areas

Medical sensors are used to monitor a person's vital signs such as ECG, EEG, O_2 Stats etc. Vehicular sensors are used in parking, braking and accident collision systems among a host of other things. Sensors deployed in the nature have a variety of uses including forest fires, animal tracking to name a few. With recent advancements we have been rapidly developing the ability to continuously monitor our environment and our health thanks to the increasing integration opportunities and decreasing costs and form factors derived from scaled CMOS technologies.

Increasingly sensor platforms are beginning to integrate wireless communication modules within them. Historically with the absence of these radios, communications had to be wired. This can become very cumbersome given the application. For example, a patient having his EEG taken has close to a 1000 wires from all the sensors attached to his head as shown in the Figure 1-2.

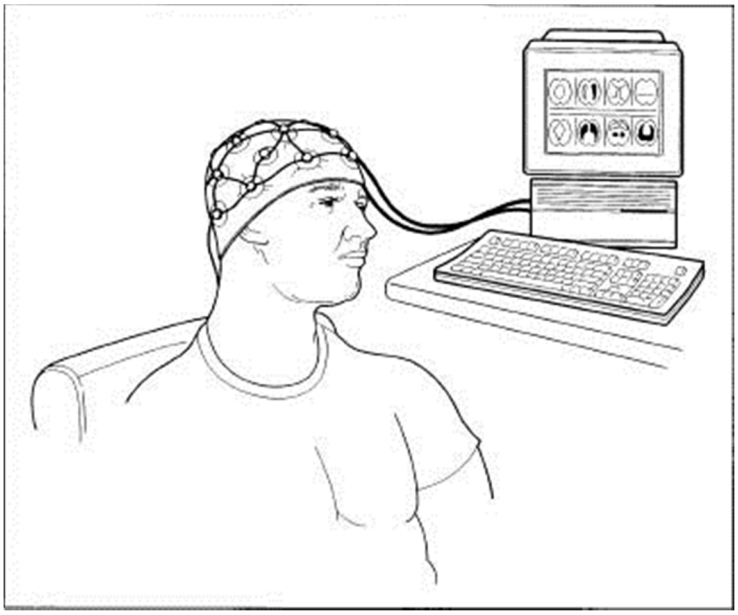


Figure 1-2: EEG Measurements

This is un-wieldy and causes a lot of issues when the patient has to move about the care center.

A typical sensor platform has a number of components on them. This includes the actual sensor which does the physical parameter sensing with the required power control and memory. The radio on the platform is used to communicate with the external world wirelessly. It consumes the maximum energy among all the other circuits. The power is usually derived out of a power source, usually a battery or probably even energy scavenging circuits. So low power circuit has become very critical to make these sensors last for a while!

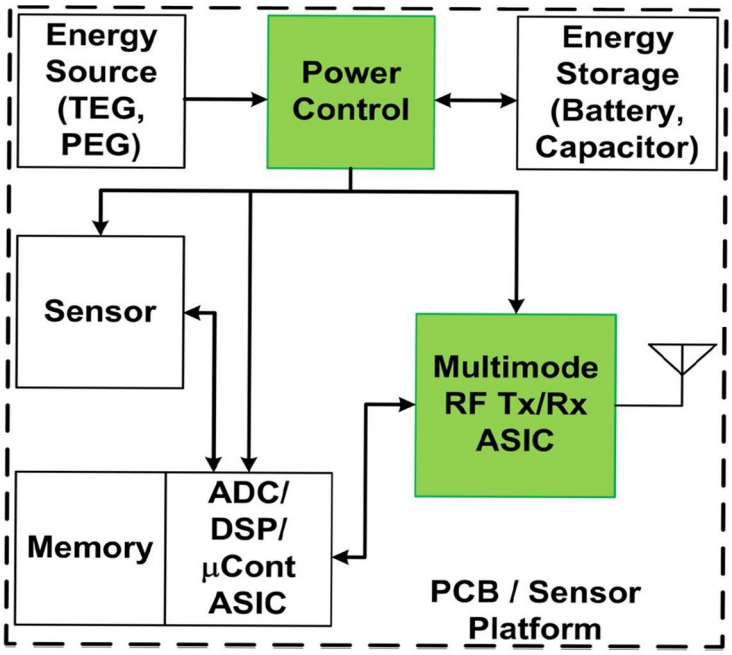


Figure 1-3: Sensor Platform

Among the applications mentioned above, body sensor networks (BSN) provide quality-of-life improvements for elderly and chronically ill patients by enhancing their mobility by removing the tethers associated with traditional medical telemetry systems. BSNs can also be used to enhance the effectiveness of training for athletes, and advance the diagnosis of impending health-related issues among aging and impoverished populations. The burgeoning use of BSNs has sparked regulatory agencies and standards associations to form task groups to establish

regulatory standards for reliable wireless links. For example, the US Federal Communications Commission recently created the *MedRadio* standard and the IEEE formed the 802.15.5 task group [1] for low-power wireless mesh networks.

A BSN comprises several wireless sensor nodes organized in a mesh network that communicate with a central control unit (CCU) (e.g., a smart phone) as shown in Figure 1-4.

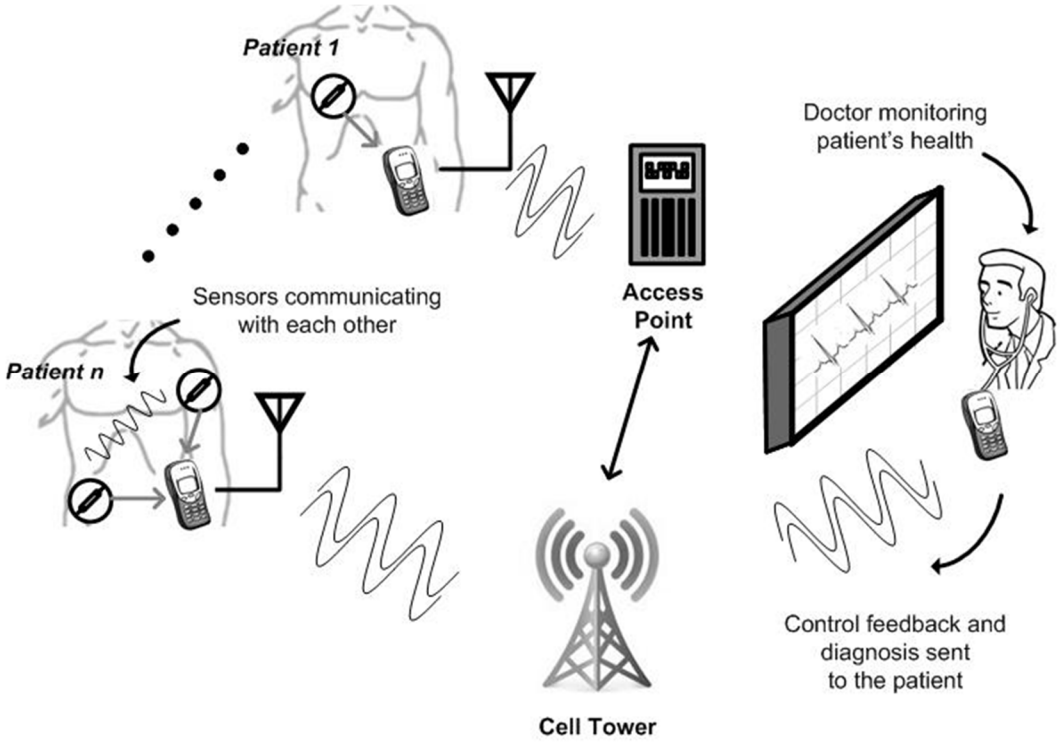


Figure 1-4: BSN Communication Model

The figure shows the communication model for the body worn sensors. All the sensors have a radio on them which they use to talk with the external world. The connection is usually established by a cellphone or a PDA within 10-50m of the sensor. This model gives patients an untethered connection with the central monitoring system. This enables the doctor to remotely

monitor the patient's health and can send real time information via the communication channel.

BSN enable point to point care for patients. There are far-stretching applications that can be realized by the sensor networks. Un-tethered monitoring of patients in medical care centers is seen as a huge advantage for both the patients and the doctors monitoring them. Un-tethered monitoring is preferred because of 2 reasons. Imagine a recovering patient under the supervision of a doctor. At the beginning of his care period, there is not a lot of moving around, hence the sensors can communicate using a short-range radio network and save on power. This is typically done using a standard like MedRadio where the EIRP (Effective Isotropic Radiated Power) is limited to -16dBm, hence having a short range of output power. When the patient is recovering, the doctor advises the patient to move around. Once the patient is more mobile, he might want to step away from the central monitoring station. Now the sensor must still communicate with the doctors but the limited output power from the MedRadio standard limits the mobility to a few meters before the communication link is broken. In such a situation, it is advantageous to have a re-configurable radio which can switch from a low-power short-range MedRadio standard to a standard that supports higher output power for achieving long-range communications. Seamless configurability of the transmitter will ensure that this model of the BSN is achieved.

Figure 1-5 tries to explain this in a bit more detail. When near the care-giver, the communication channel used is the MedRadio (400MHz), EIRP = -16 dBm standard. When moving further away, the communication channel is ISM (433MHz), EIRP = 30 dBm.

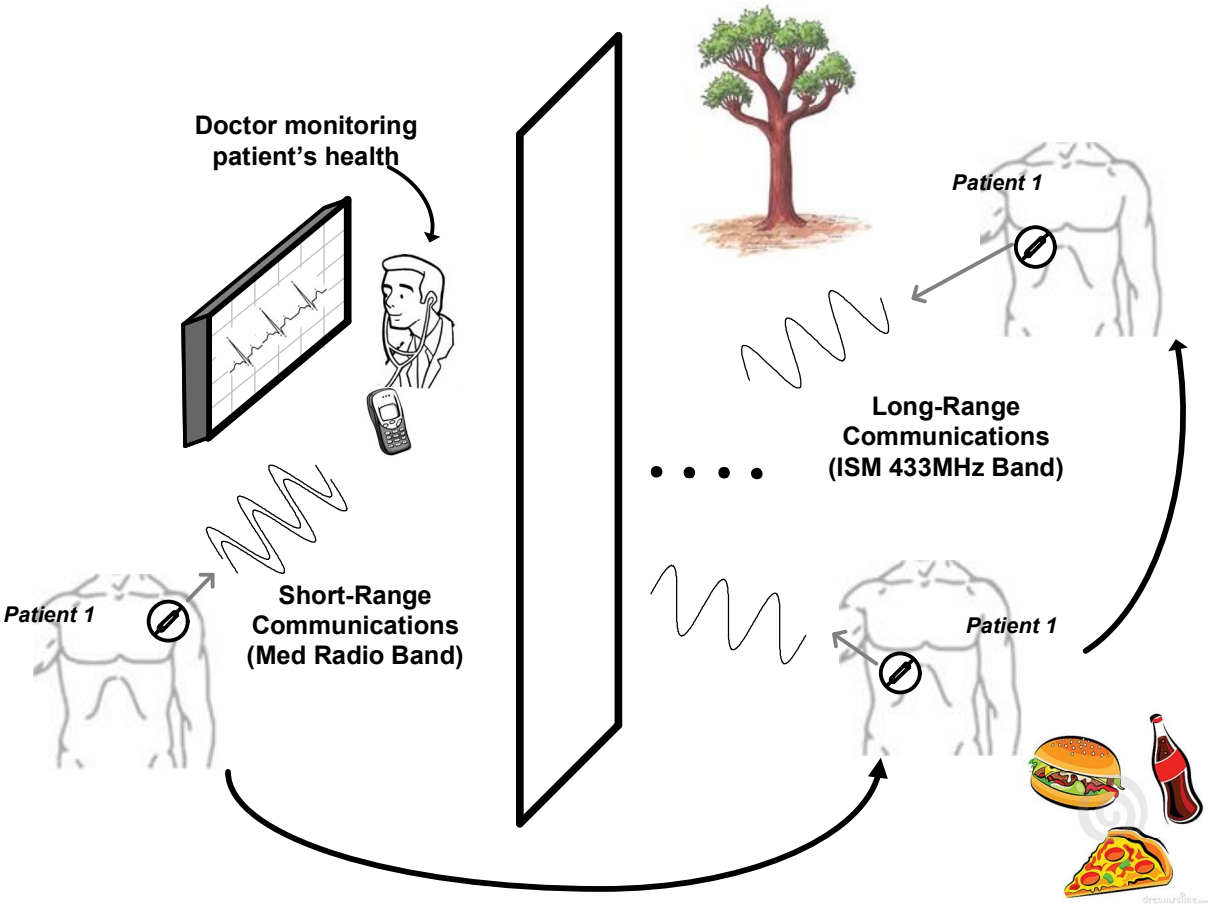


Figure 1-5: Reconfigurable Power Amplifier Use-case I

Wireless sensor network security is a challenging task because of the nature of the shared communication medium and also the limited resources associated with a low-cost sensor network. Wireless technologies are commoditized which gives the ability to adversaries to purchase their own sensor devices and gain access to the communication data between other sensors by running themselves on a monitor mode. Despite of the application of network security protocols, this wireless medium will always be vulnerable to attack.

The adversary targets the radio-communication channel. There are two main methods of causing a security breach. One is the more traditional denial of service (DOS) wherein the

attacker fills up the user domain and kernel domain buffers. The second method of attack is on the PHY (Physical) layer and is called Jamming. In this method, the shared nature of the wireless medium is exploited to prevent devices from communicating or receiving. Typically, the jammer's objective is to deny the reception of communication by spending as low a power as possible. Such an attack is mitigated by using spread-spectrum technologies. With the exception of military, these types of techniques are not employed in commercially available off-shelf transceivers for the main reason of cost. Unfortunately, the MedRadio or Zigbee standards use carrier sensing to multiple access as the medium access control (MAC). This becomes a soft target for the jammers who disregard the MAC and continually transmit on the wireless channel. The existence of the adversary in the wireless channel will prevent legitimate users from commencing the MAC operations and can results in packet loss, collision or even jam transmission. These MAC and PHY layer attacks are critical security threats and pose to be a big vulnerability in ubiquitous presence of these wireless sensor nodes [6] [7] [8].

Two methods have been proposed in literature for prevention of attack on the PHY and MAC layers. The first one involves avoiding the jammer in spectral or spatial sense and can be achieved by changing channel allocations or possibly move to another frequency band if the standards allow for it. The second strategy involves competing directly with the jammer by adjusting the transmission power levels. The Figure 1-6 below shows this in a pictorial fashion.

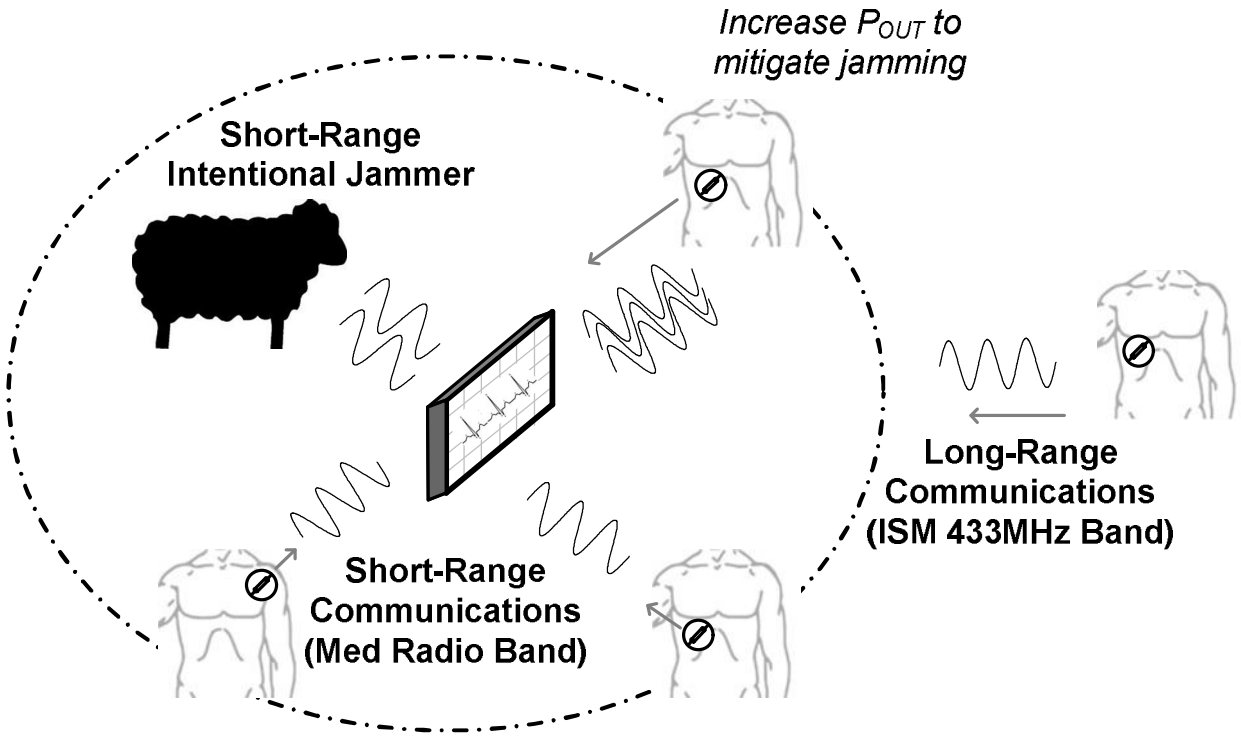


Figure 1-6: Reconfigurable Power Amplifier Use-case II

For BSNs to reach their full potential, individual sensors must be minimally invasive to the individuals using them. In the case of implantable devices this means they must operate from the same battery for many years to minimize the surgical procedures necessary to implant them. Energy efficiency is, therefore, of utmost importance. Ultra-low power wireless sensors are critical to autonomous operation. They must be minimally invasive and operate from the same battery for many years in order to minimize surgical procedures of replacing them each time. Energy efficiency is of utmost importance. Although the power amplifier (PA) operating as an antenna interface is not the dominant consumer of energy in a low-power wireless network, its energy usage is still significant. To this end, substantial energy can be saved with careful design of the transmitter and PA.

A class-C PA for use as an antenna interface in BSNs is introduced. It achieves high efficiency for a PA that operates in the *MedRadio* frequency band, and it promises to provide even higher efficiency at lower output power levels. This is a natural application for class-C amplifiers. Also, robustness to PVT variations is critical for a class-C operation mode reason being the output power is dependent on the threshold voltage of the input pair. The PA is fabricated in a 0.13 µm RF CMOS process for operation in the 400 MHz *MedRadio* band. It achieves a measured peak output power and drain efficiency of -4 dBm and 43%, respectively [13].

The idea of a high-efficiency low-power class-C PA is extended and a re-configurable PA is designed and fabricated in the IBM 130nm CMOS process. The PA can be configured to be in two power modes. The high-power long-range mode transmits a maximum of -2 dBm output at an efficiency of 47% while the low-power short-range mode transmits a maximum of -12 dBm output at an efficiency of 43%. An on-chip PLL provides closed-loop modulation of the baseband data for BFSK transmission. The PLL consumes 72 µW and achieves a closed-loop bandwidth of 80 KHz, a phase noise of -111 dBc @ 1 MHz offset and -133 dBc @ 10 MHz offset with a reference spur of -48 dBc. On-chip PVT variations are calibrated using an open-loop technique. The output power drift over temperature and supply variations are calibrated and the PVT calibration technique reduces output power variations by about 2.5X compared to conventional class-C PA designs.

2. Power Amplifier Basics

In this chapter basics of power amplifier are introduced. A basic background on transmitters operating in the *MedRadio* or the MICS band is given. Finally a class-C amplifier is fully investigated and its operating principles are discussed.

2.1. Power Amplifier Background

Power amplifiers are used in the transmitter to drive a signal to the antenna at the desired output power level. The transmitted power level is typically set by the communication system which takes into consideration factors such as channel loss etc., and also to ensure that the receiver is able to sense and recover the transmitted signal. The transmitted power level varies significantly depending on the application. Figure 2-1 shows the wide variation in the transmitted output power.

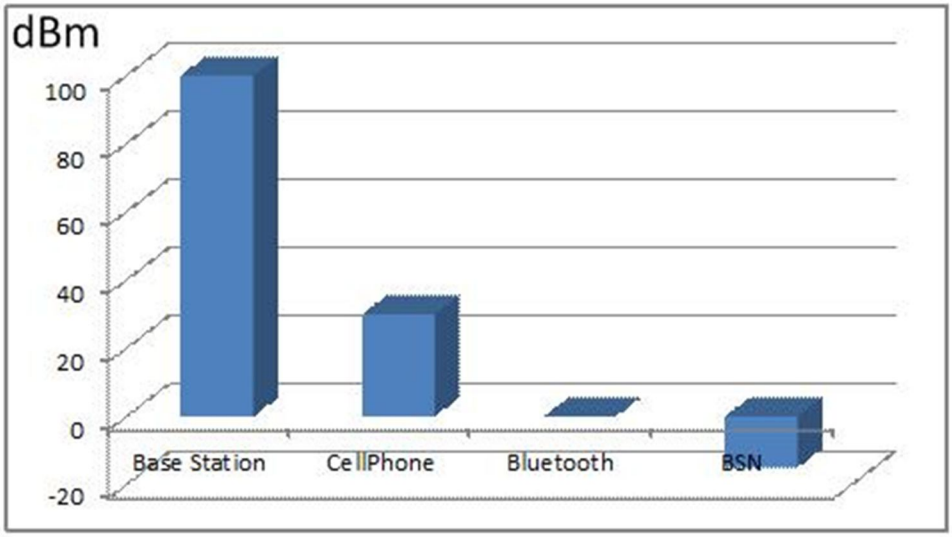


Figure 2-1: EIRP Variation

The power transmitted from the base stations varies from hundreds of watts. For wireless communication systems such as cellphone networks and WI-FI, the output power varies from hundreds of milliwatts. Applications such as Bluetooth and BSN transmit a much lower output power.

Radios embedded in the sensor are powered by a small form factor battery like a coin or button cell. The PA which is responsible for delivering the power to the antenna essentially converts the DC power from the battery into the RF power. This power conversion is lossy and as a result, PA will consume power which is over and above what it delivers. The PA's efficiency is a metric that quantifies this key parameter and is given by:

$$Efficiency = \frac{Power\ Delivered\ to\ Load}{Power\ Consumed\ from\ Battery} \quad (1)$$

This is a key metric when it comes to radios used in body area networks as this power directly reduces the battery life.

2.2. Types of PA

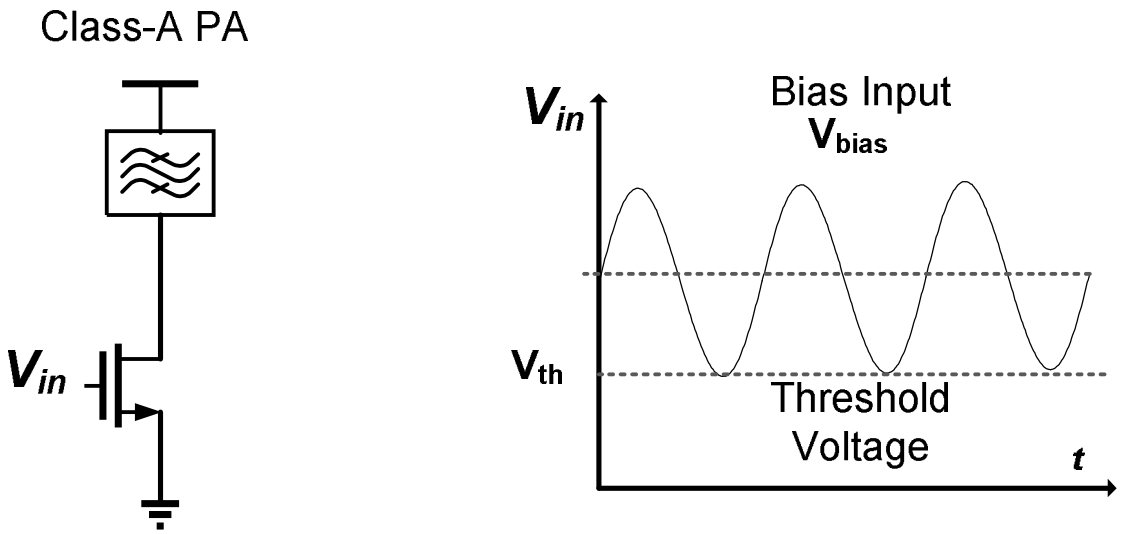
PA's are generically classified into 2 categories depending on whether the transistor acts as a current source or a switch [1]. The former is called as linear class of PA's and latter as the switch mode PA. Linear and switch mode PAs are further classified into categories. It is informative to delve into a brief background for the linear PA.

2.2.1. Linear PA

The term 'linear' in the title is a misnomer to a certain extent. This is due to the fact that the relation between the input and the output need not necessarily be linear. But this does not

preclude the fact that the transistor in these types of PA operates in the saturation region where the output is amplified directly in proportion to the magnitude of the input. Consequently there is a relation between the input signal and the output, however (non)linear it maybe.

The linear PA has an inherent trade-off between linearity and efficiency. The most linear PA would be the one which conducts a current irrespective of the input signal. For this to be true, the DC bias has to be at least higher that the input signal swing. As a result of dissipating this fixed amount of power even when the signal is absent, these types of amplifiers have a poor efficiency. This type of the amplifier is called as a class-A PA. As shown in the Figure 2-2, the bias input voltage, V_{bias} is such that it keeps the device from entering into sub-threshold values for all values of the input signal swing. The output signal swing is also shown in the figure.



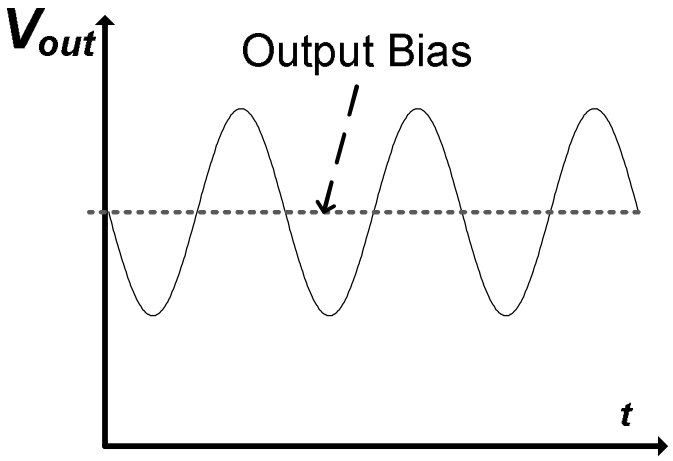


Figure 2-2: Class A Power Amplifier Operation and Voltage Swing

The output bias voltage is usually close to VDD because of the output matching network. In order to achieve maximum efficiency, the output voltage swing is optimized to be around VDD. Thus the maximum efficiency of such a configuration can be calculated.

I_{avg} = Average current of the PA,

The maximum efficiency is defined as

$$\eta = \frac{0.5 * V_{dd} * I_{avg}}{V_{dd} * I_{avg}}$$

$$\eta = 50\%$$

This is the theoretical limit of efficiency for the Class-A linear amplifiers. Practical implementations of the linear PA suffer loss from various mechanisms. To begin with, the active device (NMOS in this case) is lossy because of various parasitic resistance and capacitance associated with them, thus introducing some kind of resistive loss of the drain currents.

Secondly the output matching network losses accounts for a few dBs of output power loss because of low-Q on-chip inductors. Even though the relative Q of the metal capacitors implemented on-chip is high, the loaded Q of the output matching network degrades the signal before transmission to the antenna. Finally, there are practical limits on the output voltage swing. The assumed voltage swing of V_{dd} is not possible because the MOS transistor will no longer be in the saturation region and will enter a more linear region where the magnitude of the gain drops and hence introducing non-linearity in the output. Practical implementation limits the efficiency close to 25% and even lower for low-power output.

The next logical design attempt would be to make the active device to not conduct current for the entire input cycle. Class-B amplifiers are an interesting extension of controlling the transistor 'on-time' [15].

Consider the class-B amplifier shown in the Figure 2-3:

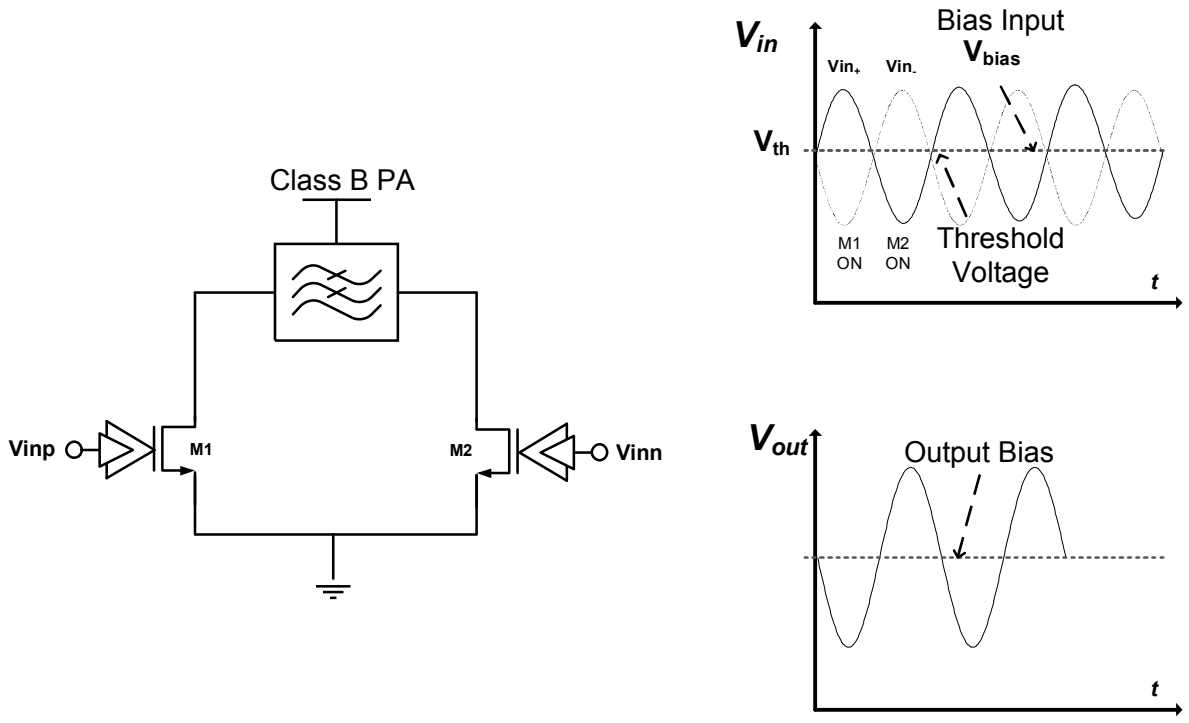


Figure 2-3: Class B Power Amplifier Circuit and Voltage Swing

The class-B amplifier is also known as the push-pull amplifier because of the way the transistors are arranged. The transistors M1 and M2 amplify during either the positive or the negative cycles of the input signal swing. The bias voltage V_{bias} is adjusted exactly to the threshold voltages of the active devices. The input signal swings the transistor above and below the transistor's threshold voltage V_t. M1 is turned on and is linear during the phase when the input signal swings above V_t. During the negative, phase M1 is turned off (leakage current exists) and M2 is now amplifying. The output is taken differentially; hence it is a continuous sinusoidal output. Owing to the fact that the devices conduct for only one half of the cycle and there quiescent current is reduced, the efficiency of the class-B amplifier is higher than the class-A counterpart. Theoretical limit of the efficiency is [15]

$$\eta = \frac{\pi}{4} = 78\%$$

A basic implementation of a class C amplifier is shown in Figure 2-4.

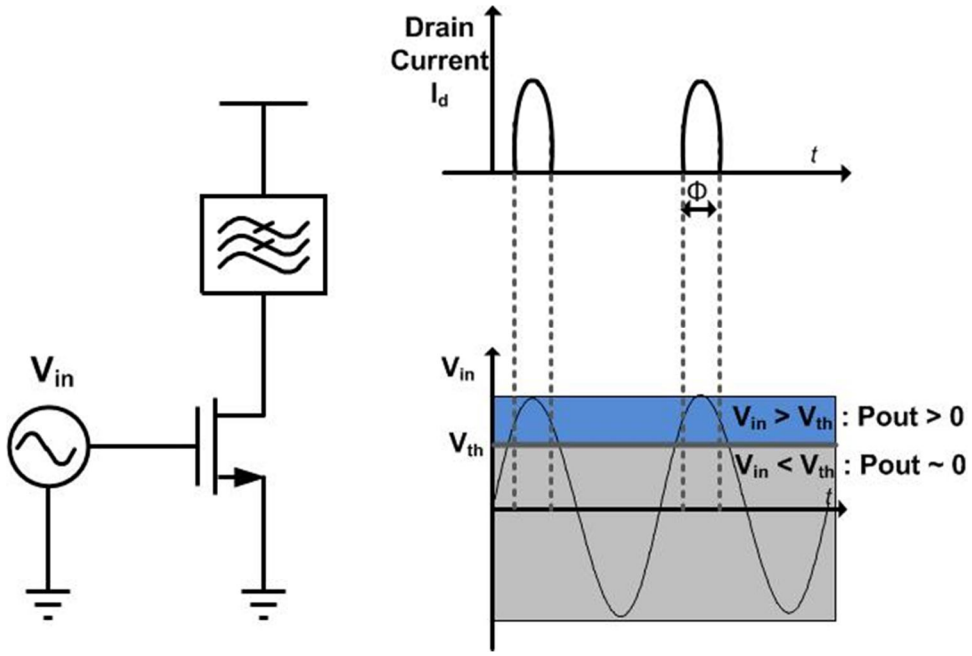


Figure 2-4: Class C Power Amplifier

The active device in the amplifier is biased below its threshold voltage (in some cases, the bias can also be negative). The input signal swing is chosen such that it turns the device on for a certain fixed fraction of the cycle which is termed as the conduction angle Φ. As the signal turns the device on, it sets up a finite current through the device. This current passes through the filtering network which chooses the fundamental frequency. This basic analysis shows that for transmitting similar output power, the class C has a better efficiency as compared to the other linear amplifiers.

It would be instructive to plot the output power and efficiency as a function of the conduction angle. Consider the circuit shown in Figure 2-5

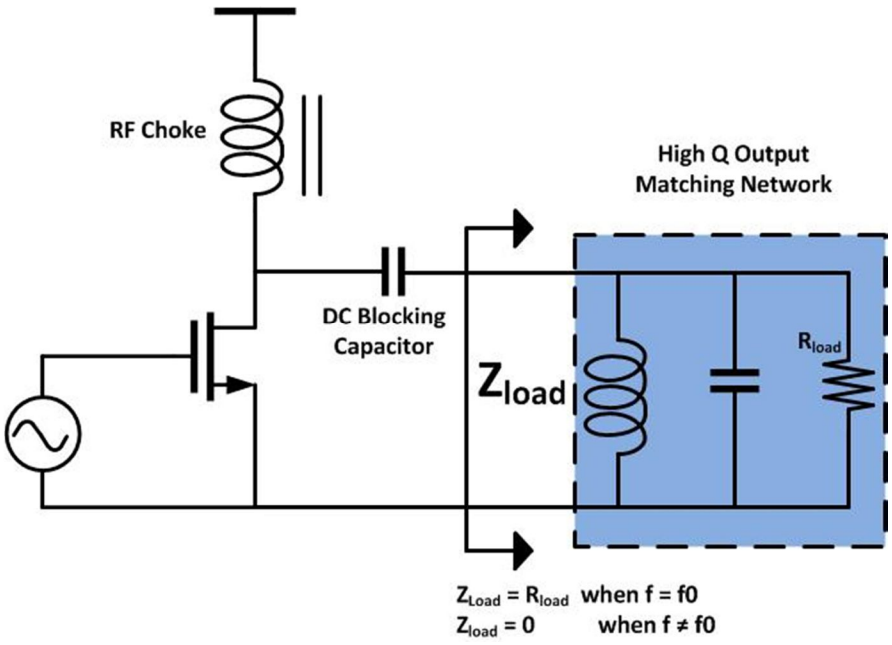


Figure 2-5: Idealized Class C PA

Harmonics of the load are shorted and generate no voltage. The drain voltage is approximated by a sinewave, the magnitude of which is set by the load resistor. Further assuming that the maximum voltage swing is generated corresponding to the peak current I_{pk}. The RF fundamental power is:

$$P_1 = \frac{V_{DC}}{\sqrt{2}} \frac{I_1}{\sqrt{2}} \quad (2)$$

I_1 corresponds to eqn. 9 and the DC power consumed is given by

$$P_{dc} = V_{DC} I_{DC} \quad (3)$$

The efficiency is given by

$$\eta = \frac{P_1}{P_{dc}} \quad (4)$$

Figure 2-6 shows the variation of efficiency and output power as a function of the conduction angle.

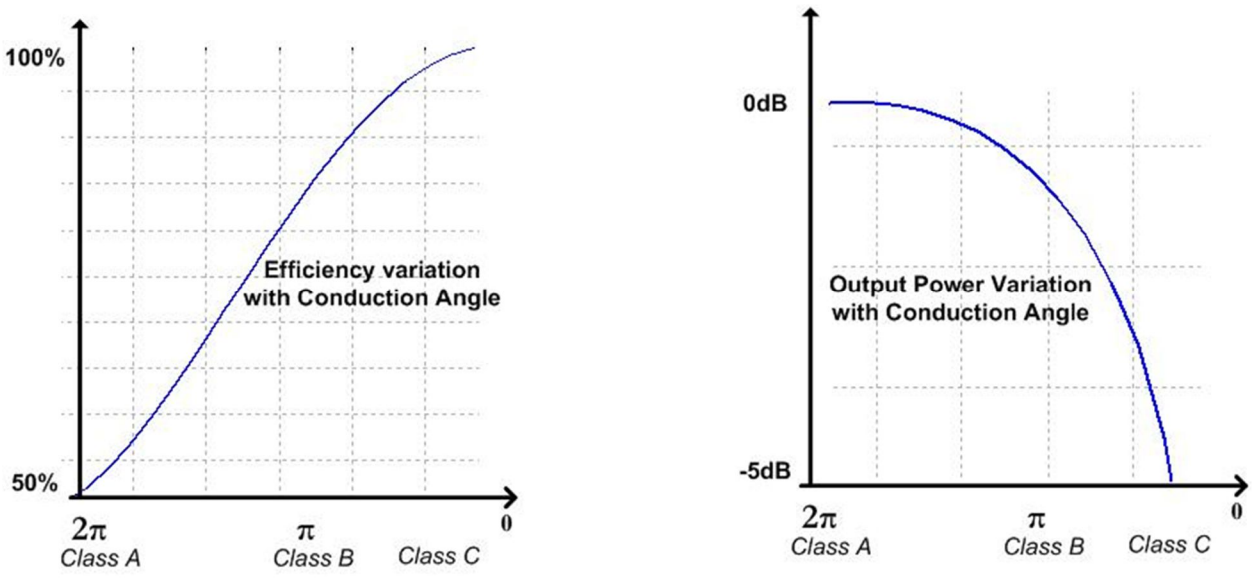


Figure 2-6: Efficiency and Output Power Variation VS Conduction Angle

These plots reveal an important property of the class C amplifiers. The class C condition shows a rapidly increasing efficiency with reducing conduction angles but accompanies with significant reduction in the RF output power. This is the primary reason why class C amplifiers are the most naturally suited to function as power amplifiers in BAN, whose EIRP is limited to ~0dBm.

As the conduction angle reduces, the transmitted power reduces with an increase in the efficiency. The essence of this discussion is well captured in the Figure 2-7 shown below.

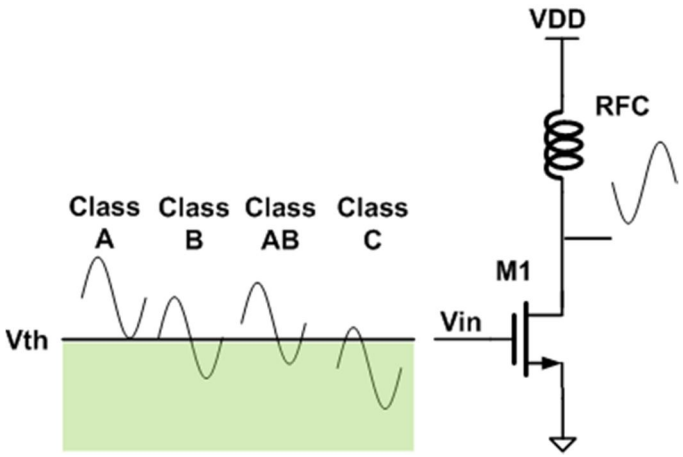


Figure 2-7: Operating Principles of Linear Power Amplifier

The table 1 summarizes the different classes of PA and their effective conduction angle. Theoretical maximum efficiencies are also mentioned as a comparison point. As mentioned before, efficiency is sacrificed for linearity among the different linear PA.

Table 2-1: Linear PA Classification

Amplifier	Conduction Angle	Maximum Efficiency
Class A	$\Theta_c = 360^\circ$	50%
Class B	$\Theta_c = 180^\circ$	78.5%
Class AB	$180^\circ < \Theta_c < 360^\circ$	50% - 78.5%
Class C	$\Theta_c < 180^\circ$	100%

2.2.2. Switching PA

A switch-based amplifier such as Class-D and Class-E power amplifiers uses transistors as switches rather than linear amplifiers. Recalling the discussion of the g_m-based power

amplifiers, there is power consumption whenever there is simultaneous non-zero current and non-zero voltage in the transistor. If the product of voltage and current in transistor becomes zero, however, there is no loss in the transistor and the efficiency will be 100%. The trade-off is fixed output power since the operation of the switch-based power amplifier is based on the switch, instead of transconductance which generates output power that changes linearly with the input signal. The most popular of switching PA are class D, E, F and inverse class F.

Class D PA is a push-pull type of amplifier where the current is steered between the device and the load depending on the position of the switch (Figure 2-8). All other frequency components other than ω_0 will see a high impedance assuming ideal filter and matching networks. Intuitively, power will be delivered to the output only at the fundamental frequency, ω_0, and there will be no other power consumption at other frequencies. Consequently, overall efficiency will be 100%, if the load impedance including the filter is purely resistive (Figure 2-9).

Class E PA uses soft switching to reduce any power consumed by the active device. It is a widely used architecture where high efficiency is required when transmitting high output power. A simple class-E amplifier is shown in Figure 2-10**.** The transistor M1 switches current into the output load, R_{out}, through the matching network. The product of voltage and current at the drain of the transistor is ideally zero, thereby achieving a theoretical efficiency of 100%. Different from the class-C amplifier, a class-E amplifier delivers a constant and high output power through the use of a switch instead of the transconductor [22] [23].

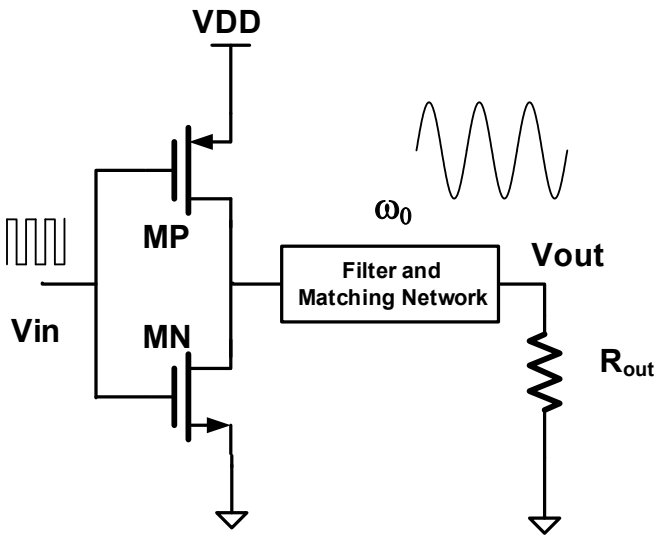


Figure 2-8: Class-D power amplifier

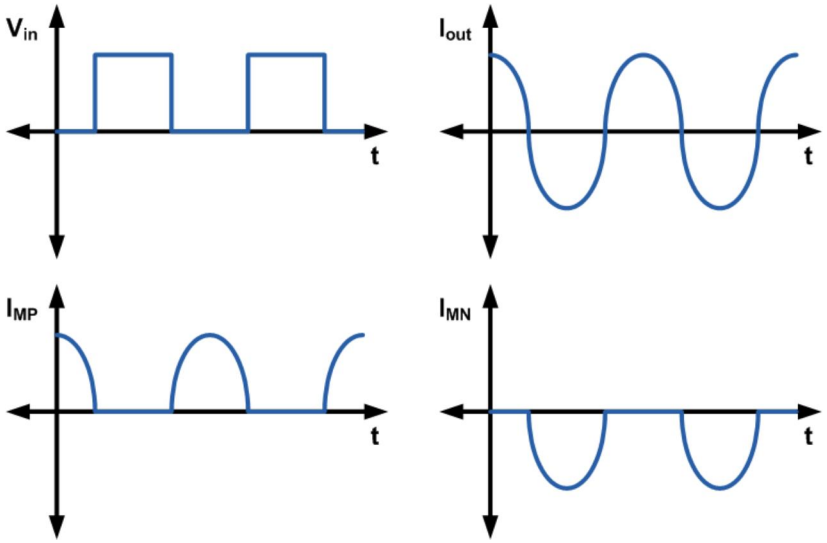


Figure 2-9: Class-D Amplifier Waveforms.

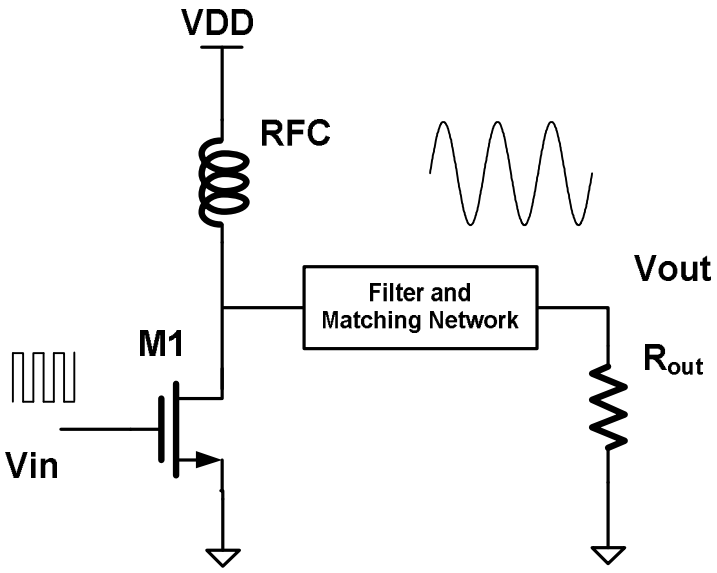


Figure 2-10: Class-E power amplifier

The output matching network is tuned to achieve this artifact of switching. The theoretical maximum efficiency can reach a 100% as in the case of Class-D [18]. Further references of these types of switching amplifiers can be found in [16][17].

In the following section, detailed analysis and design of a class-C power amplifier is presented.

3. Design and Analysis of Class-C Power Amplifier

Traditionally, a class-C PA was designed using theoretical analysis which considers the transistor as an ideal transconducting device, converting input voltage swings to output current at the required RF frequency [19] [20] [21]. As we move towards smaller nodes, a more realistic design approach is needed which considers the drain current variation with drain voltages and other second order effects. Also, controlling of the conduction angle with the gate voltage V_{RF} and drain voltage V_{DS} and threshold voltage V_{tN} is important for output power and efficiency. Consider the simple representation of the different amplitudes of input voltage swing and its effect on the conduction angle. The conduction angle is defined as the ratio of the time for which the input signal swing is higher than the threshold voltage V_{tN}. There are two ways to change the conduction angle for a fixed transistor size. First method is by changing the input voltage swing. As the input voltage swing amplitude increases, the conduction angle increases. Second method is to adjust the input signal bias. The RF signal sits on top of the bias-voltage V_{BIAS} and swings above and below it with amplitude equal to V_{RF}. Same conduction angles can be obtained for 2 pairs of (V_{RF}, V_{BIAS}). With a lower V_{BIAS} we expect a higher input signal swing, V_{RF}, to achieve the same conduction angle. Similarly, with a high V_{BIAS}, this is translated to a lower required input RF signal swing, V_{RF} Figure 3-1. This essentially transfers the burden of the power budgeting to either the input signal driver or the PA core. Obviously, a higher RF swing driving the PA core, would mean that more power is spent in the driver stage. On the other hand, more DC bias, translates to higher static power consumption of the PA core. A noteworthy point is the essential separation of power budgeting schemes allows us to critically

design the PA for shaving off that extra few µWs of power which in context of transmitting 25 µW is critical for overall efficiency.

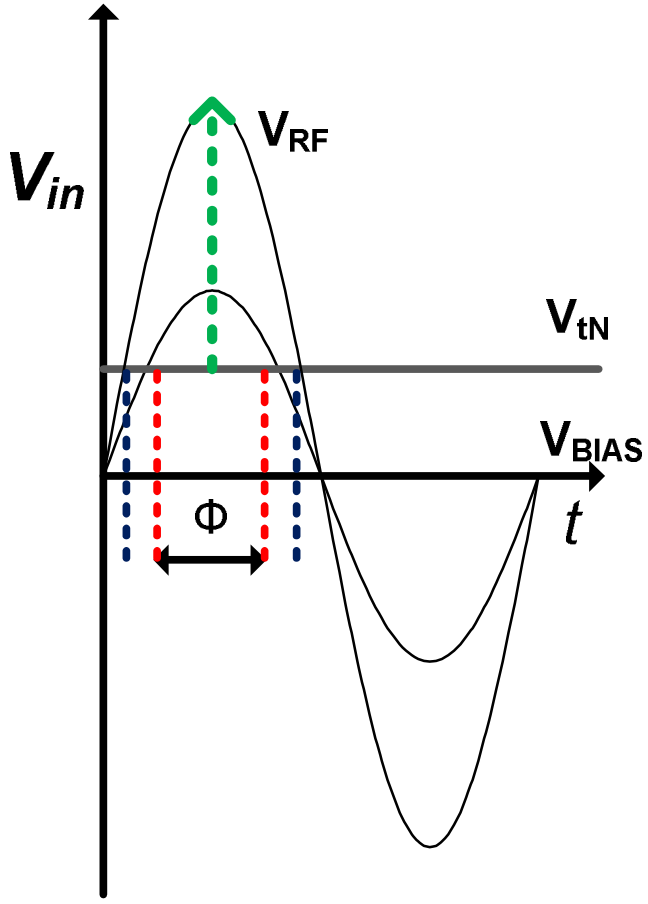


Figure 3-1: Conduction Angle Dependency

Figure 3-2 plots the variation of conduction angle θ, with (V_{RF}, V_{BIAS}). An instructive way to understand this plot is to trace out at a single value of (V_{RF} or V_{BIAS}). For example, with $V_{tN} – V_{DC}$, at 0.4V, higher the V_{RF}, higher the conduction angle θ. At V_{RF} = 0.45, θ = 55°, and at V_{RF} = 0.7, θ = 70°.

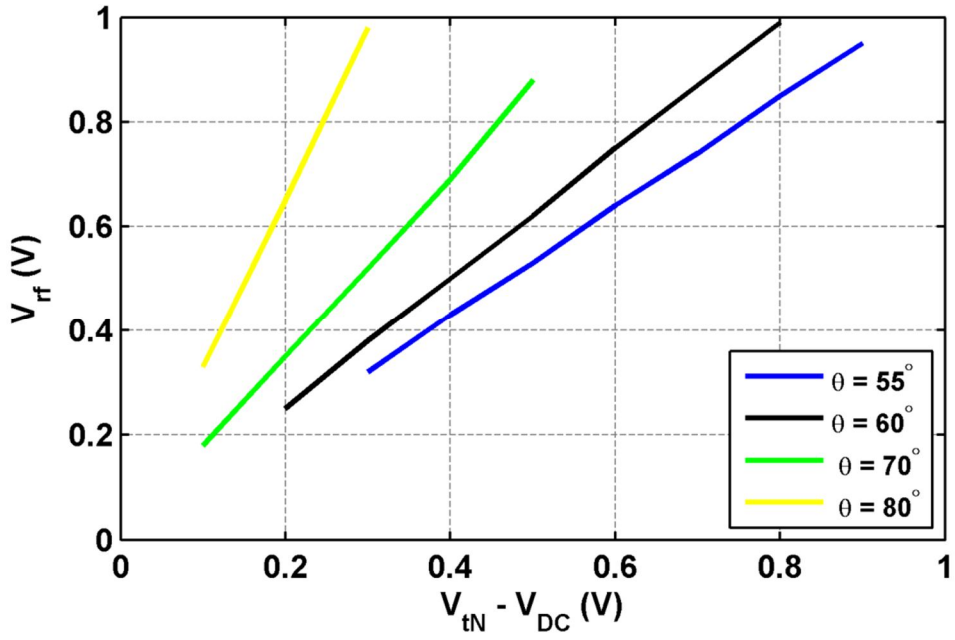


Figure 3-2: Variation of Conduction Angle with Voltages

We can define the gate voltage as:

$$V_{gs} = V_{bias} + V_{rf} sin(\omega t)$$

The output voltage is sinusoidal assuming the matching network filters the harmonics and is given by:

$$V_{out} = I_{out} R_{transform}$$

where I_{out} is the fundamental at the required RF of the output current waveform. $R_{transform}$ is converted impedance by the matching network. Note that for transmitting low output power, the output 50 Ω is transformed to a higher value.

Among the many definitions of the output efficiency of an amplifier, we define the total output efficiency of the amplifier as:

$$\eta_{total} = \eta_{intrinsic} + \eta_{OMN}$$

$$\eta_{intrinsic} = Transconductor\ Efficiency$$

$$\eta_{OMN} = Matching\ Network\ Efficiency$$

The transconductor efficiency is a measure of how well the output power is transferred to the output matching network (OMN) and is defined as:

$$\eta_{intrinsic} = \frac{I_{out}^2 * R_{transform}}{2 * I_{DC} * V_{dd}}$$

Where I_{DC} and V_{dd} are the DC bias currents and supply voltages.

An alternate way of looking at the efficiencies for reduced conduction angle is presented in [4] with rigorous mathematical analysis of drain currents and output voltages but the final result is reproduced here for simplicity. The theoretical drain efficiency of a class C amplifier is given by:

$$\eta = \frac{2\Phi - \sin 2\Phi}{4(\sin 2\Phi - \Phi \cos 2\Phi)}$$

The equation reveals that as the conduction angle Φ approaches zero, the efficiency reaches 100%. This has no physical significance as when the conduction angle is near zero, the output power and the gain simultaneously tend towards zero owing to the reason that the fundamental component of the drain current approaches zero value.

While it is obvious that the average/ dc component of the current waveform decreases when the conduction angle decreases, the variation in the fundamental component is more relevant for RF power transmission. Also, linearity of the PA is dependent on the harmonics generated. A simple Fourier analysis of the current waveform reveals the required information. Consider Figure 3-3

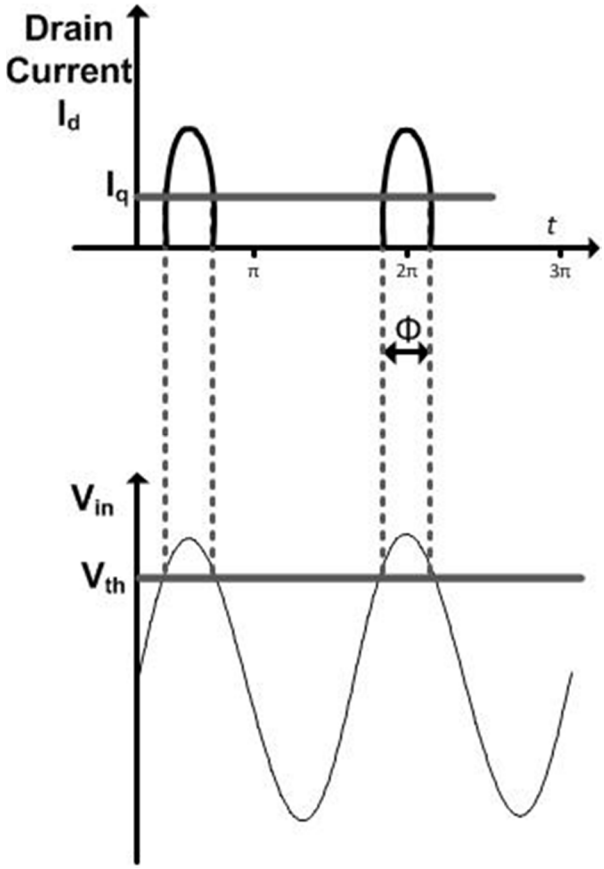


Figure 3-3: Drain Current Variation as a Function of Gate Voltage

The current waveform can be written as

$$i_d(\theta) = I_q + I_{max}\cos\theta \qquad -\frac{\Phi}{2} < \theta < \frac{\Phi}{2}$$

$$i_d(\theta) = 0 \qquad otherwise$$

$$\cos\left(\frac{\Phi}{2}\right) = -\left(\frac{I_q}{I_{max}}\right) \quad (5)$$

$$I_{max} = I_{pk} - I_q$$

The expression for the RF current can be written as:

$$i_d(\theta) = \frac{I_{max}}{1-\cos\left(\frac{\Phi}{2}\right)}\left(\cos\theta - \cos\left(\frac{\Phi}{2}\right)\right)$$

The DC component is given by

$$I_{dc} = \frac{1}{2\pi}\int_{-\frac{\Phi}{2}}^{\frac{\Phi}{2}} \frac{I_{max}}{1-\cos\left(\frac{\Phi}{2}\right)}\left(\cos\theta - \cos\left(\frac{\Phi}{2}\right)\right) d\theta$$

The magnitude of the nth harmonic is given by

$$I_n = \frac{1}{\pi}\int_{-\frac{\Phi}{2}}^{\frac{\Phi}{2}} \frac{I_{max}}{1-\cos\left(\frac{\Phi}{2}\right)}\left(\cos\theta - \cos\left(\frac{\Phi}{2}\right)\right)\cos n\theta \, d\theta$$

Simplifying the above equations,

$$I_{dc} = \frac{I_{max}}{2\pi}\left(\frac{2\sin\frac{\Phi}{2} - \Phi\cos\frac{\Phi}{2}}{1-\cos\left(\frac{\Phi}{2}\right)}\right)$$

The first harmonic is given by:

$$I_1 = \frac{I_{max}}{2\pi}\left(\frac{\Phi - \sin\Phi}{1-\cos\left(\frac{\Phi}{2}\right)}\right)$$

The current harmonics are plotted in Figure 3-4. Harmonics up to the 5th order are shown. As it can be noted, the levels of the harmonics increase rapidly as the conduction angle reduces.

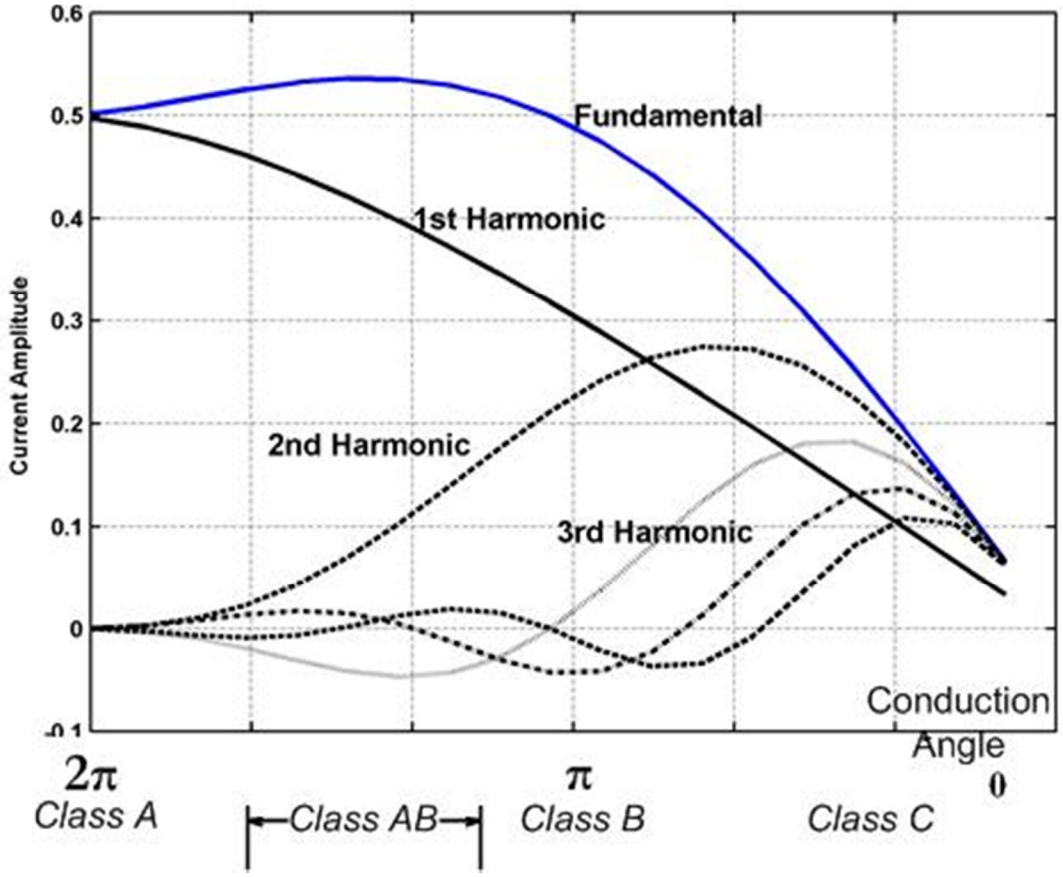


Figure 3-4: Drain Current Harmonics

This is the inherent tradeoff between linearity and efficiency. Class C PA typically operates with a conduction angle less than π/2 and the presence of harmonics necessitates a high Q output filter. For a BAN operating in the MHz range, we typically require large on-chip passives. Inductors are not native in CMOS processing and on-chip passive inductor have a maximum Q of ~10 at frequencies in GHz range. This makes the usage of off-chip inductor unavoidable but this has a mixed blessing in terms of the output load definition for class C amplifier, transmitting low output power. Typical impedance conversion ratios required at these frequencies are 100-150 which requires big inductors. Off-chip inductors in the order of hundreds of nH with Q ~100 are readily available.

Once we have the data of the required conduction angle and the drain current associated with that conduction angle chosen, we need to figure out the transistor characteristics required for producing the drain-current required. This is done using simulation in cadence using the PDK supplied in the CMOS process kit. We use IBM 130nm CMOS process for the design of the PA.

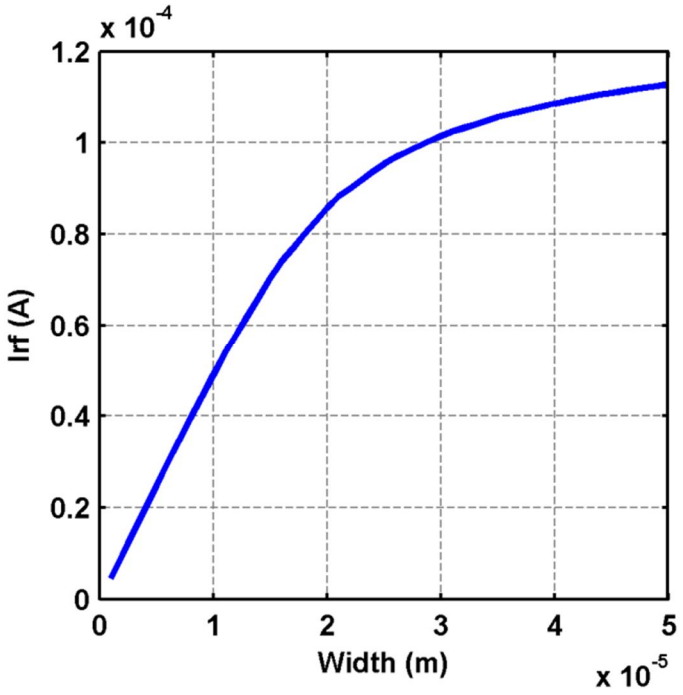


Figure 3-5: Current Density of a Transistor

For a fixed V_{RF}, V_{BIAS}, W/L ratios are swept. It is instructive to limit L to minimum. The Figure 3-5 shows the variation of the fundamental component of the drain current. Once the choice of W/L is made, we can check the theoretical transconductor efficiency. This is shown in the Figure 3-6. Careful designing the matching network is important for various reasons. The matching network supplies the VDD to the transistor core and also interfaces between the 50 Ω antenna and the transistor core. The next section talks about the design of a PA using the techniques described above.

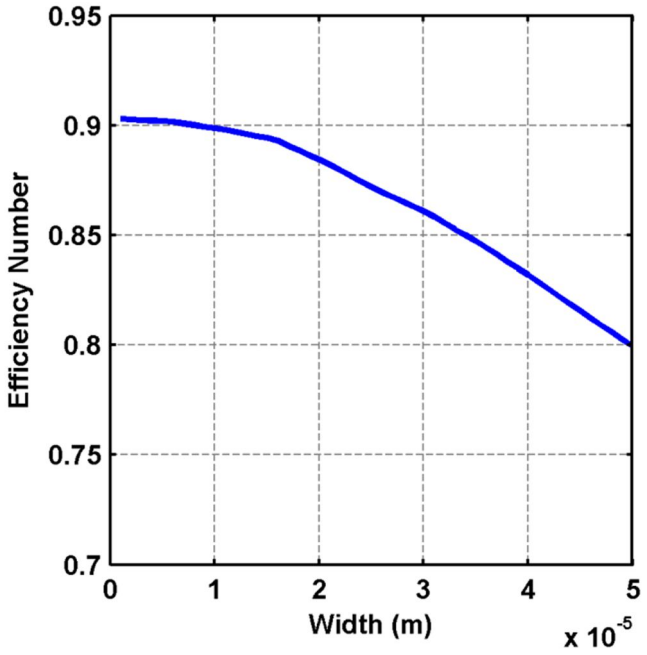


Figure 3-6: Efficiency Variation with Transistor Width

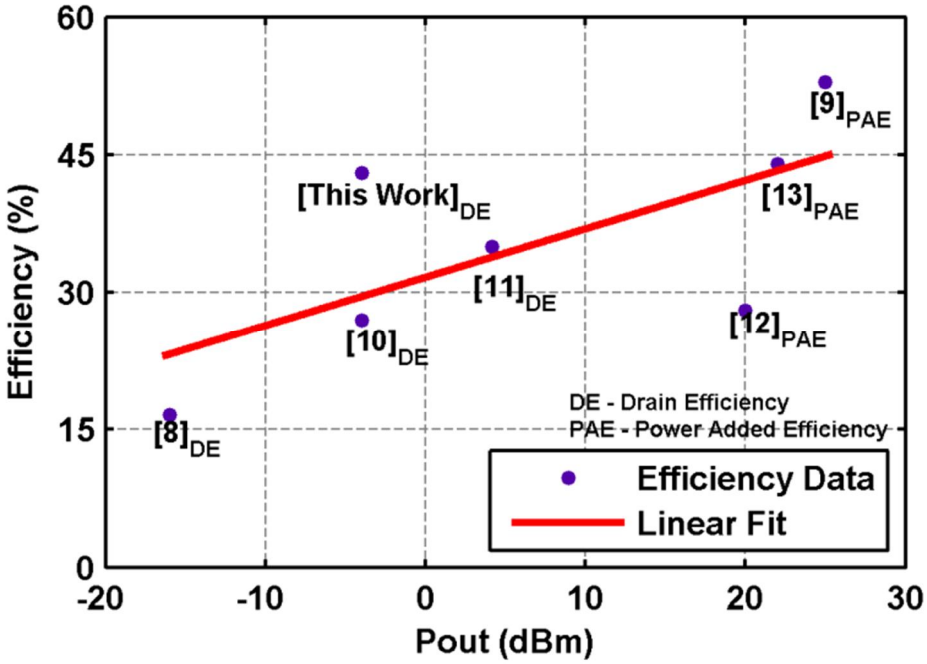


Figure 3-7: Efficiency comparison of recent power amplifiers

A class-C PA for use as an antenna interface in BSNs is introduced in this section. It achieves the highest efficiency reported to date for a PA that operates in the *MedRadio* frequency band, and it promises to provide even higher efficiency at lower output power levels. Figure 3-7 shows the efficiency of recent power amplifiers. By increasing the gate bias voltage, V_{BIAS}, relative to the NMOS threshold voltage, V_t, the PA (Figure 3-8) can be tuned to a output higher power level to operate in a more linear, class-A mode.

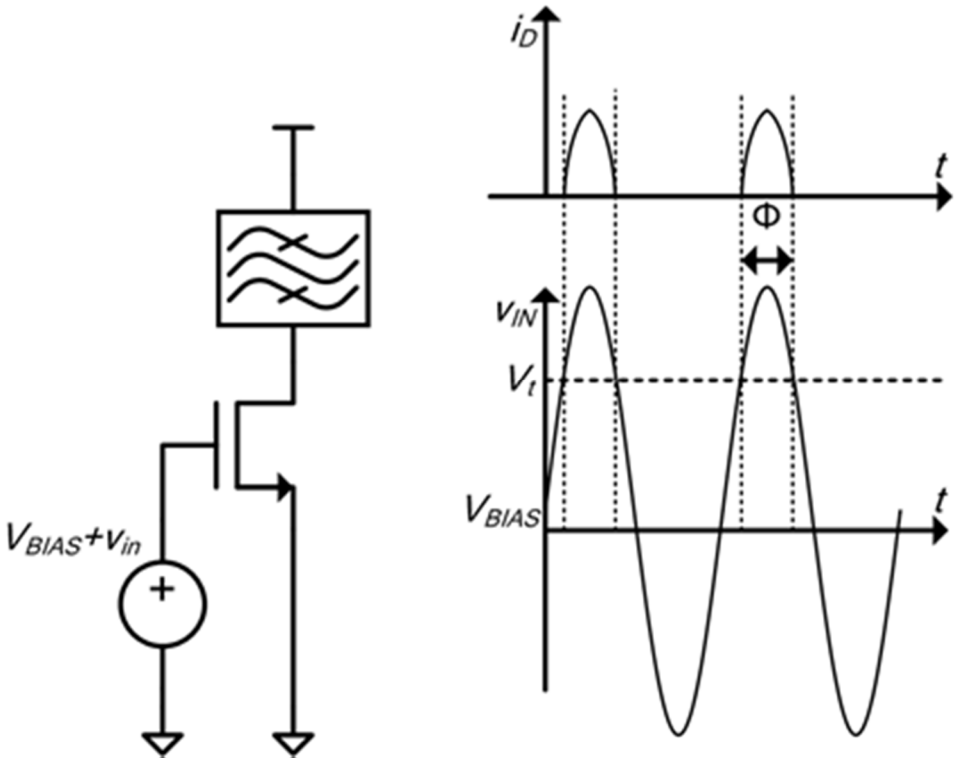


Figure 3-8: Ideal class-C PA operation and conduction angle.

The following section presents the design of the class-C PA and its driver circuit.

For enhancement-mode NMOS transistors, class-C operation refers to an amplifier where the DC-bias point, V_{BIAS}, is set below the threshold voltage, V_t, as shown in Figure 3-8. In normal operation, a voltage input signal with high amplitude is applied to the gate of the device such

that it conducts drain-current, i_D, only when the input signal is greater than V_t. The period that the device conducts relative to a complete cycle of its input signal is called the conduction angle. Because the PA conducts current only for a fraction of the full cycle, the power consumption due to signal voltage and current overlap in time is reduced; hence, the efficiency is increased relative to a traditional linear amplifier that consumes bias current during the full cycle of the input signal.

Because of the non-linear operation of the PA, the output signal should be filtered to select the desired RF carrier frequency and reduce unwanted spectral content. To this end, a band-pass matching network can be used to perform this filtering and present optimum impedance to the PA in order to achieve efficient class-C operation.

A schematic of the class-C PA output stage is shown in Figure 3-9. The amplifier consists of a pseudo-differential transistor pair, $M_{1,2}$, and a matching and filtering network that is described below. Because of the non-linear operation of the class-C PA, differential operation provides the even-harmonic part of the filtering. That is, by driving the PA with differential signals, any even-harmonic content is effectively filtered so that its contribution is minimized at the output.

To further enhance the filtering provided by the pseudo-differential operation, an on-chip 3rd-harmonic trap is designed by placing parallel-resonant networks (Figure 3-9) in series with the outputs of the PA. The networks are tuned to present high impedance at the third-harmonic frequency of the drain currents flowing through M_1 and M_2.

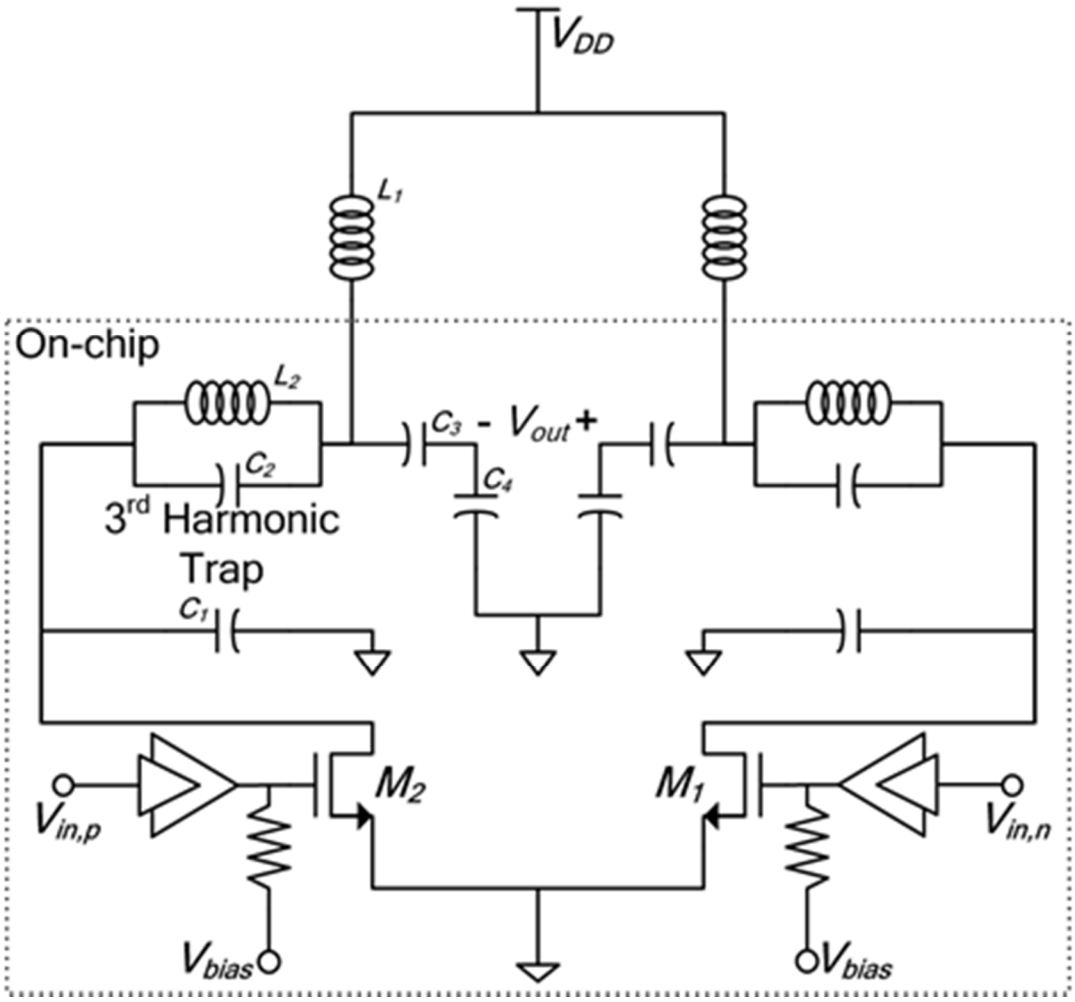


Figure 3-9: Pseudo-differential class-C PA circuit.

Because the PA is intended for use in energy and voltage constrained applications, it is designed to operate from a 0.7 V power supply. For an output power of ~100 µW, this requires a matching network that up-converts the impedance of a typical 50 Ω antenna to a useable impedance of ~500 Ω. For this reason, a tapped capacitor match, consisting of the off-chip inductor, L_1, and capacitors C_3 and C_4 was used. This matching network allows for reasonably-sized on-chip passives at the relatively low operating frequencies of the *MedRadio* band, while simultaneously providing a DC path for the bias currents of the transistors. Capacitor C_1 in

conjunction with the parasitic capacitance at the drain of M_1 is used to limit the size of the off-chip inductor so that one with both a high quality factor and self-resonant frequency can be chosen. Because the high impedance is used in junction with a reduced conduction angle, the output power is limited to the desired range, and can be adjusted slightly by changing the bias voltage, V_{BIAS}.

The PA driver must provide enough voltage swing to cause the output stage to conduct for the desired conduction angle. For this amplifier, voltage amplitude of ~150 mV is necessary to achieve the desired output power.

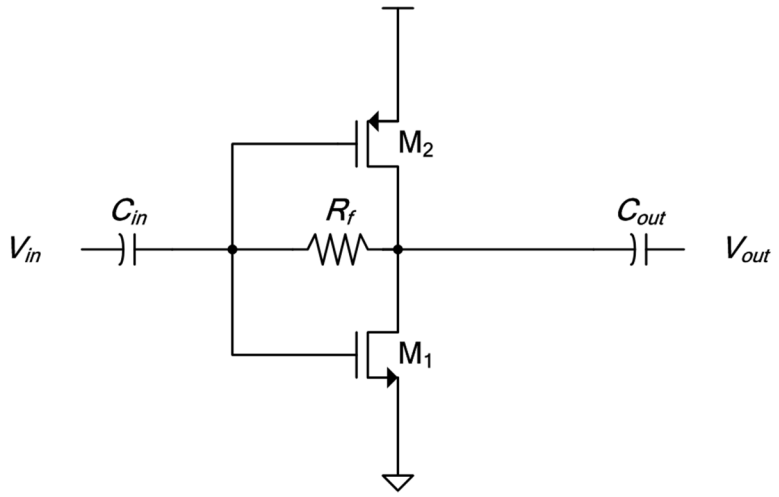


Figure 3-10: PA driver circuit.

The driver is a self-biased inverting amplifier as shown in Figure 3-10. It is designed with complementary NMOS and PMOS transistors, M_1 and M_2, respectively, in order to provide enough voltage headroom to achieve the desired signal swing. For standalone operation, the feedback resistor R_f is chosen such that the amplifier has a broadband input reflection coefficient < -10 dB when driven with a 50 Ω source. Of course, for integrated operation this

requirement is not necessary. The drivers are designed to have a large gain of ~15 dB in order to reduce power consumption.

An experimental prototype of the class-C PA is fabricated in a 0.13 µm RF CMOS process with eight metal layers, including a thick layer for high-quality passive elements. A chip microphotograph of the PA is shown in Figure 3-11. For experimental evaluation, the PA was chip-on-board bonded to a two-layer PCB with a high-quality factor chip inductor serving as the external inductor (Fig. 4, L_1). The completed test assembly board is shown in Figure 3-12

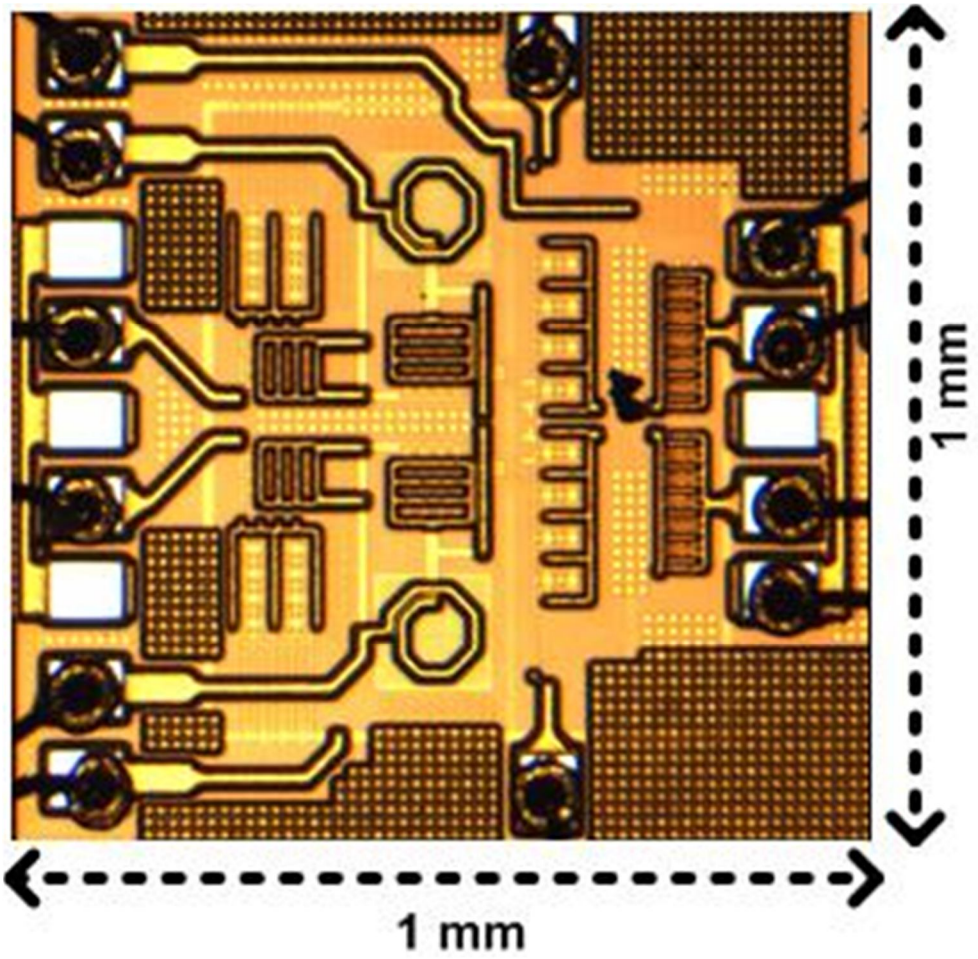


Figure 3-11: Chip Micrograph

Figure 3-12: Testing Board

The output power transfer characteristics for operation at 390 MHz for four different bias voltages are shown in Figure 3-13. Note that class-C operation corresponds to the curve labeled V_{BIAS} = 0 V. The PA output saturates at approximately -5 dBm. One observation from this figure is that the output becomes more linear as the bias voltage is increased until the bias voltage approaches the devices threshold voltage, V_t. At this voltage (V_{BIAS} = 0.3 V) the device operates at the boundary of the triode and saturation regions and is thus less linear.

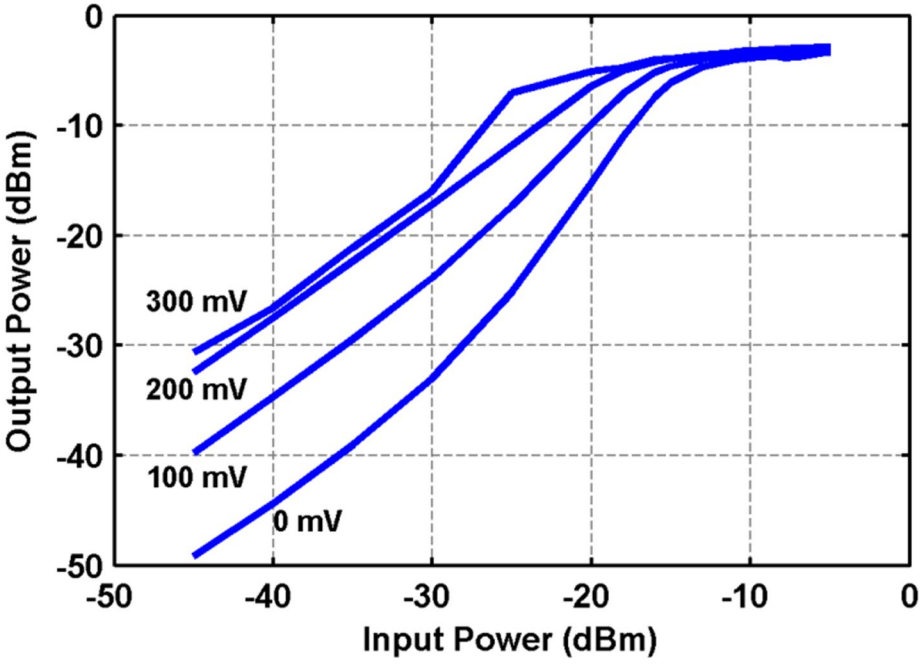


Figure 3-13: Power Transfer Characteristics

The drain-efficiency of the device is plotted in Figure 3-14 while operating in the class-C mode (Fig. 8, V_{BIAS} = 0 V) at 390 MHz. The PA achieves a peak drain efficiency of 43 % with an output power of -5 dBm.

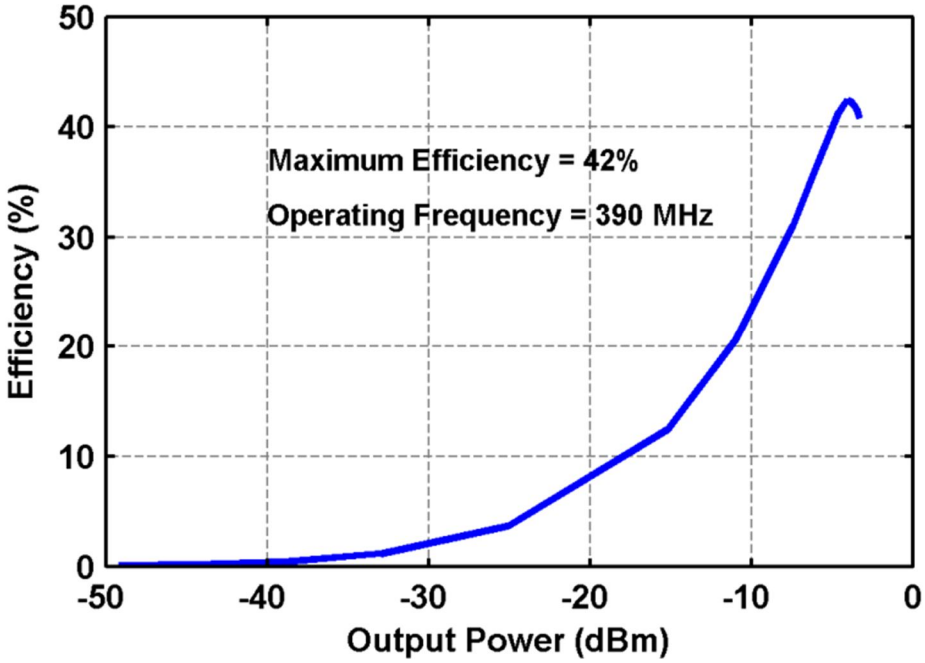


Figure 3-14: Efficiency VS Output Power

The PA operates at a center frequency of 390 MHz, as shown in Figure 3-15. Also shown in the figure is the frequency response of the PA at -1 dB power backoff, showing little difference in the responses. The -3 dB bandwidth of the PA is ~100 MHz owing to the relatively high loaded quality factor of the matching and filtering networks.

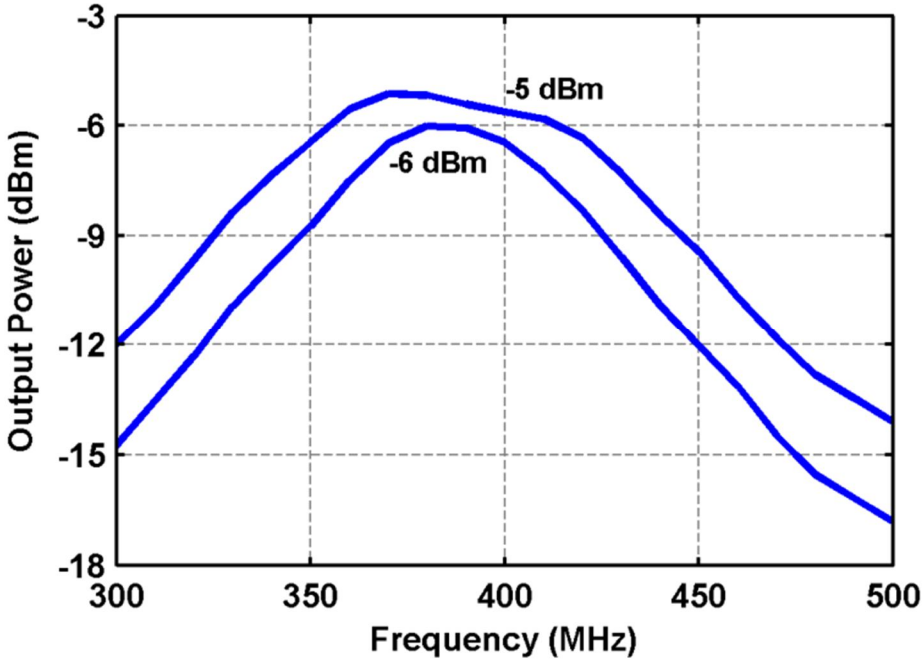


Figure 3-15: Bandwidth of the PA

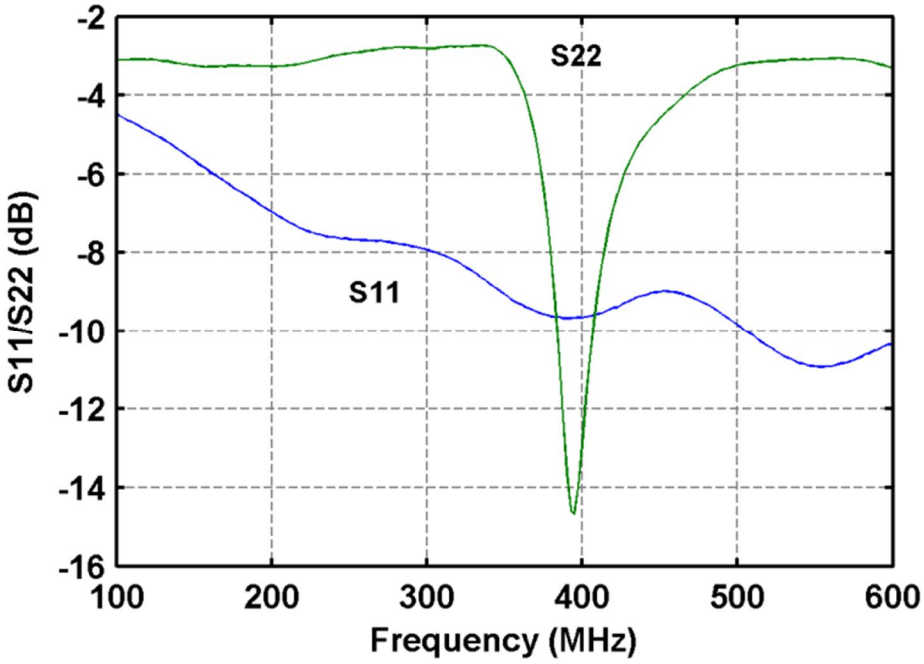


Figure 3-16: Input and Output Return Losses

The PA driver achieves a broadband input match while the output stage exhibits the tuned match expected of the band-pass circuit as demonstrated by the input and output return losses in Figure 3-16.

The next section extends this idea of using a class-C amplifier and an entire transmitter for the medical applications is designed and fabricated.

4. Transmitter Architectures for BAN

Two big challenges impeding the widespread deployment of autonomous sensor nodes are power consumption and level of integration. In order to become omnipresent, they should have form factors smaller than a coin, which necessitates operation from either scavenged energy or a small battery. Moreover, implanted sensor nodes should be deployable for many years on a single battery charge to minimize invasive operations. All of these goals require a typical wireless sensor node to operate with an average power consumption of only ~10 µW, which imposes difficult challenges in the design of the radio.

Several interesting architectures for implementing the radio on a wireless sensor node have been proposed recently. The direct modulation approach described by Cho, et al. [24] uses a low-power oscillator followed by a PA/antenna interface. In order to save power, the architectures presented by Bohorquez, et al. [3], and Chee, et al. [25], eliminate the PA and couple the oscillator directly to the antenna using it as the inductive element. Finally, Rai, et al. [4] use a frequency multiplication method wherein frequency synthesis and data modulation are first performed at a lower frequency and then multiplied up to the RF carrier frequency using the antenna interface. These solutions are evaluated and compared to determine their advantages and disadvantages. The results of this work may stimulate new architectures with higher energy efficiency.

4.1. Low Power Transmitters

The average power consumption in a duty-cycled transmitter is given by [25]:

$$P_{TX,AVG} = \frac{T_{SETUP}P_{TX,SETUP} + T_{TX}\left[P_{PRE-PA} + \frac{P_{PA}}{\eta_d}\right]}{T_{DATA}}$$

where T_{SETUP} is the set-up time of the transmitter, $P_{TX,SETUP}$ is the power consumed during setup, T_{TX} is the total transmit time, P_{PRE-PA} is the power consumed by all circuits preceding the power amplifier, P_{PA} is the power output by the PA, η_d is the drain efficiency of the PA, and T_{DATA} is the duration of the transmitted data. All of the timing parameters are determined by the protocol that is used; thus, in order to minimize the overall power dissipation, the design should minimize the power dissipated by the baseband circuitry ($P_{TX,SETUP}$) as well as that consumed by the radio circuitry (P_{PRE-PA} and P_{PA}). Unlike high-speed communication applications (e.g., *WiFi* and cellular), the power amplifiers used in sensor network applications are designed to transmit at ultra-low-power levels. The best reported CMOS PAs to date achieve peak efficiencies of about 40-60% for relatively high output power levels (0.25-1 W) [5], but, unfortunately, the efficiency decreases dramatically a low power levels [32][33][34].

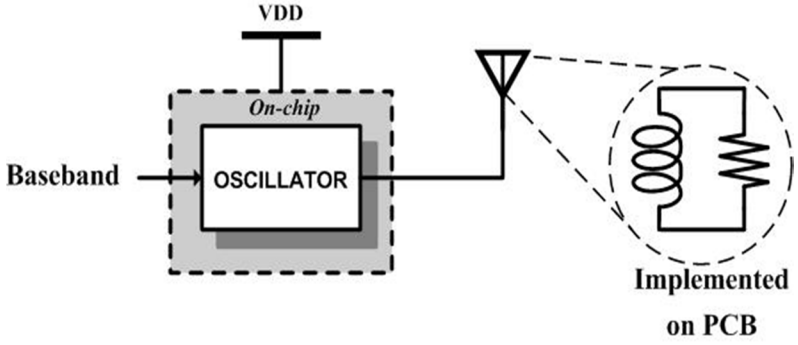


Figure 4-1: Sensor node with an oscillator driving an off-chip antenna.

In order to totally eliminate losses from the PA, the approach of Bohorquez, et al. [3] (Figure 4-1) simply does not use one; instead, the (power) oscillator drives the antenna directly while

simultaneously using it as the inductive element in its resonant tank. The underlying assumption is that such a design is more energy efficient because of the use of fewer circuits that consume power. Clearly, this solution reduces the number of circuits; however, it transfers most of the overall power budget to the (power) oscillator. Because the antenna element is also operating as the inductor in the loaded resonator network, its operation as an antenna is less efficient, so the oscillator must deliver additional power to compensate for this effect. This architecture is also subject to frequency pulling of the oscillator because there are no intermediate circuits to isolate the oscillator from the load variations seen by the antenna. In the following section, the energy efficiency of a transmitter architecture that employs no interface to the antenna is analyzed and compared to that of an architecture in which the oscillator drives an intermediate buffer that interfaces to the antenna.

4.2. Transmitter Comparison

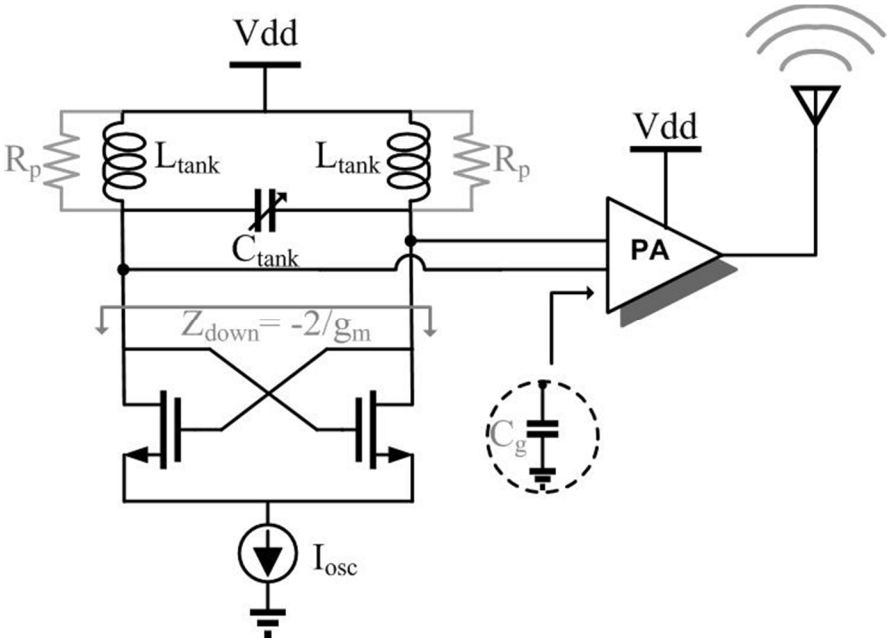


Figure 4-2: A direct modulation transmitter with a DCO driving the PA.

In a direct modulation transmitter (Figure 4-2), a PA stage provides a buffer interface between the oscillator and the antenna. In a typical implementation, the oscillator is a digitally-controlled oscillator (DCO) operating with an NMOS (or CMOS) cross-coupled transistor pair(s). Switched-capacitor arrays provide a means for digital frequency tuning and direct frequency shift keying (FSK) modulation. The power-added-efficiency (PAE) of the PA is:

$$PAE = \frac{P_{out}}{P_{in} + P_{DC}}$$

where P_{out} is the output power, P_{in} is the input power and P_{DC} is the DC power dissipated by the PA. For a PA with a power gain of G, the PAE can also be expressed as:

$$PAE = \frac{P_{out}}{P_{out}/G + P_{DC}}$$

Rearranging (3), the DC power consumed by a PA can be related to its gain and PAE (Figure 4-3):

$$P_{DC} = P_{out}\left[\frac{1}{PAE} - \frac{1}{G}\right]$$

Because the input capacitance of the PA is absorbed in the resonant tank of the oscillator, it reasonably can be assumed that all of the power generated by the oscillator is input to the PA; hence, the power generated by the oscillator can be expressed as:

$$\boldsymbol{P_{OSC} = P_{out}/G = \frac{\left(V_{p-p}/2*\sqrt{2}\right)^2}{R}}$$

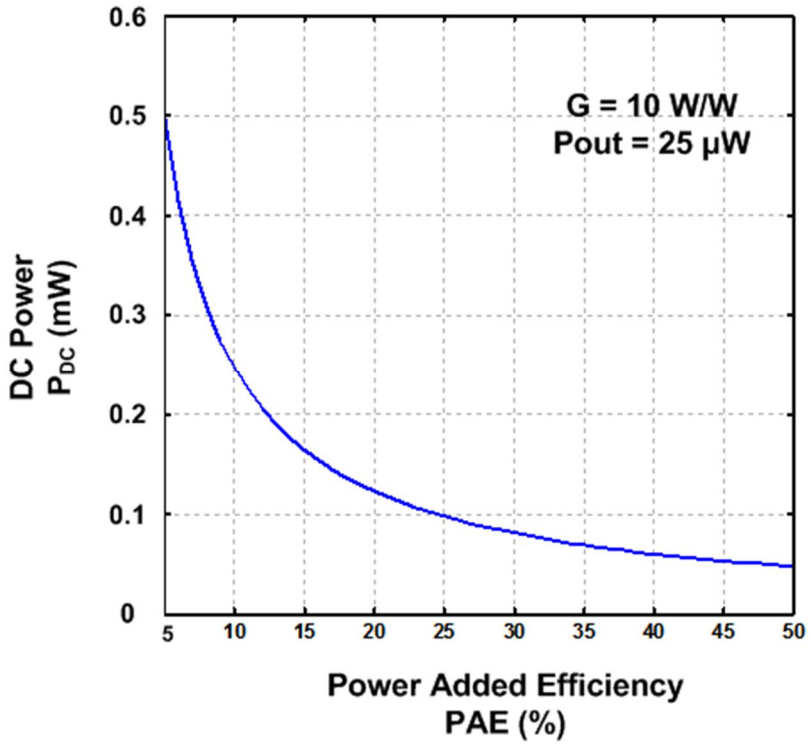


Figure 4-3: PA DC power consumption VS PAE

where V_{p-p} represents the peak to peak amplitude swing of the oscillator. The voltage peak to peak amplitude of a fully-differential LC- DCO (Figure 4-2) is:

$$V_{p-p} = \frac{4}{\pi} I_{osc} R_p$$

where R_p is the equivalent parallel resistance of the resonant tank and I_{osc} is the tail current source. Thus, the power delivered by the oscillator to the PA and that delivered by the PA to the antenna are:

$$P_{osc} = \frac{2}{\pi^2} I_{osc}^2 R_p$$

$$P_{out} = G \frac{2}{\pi^2} I_{osc}^2 R_p$$

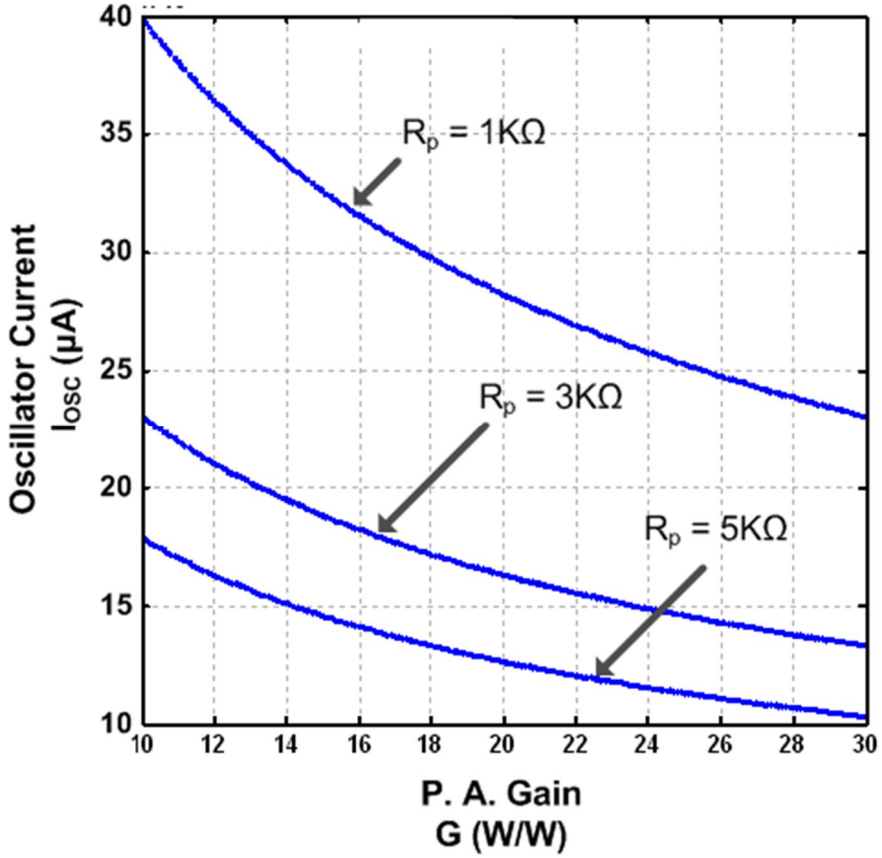


Figure 4-4: Oscillator current (IOSC) versus PA gain, G

The required oscillator tail current, I_{osc}, versus PA gain, G, for several values of R_p (with P_{out} = 25 μW) are plotted in Figure 4-4. Two key observations follow from the figure. First, by employing a PA with power gain, the oscillator is able to operate using significantly less power (i.e., lower I_{osc}) than when no PA is used. Second, using a resonant tank with a higher quality factor (i.e., higher R_p) also allows the oscillator to operate at lower bias current. Thus, the power consumed by the oscillator in such a transmitter is strongly dependent on both the gain of the buffer/PA that interfaces it to the antenna and the Q of the passive components used in the resonant tank. When driven directly by the oscillator, however, the inductance and associated parasitic resistance of the antenna is effectively in parallel with the tank, which degrades the overall

energy efficiency. Moreover, the impedance represented by the antenna is strongly dependent on its external environment, and it is well known that such impedance variations adversely affect both the frequency of oscillation and the power radiated from the system.

Consider a transmitter operating in the MICS band at a maximum *EIRP* of 25 μW. Further, assume it employs a PA with a PAE of 30% and a power gain of 10 W/W. The oscillator uses a combination of bond-wire and ceramic off-chip inductors so the quality factor of its resonant tank is ~50. A large inductance of ~30 nH is necessary for operation in the MICS band (402-405 MHz); thus, the equivalent parallel resistance of the tank circuit is R_p = 3.8 kΩ. For the PA, the required P_{in} is 2.5 μW. Assuming the power generated by the oscillator, P_{osc}, is completely transferred to the PA, the bias current of the oscillator is found from (7) as 56.9 μA. For reliable startup of a cross-coupled oscillator, the product of the small-signal transconductance, g_m, and the parallel resistance, R_p, of the resonant tank circuit should be greater than 1. In a 130 nm CMOS process, an NMOS transistor operating at the onset of strong inversion where g_m is maximized has $g_m \approx 25 I_{DRAIN}$ ($I_{DRAIN} = I_{OSC}/2$)[9]. For the oscillator assumed here, $g_m R_p$ = 2.7, which guarantees reliable startup and oscillation. From (4), the DC power consumed by the PA is 80.6 μW. With a 1V power supply for the PA and 700 mV for the oscillator [6], the total power consumed by both is 120.4 μW in order to deliver 25 μW to the antenna; hence, the overall efficiency of the transmitter is 20.7%. From this calculation, it is clear that improvement in the PA architecture for higher efficiency, as well as improvement in the oscillator architecture, can offer a significant improvement in energy usage for a sensor system.

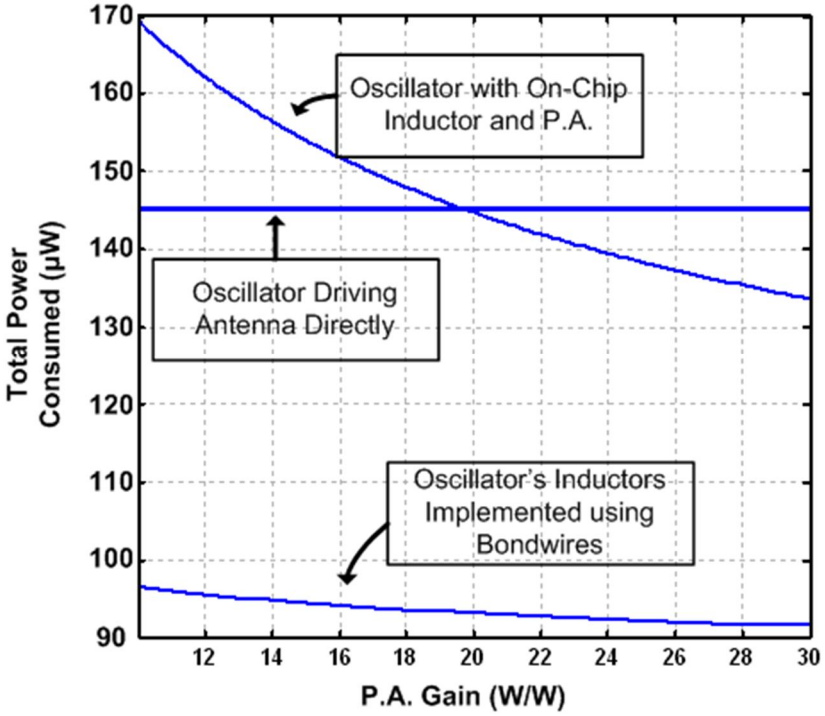


Figure 4-5: Total power consumption versus PA gain

A plot of the total power consumed by the three different transmitters versus PA gain is shown in Figure 4-5. The three architectures include an oscillator directly driving an antenna with no PA, an oscillator with on-chip inductors driving a PA and an oscillator with bond-wire inductors driving a PA. When the level of integration is not an issue (i.e., off-chip components are allowed) it is noted that the oscillator with the high-*Q* (30-70) bond-wire and external inductors always uses less power than the other two architectures. If an efficient PA with gain > 20 is available, a PA with on-chip inductors ($Q \approx$ 5-10) is more efficient than an oscillator directly coupled to the antenna; however, for smaller PA gain, the directly-driven antenna should be chosen. The calculations used for Figure 4-5 can be used to estimate the total power consumed as a function of the quality factor of the inductors. The power calculations for the oscillator directly coupled to the antenna were taken from [3].

With the background obtained in this chapter, a PLL-based BFSK Transmitter with Reconfigurable and PVT-Tolerant Class-C PA for the MedRadio and ISM (433MHz) Standards is designed and fabricated in the IBM 130nm CMOS process. It is described in the Figure 4-6.

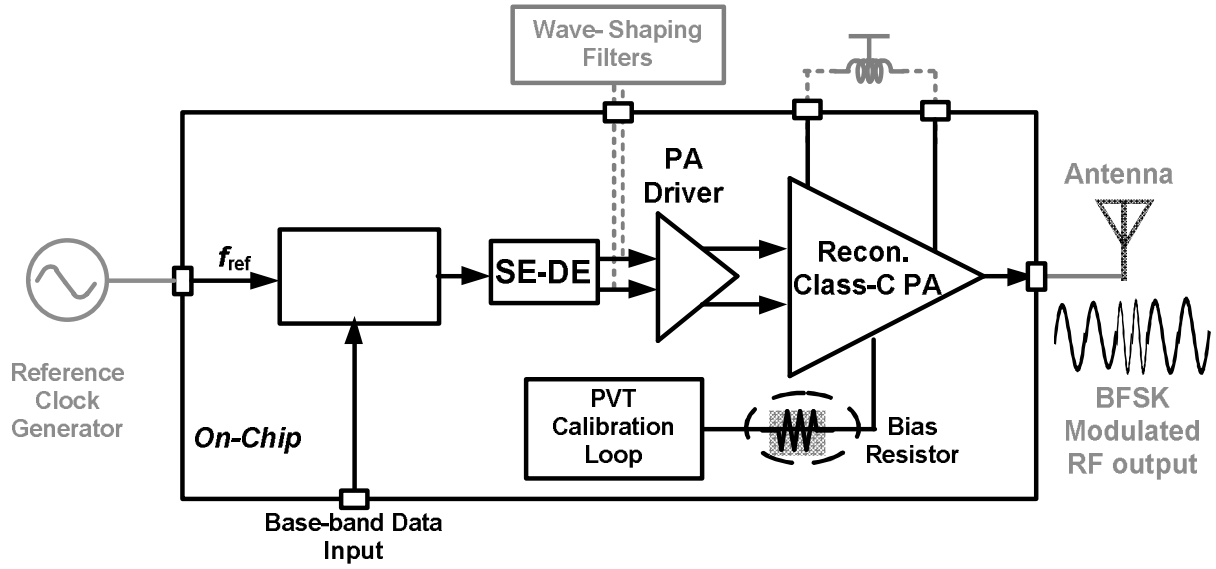


Figure 4-6: Reconfigurable Medical Transmitter

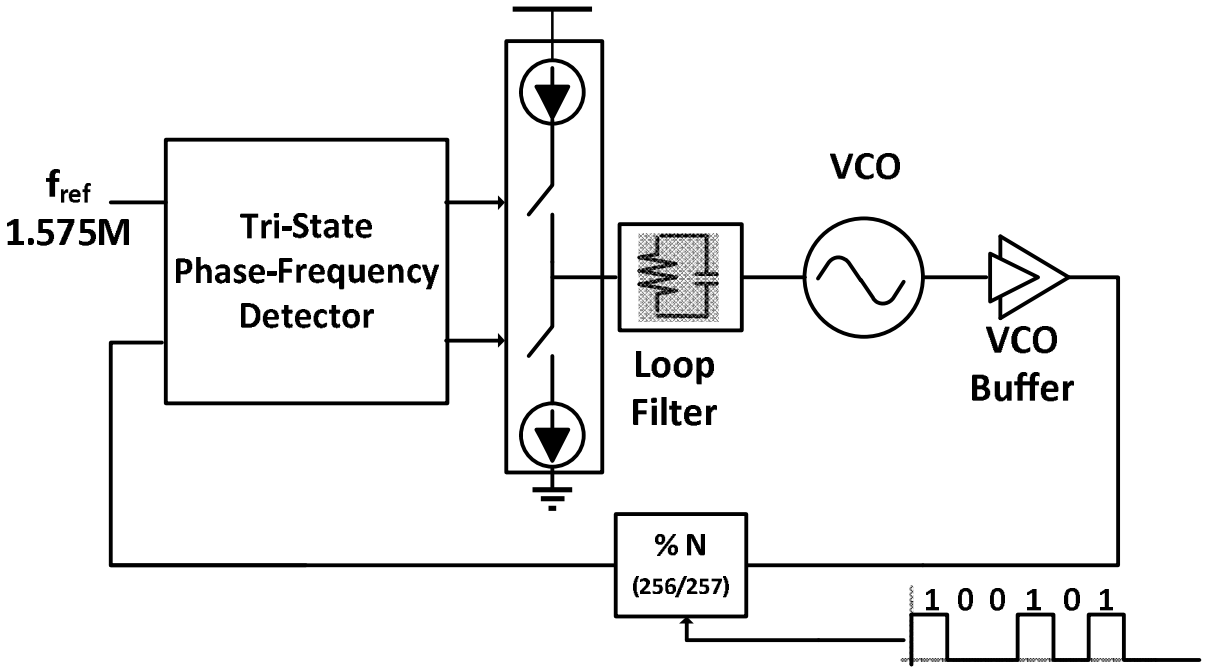
The reconfigurable transmitter consists of a Phase Locked Loop (PLL) used as a frequency synthesizer. The base-band input data is binary FSK modulated where the modulation bit 0 and bit 1 corresponds to two different frequencies separated by the reference of the PLL. The VCO is implemented as a delay based ring oscillator to save power and the single ended output is converted to differential output to feed into the PA. The waveform might is buffered before driving the PA input and hence requires shaping to extract the fundamental signal. This is done off-chip by the wave shaping filters. The reconfigurable PA is designed to output at two different power levels at almost similar drain efficiency values. For the first time in literature,

the PVT variation in the class-C amplifiers is compensated using an ultra-low power open-loop calibration loop. The transmitter can be reconfigured to operate in the MedRadio (402MHz) or the ISM 433MHz band. Following sections talk about the individual building blocks of the transmitter.

5. Phase Locked Loop

A PLL is used to generate the signal at 402MHz or 433MHz for the MedRadio or the ISM bands. BFSK modulation is achieved by changing the divide ratio of a dual-modulo divider. Presence of process, temperature and voltage variations necessitate locking the free-running ring oscillator frequency and at the same time power consumed in the loop is kept to a minimum.

5.1. PLL Description



The PLL block diagram is shown in the figure. A type II 3rd order PLL is designed and used in the ultra-low power transmitter. It consists of the phase frequency detector (PFD) to identify the phase or frequency variations, a charge pump (CP), loop filter and a dual-modulo divider. To optimize of the design simplicity and power, an integer-N divider is chosen over fractional-N divider. An external crystal source (or an RF signal source) is used as the frequency reference.

The VCO and the first few stages of the divider are the most power hungry blocks of the PLL. Consequently careful design techniques along with few novel ideas help reduce this power consumption drastically. The following few sections describe each of the blocks in detail.

5.2. Phase Frequency Detector

The PFD is used to compare the divided frequency and the input reference frequency. It is edge-triggered and generates the control signal according to the time difference between the 2 input signals. UP/DN signifies the charge pump to increase/decrease the control voltage to the oscillator. A static PFD proposed in [26] used an asynchronous state machine. The operating speed is dominated by the reset operation of the flip flops. The critical path includes the reset path has six gate delays and is a major limitation in high-speed designs.

To overcome the issues mentioned above, [27] proposed a new dynamic logic style PFD. The key advantage of this architecture is the number of transistors used in the PFD core is less and the delay of the reset paths is three delays shorter than the conventional implementation style. This allows increase in operation speed.

Another common drawback in some PFDs is the presence of the dead-zone in the transfer characteristics. It is the flat region of the transfer curve between phase and delay, where non-linearity occur. This leads to generation of phase jitter since the control system does not change the control voltage input to the VCO. To overcome this issue, reset signal has been delayed to assert UP and DN output as shown in the figure even when F_{REF} and F_{DIV} are in phase.

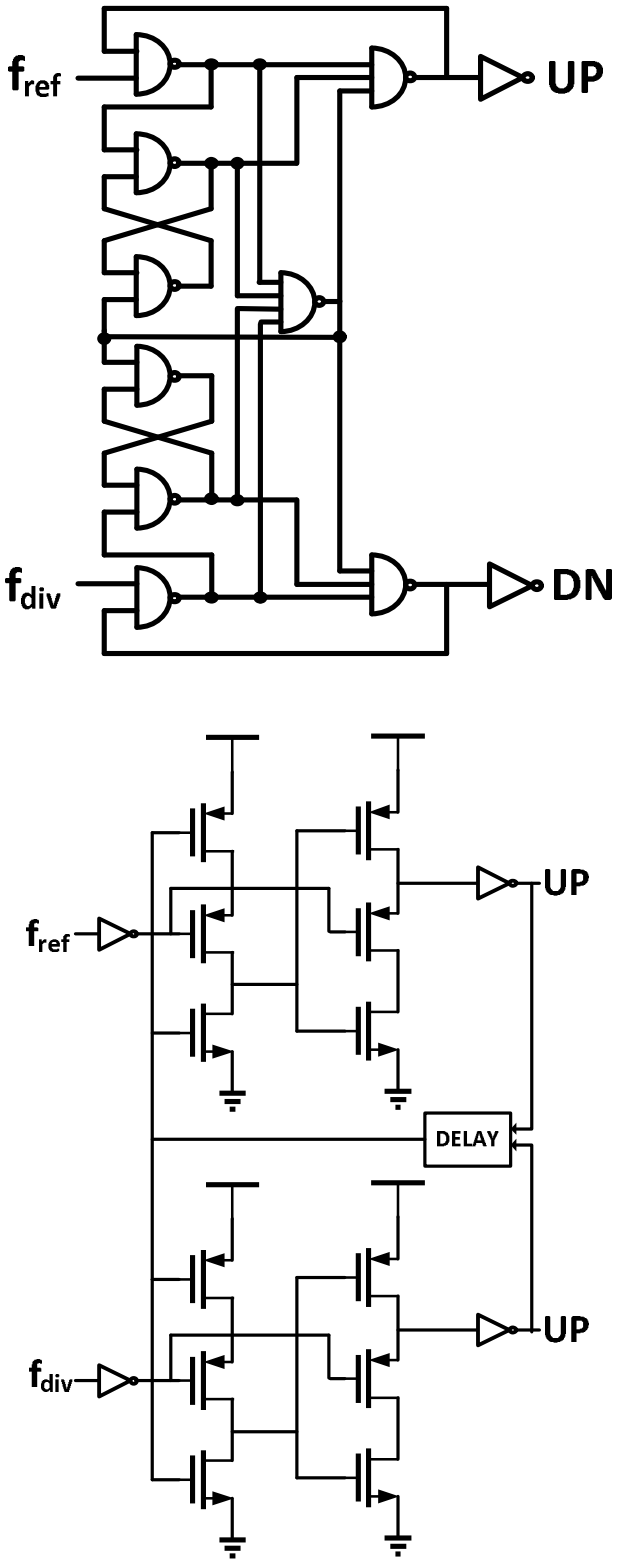


Figure 5-1: Phase Frequency Detector (Top-Bottom): Conventional Implementation, High-Speed Implementation

5.3. Charge Pump

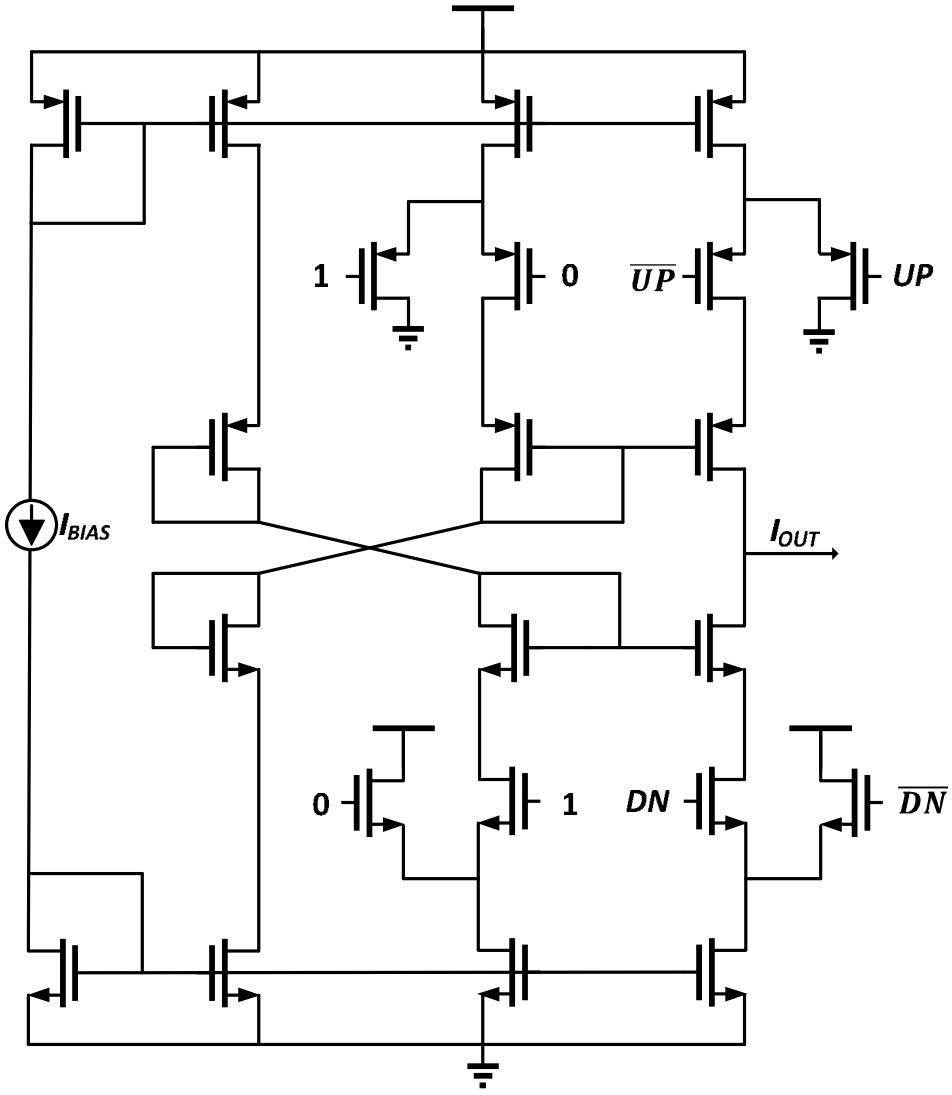


Figure 5-2: Charge Pump Implementation

The implemented charge pump is shown in figure below. The cascoded current mirror is used to generate the UP and DN current signals. Charge injection errors induced by parasitic capacitors of the current sources and switches are common concern in charge pump and causes a static phase errors between the two inputs of the PFD. To mitigate this problem, the current source transistors, M4 and M8, are connected to output node VCP. If transistor M1 is off and M2 is on,

source current from M3 still remains to GND and the voltage of node A must be equal to VCP due to the gate overdrive of the current source device. When M5 is off and M6 is on, the sink current from M7 remains from VDD and the voltage of node B is also equal to VCP, reducing the charge sharing effect. Moreover, the controlled voltage is isolated with M4 and M8 from the switching noise induced by the gate-to-drain overlap capacitance of the switching transistors, M1 and M5. For matching concern and improving performance, the dummy switch transistors are added in the cascode current source to matching the capacitive load from the current steering devices in the output current path.

5.4. Dual-Modulo Divider

The divider implemented is a 256/257 dual modulus prescaler. Apart from the VCO, the divider is one of the most critical blocks in the frequency synthesizer in terms of power consumption. The implemented divider is shown in the Figure 5-3 [].

It is implemented as a synchronous divide by 4/5 circuit and an asynchronous divide by 64 circuit as shown in the figure. The divide ratio is 256 when the modulation input is set to 0 and the ratio becomes 257 when the modulation input is set to 1.

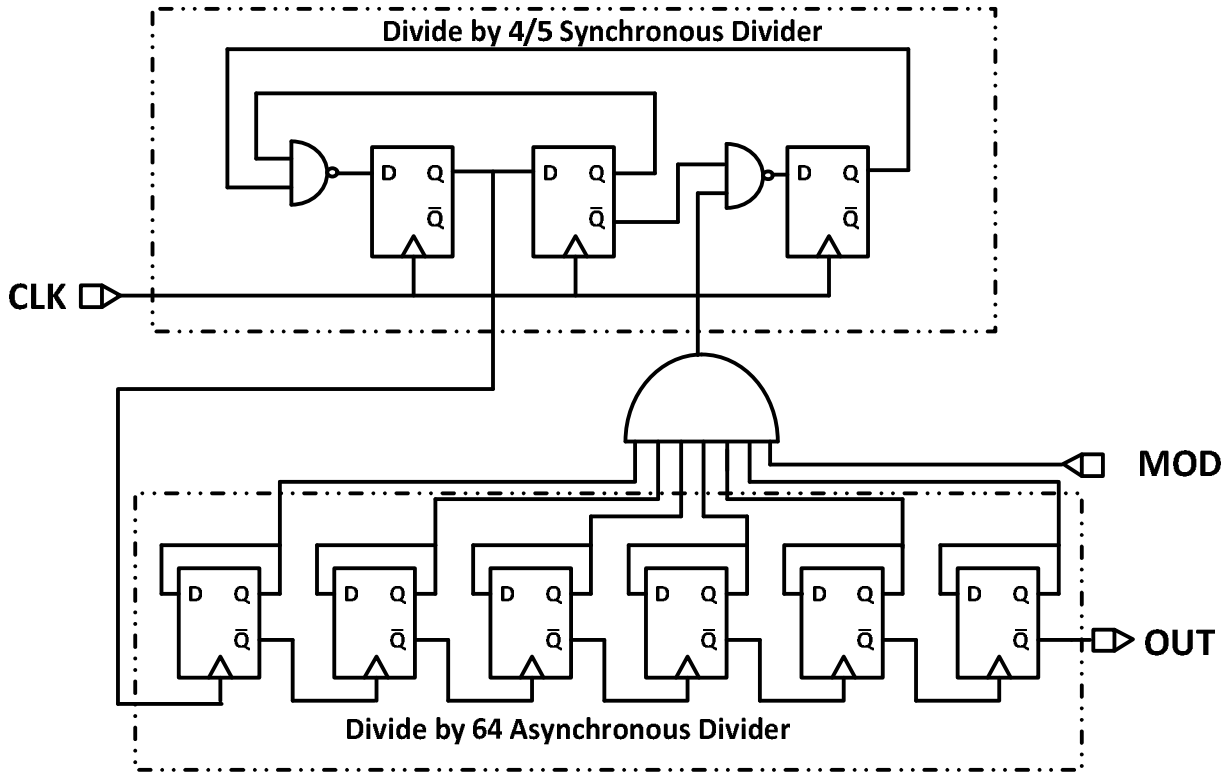
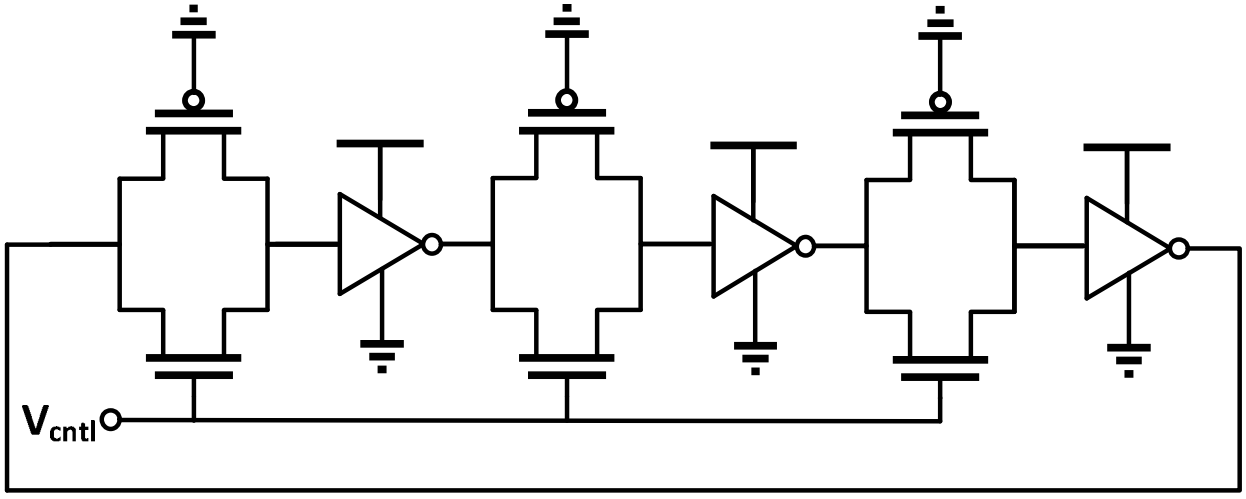


Figure 5-3: Dual Modulo Divider

The synchronous divide by 4/5 is the most critical part as it operates at the highest frequency. The divide by 4/5 circuit consists of three D flip-flops and two nand gates. The arrangement shows the first two flip-flops connected as a divide-by-4 circuit. The last flip-flop adds an extra clock cycle delay to give the divide-by-5 operation. The critical path is limited by both the flops and the nand gates. Critical path analysis can show us the maximum frequency at which the circuit can function reliably. The knowledge of critical path also allows us to smartly design the circuits which do not operate at high speeds. The operating speed of the divider is also mainly limited by the first divider. To maximize this parameter, a nine-transistor TSPC DFF in implemented. The main advantage of the using such architecture is the high operating speed and simple circuits required besides just requiring just one single phase clock signal for the TSPC

(True Single Phase Clock). Only the first two divide-by-2 DFF uses this dynamic implementation with the following DFFs using the conventional static circuit for power saving considerations.



$$f_{NDRO} = \frac{1}{2N\tau} = \frac{1}{2NC_{inv}(R_{NMOS} + \frac{1}{Gm})}$$

Figure 5-4: NMOS Delay Based Saturated Ring Oscillator

5.5. Ring Oscillator

The two main options for implementing the oscillators are the LC oscillator or the ring oscillator. While the LC oscillator achieves superior phase noise performance, the ring oscillator wins in terms of area occupied. The phase noise requirement for medical applications is not that stringent. This allows us to utilize the ring oscillator. The novel NMOS delay-based ring oscillator (NDRO) is shown in Figure 5-4. Rather than controlling V_{DD} to set the oscillation frequency, NDRO controls the resistances of switches in series with the gate capacitances of inverters [32]. However, both V_{tune} and (V_{DD}-V_{tune}) signals are required for transmission-gate switches. The latter requires a level shifter that adds area, power, and noise coupling from V_{DD}

to the output. These concerns are eliminated in Fig. 3 where only NMOS switches are tuned. Compared to conventional RO-based PLL designs, this approach save power, reduces K_{VCO} for higher stability, and reduces phase noise at the expense of reduced tuning range.

Consider one of the delay cells in the ring oscillator. The gate combination is shown as a resistor R_{eff} in series with gate input capacitance C_{eff}.

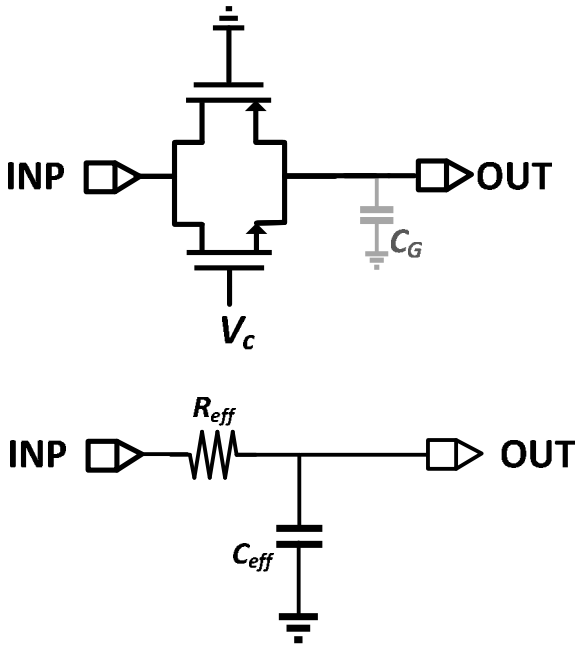


Figure 5-5: Delay Stage

With the control voltage V_c being high, the NMOS is in the conduction region and the resistance of the gate is very small. If the control voltage V_c is low, the NMOS is in the cutoff region and the switch acts as an open circuit. Ideally the impedance of the switch is infinite in such cases.

The drain current in the linear region of a MOS is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

Consequently the resistance associated with the channel from the source to drain is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$

Considering the charge and discharge of the inverter cell along with the NMOS delay cell, we have a simplified circuit as shown [29][30]:

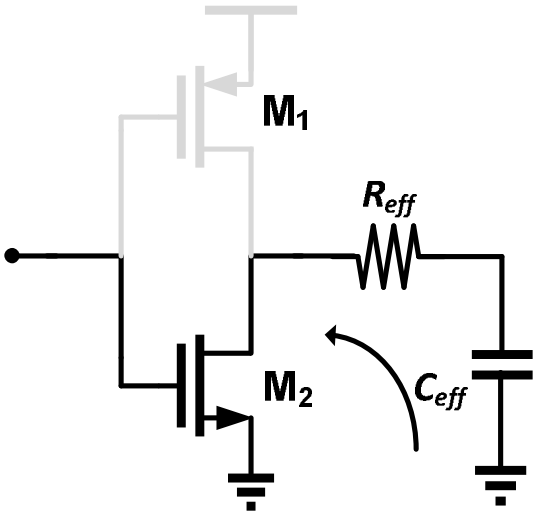


Figure 5-6: Charging/Discharging Characteristics

$$f_{osc} = \frac{1}{2N\tau}$$

$$f_{osc} = \frac{1}{2N\left(\frac{1}{g_m} + R_{ON}\right)C_{eff}}$$

Where f_{OSC} is the frequency of oscillation, N is the number of stages of the ring oscillator, g_m is the transistor transconductance, RON is the effective impedance of the switch and C_{eff} is the

effective capacitance including the switch capacitance and the gate capacitance C_{GS} of the next stage of the inverter cell.

5.6. Loop filter design

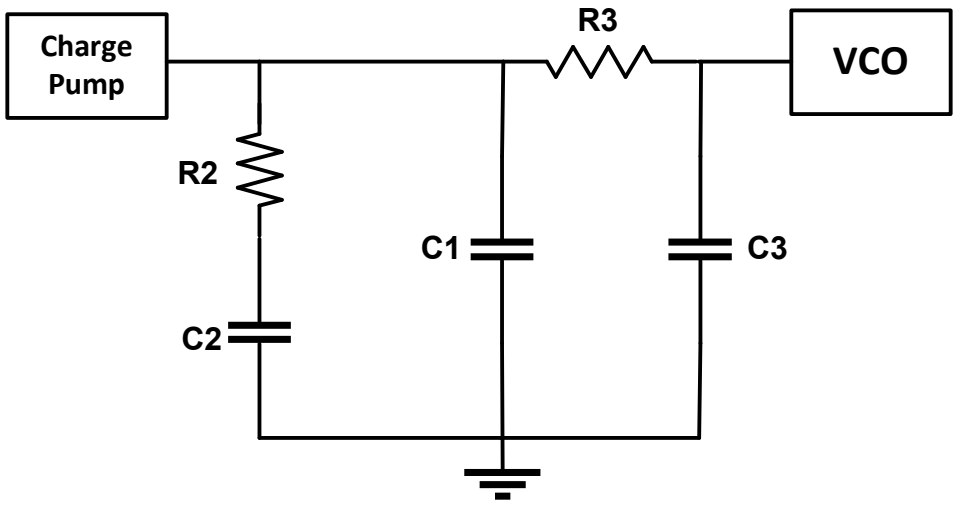


Figure 5-7: Loop Filter Implementation

$$Z(s) = \frac{(1 + sT_2)}{(1 + sT_1)(1 + sT_3)} * \frac{T_1}{C_1 T_2}$$

where $T_1 = R_2 \frac{C_1 * C_2}{C_1 + C_2}$, $T_2 = R_2 C_2$ and $T_3 = R_3 C_3$

An additional pole realized from R_3 and C_3 decreases the spurious attenuation. This causes the bandwidth reduction and the attenuation from the filter is given by:

$$Atten = 20.\log_{10}[1 + ((2\pi.F_{REF}.R_3.C_3)^2)]$$

While T1 and T3 correspond to the poles of the filter, T2 corresponds to a zero to compensate for the phase margin. Stability concerns dictate the values of C_3 and C_1 such that $C_3 \leq C_1/10$ and $R_3 > 2R_2$.

Table 5-1: PLL Specification Table

Parameters	Value
Type/Order	Type II/Third Order
Output Frequency	402 MHz (MedRadio) 405 MHz (ISM)
Reference Frequency	1.575M (MedRadio 1.692M (ISM)
Divide Ratio	256/257
Loop Bandwidth	100KHz
K_{VCO}	140MHz/V
K_{VDD}	500MHz/V
I_{CP}	10µA
C1	133p
C2	1.72n
R2	43.3K
R3	1K
C3	1p

The PLL is a complicated system to simulate on the top-level. Transient simulations can take close to few days if not weeks to complete simulation. Thus system level simulations are performed in a PLL design software to reduce this design cycle time. The phase noise

contribution from the PFD and the VCO are plotted along-with the total PLL noise. The primary contribution of the phase noise at low offset frequencies is from the PFD and it is dominated by VCO at far offsets.

The following plots show the transfer function of the PLL loop, settling time and the phase noise of the output with the individual contributions from the blocks.

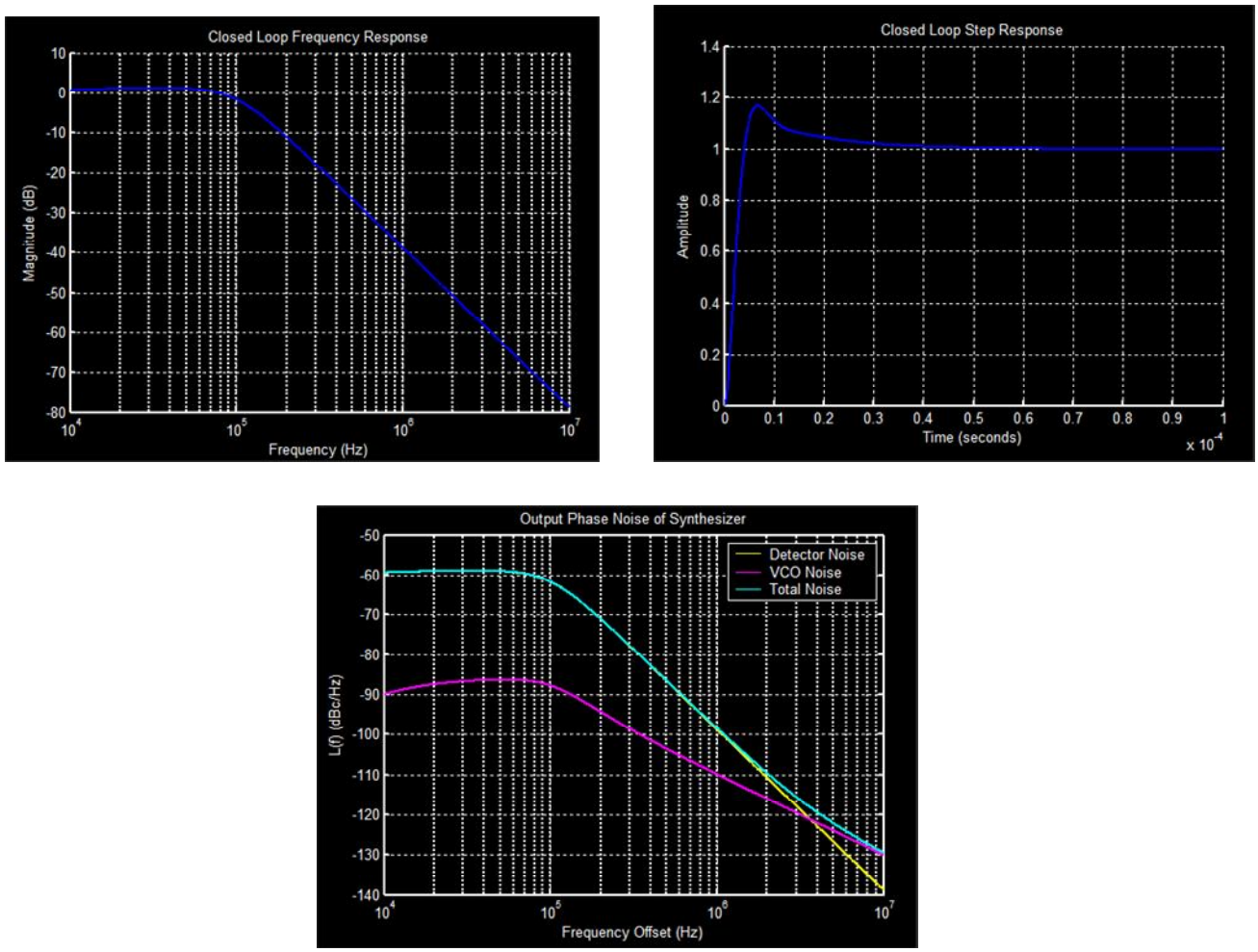


Figure 5-8: System Simulations Results

5.7. Summary

The PLL simulation results are summarized in table.

Table 5-2: PLL Simulation Results

Parameters	**Value**
Type/Order	Type II/Third Order
Output Frequency	402MHz
Phase Noise@ 1MHz offset	-112dBc/Hz
Power (including VCO)	65µW

6. Reconfigurable Power Amplifier

Extending the same idea of a high efficiency class-C power amplifier, the proposed architecture uses two cores connected to the antenna by a single digitally reconfigurable matching network. The digital input word is fed through from the SPI interface on the board. The methodology to design a highly efficient class-C amplifier is explained in the previous chapters. Once the output power levels and the conduction angles are defined, the output characteristics follow the typical power amplifier output characteristic where maximum efficiency is obtained at the saturated output power and the efficiency reduces at back-off. In order to make this power amplifier truly reconfigurable we would need to maintain the same efficiencies when transmitting low or high output power [32].

6.1. Reconfigurable Power Amplifier Architecture

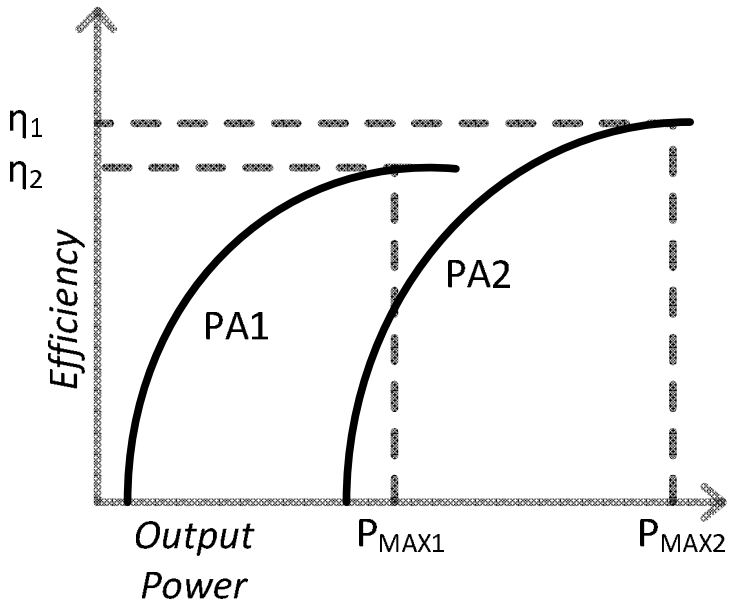


Figure 6-1: Power Amplifier Optimization

Consider the Figure 6-1 shown above where the output efficiency is plotted as the output power varies for two different class-C power amplifiers. Depending on the impedance transformation ratios and the core transistor size chosen, the maximum output power and consequently the peak efficiency can be varied. However once these parameters are chosen, the maximum output power cannot be varied. The efficiency transfer curve 1 and 2 are shown as ideal curves for two different power amplifier which are optimized for to have a maximum output power P_{OUT} of either P_{MAX1} or P_{MAX2}. It is also obvious from the plots that if we choose to implement PA1, we can obtain the lower output power P_{MAX2} but the resultant output efficiency is greatly reduced. Similarly if we decide to implement PA2, we do not have an option to retune the PA to transmit output power of P_{MAX1}.

The ability to digitally tune the output power has several advantages, many of which were talked in detail in chapter 1. In the following section, a new class-C power amplifier with a single reconfigurable matching network is presented that can digitally be tuned to output high or low power. The power amplifier is shown in the Figure 6-2. The two selectable cores are digitally controlled by a switch network to selectively turn them on or off. The single reconfigurable matching network is also controlled by switches. The two power amplifiers shown in Fig 1 are driven by a common driver amplifier. The gain of the driver amplifier is tunable in steps of ~5dB. The individual power amplifiers are configured to work in the class-C mode of operation. The amplifiers share a common antenna as well.

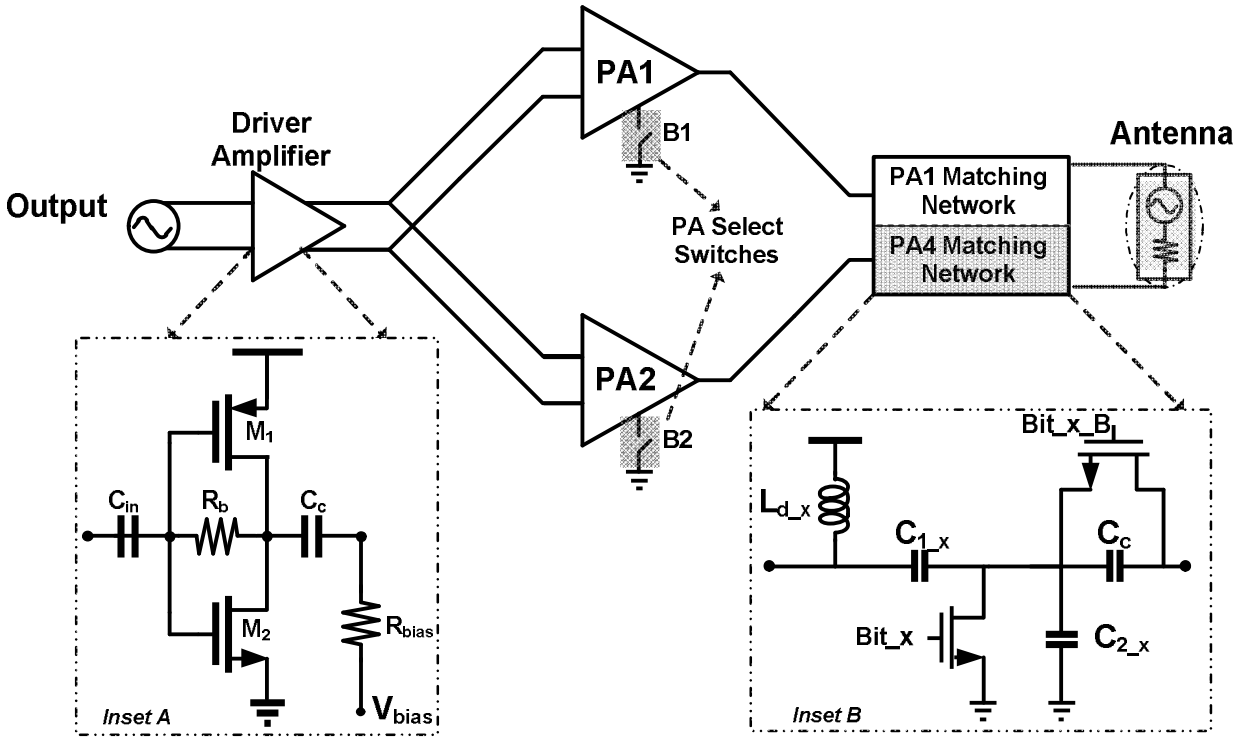


Figure 6-2: Reconfigurable Power Amplifier

6.2. Output Matching Network Design

The main challenge when interfacing two individual power amplifiers is the design of the output matching network. At any given point, only one of the amplifiers is function, hence the other path needs to be turned off completely. Active devices can be controlled using a suitable switch but the passives tend to contribute to the output matching network even if the corresponding amplifier is switched off. As a result, the design of the matching network of each stage needs to take this into consideration. Another related issue is the efficiency of the matching network severely degrades in the presence of unwanted serial impedances. This is particularly true for a matching network designed to have a large transformation ratio. The switchable output matching network is shown in Figure 6-3.

The 2 control bits are shown in the Figure 6-3. Series capacitor Cc is designed to decouple the output individual matching networks. Depending on the control bit chosen, the matching network is enabled or disabled.

Only one matching network is active at any given point in time. For example if *Bit1* is 0, it signifies core 1 is active. The control *Bit2* is set to 1 in this case which disables the core 2. Isolating the matching network is accomplished using a clever arrangement of the capacitors. With *Bit2* set at 1, the matching network associated with the core2 has the coupling capacitor C_c in parallel with the C_2 of matching network 1. The value of C_c is small in comparison of C_2 hence making it easy to account for in the design phase of the network. This scenario is depicted in the Figure 6-4

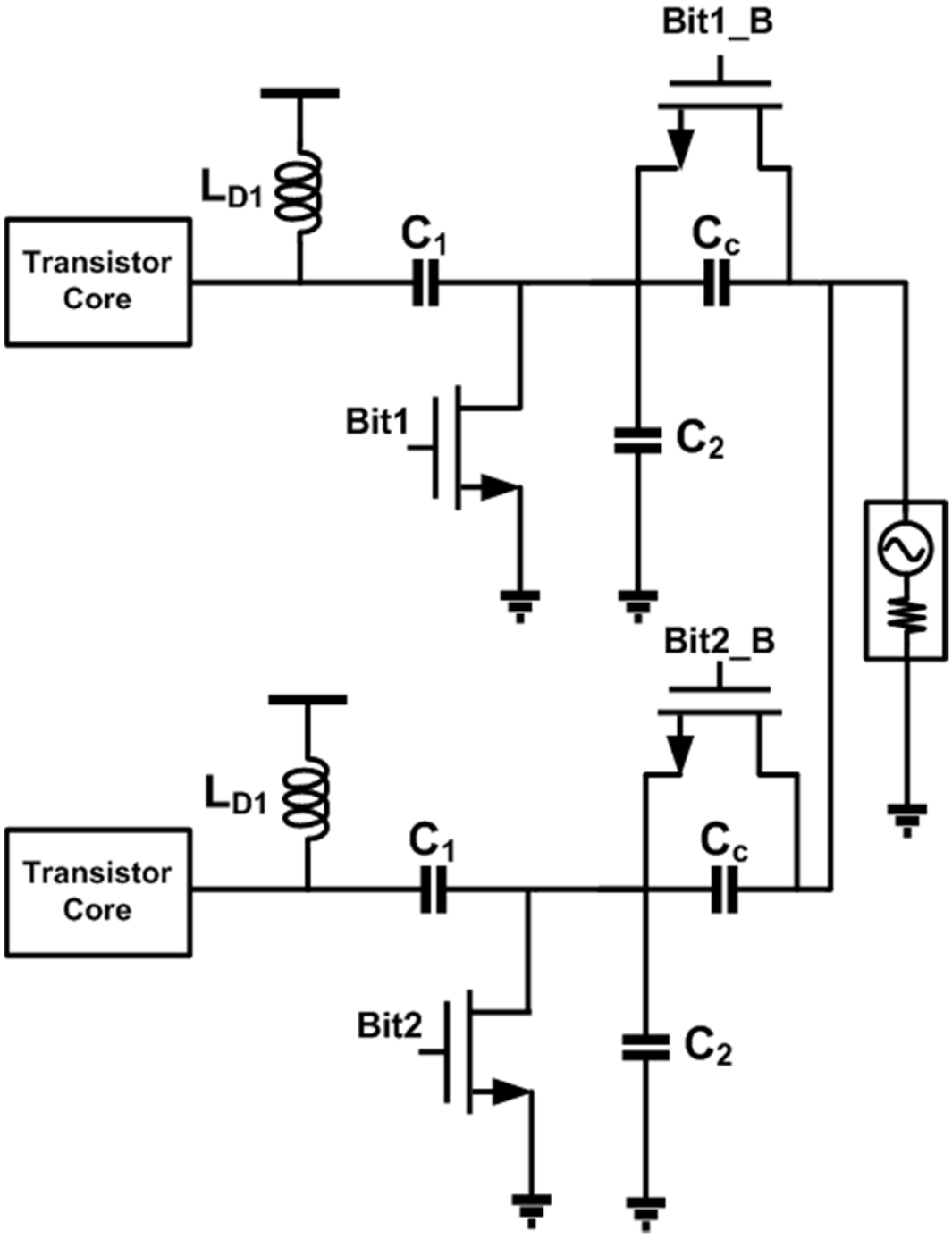


Figure 6-3: Output Matching Network

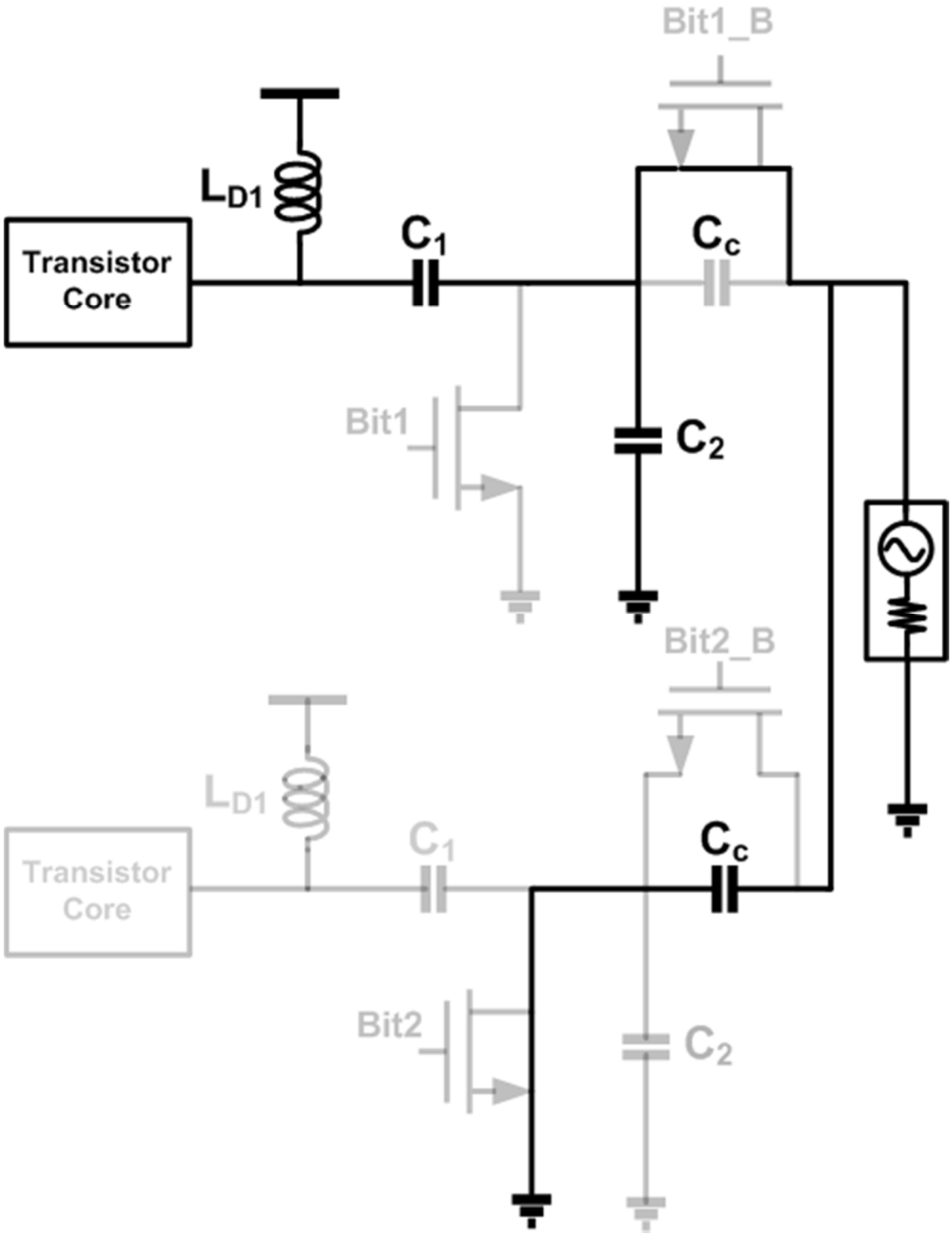


Figure 6-4: Matching Network Explanation

Consider the individual matching network of a single core. For illustration purpose a single ended version is shown in the Figure 6-5.

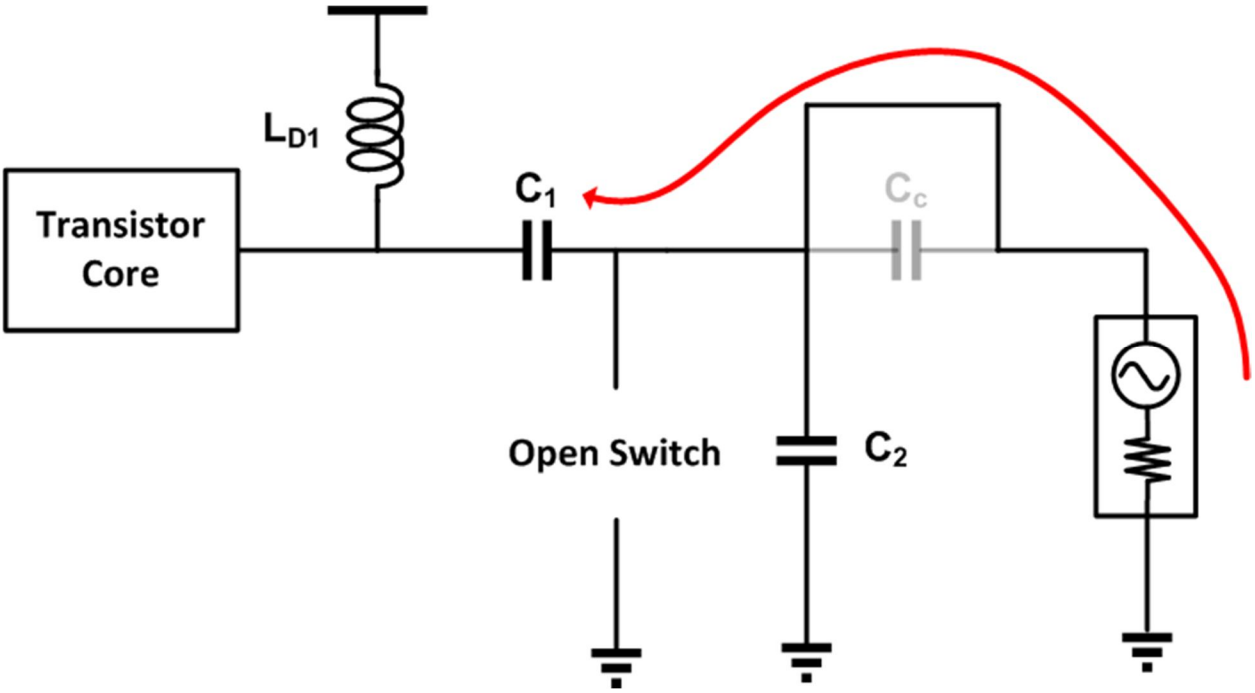


Figure 6-5: Single-ended Matching Network

Considering ideal switches, the signal flow is shown in the figure. The antenna sees an effective tapped capacitor matching network.

It is also useful to observe the impedance change on the smith chart as we add components to the circuit. Ideally we start with a real impedance of the antenna which is presented to the matching network. This is typically 50 Ω. The matching network converts this to higher or lower impedance as per the requirement. In the case of a power amplifier that transmits power in the order of a few mW, the impedance is transformed from 50 Ω to a higher value dictated by the output power requirement.

Addition of passives causes a change in the impedance as shown in the smith chart. The loaded Q of the matching network is also governed by the movement of the impedance along the smith chart. (Figure 6-6)

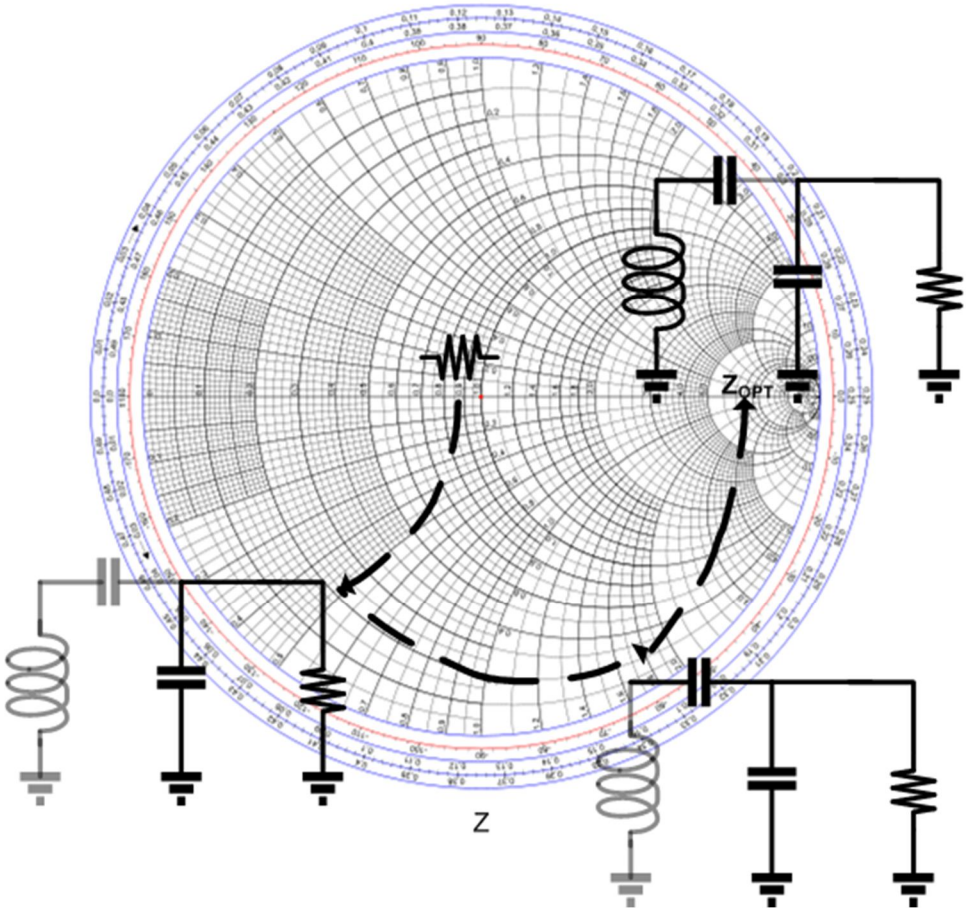


Figure 6-6: Impedance Movement along Smith Chart

The design of a reconfigurable matching network involves awareness of two specific things. The first one being the contribution from the other portion of the network that is turned off and second, parasitics involved with the signal path due to all the passives. Presence of switches in the series path further complicates the design as a switch can contribute both resistance and capacitance to the network. While addition of a resistor does not change the phase of the

impedance, it does reduce the matching network efficiency significantly if not designed properly. The Figure 6-7 below shows the output matching network with the parasitic capacitances added to each node. For a lack of a better convention a large resistor is shown by the red annotation. The parasitics are added at every node. Parasitic capacitance Cp2 is in parallel with the matching network capacitor C3 and the value is higher than the sum of the coupling capacitor CC2 and the parasitic Cp1. Hence the net capacitance added to the design capacitor C2 is taken into account while designing for it.

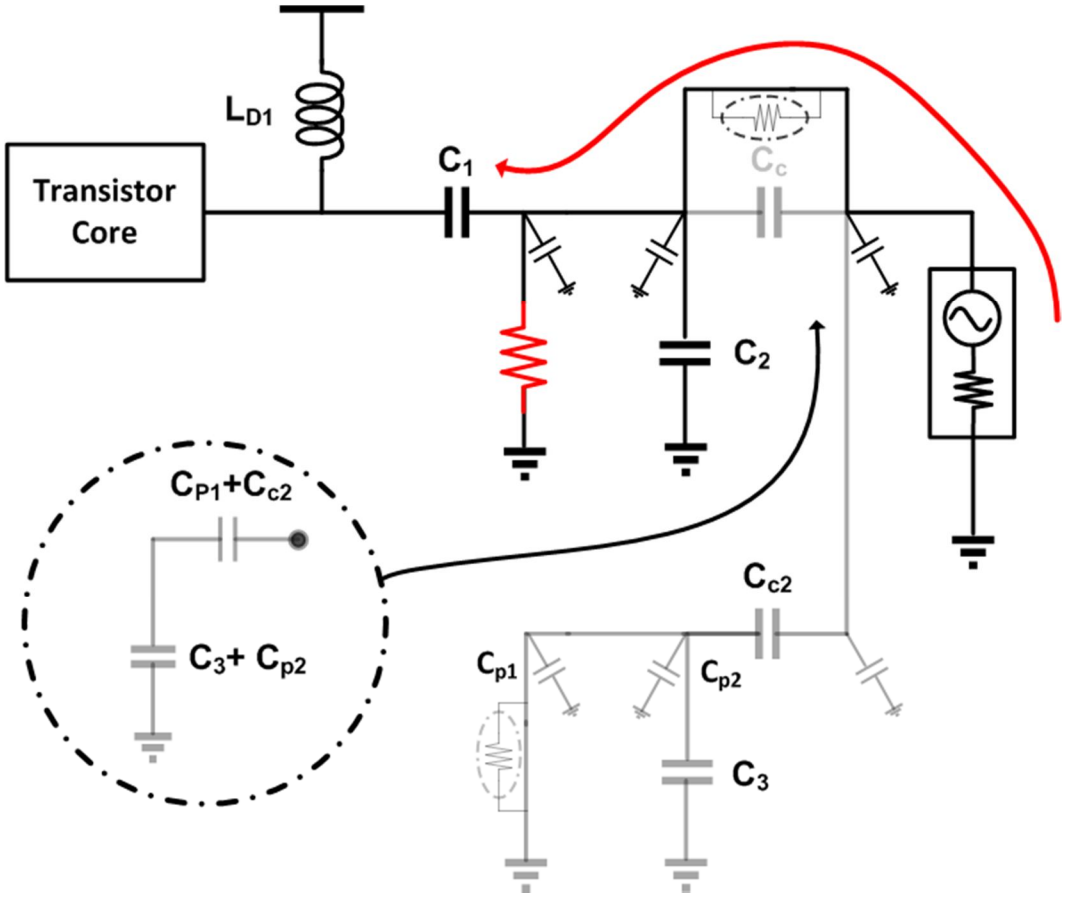


Figure 6-7: Parasitics in the Matching Network

7. PVT Tolerant Class C Power Amplifier

A power amplifier biased in the class C mode depends on the gate drive to turn the device on and off. As the gate drive increases above the threshold voltage of the active device, it sets up a finite drain current. The first harmonic of drain current flows into the output resonant network and is responsible for the output power. Consequently, the power amplifier's main characteristic, the output power is highly dependent on the threshold voltage of the transistor. In a given process a fabricated transistor may be a fast, slow or nominal with equal probabilities. Hence it becomes critical to have some kind of calibration loop that sets up the bias voltage to transmit a constant power. The advantage of the architecture shown in Figure 4-6 is that the resistors R_{bias} are not only used to bias the class C amplifier but can also be setup to mitigate PVT variations.

Process variations create deviations from the nominal values which in turn vary the circuit functionality. Designers, in their effort to account for the variations, verify the performance under extreme process conditions under the assumption that a circuit performing at the extremes should be able to function properly in the nominal condition. For doing this, five different SPICE model decks are used to determine the performance under extreme conditions. Figure 7-1 shows the different bins with a two letter acronym indicating the relative performances of a *p* and *n* channel device generated with maximum and minimum values of saturation current and threshold voltages.

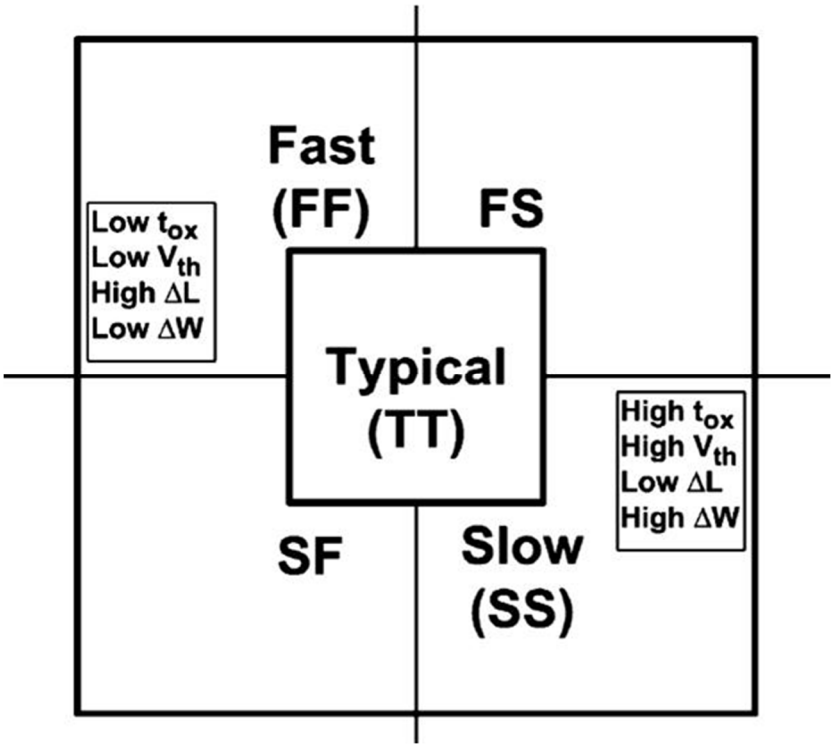


Figure 7-1: PVT Corners

A fast device means lower threshold voltage value and a slower device means higher threshold value. In terms of output power, a faster device has a higher output power in comparison to the slower one assuming the input gate drive is held constant. Clearly this is undesirable as far as the power amplifier is concerned. Fortunately this situation can be remedied by adaptively varying the bias voltage. The input drive is given by

$$V_{inpDrive} = V_{dc} + V_{rf} \sin \emptyset$$

V_{rf} is controlled by the prior driver stage or by the VCO in the case of direct conversion transmitter. Vdc can be adjusted to mitigate the change in the threshold voltage V_{th}. Maintaining a constant difference between the threshold voltage and the applied bias enables constant output power to a first order. This idea is further explained using the Figure 7-2 below.

For the different process corners the V_{th} moves as shown in the figure. So if V_{th} changes, P_{out} changes and that is undesirable. But the good thing is it is fixable fairly easily. If V_{th} moves down, i.e. reduces then all we need to do is the move the entire signal downward so that the net signal swing above V_{th} remains the same. Similarly for V_{th} moving up, we need to make it move up! And this is accomplished by changing the DC bias.

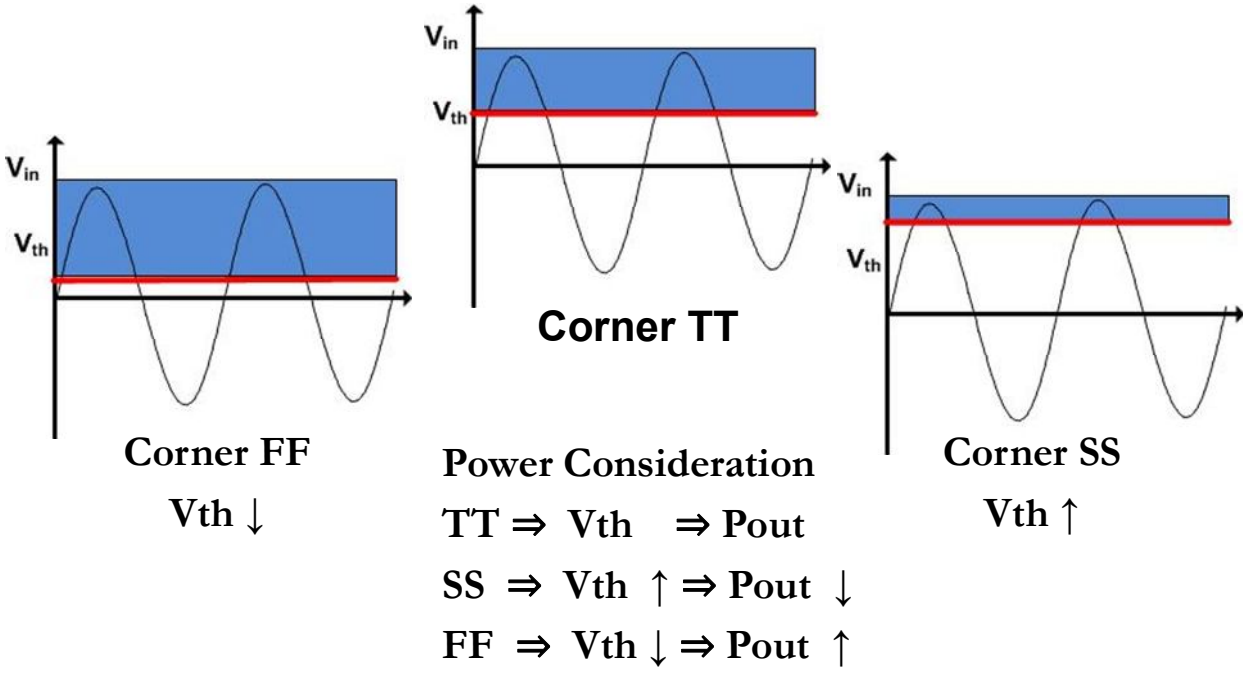


Figure 7-2: PVT Variation Effects

An open-loop ultra-low power calibration loop is implemented to achieve this. This is explained in the section below.

7.1. PVT Calibration Loop

The block diagram shown in Figure 7-3 is used for the PVT calibration. A ring oscillator is used as a PVT detector. In other words, the frequency of the oscillation of a free-running ring oscillator

is proportional to the PVT. The varying frequency implies the time period of the square wave also changes. The square wave controls the charging time for a capacitor. The capacitor is allowed to charge for a fixed number of cycles set by the N-bit counter. Once the end of count is reached, the capacitor is disconnected from the rest of the circuit and the voltage is maintained on the capacitor which now serves as the bias voltage to the PA. The following sections describe each block in detail.

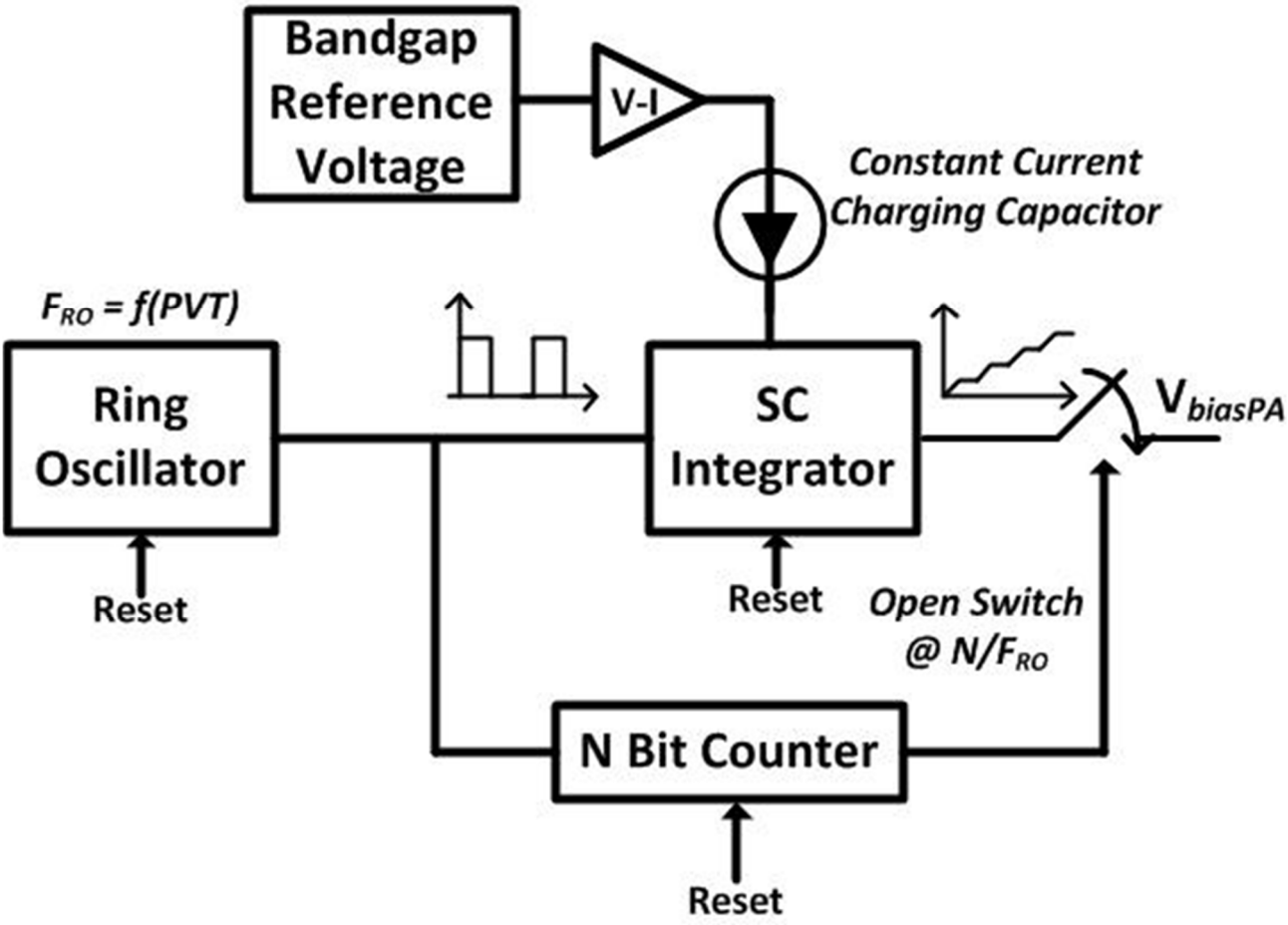


Figure 7-3: PVT Calibration Loop

7.1.1. Ring Oscillator

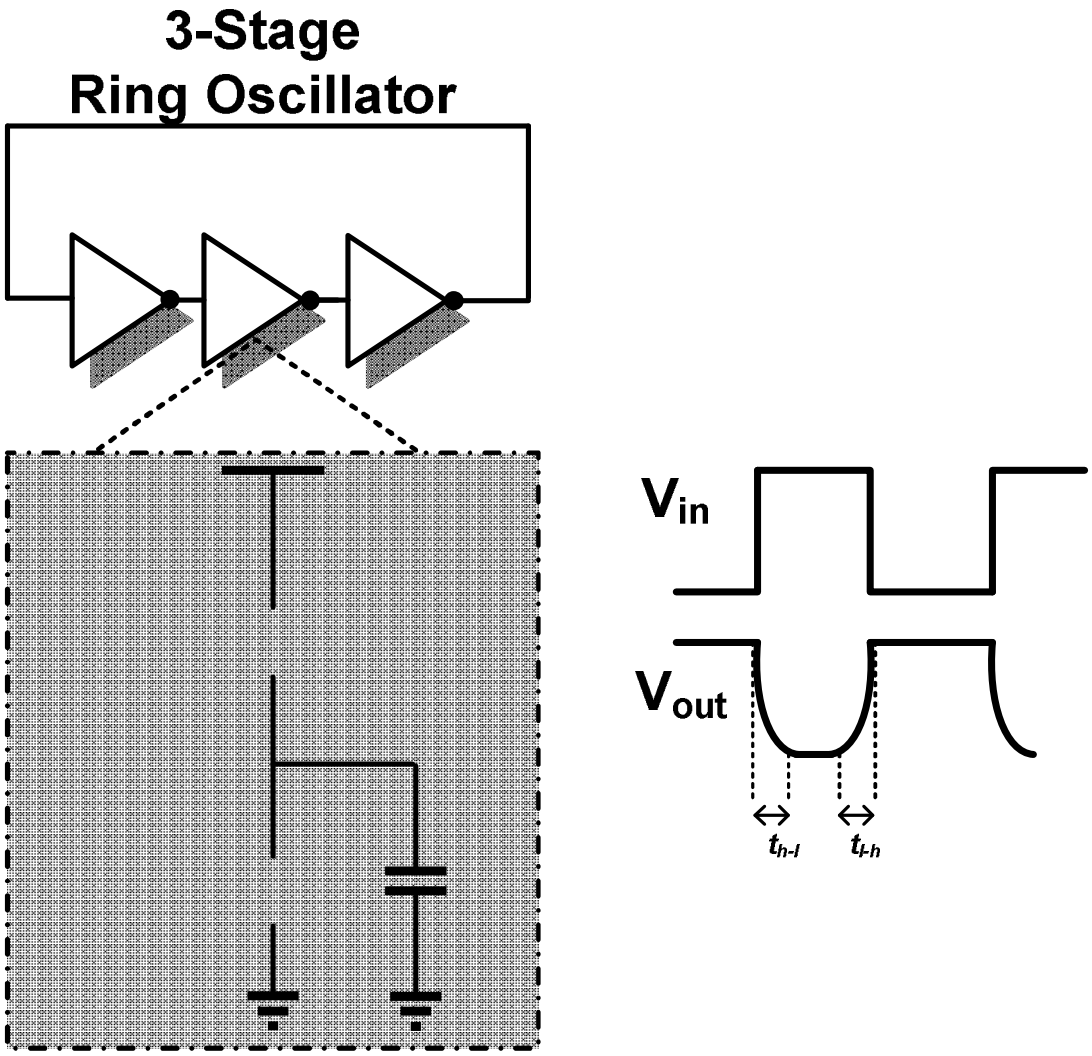


Figure 7-4: Ring Oscillator

A three stage ring-oscillator is presented in Figure 7-4. Individual delay cells are shown in the inset. A small amount of capacitor is added to each stage to keep the oscillation frequency small. The main idea behind this is to keep the power consumed in the digital stages to be as low as possible. Power is proportional to rate at which the gates need to toggle. Hence a slower

oscillating clock not only saves power for the digital block but also prevent it from injection any kind of noise into the other sensitive RF circuits.

Since the core is directly coupled to the power supply, the frequency of oscillation is directly proportional to the variations in the power supply. It is informative to look at the propagation delay of the unit inverter cell. The charging time is calculated using the following circuit (Figure 7-5).

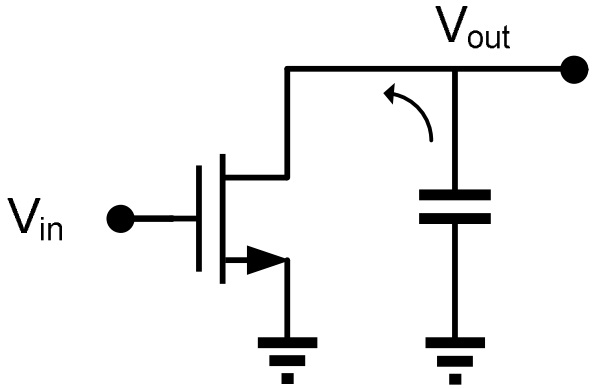


Figure 7-5:Delay Cell Charging/Discharging Time

KCL analysis on the output node gives:

$$C_l * \frac{dV_{out}}{dt} + I(t) = 0;$$

C_l is the effective capacitance on the drain node. It consists of both the designed value and the parasitic capacitor. For simplicity, the device is assumed to be in the saturation region to show the dependence of the frequency with the power supply variations.

$$I(t) = k_n(V_{in} - V_{tN})^2$$

An input voltage step causes a capacitive discharge at the output which has a shape that looks an exponential delay. The delay time is a sum of two individual delays. The output capacitor is discharged from high to low when the input is high and this is controlled by the NMOS. Similarly the capacitor is charged to the supply rails through the PMOS device. Hence the two parameters th-l and tl-h are controlled by different devices and hence are independent of each other to the first order. The time period th-l is given by:

$$t_{h-l} = \frac{C}{k_n}\left(\int_{Vdd-Vtn}^{Vdd} \frac{dv_0}{(Vdd - Vtn)^2}\right)$$

$$t_{h-l} = \frac{C}{k_n}\frac{V_{tn}}{(Vdd - Vtn)^2}$$

The same argument holds good for the PMOS charging the capacitor to the supply. The charging time is given by:

$$t_{l-h} = \frac{C}{k_p}\frac{|V_{tp}|}{(Vdd - |V_{tp}|)^2}$$

The oscillation time-period is given by $3*t_{delay}$

$$t_{delay} = \frac{t_{h-l} + t_{l-h}}{2}$$

The frequency of the ring oscillator is plotted as a function of voltage and temperature.

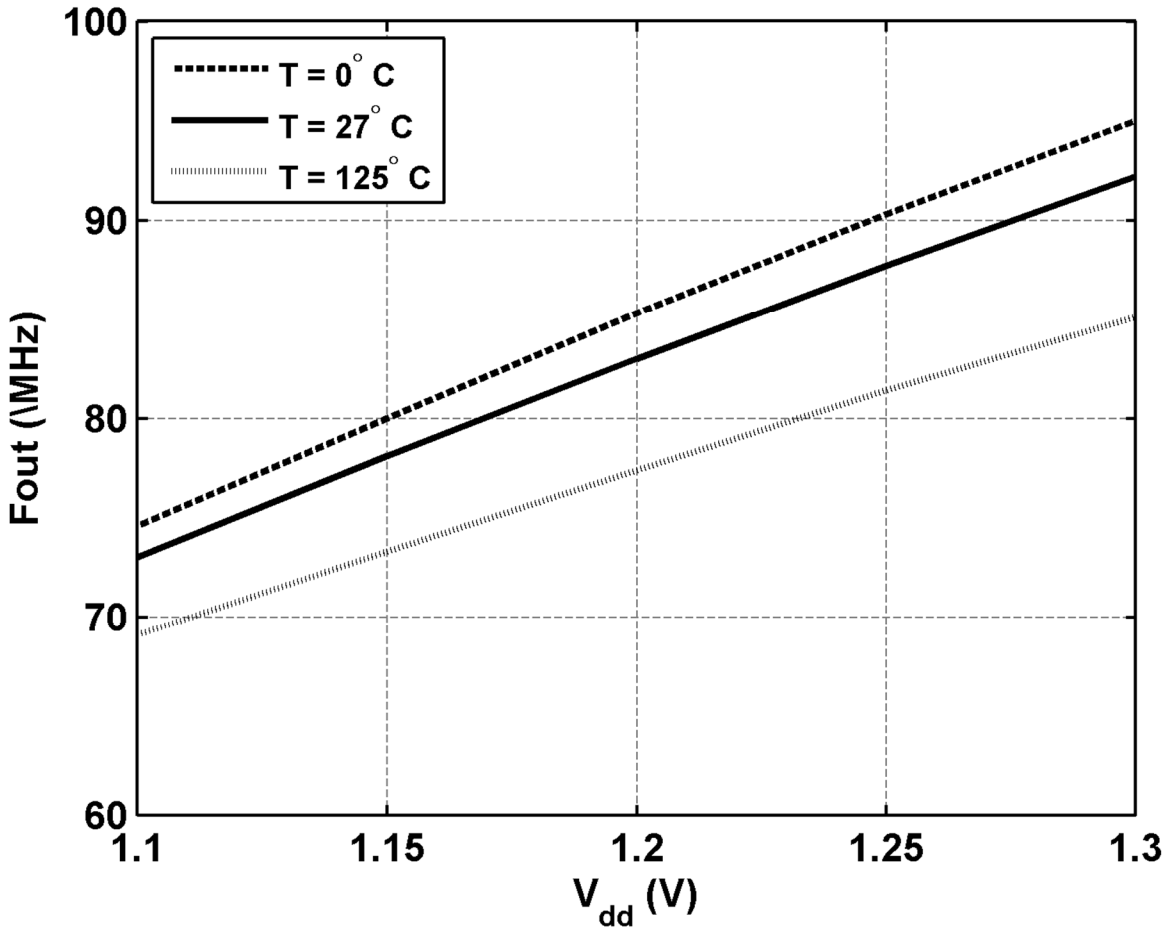


Figure 7-6: Ring Oscillator Ouput Frequency as a Function of Voltage and Temperature

As it can be observed from the Figure 7-6, the frequency of the ring oscillator varies with the supply voltage (V_{dd}) and the temperature. The three different temperature sweeps are shown in the figure above. This variation in frequency and consequently the time period of the waveform is converted to a voltage variation using a switched-mode integrator which is described in the section below.

7.1.2. Switched Mode Integrator

The integrator along with the charging and reset switches is shown in Figure 7-7. The input time domain waveform from the ring oscillator is split into two non-overlapping clocks Φ_{charge} and $\Phi_{chargeb}$. At the beginning of a compute cycle, Φ_{reset} resets all capacitors. Once the reset phase is done, during Φ_{charge} the capacitor is charged by a constant current source. This causes a linear increase in the voltage across the capacitor. During $\Phi_{chargeb}$ the voltage is held on the capacitor. This is repeated for 16 cycles and once the count is reached, the capacitor is effectively disconnected from the rest of the circuit and holds its value. This voltage might need refreshing every once a while but that is easy to accomplish.

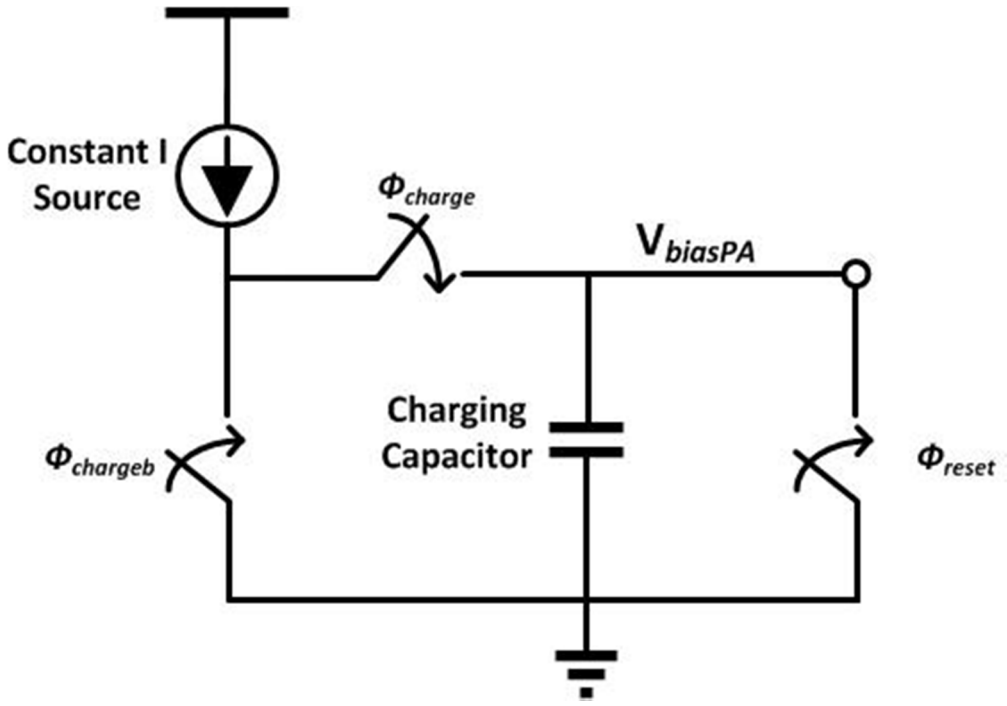


Figure 7-7: Switched Mode Integrator

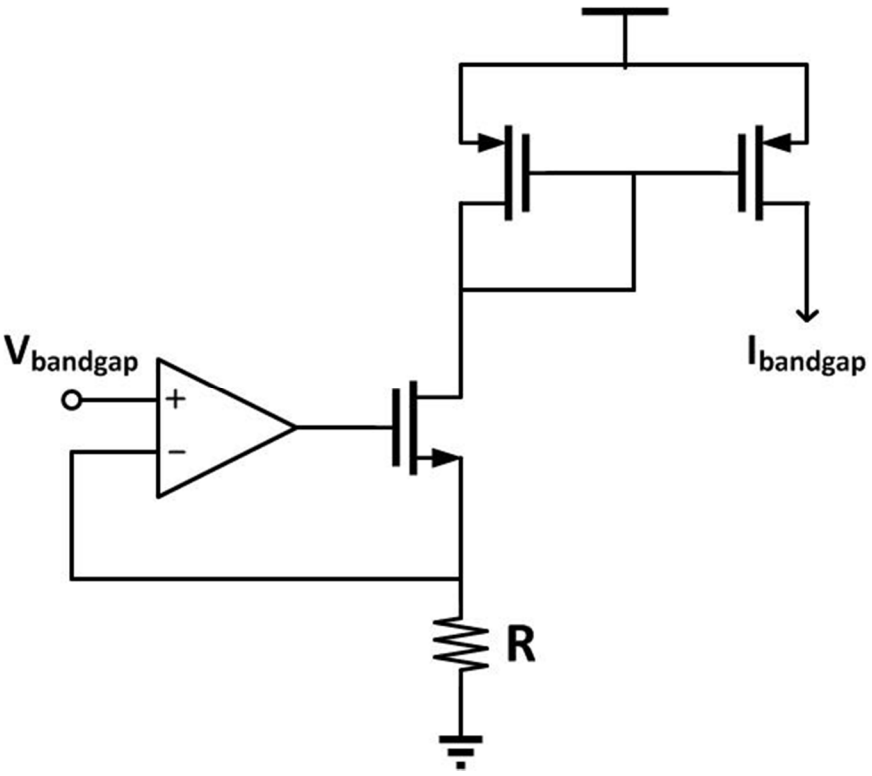


Figure 7-8: Voltage to Current Converter

A PVT stable source is obtained from the bandgap generator and the bandgap voltage is converted to a current using feedback circuit as shown in Figure 7-8

The low-power opamp along with the NMOS and resistor sets up a current equal to $V_{Bandgap}/R$. The opamp's virtual ground forces the voltage across the resistor R to be the same as the input to the non-inverting terminal. A current mirror is used to copy the current across and is used as the constant current source in the integrator block of Fig. 22.

7.1.3. Timing Diagram

The entire description of the calibration circuit can be easily explained using the timing diagram shown in the Figure 7-9.

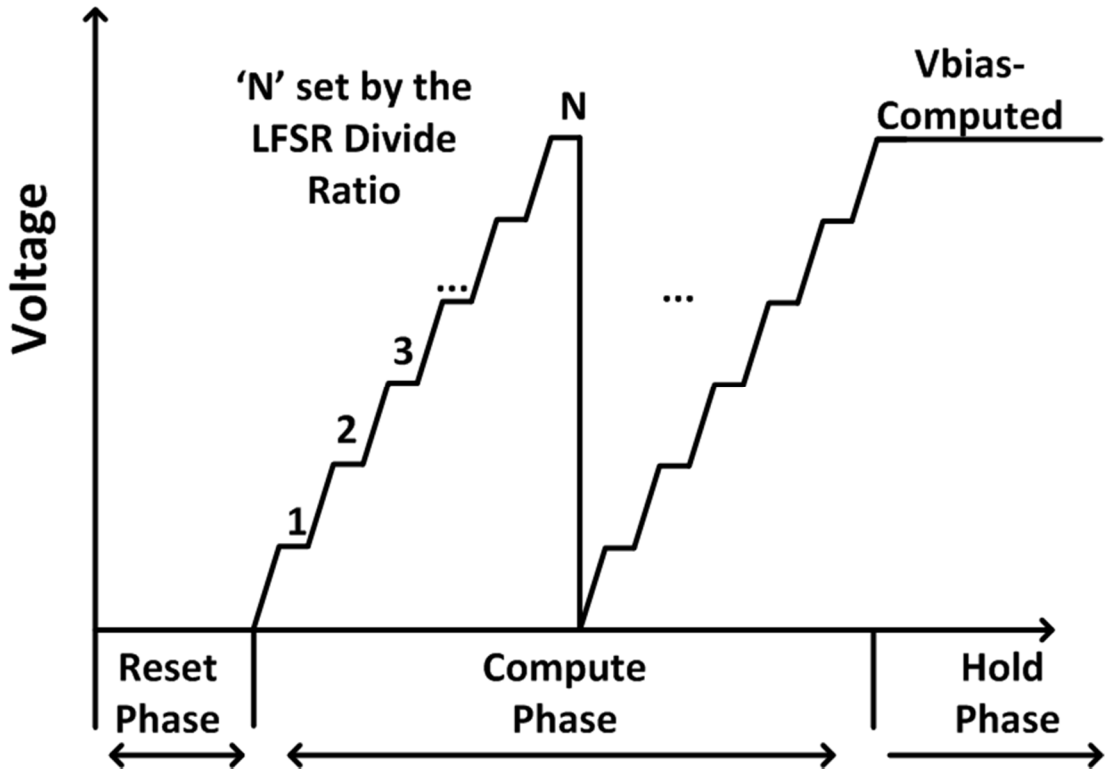


Figure 7-9: Calibration Loop Timing Diagram

The circuit operation can be split into 3 distinct phases.

1. During the reset phase, all the digital circuits are being reset. (This is done using an external sync pulse that is supplied on the board before calibration loop is activated)
2. After the reset is done, the counter begins counting the pulses coming from the Ring-Oscillator (RO). During the t_{on} time of the RO, the constant current is charging the capacitor, so we observe a linear ramp of output voltage. During t_{off} , any possible discharge paths are disconnected.
3. This linear ramping of voltage continues for N cycles set by the LFSR divide ratio.
4. At the end of the LFSR count, everything is disconnected from the charging capacitor.

5. To avoid any false starts or any bad compute cycles, steps 2-4 are repeated for 4 cycles and once they are done, the digital circuits including the oscillator are disconnected and the voltage bias to the PA is maintained, in essence powering down the entire calibration loop.

Measurement results are presented in the next chapter.

8. Experimental Results

The design strategies for implementing a power efficient transmitter were discussed in the previous chapters. These ideas which include the reconfigurable power amplifier along-with the PVT calibration loop and the ultra-low power frequency synthesizer are implemented on silicon. This chapter presents the comprehensive descriptions of measurement results of each block.

8.1. Process and Layout.

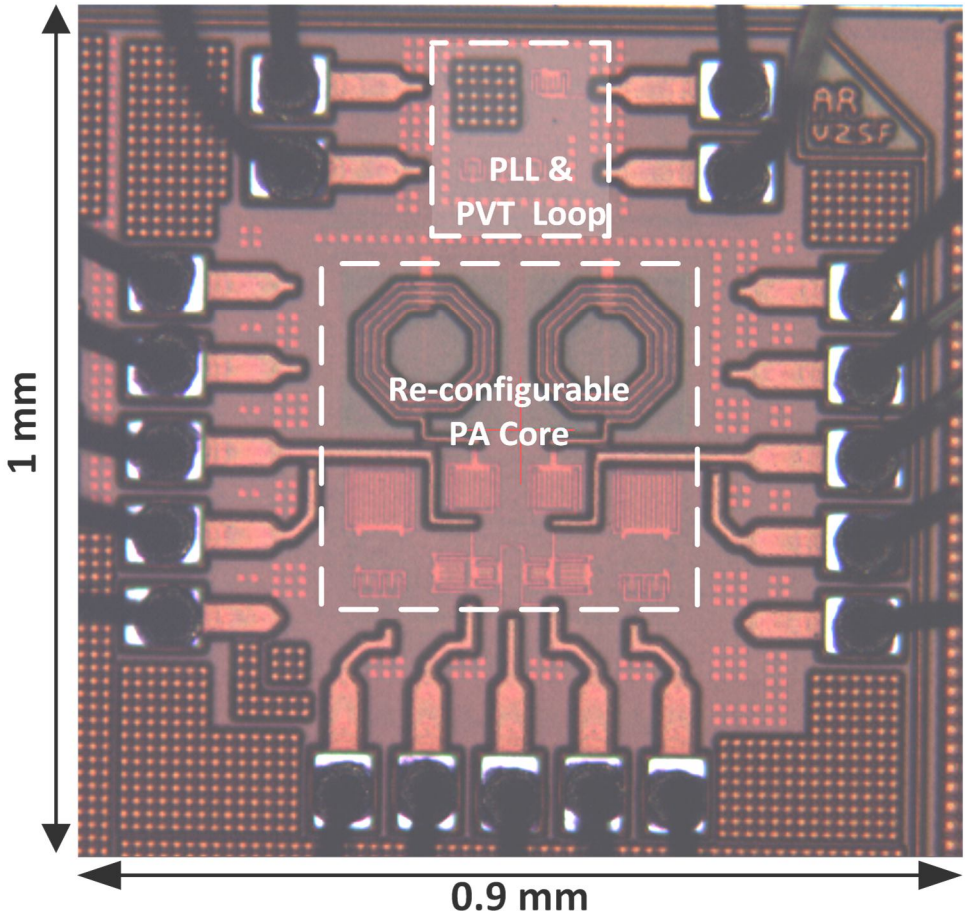


Figure 8-1: Chip Micrograph

The reconfigurable PA, low power PLL and the open loop calibration circuits is implemented in the IBM 130nM CMOS process. It is a single-poly, eight metal RF CMOS process. The chip micrograph is shown in the Figure 8-1. The overall die-area is 1mm*0.9mm including the bonding pads with the active area being 0.41mm^2. The top metal is 4µM thick aluminum which helps in the realization of high quality factor on-chip inductors for the harmonic trap. High density MIM capacitors (4 fF/µm^2) allow minimizing the die-area for the input stages in the PA.

Owing to the symmetric nature of the PA, the differential positive and negative lines of the core are carefully laid out to prevent layout mismatches. Power supplies are separated for the different cores of the transmitter like the VCO, PA and the digital circuitry of the PVT compensation loop. Multiple pads and multiple bonding are used to minimize common mode noise from the bonding wire inductance.

8.2. Test Setup

The test setup is shown in the Figure 8-2. To test the PLL, the RF signal generator supplied the input reference frequency. Phase noise was characterized using the signal source analyzer and the spectral measurements were done using the spectrum analyzer. The existence of various digital signals necessitates the need for inputting digital control to the chip. The digital control was sent to the board from the computer using the Aardvark SPI interface. Open loop calibration circuit measurements need to be performed under varying temperature setting. Thermal measurements were done in the temperature chamber.

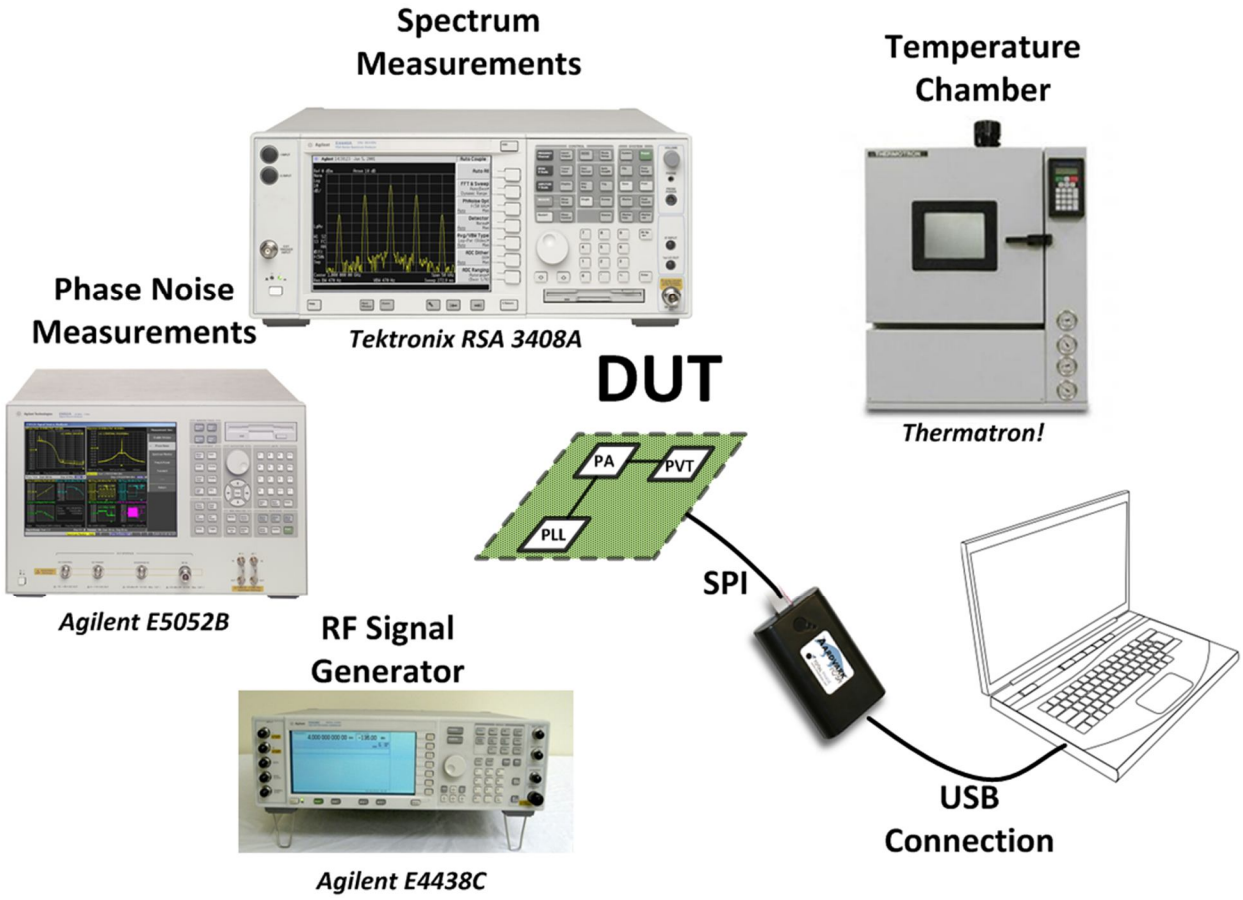


Figure 8-2: Test Setup

8.3. Printed Circuit Board Design

To minimize the package parasitic inductance and capacitance, the circuit is not packaged but embedded on the PCB through chip-on-board (COB) packaging. The COB has advantages of high packaging density (size, weight and volume), short interconnects to improve signal integrity, applicability to most substrates, adaptation to high frequencies and layout flexibility. With COB, the bypass capacitors can be put much closer to the circuits compared to a conventional package.

The bare silicon die is placed on the FR4 substrate PCB. The PCB is designed as a four layer board. Each on-chip pad has a corresponding pad on the PCB. The PCB pads are coated with gold to ensure proper adhesion of the wire-bonding. A pure gold bonding wire connects each on-chip pad to the corresponding pad on the PCB. PCB design is critical for measurement purposes. Any non-idealities in the board design can directly affect the performance of the chip. Careful selection of components is tantamount in getting realistic results.

Various power/ground supplies are used in the board. This includes supplies to the PA, PLL and the digital circuitry of the PVT compensation loop. Ground signal associated with these supplies can cause ground loop problems which degrades the performance severely. Different ground signals are connected together. This is done by covering the entire third layer of the PCB with copper and using it as a ground plane. The PCB was designed using Altium designer software.

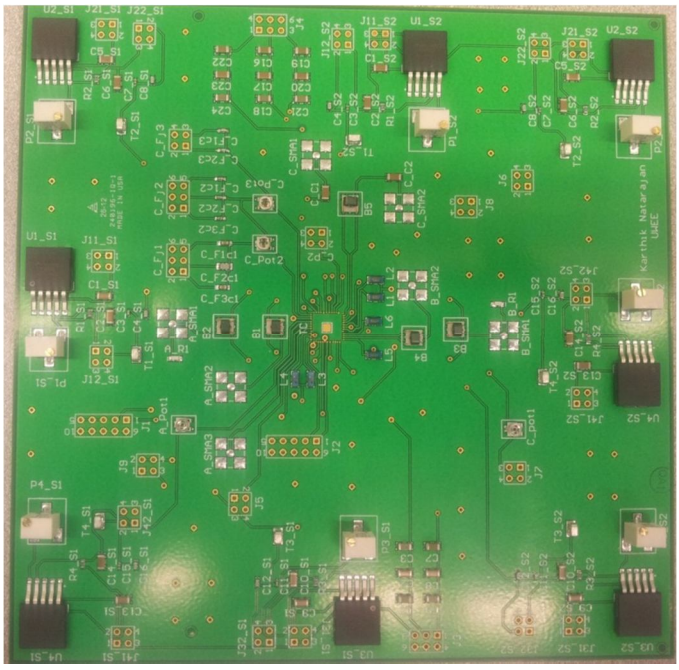


Figure 8-3: Printed Circuit Board

8.4. PLL Performance Results

Figure 8-4 shows the tuning characteristics of the PLL. The control voltage is swept from 0.6V to 1.2V as the output frequency is noted. As it can be observed the tuning range is limited because of the NMOS delay based architecture. The measure K_{VCO} is around 140MHz/V with the V_{DD} set to 1.1V. The tuning range obtained from varying the power supply V_{DD} is higher and can be used to adjust the self-oscillating frequency of the ring VCO in such a way that the loop is able to lock given the limited tuning range of the oscillator. The measured K_{VDD} is close to 500MHz/V when the V_{tune} is held at 0V.

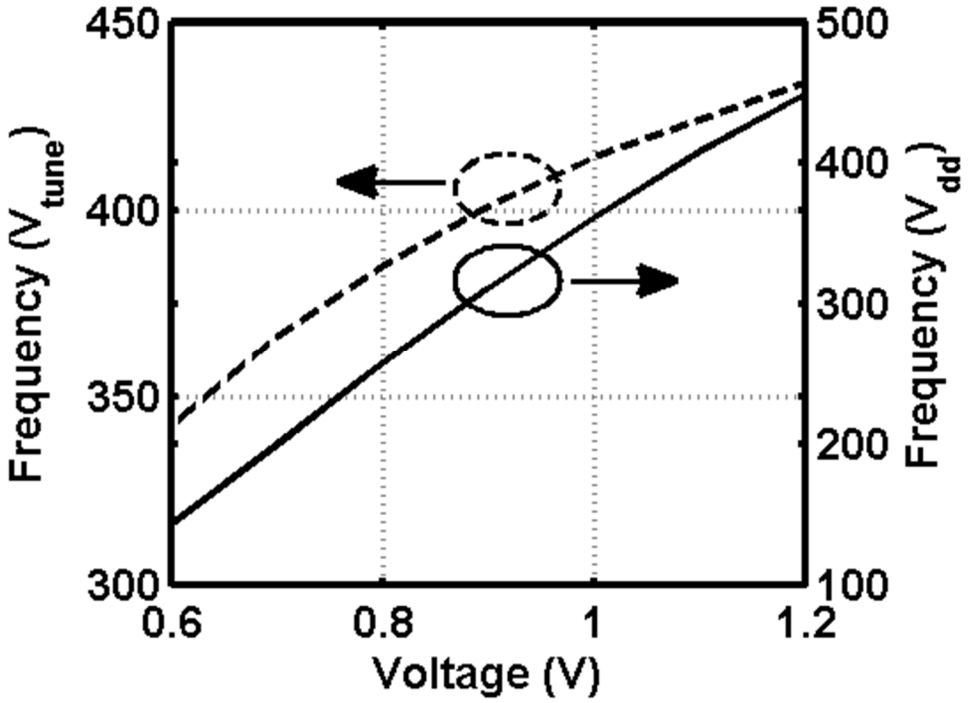


Figure 8-4: PLL Tuning Characteristics

The phase noise requirement for the PLL is governed by the MedRadio channel mask. This is shown in the Figure 8-5. The MICS (MedRadio) defines the mask in the 402MHz- 405MHz. The channel bandwidth is 300 KHz and the fundamental to the first lobe is 20dB. This translates to a phase noise requirement of -70dBc/Hz spot phase noise at 150 KHz offset frequency.

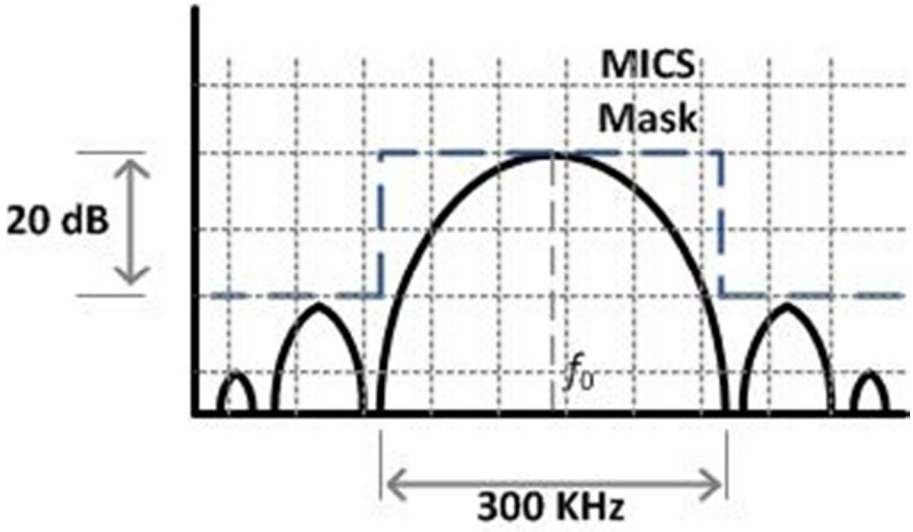


Figure 8-5: Spectrum Mask for MedRadio

$$Phase\ Noise = \ -20\ {}^{dBc}/_{Hz} - 10\log 150K = \ -\frac{70dBc}{Hz} @\ 150KHz\ offset$$

The phase noise plot is shown in the Figure 8-6. The phase noise profile is shown at a charge pump current of 10µA. The -3dB bandwidth is around 80 KHz, thus having a maximum data-rate of 80Kbps. Also owing to the relatively small bandwidth, the settling time is around 40µS. The noise profile is shown when the output frequency is at 403.2MHz with the modulation input set at 0. As it can be seen, the spot phase noise at 150 KHz offset is -75dBc/Hz which gives us a margin of almost 5dB from the specification. The minor peaking observed is due to instrument artifacts.

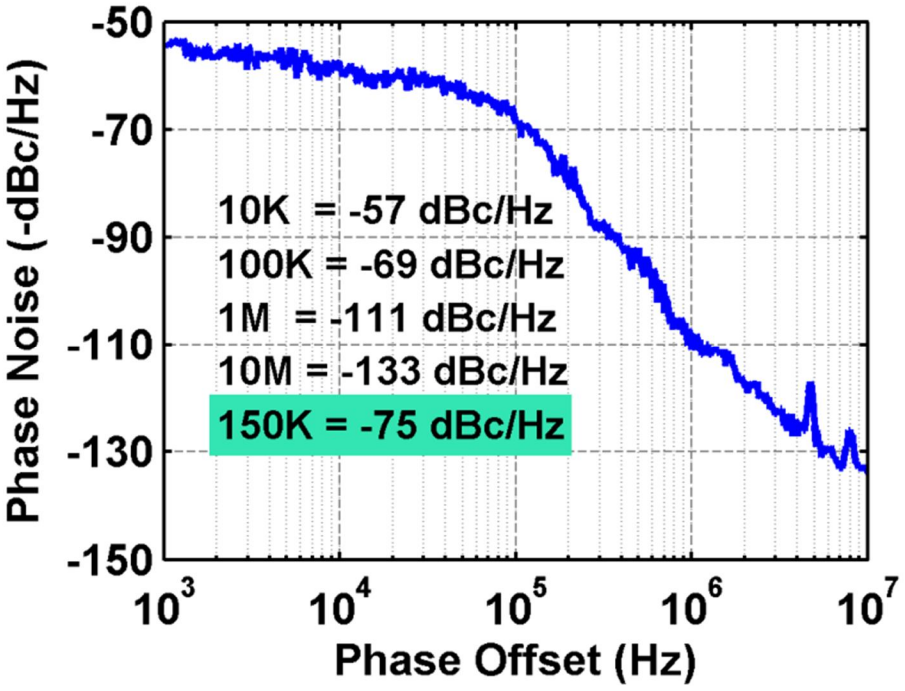


Figure 8-6: PLL Phase Noise

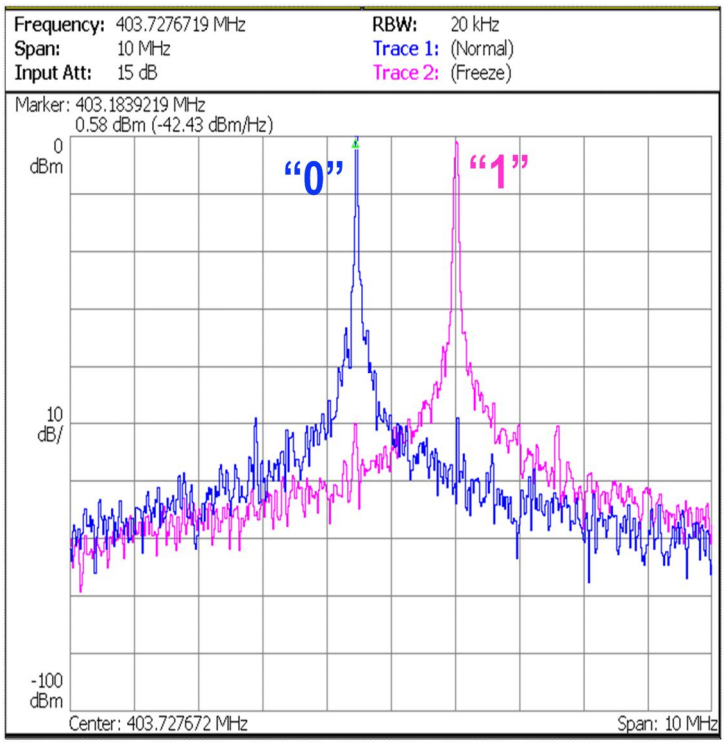


Figure 8-7: PLL Output Spectrum for Different Modulation Bits

Spectral measurements are shown in the Figure 8-7. The two spectrums are shown for different modulation inputs. With an input frequency of fin = 1.575MHz, modulation input of 0 corresponds to a division ratio of 256 and hence giving an output tone at 403.2MHz. Modulation input of 1 corresponds to a division ratio of 257, and the output tone at 404.8MHz.

The measured spur level is around -48dBc as shown in the Figure 8-8

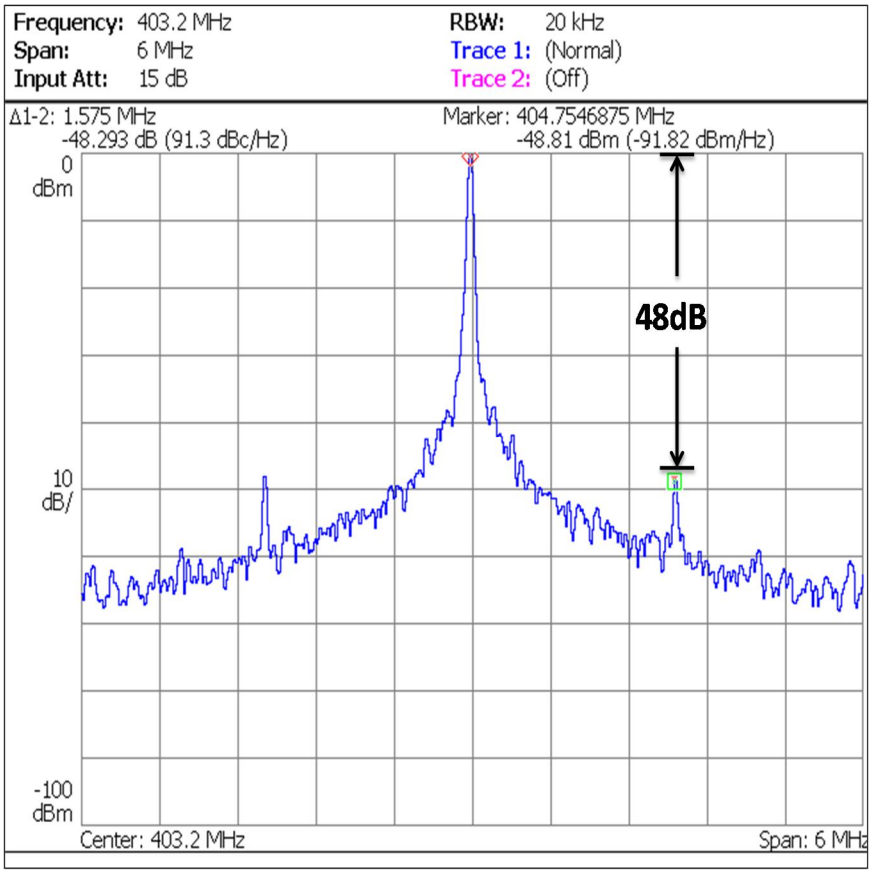


Figure 8-8: Measured Spur Level

8.5. PA Performance Results

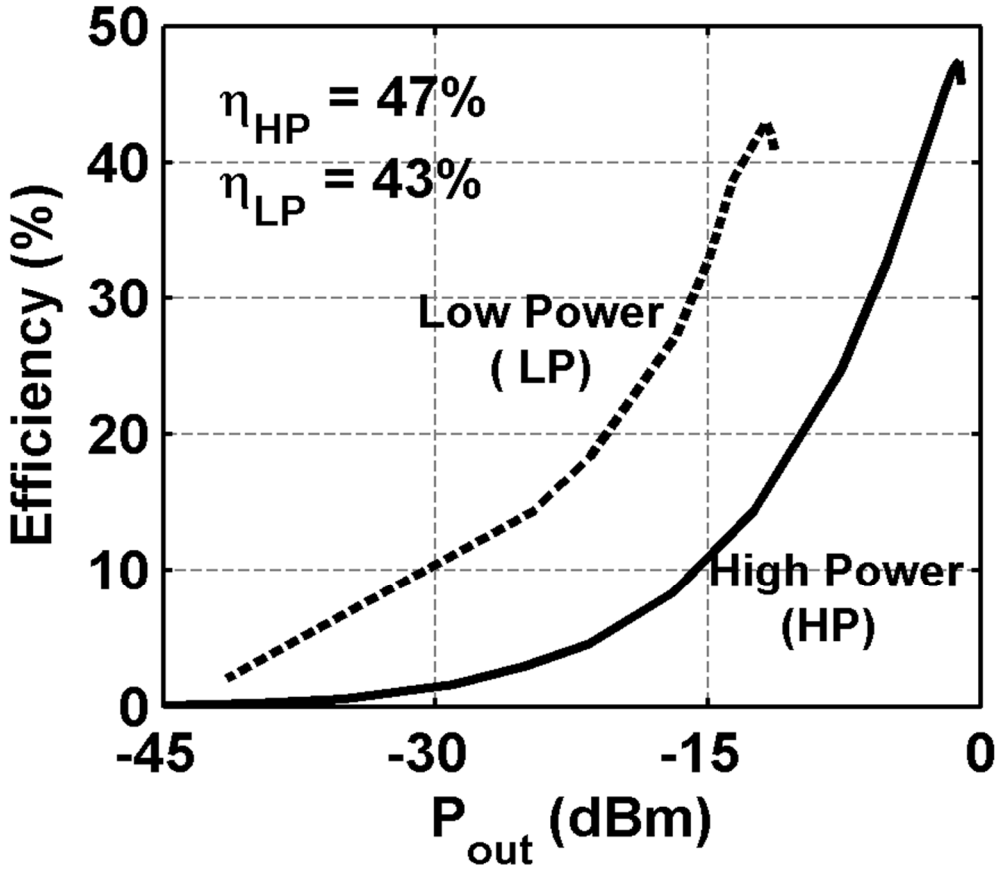


Figure 8-9: Efficiency VS Output Power

The Figure 8-9 shows the plot of efficiency VS output power. As it can be noted there are two different curves of the efficiency plot. They correspond to the high power and the low power modes which are digitally switchable. Mode 0 corresponds to the low-power mode ideally suited for transmission in the MedRadio bands where the EIRP is limited to -16dBm. This maximum transmission distance is limited to a few feet and the overall power consumption of the radio is kept at a minimum.

Mode 1 corresponds to the high power mode where the maximum output power is limited to -2dBm. This setup is ideally suited for reconfigurable medical applications where we need to transmit higher power for two primary reasons: 1) To maintain the radio-link between the transmitter and receiver with increasing distance between the two. 2) To prevent jamming and to enhance wireless data security.

The Figure 8-10 shows the power transfer characteristics of the reconfigurable power amplifier. Input power is varied and the output power is measured. Note that since the output is not wafer-probed, the output is passed through a balun on board to a SMA connector. Consequently the measurements need to be calibrated for the balun losses in the region of the operation.

As the plot indicates, the maximum saturated output power in the mode 0 (Low-Power) is limited to -12dBm or 65µW. This is ideally suited for transmission in the MedRadio band. An interesting point to note is that even though the EIRP for the MedRadio band is limited to -16 dBm, we add a few dBs to the output power. The primary reasoning behind this is irrespective of the line-of-sight of the receiver, there is always a path-loss associated with sensors on the human body. This causes the output power to be reduced the moment a sensor is interfaced with the human body.

High power mode has a maximum saturated power of -2 dBm which is ideally suited for transmission in the 433MHz ISM band.

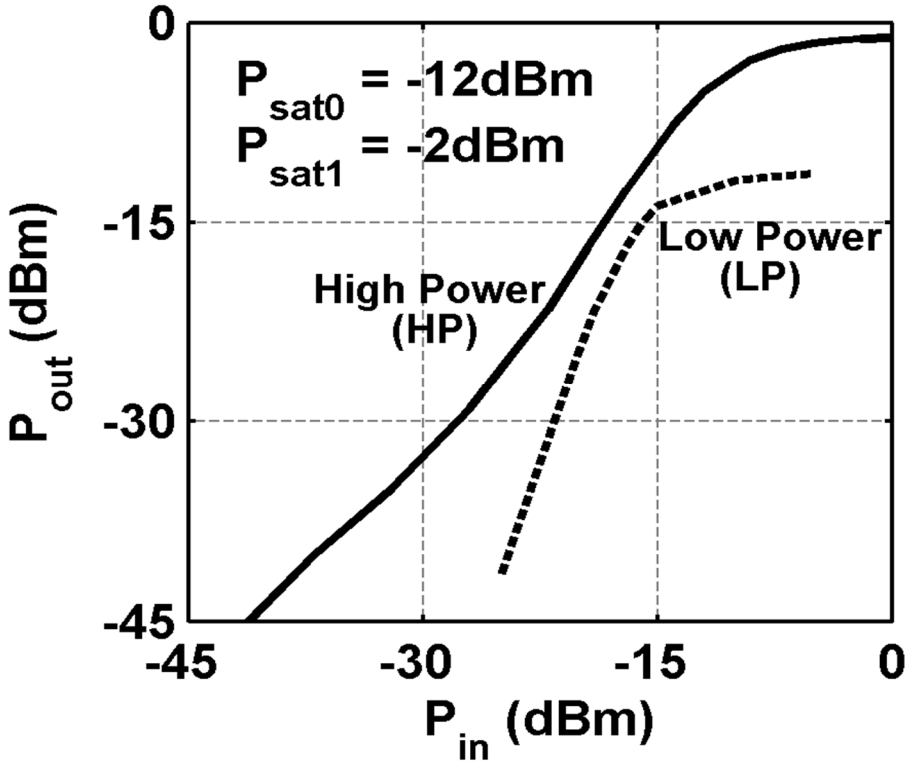


Figure 8-10: Power Transfer Curve

8.6. Tunability measurements

For being able to tune to the MedRadio (405MHz) and the ISM band (433MHz), there are two important measures. The PLL must be able to tune to the required center frequencies and the bandwidth of the power amplifier needs to be large enough to have sufficient gain over the entire band of interest.

The bandwidth of the PA is shown in Figure 8-11. As it can be observed, the bandwidth is close to 70MHz centered around 410MHz making this ideally suited for the two medical bands of interest. The bandwidth is mainly governed by the loaded quality factors of the output matching network.

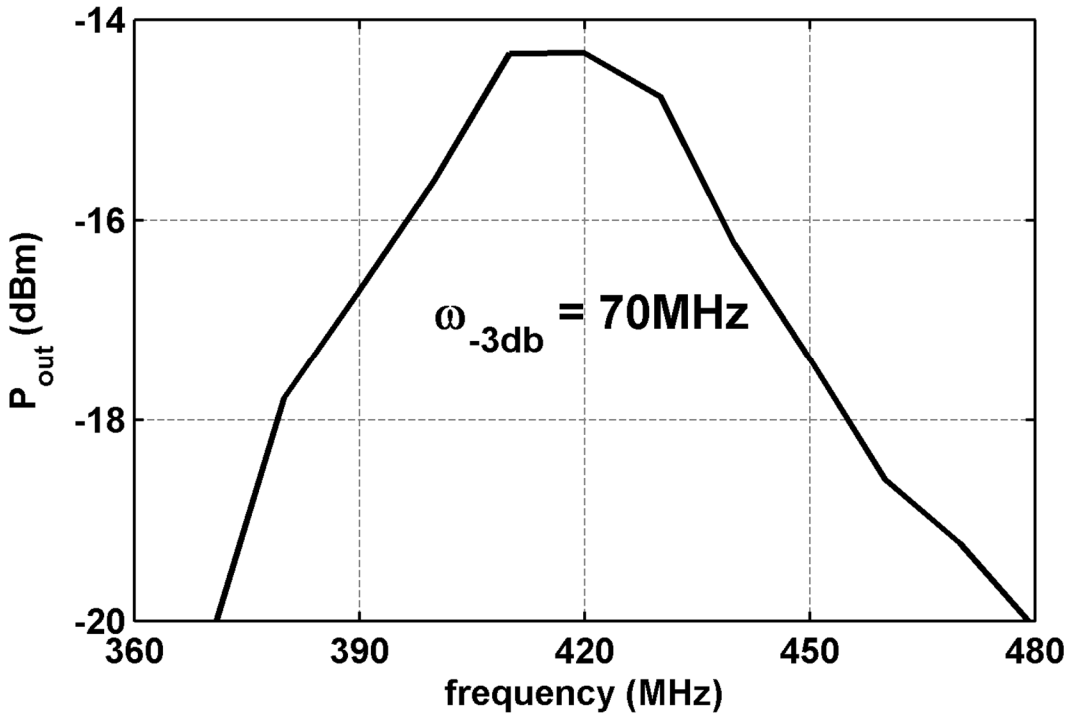


Figure 8-11: PA Bandwidth Measurement

The next set of measurements illustrates the tuning ability of the frequency synthesizer. Input reference frequency is changed from 1.575MHz to 1.692MHz. Figure 8-12 shows the spectral measurement of the output when the modulation input is varied from 0 and 1. The phase noise at the output is shown in the Figure 8-13. As it can be observed, there is only a minor variation in the output phase noise when moving from one band to the other.

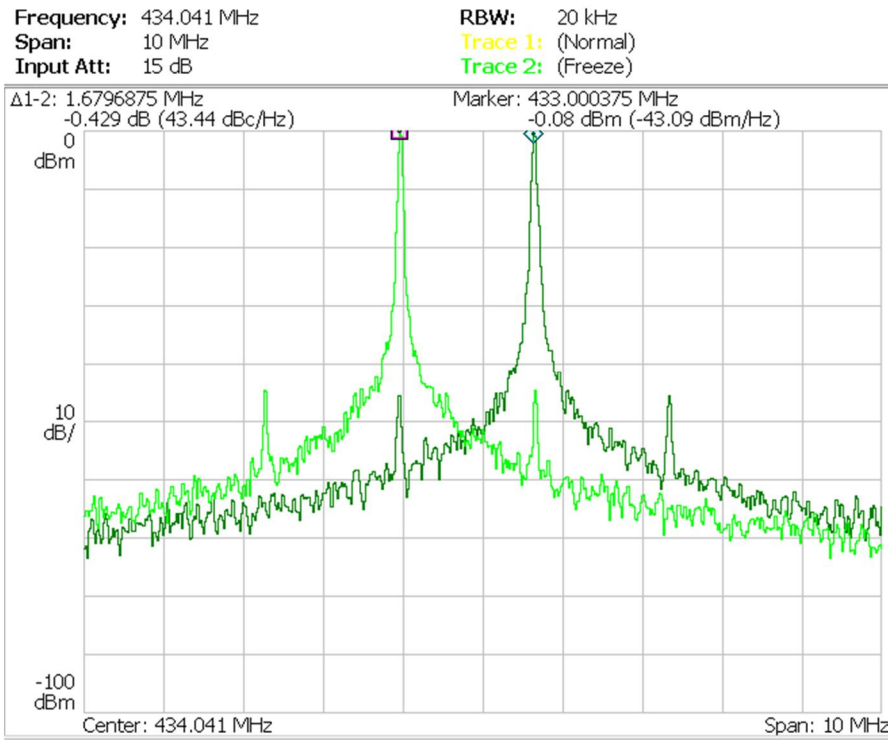


Figure 8-12: Measured Output Spectrum @433MHz ISM Band

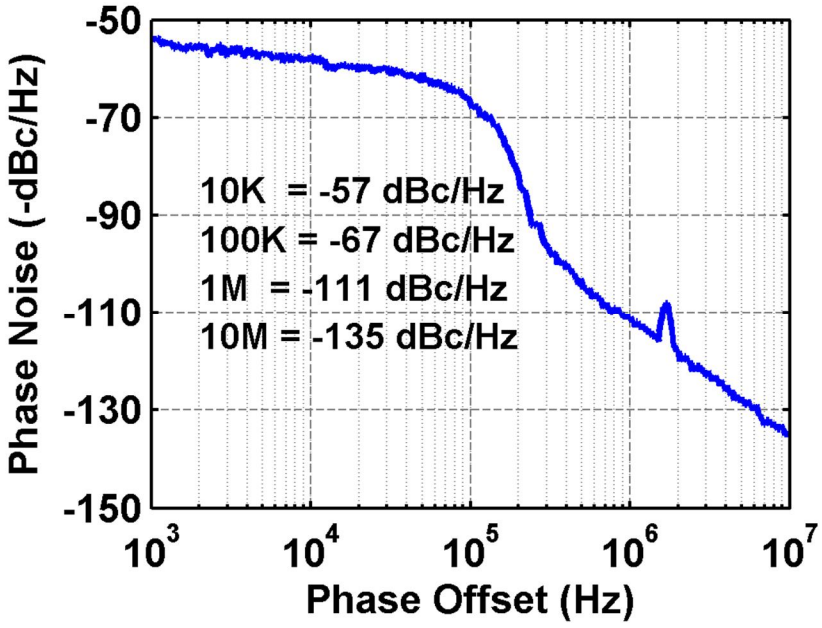


Figure 8-13: Measured Phase Noise @433MHz

8.7. PVT Measurements

The open loop calibration test results are presented in the following section. The calibration loop accounts for variation in the process, temperature and supply voltage drifts. In the real world, we would ideally be able to define the process corner or the skew of the silicon that is fabricated by specially requesting it from the foundry. Voltage and temperature drifts are entirely a function of the environment which the chip is exposed to. The primary target for this work is medical application and body-worn sensors. The human body is a wonderful regulator of temperature with the ideal body temperature around 98F. A change of even 4F on either side is considered extremely dangerous to the human health. In such cases we need to account for only a very small temperature drift. In our work, we have been to demonstrate tighter control of output power over larger range of temperature drifts. The three operating temperatures are 0F, 27F, and 100F.

The power amplifier operates over a nominal voltage of 0.7V. Power supplies are swept ±10% from the nominal value. Again, in real life scenarios, such a large voltage drift is not practical but we have exaggerated the measurements to validate the accuracy of the calibration loop.

Figure 8-14 shows the variation of the output power as a function of supply voltage drift without PVT compensation. The measurements are repeated for three different temperature setting. The absolute difference between the output power P_{OUT} is 31µW and has a standard deviation of 10.63 µW. With the calibration loop turned on, the POUT variation decreases by 30% to 13 µW and the standard deviation reduces by 59% to 4.34 µW. (Figure 8-15)

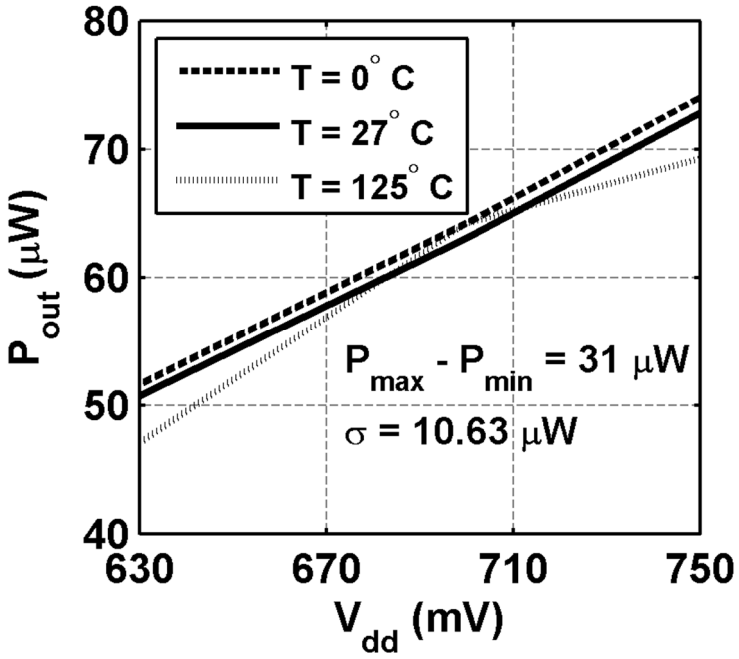


Figure 8-14: Uncompensated PA, PVT Measurements

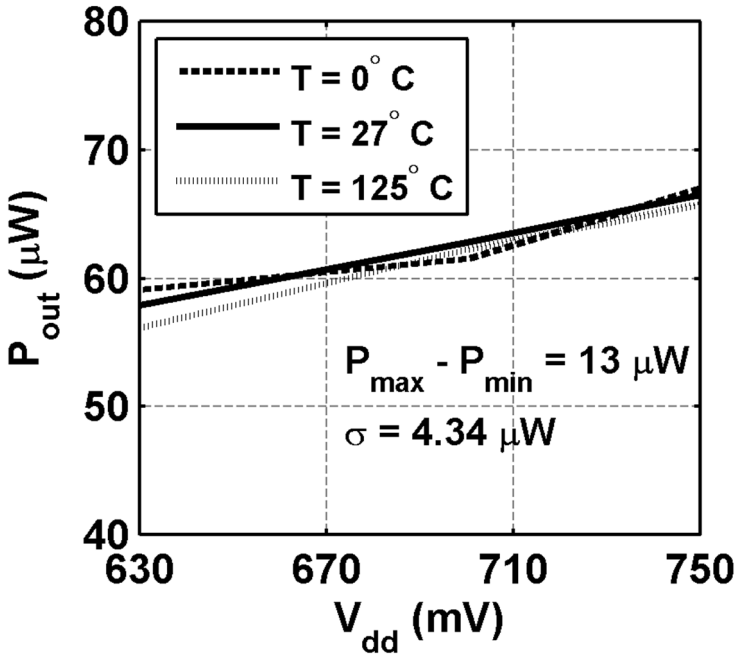


Figure 8-15: Compensated PA, PVT measurements

The presented transmitter is compared with the existing literature in the table. The main innovations for this work are the presence of a truly digital reconfigurable power-amplifier core and the first to be published PVT compensated class-C power amplifier.

Table 8-1: Transmitter Comparison

TX	This Work	[35]	[4]	[3]
Supply (V)	0.7-1.2	1.2	1.2	1
Tech. (µm)	0.13 CMOS	0.13CMOS	0.13CMOS	0.09 CMOS
Area (mm^2)	0.41	0.04	2.5	0.5
Architecture	NDRO-PLL-PA-MN-ANT[1]	Edge-combing PA-MN-ANT	Edge-combing PA-MN-ANT	DCO-ANT
Reconfigurable PA	Yes	No	No	N/A
Modulation Clock Gen.	PLL	ILVCO	DLL	DCO (open loop)
On-chip PVT calibration	Yes	No	No	No
Power Consumption (µW)	150	90	400	350
Output freq. (MHz)	400/433	400	400	400
Max. Data-rate (Kbps)	80	200	100	120
PA efficiency (%) @ o/p pwr. **-16 dBm** **-12 dBm** **-2 dBm**	 33 43 47	 30 29 N/A	 16 N/A N/A	N/A
TX efficiency (%) @ o/p pwr. **-16 dBm** **-12dBm** **-2dBm**	 17 29 44	 23 26 N/A	 5 N/A N/A	7.14 N/A N/A
Modulation	BFSK	BFSK	BFSK	MSK

The overall transmit efficiency is 44% at for a BFSK type modulation. All the compared work use similar or better CMOS technology node. The presented architecture is also the first one to employ a phase locked loop to perform the frequency synthesis. The transmitter can be tuned to function as a low-power short distance transmitter for the MedRadio band or can be digitally selected to operate in the high power long distance transmitter for the ISM band.

The latest published PLL architectures are compared in the table below. The presented work achieves similar noise performance while consuming almost 6X less power in doing so.

Table 8-2: PLL Performance Comparison

PLL	This Work	[36]	[31]	[29]
Supply (V)	0.7-1.2	0.5	0.5	0.6-1.2
Tech. (µm)	0.13	0.13	0.09	0.09
Area (mm^2)	0.02	0.0736	0.074	0.1
VCO type	Ring	Ring	Ring	LC
Power Consumption (mW)	0.072	0.440	0.400	10
Output freq. (MHz)	400/433	400/433	400	5000
PN @ 1MHz(dBc/Hz)	-111	-91.5	-87	-115
Reference Spur (dBc)	-48	-38.5	-40.3	-
FOM[2] (dB)	174.5	147.1	143.0	178.9

[1]MN--matching network, ANT--Antenna

[2]PLL Figure of Merit $(FOM) = -\mathcal{L}(\Delta f) + 20\log\left(\frac{f_O}{\Delta f}\right) - 10\log\left(P(mW)\right);\ \Delta f = 1\ \text{MHz}$.

9. Conclusion

Scaling of CMOS technology and improvements in wireless communications portend a new age of micro-scale wireless sensors with myriad applications. The FCC has allocated spectrum for Medical Implant Communication Services (MICS), specifically for low-power, low-data-rate implanted systems. Conventional wireless sensors consume significant power for the interface circuits, signal processing and wireless transceiver. A battery is not an appropriate energy source because the dissipation would prohibit a small form factor. Alternatively, a smaller battery would necessitate costly frequent replacement, and possibly invasive surgery in the case of a medical implant.

To accomplish this, we proposed to implement a reconfigurable antenna interface. Reconfigurability is needed because of power, frequency and modulation differences between the various standards that exist for medical applications. MICS radios use FSK modulation with an effective isotropic radiated power (EIRP) of 25uW in the 400-MHz MICS band. The 433MHz ISM band supports 30 dBm of output power. The ability to reconfigure the transmitter opens up new opportunities in the field of reconfigurable medical radios.

9.1. Transmitters for Body Sensor Networks [37]

Transmitters for ultra-low-power sensor networks are continuously evolving to transmit low output power in a highly efficient manner. To this end, various architectures have been introduced with trading off distinct advantages and disadvantages. A comparison of several recent transmitter architectures is presented in terms of power efficiency and it is also shown

using theoretical calculations that certain architectures are better suited to efficient ultra-low-power transmission.

9.2. A Class-C Power Amplifier/Antenna Interface for Wireless Sensor Applications

The power budget of a transmitter is critically dependent on the design of the Power Amplifier (PA). Different applications require widely different values for the Effective Isotropic Radiated Power (E.I.R.P). These values range from as low as -20 dBm for Body Area Networks (BAN) to as high as 30 dBm for cellular communications. The PA used as the antenna interface in a wireless sensor consumes significant energy, but substantial energy is saved with proper design.

A class-C PA for operation as an antenna interface in body sensor network (BSN) applications is presented. The PA is fabricated in a 0.13 µm RF CMOS process for operation in the 400 MHz MedRadio band. It achieves a measured peak output power and drain efficiency of -4 dBm and 43%, respectively.

9.3. Reconfigurable Power Amplifier Design

Two class-C power amplifiers are driven by a common driver amplifier. The gain of the driver amplifier is tunable in steps of ~5dB. The individual power amplifiers are configured to work in the class-C mode of operation. The amplifiers share a common antenna as well.

The main challenge when interfacing two individual power amplifiers is the design of the output matching network. At any given point, only one of the amplifiers is function, hence the other path needs to be turned off completely. Active devices can be controlled using a suitable switch

but the passives tend to contribute to the output matching network even if the corresponding amplifier is switched off. As a result, the design of the matching network of each stage needs to take this into consideration. Another related issue is the efficiency of the matching network severely degrades in the presence of unwanted serial impedances. This is particularly true for a matching network designed to have a large transformation ratio. This achieves a truly reconfigurable power amplifier with digitally tuned output power.

9.4. Future Directions:

Design methodology for power efficient ultra-low-power antenna interface was developed. Class-C amplifiers are best suited for BAN applications. This opens up quite a few possibilities in terms of digital power-amplifier design. Digital power amplifiers utilize small unit power amplifiers and combine their output powers using power combining matching networks. Individual class-C amplifiers can be tuned to output a fixed power where they operate at efficiencies greater than 40%.

An open-loop PVT correction method was implemented in this project. Another interesting possibility is to implement a closed-loop PVT detection/correction scheme. Output power is detected using a peak detector. Depending on whether this peak output is higher or lower than a fixed level, the bias voltage input to the PA is suitably adjusted.

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Doctor of Philosophy in Electrical Engineering (*Sep 2012*)

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Advisor: *Prof David Allstot*

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Master of Science in Electrical Engineering (*Aug 2008*)

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Advisor: *Prof David Allstot*

Thesis Title: *A Second Order Quadrature Bandpass Sigma Delta Modulator*

Bachelor of Science in Electrical Engineering (*May 2004*)

BMS College of Engineering Bangalore, India

Advisor: *Prof P.S.Satyanarayana*

Research/ Work Experience:

Research Assistant *(Sept 2007- present)*

Dept. of Electrical Engineering, University of Washington

Quadrature Band-pass ΣΔ ADC:

Design and layout of a novel quadrature bandpass sigma delta modulator to be used in GPS receiver front end. The modulator was targeted to be low power with acceptable performance.

To meet the resolution and the power specifications, a second order continuous time sigma delta modulator was designed and taped-out in IBM 130nm process. The ADC achieved 60dB SNR consuming 4mW. The work was presented in ISSCC 2009.

Single OP-AMP Second Order CT ΣΔ ADC:

A novel continuous-time second-order low-pass ΣΔ modulator is implemented. The loop filter uses one op-amp and the loop is stabilized using 2 negative feedback signals. Modeling of the bi-quad filter and the feedback loop is done using MATLAB and feedback coefficients are calculated using MAPLE.

To be published.

Low Power PA for Biomedical Applications:

An ultra-low power, power-amplifier is designed to operate as the antenna interface for BSN. The PA is fabricated in 0.13 μm RF CMOS process for operation in the 400 MHz *MedRadio* band. It achieves a measured peak output power and drain efficiency of -4 dBm and 43%.

A direct conversion transmitter using the above mentioned PA is designed for the MICS band. The work was presented in RFIC 2011.

Summer Intern (*Jun 2007 – Sept 2007*)

Cypress Semiconductors, Seattle, WA

Design and verification of discrete time ΣΔ ADC used in audio applications.

INTEL Corporation (Jun 2011 – May 2012)

Worked with the Mobile Wireless Group

1) VCO design (65nm CMOS) for low-band of 802.11 standards. Chip taped out and expected back soon.
2) Design of sub-harmonically injection locked ring oscillators for 802.11 standards for the 2.4G and 5.6GHz band in 28nm CMOS process. Injection source derived from a PLL designed to operate in the 800MHz band.

Design Engineer (*Nov 2004 – Aug 2006*)

LSI Logic, Bangalore

Design flow verification of test chips. Complete run of test chip from synthesis to GDSII using native LSI Logic design flow.

Publications:

- **K. Natarajan,** J. Walling and D. J. Allstot, "A Class-C power amplifier/antenna interface for wireless sensor applications", in *IEEE Radio Frequency Int. Circuits Dig. Tech. Papers ,2011*, pp. 549-552
- K.-W. Cheng, **K. Natarajan,** and D. J. Allstot, "A 7.2mW quadrature GPS receiver in 0.13um CMOS", in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 422-423.
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- **K.Natarajan,** S.M. Yoo, J. Walling and D. J. Allstot, "Towards Greener Wireless Transmission: Efficient Power Amplifier Design**",** in *IEEE Int. Conf. on Green Computing Dig. Tech. Papers,* July 2011, pp. 1-4
- **K.Natarajan** et al., "Transmitters for Body Sensor Networks: A Comparative Study", in *IEEE Biomedical Circuits and Systems Conf. (BioCAS*), Nov 2011, pp. 185-188
- **K.Natarajan** et al., "Robust Class C Power Amplifier for BAN Applications**",** *S.R.C. Techcon, Austin, Texas*

Awards

- **Outstanding Teaching Assistant**, Univ. of Washington, Seattle, 2011
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- **J Watumull Scholarship**, Univ. of Washington, 2007
- **Outstanding Student Award**, BMSCE, India, 2003-2004