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Current Mode Processing and Architecture for Optoelectronically Interconnected Arrays

Mohammad Azadeh

A dissertation submitted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

University of Washington

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Program Authorized to Offer Degree: Department of Electrical Engineering

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And have found that it is complete and satisfactory in all respects,
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Date: July 18, 2000

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Abstract

Current Mode Processing and Architecture for Optoelectronically Interconnected Arrays

Mohammad Azadeh

Chairperson of the Supervisory Committee:
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Department of Electrical Engineering

The combination of optoelectronic arrays consisting of optical emitters and detectors with processing electronics constitutes the basis of smart pixel arrays. These architectures present an attractive basis for optoelectronic systems. Ideally, they combine the efficiency of electronic circuits with the interconnection capabilities of optics to achieve improved performance or implement new functionalities. This dissertation deals with optoelectronic interconnections in general, and with the important special case of optoelectronic feedback. Such systems, whether integrated or distributed, open up a variety of new prospects for optoelectronic systems, especially in sensor applications. These concepts are first developed for a single pixel, and then generalized to in a matrix formalism for an arbitrary smart pixel array. An important part of a smart pixel array is the electronic circuits required to interface the optoelectronic devices and to perform the necessary signal processing tasks. A new approach based on a current mode processing architecture is presented and implemented in CMOS technology as an ASIC integrated circuit. Experimental results from two fabricated CMOS chips as well as LED and VCSEL-based optoelectronic arrays are presented.

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To my parents,

without whose support,

I couldn't have achieved any of my goals.

Chapter 1. Introduction

Within the past decades, modern electronics has triumphantly experienced a thorough revolution. This success can largely be attributed to the process of integration, whereby large numbers of semiconductor devices are integrated on a single substrate with ever-shrinking feature sizes. These integrated circuits exhibit improved results over their discrete-device counterparts in terms of speed, size, reliability, performance, cost, and functionality. In fact, many of these modern electronic circuits are unrealizable with discrete devices.

On a rather different track, a new field has been emerged which has come to be known under such various titles as quantum electronics, electroptics, photonics, and optoelectronics. In principle, this field deals with the study of the interaction of photons and atomic systems (electrons). An important milestone in this field has been the invention of the laser. Ever since its invention, the laser has gone through drastic improvements with numerous applications in almost all fields of science and technology. The laser is but one of the new optoelectronic devices available (although probably the most important one). Other light sources, such as superluminescence LED's, quantum light modulators, and various light detectors, are all examples of devices that in one way or another deal with photons in addition to electrons.

An important question arises here: is it possible to combine the advantages of these newly developed optoelectronic devices with the performance of conventional electronics? And if yes, what classes of applications are likely to benefit from such combination? What methodologies should be developed for such hybrid optical-electronic systems to optimize their performance? Is it possible to integrate optical and electronic devices, so as to duplicate the success of integrated electronics? Such questions have recently received considerable attention, partly due to the advancements in the fabrication of integrated

semiconductor lasers and photodetectors, rendering their direct interface and integration with electronic circuits more easily achievable.

1.1. Optoelectronic Arrays and Smart Pixels

From a historical perspective, the first concepts of integrated optics may be traced back to the late sixties [1]. The first optoelectronic integrated circuit (OEIC) was reported in late 70s [2], with more complicated OEIC's having been reported ever since. The initial promise for the integration of optical devices was to totally duplicate the success of integrated electronics in optics. However, this promise has not quite met the expectations, both technologically and economically, mainly because of issues like fundamental dimensional differences between electronic and optical components, the wave nature of light, packaging, and availability of on-chip amplification and feedback in electronics versus optics [3]. As a result, a new philosophy has increasingly become popular: complimenting instead of competing. Instead of competing with electronics in tasks electronics excells, the attention is focused on using optics to compliment electronics in the areas where it is less efficient [4]. The interest in smart pixels is in a way the result of this approach. "Smart pixels" are a class of optoelectronic devices based on integrated arrays of optical devices (such as LED's, diode lasers, and photodetectors) and potentially processing electronics on the same chip [5,6]. The idea is that such an integrated architecture greatly facilitates the communication between electronics and optics by allowing easy conversion between electronic and optical signals in various ways and at multiple points in a single chip. Therefore, it is argued, such an approach allows for relatively optimal distribution of tasks between optical and electronic devices in an integrated environment. For practical reasons, it is also possible to have advanced processing electronics and optoelectronic devices on separate chips. In such cases the concept of smart pixels has a more system-level significance, whereby in reality the optical functions are carried out on an "optoelectronic array", consisting mainly of optical sources and detectors, and the "smartness" is realized on a separate purely electronic chip. Within

this dissertation the terms "smart pixels" and "optoelectronic arrays" are mainly used with this distinction in mind, although at times they can be used interchangeably.

One of the major areas where electronics has had difficulty is interconnection. Thus, the main focus of smart pixels research has been optical interconnects. The integration of more transistors in a chip, more processing units per printed circuit board, and more printed circuit board per rack results in what is commonly referred to as an "interconnect bottleneck"[7]. In modern electronic circuits, the bulk of the chip area is used for interconnection, and it is generally accepted that the performance of electronic circuits is now limited not by the transistors, but by the interconnections. In fact, as the number of channels and communication speeds increase, electrical interconnects impose increasingly fundamental performance limitations, and optical interconnects (either free space or fiber based) are attractive candidates to bypass this bottleneck because of their wide bandwidth and low cross-talk characteristics. A review of the fundamental limitations of electronic interconnects and advantages of optical interconnects is given in [8]. Optical interconnections, especially benefiting from integration of optical sources and modulators along with photodetectors and other on-chip electronics [9-11] has become the driving force for a variety of optical processing applications such as optical switching and routing [12-14], optical backplanes [7,15], interfacing [16], massively parallel computing [17] and optoelectronic field-programmable gate arrays (OE-FPGA's)[18]. A review of the related issues and challenges in optical interconnections is given in [19].

Smart pixels are also promising candidates for image processing applications [20]. Parallel processing of image information is usually more efficient, and smart pixels naturally provide the light detection hardware and the parallel electronic processing capabilities for this task [21]. For example, silicon chips consisting of arrays of photodetectors and VLSI electronics offer the potential to perform low-level real-time image processing routines on-chip and produce a manageable output for an outside

processor [22-25]. Other application examples include early vision processing [23], position sensing [26], crystallography [27], image filters [28], adaptive signal processing [29], delay generation [30], and neural network applications [31] like multi-layered systems [32], pattern recognition [33], winner-take-all networks [34], weighted interconnections [35] and sorters [36].

1.2. Optical Design Issues for Smart Pixel Arrays

Most optoelectronic systems require some type of imaging optics to spatially control the light beams properly. The optical system in a smart pixel array (SPA) has the function of directing and imaging the optical beams between the pixels themselves and also with the outside world.

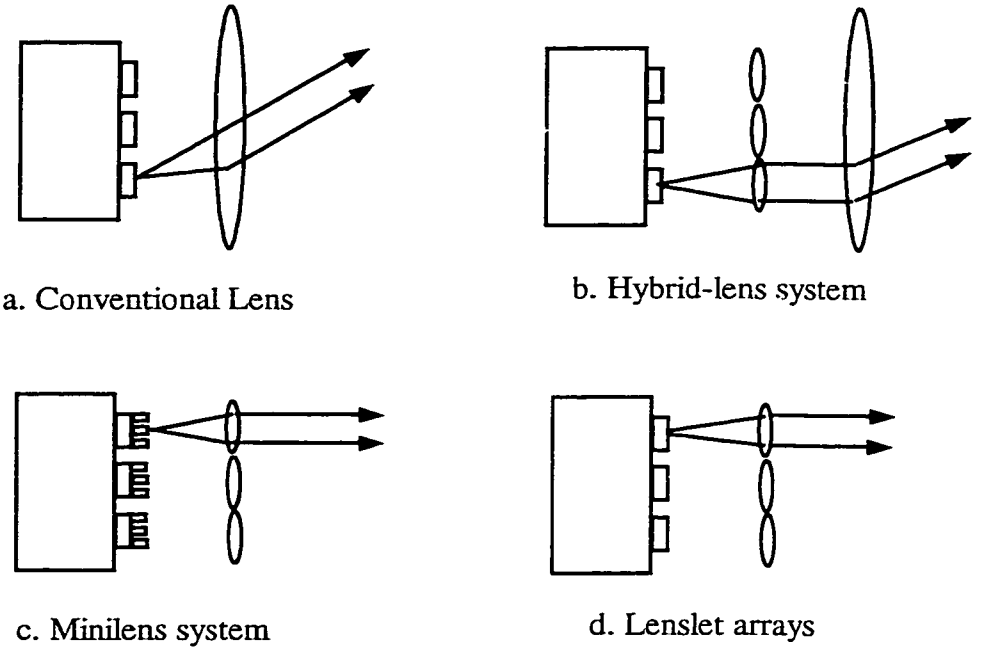


Fig. 1.1. Common optical configurations for smart pixels.

Achieving low loss, low f #, large imaging area, and a small spot size are among the challenges the optical system faces. The details of the optical design depend on the

application, but in general four configurations have been used to perform the imaging task [4,19]. These include: (a) Regular compound lenses (the whole smart pixel matrix uses one lens) (b) Hybrid lenses (where a conventional lens is used in conjunction with an array of microlenses) (c) Mini-lenses (each lens supports a sub-set of pixels), and (D) Microlens (lenslet) arrays (each pixel has a lens). These configurations are illustrated in Fig. 1.1. In addition to lenses, other optical elements such as fibers and beam splitters are also used. Among these elements, phase gratings are particularly interesting since they can provide high efficiency alignment tolerant beam splitting and shifting functions without the need for expensive bulky optics [37]. This feature of phase gratings is important to the topic of this dissertation, and has recently been proposed for use in an edge detection system based on optoelectronic feedback [38]. It will be considered in more detail in Chapter 2.

1.3. Integration Technologies

One of the main challenges in smart pixel technology is the actual integration of optical devices and electronic circuits. Several methods to achieve this goal have been proposed and demonstrated. In general, these technologies can be based on either monolithic or hybrid integration. The advantage of hybrid methods is that they decouple the parameters of different technologies required for fabrication of receivers, emitters, and electronics. Monolithic methods in general are more complicated in terms of material processing because of the inherent differences between these technologies [39]. These technologies may also be divided based on whether the pixels produce their own light or modulate an external light source (modulator/source based) or according to their electronic substrate technology (usually Si or GaAs). Below the main trends in fabrication of smart pixels arrays are briefly reviewed.

Hybrid Integration

One of the major trends in smart pixel fabrication is to integrate optoelectronic devices with the already well-established Si-based electronics [40,41]. Si itself is not suitable for

optical devices (especially light sources) because it is not a direct band gap semiconductor. One of the most popular approaches to integrate optical devices with CMOS electronics is the hybrid CMOS-MQW smart pixel technology. This approach is based on flip-chip bonding GaAs-AlGaAs Multiple Quantum Well (MQW) photodetectors and modulators onto a prefabricated CMOS circuit which contains the receiver and modulator driver circuits as well as any additional necessary electronics [42]. Systems with more than 4000 optical I/O's based on this method have been demonstrated [43,44].

Another hybrid technology is the Polyimide CMOS-based Integration. In this method the layers for optical devices are deposited on a GaAs substrate. The wafer is then bonded to a Si circuit with polyimide. The GaAs substrate is then removed by selective etching so that only epitaxial layers remain. Finally the optical devices are fabricated. Using this technology, MSM detectors [45] and vertical cavity surface emitting lasers (VCSEL's) [46] have been integrated with Si circuits.

Liquid Crystal on Silicon (LCOS) technology is another hybrid method which uses the integration of arrays of liquid-crystal modulators on CMOS circuits [47,48]. This process starts with a CMOS circuit which is solder bonded to a Si substrate. The Si substrate provides mechanical support and electronic connections to the smart pixel. A glass cover is then mounted on top of the CMOS circuit, and liquid crystal is subsequently placed between the Si circuit and the glass by capillary action and through heating of a ferro-electric liquid crystal paste. Variations of this technology have been used for novel filter applications [28].

Hybrid integration is not limited to Si substrates only. Various forms of GaAs based hybrid technologies have also been demonstrated. For instance, the flip-chip bonding of an 8×8 VCSEL array to foundry fabricated GaAs MESFET electronics has been demonstrated [49].

Monolithic Integration

Monolithic integration techniques have always been attractive because of their potential performance and cost-effectiveness. One of the main trends in monolithic techniques is the FET-SEED technology which was the first to monolithically integrate electronics, photodetectors, and modulators into a single chip [4]. This technology uses GaAs-AlGaAs multiple-quantum-well (MQW) reflection modulators, p-i-n photodetectors, and doped channel MIS-like FET's [50]. Monolithic epitaxial growth of optoelectronic devices on VLSI GaAs circuits [51-53] is also the basis of the MIT OPTOCHIP project, and a smart pixel design fabricated with this method is used in this study as will be discussed later. Reviews of the principles and the current status of optoelectronic VLSI circuits based on this technology can be found in [54] and [55].

VCSEL's have also been monolithically integrated on GaAs substrates. The monolithic integration of MSM photodetectors, MESFET's, and VCSEL's (or MQW Modulators) on GaAs substrate pioneered by NTT is an example [56]. Devices based on this technology have shown a bandwidth of more that 200 MHz [57]. It has been shown that both modulator-based and VCSEL-based smart pixels have about the same bandwidth/cm^2 while VCSEL's have an advantage over modulators in that they don't need external light sources [58]. A review of hybrid and monolithic based integrated VCSEL SPA's is given in [59]. Although the vertical cavity lasers and modulators are more suitable for smart pixel applications, monolithic integration of other types of laser and modulator structures have also been demonstrated [60].

1.4. Source-Based versus Modulator Based Smart Pixel Arrays

Although SPA's may incorporate many devices, from a fabrication viewpoint, it is the integration and optimization of optical sources which is most challenging. SPA's can generally be divided into two main categories depending on whether the optical source is

physically located on-chip, or the SPA just modulates light originated from sources off-chip [58]. Although modulation based smart pixel arrays are easier to fabricate [4], the interest is increasingly focused on source based architectures, partly because of the technological advancements which make the fabrication of such arrays possible and practical [60,61]. The primary candidates being considered as smart pixel optical sources are LED's and laser structures, such as VCSEL's. VCSEL's have attracted much attention because of their low threshold current, high efficiency and speed, and good output directionality [62-64]. VCSEL's are particularly suitable for smart pixel applications because they can conveniently be fabricated in the form of two-dimensional arrays with a perpendicular optical axis in the third dimension. Integration of light detectors such as metal-semiconductor-metal (MSM) detectors on the same substrate provides the necessary functionalities for the SPA. However, VCSEL's are complicated structures and their fabrication is costly and involves many steps. LED's, on the other hand, generally lack some of these properties, but they are simpler devices and easier to fabricate. Therefore, their use may be better justified in areas where high performance is not required.

1.5. Scope of Work Presented in This Dissertation

The work presented within the scope of this dissertation starts in Chapter 2 by the introduction of the smart pixels with smart illumination (SPSI) concept, which is an essential and conceptually critical part of this work. This concept will be revisited again in Chapter 3 in a more formal way, where it is discussed within the context of optoelectronic feedback loops. In both Chapters 2 and 3 experimental results from an LED-based optoelectronic chip are presented. In Chapter 4 the single optoelectronic feedback loop of Chapter 3 will be generalized to a matrix formalism for modeling an arbitrary interconnected optoelectronic array, while on the experimental side, a VCSEL-based chip is used for various demonstrations.

Starting from Chapter 5, the focus shifts from the optoelectronic aspects of smart pixels to electronic aspects, dealing mostly with current-mode modules and a general processing architecture for interfacing with optoelectronic arrays. Thus, Chapter 5 discusses several current-mode modules that can be connected together in various configurations to implement optoelectronic functions. The approach, based mostly on current mirrors, allows for digital accuracy while maintaining analog functionalities. Results from a demonstration CMOS-chip fabricated through the MOSIS service and based on the discussed modules are also presented in Chapter 5. These experimental results include both purely electronic data on the performance of the modules, and demonstrations of various optoelectronic concepts discussed in the previous Chapters. In Chapter 6 the individual modules discussed in Chapter 5 are integrated in a more general architecture, consisting of additional processing units such as digital control and programming circuits. In addition, experimental results from a second CMOS chip, designed and fabricated to demonstrate the proposed architecture, are presented. Finally Chapter 7 consists of conclusions, critical review of the discussed concepts, and thoughts on future research ideas and directions.

Chapter 2. Smart Pixels with Smart Illumination

In this chapter the concept of smart pixels with smart illumination (SPSI) is introduced as a new concept in the smart pixel technology. Much of the work presented in this dissertation is related to, originates from, and motivated by the SPSI concept. Thus, a thorough understanding and discussion of this concept and its ramifications is essential and serves as a proper background and motivation for the rest of the chapters.

This chapter starts by introducing SPSI as a new concept in sensor array technology based on structured built-in illumination and optoelectronic feedback. An edge detection system is discussed in detail as an example of how smart illumination can advantageously be used to achieve a variety of functions. Experimental results from a fabricated chip based on this concept are also presented. Finally, a variety of other potential applications that may benefit from SPSI technology are mentioned.

2.1. Motivation

As was mentioned in the introduction, the integration of optical and electronic devices has in recent years been the subject of intense research, with optical interconnects as the main driving force behind much of the applications. But there are also other areas where smart pixel technology has many promising applications. This chapter focuses on the applications of a new class of smart pixel sensors that take advantage of structured illumination and optical feedback: smart pixels with smart illumination [38].

Normally, photodetector sensor arrays require the scenes they sense to be illuminated by some light source. Conventional passive arrays usually rely on the ambient light, and suffer from the effects of spatial, temporal, and spectral variations in the illumination. This is because the signal received by the sensor is the product of the illumination and reflectivity of the scene at each point. Thus, it is impossible for a sensor to differentiate between the actual characteristics of the scene and those of the illumination because

except for the product of the two, no additional information is available to the sensor. Various characteristics of illumination, such as intensity, modulation, and spatial distribution are usually set outside the sensor circuitry and as such, these characteristics are random and unpredictable as far as the sensor is concerned. Thus, even the most comprehensive image processing routines can not improve the signal to noise ratio for a signal detected from a poorly illuminated scene.

Sources with built-in illumination can greatly reduce the unwanted effects of ambient light, however there is still noise from the ambient background. Built-in illumination can either flood the image or supply an array of beams that match the pixel spacing. Non-integrated sources typically require bulky beamsplitters. Structured illumination has the advantage over flood light illumination of more efficient light usage, but introduces tight tolerances on the imaging system if the emitters and detectors are separate. These tight tolerances on uniformity, rotation, translation, and defocus lead to high design and fabrication costs. High optical efficiency requires polarization optics that can be expensive and bulky and impose limits on the sensed image's polarization properties. In addition, illuminating the image with a static uniform light source or a static array of uniform beams is not ideal. A fixed illumination level, set to keep the typical photodetectors within their dynamic range, results in the bright areas and dull areas of the image becoming saturated or lost in the noise on the detectors, respectively. In addition, the total optical power output from the illuminator is typically limited by power consumption and thermal dissipation constraints, reducing the average signal amplitude detected. A spatially structured illumination source that is spatially and electronically integrated with a photodetector array and dynamically controllable would alleviate these problems.

The SPSI concept is based on the integration of an individually addressable emitter array and an individually addressable detector array on a single chip. Structured illumination can be achieved by controlling the output power of each emitter individually, with the

additional advantage that now the illumination can also be a function of the feedback light received by the sensors on the same chip from the scene. In other words, the SPSI array both illuminates and senses the scene in a closed loop scheme. The concept of optoelectronic feedback thus plays a central role in SPSI sensors, because the closed loop characteristics can be modified and adjusted to achieve enhanced and potentially new functionalities. Such a sensor array offers considerable potential advantages over more conventional sensing methods. Instead of uniformly illuminating the whole scene, the light output of each pixel can be set independently and according to the local needs, thus greatly relieving power consumption and heating concerns. Moreover, significant dynamic range compression can be achieved by controlling each pixel's illumination level. Modulating the illumination of each pixel enables an improvement in signal-to-noise ratio (SNR). The SPSI concept has many potential applications in sensor array technology, including edge detection, dynamic spot-light tracking, tracking sensors monitoring focus, translation, and rotation of a scribe line, pixel by pixel background subtraction, intensity compression algorithms, and range finding. Some of these applications are briefly described at the end of this chapter. However, an edge detection application is discussed in more detail in Sec. 2.3 as an example to further elaborate the SPSI concept and the way an optoelectronic feedback loop can be utilized to improve upon passive detector arrays in a variety of aspects.

It is worth mentioning here that although in principle the optical sources and detectors do not need to be integrated on the same chip, such an integration is ultimately crucial. This is because in optical processing applications usually massive amounts of information need to be processed at high speeds, making the performance and reliability of discrete systems unacceptable. Integrated systems can be cheaper, faster, more reliable, less bulky, and less power consuming. Moreover, integration allows for the implementation of neural network schemes where the initial parallel processing of the information is carried out on chip and in real-time and only the pre-processed information is brought off-chip to reduce the

computational load on the outside processor. There are, however, practical obstacles for such integration as mentioned in the introduction. This issue and how it effects the SPSI concept is further discussed in Chapter 7.

2.2. Optical Imaging System

Efficient use of an integrated emitter and detector sensor array requires an optical system that images each emitter of the array onto a spot (or spots) on the scene and then efficiently and accurately images the illuminated spot(s) onto the photodetector(s) associated with the emitter. The design of such an optical system is a challenging task, because a conventional imaging system would image the illuminated spots back onto the emitters, not the detectors. Various schemes employing bulk image shifters can be envisioned but are not practical due to their bulky size and alignment tolerances.

A recently proposed SPSI imaging system is particularly suitable for edge detection applications and differential sensors, although it can be used in other applications as well. The system utilizes a 1×2 binary phase grating (BPG) like those used in free space optical interconnects and for image split and shift modules [37,65]. Other designs utilizing polarization optics are also possible. The proposed SPSI optical system is shown in Fig. 2.1. for a single pixel of the array [38]. Though only an on-axis pixel and f to f Fourier imaging are shown, the design works for an array of pixels and for other imaging configurations. The light from the emitter is split into two beams by the BPG and illuminates two spots (A and B) on the object. The return light beam from each spot is split into two beams: one beam illuminating a detector and the other beam retracing back to the emitter. Detector PD-A (or PD-B) detects the reflected spot from A (or B). As the BPG can be close to 100% efficient in splitting beams, this system has an impressive maximum 50% optical efficiency. This optical design is compact, efficient, low cost, requires minimal alignment, and has no polarizing elements. It eliminates the need to tightly match the focus, translation, and rotation of the detectors and illuminators.

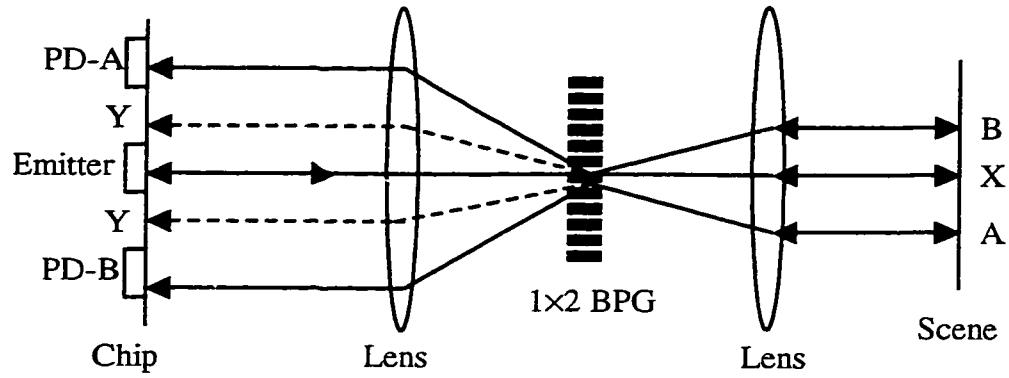


Fig. 2.1. SPSI Optical System.

Since BPG's are not 100% efficient, light due to the undiffracted order of the BPG will hit spot X on the object and spots Y on the chip. These stray spots do not affect the operation of PD-A and PD-B. The second and higher order diffraction of the BPG will eventually need to be considered, but can be made small by proper design of the BPG. Note that half the return light images back on the emitter. With LED arrays, such optical feedback is not a factor. For some laser arrays, such feedback may be intolerable when the object is highly reflecting, causing phase and intensity noise. However, in typical sensing applications, the level of light scattered from the object will likely be very small and will be within the range of acceptable optical feedback level for lasers.

2.3. Edge detector

Edge detection is one of the most important functions required in many image processing and sensing applications. Edge detection is also a function particularly amenable to being implemented with SPSI sensors. Therefore, an edge-detector SPSI sensor is discussed as an important example to elaborate on the advantages of a SPSI sensor over a conventional

one [66,67]. The basic imaging and electronic system for a single pixel of a SPSI edge detector is illustrated in Fig. 2.2.

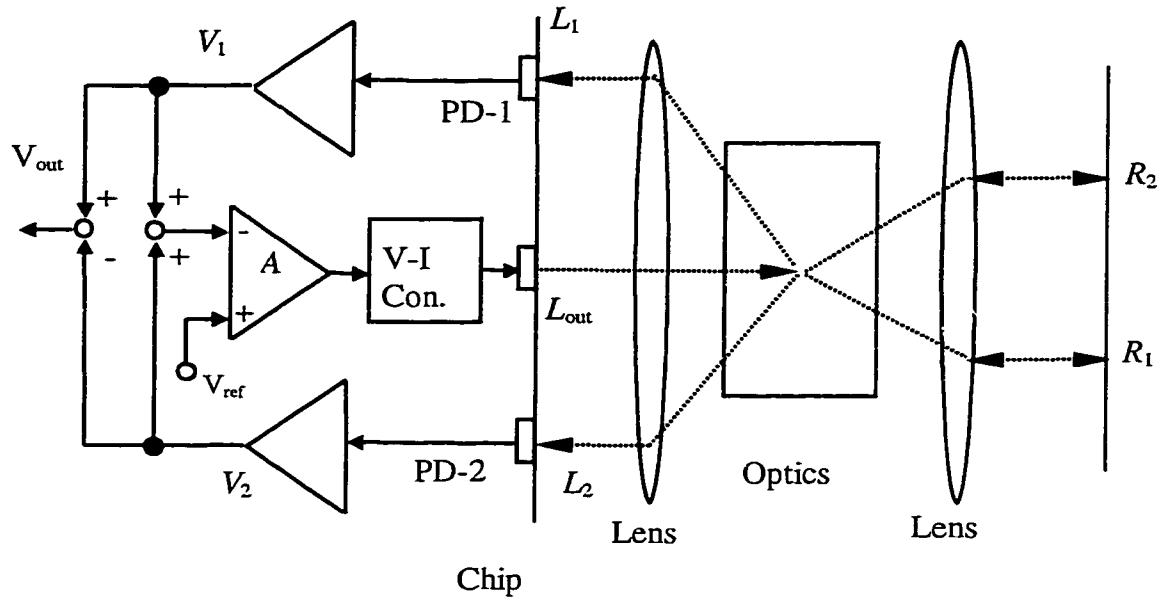


Fig. 2.2. Schematic of the electronics and optics for a single pixel edge detector.

It is worth noting that the optical function in Figs. 2.1 and 2.2 is identical. The only difference in the two figures is that in order to keep the discussion general, in Fig. 2.2 only the *function* of the optical system is shown and emphasized, without regards to the particular way it may be implemented.

The function of the system can be described as follows. The light output from the emitter (L_{out}) is split by an optical element into two equal intensity beams. Each beam illuminates one of two adjacent spots with reflectivities R_1 and R_2 on the scene, and then gets reflected and focused back (L_1 and L_2) into a detector (PD-1 or PD-2). The electronic circuit generates the voltages V_1 and V_2 proportional to the incident light power on each detector. These two voltages are first added, and then subtracted from a reference voltage

V_{ref}. The resulting voltage is amplified and converted to a current which drives the emitter. If the gain of the amplifier A is very large, and assuming the system is in its active region of bias, the output of the amplifier (and thus the emitter light output) must change such that it maintains the condition of $V_{ref}=V_1+V_2$. This situation is similar to an electronic opamp circuit, except that in this system the feedback loop is optical. If V_1 and V_2 are proportional to L_1 and L_2 the following expression is obtained

$$V_{ref}= V_1+V_2 = a\,L_1 + a\,L_2 = a(R_1+R_2)L_{out}\ , \qquad (2.1)$$

where a is the overall gain from the light power incident on the detector L_1 (L_2) to the voltage V_1 (V_2). Therefore, the operating point of the emitter can be set by V_{ref}. The output of the pixel is defined as $V_{out}=V_1-V_2$. Therefore:

$$V_{out} \equiv V_1-V_2 = a\,L_1 - a\,L_2 = a(R_1-R_2)L_{out}=V_{ref}(R_1-R_2)/(R_1+R_2). \qquad (2.2)$$

This expression shows that the pixel output is the normalized difference between the two reflectivities. Therefore, an array of such pixels measures the normalized slope of the reflectivity of the scene at each point, and is capable of performing various edge detection functions.

It can be verified from Eq. 2.1 that with a constant V_{ref}, higher values of reflectivities result in lower values for L_{out} and vice-versa. This means that the dark regions of the scene are not buried in noise because the emitter then provides more power, and the bright areas of the scene do not saturate the detectors because the emitter provides less power. Another advantage of using feedback is the system's insensitivity to varying emitter characteristics. As long as the output power of the emitter can be changed enough to maintain the condition of $V_{ref}=V_1+V_2$, the actual current-voltage or current-power characteristics of the emitter do not affect the performance of the system as can be seen from the derivation of Eq. 2.2. This is again a unique result of utilizing an optoelectronic feedback loop. This effect may prove very useful in optoelectronic integrated circuits, because it relieves the tight tolerances required on uniformity in characteristics of light sources within the circuits. A more detailed discussion on optoelectronic feedback is given in Chapter 3.

To further illustrate the operation of the edge detector, consider the upper plot in Fig. 2.3 of the reflectivity of a scene that has a dull region (0.1% reflectivity), a bright region (50% reflectivity), and a region in which the reflectivity ramps from dull to bright.

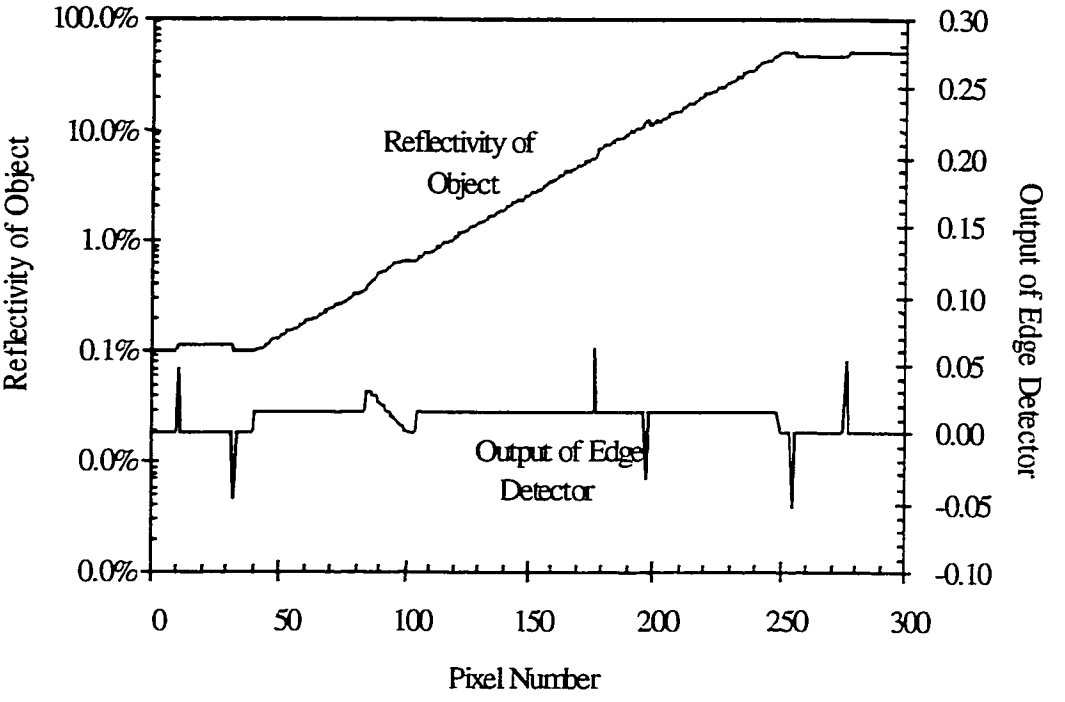


Fig. 2.3. Simulated output of SPSI edge detector for an array of pixels.

In each region, there is a point of 10% increase or decrease in reflectivity. The region of ramped reflectivity also has a rounded off (sinusoidal) variation in reflectivity, with a 20% peak increase. Open loop detection of all these variations in the reflectivity of this scene with uniform illumination would require the detectors and electronic circuits to have a dynamic range of over 5000:1. With the SPSI concept, a dynamic range of 10 is sufficient for the detectors and circuits. In the lower plot of Fig. 2.3 the simulated output of the

SPSI detector array is plotted based on Eq. 2.2. The spikes correspond to the edges of sharp increase or decrease in reflectivity, while the region with the ramping reflectivity corresponds to a small constant output.

2.4. Experimental Results

To demonstrate the SPSI concepts experimentally, an optoelectronic chip incorporating LED emitters, metal-semiconductor-metal (MSM), and optically sensitive FET (OPFET) detectors was designed. The fabrication of this chip was made possible by a unique opportunity offered by the MIT OPTOCHIP program.

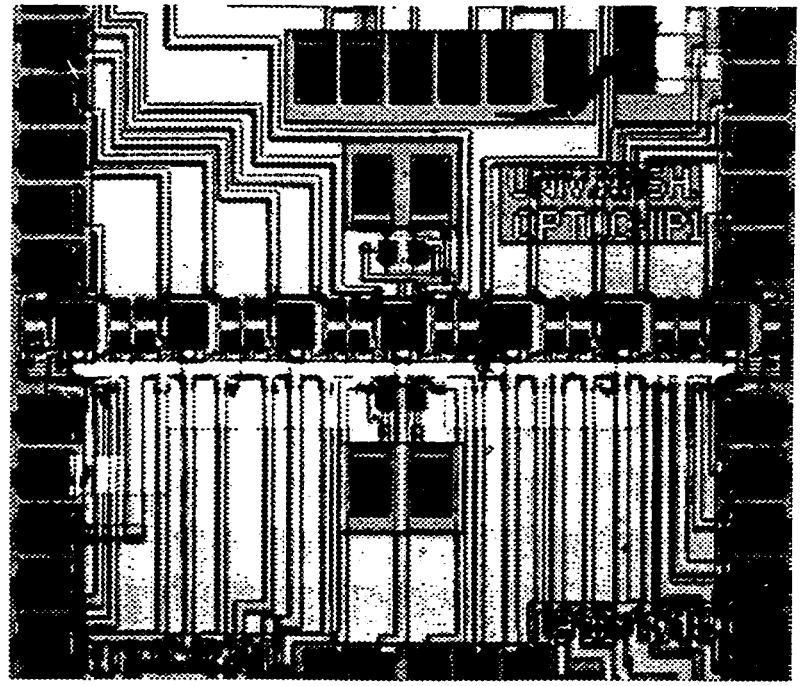


Fig. 2.4. View of the fabricated optoelectronic chip through the OPTOCHIP program.

During this program, eight groups from around the country were selected to design and have fabricated at no cost optoelectronic circuits based on monolithic epitaxial growth of

optoelectronic devices on VLSI GaAs circuits [51,52,54,55,68]. A view of the fabricated chip is shown in Fig. 2.4. The layout includes a 1×7 array of one-dimensional pixels across the chip. The pixels are considered one-dimensional because each pixel consists of an LED in the middle as the optical source surrounded on either side (along the horizontal axis in Fig. 2.4) by optical detectors. The middle LED has additional detectors above and below it, allowing it to be used as a two dimensional pixel. The chip also includes additional test structures for the electronics, detectors, and LED's.

Figure 2.5 shows the layout of one of the pixels in more detail. The structure of the LED in the middle and the surrounding detectors is clear from the figure.

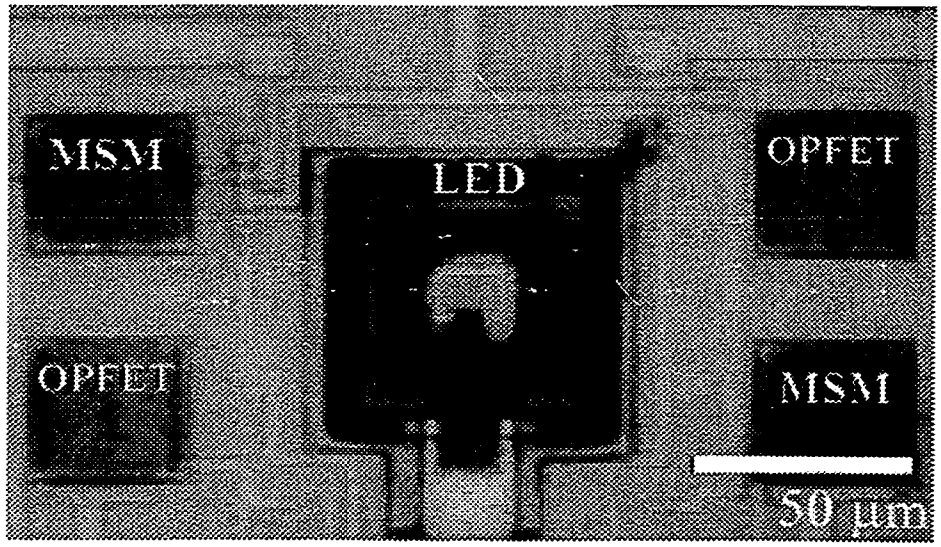


Fig. 2.5. Top view of a single pixel on OPTOCHIP, with the LED in the middle, surrounded by OPFET and MSM detector pairs.

The detectors consist of a pair of MSM and OPFET structures. Additional electronic circuits were brought off-chip to allow maximum versatility in experimental configurations and initial demonstrations.

This design allows for the flexibility to use either the MSM or the OPFET detectors by simply rotating the chip and the optics with respect to each other. To test the basic function of a pixel, a polarizing beam splitter (PBS) was used and two mirrors with variable attenuator were inserted in the path of the beams, as shown in the optical system of Fig. 2.2. This configuration, shown in Fig. 2.6, allows for the ability to vary R_1 and R_2 independently and between 0 and 1 for test purposes. The rest of Fig. 2.6 is identical to Fig. 2.2 and is repeated for convenience.

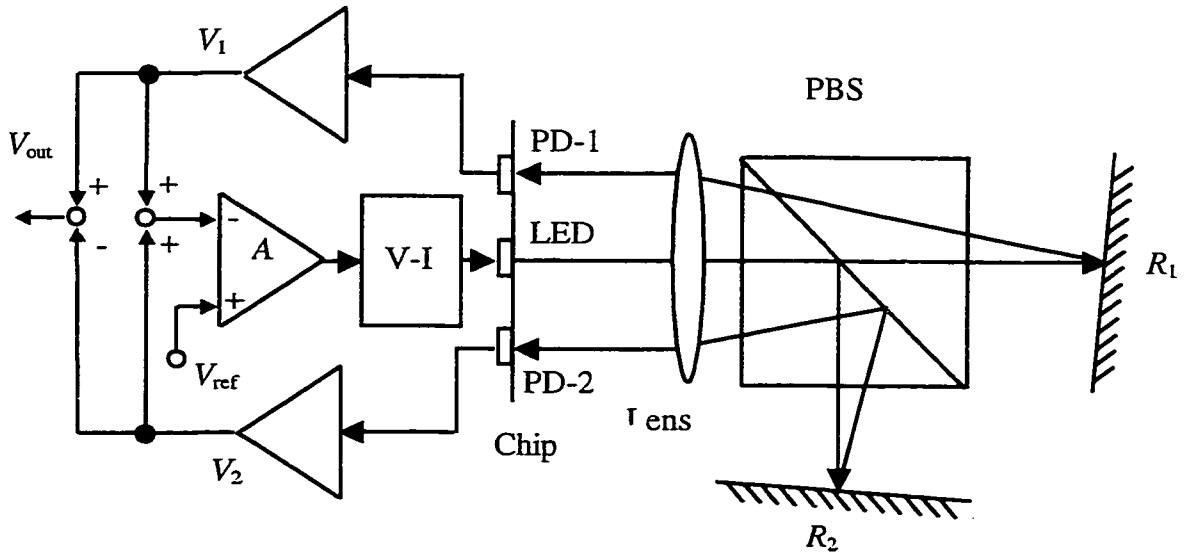


Fig. 2.6. Experimental demonstration of the edge detector with OPTOCHIP.

To explain the experimental results obtained from the chip, it is necessary to use a more detailed model. For the purpose of the edge detection system, the most important additional effect to take into account is a direct coupling between the LED output and the detectors on the chip. Due to this crosstalk, V_1 (or V_2) is not only a function of the incident light L_1 (or L_2) on the detector PD-1 (or PD-2), but also a function of L_{out}. If $V_{1(2)}=aL_{1(2)}+bL_{out}+c$ is assumed as the general form for the detector output, the expression for V_{out} is modified to

$$V_{out} \equiv V_1 - V_2 = (V_{ref}-2c)(R_1-R_2)/(R_1+R_2+2b/a). \qquad (2.3)$$

Therefore, the cross-talk modeled by b/a acts as an additional equivalent electronic reflectivity per detector. In principle, it is better to reduce this effect at the design and fabrication stage of the chip. However, it is also possible to compensate for it by the introduction of an additional electronic coupling, equal in size but opposite in sign to b.

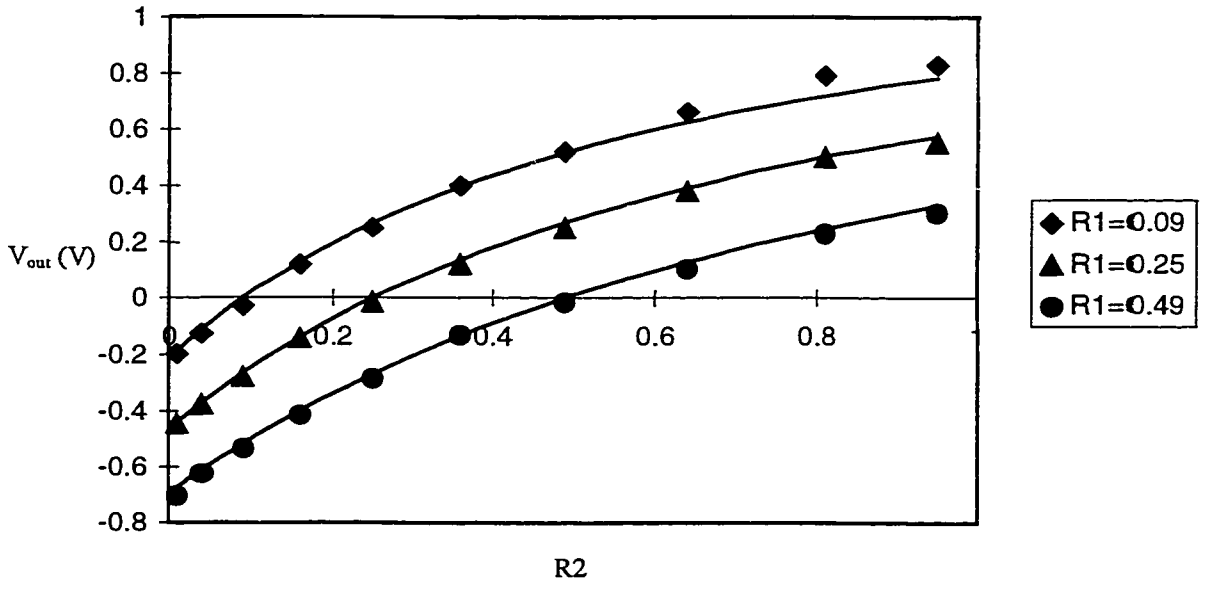


Fig. 2.7. Theoretical (solid curves) and experimental (markers) output voltages of a single pixel for three values of R_1 versus R_2.

For the experimental results presented here, the measured values for a and b are 2.0 and 0.5 V/μW respectively. Figure 2.7 shows the actual experimental measurements using the MSM detector pair, as well as the curves predicted by the expression for V_{out} with V_{ref}-2c =1.4 V. The output voltage is plotted versus R_2 for three values of R_1. The solid curves represent Eq. 2.3 with the above parameters, and the markers are the measured voltage values. The fact that the curves have a larger slope for smaller values of R_2 and that the output is zero whenever R_1=R_2 is the direct result of the normalized differencing.

2.5. Other applications of SPSI

The SPSI concept opens up a whole new area of functionalities previously unavailable to smart pixels and neural network architectures, making it a potentially revolutionary advancement in sensor and interconnect technology. For instance if the approach taken in the edge detector is generalized by using n detectors in each pixel, and if the optical system is designed such that it can illuminate n points on the scene and focus the reflected beams back on the n detectors, a bilinear expression for the output in the form

$$V_{out} = V_r (a_1R_1 \pm a_2R_2 \pm ... \pm a_nR_n) / (a_1R_1 \pm a_2R_2 \pm ... \pm a_nR_n) \qquad (2.4)$$

may be achieved, where a_i are the gains of the receivers and the plus or minus signs in the numerator and denominator may be selected by choosing to add or subtract the output of each receiver at the input of the summing node respectively. There are several useful special cases for such an n detector system such as higher order derivatives of reflectivity or more accurate expressions for the same order derivative.

The following list of applications is not necessarily comprehensive, but is meant to give a general picture of some of those applications [69].

1) The SPSI edge detector can be generalized, so that the contrast and detectivity of imaging can be tuned to the desired spatial frequencies of the image. For example, high

spatial frequency features, like sharp edges, can be distinguished in the presence of long range, low spatial frequency variations in illumination or reflectivity. In practice, this amounts to being able to distinguish fine features simultaneously within an image which is partly in strong illumination and partly in shadow.

2) A SPSI tracking sensor made of a 1×3 pixel array can monitor a scribe line and feed back focus, translation, and rotation signals to a servo system controller. An N×3 array is capable of tracking N scribe lines simultaneously. A potential application for such a system is faster CD-ROM heads or guiding automated manufacturing equipment.

3) A dynamic spotlight tracking system can preferentially illuminate objects of interest in the field of view and track them. Multiple targets can be tracked and highlighted with the proposed algorithm [70].

4) Temporal modulation of illumination of the pixels enables background subtraction on a pixel by pixel basis to eliminate the effects of high ambient noise levels and pixel to pixel crosstalk.

5) Neural networks are another potentially important application area. For example in winner-take-all circuits the increased output of the "winner" pixel acts to highlight an object for detection by another imaging or vision system. Higher orders of lateral inhibition [71] could be incorporated in neural network designs, where the inhibition circuitry could now include optical cross-links between pixels and the non-linear attributes of the SPSI feedback could be used in the calculation of the weights.

6) Tracking of non-linear (light-emitting) objects is possible using SPSI arrays. Suppose an object is fluorescent rather than reflective. The non-linear response of the object to spatially and temporally modulated illumination could be detected in a coordinated fashion to reveal movement and rotation of the object without the need for precise patterning on the object. Immediate applications of this tracking concept could be found in manufacturing and robotic control systems.

7) Compression algorithms may utilize the fact that the emitter output with optical feedback controlled illumination is the reciprocal of the object's reflectivity. The edge detection algorithm relies on this functionality. This feature of SPSI could also be used to cancel out non-uniformities of elements and to maximize the dynamic range of the sensing detectors. Neural network architectures could exploit this feature up to before the operation of division. This application is discussed further in Chapter 3 where optoelectronic feedback is studied in more detail

8) In Page oriented memory and processing systems the operations of tracking, array error code correction, and scanned readout could benefit from the attributes of SPSI [69]. The differential spots would enable extremely sensitive detection where one spot illuminates a reference track and the other a data track. SPSI array functions may be used to aid in the error correction for page-oriented memory. Real-time sum error checking and correction can be carried out by the same integrated chip that is reading the memory. Applications in both digital and analog data storage can be envisioned. The pixel by pixel optoelectronic feedback of SPSI can be used to both reduce errors due to non-uniform illumination of both digital and analog data systems as well as increase the detection dynamic range in analog storage applications. Background subtraction can be used to reduce noise on a pixel by pixel basis as well as decrease optical crosstalk between pixels, thus decreasing bit error rates directly. SPSI designs with dual detectors open up the possibility for self-referencing for each pixel. In addition to error correction, encryption and decryption are also possible via precise multiple pixel processing due to the enhanced capabilities made possible with SPSI. Practical considerations in memory systems also make SPSI attractive. The SPSI concept allows for smart power management that can be useful in conserving power in remote systems as well as increasing the lifetime of memory materials by limiting light exposure levels and heat transfer. The relaxed alignment tolerances of SPSI make it a robust design for remote applications. SPSI designs that monitor focus, rotation, and translation can be used to keep moving heads precisely aligned with all these functions integrated directly in the optical head.

9) In a pixel by pixel ranging system each pixel can act as an independent intensity modulated laser radar. The practicability of this application depends on the power level and modulation rates attainable with emitter arrays. Doppler radar imaging is also a potential application area.

An integrated array of optical detectors and emitters in the same focal plane provides for an efficient and low-cost way of coupling a set of fibers with each other and with on-chip electronics. As such, most of the above mentioned applications can be extended through coupling with various configurations of fibers. The ability to perform on-chip electronic operations in addition to utilizing optical feedback opens up new possibilities and potentials for a variety of applications. The following are examples of possible information processing and sensor applications:

1) In multi-fiber transceivers, the signals from a set of fibers are sensed by the photo-detectors in the array, processed by the on-chip electronics, and sent back either through the same set or a different set of fibers.

2) Multi-fiber sensors can benefit by utilizing a set of fibers instead of a single fiber, providing potential improvements on the already well-established fiber sensor technologies. In such a system, some of the fibers may be used to carry the optical energy/information from the chip to the site of interest, while the others are used to carry the optical energy/information back to the chip from the site.

The above list is not necessarily complete, and further studies are needed to determine the various design requirements for each of these applications. Several issues about new SPSI applications are discussed in Chapter 7.

2.6. Summary

In this chapter the new SPSI concept in sensor design was introduced and it was shown that structured illumination combined with optoelectronic feedback opens up entirely new possibilities for smart pixels. Experimental results related to an edge detector from a fabricated chip that includes integrated LED light sources and MSM and OPFET detectors were presented. The experimental results closely match the results predicted by the model, and demonstrate the new possibilities resulting from the SPSI concept.

Chapter 3. Optoelectronic Feedback

In Chapter 2 the SPSI concept was introduced and some of its potential applications in sensor technology were discussed. These applications often benefit from the fact that the sensor and the sensed object form a closed feedback loop. The SPSI array illuminates the scene, the illumination is modulated, modified, or scattered by various features and aspects of the scene, the returned light is detected by the SPSI detectors, and the information is used to adjust the illumination. Naturally therefore, a complete treatment of SPSI sensors and their applications requires an in-depth understanding of optoelectronic feedback and its characteristics.

This chapter deals with characterization and modeling of optoelectronic feedback. Applications of optoelectronic feedback in addressing various problems in smart pixel arrays are considered, with special attention paid to issues associated with light sources such as device nonlinearity and non-uniformity. These issues were generally neglected in Chapter 2 when it was implicitly assumed that the output of the light emitters is linearly proportional to their driving current. In this chapter the concept of a single optoelectronic feedback loop is discussed and developed. This is a useful and fundamental model that allows for a more formal treatment of SPSI concepts discussed in Chapter 2. More experimental results from the OPTOCHIP are also presented to demonstrate the validity of the models.

3.1. The Concept of Feedback and its Use in Optoelectronics

Feedback is used extensively in electronics for a variety of purposes. In optics, however, the implementation of feedback is usually not straightforward. The reason is that a negative optical signal could only be realized with phase control of the optical signal, an intrinsically difficult task. SPA's greatly alleviate this problem by allowing easy conversion between electronic and optical signals in various ways and at multiple points in the system, thus shifting the required operations for feedback, such as addition and subtraction of

signals, from the optical domain to the electronic domain. The term "optoelectronic feedback" as used in this dissertation refers to this capability of SPA's to perform on-chip mixing of optical and electronic signals. By so doing, not only some of the important technological problems of smart pixels can be addressed, but also interesting new concepts and applications otherwise not readily available in purely digital systems can result.

As was mentioned in the introduction, SPA's can be either source based or modulator based. Source based SPA's are becoming increasing popular especially with the advent of VCSEL's [63], although LED-based SPA's have also been constructed. These optical sources present several common challenges to the designer. On the one hand, they are intrinsically nonlinear quantum devices, i.e., their optical output is a nonlinear function of the electrical drive current. The threshold current of lasers is a common example. LED's also show a threshold current below which there is negligible light output. Even above the threshold current, the output may not vary linearly with the drive current depending on the interplay between radiative and non-radiative mechanisms. Another common problem encountered in source based smart pixels is the variation of device characteristics within a wafer and from wafer to wafer. In fact, because of the numerous steps and parameters involved in the fabrication of these devices, it is very difficult to obtain acceptable uniformity for many demanding applications [72]. In addition to these random fabrication variations, temperature dependencies and aging are other factors which further randomize the characteristics of these light sources. As will be shown later, feedback can advantageously be used to address many of these problems.

3.2. Single Pixel Optoelectronic Feedback Loop

Feedback schemes can be complicated, and thus it is useful to start the discussion with a simple case of a single feedback loop as a building block for more complicated schemes. At the center of an optoelectronic feedback loop is a light source, a device that converts electrical current to optical radiation. These light sources are commonly LED's or

semiconductor lasers, and usually share certain characteristics like threshold current, saturation, and nonlinearities in their active region. For example the experimental results presented in Chapter 2 are based on monolithically integrated, mesa-confined GaAs/InGaP double-heterostructure LED sources [54]. The I-L characteristic of a sample LED is shown in Fig. 3.1. The nonlinear behavior of this device can be modeled by a threshold current I_{th} below which the output light is assumed to be negligible, a gain factor K, a nonlinearity factor n, and a saturation current I_{sat}

$$L = \begin{cases} 0 & I < I_{th} \\ K(I - I_{th})^n & I_{th} < I < I_{sat} \\ L_{sat} & I > I_{sat} \end{cases} \tag{3.1}$$

where L_{sat} is the saturated output given by $K(I_{sat} - I_{th})^n$.

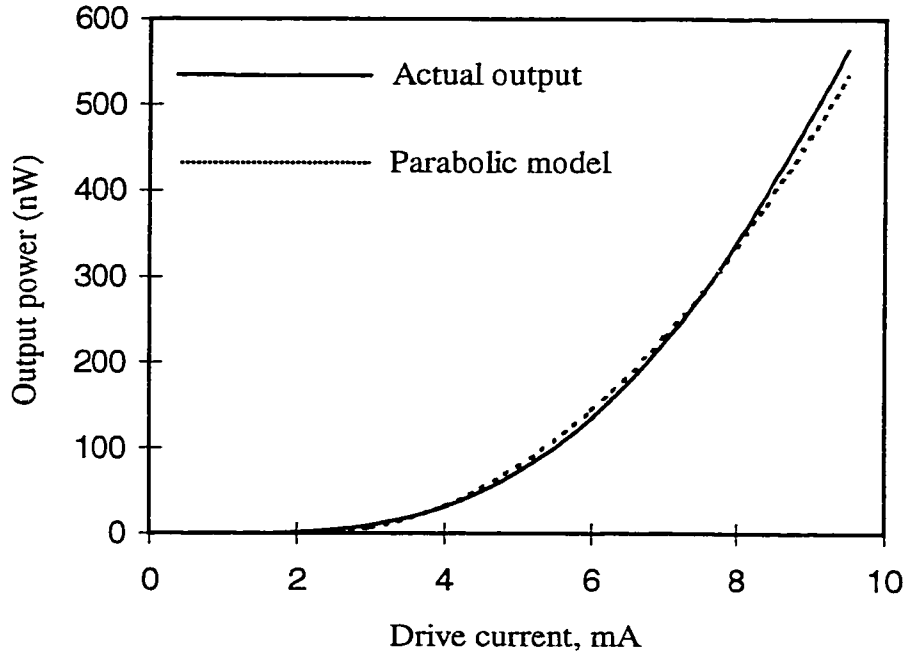


Fig. 3.1. Experimental LED output (solid line) and parabolic fit (dashed line) versus drive current.

The saturation current I_{sat}, although not shown in Fig. 3.1, may be used to model the actual saturation of the device, or other effects such as power supply clipping or current limiting circuits for preventing overloading of emitters. The non-saturated part of the output modeled by Eq. 3.1 is also shown in Fig. 3.1 for K=10 nW/mA^2, I_{th}=2.2 mA, and n=2.

Using an expression like Eq. 3.1 is beneficial because a variety of light sources can be modeled. Laser diodes, for example, generally tend to exhibit a "sharp" turn-on characteristic, with relatively linear behavior above threshold. This corresponds to n=1 in Eq. 3.1. LED's on the other hand, usually exhibit a "soft" turn-on, as can be seen from Fig. 3.1, corresponding to n=2.

A block diagram of an optoelectronic feedback loop with a nonlinear optical source is shown in Fig. 3.2.

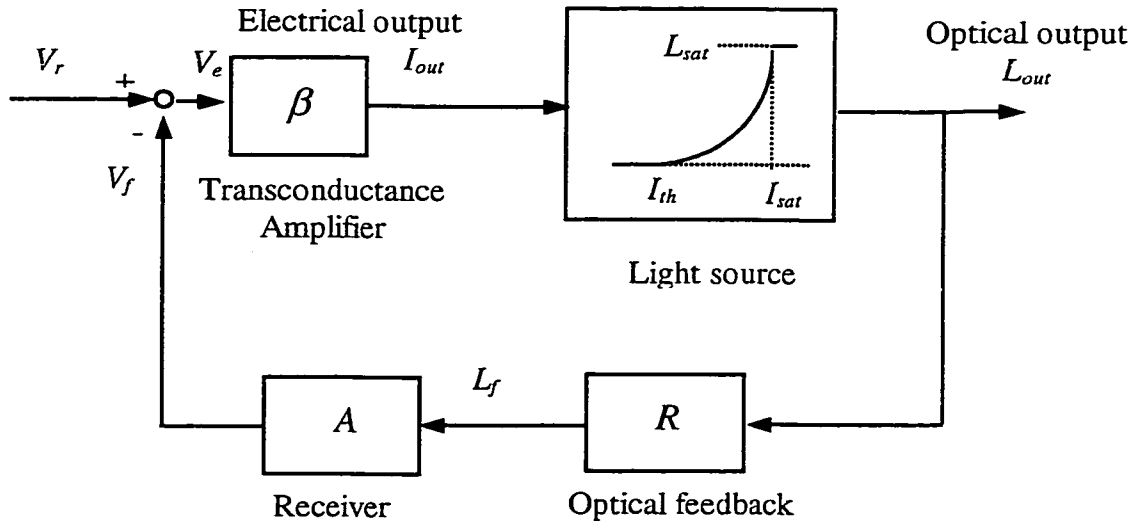


Fig. 3.2. Single optoelectronic feedback loop.

A reference voltage V_r is applied to the loop which depending on the application, may include signal information to be transmitted by the light emitter, or provide a DC bias for the loop. The error voltage V_e is applied to a transconductance amplifier with gain β and the current output of the amplifier I_{out} drives the light source. The optical output L_{out} is fed back to the receiver circuit denoted by a gain factor A. The amount of optical feedback is denoted by a factor R ($0 < R < 1$). The receiver circuit usually includes an optical detector and a transimpedence amplifier. The output of the receiver V_f is subtracted from the reference voltage to produce the error voltage. In reality the gain factors A, β, and K are each frequency dependent. However, for the purpose of this study the focus is on the DC analysis of the loop with the assumption that the signals of interest are slowly varying compared to the dominant poles and zeros of the loop.

Assuming the loop is biased in its active region ($I_{th} < I_{out} < I_{sat}$) the following implicit expressions for the outputs are found:

$$L_{out} = K(\beta V_r - I_{th} - \beta A R L_{out})^n \,, \tag{3.2}$$

and

$$I_{out} = \beta V_r - K\beta A R (I_{out} - I_{th})^n \,. \tag{3.3}$$

These expressions in their most general form have to be solved numerically. Some special cases like n=1 corresponding to most laser diodes, and n=2 corresponding to the LED's used in this study, can be solved analytically, with the latter case resulting in rather lengthy expressions. However, a graphical solution of these equations provides a better insight into the behavior of the system and the role of different parameters in setting the operating point. Equation 3.3 can be written in the form

$$\frac{V_r}{AR} - \frac{I_{out}}{\beta A R} = K(I_{out} - I_{th})^n \,. \tag{3.4}$$

The two sides of Eq. 3.4 can be plotted as a function of I_{out}, and the intersection of the two plots gives the operating point (I_{out}, L_{out}) since the quantity on the right hand side of

Eq. 3.4 is L_{out}. The left-hand side of Eq. 3.4 describes a load-line that the feedback circuit creates for the emitter characteristics. These plots are shown in Fig. 3.3. It is important to notice that although this graphical solution is used here for the kind of nonlinearity described by Eq. 3.1, it can be applied to any form of nonlinearity by simply substituting the right hand side of Eq. 3.4 with the specific nonlinear characteristic of the light source. This issue will be addressed again in the next chapter where a more accurate analysis of the optoelectronic feedback loop within a more general context is presented.

Using the graphical solution and depending on the design objectives, various parameters of the loop may be selected. For example, it is generally desirable to keep I_{out} somewhere between I_{sat} and I_{th} . It is also easy to find the output waveform for a given input waveform, since changing V_r simply shifts the load line up and down with no change in its slope, while changing R rotates the load-line around the $(\beta V_r, 0)$ point.

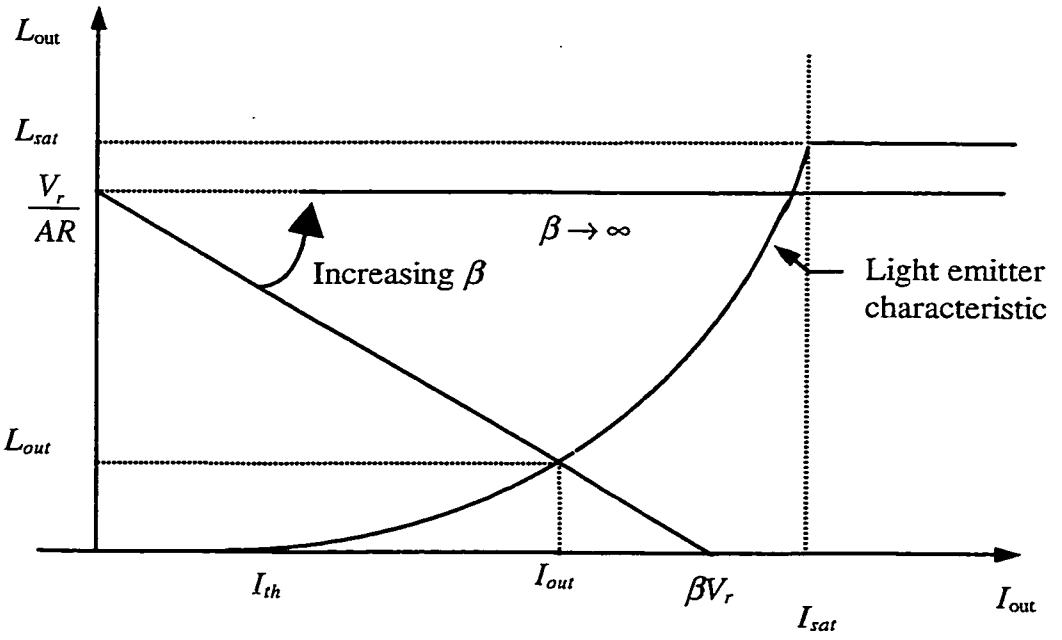


Fig. 3.3. Operational point of a single pixel feedback loop.

Another interesting fact to notice is the effect of increasing the electronic feedback. The loop gain can be increased by increasing the amplifier gain β, which rotates the load line around the (0, V_r/AR) point towards a more horizontal slope, leading to a decreased sensitivity of the optical output L_{out} to device characteristics.

If the DC gain is very large ($\beta \rightarrow \infty$), Eqs. 3.2 and 3.3 simplify to

$$L_{out} = \frac{V_r}{AR}, \tag{3.5}$$

and

$$I_{out} = I_{th} + \left(\frac{V_r}{KAR}\right)^{\frac{1}{n}}. \tag{3.6}$$

From Eq. 3.5, it is observed that the optical output is directly proportional to the reference voltage V_r, and inversely proportional to the optical feedback R. It is further seen that the optical output becomes independent of the threshold current I_{th}, the optical gain K, or the nonlinearity n. As mentioned before, the fabrication of integrated light sources such as VCSEL's or LED's involves many steps and numerous process parameters which makes the achieving of parameter uniformity within a single chip or from wafer to wafer a challenging task. For instance, the best uniformity reported so far with LED's used in the OPTOCHIP technology is about 30%, although in several cases the uniformity has been significantly lower [55]. The threshold current I_{th} is also slightly different for continuous and pulsed applications. Such nonlinear effects further complicate the performance of an open-loop pixel. The absence of these factors in the closed loop optical output provides a strong motivation for implementation of optoelectronic feedback in SPA's. In effect, parameter uniformity requirements shift from the emitters to the detectors since the optical output is a function of A (receiver circuit) and R (optical feedback) only.

It is also possible to obtain upper and lower limits for the parameters in order to ensure that the loop is biased in the active region. From Fig. 3.3 it can be seen that a sufficient condition is to have

$$I_{th} < \beta V_r < I_{sat} \ , \tag{3.7}$$

which sets limits on $V_r\beta$ product. If a lower range for R is known beforehand, the upper limit set by Eq. 3.7 may be considerably relaxed as can be seen from Fig. 3.3.

3.3. SPSI: An Optoelectronic Feedback Approach

In this section the SPSI concept is revisited through the model of a single pixel optoelectronic feedback loop.

As an example, if in the simple feedback loop of Fig. 3.2 instead of the reference voltage V_r the amount of feedback R is taken as the input to the loop, a single SPSI sensor results. In such a scheme, the reflectivity of the scene at a given point provides the necessary feedback for closed loop operation. The task of focusing the optical output of the pixel on an external scene and focusing back the scattered light on the pixel's detector(s) is carried out by the optics in front of the pixel. The details of the optical system are not discussed here as they were considered in Chapter 2.

To illustrate an example of the SPSI behavior, consider a one-dimensional scene with the sample reflectivity profile shown in Fig. 3.4, profile (a). This profile consists of two constant reflectivity regions of 0.1 and 0.5 at the two sides of the scene and a ramp connecting the two. In the areas of constant reflectivity there is an additional 10% change in the form of a step function modeling additional details in the scene.

Under ideal uniform illumination conditions, a dynamic range of 55:1 is needed to detect all the details of this scene properly. However, poor illumination may significantly increase the required dynamic range. As an example of poor illumination conditions,

assume that the illumination ramps from 0.05 to 0.55 (arbitrary units) from left to right. Since a regular sensor detects the product of the reflectivity and illumination (shown in Fig. 3.4, profile (b)) the dynamic range requirement now increases to roughly 500:1.

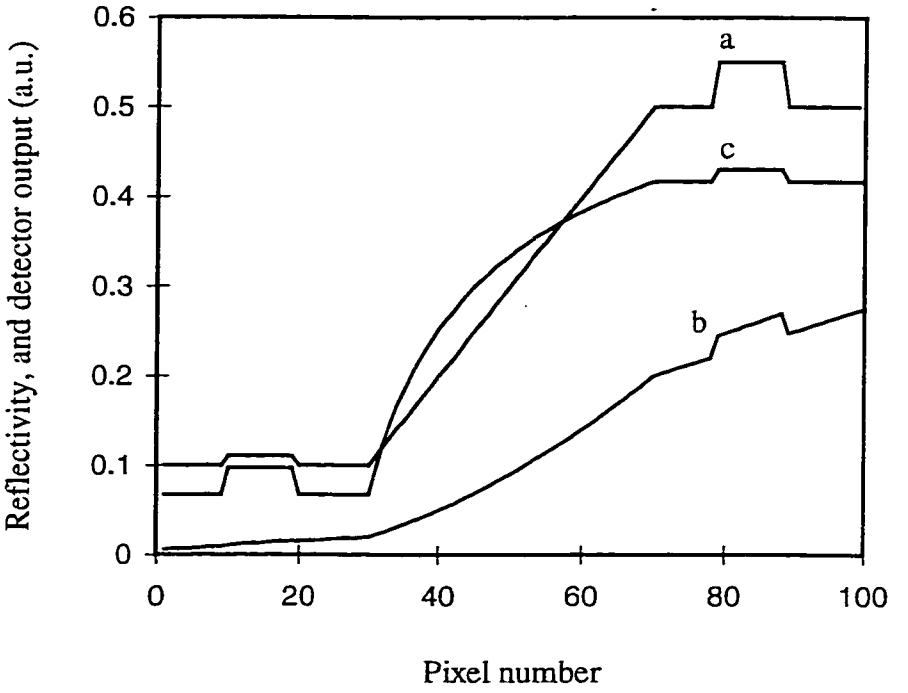


Fig. 3.4.(a) Reflectivity profile for a sample one dimensional scene. (b) Detected signal for the scene under given illumination condition (a.u.). (c) SPSI sensor output (a.u.).

Moreover, without *a priori* knowledge about the spatial distribution of illumination, it is almost impossible to filter out the effects of poor illumination. Now assume a SPSI sensor based on Eq. 3.6 with n=2 (LED source) is used. In such a sensor, the current output of each pixel is proportional to the inverse of the square root of the reflectivity of the scene at the corresponding point. To account for the reversal in the polarity of the image, the

output current of each pixel can be subtracted from a constant reference current I_{ref}. The output current of the mth pixel is therefore:

$$I_m = I_{ref} - I_{th} - \left(\frac{V_r}{KAR_m} \right)^{\frac{1}{2}} \tag{3.8}$$

The output defined by this equation for the given scene is shown in profile (c) of Fig. 3.4 (arbitrary units). Using this SPSI sensor ideally removes the dynamic range requirements on detectors since as a result of Eq. 3.5 all detectors see the same amount of light independent of the reflectivity of the scene. Also in effect a range compression algorithm is implemented due to the fact that the effective gain (defined by dI_m/dR) reduces in the high reflectivity regions of the scene. Moreover, the sensor automatically provides more illumination in the low reflectivity regions, thus preventing details of such regions to be buried in noise by automatically increasing the signal to noise ratio. It should be noted that these effects all take place as a result of feedback and without any *a priori* knowledge about the illumination or the scene itself.

3.4. Experimental Results

To demonstrate the validity of the results derived from the single pixel model, the OPTOCHIP was again used. The experimental set-up for the experiments is shown in Fig. 3.5. The driver circuits were designed to limit the current through the LED to 10 mA. Higher values of current resulted in a gradual degradation and loss of efficiency for the LED's, with the rate of degradation increasing for higher values of current. The MSM detectors were used in the experiments because they showed very linear gain characteristics, compared to the OPFET detectors. Moreover, MSM's were found to have better immunity to on-chip cross talk and noise compared to OPFET's. The overall gain of the receiver was 0.035 Volts/nW. The gain β was about 10^5 and was provided by an open-loop opamp, allowing for the high gain approximation to be valid.

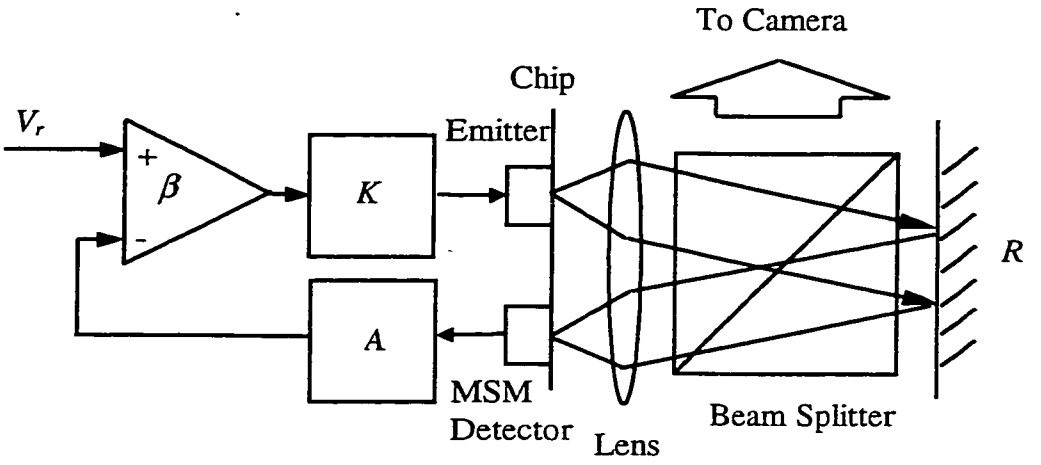


Fig. 3.5. Experimental setup for a single pixel feedback loop using OPTOCHIP.

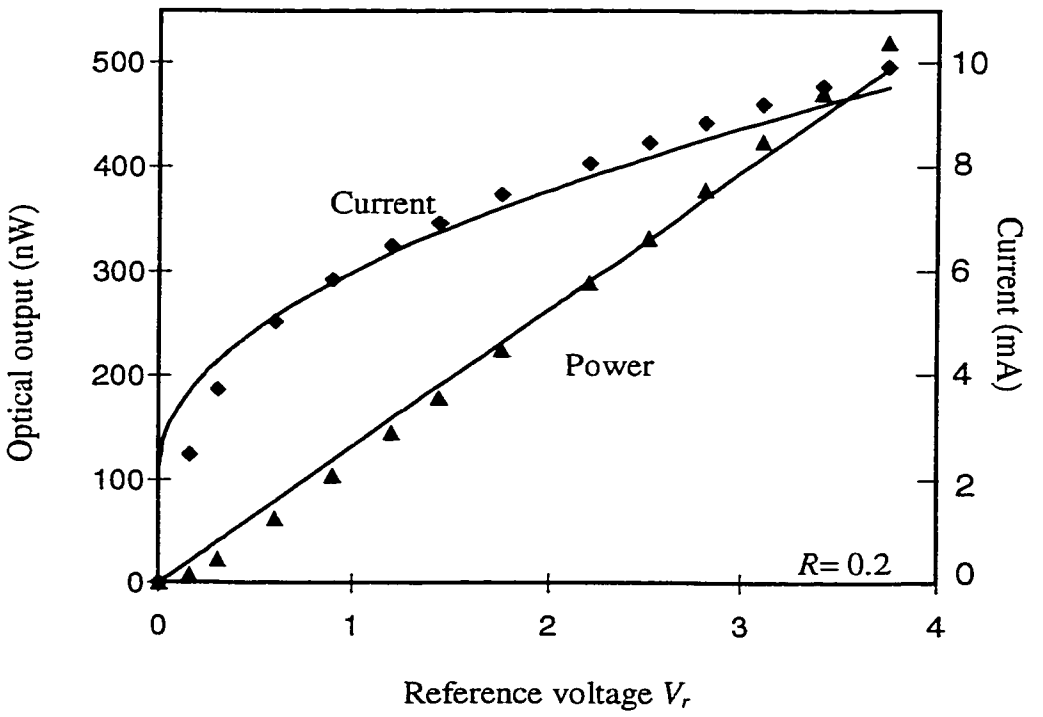


Fig. 3.6. Closed loop electrical and optical outputs as function of V_r. The solid lines are model predictions (Eqs. 3.5 and 3.6) and the markers are experimental results.

The closed loop behavior of the pixel for a constant value of optical feedback and various values of reference voltage is shown in Fig. 3.6. Measured values are shown with markers and solid lines are model predictions. This case corresponds to transmitter applications, where the linearity of the output with respect to the pixel's input is desired. It is seen from the figure that the optical power output is linearized with respect to the input compared to the electrical output (in this case current). The reason is obvious from Eqs. 3.5 and 3.6: the optical output only depends on the reference voltage and optical feedback, whereas the current output additionally depends on the threshold current, the gain K, and the nonlinearity factor n.

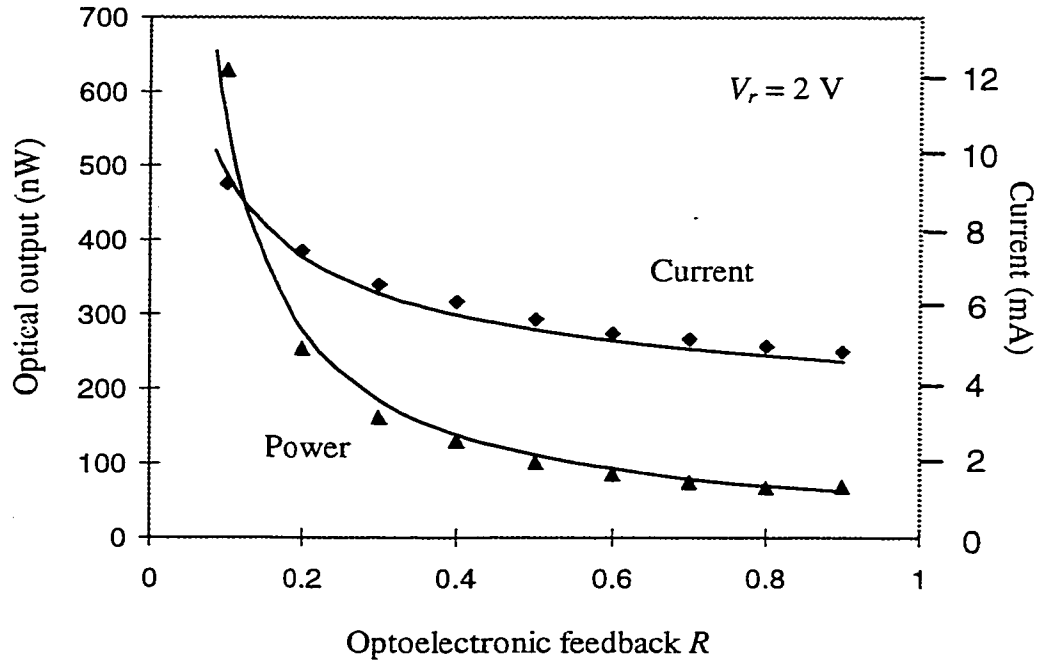


Fig. 3.7. Closed loop electrical and optical outputs as function of optical feedback R. The solid lines are model predictions Eqs. 3.5 and 3.6 and the markers are experimental results.

Figure 3.7 illustrates the closed loop behavior of the pixel for various amounts of optical feedback ($0.1<R<1$) as the input to the pixel and for a constant V_r of 2 Volts. This case corresponds to SPSI sensors where the input to the pixel is the amount of optoelectronic feedback. The markers are the measured values and the solid lines are model predictions. It is seen both from Fig. 3.6 and Eq. 3.6 that the current output approaches the threshold current as R approaches unity. The optical power output, however, approaches zero for high values of R as predicted by Eq. 3.5. These results verify the validity of the high-gain model described by Eqs. 3.5 and 3.6. If the high-gain approximation does not apply, the more general form of the model given by Eqs. 3.2 and 3.3 should be used.

3.5. Summary

In this chapter modeling studies and experimental results were presented for optoelectronic feedback loops focusing on integrated source-based SPA's. It was shown that feedback can be used to minimize certain problems encountered in smart pixel technology. System linearization and reducing the dependence of system performance to light source parameters are among the most important benefits of optoelectronic architectures based on feedback. These results were also applied to the SPSI concept, where the concepts of Chapter 2 were revisited from the optoelectronic feedback perspective. The presented models were also validated with additional experimental results from the OPTOCHIP.

Chapter 4. Smart Pixels with Optoelectronic Interconnection

The last chapter introduced the principles of optoelectronic feedback. The discussion is continued in this chapter by first generalizing the models introduced in Chapter 3 by allowing a general form of non-linearity for the emitters, and also by taking into account the leakage current from emitters to detectors. An independent optical input is also allowed. Next, a matrix formalism is introduced for generalization of the theory to include the behavior of an entire SPA consisting of interacting pixels with arbitrary optical and electrical interconnections. The concept of positive feedback is exploited in the design and implementation of an optoelectronic flip-flop, where VCSEL's are used for the experimental demonstrations instead of the LED-based SPA used in last chapters.

4.1. Issues in modeling SPA's

An in-depth analysis of SPA's is complicated by several factors. The individual pixels in a practical SPA are usually not completely isolated from each other. One of the inherent causes of this lack of isolation is the electrical and optical crosstalk between adjacent detectors and emitters. These devices are fabricated on the same chip and therefore share the same substrate. With shrinking dimensions and the interest in increasing the number of devices on a single chip, the devices may no longer be completely isolated and various electrical leakage mechanisms may exist between adjacent pixels. The same factors result in additional complications for the emitters. While the ability to integrate relatively powerful VCSEL's into arrays on a single chip is a definite advantage, the increased possibility of unwanted optical couplings between a VCSEL and the adjacent detectors is a parasitic effect to be considered. Therefore, in addition to electrical crosstalk, optical crosstalk between adjacent pixels has to be taken into consideration. Another complicating fact in the behavior of SPA's is the nonlinearity of light emitters, the most evident demonstrations of which are the threshold current and saturation effects. All these factors and their effects limit the dynamic range and the available space-bandwidth products for a given SPA and must be understood and modeled as thoroughly as possible

for SPA's to be used in their fullest capacity in various information processing applications.

Cross-couplings between pixels within a SPA are not limited to crosstalk. There are numerous situations where the designer wants to take advantage of the on-chip processing capabilities of SPA's by introducing additional electronic or optical interconnection schemes within and between pixels to achieve improved performance or new functionalities. Such SPA's have applications in, among other areas, neural-networks, analog optoelectronics, and optoelectronic field-programmable gate arrays (OE-FPGA's). A special case of such cross-couplings is optoelectronic feedback, which may be used to address problems related to the nonlinearity and non-uniformity of optical sources.

In this chapter a formalism is developed for modeling source-based SPA's to include arbitrary optoelectronic interconnections as well as crosstalk and/or various feedback schemes within and between pixels in the presence of optical source nonlinearities. From a mathematical perspective these schemes can all be modeled using a single formalism, because they result in coupled equations for various variables within a single pixel or among various pixels within an array. Hence, the term "interconnection" is used in its general sense to mean any electronic or optical coupling between the variables of one pixel or multiple pixels in a SPA. Models capable of accounting for such single- and multiple-pixel interactions are essential for better understanding the behavior of SPA's and are crucial tools in the process of designing practical and new applications for such arrays.

Initially, the modeling of various interconnections and crosstalk mechanisms in the presence of source nonlinearity within a single pixel is addressed. Then the resulting concepts are generalized to multi-pixel interactions within an arbitrary SPA. The single pixel analysis presented is a continuation of the models discussed in Chapter 3 [73], with

the difference that here a more general approach is taken and the focus is on developing the concepts towards a multi-pixel array with nonlinear optical sources and arbitrary interconnectivity. As an experimental demonstration, optical feedback, positive electrical feedback, and the inherent nonlinearity of the VCSEL's are exploited to implement a VCSEL-based optoelectronic flip-flop.

4.2. General Treatment of an Optoelectronic Loop

In order to develop a general model for a SPA, it is useful to expand the concept of a single pixel further. Fig. 4.1 shows the schematic diagram of a single pixel which consists of a light source, a detector, and driver and receiver circuits.

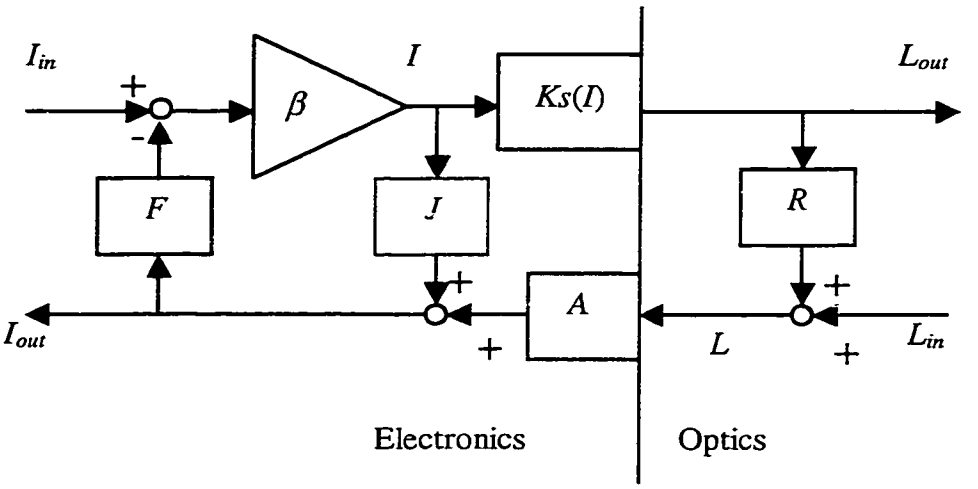


Fig. 4.1. Generalized schematic diagram of a single smart pixel.

The pixel has an electronic input and an electronic output, I_{in} and I_{out}. It also has an optical input and an optical output, L_{in} and L_{out}. These optical signals refer to the intensity of the light. It is further assumed that the optical signals are mutually incoherent so there are no interference effects present. Comparison of this figure with Fig. 3.1 clarifies the more general approach here, which includes a general nonlinearity for the emitter as opposed to a specific form of nonlinearity given by Eq. 3.1, the inclusion of a leakage current from emitter to detector (neglected in Chapter 3), and allowing for an independent optical input L_{in} (assumed zero in Chapter 3). These generalizations allow for viewing the pixel as an interface element for bi-directional exchange of electrical and optical signals. An important aspect of this model is that the optical source is modeled with a nonlinear function $Ks(I)$, where I is the output of the driver circuit β. This is important, because in general all optical sources are nonlinear. They cannot produce negative light if their input becomes negative, and usually they have a saturation current limiting the maximum output power of the pixel. Even within these two limits the output may not be a linear function of the drive current. The same nonlinear function may also be used to model other nonlinearities in the system, such as power supply clipping of the signals or the nonlinearity in the gain of the driving circuit β. Therefore, all the nonlinearities are assumed to be lumped into the function $Ks(I)$. It should be noted that the same concerns are generally not applicable to the detector, because the optical input to the detector is always positive. Also the optical signal levels at the input of the detector are usually much lower than the pixel's optical output levels, which means it is usually sufficient to model the detector with a linear (possibly small signal) gain A.

In addition to the source and detector circuits, there may be several interconnection or crosstalk paths. There can exist optical feedback (or crosstalk), represented by R, from the output of the source to the detector's input. Another effect to be modeled is the current leakage from the source to the detector. This term is represented by J, and as shown later, can negatively effect the performance of the SPA. It should be noted that the opposite effect (current leakage from the detector to the emitter) is usually negligible,

because the signal level at the output of the detector is usually very small compared to the emitter drive current I. Electronic feedback from the output of the detector to the input of the pixel is also allowed. This feedback, denoted by F, is usually intentionally introduced to achieve closed loop behavior. For convenience and without any loss of generality, the output of the F block is subtracted from the electrical input because usually F represents a negative feedback scheme to stabilize the output of the pixel. Later F is generalized to model arbitrary electrical interconnection schemes between various pixels.

Ideally when there is no electrical and/or optical crosstalk and also when no feedback is present ($F = J = R = 0$), the electrical and optical outputs of the pixel are given by:

$$I_{out} = AL_{in}, \tag{4.1}$$

$$L_{out} = Ks(\beta I_{in}). \tag{4.2}$$

As mentioned earlier, however, in practical cases the situation is usually more complicated. The terms J and R may no longer be zero due to proximity of the detector and the source on the same substrate. Moreover, it may be useful to intentionally introduce additional on-chip processing capabilities or feedback schemes to achieve improved performance or specific functionalities. For example, as can be seen from Eq. 4.2, the optical output of the pixel depends on the form of the function Ks, which in general is nonlinear and depends on the characteristics of the individual device, with random variations from one device to the next. The most straightforward solution for these problems is to use negative feedback as represented by the F block.

In the general case, where F, J and R are nonzero, tracing of the signals around the loop results in the following implicit equation for L_{out}

$$L_{out} = Ks\left(\frac{\beta}{1+FJ\beta} I_{in} - \frac{FA\beta}{1+FJ\beta} L_{in} - \frac{\beta FAR}{1+FJ\beta} L_{out}\right). \tag{4.3}$$

Once L_{out} is found, other loop variables can also be found. A graphical solution to Eq. 4.3 provides insight into the behavior of the single pixel. Realizing that the argument of

the Ks function is simply the drive current I, one can find the solution as the intersection of the function $L_{out} = Ks(I)$ and a load line given by

$$L_{out} = -\frac{1+FJ\beta}{FAR\beta} I + \frac{1}{FAR} I_{in} - \frac{1}{R} L_{in} . \qquad (4.4)$$

Figure (4.2) illustrates this situation for a typical $Ks(I)$ function with a threshold and saturation behavior. The intersection of the load line with each axis is also shown in the figure.

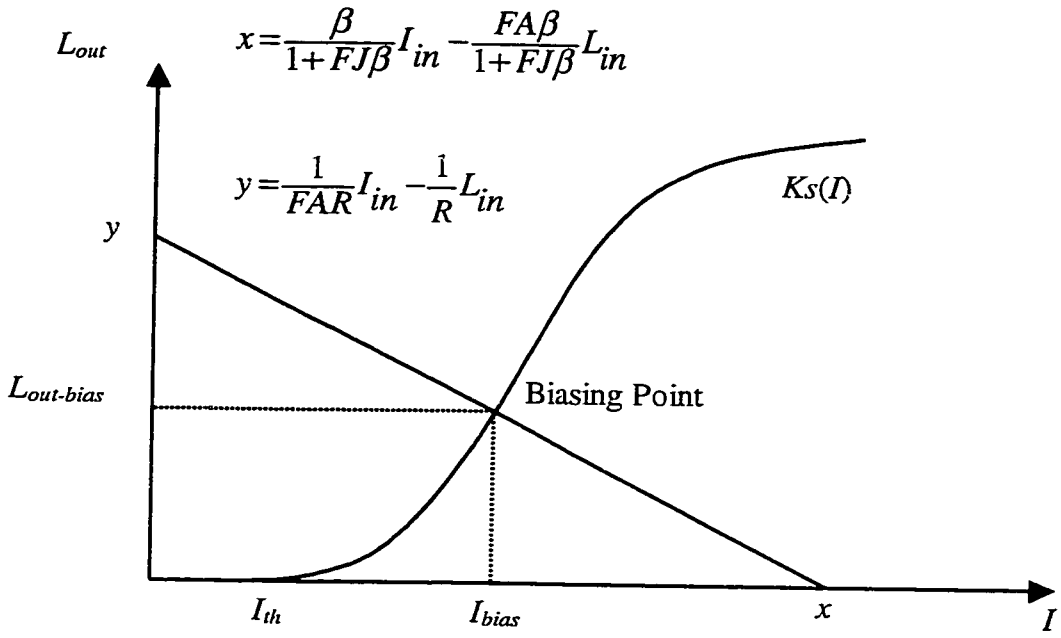


Fig. 4.2. Graphical load-line solution for a single pixel.

It is realized that in order for the loop to be biased in the active region with a single solution, (the situation implicitly assumed in the figure), a necessary condition is that *both* these relations hold

$$\frac{1}{FA} I_{in} > L_{in} , \qquad (4.5)$$

$$I_{in} - FAL_{in} > \frac{1+FJ\beta}{\beta} I_{th} \quad . \tag{4.6}$$

Equation 4.5 requires negative feedback (positive F) while Eq. 4.6 limits L_{in} for a given I_{in} and I_{th}. If, on the other hand, a multi-stable or digital on-off behavior is needed, Eqs. 4.5 and/or 4.6 can be violated and the desired behavior can be achieved by proper choice of the loop parameters. For example, the bistable behavior in the optoelectronic flip-flop discussed at the end of this chapter is achieved by violation of these inequalities. A case of special interest for analog applications is to use negative feedback to make the output of the pixel independent of the device characteristics. Usually this is achieved by increasing the loop gain β and making it large ($\beta \to \infty$) in which case the load line in Fig. 4.2 tends to become horizontal. If the current leakage is negligible (J=0) the optical output is given by

$$L_{out} = \frac{1}{FAR} I_{in} - \frac{1}{R} L_{in} . \tag{4.7}$$

The importance of this case is that the optical output is independent of the function $Ks(I)$, and is linearized in both I_{in} and L_{in}. At the same time, this underlines the importance of having negligible leakage current levels because Eq. 4.7 holds only when J=0. Therefore, it can be deduced that in general the leakage current deteriorates the performance of a negative feedback loop.

4.3. Multi-pixel Analysis

The case of a single pixel discussed in Sec. 4.2 can be used as a basis for analyzing the behavior of a SPA with arbitrary interconnectivity. In the following analysis, an index i is added to all the signal quantities referring to an arbitrary ith pixel within the array. On the other hand, the interconnections are shown with double indexes. For example, J_{ii} and J_{ij} represent the internal emitter-detector current leakage for pixel i, and the current leakage from the emitter of pixel j to the detector of pixel i, respectively. The summation over repeated index convention is also adopted, so the repeated index is a dummy index summed over all the pixels within the array. Fig. 4.3 shows the schematic diagram of an arbitrary interconnected SPA following this notation.

In this figure $\mathbf{F}=[F_{ij}]$ and $\mathbf{R}=[R_{ij}]$ represent the electrical and optical interconnectivity matrices. These matrices model individual electrical and optical gains within pixels and cross-couplings between various pixels. The two matrices $\mathbf{A}=[A_{ij}]$ and $\mathbf{J}=[J_{ij}]$ are the detector crosstalk and current leakage matrices respectively. The matrix $\beta=[\beta_i]$ is a diagonal matrix with elements β_i.

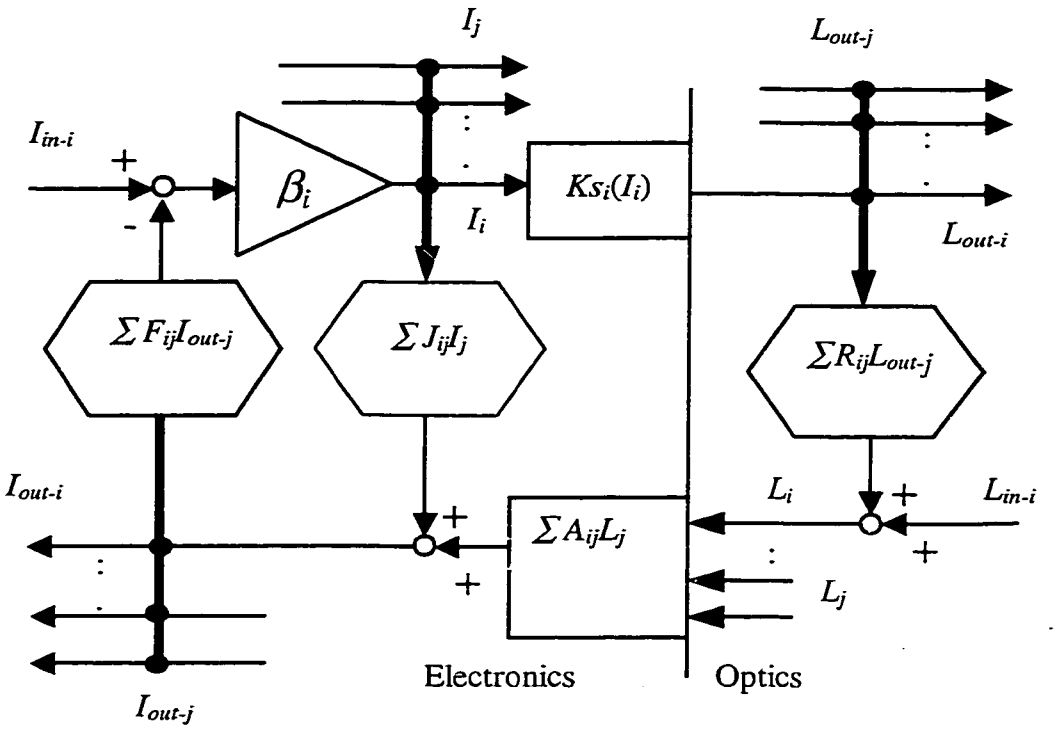


Fig. 4.3. Schematic diagram of a fully interconnected SPA.

By choosing β to be diagonal it is implicitly assumed that there is no cross-coupling between the drivers of the various pixels. This is a reasonable assumption because usually driver circuits operate on high current levels, nevertheless, generalization to a non-diagonal β is straight forward. The signal quantities are represented by $\mathbf{I_{in}}=[I_{in-i}]$,

$\mathbf{L_{in}}=[L_{in\text{-}i}]$ and $\mathbf{L_{out}}=[L_{out\text{-}i}]$; the electrical input, the optical input, and the optical output vectors respectively. Here **F**, **A**, **J**, β, and **R** are square $n\times n$ matrices, and $\mathbf{I_{in}}$, $\mathbf{L_{in}}$, and $\mathbf{L_{out}}$ are $n\times 1$ vectors, where n is the total number of pixels.

To analyze the array, it can be seen that

$$I_i = \beta_i \left[I_{in-i} - \sum F_{ij} I_{out-j} \right], \tag{4.8}$$

while $I_{out\text{-}j}$ can itself be written as

$$I_{out-j} = \sum A_{jk} L_k + \sum J_{jk} I_k \tag{4.9}$$

and L_k can be written as

$$L_k = L_{in-k} + \sum R_{kn} L_{out-n} \,. \tag{4.10}$$

Combining Eqs. 4.9, 4.10, and 4.8 and noticing the repeated indexes are dummy indexes to be summed over, the following implicit equation for **I** is obtained:

$$\mathbf{I} = \boldsymbol{\beta}[\mathbf{I_{in}} - \mathbf{FJI} - \mathbf{FAL_{in}} - \mathbf{FARL_{out}}]. \tag{4.11}$$

Solving Eq. 4.11 for **I** results:

$$\mathbf{I} = [\mathbf{I_e} + \boldsymbol{\beta}\mathbf{FJ}]^{-1}\boldsymbol{\beta}[\mathbf{I_{in}} - \mathbf{FAL_{in}} - \mathbf{FARL_{out}}], \tag{4.12}$$

where $\mathbf{I_e}$ is the square $n\times n$ identity matrix and it is assumed that $\mathbf{I_e}+\beta\mathbf{FJ}$ is a nonsingular and hence invertible matrix. It should be noticed that a sufficient condition for the nonsingularity of this matrix is $\mathbf{J}=\mathbf{0}$.

If the following vector notation is introdued:

$$\mathbf{L_{out}} = \mathbf{Ks}[\mathbf{I}] \equiv [Ks_i(I_i)], \tag{4.13}$$

a formal solution for the array can be obtained

$$\mathbf{L_{out}} = \mathbf{Ks}\left([\mathbf{I_e} + \boldsymbol{\beta}\mathbf{FJ}]^{-1}\boldsymbol{\beta}[\mathbf{I_{in}} - \mathbf{FAL_{in}} - \mathbf{FARL_{out}}]\right). \tag{4.14}$$

Eq. 4.14 can be considered as the matrix generalization of Eq. 4.3. For instance, an obvious special case is when the matrices **F**, **A**, **J**, and **R** are diagonal (no pixel-pixel interaction). Equation 4.14 then decouples into separate equations of the from given by Eq. 4.3. While Eq. 4.14 is an implicit equation in terms of $\mathbf{L_{out}}$, it is also possible to

obtain an equivalent set in terms of the variable **I** by substituting Eq. 4.13 directly into Eq. 4.11:

$$\mathbf{I} = \boldsymbol{\beta}[\mathbf{I}_{in} + \mathbf{FJI} + \mathbf{FAL}_{in} + \mathbf{FARKs}[\mathbf{I}]]. \tag{4.15}$$

The advantage of Eq. 4.15 over Eq. 4.14 is that there are no matrix inversions involved.

Although in general Eqs. 4.14 or 4.15 have to be solved numerically, for example by self-iterative methods, there are important special cases where closed form analytical solutions may be found. Two such cases are discussed here: (a) strong negative feedback and (b) a linear source.

(a) *Strong negative feedback solution*

It is often desired to implement negative feedback to stabilize and linearize the output of nonlinear sources such as semiconductor lasers. For SPA's, this can be achieved by increasing the individual loop gains ($\beta_i \to \infty$ for all i) within the negative feedback loops. For simplicity, it is assumed that the current leakage is negligible (**J=0**). In this case Eq. 4.12 reduces to:

$$\mathbf{I} = \boldsymbol{\beta}[\mathbf{I}_{in} - \mathbf{FAL}_{in} - \mathbf{FARL}_{out}] \tag{4.16}$$

Because β is a diagonal matrix with nonzero elements, it is invertible, and Eq. 4.16 can be written as:

$$\boldsymbol{\beta}^{-1}\mathbf{I} = \mathbf{I}_{in} - \mathbf{FAL}_{in} - \mathbf{FARL}_{out} \tag{4.17}$$

For the case of high loop gains ($\beta_i \to \infty$ for all i) the left hand side of Eq. 4.17 is a vector with small elements ($\boldsymbol{\beta}^{-1}\mathbf{I} \equiv \mathbf{0}$) and therefore:

$$\mathbf{L}_{out} = [\mathbf{FAR}]^{-1}\mathbf{I}_{in} - \mathbf{R}^{-1}\mathbf{L}_{in}. \tag{4.18}$$

This equation is clearly the generalized form of Eq. 4.7 for the single pixel. The importance of this solution, just like the case of a single pixel, is that the optical output vector of the array is expressed as the sum of two linear transformations of the optical and electrical input vectors. This solution also has interesting implications in optical

computing applications, because it can be used to implement the operations of matrix-vector and matrix-matrix multiplication as well as matrix inversion.

(b) *Linear source solution*

Another important especial case in which closed loop solutions may be found is when the optical emitters can be modeled with a threshold current I_{th} and a linear gain K above threshold, so for the ith emitter:

$$L_{out-i}(I_i) = \begin{cases} 0 & I_i < I_{th-i} \\ K_i(I_i - I_{th-i}) & I_i > I_{th-i} \end{cases}. \tag{4.19}$$

This model is particularly useful for VCSEL's, because they have a threshold current below which their optical output is small, and above it the optical output increases relatively linearly with drive current. The linear solution is also useful in small signal analysis, where the whole system is linearized around some operating point.

Using the matrix notation introduced in Eq. 4.13, and assuming all emitters are biased above threshold, Eq. 4.19 can be written as

$$\mathbf{L}_{out}(\mathbf{I}) = \mathbf{K}(\mathbf{I} - \mathbf{I}_{th}), \tag{4.20}$$

where $\mathbf{K}$ is a square diagonal matrix with elements K_i and $\mathbf{I}_{th}$ is a vector with elements I_{thi}. If Eq. 4.20 is substituted into Eq. 4.11, a closed form solution is obtained:

$$\mathbf{I} = \mathbf{M}^{-1}\mathbf{I}_{in} + \mathbf{M}^{-1}\mathbf{FAL}_{in} - \mathbf{M}^{-1}\mathbf{FARKI}_{th} \tag{4.21}$$

where

$$\mathbf{M} = \boldsymbol{\beta}^{-1} - \mathbf{FJ} - \mathbf{FARK}. \tag{4.22}$$

The optical output vector $\mathbf{L}_{out}$ is easily obtained from Eqs. 4.21 and 4.20. The validity of this solution is limited to the case where the array is biased in the active region, a necessary condition for which is that $\mathbf{M}$ should be nonsingular. If $\mathbf{M}$ becomes close to singular, some elements of $\mathbf{I}$ may become very large or negative, and this contradicts the assumption of active biasing. In this case the solution given by Eq. 4.21 is invalid and the general nonlinear Eqs. 4.14 or 4.15 should be used.

4.4. Application of Theory: Optoelectronic Flip-flop

As an example of the application of the theory, the analysis and design of an optoelectronic flip-flop which makes use of positive feedback and source nonlinearity to achieve bistable behavior is presented. In Sec. 4.2 the concept of a load-line generated by the feedback loop around a nonlinear optical source was discussed. In this experimental demonstration, the inherent nonlinearity of the VCSEL is exploited to create bistability. The bistable behavior of the pixel can then be used to make an optoelectronic flip-flop.

The underlying principle of such a flip-flop is illustrated in Fig. 4.4, which is essentially a special case of Fig. 4.2.

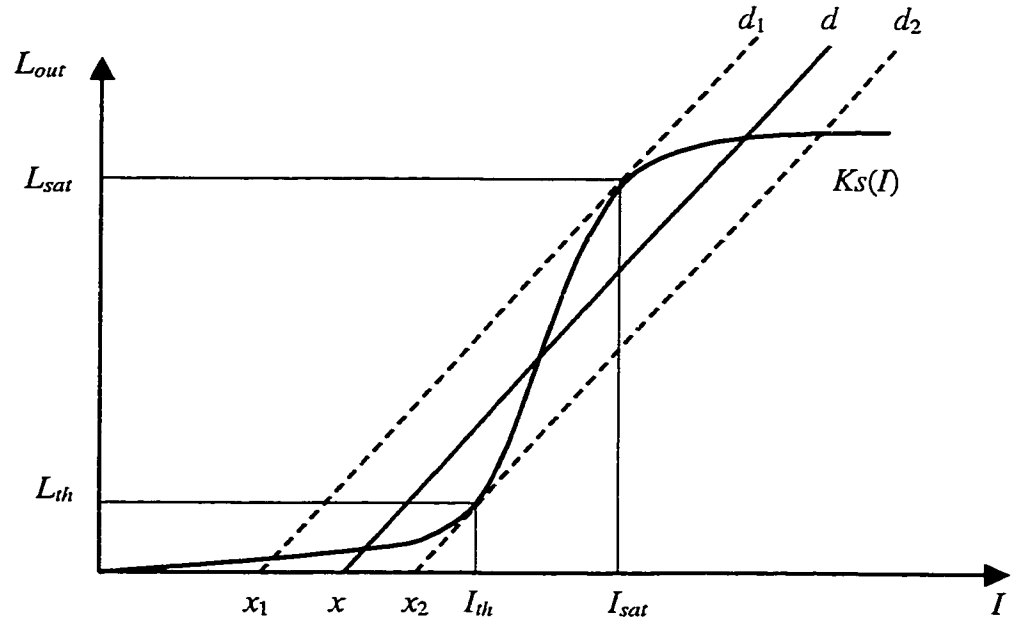


Fig. 4.4. Graphical illustration of the use of VCSEL nonlinearity and positive feedback to implement an optoelectronic flip-flop.

The difference here is that the form of the nonlinearity is chosen to represent a VCSEL with the threshold current and threshold output I_{th} and L_{th}, and the saturation current and saturation output I_{sat} and L_{sat}. The saturation can be intrinsic to the device, or be made to represent current limiting due to driver circuits. Also three instances of the load-line, d_1, d, and d_2 with horizontal axis intersections x_1, x, and x_2, are shown for a positive feedback (negative F) case. The variable x is a function of loop parameters and the optical and electrical inputs L_{in} and I_{in},

$$x = \frac{\beta}{1+FJ\beta} I_{in} - \frac{FA\beta}{1+FJ\beta} L_{in}, \tag{4.23}$$

and the slope of the load-line is given by

$$m = -\frac{1+FJ\beta}{FAR\beta}. \tag{4.24}$$

It can be seen that as the inputs to the pixel, L_{in} and I_{in}, vary, the load-line shifts left or right while its slope remains constant. As the load-line moves from left to right, the VCSEL is first biased below threshold, and as the load-line passes d_2, the VCSEL is switched on to saturation. On the other hand, if the load-line moves towards the left, the VCSEL is initially biased in the saturation region, and as the load-line passes d_1, it is switched off to sub-threshold. Therefore, hysteresis is created which can be utilized to implement an optoelectronic flip-flop. It should be noted that while the load-line is between d_2 and d_1, a third solution (in the active region) is mathematically possible. However, this is an unstable solution because of the positive feedback loop.

Using Eqs. 4.23 and 4.24, and for a given VCSEL characteristic, the pixel's parameters are chosen such that the load-line is normally located between d_1 and d_2. Once an input optical pulse L_{in} is received, the load-line moves to the right of d_2. When the optical pulse is removed, the load-line returns to its normal position, but the pixel stays on. This constitutes the "set" operation of the flip-flop. To turn off the pixel, a negative pulse on the biasing input current I_{in} should be applied. Decreasing I_{in} causes the load-line to move left passed d_1, resulting in flipping the VCSEL to sub-threshold bias. Now if the

negative pulse on I_{in} is removed, the load-line again returns to its normal position between d_1 and d_2, but the pixel stays off. This constitutes the "reset" operation of the flip-flop. This thus creates an optically-set, electrically-cleared flip-flop.

4.5. Experimental Demonstrations: VCSEL-MSM Array

In the previous chapters the optoelectronic LED-based chip provided through the OPTOCHIP program was used for the experimental demonstrations. While this technology provides a promising platform for future optoelectronic applications, it suffers from certain shortcomings at its present level of development. For the purposes of this research, the most serious problems of this technology have to do with the integrated LED's. The efficiency of the LED's are generally low, limiting their output power to below 1μW. This low level of output is the main limiting factor in their applications. Moreover, it was found that the LED's outputs deteriorated as a function of time and biasing current, such that the higher the biasing current was, the faster the output power deteriorated.

The majority of these problems could be addressed with VCSEL's and the relatively mature technology associated with them. An opportunity to use VCSEL-based arrays was opened around 1998 through the Consortium for Optical and Optoelectronic Technologies in Computing (CO-OP) as a project established by the Defense Advanced Research Projects Agency (DARPA) to enhance interaction between device researchers and systems researchers in Optics in Computing.

This program provided the research group at UW with a 4×4 array of interlaced VCSEL's and MSM detectors fully wire-bonded and packaged to provide individual addressing capability and custom lenslet arrays with 1 micron feature size and 8 phase levels. The schematic diagram of this chip is shown in Fig. 4.5. The VCSEL-MSM chip was fabricated by Honeywell Corporate Technology Center. The VCSEL's have a common cathode connection and each anode is connected to an external pin. The MSM detectors

have both their terminals connected to external pins. The parameters for the VCSEL's and MSM detectors are as follows :

•VCSEL Parameters:

Wavelength: typically 850nm, range 830 - 860nm

Threshold current: typically 5mA; range 3-6mA

Forward voltage: 1.8-2.1 volts at 10mA

Beam divergence angle: about 15 degrees FWHM

Optical power: greater than 1mW at 10mA

Array spacing: center-to-center spacing 250um

Optical window: proton-implanted VCSEL's with 15um aperture

•MSM Detector Parameters:

Refractory metal MSM detector responsivity: 0.25A/W between 830 and 860nm

MSM dark current: less than 1uA at 5 volts

MSM bias voltage: greater than 2 volts

MSM detector size: 75×75 um

Array spacing: center-to-center spacing 250um, centered within VCSEL array

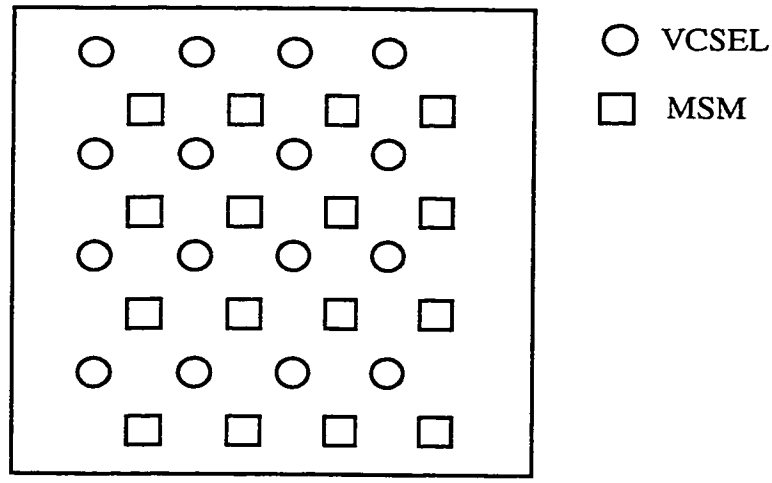


Fig. 4.5. Layout of VCSEL-MSM Chip.

The photograph of a sample VCSEL in this array surrounded by 4 MSM neighboring detectors is shown in Fig. 4.6.

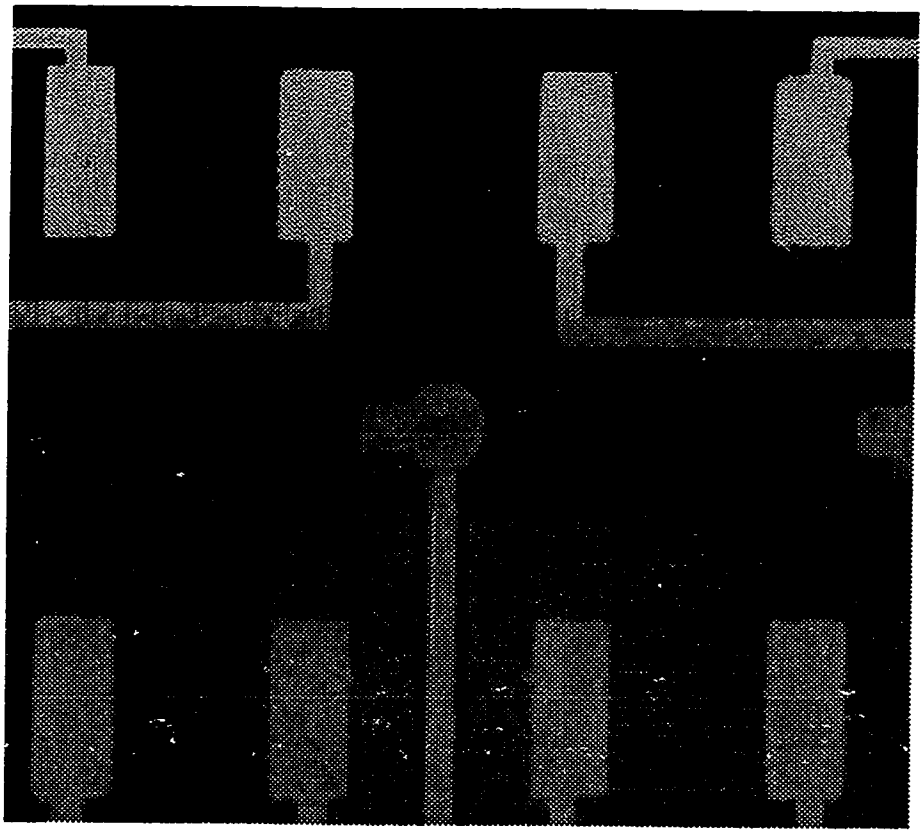


Fig. 4.6. Photograph of a sample VCSEL of the array surrounded by 4 MSM detectors.

For the purpose of these experiments, the most important feature of the VCSEL's is their output characteristic. Fig. 4.7 shows the I-L curve for a sample pixel on the chip. As can be seen from the figure, the VCSEL shows a threshold current of roughly 10mA, somewhat off from the 5mA (typical) specification. This may be attributed to the fact that all experiments were carried out with the first chip received from the CO-OP project,

which was claimed to be an experimental run, not necessarily meeting all the expected specifications. A second chip was also received but it was not used in any experiments.

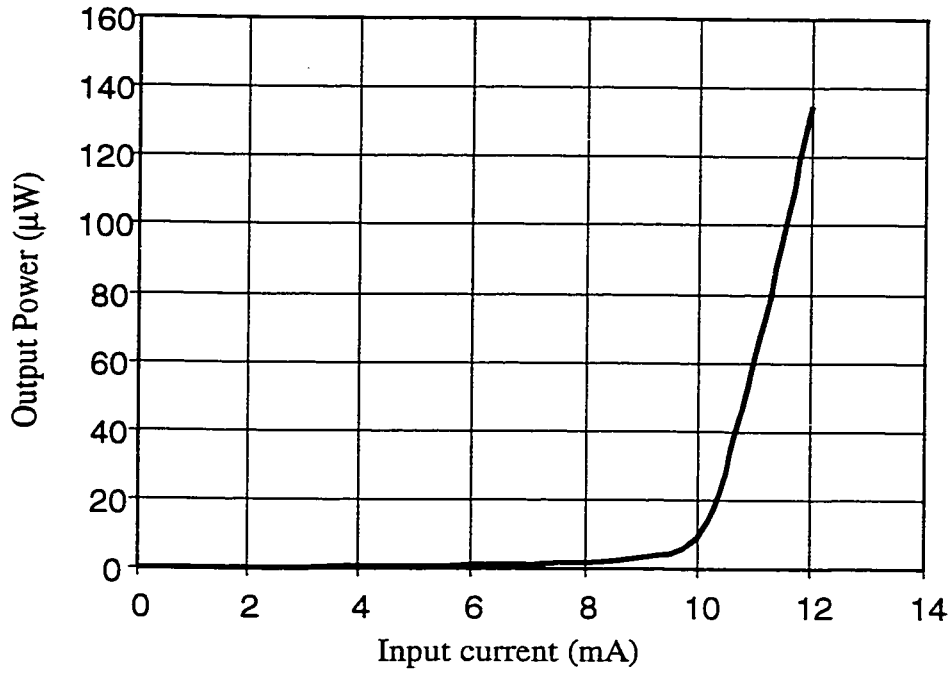


Fig. 4.7. Output characteristic of a VCSEL used in the experiments.

The VCSEL-MSM chip was first used to demonstrate the optoelectronic flip-flop. As was shown earlier, the realization of bistability requires a saturation region in the output, as is clear in Fig. 4.4. Although the output of the VCSEL would eventually saturate, pushing it to current levels much above threshold was not desirable. Therefore, using CMOS driver circuits, the saturation current and output were limited to roughly 11.5mA and 95μW respectively. This is a clear example of a case where the nonlinear function $Ks(I)$ models other nonlinearities in the system in addition to those of the VCSEL. The current leakage coefficient between the VCSEL and the adjacent MSM detector was measured to be $J=2.7\times10^{-5}$. The gain of the detector was measured at A=0.3 A/W, and

the electrical loop-gain was set at $FA\beta$= -0.79 mA/μW. The optical feedback coefficient was set to R=0.09. The leakage loop gain was $FJ\beta$= -0.071, much smaller than unity. This meant that the effect of the leakage current was small. These parameters resulted in a load-line slope of m=13 μW/mA according to Eq. 4.24.

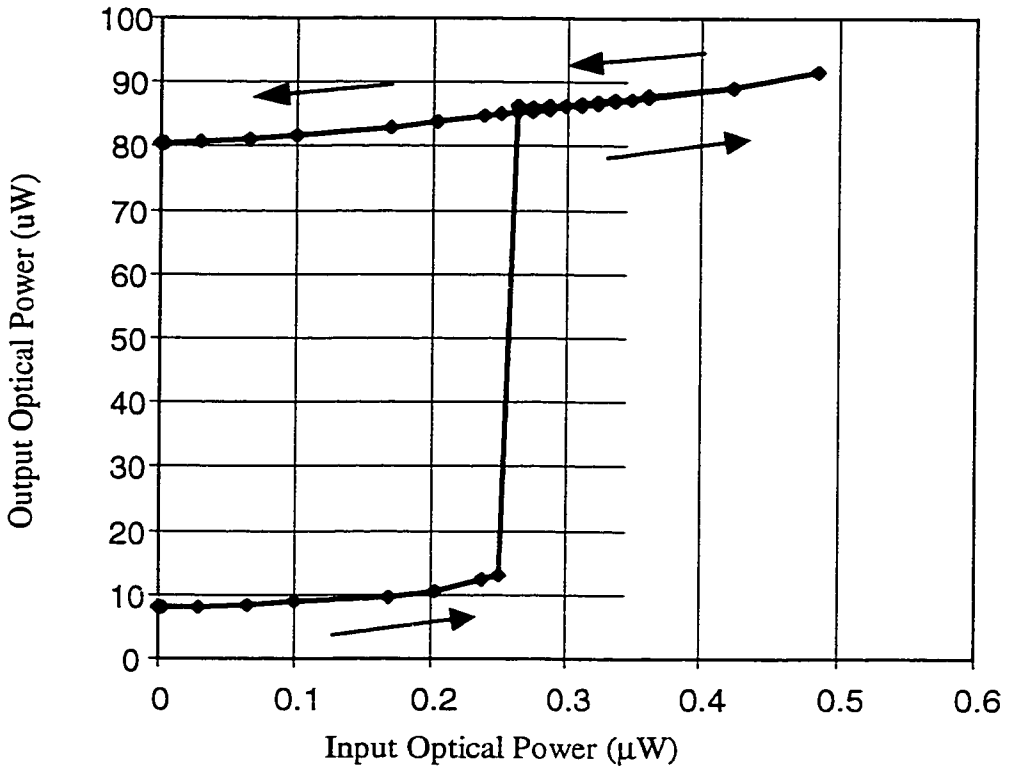


Fig. 4.8. Demonstration of input optical pulse capture.

The slope of the VCSEL characteristic in the active region was roughly 43μW/mA, larger than the slope of the load-line. This ensured that the situation depicted in Fig. 4.4 was realizable. Using an external laser source, an optical input was applied to the pixel and gradually increased while the optical output of the pixel was monitored. A plot of the optical output versus the optical input is shown in Fig. 4.8. As the optical input was

increased, the optical output of the VCSEL also increased. This corresponds to moving the load-line with the slope of m=13 μW/mA in the sub-threshold region of the VCSEL characteristic, resulting in sub-threshold output powers. From Fig. 4.8 it is seen that the pixel flips on at an optical input power of about 0.25 μW. At this point the output power is about 13μW, in agreement with the threshold output of the VCSEL seen in Fig. 4.7. Once the VCSEL is flipped on, the output is limited by the driver circuits. The slope of the curve in this region corresponds to the output impedance of the driver circuits. The optical input was then reduced, causing the VCSEL's output to also reduce. Nevertheless, the pixel stayed on even when the optical input signal was reduced down to zero. This demonstrates the capture of an optical input pulse by the flip-flop. To "reset" the flip-flop, the electrical input I_{in} which biases the loop should be decreased, as previously explained.

4.6. Multi-Pixel Effects in Optoelectronic Flip-flop

The operation of the flip-flop discussed so far is based on a single pixel analysis. To demonstrate multi-pixel effects, crosstalk mechanisms between adjacent pixels are addressed. First, the optical interconnection and current leakage coefficients (R_{ij} and J_{ij}) from VCSEL sources further away on the chip were measured. The quantities related to the flip-flop are denoted by index 1 and the adjacent VCSEL's are denoted by higher indexes. This measurement can be done by turning on the adjacent VCSEL's and measuring the output of the detector. The results of these measurements for VCSEL-1 as well as two additional VCSEL sources are: $J_{11}=2.7\times10^{-5}$, $J_{12}=7.8\times10^{-6}$, $J_{13}=9.4\times10^{-6}$, $R_{11}=0.9$, $R_{12}=0.008$, and $R_{13}=0.004$. These results are shown in Fig. 4.9. It should be noticed that the R_{11} and J_{11} coefficients are the same as the R and J coefficients of the flip-flop. The measured coefficients are plotted against the distance between the centers of the VCSEL's to the center of detector. It can be seen that the optical interconnection coefficient reduces almost one order of magnitude by going from the closest VCSEL to the next VCSEL further away.

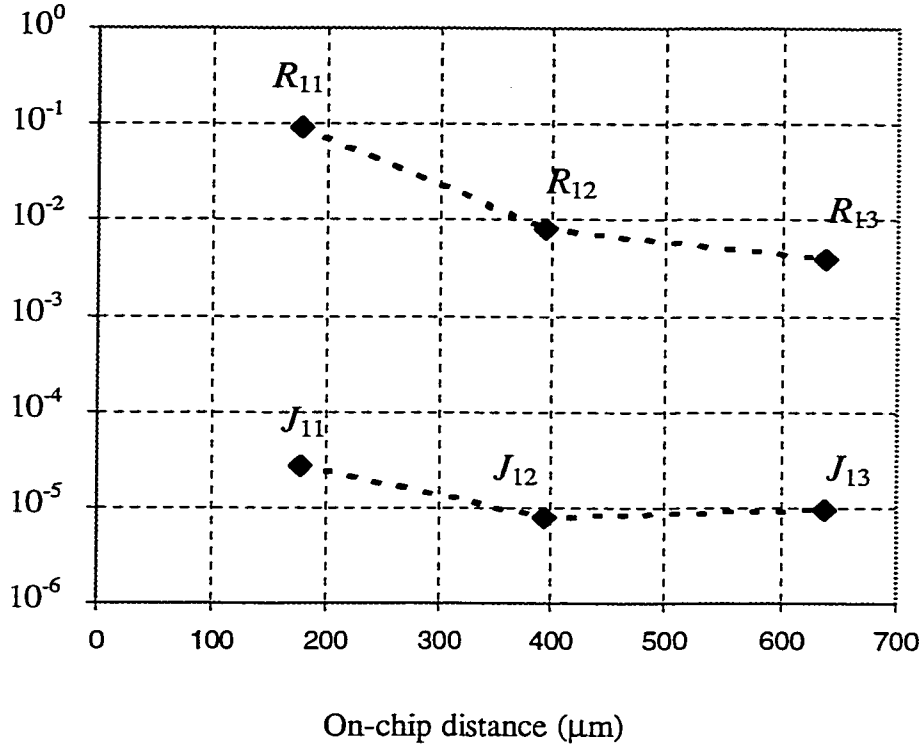


Fig. 4.9. Optical feedback and current leakage coefficients (R_{11}, R_{12}, R_{13}, J_{11}, J_{12}, J_{13}) for three VCSEL sources versus on-chip distance.

This is expected because the first VCSEL was intentionally coupled to the detector to implement optical feedback. However, the couplings from VCSEL's further away can be attributed to stray light and inaccuracies in the optical system. The current leakage coefficient also decreases by going from the adjacent VCSEL to the next VCSEL, however, it slightly increases for the third VCSEL. This anomalous behavior was verified several times in different experiments and may be due to the underlying geometry of the various layers on the chip. The determination of the exact cause(s) of this behavior lies outside the scope of this thesis and needs further investigation.

The effects of the adjacent sources on the behavior of the flip-flop can be modeled using the multi-pixel analysis of Sec. 4.4. For simplicity, only the effects of couplings with a single additional VCSEL are considered. In this case, the operating point of the adjacent pixel can be set independently because there is no electrical interconnection present (F_{22}= F_{12}= F_{21}=0). However, the operating point of the extra VCSEL effects the load-line of the pixel implementing the flip-flop.

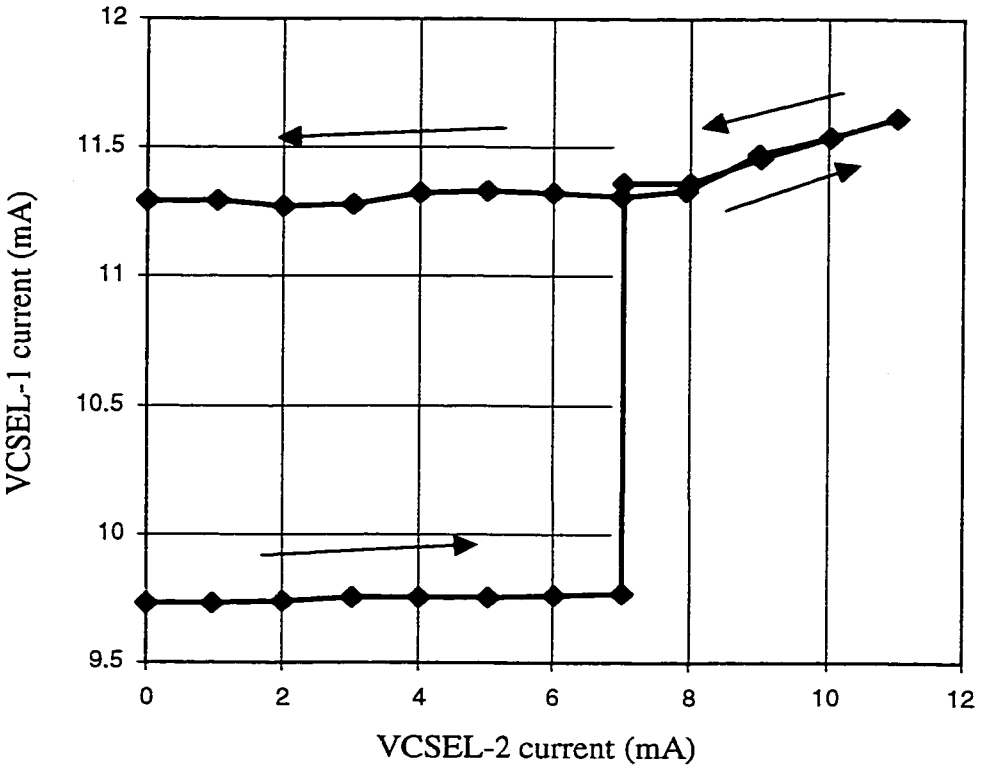


Fig. 4.10. Effect of crosstalk from a second VCSEL source on the flip-flop.

In fact, if the first component of Eq. 4.12 is written and solved for the optical output of the first pixel (flip-flop), a load line in the form:

$$L_{out-1} = -\frac{1+\beta_{11}F_{11}J_{11}}{\beta_{11}F_{11}A_{11}R_{11}}I_1 + \frac{1}{F_{11}A_{11}R_{11}}I_{in-1} - \frac{J_{12}}{A_{11}R_{11}}I_2 - \frac{R_{12}}{R_{11}}L_{out-2}. \qquad (4.25)$$

is obtained. Equation 4.25 predicts that the drive current and the optical output of the second VCSEL can shift the load-line of the first pixel to left or right without effecting its slope.

It can be verified from Eq. 4.25 that if F_{11} is negative (positive feedback for first pixel) increasing I_2 and $L_{out\text{-}2}$ shifts the load-line to the right, causing the flip-flop to turn on. This was observed experimentally and the results are shown in Fig. 4.10. In this figure the drive current of the adjacent VCSEL was swept while the drive current of the first VCSEL (corresponding to the flip-flop) was being observed. The flip-flop switched on when the driving current of the second VCSEL exceeded 7mA, which roughly coincided with its threshold current. Moreover, the slope of the curve after switch-on is significantly higher compared to when the flip-flop is off (where the slope is nearly zero). This means that in this case the main contribution to crosstalk from the adjacent VCSEL to the flip-flop is optical for two nearest neighbor VCSEL's. For VCSEL's further apart, the optical couplings may decrease to a level where optical and electrical couplings become comparable.

4.7. Summary

In this chapter the concept of single pixel optoelectronic feedback loop of Chapter 3 was expanded to make it suitable for generalization into a matrix formalism for modeling a fully interconnected SPA. These models are crucial tools for the analysis and development of new applications for SPA's especially as the number of devices per area on a single chip continues to rise while the trend to take advantage of parallel on-chip processing and full optoelectronic interconnectivity capabilities of SPA's is becoming evermore important. The models include the nonlinearities in the emitters as well as various leakage, cross-couplings, and more general optical and electrical interconnections between the pixels. Closed form solutions for two important special cases were obtained. As an experimental verification of the developed models, the application of the theory in

the design and implementation of a VCSEL-based smart pixel optoelectronic flip-flop was demonstrated.

Chapter 5. Interfacing with Optoelectronic Arrays: A Current Mode Modular Approach

In the previous chapters several issues regarding smart pixel arrays were discussed without explicitly distinguishing between the optoelectronic devices (emitters and detectors) and the driving electronics. Ideally it is desirable to have all these elements integrated on the same chip. However, such an integration faces several challenges, the most important of which is the incompatibility of Si-based electronics with GaAs based optoelectronics. An interim solution is to have the optoelectronic and electronic devices on different chips. In this approach a single SPA is physically implemented in separate sites where an optoelectronic (OE) array consisting of emitters and detectors is interconnected with a purely electronic interface circuit. The reminder of this dissertation deals with such electronic interface circuits, starting in this chapter with current mode circuits suitable for driving optical sources such as VCSEL's, detecting outputs of detectors, and basic on-chip signal processing. These circuits represent a modular approach, i.e., they can be connected together in different configurations to implement various functions. Additional specific layout or simulation results given for these circuits throughout the chapter are related to a CMOS chip designed and fabricated to demonstrate the functionality of some of the discussed concepts. Further experimental results from this CMOS chip in conjunction with the VCSEL-MSM array are given at the end of the chapter.

5.1. Current Mode Circuits

Traditionally most of analog circuits have been implemented in the voltage domain, where currents usually get transformed to voltages before any further processing. However, as the advantages of current mode processing have become clearer, current mode analog circuits have become much more popular [74]. Current mode processing also offers attractive solutions for signal processing applications where the capability of adding and subtracting signals fast and efficiently is a must. In voltage-mode circuits this is not trivial for ground-referenced signals, usually requiring opamp implementations. In current mode circuits adding and subtracting signals (currents) is trivial, as it is readily

implemented in a node following Kirchhoff's current law. Current mode circuits also can be faster, because they generally include low impedance nodes resulting in lower time-constants. Current mode circuits are also capable of larger dynamic range, typically 0.1nA to 10mA (8 decades) compared to 1mV to 10V (4 decades) for voltage circuits.

Current mode circuits are particularly suitable for interfacing with optoelectronic devices because almost all optoelectronic devices are current controlled. A diode laser, for example, is best controlled by a current source rather than a voltage source. Likewise, a diode detector produces a current as its output. Therefore, a current mode approach to the implementation of circuits for interfacing with OE arrays seems natural. The remainder of this chapter focuses on these circuits, their implementation through a specifically designed CMOS chip, and experimental results from the fabricated chip in conjunction with the VCSEL-MSM array.

5.2. Programmable Current Mirrors

A general current gain structure is one of the most useful blocks that may find applications in a variety of situations, such as in amplifying the output currents of the detectors or controlling the biasing level of the emitters. The ability to control the gain accurately is also important, because gain is one of the major factors which determines the behavior of a circuit. The necessity for accuracy in gain control suggests a digital approach. A suitable approach to the implementation of such a controllable gain module is offered by binary weighted current mirrors. This approach allows for the ability to set the gain of the stage digitally by a bit pattern, the accuracy of which depends on the number of bits implemented. Figure 5.1 shows an example of such an nMOS circuit with 5-bit gain resolution.

As can be seen from the figure, the circuit uses a series of transistors connected in parallel at its output. Each of these transistors is cascoded with another gating transistor which can be switched on or off by its gate voltage. This results in an improved output

impedance and the ability to control the gain by applying a bit pattern $a_4a_3a_2a_1a_0$ to the gates of these transistors. The current gain of the circuit can be written as:

$$I_{out} = G_n I_{in} = (a_0 + 2a_1 + 4a_2 + 8a_3 + 16a_4) I_{in}. \qquad a_i = 1,0 \qquad (5.1)$$

This circuit in fact is a digital to analog converter (DAC), which because of its compactness, is suitable for layout in OE array interface chips. However, for the applications of interest here, the term programmable current mirror is appropriate because normally I_{in} is the input and I_{out} is the output of the circuit.

Although the principles of operation of this circuit are straight-forward, a few points have to be considered in the layout of the circuit. While it is possible to simply size the width of these transistors properly, a better approach is to have a single "unit transistor" and create larger transistors by connecting these unit transistors in parallel.

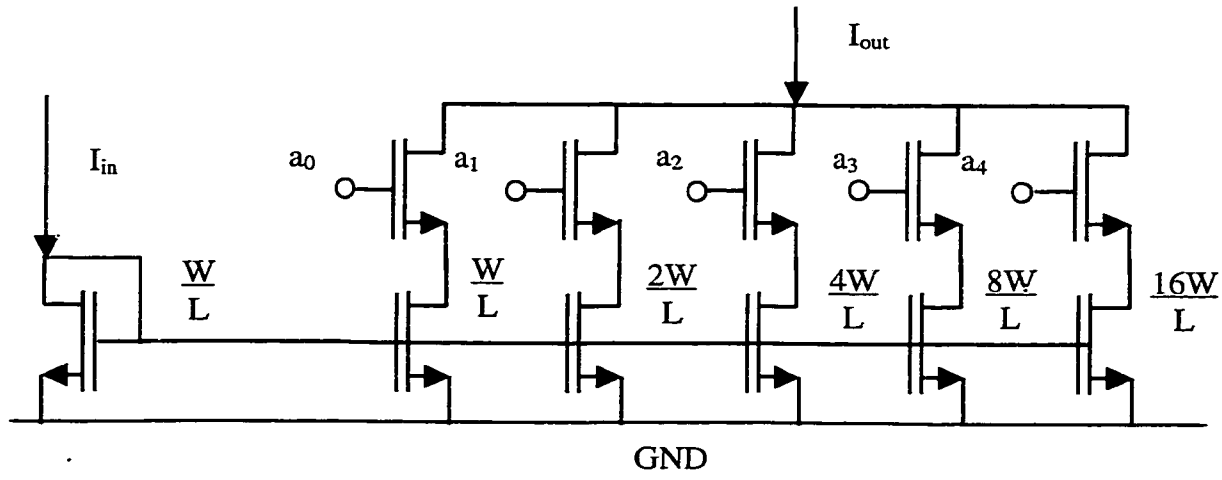


Fig. 5.1. nMOS programmable current mirror (5-bits).

This approach ensures the accuracy of the ratios between transistors while canceling the potential sizing errors due to different boundary conditions among different transistors. To further ensure the accuracy of the actual gain, a dummy transistor is included next to

the input transistor (not shown in the figure) to make the boundary conditions for all the transistors as close as possible. As a result of these considerations, the final layout of the circuit looks exactly homogeneous (except for interconnects) across its length, helping the performance of the actual circuit to approach what is predicted by Eq. 5.1. Choosing W and L for this circuit requires several considerations with respect to the input and out output impedance of the module as well as the over-all size of the block. Ideally this circuit must show zero input impedance (to prevent loading the source of I-in) and infinite output impedance (so that the output behaves like a current source). The small-signal input impedance is proportional to L/W while the small-signal output impedance of each branch is proportional to L/I_D, where I_D is the drain current of that branch. So as a general rule increasing L results in increasing both the input and output impedance. Using SPICE simulations, the values of W=3.6 μm and L=18.6 μm were chosen.

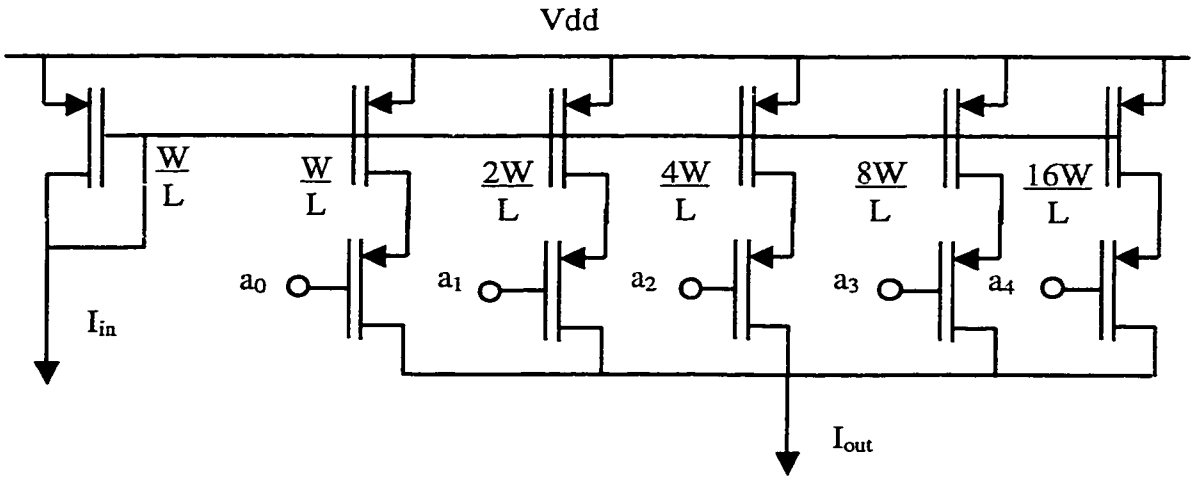


Fig. 5.2. pMOS programmable current mirror (5-bits).

The nMOS current mirror module just described can only sink current at its output. Because in general both current sources and sinks are required, the same circuit was also

implemented in the demonstration CMOS chip using pMOS transistors. Figure 5.2 shows the schematic diagram of the pMOS programmable current mirror. The same layout concerns related to the nMOS stage have to be taken into account in the layout of the pMOS stage as well. Transistor sizes were chosen at W =3.6 μm and L = 42.6 μm using SPICE simulations.

5.3. Signed Current Mirror

In the previous section essentially two implementations of the same current mirror circuit were discussed, one with a current source output (pMOS) and the other with a current sink output (nMOS). Naturally the need is sensed here for a module capable of acting both as a current source and a current sink at its output. The signed current mirror depicted in Fig. 5.3 is a simple example of such a circuit.

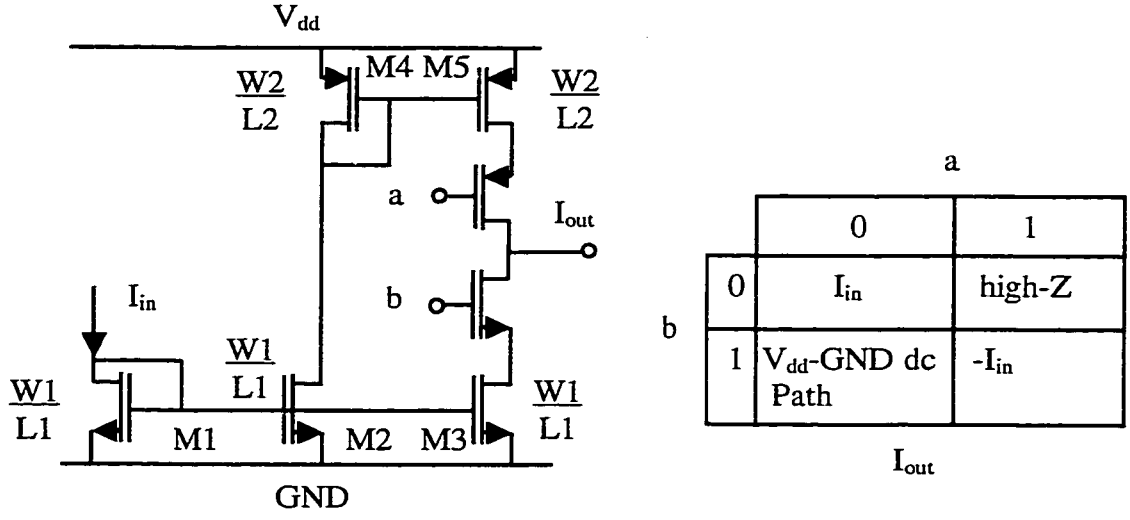


Fig. 5.3. Signed current mirror.

The term "signed" is used here because changing from current sink to source is equivalent to changing the sign of a current signal (current entering a node as opposed to current exiting a node). This goal is achieved in the circuit of Fig. 5.3 by applying proper voltages (on-off) to the gates of the two switching transistors a and b. These switching transistors also improve the output impedance of the circuit. In addition to the two states of current source and sink, the circuit has two more states: if b is grounded and a is kept at V_{dd} both the switching transistors are off and the circuit goes to a high-impedance output stage. This is useful when it is necessary to disconnect the output of the stage using its control bits. The other state is when b is at V_{dd} and a is at GND, in which case both switching transistors are on. This is not a useful state because it results in a DC current path from V_{dd} to GND. So care should be taken not to program the module in this state. The sizes of transistors (in μm) used in the layout of this circuit are W_1/L_1=21.6/18, and W_2/L_2=32.4/45.4. The table of Fig. 5.3 summarizes the function of the module as a function of its input current and the bit pattern present at its inputs.

5.4. Emitter Driver

The emitter driver has to deliver relatively high amounts of current (above 10 mA in the case of the VCSEL array) to the emitters on the OE array. On the other hand, it is important to perform signal processing in a low current level due to power and heating considerations and only amplify the current level before the final output stage. Assuming that the bulk of processing is carried out in the μA range, and that the emitters' driving current is in the mA range, about two to three orders of magnitude of current gain is required for the emitters. Therefore an emitter driver module is necessary to provide this gain at the final output stage. Figure 5.4 shows the schematic diagram of this module as implemented in the CMOS chip. The high current gain is achieved by cascading an nMOS and a pMOS current mirror (M_1,M_2 and M_3,M_4 respectively) and distributing the gain between the two by properly sizing the transistors. The sizes of the transistors in the CMOS layout (in μm) are as follows: M_1: 2.4/4.8, M_2: 66/4.8, M_3: 240/7.2, and M_4: 1500/7.2.

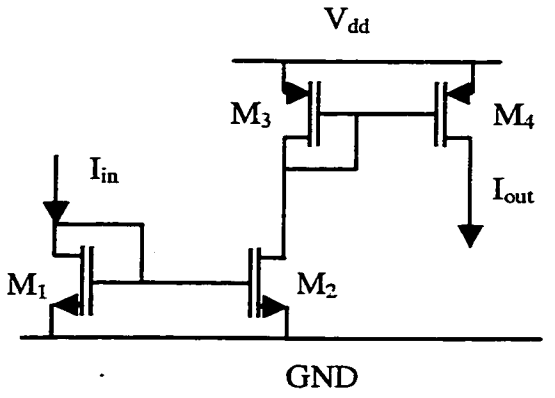


Fig. 5.4. Emitter driver.

These sizes result in a nominal gain of 170, although as will be seen later, the actual achieved gain is higher. Like the current mirrors previously discussed, here too the transistors are formed by repeating smaller unit transistors and connecting them in parallel. For example M_2 is formed by connecting together several transistors similar to M_1, which allows for accurate design of the gain.

The output of the module is deliberately designed to be a current source. This is because it was intended to run common cathode VCSEL's on the OE chip and therefore it was necessary to have a pMOS stage at the output. Considering the amount of current it must provide, the output transistor M_4 had to be made very large. In fact, it is by far the largest transistor of the demonstration chip.

5.5. Opamp

An opamp is a very useful block for a variety of analog applications. However, opamps are complicated circuits and their use often requires additional off-chip components. In fact, often for a specific application an opamp is an over-designed module, and simpler circuits can replace it. For instance, the current processing circuits discussed so far are generally simpler than an opamp, and are more efficient for the specific purpose they are

designed for. For this reason use of opamps as main blocks within the interface circuits was avoided.

Nevertheless, having a tested opamp block could in general be very useful and may become necessary for potential future applications. Specifically, a simple, low-power, and small area opamp is needed so that it can be replicated many times on a single chip if need be. Figure 5.5 shows the circuit used for this purpose. With the AMI 1.2 process parameters, SPICE simulations predict a gain of 50db, and a phase margin of about 90 degrees.

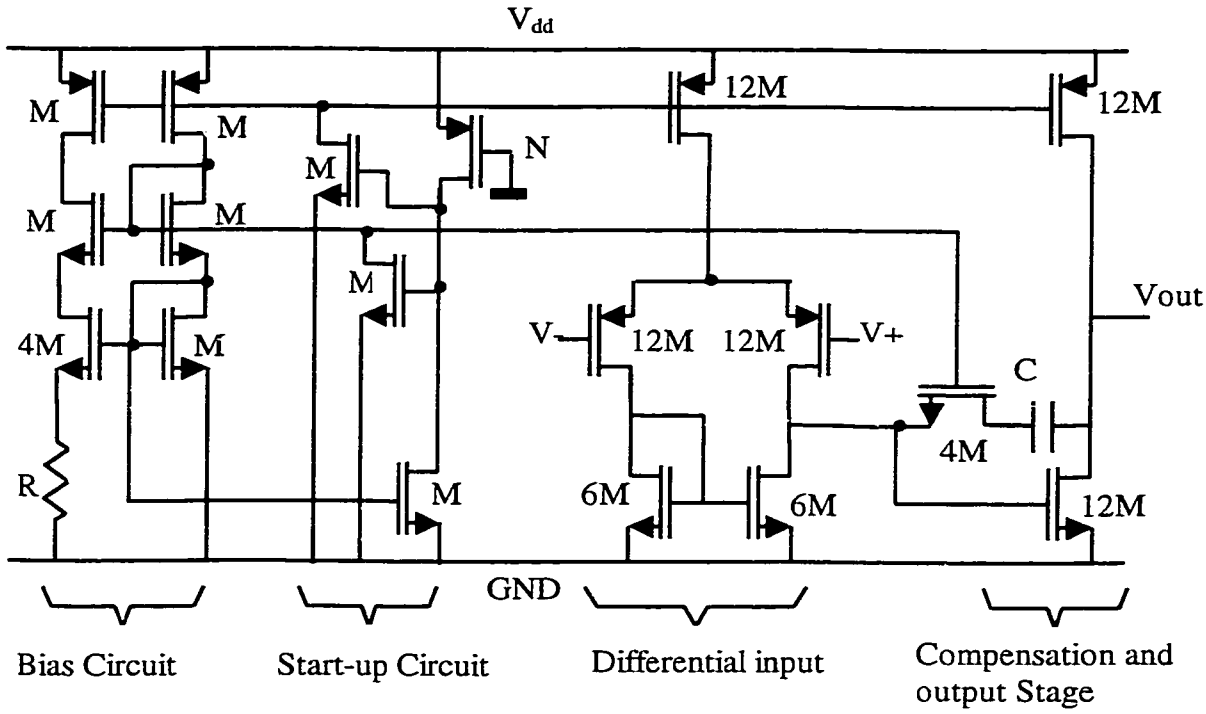


Fig. 5.5. Schematic diagram of a simple two-stage opamp.

The open-loop 3db bandwidth is more than 10kHz. The size of the opamp in the CMOS layout is approximately 390×150 μm^2. The sizes of the transistors given in Fig. 5.5. are in units of M, which means they are made of parallel connections of a unit transistor M,

with W/L=25.2/1.8). The only different transistor is N (W/L=1.8/20.4) which acts as a pull-up resistor for the start up circuit. The compensation capacitor C in this design is 5pF, and R (implemented as a poly resistor) sets up the bias (R=5.5k).

5.6. CMOS Demonstration Chip

The first CMOS chip for a proof of concept demonstration of the discussed circuits was designed in March 1999. The design and layout of the circuits was carried out with Tanner Tools software, including Ledit for layout, and Tspice for simulation of the circuits. The chip was then fabricated through the MOSIS service using the AMI 1.2 analog process. Figure 5.6 shows the floor-plan of the die (the relative size of the blocks and the die area are not to scale) and the corresponding pin numbers on the 40-pin DIP package.

The inputs and outputs of all the modules were brought off the chip. This results in maximum flexibility in arranging the blocks, allowing for testing each module individually as well as in a variety of configurations. However, the disadvantage of this approach is that the number of bond-pads on the die and pins required on the package grows fast with the number of modules, making this approach suitable only for test purposes on a small scale. The following modules were included in the layout: 5-bit nMOS and pMOS programmable current mirrors, signed current mirrors, output driver, and the op-amp described in Sec. 5.5. There are three V_{dd} and three GND connections on the pad-ring. Pins 2,3, and 4 were connected to a pair of simple nMOS and pMOS current mirrors, but due to a layout design flaw of assigning a common pad for both of their inputs, their experimental applicability was limited.

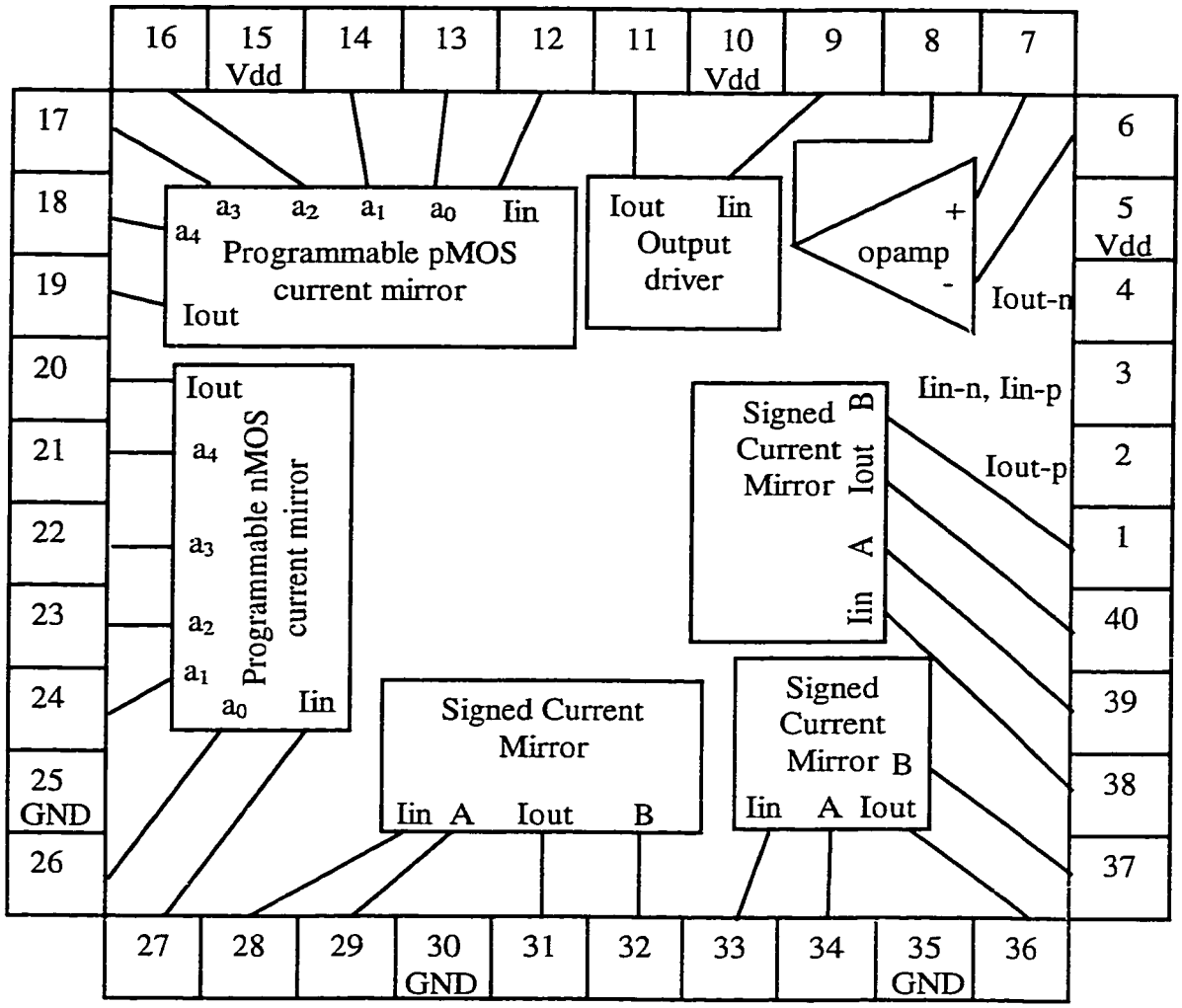


Fig. 5.6. Floorplan of the CMOS demonstration chip.

5.7. Experimental Results

The various blocks on the fabricated chip were first tested individually to verify their functionality. In the case of the nMOS and pMOS current mirrors, this was done by applying an input current and a variety of control bit patterns to the module, and measuring the output current in each case.

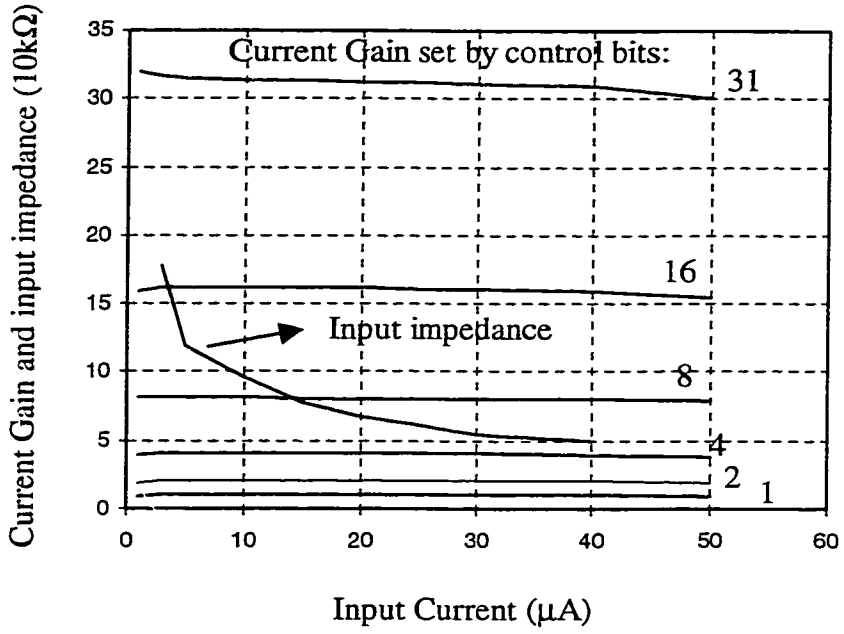


Fig. 5.7. Current gain and input impedance for the nMOS programmable current mirror.

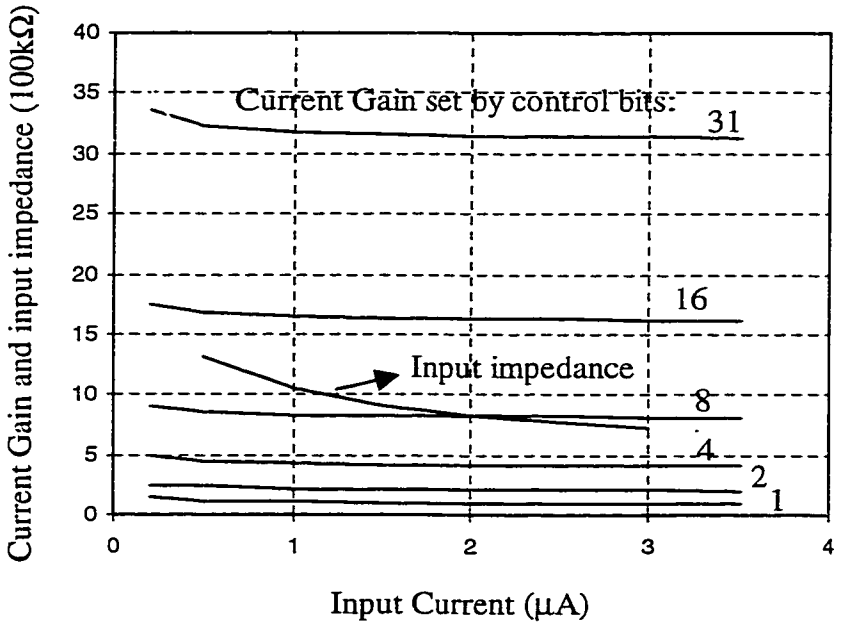


Fig. 5.8. Current gain and input impedance for the pMOS programmable current mirror.

The input impedance of the modules was also measured. Fig. 5.7 shows the results of these measurements for the nMOS programmable mirror as a function of the input current and for several values of the set gain. It is seen that when the input current is more than several μA's, the gain settles to its expected value and remains fairly constant until saturation effects start to lower the gain at high input currents.

The same experimental results for the pMOS programmable mirror are shown in Fig. 5.8. These figures also show the input impedance of the modules, which is higher for the pMOS circuit. In fact, the high input impedance limits the input current to about 3.5μA for the pMOS module because drawing more current requires an input voltage of more than 5V.

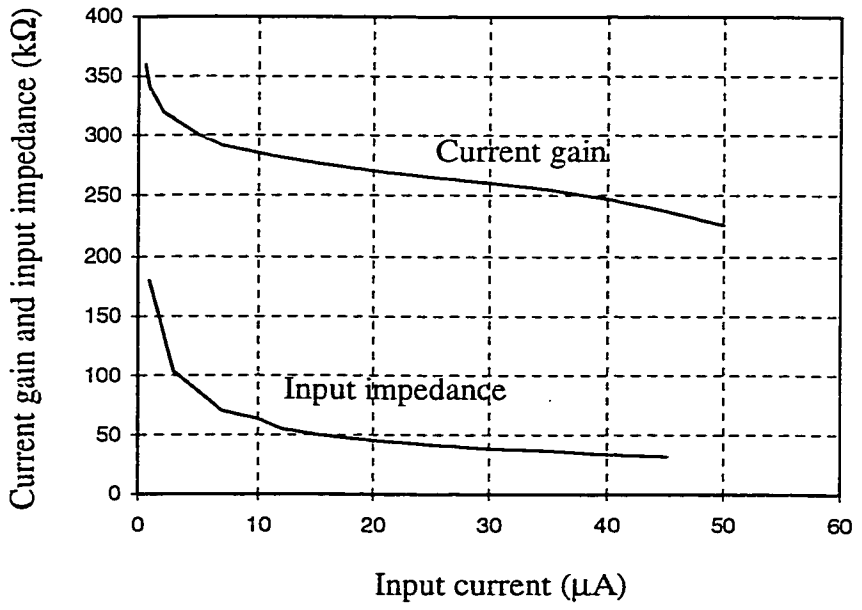


Fig. 5.9. Measured current gain and input impedance for the emitter driver.

The current gain profile and the input impedance of the emitter driver is shown in Fig. 5.9. From the figure it can be seen that the gain here is more nonlinear and varies from around 350 at low input currents to about 220 for high input currents. The fact that the measured gain is higher from the expected value of approximately 170 can be attributed to the sensitivity of the gain to the size of the input transistor in this circuit (M_1 in Fig. 5.5) which is by far smaller than the other three transistors.

Experimental results for the signed current mirror are shown in Fig. 5.10. As mentioned in Sec. 5.3, the signed current mirror must have a gain of 1 or -1 depending on the logical levels applied to its two digital inputs. Figure 5.10 shows the measured gain of this block for the two cases where the nMOS half of the output is active (a = b = 1) and when the pMOS half of the output is active (a = b = V_{dd}).

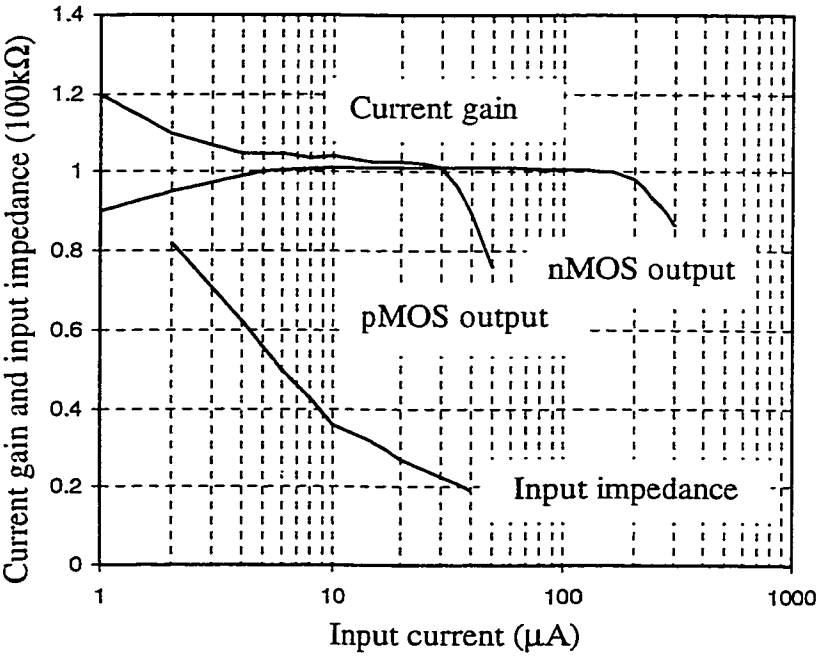


Fig. 5.10. Gain and input impedance measurements for the signed current mirror.

The point to be noticed between the two cases is that when the pMOS half of the output is active, the input current is limited to about 40μA before the output starts to saturate. However, when the nMOS half of the output is active the saturation occurs at much higher input currents (above 200μA). This means that with the given transistor sizes, this circuit can sink more current than it can source. This limitation is due to the high input impedance of the pMOS half of the circuit M4 (Fig. 5.3), which causes transistor M2 to go out of saturation at low current levels.

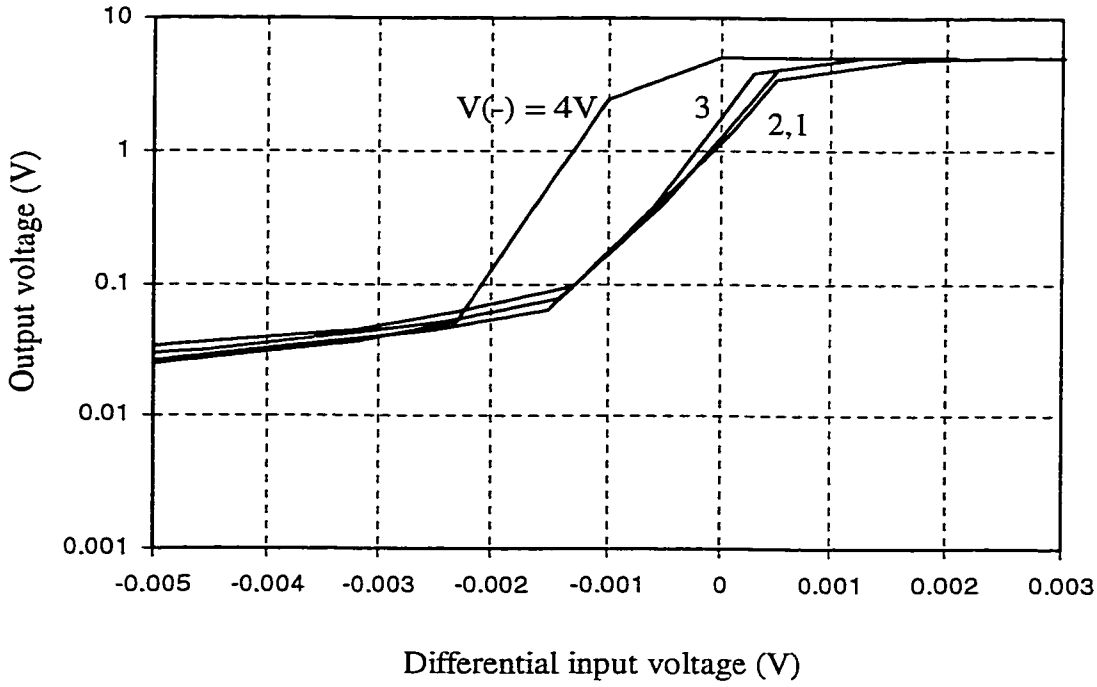


Fig. 5.11. Output voltage of opamp versus differential input voltage.

Experimental gain results for the opamp are shown in Fig. 5.11. These results depict the open loop gain of the opamp as a function of the differential input voltage ($V_+ - V_-$) for four values of V_- of 1, 2, 3, and 4V.

These results verify the functionality of the opamp, with a maximum open-loop gain of more than 5000, allowing it to perform reasonably well in closed loop configurations.

5.8. Experimental Results with VCSEL's and MSM's

Up until now the functionality of the implemented blocks has been verified individually. In this section the functionality of these blocks together with the VCSEL-MSM array is demonstrated.

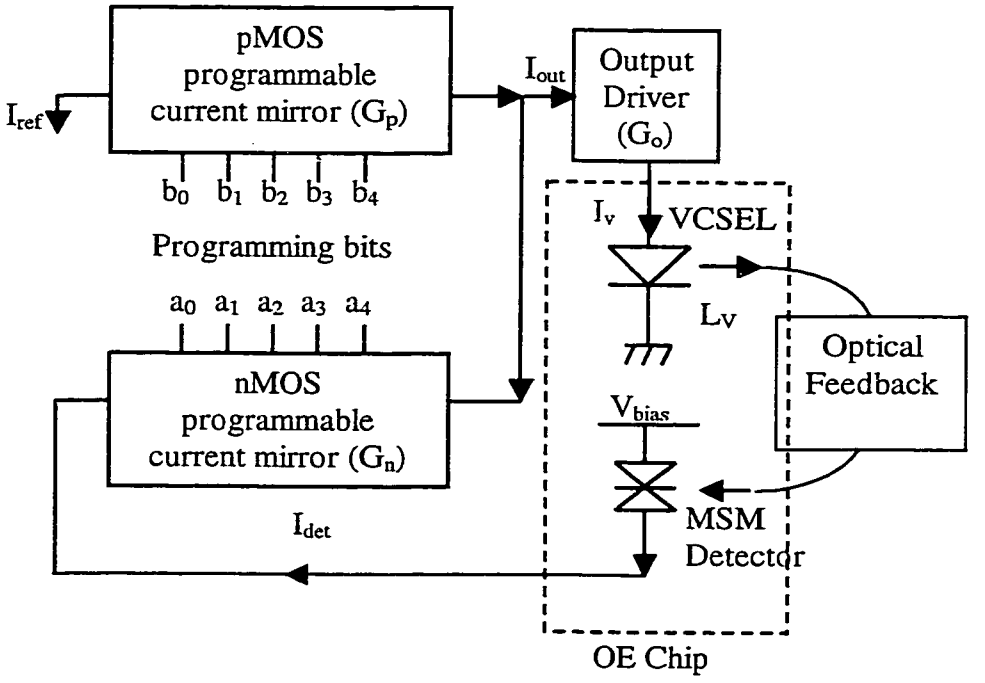


Fig. 5.12. Schematic diagram of the CMOS circuit and the OE chip.

Fig. 5.12 shows a sample demonstration circuit that utilizes three modules to achieve closed loop feedback behavior for a VCSEL-MSM pair. The pMOS and nMOS programmable current mirrors have the same structure as those shown in Figs. 5.2 and 5.1.

The pMOS current mirror is fed with an input current I_{ref} and the nMOS current mirror is connected to an MSM detector. The output currents of the current mirrors are subtracted at the output node, and the result I_{out} is fed to the output VCSEL driver:

$$I_{out} = G_p I_{in} - G_n I_{det} \qquad (5.2)$$

where I_{det} is the feedback current from the MSM detector.

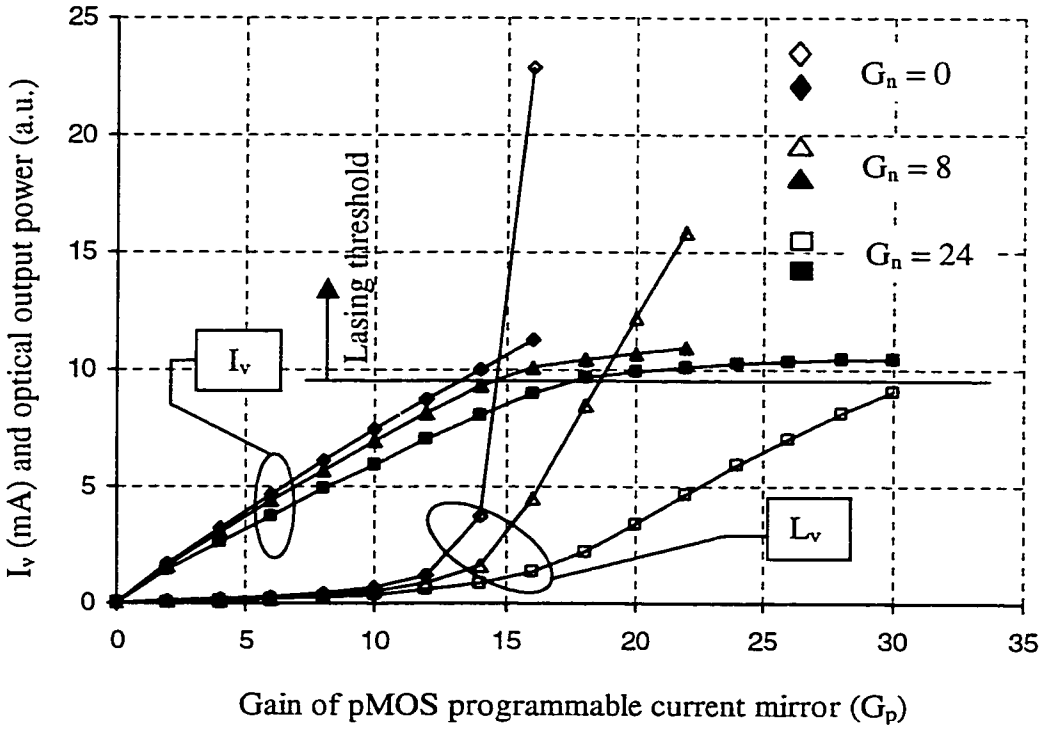


Fig. 5.13. VCSEL current I_v and optical output L_v versus pMOS module gain G_p.

The VCSEL current $I_v = G_o I_{out}$ is set by output driver's gain G_o (Fig. 5.9), providing a drive current of about 10mA for the VCSEL.

A portion of VCSEL's output L_v is fed back to the MSM detector through an optical feedback scheme. This optical feedback in the simplest case can be a partially reflecting surface, however, various configurations for SPSI applications are conceivable as well. Experimental results from this setup are shown in Fig. 5.13. The curves with solid markers are the VCSEL's optical output power and the curves with unfilled markers are the corresponding VCSEL current I_v. The independent variable is the gain of the pMOS stage G_p, which was varied from 0-30, using the control bit pattern $[b_4b_3b_2b_1b_0]$. The reference current was kept constant at $I_{ref} = 2.8\mu A$. The three pairs of curves correspond to gain values for the nMOS stage, G_n, of 0, 8, and 25.

The first case, where G_n is zero, corresponds to no feedback. In this case the VCSEL's driving current varies linearly with G_p as expected. This demonstrates the functionality of the pMOS block, where the input reference current is amplified by the amount set by the control word $[b_4\text{-}b_0]$. In this experiment G_p was not increased any further to prevent damage to VCSEL's. The corresponding VCSEL optical output curve shows the onset of lasing at a threshold current of about 10mA. For comparison the threshold current is also shown as a horizontal line across the figure. The second pair of curves corresponds to $G_n = 8$, or medium feedback. The effect of feedback can be seen by noticing that below lasing threshold the current is linearly increasing with G_p, while above threshold the current bends down because of the negative feedback from laser output. The corresponding L_v curve is also smoother compared to the case of no feedback, demonstrating the linearizing effects of feedback. The third pair of curves corresponds to $G_n = 24$, or strong feedback. Here the effects of feedback are more clear: the driving current above lasing threshold is decreased further and the corresponding optical output L_v is more controlled and linear. These results demonstrate the functionality of the

programmable current mirrors and their output connectivity, as well as capability of modules to drive VCSEL's and process the currents from MSM detectors.

5.9. Summary

In this chapter the design and experimental results for several current mode circuit blocks were presented. These blocks, consisting of an opamp and several current-mirror-based modules, are able to mix analog and digital processing capabilities and are suitable for interfacing with OE arrays of emitters and detectors. Experimental results from a CMOS demonstration chip with a VCSEL-MSM pair were also presented. These results verified the individual functionality of the modules as well as their ability to work together and with the VCSEL-MSM pair in an example of negative optoelectronic feedback. The simplicity and compactness of these circuits makes them suitable for OE array interfacing and processing applications. In the next chapter these blocks are utilized in a more general current mode processing architecture with additional digital control and storage capabilities.

Chapter 6. General Mixed-Mode ASIC Architecture for Current Mode Processing

In the previous chapter the design and implementation of several current processing modules for interfacing with OE arrays were discussed. In this chapter these blocks are incorporated into a general mixed mode architecture, resulting in a novel approach to the design of application specific integrated circuits (ASIC's) for interfacing with OE arrays. Such ASIC architectures have attracted much attention and have become an important platform for interfacing with optoelectronic devices [75-77].

6.1. OE Array interfacing requirements

Modern OE arrays may include many optical sources and detectors on a single chip. An interface circuit, such as an ASIC chip, designed to drive such OE arrays has to meet specific challenges. An obvious requirement is the ability to drive the optical sources individually. This means that an ASIC interface should be able to individually address as well as provide sufficient current for emitters on an OE array. An interface ASIC chip should also have on-chip current processing capabilities. Early on-chip processing (whenever possible) has many advantages in terms of speed, parallel processing, signal conditioning, and reducing the computational load for external circuits. Some of the most common forms of signal processing are addition, subtraction, and amplification (gain) of signals. There also needs to be sufficient digital logic and control circuitry on chip. These digital circuits can be exploited for storing data, performing logic operations, or controlling various aspects of other circuits. Finally, the issue of scalability has to be considered. If an OE array interface ASIC chip is designed for a certain array size, it should be easy to connect several such ASIC's together to form larger systems, should the need arise for interfacing with larger OE arrays.

Fig. 6.1. illustrates a system level diagram of an architecture for interfacing with OE arrays. Several approaches to the implementation of such an architecture could be envisaged. The approach presented here is based on the current mode modules discussed in the previous chapter.

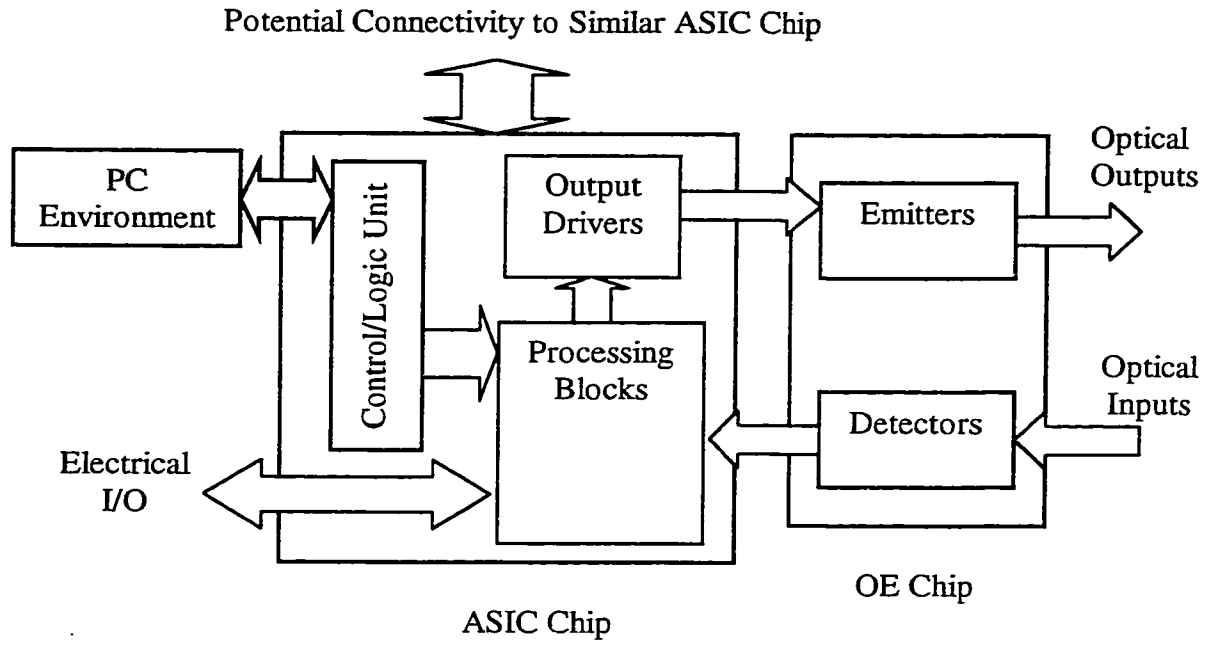


Fig. 6.1. System level diagram for OE array interface architecture.

The programmable current mirror circuits are suitable candidates for the "processing blocks" box of Fig. 6.1. Their gain, output polarity, and output impedance (high-impedance versus current source) can be controlled by their control bits. They can also implement signal addition and subtraction by means of their output polarity. The emitter driver circuit of Sec. 5.5 can serve as the "Output Drivers" block, while the output compatibility of the modules allows them to be connected together in various topologies with their current input and output ports serving as the electrical I/O in Fig. 6.1.

Therefore, in order to realize an architecture of the type shown in Fig. 6.1, some of the circuits of Chapter 5 (with occasional modifications) along with additional logic and control circuits were used in the design of an example of an ASIC interface for the VCSEL-MSM array. The additional logic circuits were necessary to provide a serial

programming scheme for the control bits of the implemented modules. This chip was also fabricated through the MOSIS service using the AMI 1.2 process, and experimental results obtained from it are given throughout this chapter. However, the discussion first focuses on the modifications and generalizations made to the circuits of Chapter 5, along with the additional control and logic circuits used in this second CMOS implementation.

6.2. Programmable Signed Current Mirror

A natural generalization of the signed current mirror and the programmable current mirror discussed in the previous chapter is to combine them into a single block. The resulting module thus has gain control abilities and can act both as a current source and a current sink.

It is also possible to address some of the shortcomings of the signed current mirror by introducing additional logical circuits in the module. From Fig. 5.3, it can be seen that a pMOS and an nMOS stage with control switching transistors have four possible states: high-impedance, current source, current sink, and dc-path from V_{dd} to GND. Of these four states, the last one is undesirable and should be avoided. The first state is useful, but it can alternatively be achieved by setting the gain of the stage to zero. The remaining two states then can be controlled by a single bit, a "sign bit", which determines whether the module is a current source or a current sink. A simple logic circuit can therefore take the single sign bit as its input and produce at its output the necessary logic levels for the nMOS and pMOS stages. The advantage of this approach is that the case where both pMOS and nMOS outputs are on can automatically be avoided because it is not allowed to happen by the logic control circuit. The schematic diagram of the module along with the logic control circuit is shown in Fig. 6.2. For simplicity, the logic control circuit is only shown for the least significant bit. The actual circuit has the same logic control for all bits, with a common sign bit. The sizes used in the actual layout are W1/L1=3.6/15.6 and W2/L2=3.6/18 (μm).

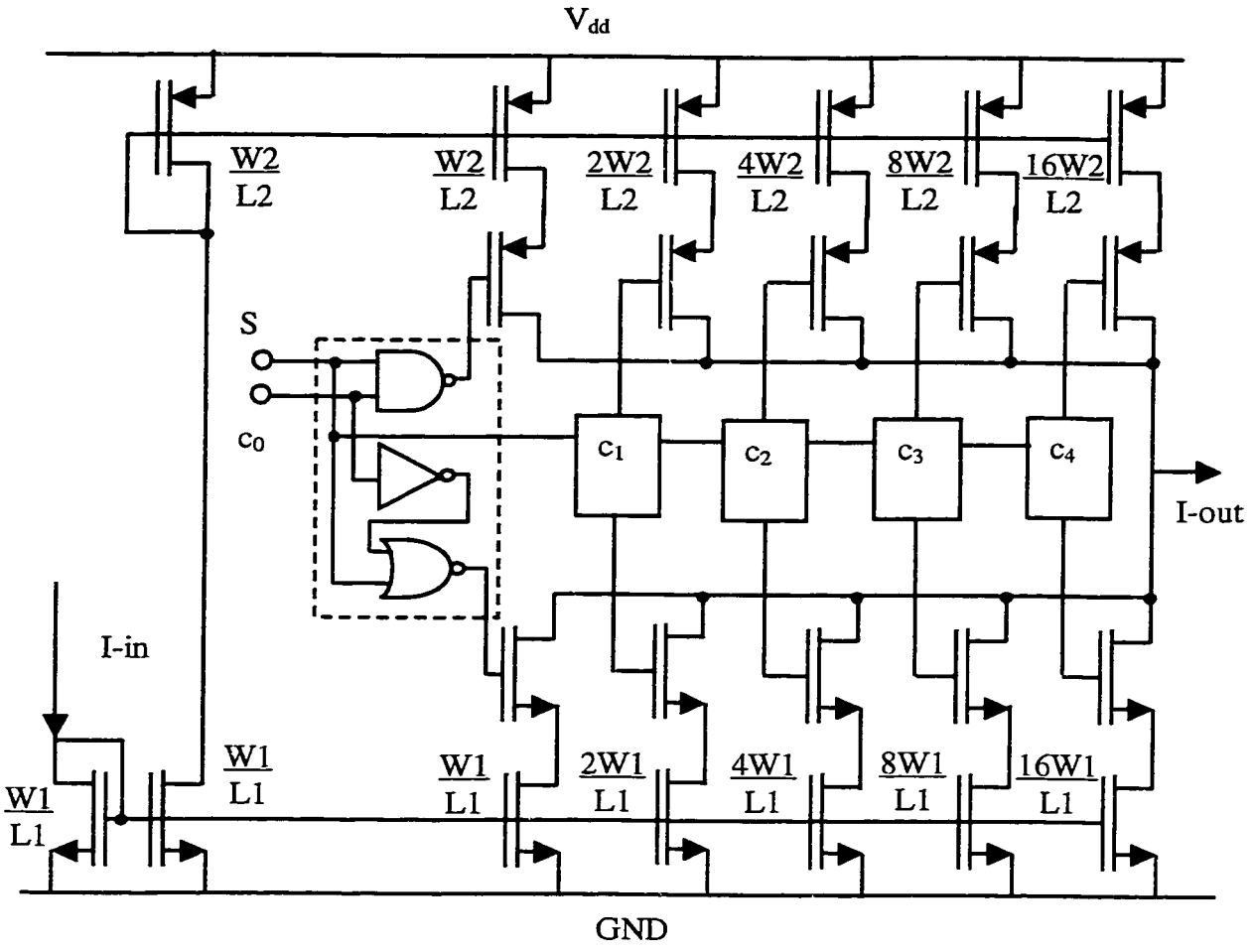


Fig. 6.2. Programmable signed current mirror.

With this design, a simple logic level at the sign bit determines whether the stage is a current source or a current sink. The output of the module can thus be written as:

$I_{out} = g(c_0 + 2c_1 + 4c_2 + 8c_3 + 16c_4)\, I_{in}$. $g = 1$ if $S = V_{dd}$, $g = -1$ if $S = 0$ (6.1)

If a high-impedance output is needed, the 5 gain control bits can be set to zero which causes the current mirror transistors in both nMOS and pMOS stages to turn off. The addition of the sign bit effectively makes this a 6-bit DAC.

6.3. Modified Emitter Driver and pMOS programmable current mirror

A second implementation of the emitter driver was included in the second CMOS chip. The only difference between the two versions was the addition of two current copiers in the latter implementation. The reason for this addition was the need to duplicate the input current to the emitter driver without any amplification for interconnecting various driver modules. This issue will be elaborated further in the last section of this chapter where the systematic interconnection of these blocks in an ASIC architecture will be discussed. For the time being, however, consider the schematic diagram of the modified emitter driver as shown in Fig. 6.3.

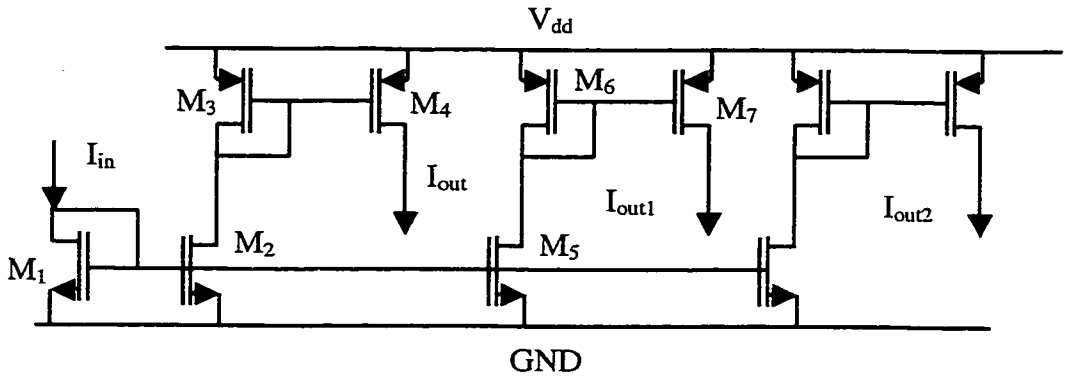


Fig. 6.3. Modified emitter driver.

The left side of the circuit is identical to that of Fig. 5.4. In addition, two current copying stages are added. The only difference between these additional stages and the original stage is that the gain of these additional stages is unity, i.e., $I_{in} = I_{out1}=I_{out2}$. This can easily be achieved by setting the size of M_5 identical to M_1 and the size of M_7 identical to M_6. If additional copies of the input current are needed, additional stages just like those shown can easily be added.

The pMOS programmable current mirror was also slightly modified in the second CMOS implementation. It was seen in Chapter 5 that the input impedance of this module was quite high, so much so that the input current was limited to about 3μA. To remedy this situation, the pMOS programmable current mirror was made narrower in the second CMOS chip with an L = 28.2μm (from L = 42.6μm). As will be seen later in this chapter, this causes a proportional reduction in the input impedance of the module and thus allows for a wider range of current inputs.

6.4. Additional Digital Circuitry: Inverter, buffer, and D Flipflops

The circuits discussed so far have many control inputs. These control inputs accept logic level voltages and determine the gain and/or the polarity of modules. If many of these modules are present on an ASIC chip, the number of required I/O pins on the chip for these control bits would soon grow unreasonably large. To reduce the number of required I/O pins, a serial input data port can be used (Fig. 6.4). The required pattern of logic levels for all the control bits can then sequentially be input through a single pin and stored within the chip in a "programming phase". Once all the control bits have the desired logic levels present at their inputs, the chip can enter its actual "operation phase". Internally, a chain of D-flipflops connected in series and forming a shift-register can be used to store the necessary logic values. The data is fed to the chain from one side and clocked through the chain. After the right number of clock cycles, the correct pattern of logic levels is present along the shift-register chain. Then a "load" signal can transfer these logic levels to the gates of the transistors within the blocks.

The clock signal is first passed through a buffer B with enough drive capability for the whole chain. In reality the buffer produces out-of-phase copies of the clock signal, because the D-flipflops require both polarities of the clock. It is also a good practice to consider clock distribution techniques. For example feeding the clock signal from the

middle of the chain helps minimize the clock delay difference to the flip-flops at either end of the chain.

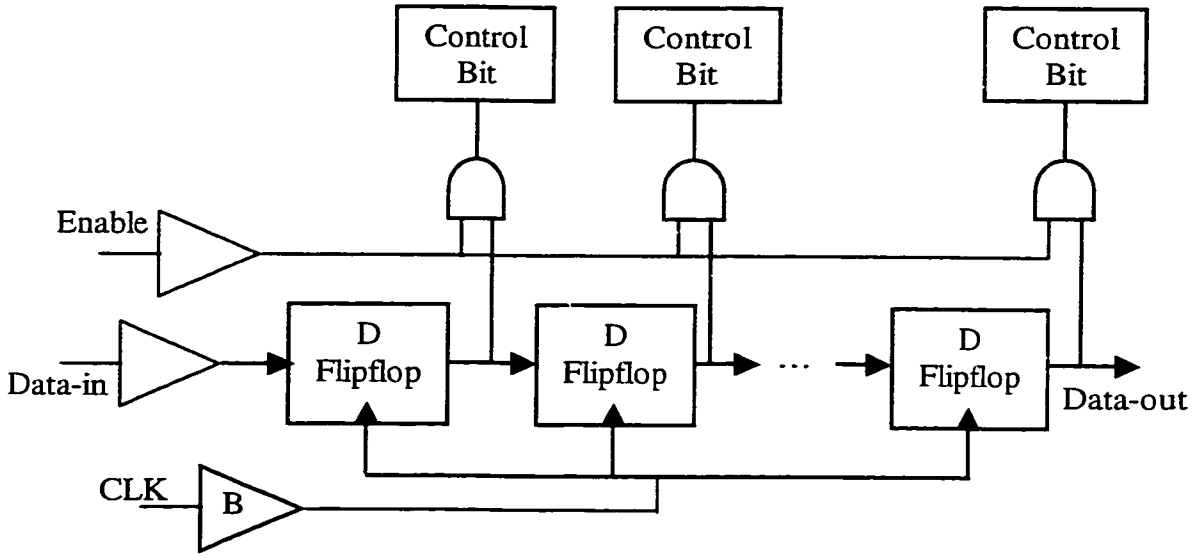


Fig. 6.4. Serial data feed chain.

The input data, after passing through the chain of the flip-flops, is brought off-chip for test purposes or for connecting to the data input of another ASIC chip when multiple chips are to be used. The outputs of the flip-flops are passed through AND gates before being applied to the control bits of current processing modules. Another "enable" signal is applied to the AND gates as well, making it possible to keep the outputs of the AND gates at a logic zero during the programming phase and passing the correct data at the proper time during the operation phase. The enable signal can also be used to over-write all data present in the chain and shut down the circuits in an emergency situation. The D-flip-flops used in the chain were obtained by connecting two latches in series and feeding each latch with an opposite polarity of the clock signal. The schematic diagram of a D-flip-flop is shown in Fig. 6.5.

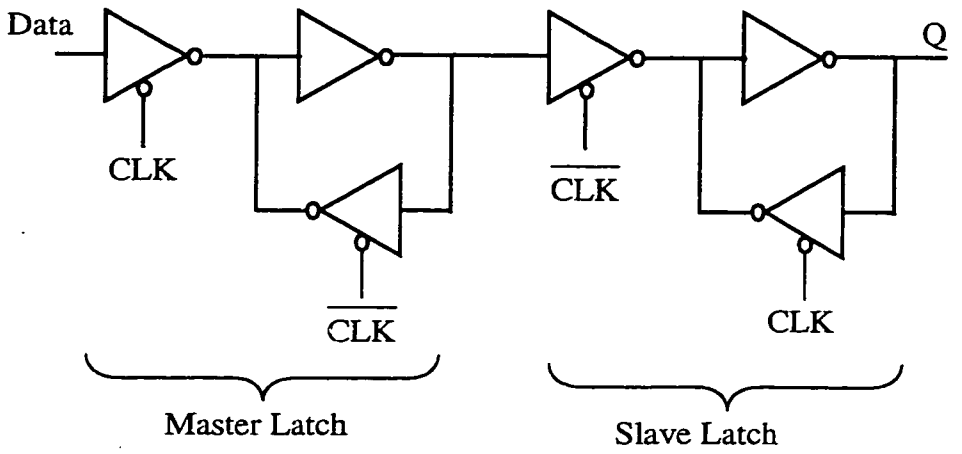


Fig. 6.5. Schematic of D-flipflop.

Having a master-slave configuration ensures that the flip-flop changes state only on the edges of the clock, and this makes the operation of the circuit more reliable compared to when only simple latches are used.

6.5. Implementation of a Mixed Mode Architecture

As mentioned in the beginning of this chapter, the current mode blocks and control/logic circuits were used in a sample ASIC CMOS architecture. Obviously the choices of blocks, their implementations, and details of the architecture were not unique, although the goal of interfacing with the VCSEL-MSM array did provide certain design guide-lines. Despite the fact that the main purpose of the project was to provide a platform for SPSI applications, there was not enough design data for any specific SPSI application to be used as a major guide in the design process. Therefore a general approach was opted for, so that a maximum number of possible applications can benefit from the resulting ASIC chip. The particular choices made in the layout of this ASIC chip were therefore

the result of several considerations and tradeoffs between flexibility and generality on one side, and complexity, die area, and pad number limitations on the other side.

Following several SPSI applications discussed in Chapter 2, it was decided that the ability to control the current for each emitter independently through an electrical input (from outside circuits) and an optical input (from the same emitter or a different emitter on the array) both in closed loop and open loop configurations was of primary importance. Moreover, each pixel needed to be able to receive inputs from its neighboring pixels and at the same time send its output to them. The approach used in the experimental CMOS ASIC chip is shown in Fig. 6.6. Again it should be emphasized that the choices are not unique, and other configurations are possible depending on, among other factors, the specific application, desired complexity, die area, and number of pads available on chip.

Due to area limitations, a pMOS, an nMOS, and a signed programmable current mirror were fabricated for each pixel. Their control bits are connected to the shift register chain as explained in Sec. 6.4. The main current processing takes place at the node shared between the outputs of the current mirrors and the input of the output driver module (as indicated in the figure). According to Kirchhoff's current law the currents entering this node should be equal to the currents leaving it. In this figure, the directions of the arrows illustrate the direction of current flow. It is clear from the figure that

$$I = I_1 - I_2 + S.I_3 \quad (S = \pm 1) \tag{6.2}$$

and

$$I_a = I_b = I. \tag{6.3}$$

Equation 6.3 is the result of the internal design of the output driver (see discussion on modified output driver in Sec. 6.3). Here the factor S is a function of the sign bit and determines whether I_3 is added to or subtracted from the node. The gain control bits at each module determine the weight of the particular signal connected to the input of that block:

$$I = G_p I_{in} - G_n I_{det} + S\, G_s I_{a\text{-}adj} \quad (6.4)$$

where $I_{a\text{-}adj}$ represents a current from an adjacent pixel. This expression implements the feedback concepts discussed in Chapter 2 and also allows for interconnection of adjacent pixels.

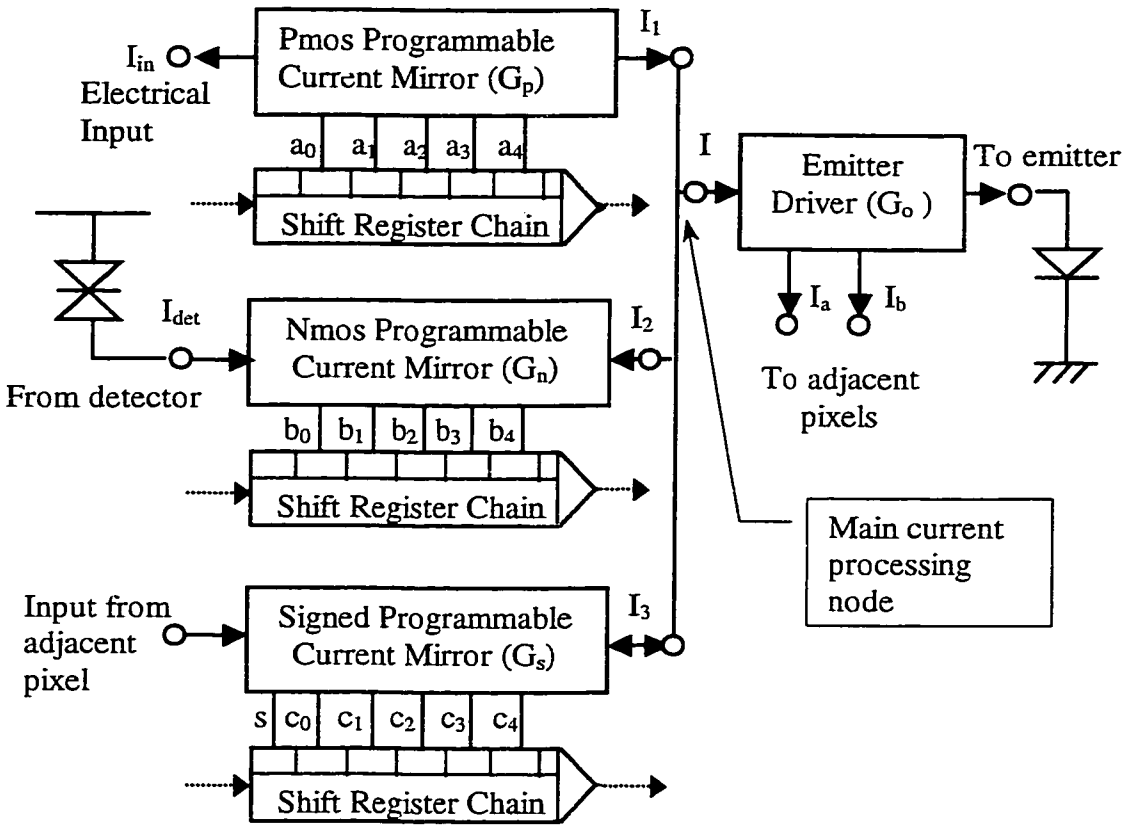


Fig. 6.6. General architecture for a single pixel.

The diagram shown in Fig. 6.6. has a certain level of flexibility to it because the current inputs and outputs of all the blocks are brought off-chip. The circles shown in Fig. 6.6 at the inputs and outputs of each block represent a pad on the die and a pin on the package. This makes it possible to arrange them in different topologies by hard-wiring them off-chip, or if needed, use more than three blocks per pixel by borrowing blocks from other pixels. In this design, each ASIC chip has three such configurations with wired inputs and outputs. A forth configuration is also included on the die to demonstrate that a tiny chip can fit four of these configurations, although it was not wired because of lack of enough I/O pads on the pad-frame and pins on the package (the I/O pads were limited to 40). Figure 6.7 shows the simplified diagram of the floor-plan of the whole ASIC chip which was fabricated through MOSIS using the AMI 1.2 process. A photograph of the fabricated chip is also shown in Fig. 6.8 .

Several features of the design are illustrated in these figures. The four pixel-configurations are clearly seen (although the top one is not wired). The shift register chain is fed from one side through a buffer, and after passing by all the blocks, it is connected to an output pin. The clock signal is brought to the middle of the chip and after buffering and creating two out-of-phase copies, it feeds the register chains from both sides (not shown in the figure) for delay balancing purposes. The enable signal (which applies the logic values present in the shift registers to the modules) is also buffered first and then feeds the individual enable inputs of the shift registers in each chain. A separate pad on the frame is designated only for feeding the supply of the emitter drivers (G_o blocks) because of their high current requirements. Isolating the V_{dd} supply for VCSEL drivers also has the advantage that the VCSEL's can be powered after the circuits are set in their desired states in a wake-up mode, or shut down immediately and independent of the internal circuits in a case of emergency.

Other blocks share their V_{dd} and GND supplies. Although in mixed signal circuits it is a good practice to keep the supplies of digital and analog circuits separate, in this

architecture this is not necessary, because the two modes of the chip (programming versus operation) are never operated simultaneously.

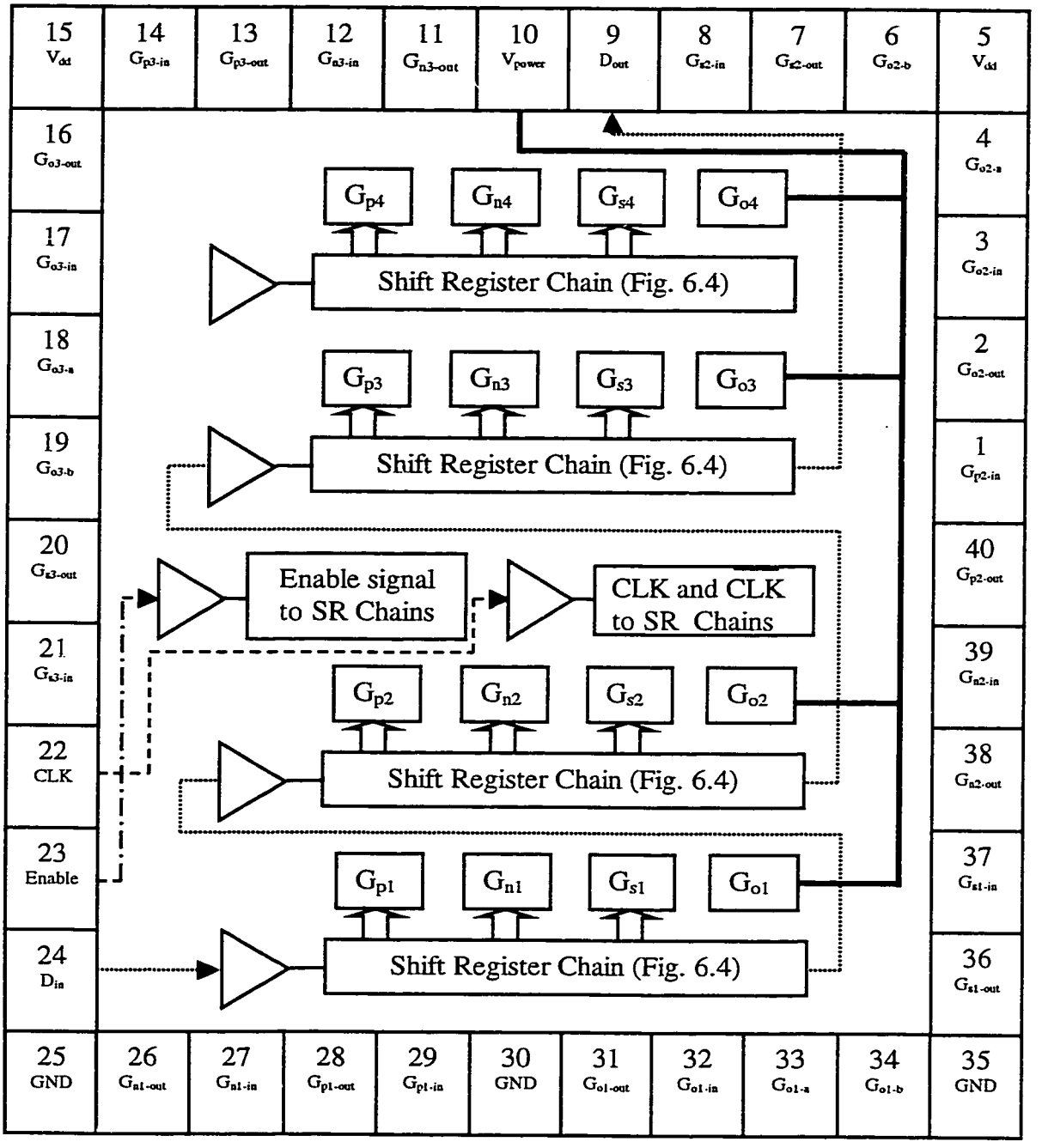


Fig. 6.7. Floor-plan of ASIC chip.

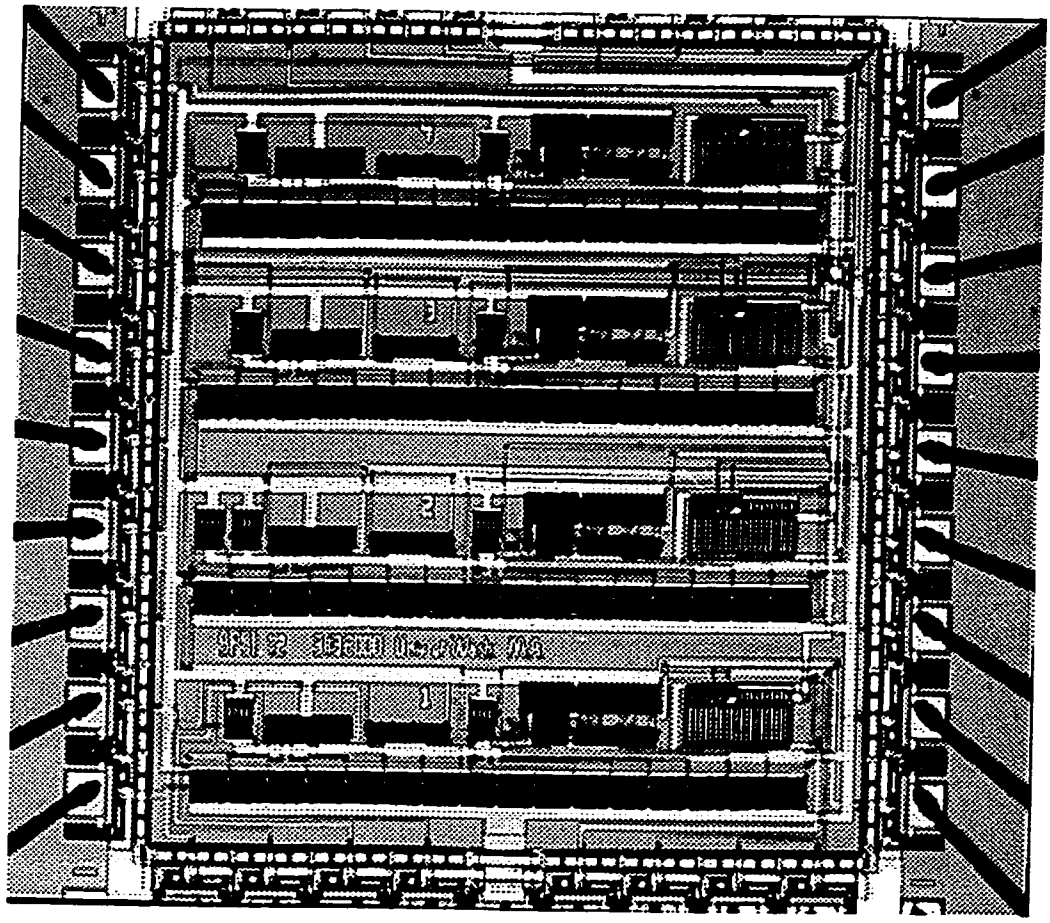


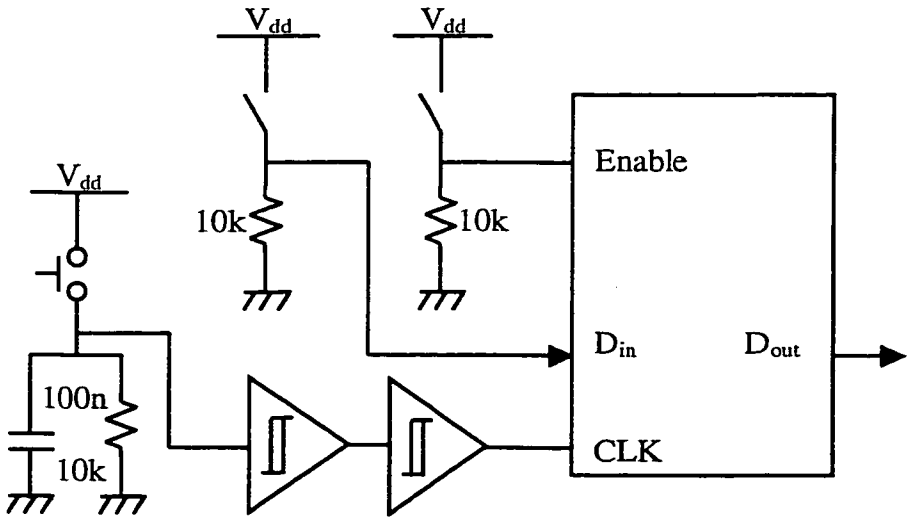
Fig. 6.8. Photograph of demonstration CMOS ASIC Chip.

Other blocks shown in the figure are G_p (programmable pMOS current mirror), G_n (programmable nMOS current mirror), and G_s (programmable signed current mirror).

The control bits for each of these modules are connected to the corresponding shift registers in the chain, whereas their inputs and outputs are brought off chip. As mentioned before, this allows for connecting these blocks in various configurations. If the configuration of Fig. 6.6 is used, each AISC chip can drive three pixels on the VCSEL-MSM array. Thus if the whole array is to be driven, a total of 6 AISC chips are required. This is a rather high number, but if a larger pad-frame is used and if a specific application is to be implemented so that not all inputs and outputs are needed off-chip, a single ASIC is sufficient for the whole VCSEL-MSM array. Finally it should be noted that this architecture is easily scalable, ie., several such ASIC's can be connected together by connecting D_{out} on one chip to the D_{in} of the next chip and tying the enable and clock signals for all of them together.

6.6. Experimental Results

In this section the experimental results from the fabricated chip are presented. These results verify the functionality of the various blocks in the chip as well as the control and logic circuits within the shift register chain.



4585 (CMOS Shmitt trigger buffer)

Fig. 6.9. Manual clock generation for the ASIC chip.

Because of the design of the chip, it was important to set-up a correct manual clocking scheme to test the functionality of the shift-register chain. Several de-bouncing circuits were tested but were not found to perform satisfactorily. Finally the circuit shown in Fig. 6.9 was used, and was found to correctly produce the clock signal for the chip, in that a pulse present at D_{in} appeared at D_{out} exactly after 48 clock cycles (the number of shift registers in the chain). Once the functionality of the logic control circuits was established, each of the individual blocks was tested by measuring the current gain of the module as a function of its input current for programmed gain values of 1,2,4,8,16, and 31. These results make it easy to compare the programmed gain and the actual gain for different values of input current.

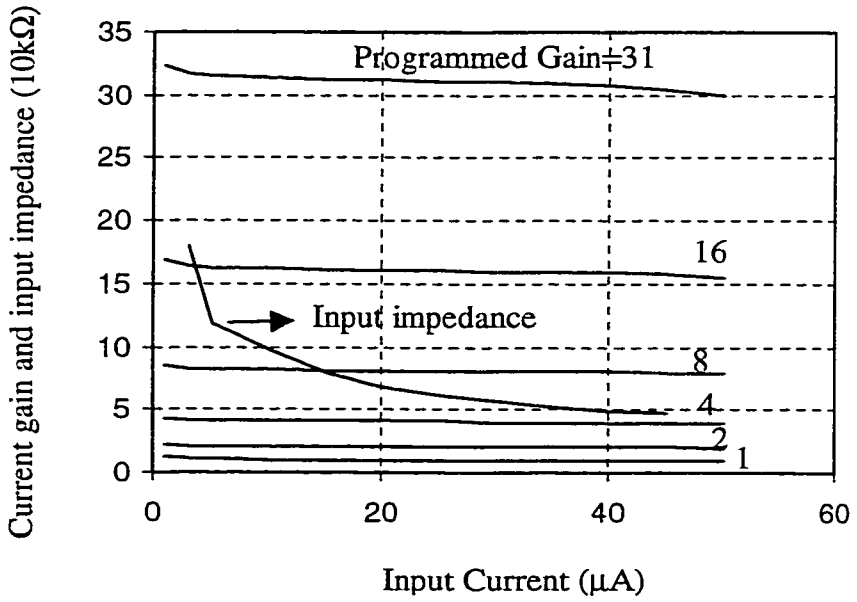


Fig. 6.10. Current gain and input impedance for nMOS programmable current mirror.

Figure 6.10 shows these results for the nMOS programmable current mirror. Also shown is the small signal input impedance of the circuit. As can be seen from the figure the actual gain is generally close to the programmed gain, with only a slight slope as the input current increases. The input impedance starts at around 180kΩ for low input currents, but then decreases to about 50kΩ. Similar results for the pMOS programmable current mirror are shown in Fig. 6.11.

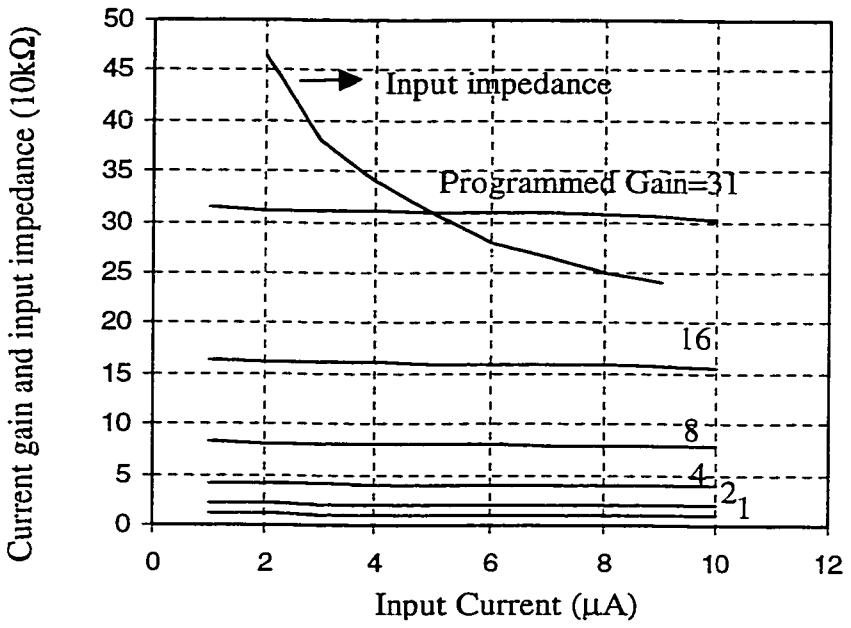


Fig. 6.11. Current gain for pMOS programmable current mirror.

Again a reasonable agreement is seen between the programmed and the actual gains. The noticeable difference between the nMOS and pMOS modules is the higher input impedance of the latter.

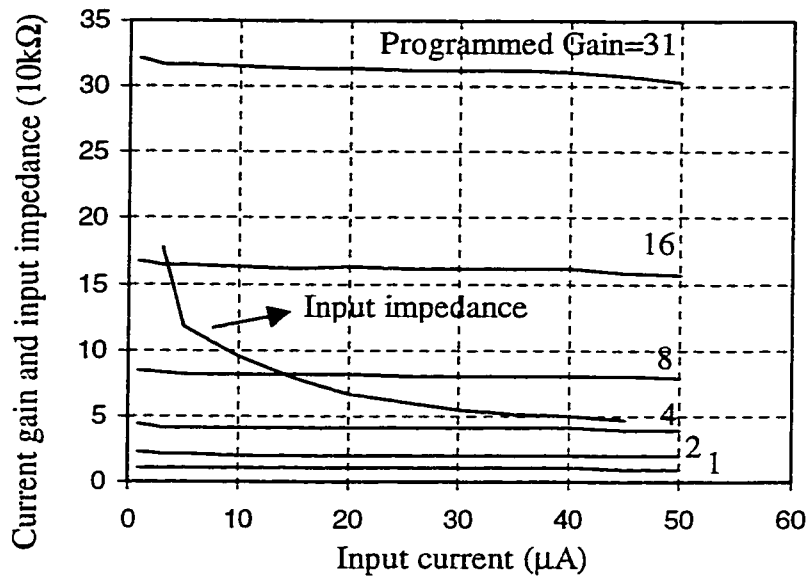


Fig. 6.12. Signed programmable current mirror, nMOS output current gain.

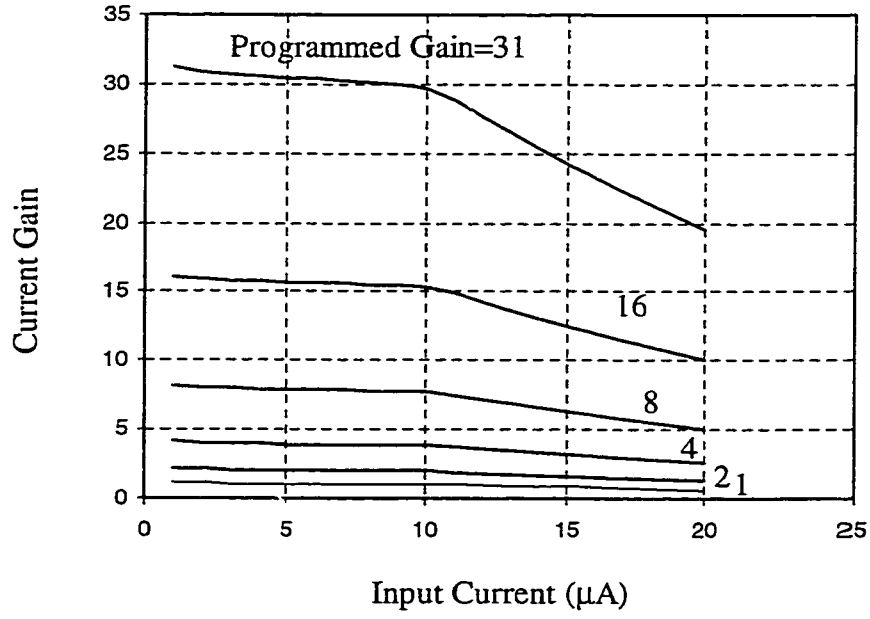


Fig. 6.13. Signed programmable current mirror, pMOS output current gain.

This accounts for the smaller range of the input currents (10μA versus 50μA), because drawing more current from the pMOS module required more than 5V of potential difference applied to the input of the pMOS module.

The signed current mirror was tested in two cases, once with the sign bit being zero, which resulted in the activation of the nMOS half of the output stage, and once with the sign bit being 1 which resulted in the activation of the pMOS half of the output stage. The results from these two cases as well as the input impedance of the module are shown in Figs. 6.12 and 6.13. From these figures it can be seen that the module functions correctly in both modes which verifies the functionality of both the current mirror structures and the logic circuits for selecting the pMOS or nMOS outputs. However, the point to notice in Fig. 6.13 is that the output curves demonstrate an increased slope for inputs above 10μA. This is because of the high input impedance of the pMOS stage: a potential difference of more than 5V is required to draw more than 10μA, a voltage difference that the input stage cannot deliver.

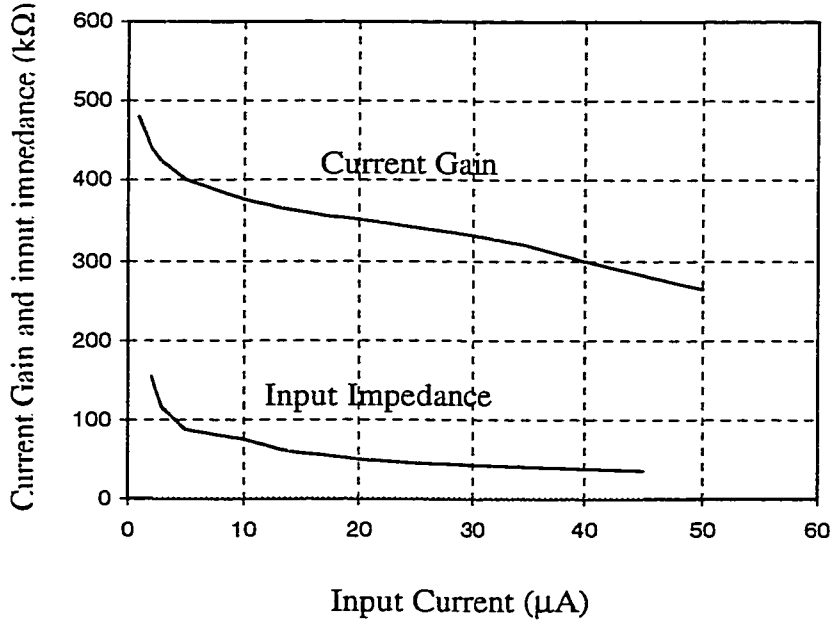


Fig. 6.14. Current gain and input impedance for emitter driver.

As mentioned earlier, two circuits were implemented in the emitter driver in the ASIC chip. One section was the power driver for the VCSEL's, and the second section included two current copies. The current gain and the small signal input impedance of the output driver module are shown in Fig. 6.14 as functions of the input current.

The current gain characteristics of the two current copies were virtually identical and shown in Fig. 6.15. As mentioned earlier, these current copiers can be used to replicate the input current to the emitter driver for use as inputs to other modules.

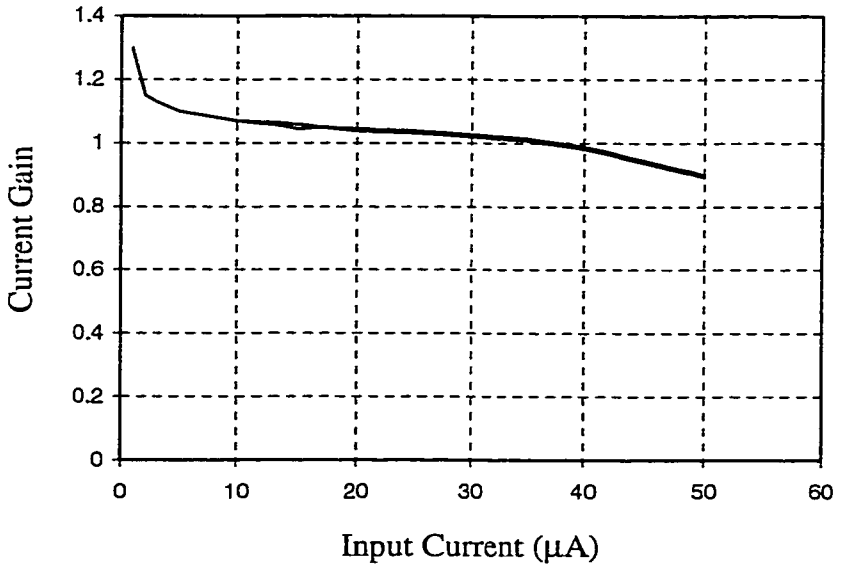


Fig. 6.15. Current gain of the current copiers.

These results complete the verification of the functionality of the individual modules and the control and logical circuits implemented in the ASIC chip. In the next section the

ASIC chip is used in conjunction with the VCSEL-MSM array to demonstrate the functionality of the ASIC chip as an interface architecture for OE arrays.

6.7. Demonstration of an Optoeletronic Flip-flop Implementation

In this section the application of the ASIC chip in the implementation of an optoelectronic flip-flop is presented. In so doing, positive feedback along with the nonlinear characteristic of the VCSEL's are employed to achieve bistability. The theory involved in the operation of the system was previously discussed in Sec. 4.5 and is not repeated in this section. Here, however, the emphasis is on the use of the current modules to implement the set and reset functions of the flip-flop, demonstrating the applicability and flexibility of the discussed architecture in implementing various optoelectronic functionalities. In addition, a new functionality involving a hysteresis loop with the optical feedback as input is demonstrated. This is a novel SPSI application which is based on positive feedback instead of the previous applications that were based on negative feedback.

In order to implement a flip-flop, a variation of the architecture shown in Fig. 6.6 is used as depicted in Fig. 6.16. Although the shift register chain is not shown explicitly for simplicity, all the gain bits are programmed through the chain. As can be seen from the figure, the output of the VCSEL (L_v) is fed back to the MSM detector through some feedback means, represented by the factor R. This feedback is set to 0.9 for the present experiments. In reality the feedback factor is much smaller due to the optical losses throughout the path of the beams, however, this fact just results in a change in the scaling factor and is inconsequential for the purpose of the following demonstrations. The MSM detector current I_d is connected to the signed programmable current mirror. The value of the sign bit(s) determines whether the output current is added to or subtracted from the output node, corresponding to positive and negative feedback respectively.

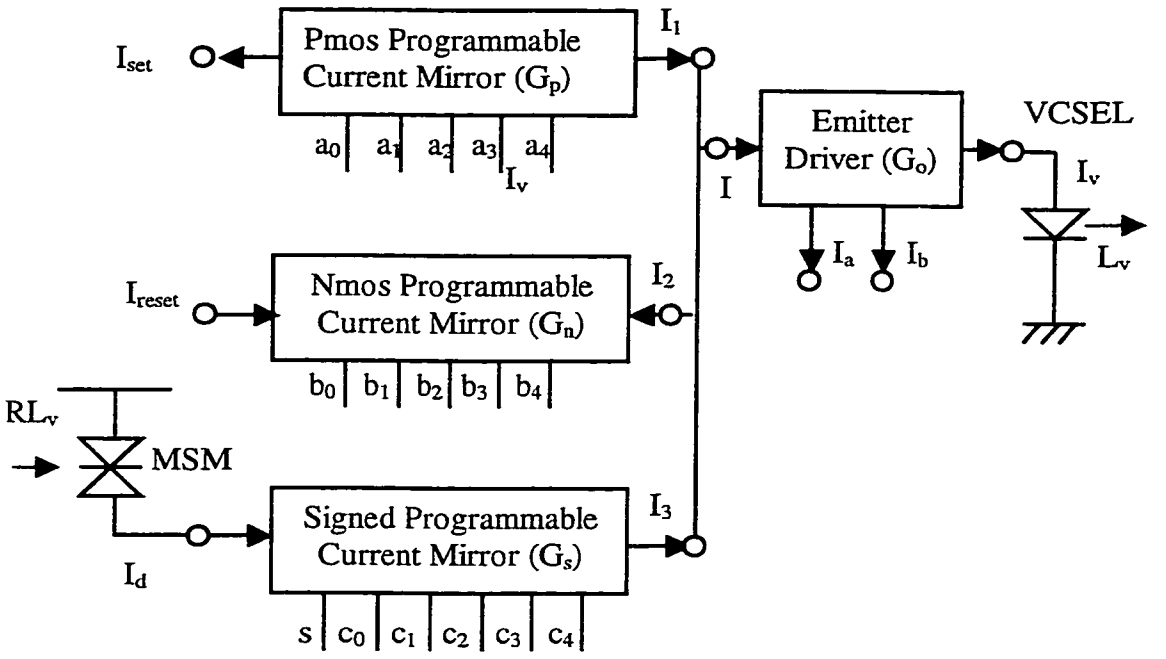


Fig. 6.16. Architecture used to implement optoelectronic flip-flop.

Here s is assigned a high logical value (s=1) to achieve positive feedback and bistability. Without considering the other two inputs (I_{set} and I_{reset}) , it can be seen that this system has two stable states: either the VCSEL is off and $I_v = L_v = I_d = 0$, or it is at its maximum allowable power, when its current is limited only by the driver circuits or possibly by the saturation effects from the VCSEL itself. The latter case can be achieved if the overall loop gain is more than unity so that the positive feedback can sustain the biasing levels. To ensure that this situation is realizable, the gain of the signed programmable current mirror was set at its maximum value of 31. The role of the other two inputs become clear now, as they can be used to toggle the system between the two states. I_{set} is applied through a pMOS mirror, thus it is added to the output node and its effect is the same as the MSM current. It can therefore be used to toggle the flipflop to its on state. On the other hand, I_{reset} is applied through an nMOS mirror and it is subtracted from the output node. So it can be used to switch the flipflop to its off state. In this demonstration the

gains of both the pMOS and nMOS mirrors were programmed at 31 to achieve maximum sensitivity to I_{set} and I_{reset}. In this experiment these inputs are supplied and controlled from outside, but they can very well be supplied from other pixels. In the same manner, the two currents I_a and I_b can be used to drive other modules on the ASIC chip. With these settings the VCSEL driving current is given by:

$$I_v = G_o\, I = G_o\,(G_s I_d + G_p I_{set} - G_n I_{reset}) \qquad (6.5)$$

where G_o , G_p , and G_n are the gains of the block and defined in the figure.

The set operation of the system using I_{set} is shown in Fig. 6.17, where both VCSEL's optical output L_v and its driving current I_v are shown as functions of I_{set}.

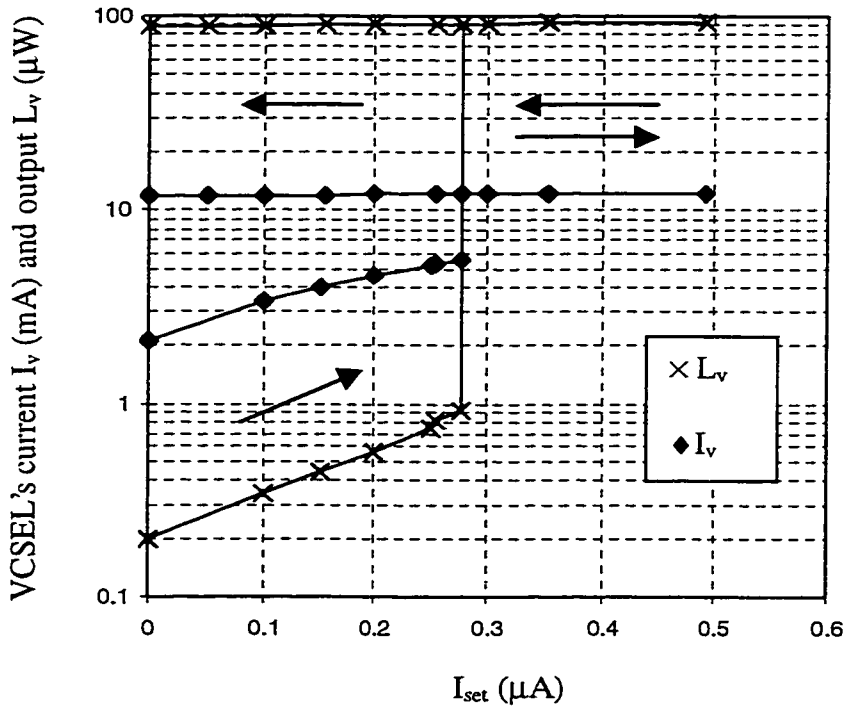


Fig. 6.17. Flipflop set operation.

When $I_{set} = 0$ the loop is only biased by the detector's leakage current which results in an I_v of about 2mA and L_v of about 200nW (the actual L_v is at least a factor of two higher because the measurement of L_v was done after the passing of VCSEL's optical output through a lens and a beam-splitter. But this results only in a proportionality factor and is inconsequential in the demonstration). As I_{set} is increased, both the drive current and optical output increase, until the flip-flop toggles its state at $I_{set} = 0.278$ μA. After that the VCSEL's current is limited by the driver to about 12mA translating to about 90 μW of optical power at VCSEL's output. After the on-state switch, decreasing I_{set} does not have any significant effect on the system as the biasing point is sustained through the positive feedback of the signed current mirror. This completes the set cycle for the flip-flop.

To reset the flip-flop, I_{reset} can be used. The reset operation is shown in Fig. 6.18.

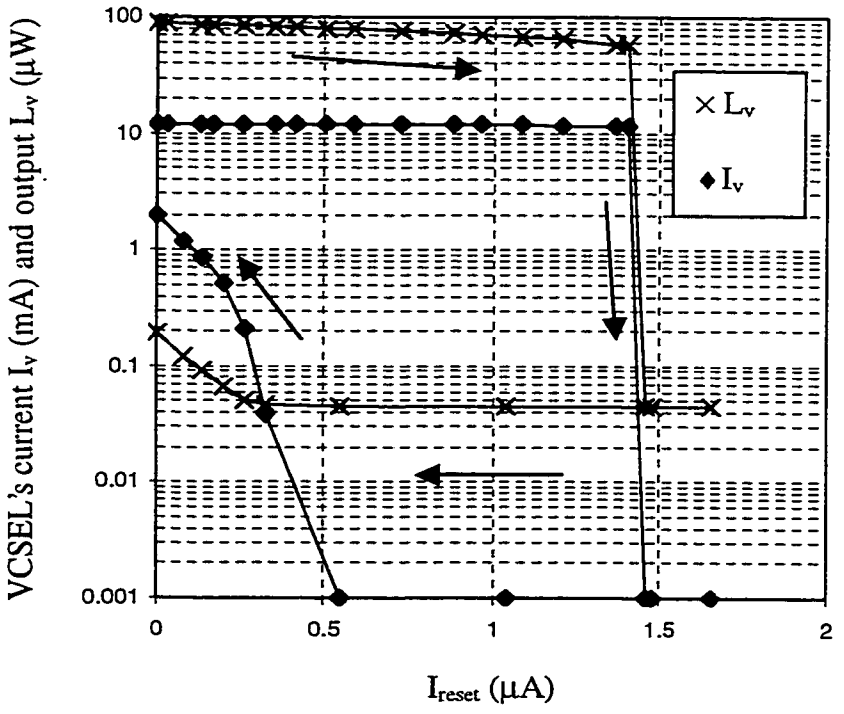


Fig. 6.18. Flip-flop reset operation.

In this case the initial state is when the VCSEL is on with I_v=12mA and L_v=88μW. Increasing I_{reset} subtracts from the output node, the result of which can be seen in the decrease in the VCSEL's optical output. The current remains approximately constant because the VCSEL is above threshold and only a slight change in current makes a large change in the output optical power. The point where the VCSEL is toggled is at I_{reset} =1.4 mA. Once the VCSEL is switched off, I_v and L_v are practically pushed down to zero. The reason is that now the small dark current of I_d is being sinked out from the output node by the rather large I_{reset}. Thus, decreasing I_{reset} does not effect the biasing point until I_{reset} is decreased down to about 0.5μA where it is now comparable with the detectors dark current. If I_{reset} is decreased further, it can no longer compensate the dark current completely and the difference (I_d - I_{reset}) starts to bring the biasing point above zero. At I_{reset} =0, only the detector's dark current biases the loop at the I_v=2mA, L_v=200nW point from which the set operation started. This completes the reset cycle of the flip-flop.

As mentioned previously, it is important to notice that the two input currents I_{set} and I_{reset} can be provided by any source. For example, they can each readily be connected to an MSM detector. In such a case both the set and reset operations can be done completely optically. Alternatively, I_{set} and I_{reset} can be controlled by the current outputs of other pixels. This flexibility is the result of the modular approach behind the architecture and underlines the power of the current mode processing techniques.

An interesting alternative mode of operation for the flip-flop is when the optical feedback R is taken as the input to the loop. Such a mode of operation suggests the SPSI sensor concepts, where the reflectivity of a scene provides the optical feedback necessary for the operation of the loop. Such SPSI concepts were discussed in Chapter 2, but they were generally based on negative feedback. However, there is no reason why positive feedback cannot be used in SPSI applications as well. In fact, if in the flip-flop discussed

above the optical feedback R is taken as input, an SPSI sensor based on positive feedback results.

Fig. 6.19 depicts a situation where the optical feedback R is taken as the independent variable of the loop and varied almost over a decade (as explained before the actual R is proportional to the R shown in the figure but this does not effect the discussion).

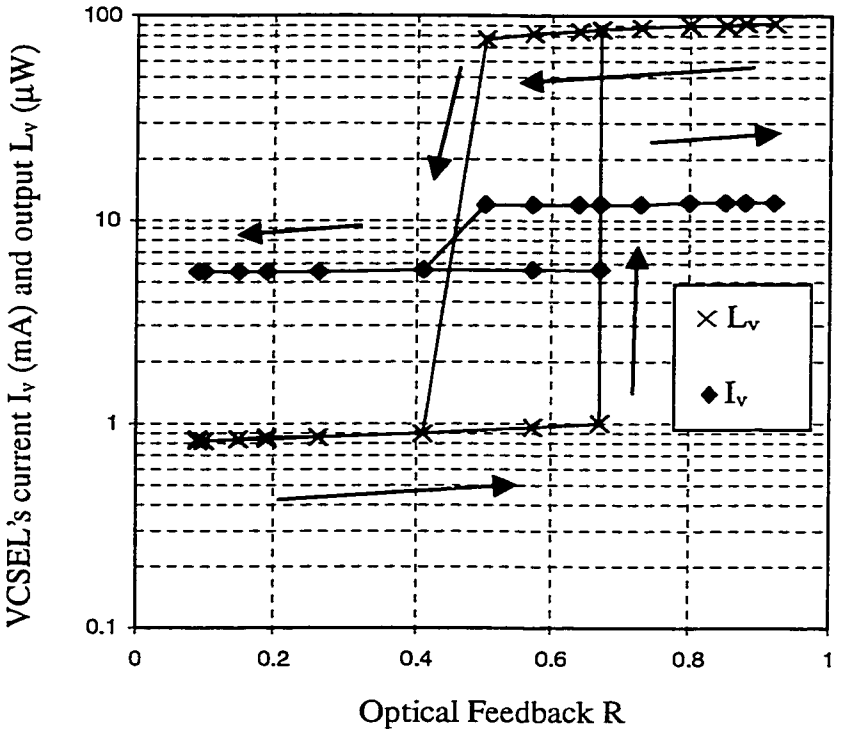


Fig. 6.19. Flip-flop with optical feedback input.

In this example the loop is initially biased by setting I_{set} to 0.300 μA, which results in I_v=5.6 mA and L_v=0.83 μW when R=0.1. Then R is increased, which causes the biasing point to also increase slightly. Nevertheless, the VCSEL is still off. At R=0.67 the VCSEL is switched on to saturation. Further increasing R beyond this point does not

significantly increase the biasing point. On the other hand once R is decreased, the curve does not exactly trace itself after a point, resulting in a hysteresis loop. It should be noted that both curves can be shifted left or right by increasing or decreasing I_{set} respectively.

The operation just discussed may be used in a variety of applications. For example it could implement an optical sensor equivalent of a Schmitt trigger. In such as sensor the variations in the reflectivity of the scene are digitized into two values represented by the two states of the VCSEL while the small "noise" in the scene is suppressed because of the hysteresis nature of the transfer function. The curves can be shifted left or right by means of I_{set} to adjust for average reflectivity changes in the scene, thus increasing the dynamic range of the sensor. Other possibilities include set-reset-type sensors, where once the reflectivity of the scene exceeds a predetermined value the pixel is set. Such sensors can find applications in optical memories and CD-ROM systems. More generally, they can be used to "latch" a change beyond a predetermined value in the reflectivity of the scene.

6.8. Summary

In this chapter a general modular current mode architecture for interfacing with OE arrays was presented. The architecture was implemented through a CMOS ASIC chip and experimental results from the chip validated the concepts. Several modules in the chip were used to drive a VCSEL-MSM pair in an optoelectronic flip-flop configuration. The experimental results demonstrated the functionality of the modules as well as the efficiency of the architecture to implement various optoelectronic functions.

Chapter 7. Critical Review, Conclusions, and Future Developments

Throughout the previous chapters a variety of topics related to SPA's and especially the SPSI concept were covered. Moreover, several issues regarding the electronic circuits, modules, and architectures required for interfacing with OE arrays were also studied. These circuits were generally implemented in CMOS (through two different AMI 1.2 runs). The underlying assumption here is that such CMOS ASIC's are critical in the development of SPA and OE technology in the foreseeable future, because not all electronic processing requirements can be fulfilled by purely GaAs technology (which is the basis of OE devices). In this chapter some general observations and conclusions are made regarding the topics discussed so far.

7.1. SPSI: A Critical Review

The concept of SPSI is a novel concept in SPA sensors with many potential applications. By controlling the source of illumination in a structured manner, it offers a variety of advantages over more traditional sensors. The SPSI concept, some of it's applications and merits, as well as experimental demonstrations for a SPSI edge detector were discussed in Chapter 2.

For a better review of the SPSI concept, it is useful to distinguish between two areas of applications: sensors, and image processing. The main differentiating factor in this distinction is the number of pixels in the scene, although drawing an exact line between the two areas is difficult. In image applications information from many pixels has to be processed. For example, a CCD camera produces an image quality output from a scene, whereas a single optical detector normally averages the optical intensity over the whole scene. The utilization of the SPSI concept in image processing applications is mainly limited by the number of available emitters and detectors as well as the fill factor of an OE array. For example with the VCSEL-MSM chip used in the previous chapters, a scene can only be sampled in a 4×4 pixel format, a resolution hardly enough for any image processing. Using OE chips with higher number of sources and detectors will

alleviate this shortcoming, but creates a new problem of interfacing with the chip. For example if a 50×50 array of emitters and detectors is assumed, 5000 devices and about the same number of connections have to be taken into consideration. Obviously it is not practical to bring several thousand lines off the chip, which means the only remaining solution is to have on-chip multiplexing capabilities. Because most OE arrays are GaAs based, this in itself is a challenge as the wealth of information and technology available in Si-based electronics is not readily available in GaAs integrated circuits.

There may be a variety of approaches to address this problem, some of which may require a certain level of departure from the main SPSI concepts presented in Chapter 2. A possible solution is to separate the emitter array and the detector array. In such an approach, a high efficiency detector array (such as a CCD chip) can be combined with a separate array of emitters, not necessarily with the same resolution. In such a scheme a one-to-one correspondence between the emitters and detectors is no longer maintained, as a single emitter may illuminate part of scene which is imaged back to many detector pixels.

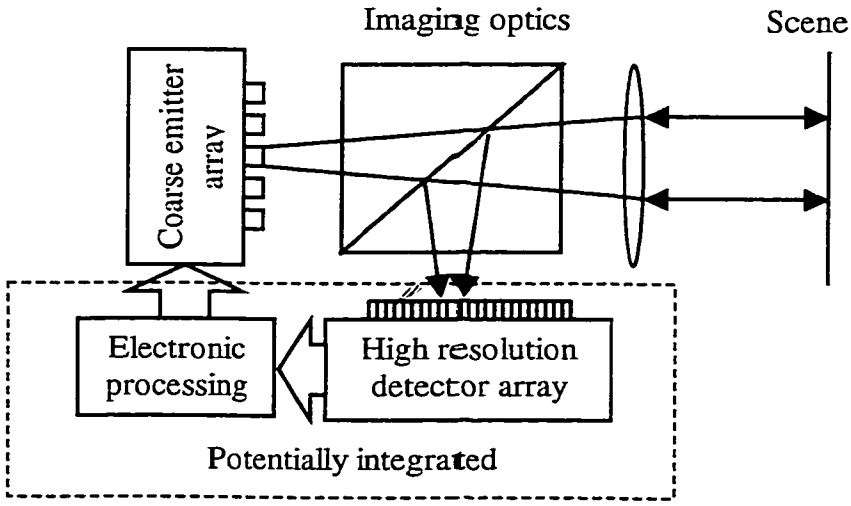


Fig. 7.1. Separation of Emitter and Detector Arrays.

Figure 7.1. illustrates such a system. Several issues may be pointed out if this system is compared to an integrated emitter detector array. This system solves the problem of insufficient imaging pixels because it uses a high-resolution detector array. It also addresses a very important problem: the technology for the emitter array does not need to be the same as the technology for the detector array and electronic circuits. This means that very efficient and sensitive detectors (such as Si detectors or CCD arrays) can be used with efficient light sources such as VCSEL's. The same does not necessarily hold for integrated OE arrays, for example the MSM detectors on the VCSEL-MSM chip do not have very impressive specifications compared to other Si detectors. This approach is also attractive because of the possibility to integrate the detector array with the processing electronics (but still have a separate emitter array), thus partially recovering the integration benefits. It should be noted that the underlying ideas behind "smart" and "structured" illumination are still applicable in a system like this because the illumination of individual emitters can be controlled as a function of signals detected by individual (or groups of) detectors.

However, there are disadvantages to this system as well. Having separate emitter and detector arrays requires additional (possibly expensive) optics such as beam-splitters, and introduces more tolerances on the alignments. On the electronic side, if the emitter array and processing electronics are not integrated, the information from the detector array must travel to a separate chip, be processed, and then delivered to the emitter array. This interconnection overhead reduces the speed of the system (especially if large amounts of data are involved) and may require additional electronic considerations. Although the same interconnection overhead exists in the ASIC approach presented in Chapter 6, ideally a totally integrated array with on-chip processing power does not face this limitation. Considering these advantages and limitations, this approach may in general be suitable for applications where speed is not critical but high resolution or high detector sensitivity is needed.

A different approach can be taken by scanning a scene when the number of detectors and emitters is limited but high spatial resolution is still required. In this case the resolution is set not by the emitter or detector pitch, but by the scanning system. Figure 7.2 illustrates a scanning SPSI system.

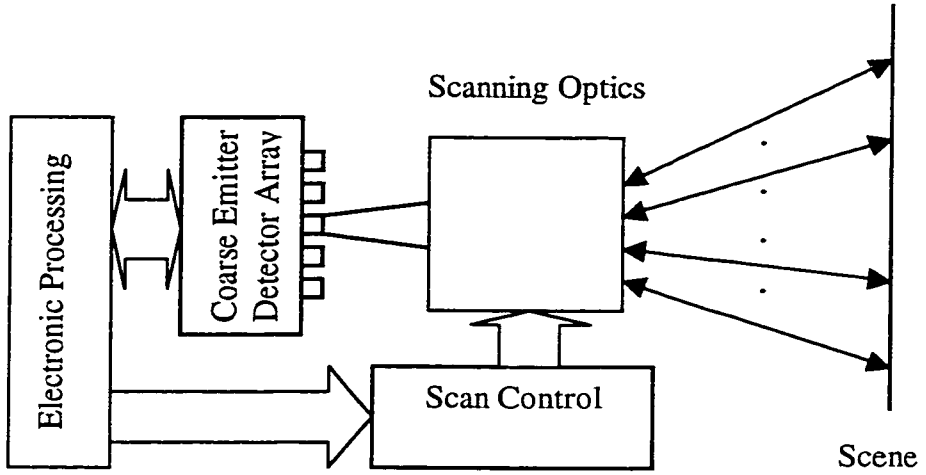


Fig. 7.2. Scanning SPSI system.

In general a trade-off between resolution and speed exists, as is the case with most scanning systems. A mechanical system allows for slow but very high-resolution detection, where as an acousto-optic modulator results in fast but low-resolution operation. Compared to a simple SPSI system, here again additional issues such as alignment tolerances, electronic interconnections, and synchronization with the scanning system have to be considered.

SPSI sensor applications do not necessarily require high resolution and therefore may be realizable more readily with current state of the art OE technology. For example a tracking sensor may require only a few sources and detectors. An important issue here seems to be the range, which is directly related to the dynamic range of detectors and the

power of the emitters. In the case of the VCSEL-MSM array, in all the experiments a partially reflecting surface was used to implement the optical feedback. If a diffracting surface is used instead, the amount of light focused back on the detectors will be reduced substantially. This causes additional challenges for the circuits, and eventually limits the range due to the limited dynamic range of the detectors. Increasing the useful range of the SPSI system in such situations would require additional solutions, such as modulation of the emitters, or operating them in pulse mode to increase their instantaneous power.

The last two solutions bring up an important point. In most SPSI applications it is implicitly assumed that the primary quantity to be controlled is the illumination intensity. But optoelectronic feedback is not limited to intensity, in fact, *any* aspect of illumination can be changed as a function of the information received from the scene. The major parameters (in addition to intensity) that can be controlled are modulation frequency, and the shape of the modulation. For example pulse mode operation can be viewed as a special case where the shape of modulation is changed to achieve a higher peak power while keeping the average power low. A "strobe" mode operation is another example, where in the case of a scene with temporary periodic modulation, the frequency of the pulses are varied such that the sensor is "locked" to some frequency of the scene. Multiple sources can be used to lock to several frequencies in the scene, or different frequencies at various points across a scene. There are other cases where even the wavelength of the light can be a variable. If different VCSEL's on the chip can be tuned individually, a color feedback scheme can be envisaged, where either the individual VCSEL's on the chip tune their lasing frequency in response to changes in the scene, or different VCSEL's with different frequencies are turned on accordingly.

Another common assumption in Chapter 2 was that SPSI sensors are based on negative feedback schemes. However, as shown in Chapters 4 and 6, positive feedback can also be used in a variety of situations. SPSI sensors based on positive feedback demonstrate switching behaviors, making them more suitable for interfacing with digital control and

processing systems. An example of such SPSI system was demonstrated in Chapter 6 where the reflectivity of the scene was used to switch the pixel on or off within a hysteresis loop. Such SPSI sensors may find practical applications in optical memories, CD ROM's, and similar optical data processing systems.

These potential applications need further studies, and some may require technological advancements not currently available. Nevertheless, they may provide motivation and future directions for research in the area. Even with simple intensity feedback schemes, there are new possibilities that can motivate and expand the radius of research in SPSI sensor applications. In the next section one such new area of SPSI applications is briefly introduced.

7.2. SPSI in Spatial Frequency Domain

One of the interesting aspects of SPA's is the spatial bandwidth that they provide. Just like temporal signals that can be represented or processed in time or frequency domains, optical signals (images) can be processed in real space or the spatial frequency domain. All of the SPSI applications considered so far deal with optical signals in real space. It is interesting, however, to consider the applicability of the SPSI concept in spatial frequency domain.

In general, an image can be considered as the two dimensional sum of various spatial frequencies in perpendicular directions. Just like temporal signals, low spatial frequencies correspond to the average or long range intensity variations, where as high spatial frequencies represent sharp edges and other short distance effects. It is also a well-known fact that a lens in an f-to-f imaging system can be used to transfer between the two domains.

To illustrate an example of a SPSI in spatial frequency domain, consider Fig. 7.3 where a single emitter illuminates the scene through a Fourier lens. Because the emitter is a point

source compared to the size of the lens, it acts approximately as a delta function in the spatial frequency domain. The Fourier transform of a delta function is a dc function, which means the scene is now illuminated with a uniform light. Thus, the reflected field close to the scene, r(x,y), is the exact image of the scene.

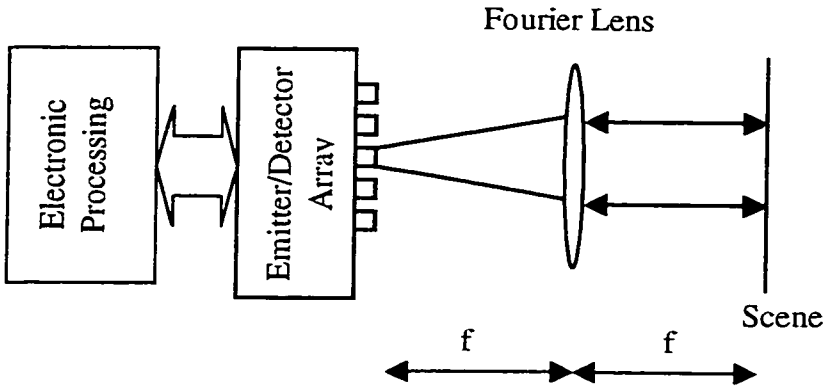


Fig. 7.3. Simple spatial frequency domain SPSI sensor.

However, after this field has traveled back to the OE array it has passed through the Fourier lens again. This means that the field received by the detector array, R(x,y), is the Fourier transform of the image of the scene. Thus the detectors in effect see the spatial frequency content of the scene. The intensity at the center of the OE chip represents the dc component if the image, and the higher spatial frequencies are imaged onto detectors further away from the center. Various information about the scene not readily available in the real space domain can now be extracted, for example a peak in a certain location corresponds to a periodic pattern in the scene. More complex image processing tasks may be performed if the resolution of the detector array is high enough. For example, certain features in the scene may have known spatial frequency signatures. In an image recognition application once that signature is encountered by the detectors, a

corresponding emitter can be turned on, marking that particular feature within the scene. The scene can also be illuminated from different angles if different emitters on the array are used. This is because a displacement on the OE array plane translates to an angle in the Fourier plane (the scene). An application of this property is that by using different sources on the array for illumination the Fourier image can be shifted against the detectors on the pixel, resulting in an increased effective resolution. Such a system may find applications in areas such as optical character recognition (OCR), bar code systems, and surface analysis.

The intention here is not to fully analyze such spatial frequency domain applications for SPSI, rather, to point out that many novel potentials exist in this area that future SPSI studies should consider.

7.3. Modeling OE arrays

One of the important aspects for research in SPSI and related optoelectronic applications is modeling. Having proper models plays an important role in the understanding, evaluation, and development of new applications. Chapters 2 and 3 included several modeling details for SPSI concepts and optoelectronic feedback loops. In Chapter 4 those models were integrated into a general matrix formalism for modeling various optoelectronic interconnections (including feedback) in SPA's. The models include several effects such as emitter nonlinearity, current leakage, and cross-couplings between various elements.

There are several areas where these models can be improved. A main limitation on these models is that they essentially result in steady-state solutions. In other words, they do not take into account the dynamics of the system, because in reality most of the involved parameters are frequency dependent. Under certain assumptions it is not hard to generalize the formalism to include dynamic effects. One approach is to replace the parameters with their frequency dependent equivalents by including the proper poles and

zeros in them. For example the gain A of a detector can be replaced by $A/(s+s_0)$ if it has a dominant pole at s_0. Making parameters frequency dependent in this manner results in frequency dependent matrices, and classical techniques can be used to analyze them. Important insight into the analysis of such issues as stability of the loops can be gained in this way. Whether and to what extent such an approach is possible is to a great degree a function of the linearity of the system. For example for small signal analysis and for negative feedback loops this approach seems most suitable. However, for large signal analysis and for positive feedback loops numerical methods may present the only practical modeling tool.

In any case, and even if certain analytic methods are applicable, numerical methods are valuable tools in analysis of large systems. The power of such numerical methods is a function of the models they are based on. Complex OE systems are comprised of various devices. There exists a large amount of research, methods, models, and software for analysis of purely electronic devices (such as MOSFET's) and circuits. However, the situation is not the same for optoelectronic devices such as VCSEL's. More work needs to be done to develop suitable models for such OE devices and to incorporate such models into the existing simulation tools such as SPICE and SABER.

7.4. Electronics Interface Architectures

In Chapters 5 and 6 a modular approach to interface electronics for OE arrays based on analog current processing modules combined with digital programming capabilities was presented. There are several advantages to this approach. The electronic blocks can be connected together in a variety of configurations to build up the necessary functionalities for different applications. The addition and subtraction of signals automatically takes place at connection nodes. The fact that the circuits are current mode makes them readily interfaceable with emitters and detectors, while the digital programming ability allows for accurate control of loop gains. It also makes it possible to change the topology of the circuits without any change in the hardware, because programming a zero gain in a block

causes it to go to a high-impedance state, thus disconnecting it from the rest of the modules. Moreover, by changing the sign of the currents it is possible to switch between different functionalities, for example between positive and negative feedback schemes.

However, one limiting factor in this architecture was that the design was pad-limited. In order to keep the ASIC chip general, it was necessary to bring all the inputs and outputs off-chip. If a more specific optoelectronic function is to be implemented, it would not be necessary to bring all the inputs and outputs off chip. This allows more modules to be included on the die, which translates to more per-chip processing power.

Another factor to be considered is that the circuits were primarily designed with low frequency applications in mind. SPICE simulations estimate the current-gain bandwidth of these modules to be between 1-10MHz depending on the module and bias currents. The primary goal was to demonstrate the functionality of the circuits, and other issues, such as bandwidth, were not of primary importance. As was previously mentioned, there are many potential SPSI applications where some form of modulation of the emitters may be necessary, i.e., not all signals within the system are necessarily DC. This becomes more important with VCSEL's because of their wide bandwidth characteristics. In any case, these circuits are not necessarily optimized for high frequency applications and their designs may need some modifications. It should be mentioned, however, that the maximum speed needed for sensor applications is not likely to be very high, because generally physical changes in the scene are slow compared to electronic speeds.

Most of the electronic modules discussed in Chapters 5 and 6 (and in general most current -mode circuits) are based on current mirrors. One of the issues of potential concern with the current mirror circuits discussed in the previous chapters is their relatively high input impedance, which ranges in the 500-50kΩ range depending on the polarity of the circuits and the biasing points. This high input impedance limits the range of the input currents and creates loading effects for the driving circuits. This problem can

be addressed in several ways. The simplest solution is to use shorter channel transistors (smaller L's). This approach simultaneously decreases the input impedance levels and increases the speed. The draw-back is that it also decreases the output impedance level of the modules. However, this may not be as problematic as it first appears to be, because the output impedance of many of the modules is very high to begin with. Moreover, the lower impedance levels at the outputs of modules is somewhat compensated by the lower input impedance levels they see at the inputs of other blocks.

Another approach to decrease the input impedance of the modules at the cost of increased circuit complexity and area is using the so-called "active input" approach [78]. A simple example of this approach is shown in Fig. 7.4. This circuit isolates the gate-source and the drain-source voltages of the input transistor.

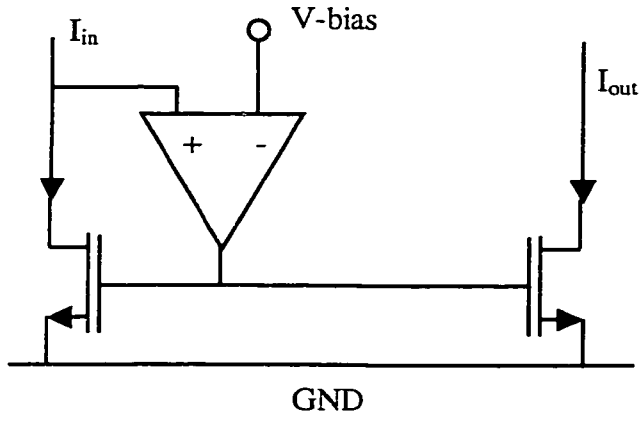


Fig. 7.4. Active input current mirror.

By keeping the drain-source voltage constant and equal to V-bias, it lowers the effective input impedance. It is also possible to enhance other performance aspects of the mirror such as output impedance, dynamic range, and current matching by using additional

feedback schemes [79,80]. Employing such schemes requires application-specific considerations, as they usually require more complicated (and therefore larger) circuits than those discussed in Chapters 5 and 6. There are also issues with respect to the size of these circuits. The chips used in this study were fabricated with the AMI 1.2 μm process. Given the progress in state of the art deep sub-micron CMOS circuits, it is eventually necessary to consider using a smaller technology. The benefit of using smaller technologies is that the transistors are generally faster and more circuits can be included in a certain die area. However, it should also be remembered that smaller transistors are mostly optimized for digital applications and various short-channel effects should be taken into consideration when using such sub-micron technologies.

7.5. Summary and Conclusion

This chapter started with a critical review of the SPSI concept. Several suggestions were made to address certain shortcomings that currently exist with the state of the art optoelectronic technology available. Some of these suggestions, like the separation of emitters from detectors, included a certain level of departure from the approaches presented in Chapter 2. Others represented more emphasis on time and pulse modulation, as well as broadening of SPSI concepts to include positive feedback and spatial domain applications.

This chapter also included a brief review of the modeling techniques presented in Chapters 2, 3, and 4. It was mentioned that an important area of expansion for these models is to include dynamic effects in them. In addition, more accurate models of optoelectronic devices have to be developed and incorporated into numerical techniques as well as standard simulation tools such as SABER or SPICE.

Finally, the electronic interface circuits and architecture presented in Chapters 5 and 6 were reviewed. It was mentioned that in addition to basic functionality, other goals such as dynamic range, linearity, input/output resistance, speed, and use of smaller CMOS

technology have to be considered eventually, in which case these circuits may not represent an optimal approach. A trade-off between the simplicity and the small size of the existing circuits and the possible complexity required for some of these goals should be addressed based on the specific needs of the particular applications for which such ASIC chips are designed.

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Selected Publications

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