Integrated circuit design to enable quartz free miniature wireless sensing systems

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Abstract

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Emerging technologies such as Internet of Things (IOT) and Wireless Body Area Network (WBAN) demand wireless sensors with ultra low power consumption, low cost and previously impossible form factors. Moore's law is exponentially scaling down the size of CMOS circuits making them faster and cheaper. However, frequency references, antennas and power sources which are essential for wireless sensors do not benefit from such scaling. These components are increasingly becoming a bottleneck in achieving size/cost/power reduction in wireless sensors.

Quartz crystal is the most commonly used frequency reference in radios. Quartz crystal is bulky, needs a complicated manufacturing process increasing cost and does not yield itself to integration with CMOS circuits. This has prompted circuit designers to look for MEMS based alternatives to Quartz crystals. While MEMS resonators are successfully replacing quartz in timing applications, a quartz alternative with stability / power consumption suitable for radio applications has not been reported so far.

The first part of this thesis addresses this problem and develops circuits and systems to demonstrate an FBAR (thin-Film Bulk-Acoustic-Resonator) based quartz replacement. Circuit solutions to improve phase noise and temperature stability of FBAR oscillators are discussed. These efforts culminate in a 750 MHz FBAR frequency reference with a ± 3 ppm stability and 1.1 mW power consumption.

The second part of the thesis addresses the challenge of power delivery to miniature subcutaneous sensors. At mm scale inductive power transfer efficiencies drop below 0.1 %. In applications where the implant is just below the skin optical powering becomes a viable option due to high transmission of skin at infrared wavelengths. We demonstrate an operational mm scale tag with optical power and data links across a pig skin barrier.

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GLOSSARY

FBAR: thin-Film Bulk Acoustic Resonator

ZDR: Zero Drift Resonator

MBVD: Modified-Butterworth-Van-Dyke model for FBAR resonators

QUARTZ CRYSTAL: State-of-the-art frequency reference used in radios

WBAN: Wireless Body Area Network

IOT: Internet of Things

PHASE NOISE: A measure of short term frequency stability of an oscillator

ALLAN DEVIATION: A measure of long term frequency stability of an oscillator

TDC: Temperature to Digital Converter

MEMS: Micro - Electro - Mechanical Systems

CMOS: Complementary Metal Oxide Semiconductor

DCO: Digitally Controlled Oscillator

TOT: Turn Over Temperature

MPE: Maximum Permissible Exposure

ACKNOWLEDGMENTS

Professional acknowledgements

I remember myself waiting for my pickup sitting in a bench in SEATAC airport about 4 years ago. I had just landed in the US not knowing many people in this country. In a weird coincidence I am almost at the very same spot in SEATAC when I am writing this. I have grown, changed and learnt a lot in the years in between. That would not have been possible without the help and support of several people.

First and foremost, I would like to thank my advisor and mentor Prof. Brian Otis. I have learnt a lot from him in these 4.5 years I have worked with him. He has taught me so many things directly or indirectly : circuit design, being passionate about what you do, how to effectively interact with people and so on. There were several moments in my PhD when I almost considered quitting. Brian's support and his trust in me were the key reasons I kept on. I made several stupid mistakes in my initial years. Not once can I remember him getting upset or frustrated with my mistakes. He gave me second chances and helped me correct my mistakes.

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I have always enjoyed a large degree of freedom in my research. He has let me explore, fail, learn and grow as a researcher. I am extremely grateful to have such a wonderful person as my advisor and mere words cannot express my gratitude

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DEDICATION

The dedication goes in 3 ways
To
My parents
My wife Saravanya
and
Prof. Bharadwaj Amrutur

Chapter 1

INTRODUCTION: CHALLENGES IN BUILDING NEXT GENERATION WIRELESS SENSOR NODES

Sensing and manipulating the environment has always been a subject of great fascination to the humans. This interest in 'knowing our environment' will continue to grow in the future and the number of sensors is predicted to reach 1 trillion by 2025 [1]. These ubiquitous sensing nodes will be wirelessly connected to one another though emerging technologies such as Internet of Things (IOT) and Wireless Body Area Networks (WBAN). IoT is expected to connect more than 50 billion devices by 2020 (Figure 1.1) [2] enabling new applications such as environmental monitoring across large urban areas(Intel-Dublin smart city project [3]) and home automation.

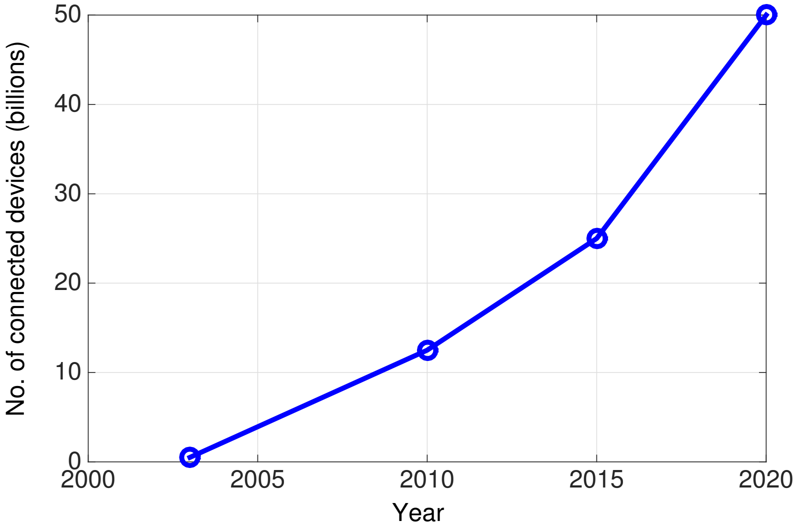


Figure 1.1: Estimated number of devices connected to Internet of Things

A WBAN wirelessly connects several physiological sensors placed on or inside the human

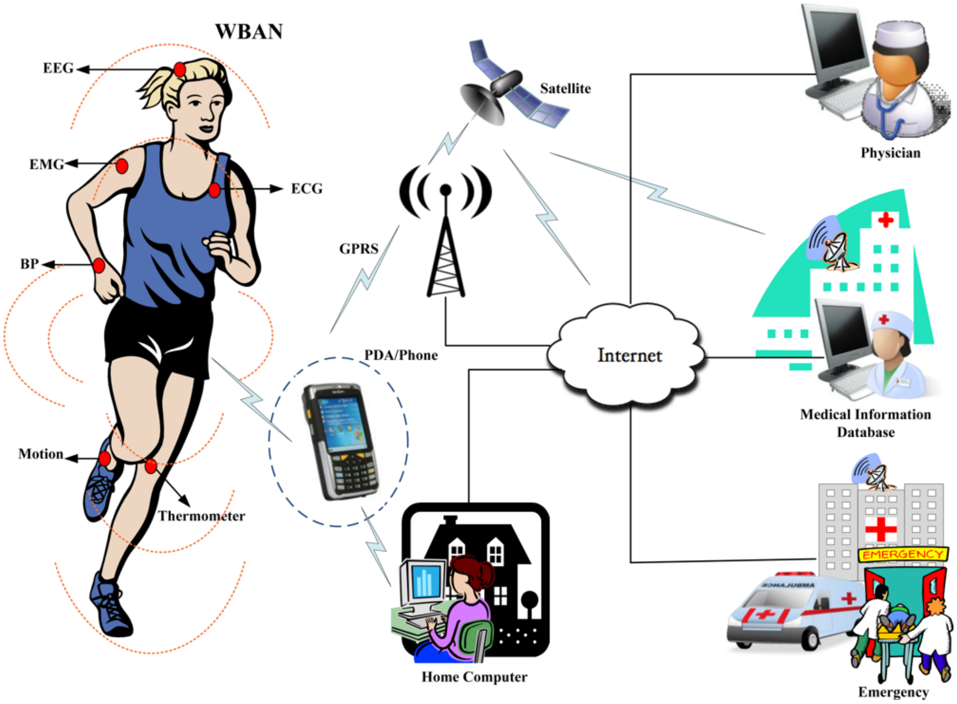


Figure 1.2: Illustration of a Wireless Body Area network

body as illustrated in figure 1.2. Such body-worn or implanted sensors enable continuous monitoring of bio-signals which helps health-care professionals to diagnose, prevent and respond to various illnesses in a timely fashion. For example, they can be used to monitor glucose levels [4], electrocardiogram [5] intraocular pressure [6] etc..

1.1 Requirements of a wireless sensor node

The above mentioned applications impose the following requirements on a wireless sensor node.

- **Small form factor**

  These emerging applications demand highly miniaturized wireless sensors with previously impossible form-factors. For example in [4], the entire electronics for sensing and transmission had to be integrated in a small area of 0.5 mm^2 to account for the curvature of the contact lens. In [6] the intraocular pressure monitor need to have a volume of $\approx 1mm^3$ so that it can be surgically implanted into the anterior chamber of the human eye. Such stringent size limitations demand a high level of integration with the energy source, transducer, interface circuitry, radio and the timing reference integrated together in a volume ≤ 1 mm^3 .

- **Ultra low power operation**

  Sensor nodes need to operate from a small thin film battery or from wirelessly delivered / harvested energy. This necessitates ultra-low-power (ULP) operation for the sensor node. Let us assume we use a Cymbet thin film battery with a storage capacity of 12uAh, [7] and assume the peak power of an active wireless sensor is 25uW. With no recharge, the sensor node will last only for 48 hours with 1% duty cycling. For sustained long term operation, the required energy must be harvested from the ambience or must be delivered to the node wirelessly.

- **Low cost**

  Commercial viability of large scale sensor networks dictates that the cost of a single sensor node must be small. For example, assume the sensors market is 0.1% of the global GDP of $130 trillion, To get to a trillion sensors, the cost per sensor has be less than 13 cents. This requires the use of a minimal number of components, a high level of integration, and cheap manufacturing/packaging processes.

To summarize, every component of a sensor node must be designed with power consumption,cost and size considerations.

1.2 *Quartz replacements for wireless radios*

1.2.1 Need for quartz replacements

Every wireless radio operates at a specific frequency dictated by standards and regulation bodies (Federal Communications Commission in the USA). This necessitates radios to have a frequency reference. The current paradigm in radio design is to use an AT-cut quartz crystal as the frequency reference due to its high quality factor ($\geq$ 100,000) and exceptional frequency stability. But, quartz crystal is becoming a huge bottleneck in achieving cost/size reduction in next generation wireless sensor nodes. A typical quartz crystal has volume of 1.2mm x 1mm x 0.3 mm [8]. Figure 1.3 shows a bio-signal sensing system built at the University of Washington. We see that the quartz crystal is comparable in size to the integrated electronics fabricated in a 130nm process. With the size of integrated circuits scaling down exponentially due to Moore's law, quartz crystal is bound to become the biggest component in a radio in the near future.

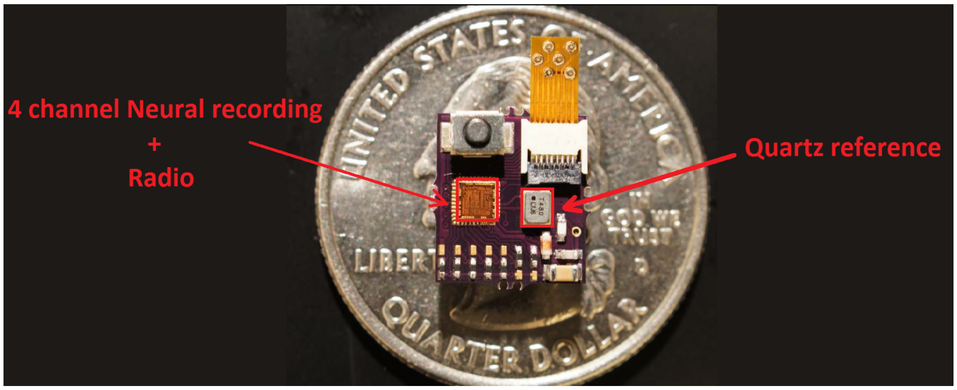


Figure 1.3: Bio-signal recording system developed at Univ. of Washington

Commercial crystals are made from quartz synthetically grown in a special furnace using a slow process that takes more than 45 days. This complex manufacturing process makes quartz a cost prohibitive solution for wireless sensor nodes. (Typical 26 MHz, +/- 10ppm

Quartz crystal costs $\geq$ 10 cents in volume.).

The resonant frequency of quartz crystals are typically $\leq$100 MHz, while radios need higher frequencies for transmission (WBAN commonly uses 2.4 GHz). A phase locked loop (PLL) is typically used to synthesize higher frequencies from the low frequency reference provided by quartz. Figure 1.4 shows that the frequency synthesis consumes $\sim$45% of the receiver power consumption. A quartz-less radio where the frequency reference is directly synthesized without a PLL will be more power efficient.

In short existing paradigm of using a quartz crystal as a reference for frequency synthesis will become a bottleneck in reducing size, power and cost of next generation wireless sensors State of the art sub mm^3 sensors achieve quartz-less wireless connectivity either by using a passive backscatter link [4] or by using an on-chip LC frequency reference [6]. While passive radios are attractive from size/cost perspective, they do not support peer-to-peer connectivity and make the link highly asymmetrical. On-chip LC oscillators have poor temperature stability and will violate transmit spectrum masks when used as frequency references. Next

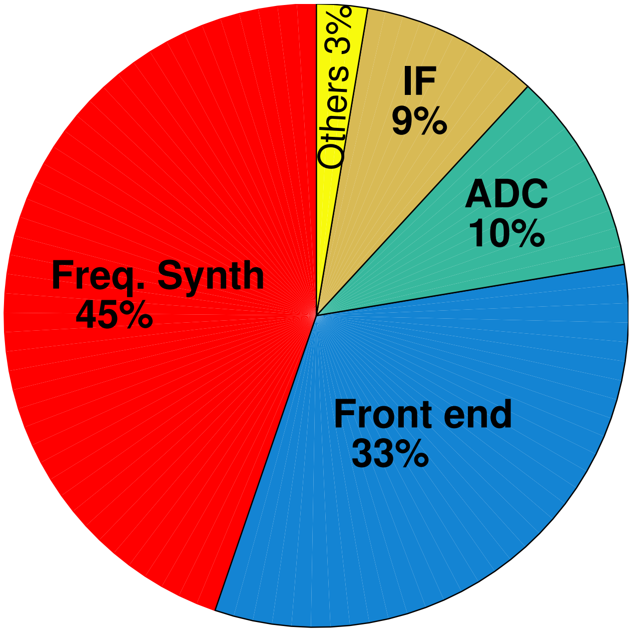


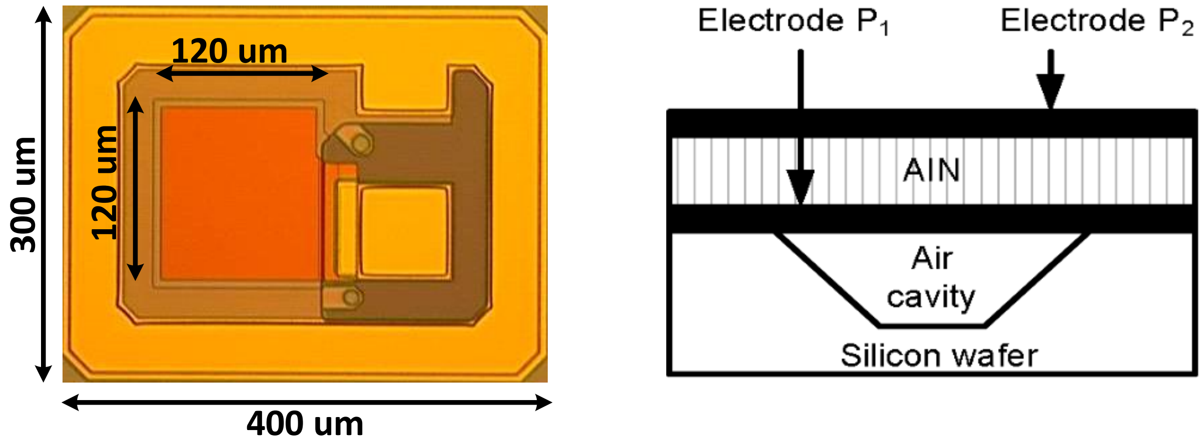
Figure 1.4: Power breakup of state of the art PLL based Zigbee receiver [9]

generation wireless sensor nodes need a new class of radios that offer cost/size approaching backscatter communication while still maintaining peer-to-peer connectivity like more complex radios.

A miniature, high quality (Q) resonator, fabricated using wafer-scale semiconductor processing will be a good alternative to quartz crystal and will enable us to achieve a sub mm^3 wireless sensor. Further, a resonator with resonant frequency in GHz range will enable power efficient PLL-free frequency synthesis architectures suitable for a sensor node [10]. Resonators fabricated using MEMS (Micro-Electro-Mechanical-Systems) technology are attractive quartz alternatives owing to their low cost and small size. Several MEMS based quartz alternatives are available in the literature [11] [12] [13] [14]. But the existing solutions are not suitable for RF frequency synthesis due to their high power consumption (100 mW) [11] or low output frequency (32 KHz) [12] or extremely poor phase noise [14]. The first part of this thesis addresses this problem and demonstrates a MEMS based quartz replacement with size (sub mm^3) , power consumption (∼1 mW) and output frequency (750 MHz) suitable for wireless radios. The demonstrated solution uses thin-Film Bulk Acoustic Resonators (FBAR) from Avago technologies. The next section gives a more detailed overview of FBARs.

1.2.2 FBAR overview

This section gives a brief overview of FBAR technology. A more detailed tutorial can be found at [15]. FBAR (Film Bulk Acoustic wave Resonator) is a miniaturized acoustic resonator with a metal-piezo-metal structure. It is fabricated in a planar silicon process with two molybdenum layers sandwiching a layer of piezoelectric material (AIN) (Figure 1.5). When an electrical signal is applied across the two electrodes, an acoustic wave is generated through the piezoelectric effect, thus energy is converted from the form of electrical signal into mechanical vibration. The thickness of the piezoelectric film and the electrodes in the FBAR structure determines the resonant frequencies, which can be reliably controlled from several hundred MHz to the low GHz range. FBARs have been demonstrated at several frequencies between 325 MHz and 10 GHz. Unlike quartz, FBAR can be manufactured in batch mode on Silicon substrate using wafer scale semiconductor fabrication processes. FBAR devices have been fabricated as small as $100\text{x}\ 100\mu m^2$ about 100 times smaller than quartz crystals. Figure 1.6a shows a plot of Frequency Vs Impedance of an FBAR resonator. There are 2 resonant frequencies: Series (f_s) and Parallel (f_p). For circuit simulations FBAR is modelled using a Modified Butterworth Van Dyke (MBVD) model shown in figure 1.6b.

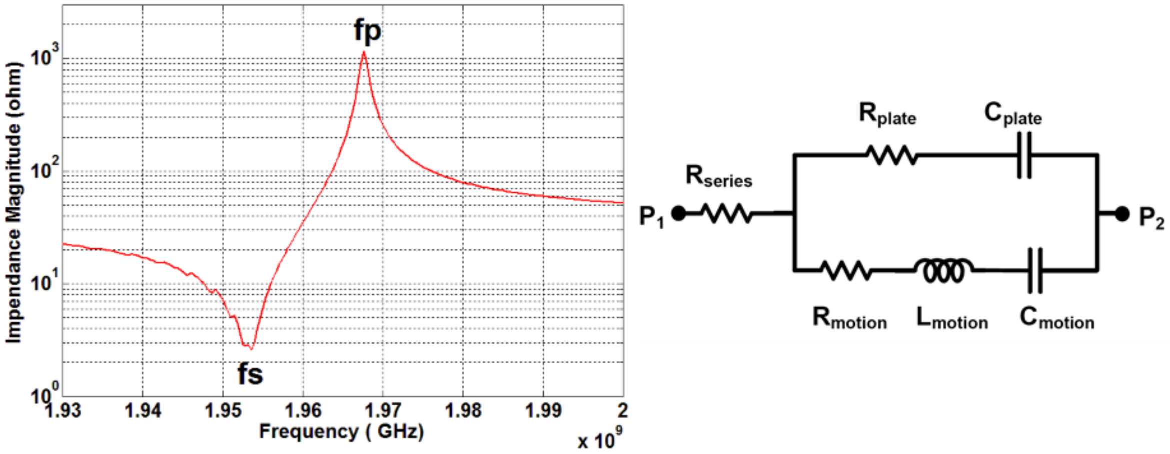


a) FBAR die (Courtesy Avago)

b) FBAR cross section

Figure 1.5: FBAR Die and FBAR cross section

Quality factors of FBARs are in the order of a few thousands. The f-Q product - a resonator performance metric - is 10^{13} which is comparable to quartz crystals. Such high quality factors enable narrowband RF filters. FBAR filters are commonly used in mainstream mobile phones and more than a billion FBARs have been fabricated and sold. FBARs also enable ultra low power oscillators [16], frequency synthesizers [10] and transceivers [17] . [10] uses an FBAR based quartz-less frequency synthesis for a zigbee receiver and achieves a 2X better power consumption than the state of the art



a) Measured Impedance of a typical FBAR **b) MBVD model used for circuit simulation**

Figure 1.6: Measured Impedance of a typical FBAR and MBVD model

FBARs have been integrated with CMOS circuits in a wafer scale package [18] offering highly miniaturized GHz oscillators. A SEM image of FMOS (FBAR + CMOS) can be seen in 1.7. Table 1.1 compares FBARs with Quartz showing FBARs are superior to Quartz in terms of size, cost and frequency synthesis power consumption. This makes FBAR an ideal candidate to use as quartz replacement in wireless sensors. But, FBARs perform worse compared to quartz in terms of phase noise and frequency stability. This is described in detail in the next section.

1.2.3 Challenges in building FBAR based quartz replacements

FBARs performs poorly compared to Quartz resonators in the following areas.

1. Phase Noise: Phase noise measures the frequency purity of an oscillator's output. A more detailed discussion of phase noise is presented in chapter 3. Figure 1.8 shows a comparison of the phase noise performances of FBARs and Quartz normalized to the

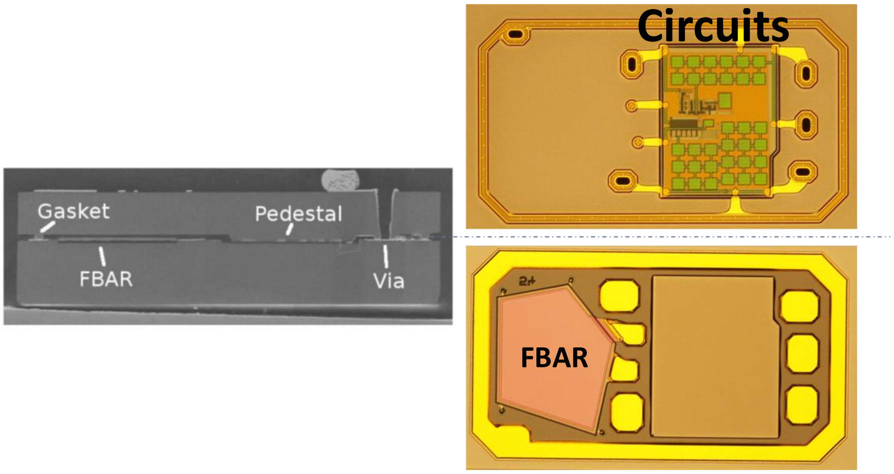


Figure 1.7: SEM cross section of FMOS Die (FBAR + CMOS)

Table 1.1: Comparison of FBAR and Quartz

Metric	Quartz	FBAR
Frequency	<100 MHz	384 MHz-3.5 GHz
f-Q Product	10^{13}	10^{13}
Size	> 1.2 x1.0 mm^2	0.1 mm x 0.1 mm
fabrication process	Complex	simple
CMOS Integration	No	Yes
Needs PLL?	Yes	No

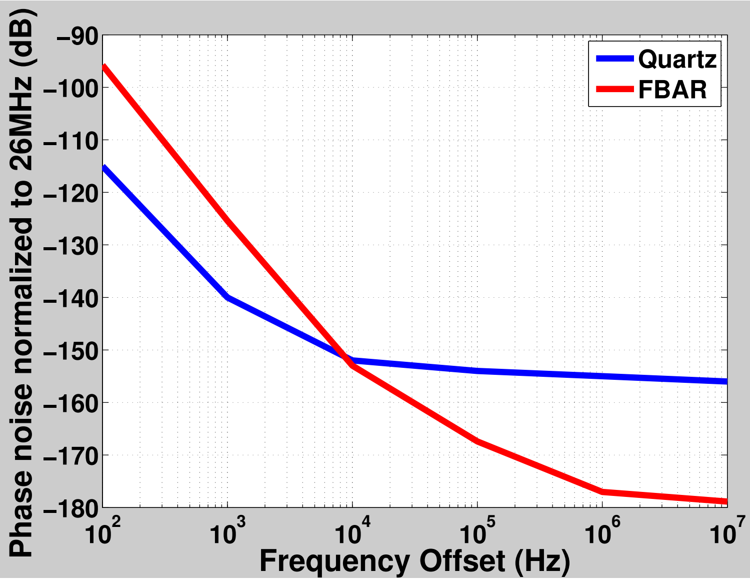


Figure 1.8: Phase noise of FBAR compared to quartz (normalized to 26 MHz)

same frequency. We see that FBARs perform ∼20 dB worse than quartz at offsets $<$ 10KHz. While phase noise of an FBAR oscillator is still sufficient to meet the specifications of several wireless standards, a fundamental understanding of the reason for this phase noise degradation is needed.

2. Frequency stability: Initial frequency accuracy of FBAR resonators across a wafer is about ±50 ppm [19]. Frequency drifts due to aging and stress are about 60 ppm [20]. Frequency of an FBAR (zero-drift-resonator) oscillator has a quadratic dependence over temperature and moves by about a 100 ppm over temperature (see Figure 1.9). This stability does not meet the requirements of radio standards given in Table 1.2 [21]
.

These issues must be solved to build an FBAR based quartz replacement. The first half of this thesis presents circuit and system level techniques to improve the phase noise and frequency stability of FBAR oscillators. The proposed techniques culminate in a demonstration of a 750 MHz FBAR frequency reference with a frequency stability of ± 3 ppm and

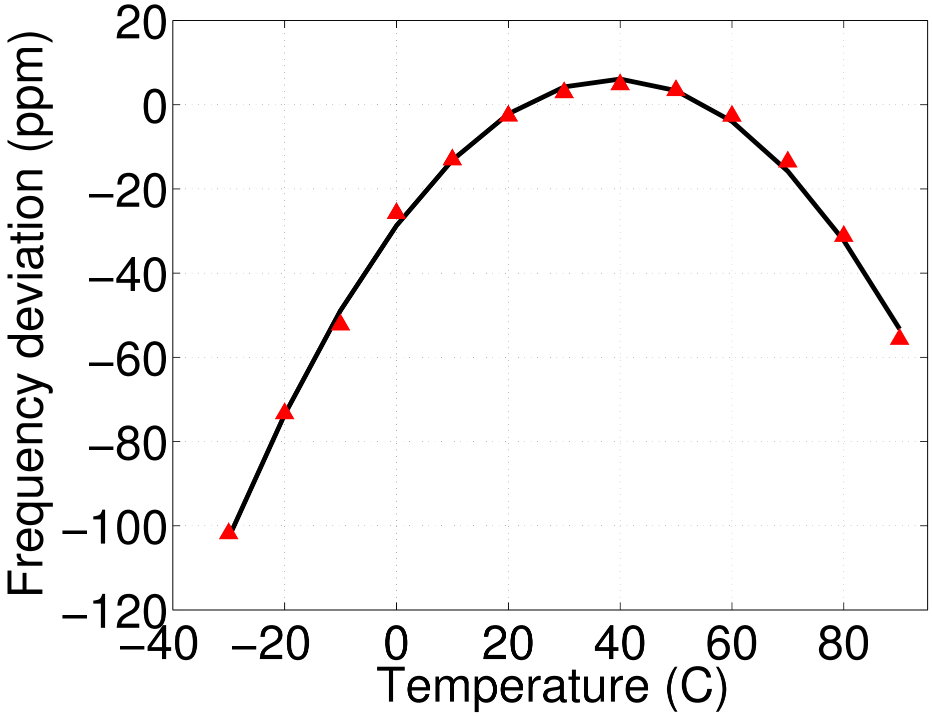


Figure 1.9: Frequency drift of FBAR over temperature

Table 1.2: Frequency stability specification for various radio standards

Radio standard	**Frequency stability specification (ppm)**
Zigbee	±40
Bluetooth	±60
WLAN	±20
GSM	±5
WCDMA	±5
GPS	±1

sufficient phase noise for radio applications.

1.3 optically powered bio-sensing platform

The second half of the thesis focuses on the development of a fully integrated implantable sensor for subcutaneous bio-sensing. State of the art bio-sensors use inductive coupling or RF power transfer to deliver power to implantable sensors. Aesthetic reasons and surgical limitations restrict the size of a sub-cutaneous implant to the mm-scales. Efficiencies of RF wireless power transfer schemes are less than 0.1% when the antenna/coil size are restricted to mm scales. [22] [23]. A barely sub-cutaneous implant which resides just below the human skin opens up another more efficient mechanism for power transfer- optical. Human skin has a high transmittance at infrared wavelengths 650nm - 950 nm known as the diagnostic or therapeutic window. Exploiting this property of skin, an optical power and data link can be established between the implant and a body worn external reader as shown in figure 1.10. The last part of this thesis addresses the design of an optically powered bio-sensor and demonstrates a 8mm x 3.5 mm implant with a 1.5 mmx 1 mm CMOS IC at its core.

1.4 Contributions of this thesis

This thesis is organized as follows

- **FBAR-CMOS co-design**
  Chapter 2 derives the design equations to aid the co-design of FBAR-CMOS oscillators. The principles from this chapter are used in all FBAR oscillators designs discussed in the other chapters.

- **Close-in phase noise improvement technique**
  Chapter 3 addresses the dominant close-in-phase noise mechanism in an FBAR oscillator and proposes a phase noise reduction technique. Measurements from an FBAR oscillator fabricated in a 130nm CMOS process demonstrate a 4 dB improvement in phase noise with no power penalty.

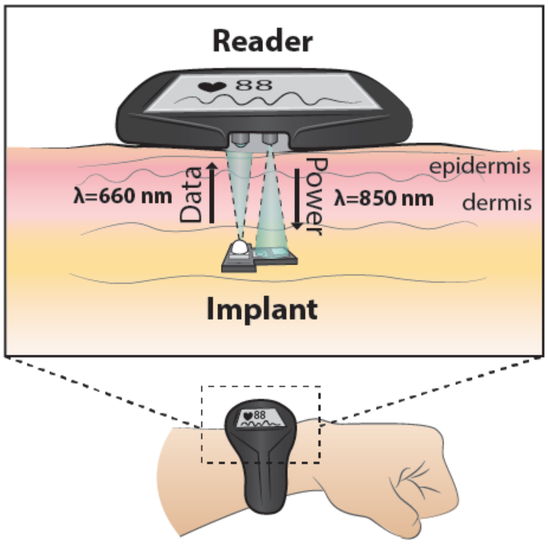


Figure 1.10: Illustration of a barely subcutaneous sensor

- **FBAR based quartz replacement**

  Chapter 4 and 5 present circuits and system design to improve the temperature stability of FBAR oscillators to enable an FBAR-based quartz replacement for radio receivers. Two proof-of-concept designs fabricated in 65nm CMOS process are presented. The first design achieves a ± 20 ppm stability across temperature and consumes $\sim$ 2.5 mW from a 0.75V supply. Several issues in the first design were rectified and an improved version of the system was fabricated. The second prototype includes a novel low voltage temperature sensor and achieves a ± 3 ppm stability. Power consumption was also reduced to 1.1 mW in the second design.

- **Optically powered bio-sensing platform**

  Chapter 6 discusses the circuits and system level techniques for realization of an optically powered bio-sensing platform. A CMOS chip with all sensing and communication functionalities was fabricated in a 130nm CMOS process. This chip is integrated with on-board photodiodes and LED to realize a 8mm x 3.5 mm implantable subcutaneous sensor.

Chapter 2

DESIGN EQUATIONS FOR CO-DESIGN OF FBAR-CMOS OSCILLATORS

2.1 Introduction

When designing an FBAR oscillator, a circuit designer need to choose the right FBAR for the problem in hand. The following are the key FBAR parameters one need to choose

1. Area (A) - Physical area of the FBAR membrane

2. Quality factor(Q) - quantifies the losses in the FBAR stack

3. K_t^2 - Electromechanical coupling coefficient that captures the interaction between the electrical and acoustic domain

4. R_p - Effective impedance looking into the FBAR @ the parallel resonance

In this chapter we provide thumb rules and basic equations to aid the circuit designer in this selection. To achieve this, we need to model the FBAR and the oscillator. As mentioned in chapter 1, FBARs are modeled using the Modified Butterworth VanDyke (MBVD) model shown in fig.2.1. There are 6 parameters in this model.

1. Motional inductance,L_{mot} and motional capacitance C_{mot} capture the series resonance of the FBAR.

2. Plate capacitance C_{plate} models the parallel plate capacitance between the two electrodes of FBAR.

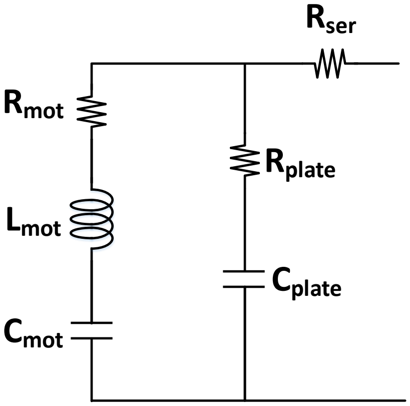


Figure 2.1: MBVD model for FBAR

3. L_{mot} together with C_{eff} (effective capacitance formed by adding in C_{mot} series with C_{plate}) captures the parallel resonance of the FBAR.

4. R_{mot} and R_{plate} model the acoustic losses in the resonator stack.

5. R_{ser} captures the series resistance in the electrode connections to the pads

Typically S11 parameters are measured for FBARs and the MBVD parameters are obtained though curve fitting [24]. We can write the following equations relating the FBAR parameters and the MBVD model parameters.

$$Series\,resonance\,frequency,\; f_s = \frac{1}{2\pi\sqrt{L_{mot}C_{mot}}} \tag{2.1}$$

$$Parallel\,resonance\,frequency,\; f_p = \frac{1}{2\pi\sqrt{L_{mot}\frac{C_{mot}C_{plate}}{C_{mot}+C_{plate}}}} \tag{2.2}$$

$$k_t{}^2 \approx \frac{\pi^2}{8}\frac{C_{mot}}{C_{plate}} \tag{2.3}$$

$$C_{plate} = A \times C_0\, where\, C_0 \,=\, plate\, capacitance\, per\, unit\, area \tag{2.4}$$

$$Impedance\,, Z_0 = \frac{1}{2\pi f_s C_{plate}} \tag{2.5}$$

The resistances are typically fitted to account for the measured S11 parameters. The loading from the CMOS oscillator is modelled using a capacitance in parallel with the FBAR as shown in figure. 2.2. We assume that the resisitve loading from the CMOS circuit is negligible compared to the R_p.

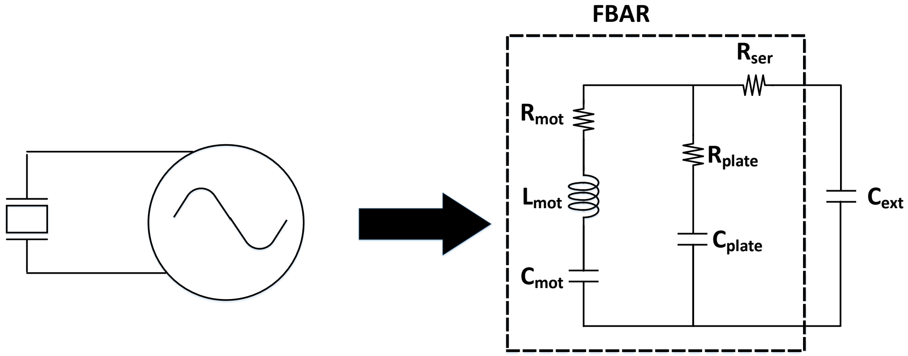


Figure 2.2: Model used to analysis oscillator tank

2.2 FBAR CMOS co-design

Depending on the problem in hand, a circuit designer might be optimizing for 4 metrics.

1. Phase noise in $\frac{1}{f^2}$ region
2. Phase noise in $\frac{1}{f^3}$ region(Close-in phase noise)
3. Oscillator power consumption
4. Tuning range

The subsequent subsections describes each of these scenarios in detail.

2.2.1 Phase noise in $\frac{1}{f^2}$ region

Phase noise at frequency offsets far from carrier is usually dominated by white noise from buffers following the oscillators. Phase noise in this region can be minimized by sizing up the buffers and by increasing the buffer current consumption.

Phase noise in the $\frac{1}{f^2}$ region is inversely proportional to the signal power and the square of the quality factor as given by the following equation [25]

$$L(\Delta\omega) = 10log_{10}\left\{\frac{2kT}{P_{sig}}\left(\frac{\omega_0}{2Q_{tank}\Delta\omega}\right)^2\right\} \tag{2.6}$$

Maximum signal power in an oscillator is limited by V_{dd} and can be written as.

$$P_{sig} = \frac{{V_{dd}}^2}{R_{p,tank}} \tag{2.7}$$

To minimize phase noise in $\frac{1}{f^2}$ region without any constraint on power consumption the circuit designer needs to

1. Maximize Q_{tank}

2. Minimize $R_{p,tank}$

The rest of this section tries to evaluate closed form expressions for Q_{tank} and $R_{p,tank}$ in terms of MBVD parameters. Q_{tank} and $R_{p,tank}$ are functions of oscillator loading capacitance C_{ext}. To find out the expressions for Q_{tank} we reduce the complex series parallel circuit in figure.2.2 to a series RLC circuit as shown in figure.2.3.

Using circuit theory we can write the following expressions for L_{eff},C_{eff},R_{eff}.

$$L_{eff} \approx L_{mot} \tag{2.8}$$

$$C_{eff} \approx \frac{C_{mot}(C_{ext} + C_{plate})}{C_{mot} + C_{ext} + C_{plate}} \tag{2.9}$$

$$R_{eff} \approx R_{mot} + \frac{(R_{plate}C_{plate}^2 + R_{ser}C_{ext}^2) + w^2(R_{plate}R_{ser}(R_{plate} + R_{ser})C_{plate}^2C_{ext}^2)}{(C_{plate} + C_{ext})^2 + w^2((R_{plate} + R_{ser})^2C_{plate}^2C_{ext}^2)} \tag{2.10}$$

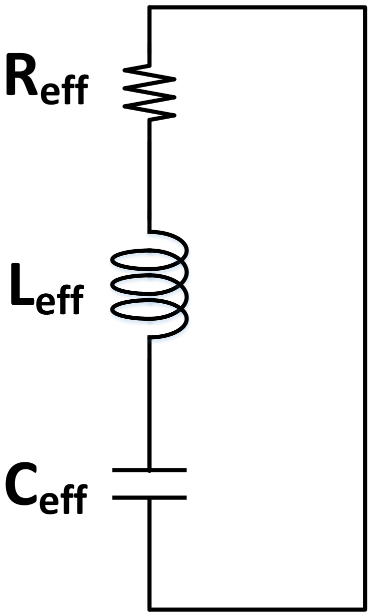


Figure 2.3: Equivalent reduction of oscillator tank

The Q of an RLC structure could be readily computed as

$$Q_{tank} = \frac{\sqrt{\left(\frac{L_{eff}}{C_{eff}}\right)}}{R_{eff}} \tag{2.11}$$

Now equations (2.8) - (2.11) together gives a closed form expression for the Q of FBAR as a function of external loading based on MBVD parameters. The oscillation frequency is

$$f_{osc} == \frac{1}{2\pi\sqrt{L_{eff}C_{eff}}} \tag{2.12}$$

To compute R_{tank} we note that R_{tank} is a manifestation of the energy lost in the tank referred across the ports of the FBAR. Let us assume all the energy loss mechanism are lumped into one equivalent resistance, R_{tank} connected across C_{ext}. Assume the input of the FBAR has a voltage signal of amplitude V_p

Then it can be shown that the energy stored in the resonator is

$$E_{stored} = \frac{1}{2}(C_{plate} + C_{ext})V_p^2 \left(1 + \frac{C_{plate}}{C_{mot}}\right) \tag{2.13}$$

So the energy dissipated per cycle could be obtained knowing Q_{tank}.

$$E_{disspercycle} = \frac{2\pi E_{stored}}{Q_{tank}} \tag{2.14}$$

The equivalent R_p should dissipate the same amount of energy per cycle.

$$E_{diss,R_p} = \frac{V_p^2}{2fR_p} \tag{2.15}$$

equating the two energy dissipation we can get R_{tank}

$$R_{tank} = \frac{Q_{tank}C_{mot}}{w(C_{plate} + C_{ext})(C_{plate} + C_{ext} + C_{mot})} = \frac{8}{\pi^2}\frac{1}{\omega(C_{plate} + C_{ext})}Q_{tank}\ {k_t}^2{}_{eff} \tag{2.16}$$

where

$${k_t}^2{}_{eff} \approx \frac{\pi^2}{8}\frac{C_{mot}}{C_{plate} + C_{ext}} \tag{2.17}$$

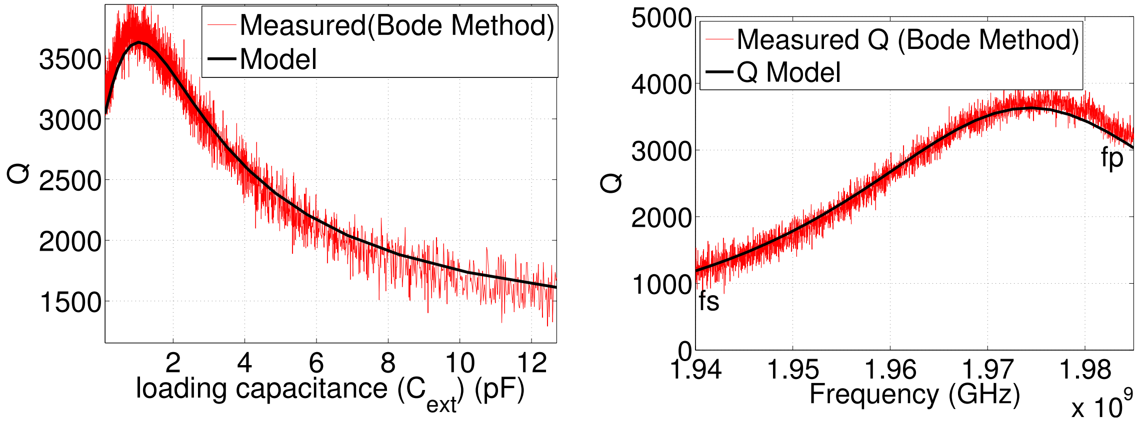
A typical plot of Q_{tank} based on this model as a function of external loading capacitance and oscillation frequency looks as shown in figure 2.4. We can see that there is an optimum loading at which the quality factor is maximum. The peak quality factor occurs at a frequency where

$$\frac{C_{ext}}{C_{plate}} = \frac{R_{plate}}{R_{ser}} = \frac{w_p^2 - w_{opt}^2}{w_{opt}^2 - w_s^2} \approx \frac{w_p - w_{opt}}{w_{opt} - w_s} \Rightarrow w_{opt} = \frac{w_p + \left(\frac{R_{plate}}{R_{ser}}\right) w_s}{1 + \frac{R_{plate}}{R_{ser}}} \tag{2.18}$$

and the magnitude of the Q at peak can be computed approximately as

$$Q_{peak} \approx \frac{\sqrt{\frac{L_{mot}}{C_{mot}}}}{R_{mot} + \frac{R_{plate}R_{ser}}{R_{plate}+R_{ser}}} \tag{2.19}$$

R_{tank} as a function of C_{ext} is shown in figure 2.5



(a)

(b)

Figure 2.4: (a) Q_{tank} as a function of Loading capacitance (b)Q_{tank} as a function of oscillation frequency

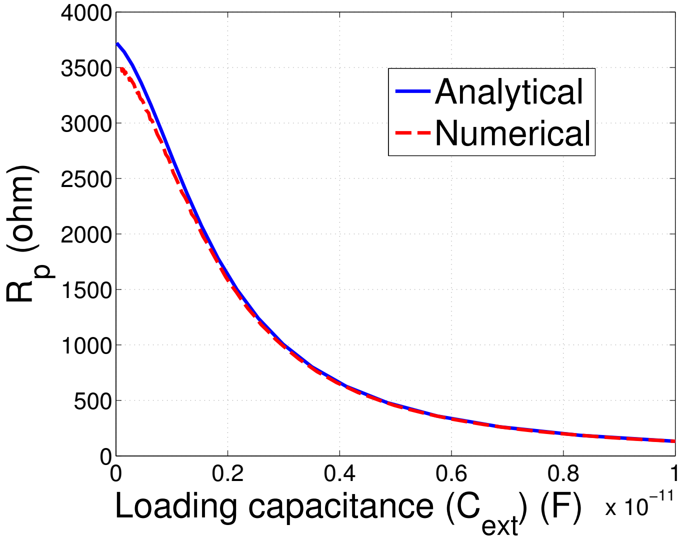


Figure 2.5: R_{tank} as a function of loading capacitance

The above analysis assumed that the external capacitance added has no losses, which is not true. We can include this loss by adding another resistance in series with Rser. If Q_{ext} is the quality factor of the external capacitive loading, it can be proved that if

$$Q_{ext} \leq \frac{1}{2R_{plate}C_{plate}\omega_p} \tag{2.20}$$

the loaded Q drops with any additional loading and the maxima for Q occurs at zero C_{ext} i.e at the parallel resonance. In such cases the designer must try to minimize the capacitive loading from the oscillator and try to operate as close as possible to fp to maximize Q.

2.2.2 Phase noise in $\frac{1}{f^3}$ region (Close- in phase noise)

This will be discussed in more detail in Chapter 3. We discuss this here briefly. We can prove that close in phase noise is propotional to the sensitivity of the oscillation frequency to the capacitive loading.

$$L(\omega) \propto \frac{\partial f}{\partial C_{ext}} = \frac{-f_{osc}}{\omega}\, {k_t}^2\, \frac{C_{plate}}{(C_{plate}+C_{ext})^2} \tag{2.21}$$

Based on the above expression, to minimize close in phase noise the designer should use an FBAR with

1. low ${k_t}^2$, and
2. high area.

2.2.3 Power consumption

In some applications with relaxed phase noise specifications, the designer might try to minimize the oscillator power consumption. From Barkhausen criteria, oscillation occurs when

$$g_m \geq \frac{\alpha}{R_{tank}}\, where\, \alpha\, =\, constant\, dependent\, on\, oscillator\, topology \tag{2.22}$$

Assuming sub-threshold MOS operation

$$\frac{g_m}{I_d} \approx 25 \tag{2.23}$$

Using Equation 2.16 and 2.23 we can write

$$P_{min} = \frac{\alpha\pi^2}{8}\frac{V_{dd,min}(C_{plate} + C_{ext})\omega}{25Q_{tank}{k_t}^2_{eff}} \tag{2.24}$$

To minimize power consumption equation 2.24 tells us that we should

1. use an FBAR with high k_t^2
2. use an FBAR with Small area
3. use an FBAR with high Q
4. Add minimum capacitive loading from the oscillator

2.2.4 Tuning range

In applications where FBAR oscillator is used as a VCO, the designer might wish to maximize the tuning range of the oscillator. FBAR looks like an inductor only at frequencies between f_s and f_p . To maximize the tuning range, separation between f_s and f_p should be maximized. We can show that

$$f_p - f_s \approx {k_t}^2 \frac{f_p}{2.4} \tag{2.25}$$

To maximize tuning range, one need to use an FBAR with high ${k_t}^2$.

2.3 Conclusion

In this chapter, basic design equations for co-design of FBAR-CMOS oscillators are given. Thumb-rules to choose an FBAR when designing with different design goals are mentioned.

Chapter 3

A 220 dB FOM, 1.9GHz OSCILLATOR USING A PHASE NOISE REDUCTION TECHNIQUE FOR HIGH-Q OSCILLATORS

3.1 Introduction

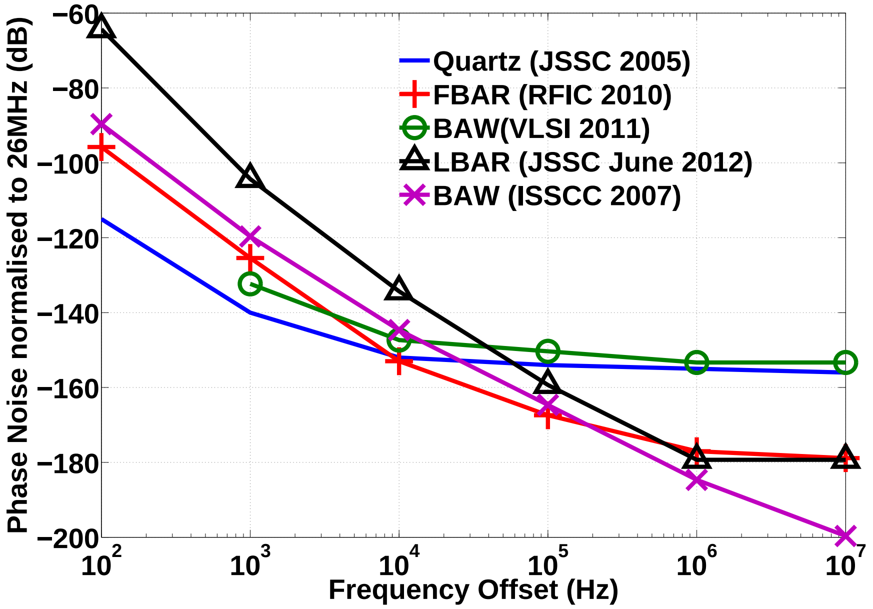


Figure 3.1: Normalized phase noise of several MEMS oscillators compared to Quartz oscillator

Close-in phase noise is an important performance metric for a reference oscillator as it dominates the in-band phase noise of a frequency synthesizer in a radio. Fig.3.1 compares published MEMS oscillators [26] [27] [28] [29] [30] with quartz oscillator showing that MEMS oscillators perform poorly compared to quartz oscillators in terms of close-in phase noise.

To successfully replace quartz references with MEMS references in all applications, advancements in close-in phase noise reduction techniques are needed,

Existing studies on close-in phase noise focus on ring oscillators and LC Oscillators [31] [25]. While Groszkowski's effect is the dominant source of close-in phase noise in LC oscillators [31], it is not the dominant mechanism in high-Q oscillators (we discuss this further in section II). So the existing phase noise reduction techniques do not directly apply to high Q MEMS oscillators. In this chapter we use an FBAR oscillator to study the close-in phase noise mechanisms of a high Q oscillator and accomplish the following.

- We show that AM-PM (amplitude modulation to phase modulation) arising from non-linear device parasitics is the dominant mechanism of close-in phase noise generation in an FBAR oscillator.

- We demonstrate that by making the oscillation frequency independent of bias current (at the operating point of the oscillator), one can suppress AM-PM conversion and reduce close-in phase noise.

- We accomplish the required AM-PM suppression by connecting a non-linear compensation capacitor across the tank.

- Measurements from a fabricated 1.9 GHz FBAR oscillator show a 4 dB reduction in close-in phase noise with no power penalty, using the proposed AM-PM suppression technique.

The proposed AM-PM suppression technique is demonstrated using an FBAR oscillator but applicable to any oscillator employing a high - Q resonator.

The chapter is organized as follows. Section II describes the proposed AM-PM suppression technique. Section III describes the circuit implementation and Section IV gives the experimental results and compares the oscillator in this work with previously published FBAR oscillators.

3.2 *Proposed AM-PM suppression technique*

We use the Pierce oscillator topology shown in Fig. 3.2 as a test vehicle for the proposed technique. One can model the oscillator as shown in Figure 2b, where the active circuitry is replaced by a capacitor and negative resistance connected across the FBAR. C_{eff} and R_{eff} are large signal parameters and are nonlinear in a typical oscillator.

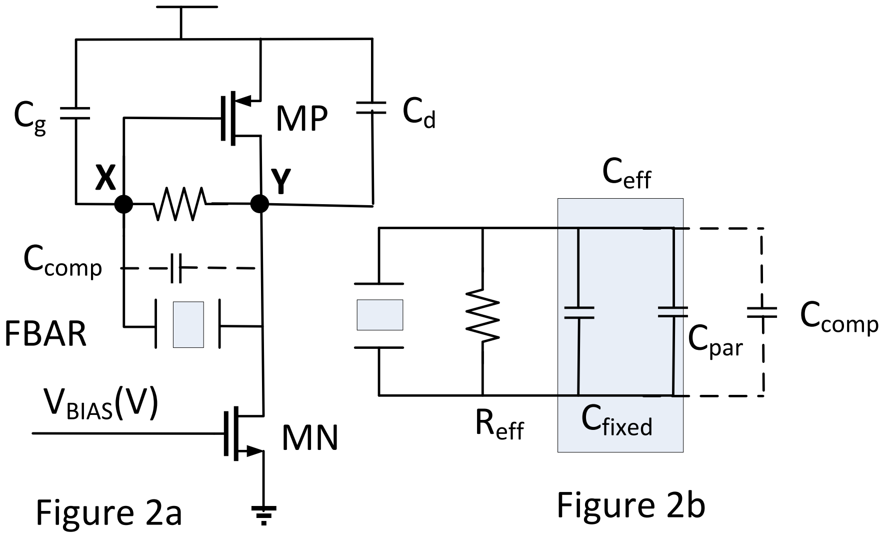


Figure 3.2: Pierce oscillator and circuit model

3.2.1 AM-PM conversion

Large voltage swings at node X and Y in Fig.3.2, which are desirable for low far-out phase noise, cause transistors MP and MN to span multiple operating regions. This makes the gate and drain parasitic capacitances non-linear, thereby making C_{eff} nonlinear. Any $\frac{1}{f}$ noise in the bias current of the oscillator modulates the oscillation amplitude (AM) and hence modulates C_{eff}. This leads to frequency modulation of the oscillator, generating phase noise. This up-conversion of $\frac{1}{f}$ noise into phase noise through capacitance non-linearity, is the well known AM-PM phase noise generation mechanism in oscillators. We can estimate the phase noise due to AM-PM conversion using the following formula [31].

$$L_{AM-PM}(\omega_m) = \frac{1}{2}\left|\frac{\partial\omega}{\partial I_{bias}}\right|^2 \frac{S_I(\omega_m)}{{\omega_m}^2} \tag{3.1}$$

Where S_I is the PSD of the noise in the bias current, ω_m is offset at which phase noise is measured, ω is the oscillation frequency and I_{bias} is the oscillator bias current. We estimate the term $\frac{\partial\omega}{\partial I_{bias}}$ from large signal periodic steady state (PSS) simulations of the Pierce oscillator and plug it in eq.(3.1). Figure.3.3 compares the total simulated phase noise of the oscillator with the phase noise estimated from eq.(3.1). We see that AM-PM conversion accounts for almost all of the phase noise at low frequency offsets, and hence is the dominant close-in phase noise generation mechanism for an FBAR oscillator. This mechanism is similar to the varactor non-linearity discussed in [32] except the non-linearity arises from device parasitics and not from explicitly added varactors.

In contrast to an FBAR oscillator, the dominant close-in phase noise mechanism in LC oscillators is the incremental Groskowzski's effect [31]. Phase noise due to incremental Groskowzski's effect is derived in [31] as

$$L_{Groszkowski}(\omega_m) \propto \frac{1}{Q^4}$$

FBAR/MEMS/Quartz resonators have more than two orders of magnitude higher Q compared to on-chip LC tanks. Hence, phase noise due to Groskowzski's effect is heavily suppressed in high-Q oscillators.

3.2.2 AM-PM suppression technique

Referring to equation(3.1), we see that $\frac{\partial\omega}{\partial I_{bias}}$ is the gain with which flicker noise gets up converted to phase noise. To suppress this AM-PM up-conversion, the designer should strive to reduce $\frac{\partial\omega}{\partial I_{bias}}$ i.e make the oscillation frequency independent of bias current around the operating point of the oscillator. We can write

$$\frac{\partial\omega}{\partial I_{bias}} = \frac{\partial\omega}{\partial C_{eff}}\frac{\partial C_{eff}}{\partial I_{bias}} \tag{3.2}$$

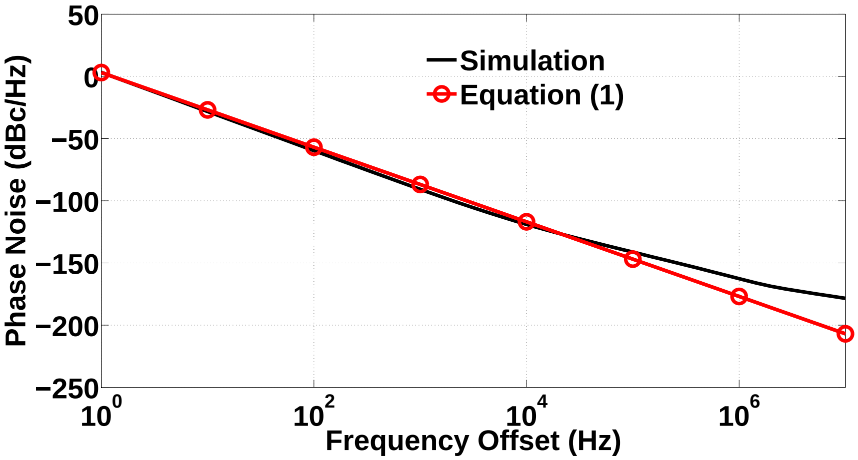


Figure 3.3: Simulated phase noise compared to equation (1)

The term $\frac{\partial\omega}{\partial C_{eff}}$ is constrained primarily by the resonator and is typically not a degree of freedom for the circuit designer. But the term $\frac{\partial C_{eff}}{\partial I_{bias}}$ can be manipulated to reduce $\frac{\partial\omega}{\partial I_{bias}}$. For the oscillator in Fig.3.2 we can write

$$C_{eff} = C_{fixed} + C_{par} \tag{3.3}$$

C_{fixed} is made of the explicitly added capacitors C_d and C_g. C_{par} is made up of parasitics of MP and MN. One can use linear MIM capacitors for C_d and C_g, thereby making C_{fixed} linear. C_{par} is typically non-linear and varies with bias conditions and voltage swing. From eq.(3.3) we can write.

$$\frac{\partial C_{eff}}{\partial I_{bias}} = \frac{\partial C_{fixed}}{\partial I_{bias}} + \frac{\partial C_{par}}{\partial I_{bias}} \approx \frac{\partial C_{par}}{\partial I_{bias}} \tag{3.4}$$

Typically, C_{par} is defined by the width and length of MP and MN, which are chosen with other considerations in mind (power consumption,far-off phase noise, oscillator swing etc). So the designer does not have any degree of freedom to reduce $\frac{\partial C_{eff}}{\partial I_{bias}}$. To provide the required additional degree of freedom to the designer, we add a compensation capacitor C_{comp}. The new effective capacitance is

$$C'_{eff} = C_{fixed} + C_{par} + C_{comp} \tag{3.5}$$

If we chose

$$\frac{\partial C_{par}}{\partial I_{bias}} = -\frac{\partial C_{comp}}{\partial I_{bias}} \tag{3.6}$$

we can write

$$\frac{\partial C'_{eff}}{\partial I_{bias}} = \frac{\partial C_{par}}{\partial I_{bias}} + \frac{\partial C_{comp}}{\partial I_{bias}} \approx 0 \implies \frac{\partial \omega}{\partial I_{bias}} \approx 0 \tag{3.7}$$

By choosing an appropriate non-linear compensation capacitor C_{comp} the designer can desensitize the oscillation frequency with respect to the bias current, thereby suppressing AM-PM conversion. In our design C_{eff} increases with the bias current and voltage swing. This increase in capacitance is primarily caused by the increase in drain-bulk diode capacitance of MN. So we choose a C_{comp}, made up of zero-VT NMOS transistors shown in Figure.3.4. C_{comp} decreases with increasing oscillation amplitude, cancelling the increase in C_{par}. We size the NMOS transistors in Fig.3.4 to satisfy eq.(3.6).

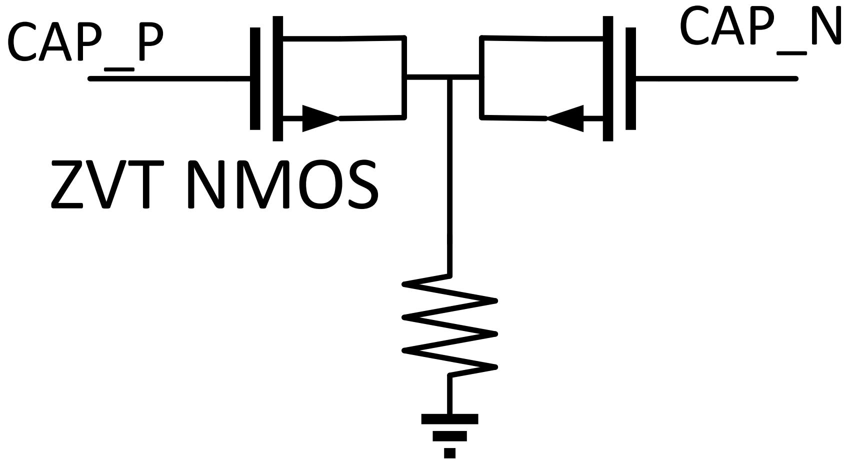


Figure 3.4: Non Linear Compensation capacitor

Fig. 3.5 plots simulated C_{eff}, C'_{eff} and the compensation capacitance,C_{comp} as a function of bias current. In Fig. 3.5 the mean value of the capacitances are subtracted out to bring out the compensation more clearly. We see that the slope of C'_{eff} is much smaller than that of C_{eff}. With a reduced $\frac{\partial C'_{eff}}{\partial I_{bias}}$ we see a suppression in the simulated close-in phase noise. Fig.3.6 shows the achieved close-in phase noise suppression in simulation.

It may appear that a simple reduction in flicker noise in the bias path will reduce close-in phase noise, obviating the proposed scheme. This is not the case, and it should be noted that the proposed scheme is complementary to flicker noise reduction in the bias circuit. Referring to eq.(3.1), the proposed scheme reduce $\frac{\partial \omega}{\partial I_{bias}}$, while one can independently reduce the bias noise S_I. In fact, for a given target phase noise, the proposed technique simplifies the bias circuit design, by relaxing its noise specification.

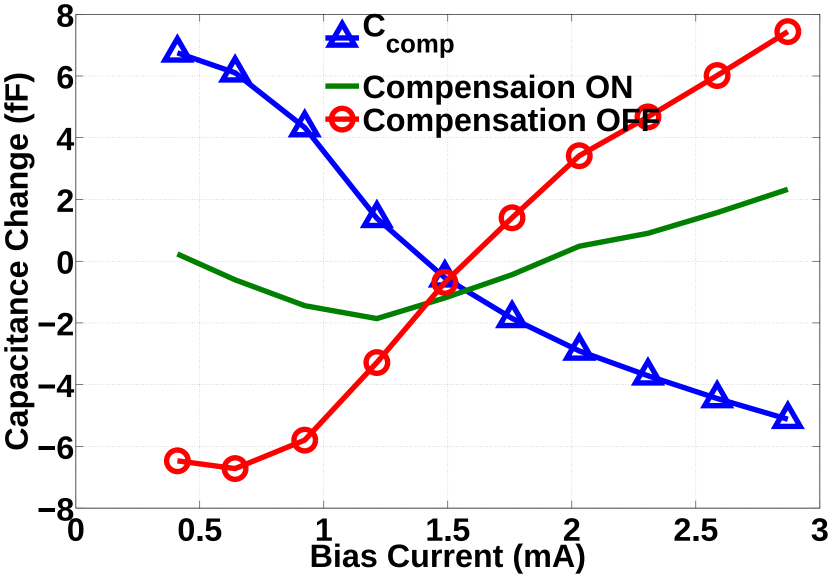


Figure 3.5: Effective capacitance of the circuit with compensation

3.3 Circuit Implementation

To experimentally verify our AM-PM suppression technique, we fabricated the test circuit shown in Fig.3.7. MP1 and MN1 form a Pierce oscillator. The compensation capacitor is made of two zero VT NMOS sized $\frac{27\mu m}{0.42\mu m}$. The mean value of C_{comp} is 60 fF. A digital control D_{comp} selects either C_{comp} or C_{MIM}, a linear 60fF MIM capacitor to be connected across the

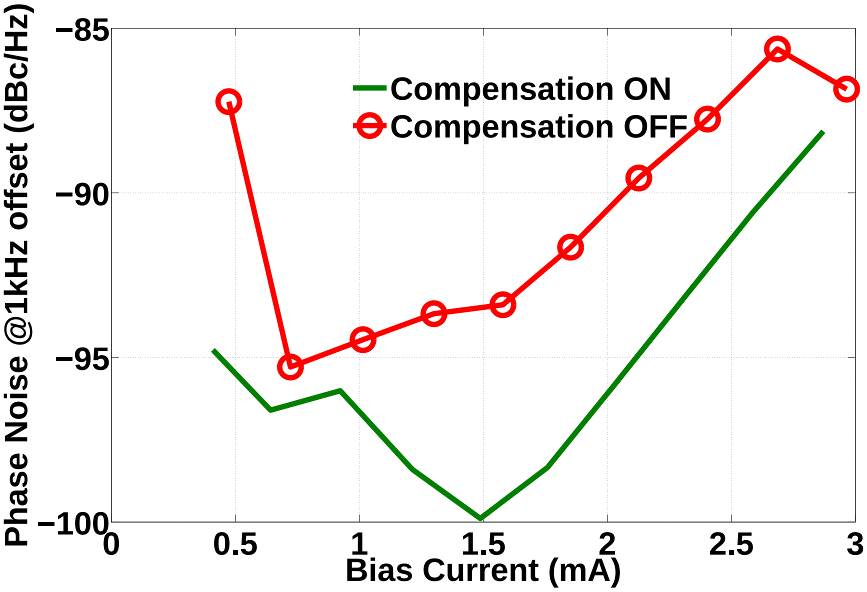


Figure 3.6: Simulated Phase noise suppression

FBAR. This enables us to turn the compensation ON and OFF, without affecting the total tank capacitance and other oscillator parameters.

A digitally programmable bias circuit controlled by D_{BIAS} biases MN1, providing an experimental knob to vary the current through the oscillator. The oscillator is followed by a multi-stage buffer made of transistors MN2-MN6, MP2-MP3 and multiple CMOS inverters to square up the signal. The last stage is an open drain buffer feeding the output pads. The oscillator core occupies an area of 250μm x 100μm. The oscillator nominally operates at a V_{dd} of 1.2V and consumes a bias current of 1.3mA.

3.4 Experimental Results

The oscillator circuit was fabricated in 0.13 μm IBM CMOS 8RF process. The CMOS oscillator is wire bonded to an 1.9GHz FBAR from Avago Technologies. Fig. 3.8 shows the board assembly of the CMOS oscillator and FBAR.

To experimentally verify whether the proposed compensation reduces the term $\frac{\partial \omega}{\partial I_{bias}}$, we

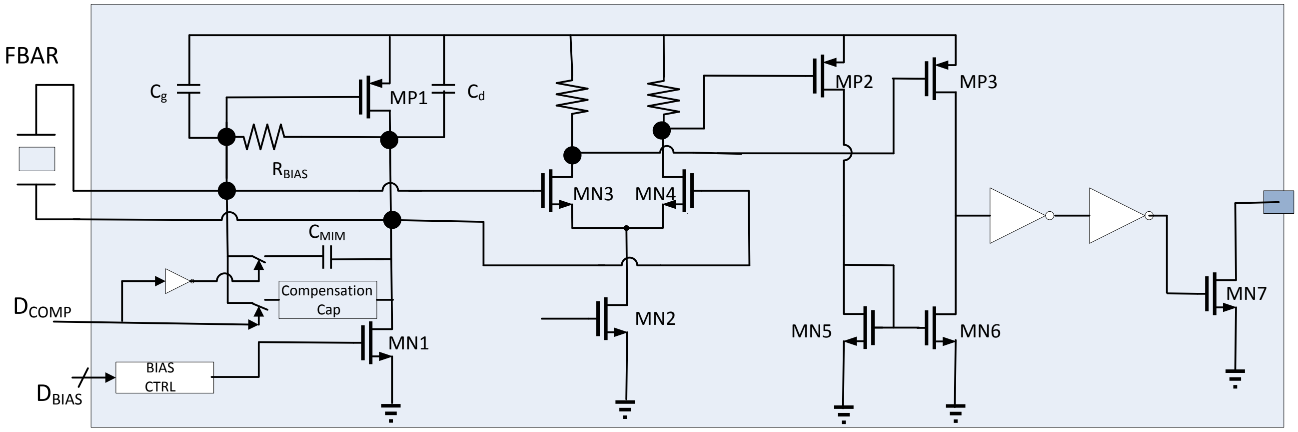


Figure 3.7: Fabricated Oscillator Circuit

measure the oscillation frequency across bias currents, with and without the compensation. Fig.3.9 shows that the oscillation frequency becomes 2.7X less sensitive to the bias current, when the compensation is turned on.

Fig. 3.10 shows the measured phase noise with and without the AM-PM suppression. Turning the compensation on reduces the close-in phase noise by 4 dB while retaining the far-off phase noise at the same value. We measured the phase noise performance of the oscillator on 4 different dies. We consistently observed a $\geq$ 3.5dB reduction in phase noise in all 4 dies using the proposed technique.

While a 2.7X reduction in $\frac{\partial\omega}{\partial I_{bias}}$ must correspond to 8dB reduction in phase noise, we measure only a 4 dB reduction. This indicates that the presence of phase noise from another mechanism at 7dB lower than the dominant AM-PM mechanism. This mechanism becomes the next dominant source of phase noise once the AM-PM up-conversion is suppressed by 8 dB. Further experimental work is required to identify and address this mechanism.

Figure 3.11 shows the screen shot of the measured phase noise of the oscillator at a Vdd of 1.2 V and bias current of 1.3mA. With the compensation turned on, we achieve a phase noise of -88 dBc/Hz at 1kHz, -116.3 dBc/Hz at 10 kHz and a noise floor of -146 dBc/Hz.

In Table.3.1 we compare the proposed oscillator with other previously published FBAR

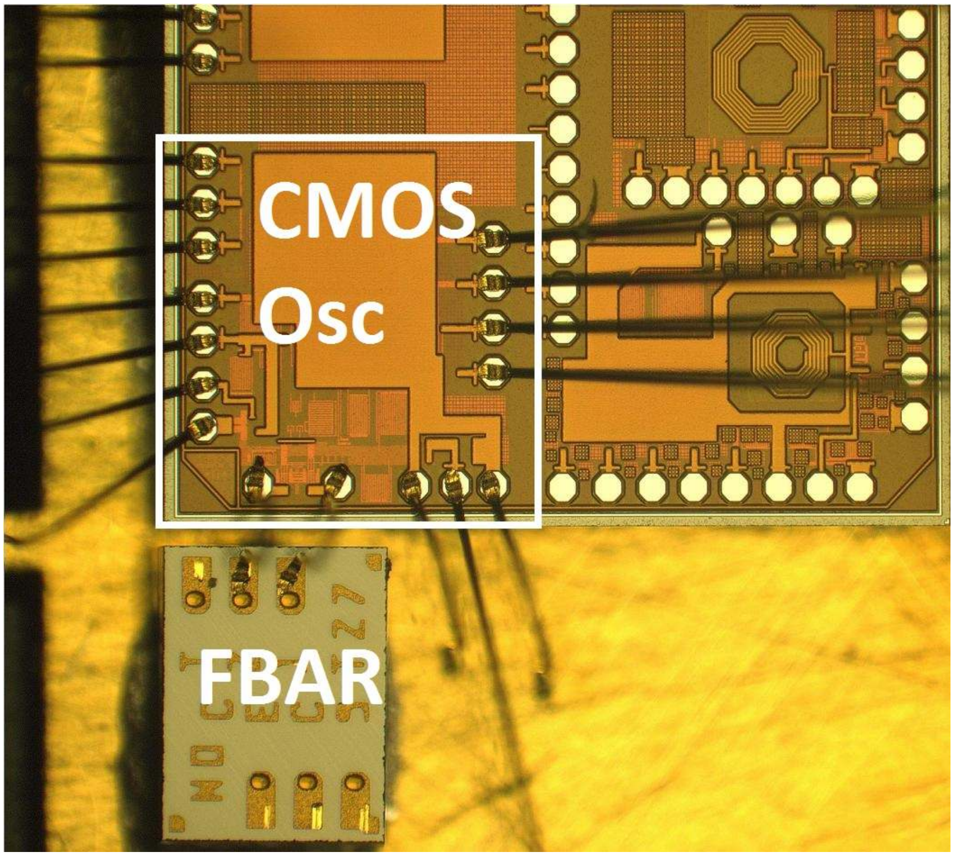


Figure 3.8: Board assembly with FBAR and CMOS oscillator

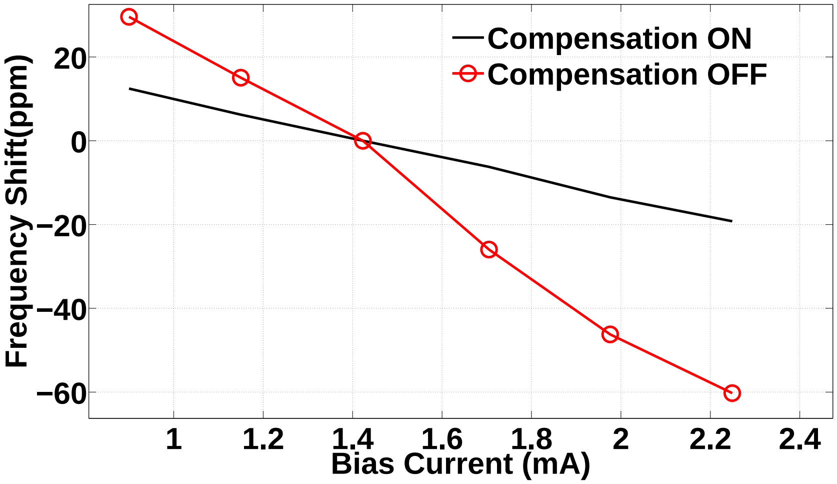


Figure 3.9: Sensitivity of oscillator frequency to the bias current

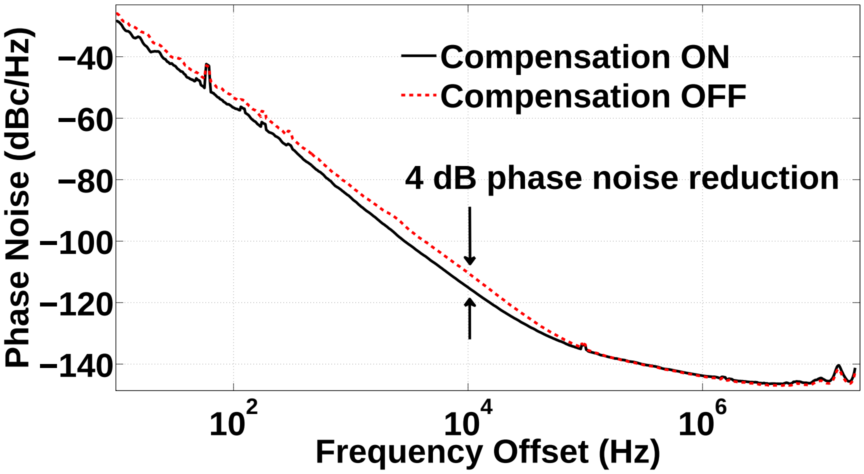
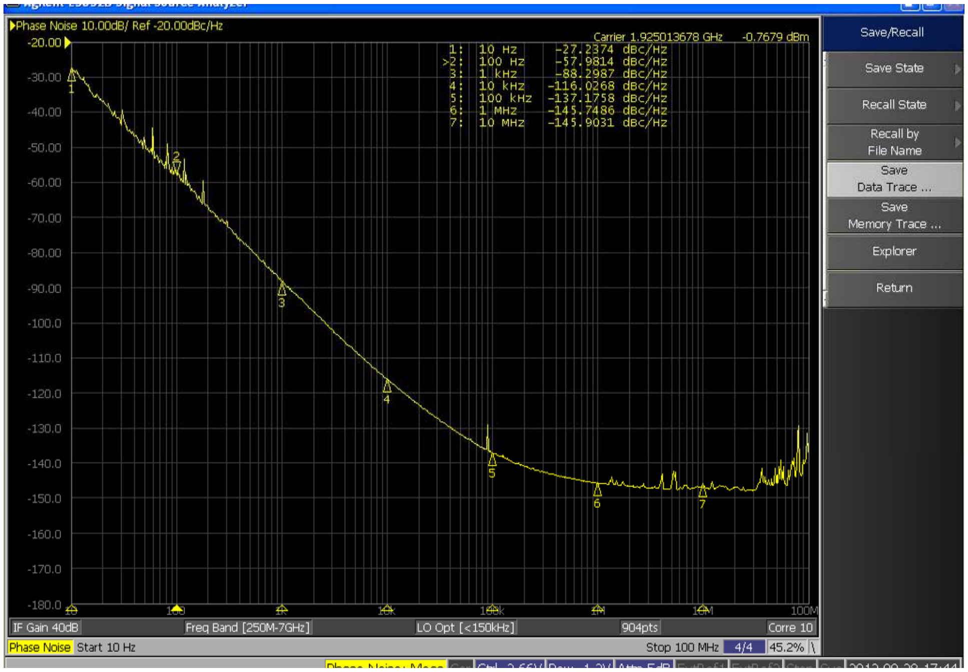


Figure 3.10: Measured phase noise suppression using proposed technique



```
Carrier 1.925013678 GHz    -0.7679 dBm
 1:  10 Hz      -27.2374 dBc/Hz
>2:  100 Hz     -57.9814 dBc/Hz
 3:  1 kHz      -88.2987 dBc/Hz
 4:  10 kHz    -116.0268 dBc/Hz
 5:  100 kHz   -137.1758 dBc/Hz
 6:  1 MHz     -145.7486 dBc/Hz
 7:  10 MHz    -145.9031 dBc/Hz
```

```
IF Gain 40dB    Freq Band [250M-7GHz]    LO Opt [<150kHz]    904pts    Corre 10
Phase Noise  Start 10 Hz                         Stop 100 MHz  4/4  45.2%
```

Figure 3.11: Measured phase noise of the oscillator

oscillators [16] [33] [34] [27] [30]. [27].

The Figure Of Merit (FOM) is computed at 10kHz offset as this study focused on close-in-phase noise. We see that the proposed technique enables the oscillator to achieve an FOM of 220dB, which is 5.5 dB better than the FBAR oscillator with the lowest close-in phase noise reported to date. The oscillator in [16] achieves a 2 dB better FOM than this oscillator. However [16] achieves this FOM by drastically trading off phase noise for an ultra low power consumption, while this work achieves a comparable FOM by improving the phase noise using the AM-PM suppression technique.

3.5 Conclusion

This work experimentally confirms that the dominant source of close-in phase noise in high-Q FBAR oscillators is the AM-PM up-conversion arising from non-linear device parasitics. A non-linear compensation capacitor added across the tank improves phase noise by $\geq$ 3.5

Table 3.1: Performance Comparison

Ref	f_{osc}	Power	PN 1kHz	PN 10kHz	FOM 10kHz
	GHz	mW	dBc/Hz	dBc/Hz	dB
This Work	**1.925**	**1.6**	**-88.3**	**-116.0**	**219.6**
[34]	1.9	0.3	-75	-100	210.8
[27]	0.6	5.6	-96	-126	214
[16]	2.0	0.025	-76	-100	222
[33]	1.9	0.089	NA	-98	214
[30]	2.0	12	-70	-100	195.8

dB. The proposed compensation technique enables the 1.9 GHz FBAR oscillator to achieve a phase noise of -88dBc/Hz at 1kHz and an FOM of 220 dB.

Chapter 4

FBAR BASED QUARTZ REPLACEMENT - PROTOTYPE - I

4.1 Introduction

Resonant frequency of FBAR decreases with temperature due to negative temperature coefficient of material properties of AlN and Molybdenum. This linear temperature coefficient of ~-30 $\frac{ppm}{C}$ can be zeroed out by adding SiO_2 of an appropriate thickness into the FBAR stack [35]. An FBAR compensated mechanically by adding an oxide layer is known as 'Zero Drift Resonator' (ZDR) and has a quadratic temperature vs frequency characteristic.

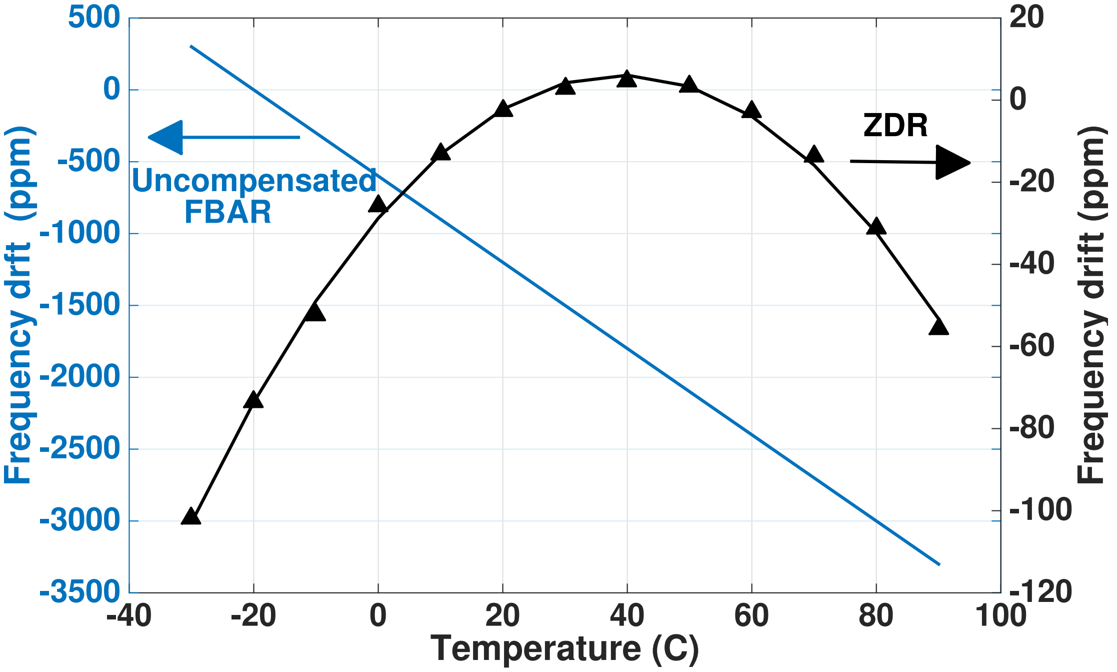


Figure 4.1: Temperature vs frequency of an uncompensated FBAR and a ZDR

Figure. 4.1 shows the frequency drift of an uncompensated resonator and the residual quadratic after mechanical compensation. In a ZDR, Turn Over Temperature (TOT) is the temperature at which the frequency attains a maximum value. The temperature response of a ZDR can be fitted with the following quadratic expression

$$f(T) = f(TOT) - \beta(T - TOT)^2 \tag{4.1}$$

TOT is not a well controlled parameter and can vary from -20°C to 100°C across process. Typical values of β are between 15 and 20 $\frac{ppb}{C^2}$. Resonant frequency of a ZDR drifts by about 100 to 150 ppm from -20 to 90°C. This drift together with frequency drift from aging and process variations, is insufficient to meet the frequency tolerance required by several wireless standards shown in table 4.1.

Table 4.1: Frequency stability requirements

Wireless Standard	Frequency stability needed
Zigbee	±40
Bluetooth	±60
WLAN	±20
GSM/WCDMA	±5
GPS	±1

One way to improve the frequency stability of a ZDR is to build an electronic temperature compensation circuitry which senses the ambient temperature and corrects the FBAR frequency. This chapter discusses the challenges in electronically compensating a ZDR and the circuits built to achieve an FBAR based quartz replacement (The terms FBAR and ZDR are used interchangeably in this chapter, but they always refer to a ZDR). A brief review of temperature compensation architectures and state of the art MEMS based quartz replacements are discussed in the first two sections. The next section describe a 65nm CMOS chip (prototype - I) built to develop an FBAR based quartz replacement. This prototype achieves a ±20 ppm stability from -10 to 90°C. Measurements from this run are used to guide the design of a second prototype (Prototype - II) . This prototype includes a temperature sensor that operates from a 0.75V supply, the lowest reported in literature so far. This prototype achieves a stability of ± 3 ppm from 0 to 90°C and consume 1.1 mW and is discussed in the next chapter.

4.2 Specifications

This section discusses the specifications for a quartz replacement in the context of radio transmitters and receivers.

4.2.1 Temperature stability

Table 4.1 mentions the temperature stability required by several radio standards [21]. Zigbee and Bluetooth are the most common standards used in wireless sensors and need ±40-60 ppm frequency stability. After accounting for aging we need ±20 ppm stability across temperature. To be competitive with quartz crystals used for similar applications we need to target ± 5 ppm stability across temperature.

4.2.2 phase noise

Phase noise is an important metric for a local oscillator in a radio and measures the short term frequency stability of the reference. In a radio receiver, phase noise increases noise figure by reciprocal mixing of interferers. In a transmitter phase noise increases the out-of-band noise floor. Phase noise requirements for radios are derived from blocker and spectral mask specifications. FBAR oscillators usually far exceeds the phase noise requirements of a radio receiver. For example, ZigBee standard requires a far phase noise specification of -88 dBc/Hz at 1 MHz offset at 2.4 GHz carrier frequency [36]. Phase noise of an FBAR oscillator without electronic temperature compensation exceeds this requirement by a factor of $\geq$ 40 dB. Noise from the temperature compensation circuitry must be designed to be lower than the phase noise of the oscillator.

4.2.3 Allan deviation

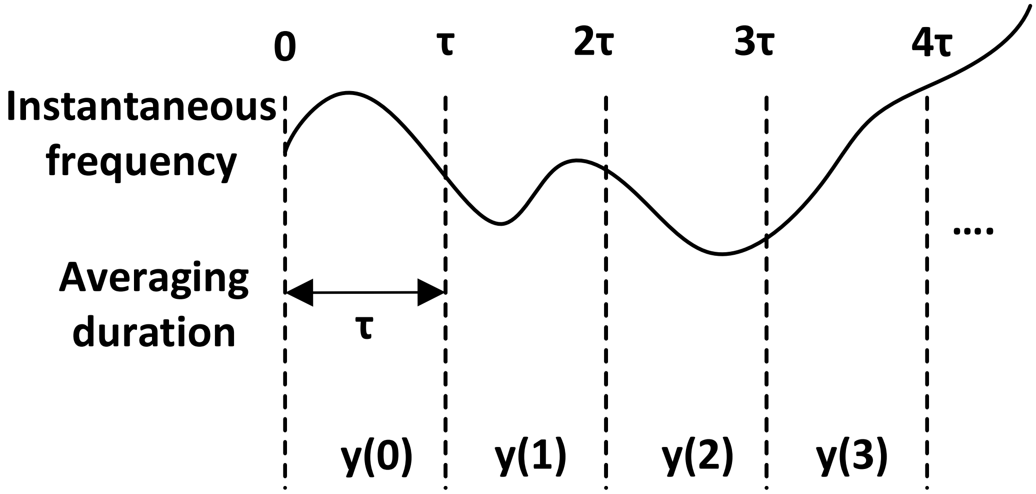


Figure 4.2: Illustration of Allan deviation measurement

Allan deviation is a time domain metric of the frequency stability of an oscillator. Frequency of an oscillator moves stochastically as illustrated in figure 4.2. Traditional variance measurement of a stochastic oscillator diverges with time and does not provide a meaningful metric of frequency stability. David. W Allan introduced the 2 sample variance in [37]. Assume we measure average oscillation frequency over an time interval τ (called as stride). Standard deviation of the difference between two successive measurements is called Allan deviation. This can be mathematically expressed as

$$\sigma_y(\tau) = \left[\frac{1}{2M}\sum_{0}^{M-1}(y(i+1) - y(i))^2\right]^{\frac{1}{2}} \tag{4.2}$$

where y(i) is the average measured frequency in the time interval [iτ (i+1)τ]. Allan deviation can also be computed from phase noise of an oscillator. It is usually plotted as a function of τ in a log-log plot as shown in figure 4.3. For quartz replacements, MEMS oscillators need to have an Allan deviation of $\leq$ 5 ppb. [11]. FBAR oscillators without electronic compensation have allan deviations about 1 - 2 ppb [38]. Noise from temperature compensation circuitry must be designed such that the Allan deviation does not degrade more than 5 ppb.

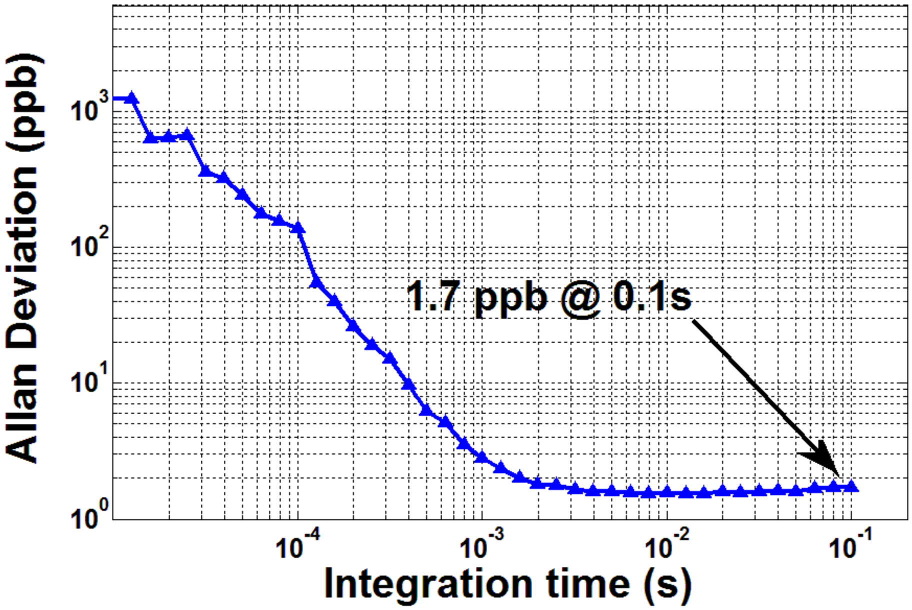


Figure 4.3: Example allan deviation plot

4.2.4 Supply voltage and power consumption

Radio in a wireless sensor node is usually powered from harvested energy. Output voltage of harvesting methodologies are usually $\leq$ 1V. For example, on-chip solar cells allow only a 200 mV to 900 mV supply; thermoelectric generators have output voltages of 50-300 mV. Although boost converters can be employed, their efficiency suffers when high conversion

ratios are needed. For this work, we target a supply voltage of 0.75V which can generated by a 2X or 3X boost converter. Choice of this voltage was primarily influenced by the availability of 0.75V models for digital standard cells in the 65nm process.
We target a power consumption ≤ 1 mW to enable low power radios for wireless sensor nodes.

4.3 State of the art temperature compensation schemes

Electronic temperature compensation of frequency references is not a new issue. It has been explored for Quartz and other MEMS devices in the past. AT cut quartz crystals have a ± 5-10 ppm (See figure 4.4)frequency drift over temperature which is insufficient for applications such as GPS. Electronic temperature compensation is used to improve the frequency accuracy to ≤ ± 0.5 ppm [39] [40] [41]. [40] uses a 12 bit SAR ADC and reduce the temperature drift from +/-3.5ppm to +/- 0.5ppm over -10 to 80C. [39] starts with a

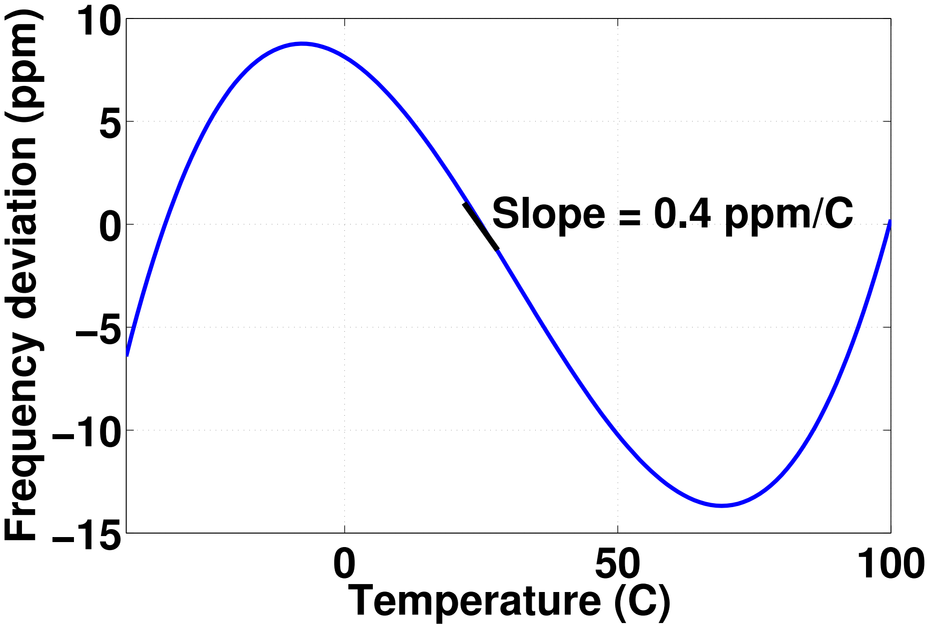


Figure 4.4: AT Cut quart temperature stability

frequency drift of +/- 4 ppm and uses a 10 bit temperature sensor to achieve a +/- 1.5ppm frequency stability. These architectures can be used to compensate the temperature drift of an FBAR oscillator [14], but lead to a heavy phase noise degradation if the noise from the temperature sensor is high.

Recently temperature compensated MEMS based frequency references have been proposed [11]. [11] achieves a +/- 0.5ppm stability with a 10 point calibration, but consumes a 100 mW of power due to the use of analog PLLs. Such high power makes the solution unusable for many radio applications. While 1uA, 32 KHz PLL have been demonstrated [12], the phase noise of such clocks will be decided by the VCO of the PLL and will be very poor compared to the native phase noise of the MEMS oscillator.

Another popular architecture used for temperature compensation is using a heater and an oven to stabilize the temperature of the resonator [13] [42] . These solutions achieve sub-ppm stability but is power hungry due to the heating requirement.

Summarizing, a sub mW, sub mm^3 reference clock with suitable performance for radio applications has never been demonstrated in literature .

4.4 Architecture evaluation

This section explores three different temperature compensation architectures reported in the literature. Benefits and challenges of each of these architectures are discussed and the most suitable scheme for an FBAR based quartz replacement is identified.

4.4.1 Architecture I

Figure 4.5 shows the architecture used in [40].

A thermistor on the same package as the quartz crystal measures the ambient temperature. This information is digitized using a 12 bit SAR ADC. A lookup table (LUT) is used to find an appropriate correction code which is used to pull a digitally controlled oscillator (DCO) to a target frequency. The DCO is realized by adding a digitally controlled cap array as part of the oscillator tank. In principle, the DCO can be replaced with a VCO as in [41].

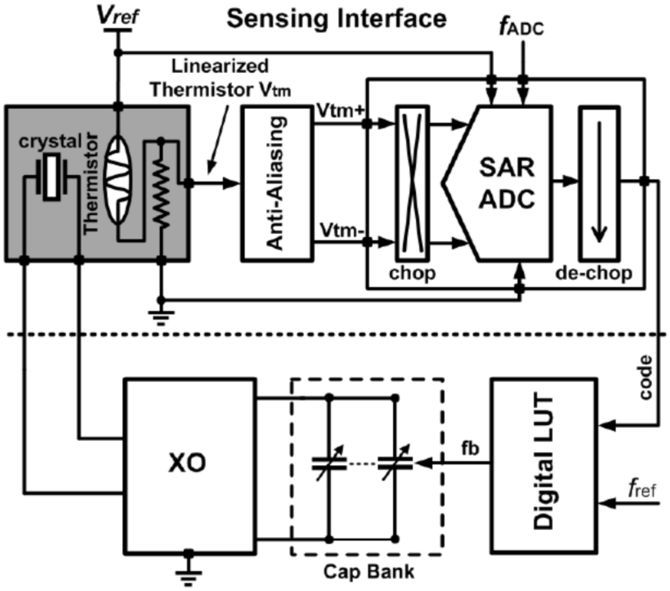


Figure 4.5: Temperature compensation of quartz oscillators

This enables a continuous frequency tuning with no abrupt frequency jumps as in the digital case. But, adding a varactor introduces a non linear capacitor in the tank and degrades the close-in phase noise significantly due to AM-PM conversion as described in Chapter 3. A digital cap array can use highly linear MIM capacitors and can avoid this issue altogether. Further, in modern CMOS processes, digitally controlled cap arrays provide a 2-3X higher tuning range than analog varactors making them a better choice.Temperature sensing can also be done in the analog domain. But the look up table will have to be replaced by complicated analog polynomial generation circuits. Maintaining an adequate noise floor at the varactor input becomes hard with several analog computations in the signal chain. Moreover, a highly digital architecture is preferable in scaled CMOS process and has potential for sub 1V operation.

frequency tuning requirements

This architecture needs an oscillator pulling range greater than the temperature drift. Quartz oscillators with a pulling range ∼50 ppm meets this requirement easily. FBARs can be easily tuned $\geq$ 1000 ppm with the highest reported tuning range of $\geq$7000 ppm. [43].

In a digital cap array the frequency jumps abruptly when the control code changes. This could lead to a huge phase noise degradation. The effect of abrupt frequency jumps can be avoided by making the unit frequency step smaller than the oscillator noise floor, i.e Allan deviation. Minimum feature size and mismatch criteria in 65nm TSMC process limit minimum achievable unit capacitor size and frequency step. Finer resolutions can be achieved by using $\Delta - \Sigma$ dithering of the unit capacitors. As an example, the DCO in [26] achieves a raw frequency step of 70 ppb. A first order $\Delta - \Sigma$ modulator is used to improve the frequency resolution from 70 ppb to 4 ppb. Further, the oscillator tuning curve needs to be monotonous, so that the oscillator is tuned smoothly during a temperature ramp. This can be achieved by using a thermometric capacitor array.

Temperature sensor requirements

Ambient temperature variations are slow and a low bandwidth of about 10 Hz is sufficient of the temperature sensor [11].

Noise from the temperature sensor modulates the DCO frequency and causes increased Allan deviation. Resolution of a temperature sensor is the minimum detectable temperature variation and is equal to the RMS value of noise integrated in the bandwidth of interest. The required resolution can be computed by using the following relation

$$T_{n,rms} \leq \frac{Allan\ deviation}{\frac{\partial f}{\partial T}} \tag{4.3}$$

For a quartz crystal $\frac{\partial f}{\partial T}$ is about 0.4 $\frac{ppm}{C}$. For a 0.1s stride Allan deviation of 5 ppb, integrated noise in a 5 Hz bandwidth should be less than

$$T_{n,rms,Quartz} \leq \frac{Allan\ deviation}{\frac{\partial f}{\partial T}} = \frac{5}{0.4} = 12.5mK \tag{4.4}$$

Assuming an FBAR with $\beta = 15ppb$ and TOT $=$ 90C and a temperature range of 0 to 90C, the maximum value of $\frac{\partial f}{\partial T}$ can be computed using the equation.

$$\frac{\partial f}{\partial T}_{max} = 2\beta(T - TOT) = 2.7\frac{ppm}{C} \tag{4.5}$$

For a 0.1s stride Allan deviation of 5 ppb, integrated noise in a 5 Hz bandwidth should be less than

$$T_{n,rms} \leq \frac{Allan\ deviation}{\frac{\partial f}{\partial T}} = \frac{5}{2.7} = 1.85mK \tag{4.6}$$

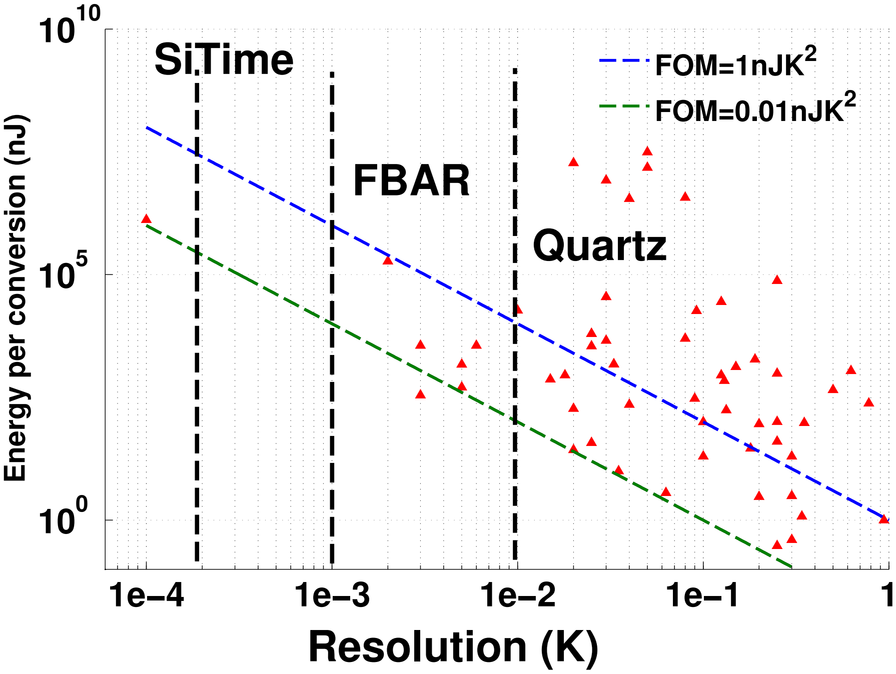


Figure 4.6: Temperature sensors - state of the art

For CMOS temperature sensors, 1.85 mK is a tough specification to achieve. Figure 4.6 shows all published state of the art temperature sensors with data collected from the smart temperature sensor survey of Prof. Makinwa [44]. Several temperature sensors that exceed the resolution required by Quartz crystals are found in the literature. [11] is the only architecture that achieves a $\leq$ 1mK resolution required by FBARs, but this temperature sensor architecture is power hungry and consumes $\geq$ 10 mW of power in 180nm process. This sensor is described in detail later in this chapter.

Building a temperature sensor with resolution $\leq$ 1.85 mK with a power budget of $\leq$ 100 uW is the key challenge in adopting architecture-I for FBAR temperature compensation.

Calibration requirements

Architecture-I corrects for temperature drift in a feed forward manner, i.e it assumes a predefined polynomial relationship between temperature and frequency. This necessitates a one-time calibration to determine the coefficients required for polynomial correction. For Quartz, a minimum of 4 point calibration is needed to correct for the cubic temperature dependence. In practice, more coefficients are used to achieve better accuracy. For FBARs with a quadratic temperature dependence, a minimum of 3 point calibration is needed. In commercial production, calibration increases test time and cost as the frequency of each sample needs to be measured at multiple temperatures.

4.4.2 Architecture - II

Some MEMS resonators have a pulling range less than the temperature drift. For example, oscillators in [45] and [11],has a pulling range of $\leq$ 20ppm and a temperature drift of 100ppm and 3000 ppm respectively.

In such cases architecture-I cannot be used to compensate the MEMS oscillator. Temperature correction can be achieved by feeding an appropriate correction code into a fractional-N PLL referenced to the MEMS oscillator. Figure 4.7 shows the temperature compensation architecture used in [11]. The division ratio in the feedback path is a convenient point in loop for adding the temperature correction. The required correction can be computed as

$$N_{correction}(T) = \frac{f_{target}}{f_{MEMS(T)}} \tag{4.7}$$

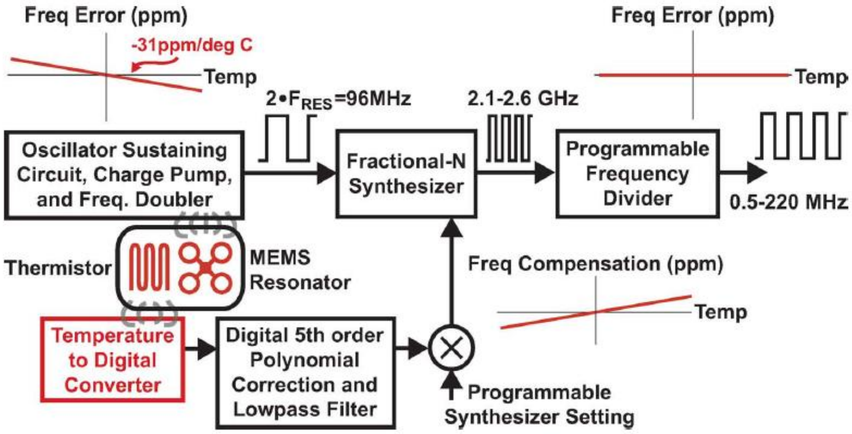


Figure 4.7: Temperature compensation architecture used in [11]

advantages

The PLL in architecture-II can be programmed to give a wide range of output frequencies by changing the feedback division ratio. The MEMS resonator can be optimized to operate at a single frequency and the output can be tuned over a wide range, achieving a programmable frequency reference. Commercially, this reduces the lead time for the product as the system can be fabricated earlier and programmed to a particular output frequency once the customer specifies the desired output frequency. SiTime products have a lead time of $\leq$ 3-5 weeks in contrast to the 8-16 weeks lead time for Quartz oscillators. (See http://www.sitime.com/technology/crystal-oscillators).

disadvantages

The main disadvantage of this architecture is high power consumption, primarily because of the PLL. For example, the frequency reference in [11] consumes $\sim$ 100 mW with $\geq$ 48 mW being consumed by the PLL. One can argue that the temperature compensation can be added to the frequency synthesis PLL already available in most radios. But, PLL-free radios have been recently demonstrated and are more power efficient than PLL-based frequency synthesis. [10]

As FBARs have sufficient pulling range to correct for the temperature drift, a PLL is unnecessary for frequency correction. This makes architecture - II unattractive for an FBAR based frequency reference.

4.4.3 Architecture - III

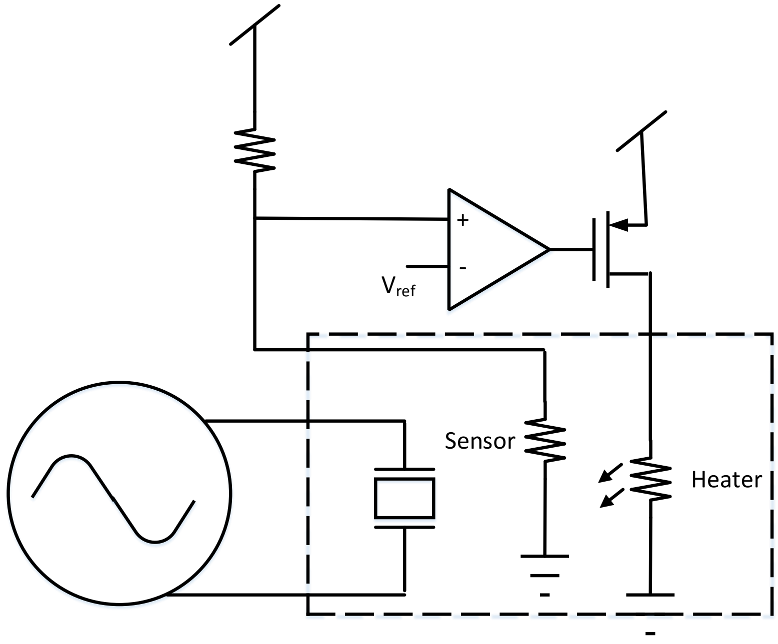


Figure 4.8: Heater based temperature compensation

In cases where a heater and temperature sensor can be assembled in the same package as the resonator, architecture shown in figure 4.8 becomes viable. In this architecture, the temperature of the resonator is sensed via a sensing resistor. A feedback circuit senses the value of this resistor and heats up the resonator till the temperature reaches a target temperature. The target temperature is usually chosen to be the greater than the maximum ambient temperature specification. This scheme has been reported in [13] [42] .

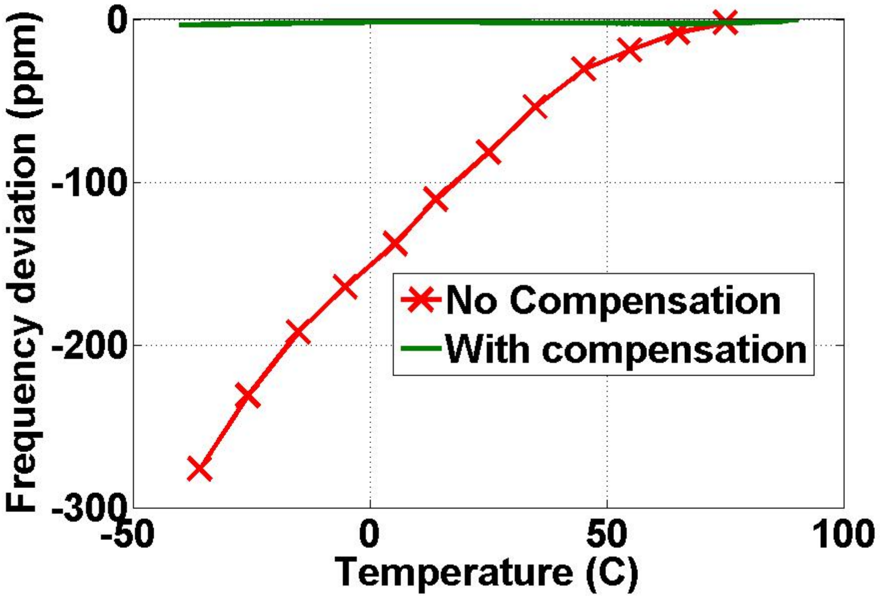


Figure 4.9: FBAR oscillation frequency with heater based compensation

Such an implementation is also possible for FBARs. Figure 4.9 shows an FBAR oscillator frequency drift with and without the heater based feedback control. Figure. 4.10 shows that the frequency drift is reduced to less than 2 ppm with the heater turned on. Figure 4.11 shows the power consumed by the heater across temperatures. At low temperatures the heater consumes $\geq$ 10 mW to heat up the resonator. High power consumption prevents one from using this architecture for low power radio applications.

4.4.4 Architecture selection

Of the three architecture described above, architecture-I is the only viable option for low power applications. We developed two prototypes in TSMC 65nm process based on this architecture. The biggest challenge in using this architecture for FBAR oscillators is designing

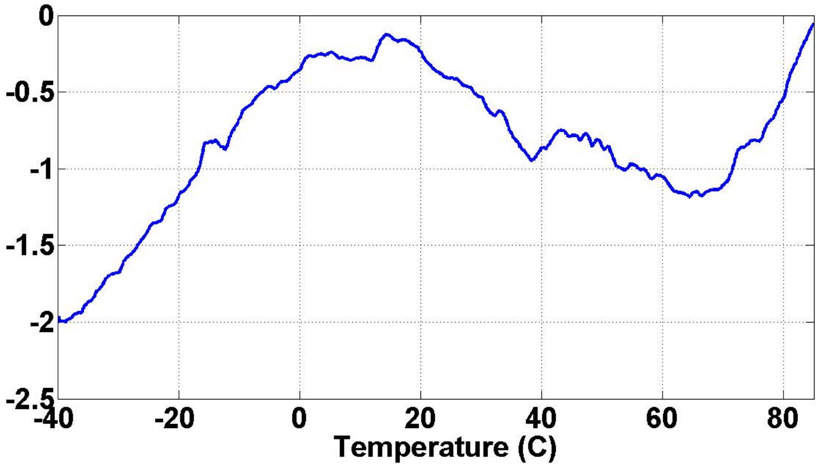


Figure 4.10: FBAR oscillation frequency with heater based compensation

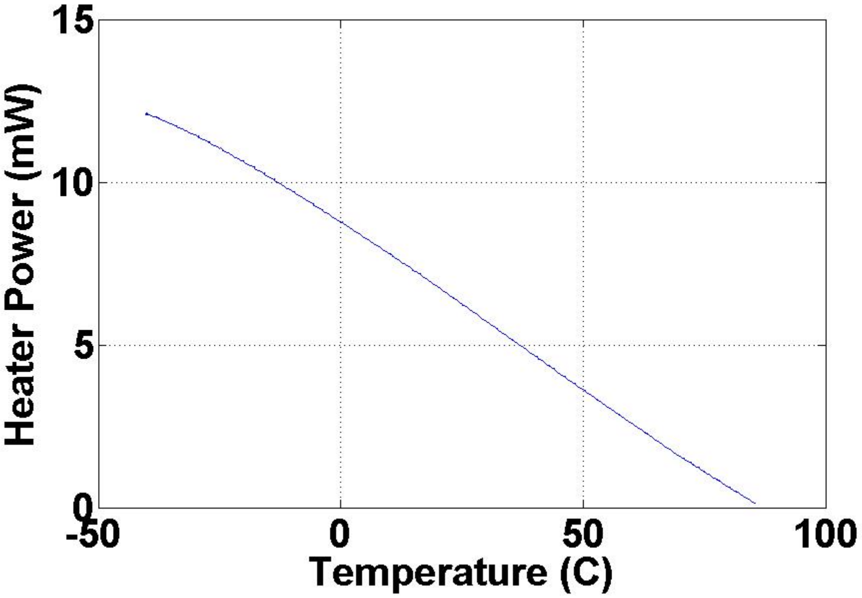


Figure 4.11: Power consumed by heater

a temperature sensor with 1 mK resolution at a supply voltage of 0.75V.
The first prototype was intended as a proof-of-concept chip and the goal was to demonstrate a temperature compensated FBAR oscillator using architecture-I . To achieve a sub mK temperature resolution , the sensor architecture in [11] was used. This prototype achieved a ±20 ppm stability and consumed 3.5 mW power. The temperature sensor consumed ∼ 2mW of power. The next section describes Prototype-I in detail with measured results.

4.5 Prototype - I

Figure 4.12 shows the architecture of prototype - I. In this prototype, the temperature sensor and the oscillator were designed as two separate chips to ease testing and debugging. A resistor on the FBAR package serves as the temperature sensing resistor. The next subsections describe in detail the circuit level schematics of the different components.

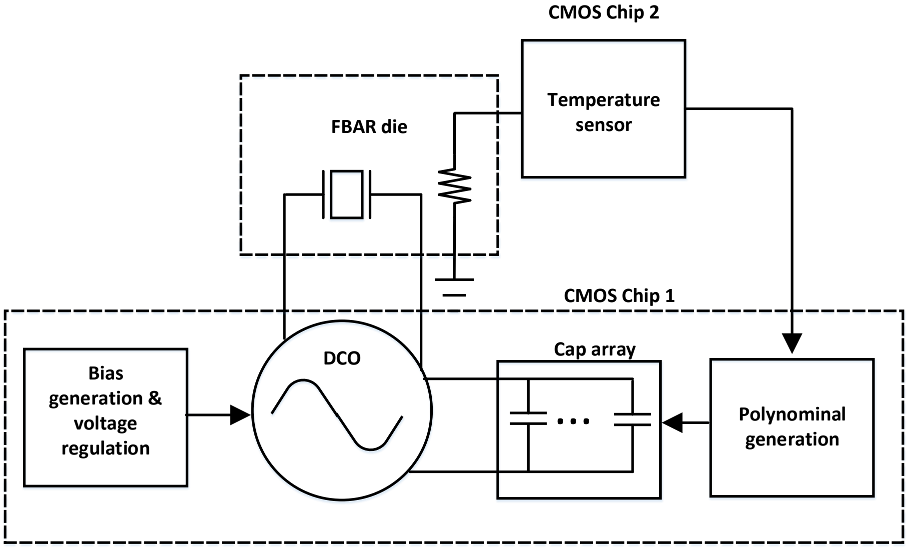


Figure 4.12: Prototype - I architecture

4.5.1 Digitally Controlled Oscillator (DCO)

The core of the frequency reference is the FBAR oscillator. Figure 4.13 shows three possible oscillator topologies commonly used for an FBAR oscillator [46] [47] [48].

- Colpitts
- Pierce
- Cross-coupled

Cross-coupled topology needs a 3 transistor stack. Assuming each transistor needs a minimum of 150mV to remain in saturation, the differential voltage swing is limited to 600mV with a 750mV supply voltage. In the Colpitts topology, the voltage swing across the resonator can be equal to supply voltage. But, capacitor C1 is a floating capacitor and cannot be used as a tuning capacitor. In contrast, both C1 and C1 in a pierce topology are referenced to ground and can be controlled using digitally using MOS switches. A pierce topology has a two transistor stack and the resonator is floating. With 0.75V supply, the maximum possible swing across the resonator is 900 mV. A pierce topology is used in this prototype because of better tuning resolution and high swing.

Figure 4.14 shows the DCO. The DCO runs from a 650mV regulated supply voltage. The oscillator is biased with 200uA current generated by a temperature independent bias generator discussed later. The capacitor array is made from a combination of fixed and digitally controlled capacitors as shown in figure 4.15. They can be varied in 32 steps each in a thermometric fashion to ensure monotonicity. The frequency step (resolution) of the DCO is designed to be 5ppm, yielding about 300ppm of tuning range for the 64 element cap array (unit cap 7 fF). To improve the the resolution, a second order sigma delta loop is used to dither a set of dithering capacitors. The second order sigma delta loop is clocked from a 175 MHz clock generated by dividing the oscillator output frequency by a factor of 4. The capacitor array is made from MIM capacitors in the process.

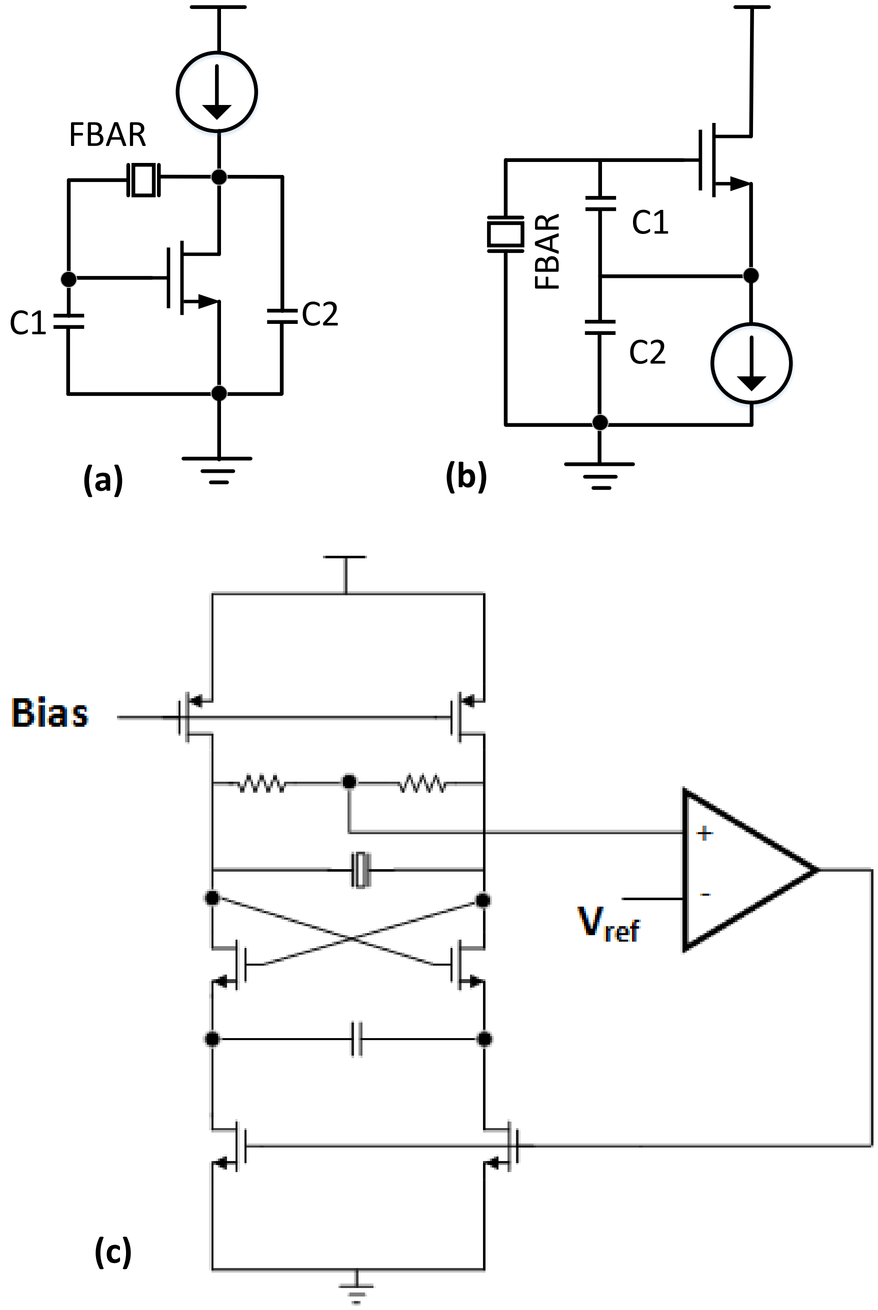


Figure 4.13: FBAR oscillator topologies, (a) Pierce, (b) Colpitts, (c) Cross coupled

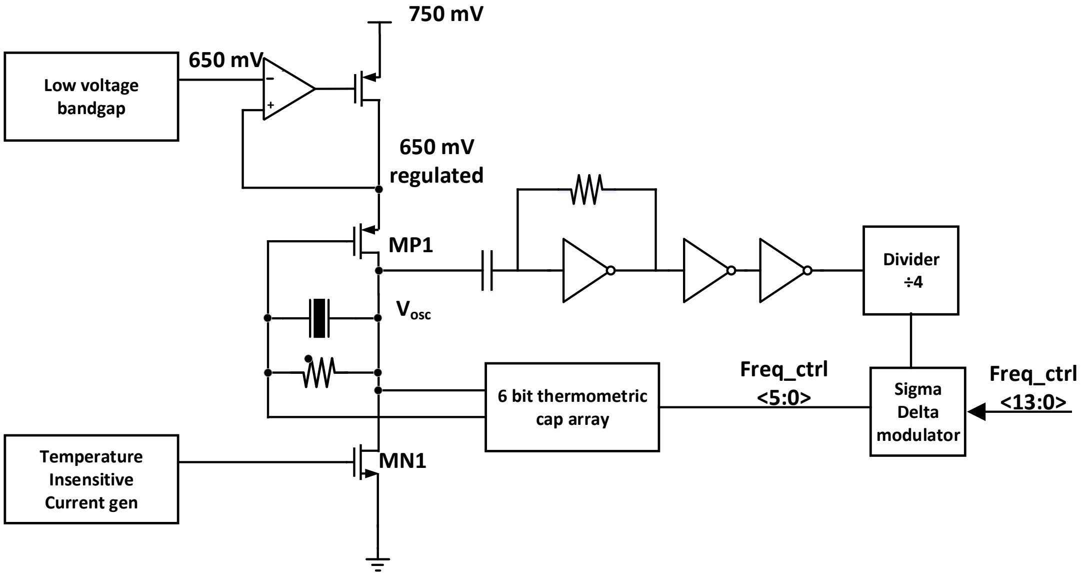


Figure 4.14: Digitally Controlled Oscillator - Architecture

4.5.2 Bias generation

All the analog blocks need well defined bias currents for their operation. Further, bias current for the oscillator need to be temperature independent, so that the oscillator does not introduce any significant variation in output frequency across temperature. Figure 4.16 shows the temperature insensitive bias generation circuit.

Transistors MN1 and MN2 are sized to operate in sub threshold region. If MP1 and MP2 are equally sized, currents I_1 and I_2 are equal. Feedback ensures that the voltages at the two inputs of the op-amp are equal. Under these conditions, voltage across resistor R can be written as

$$V_R = V_{GS,MN1} - V_{GS,MN2} = kTln\left(\frac{\left(\frac{W}{L}\right)_{MN1}}{\left(\frac{W}{L}\right)_{MN2}}\right) \tag{4.8}$$

Output currents can be written as

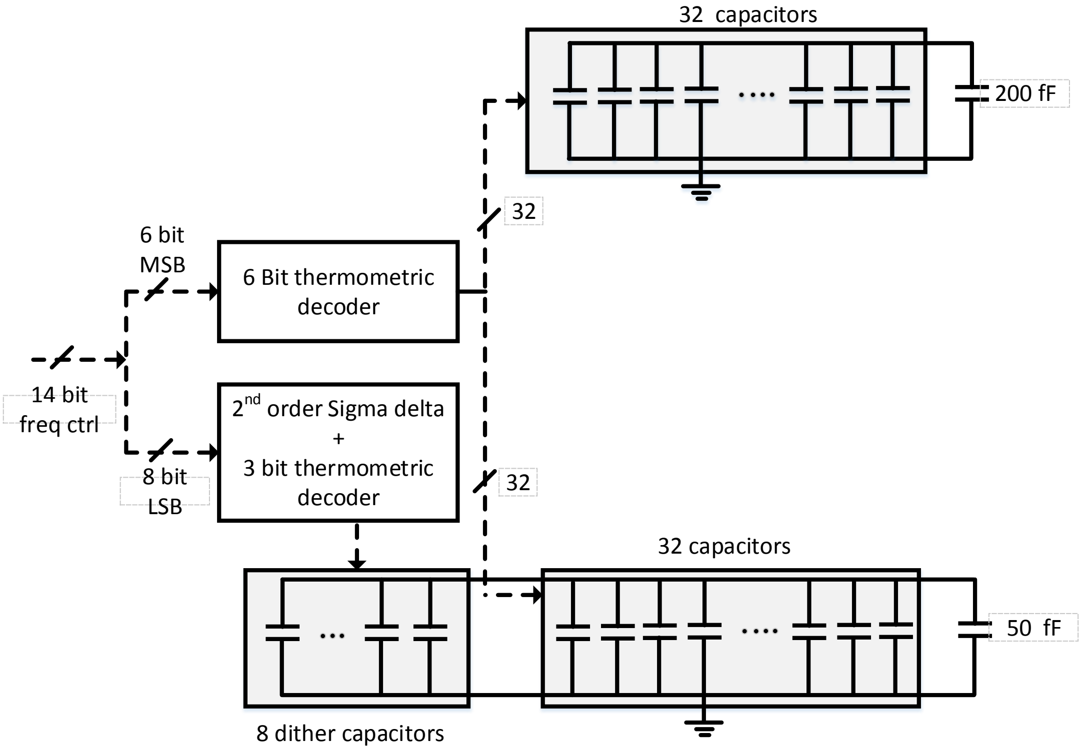


Figure 4.15: Details of the capacitor array

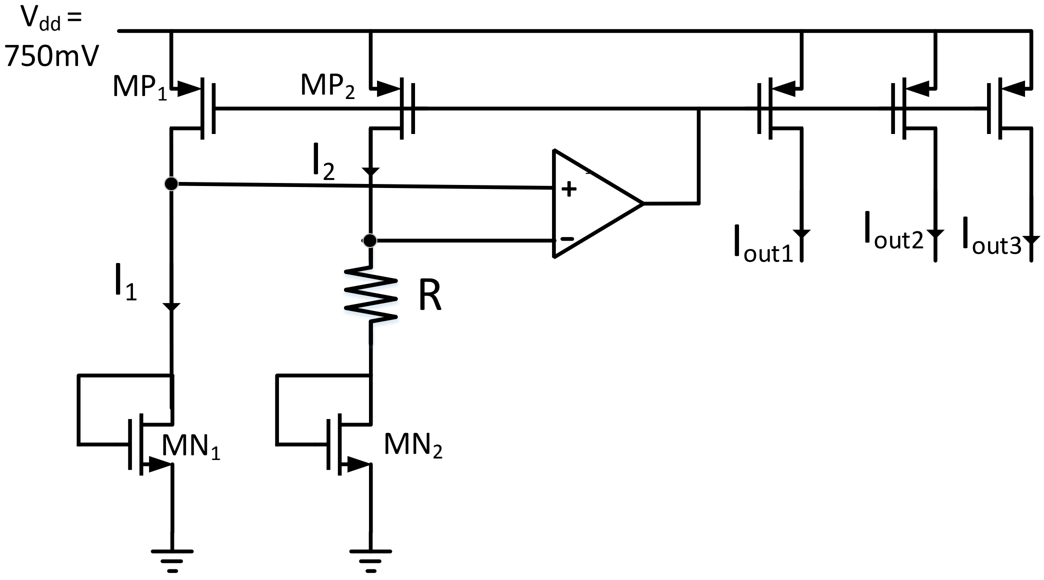


Figure 4.16: Temperature insensitive bias generation

$$I_{out} = \frac{kTln\left(\frac{\left(\frac{W}{L}\right)_{MN1}}{\left(\frac{W}{L}\right)_{MN2}}\right)}{R} \tag{4.9}$$

In this design R is an Nwell resistor and has a positive temperature coefficient. i.e $R = R_0\left(1+\alpha T\right)$. Choosing $\left(\frac{\left(\frac{W}{L}\right)_{MN1}}{\left(\frac{W}{L}\right)_{MN2}}\right)$ to match the positive temperature coefficient of Nwell resistor, we can cancel the first order temperature coefficient in the output currents. Figure 4.17 shows the simulated output of the bias generation circuit.

4.5.3 Reference voltage generation

To generate regulated 650mV for the DCO, a temperature independent reference voltage is needed. A MOS based low voltage bandage circuit shown in figure 4.18 is used to generate a 650 mV reference.

Assume feedback makes voltages V_X and V_Y equal, we can write

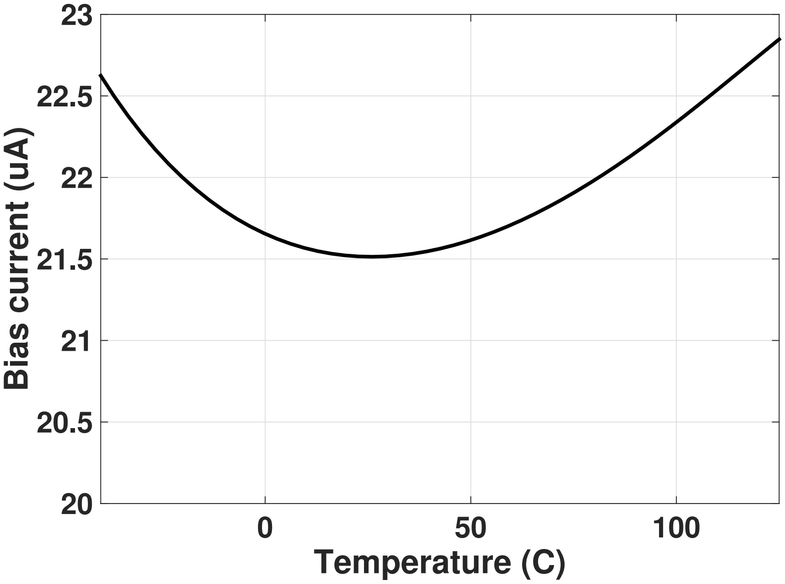


Figure 4.17: Simulated output of bias generation circuit across temperature

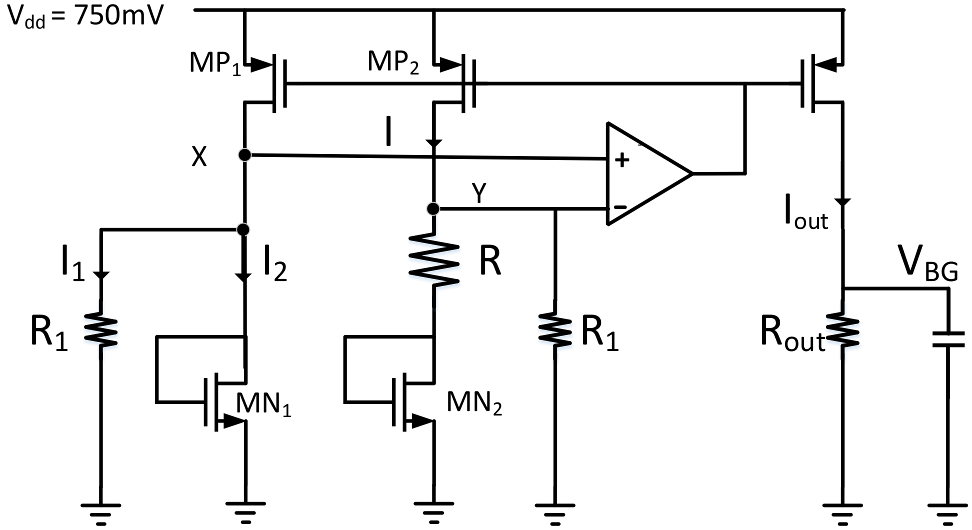


Figure 4.18: MOSFET based low voltage bandgap

$$I_2 = \frac{kTln\left(\frac{\left(\frac{W}{L}\right)_{MN1}}{\left(\frac{W}{L}\right)_{MN2}}\right)}{R} \tag{4.10}$$

I_2 has a positive temperature coefficient. Threshold voltage of a MOSFET has a negative temperature coefficient. In this process V_T reduces by 1.5mV per celsius.

$$I_1 = \frac{V_{T0} - \alpha T}{R1} \tag{4.11}$$

I_1 has a negative temperature coefficient. The output voltage can be written as

$$V_{BG} = \left(\frac{V_{T0} - \alpha T}{R1} + \frac{kTln\left(\frac{\left(\frac{W}{L}\right)_{MN1}}{\left(\frac{W}{L}\right)_{MN2}}\right)}{R} \right) R_{out} \tag{4.12}$$

By choosing R,R1,R_{out} appropriately, we can cancel the first order temperature coefficient of the output voltage. Figure 4.19 shows simulated V_{out} across temperature.

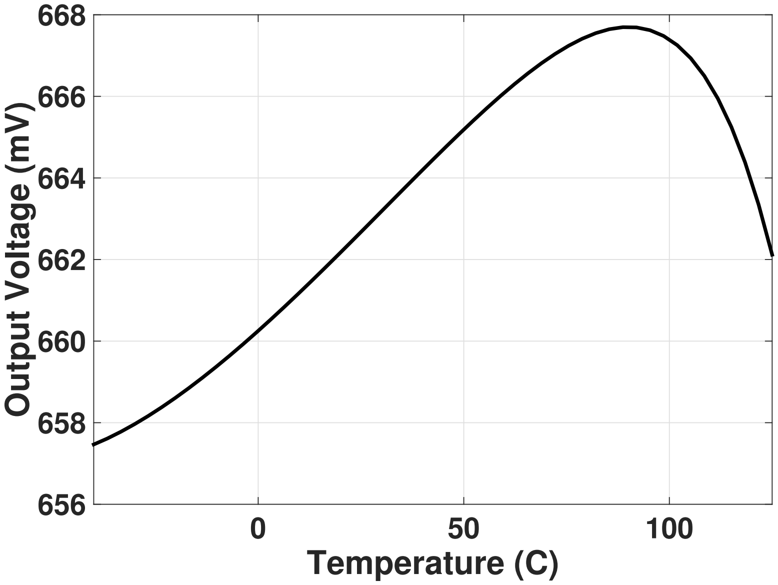


Figure 4.19: Simulated output of MOSFET based low voltage bandgap

4.5.4 Temperature sensor

As discussed earlier, temperature sensor for FBAR frequency compensation needs to have a resolution $\leq$ 1.8 mK. The only temperature sensor in the literature that achieves this specification is the sensor presented in [11]. In prototype - 1 we reuse the sensor architecture from [11].

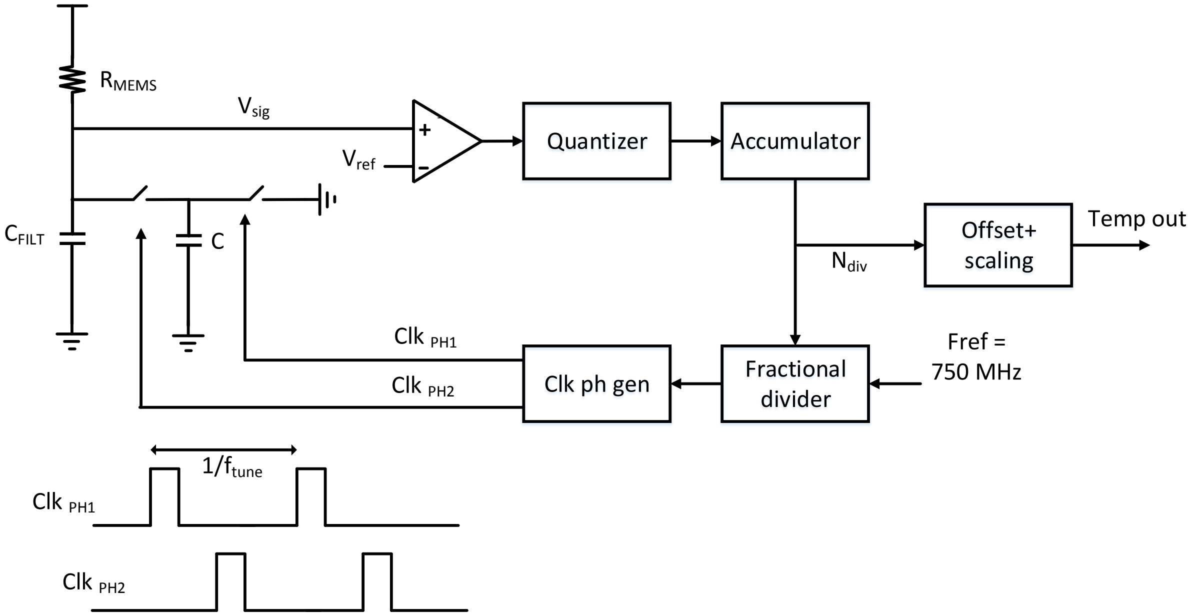


Figure 4.20: Principle of the temperature sensor in [11]

The basic principle of this architecture is as shown in figure 4.20. A resistance divider made of a sensor resistor R_{MEMS} and a tunable resistor R_{tune} is constructed. The tunable resistor is implemented as a switched capacitor resistor whose value can be controlled by varying the frequency f_{tune} of the control clock. The control clock is generated by dividing a fixed reference clock f_{ref} by a fractional number N_{div}. A feedback loop varies N_{div} such that $R_{MEMS} = R_{tune}$. At steady state we can write

$$R_{MEMS} = R_{tune} = \frac{1}{f_{tune}C} \tag{4.13}$$

$$f_{tune} = \frac{f_{ref}}{N_{div}} \tag{4.14}$$

from Equations 4.13 and 4.14 and using $R_{MEMS} = R_{MEMS0}\,(1 + \alpha T)$ we can write

$$N_{div} = f_{ref} R_{MEMS} C = f_{ref} C R_{MEMS0}\,(1 + \alpha T) \tag{4.15}$$

After offset and gain scaling N_{div} gives the desired digital representation of temperature. The quantizer shown in figure 4.20 is implemented digitally using ring oscillator. To handle flicker noise, chopping and correlated double sampling are used. A detailed description and noise analysis of the architecture is not discussed here and can be found in [11]. In this prototype the temperature sensor is designed as a separate test chip for ease of testing. The temperature sensor runs at a clock frequency of 24 KHz.

4.5.5 Polynomial correction and digital filtering

Figure 4.21 shows the digital signal processing block that takes the temperature sensor output and generates the required control for the DCO. An Infinite Impulse response (IIR) filter is followed by a polynomial generation block. Required coefficients for the polynomial generation are fed through shift registers. In practice, the shift registers need to replaced with poly-fuses to realize a ROM to hold the coefficients permanently. A one time 3 point or 4 point calibration is sufficient to generate these coefficients.

4.5.6 Experimental results

Two chips one containing the temperature sensor and the other containing the DCO and signal processing were fabricated in TMSC 65nm GP process. Figures 4.22 and 4.23 show the die photographs of the DCO and temperature sensor chips respectively. the DCO chip had an area of 1.4mm x 0.9 mm of which the area utilized by the DCO core is about 0.7 mm x 0.7 mm. The temperature sensor consumes an area of 0.9 mm x 0.5 mm.

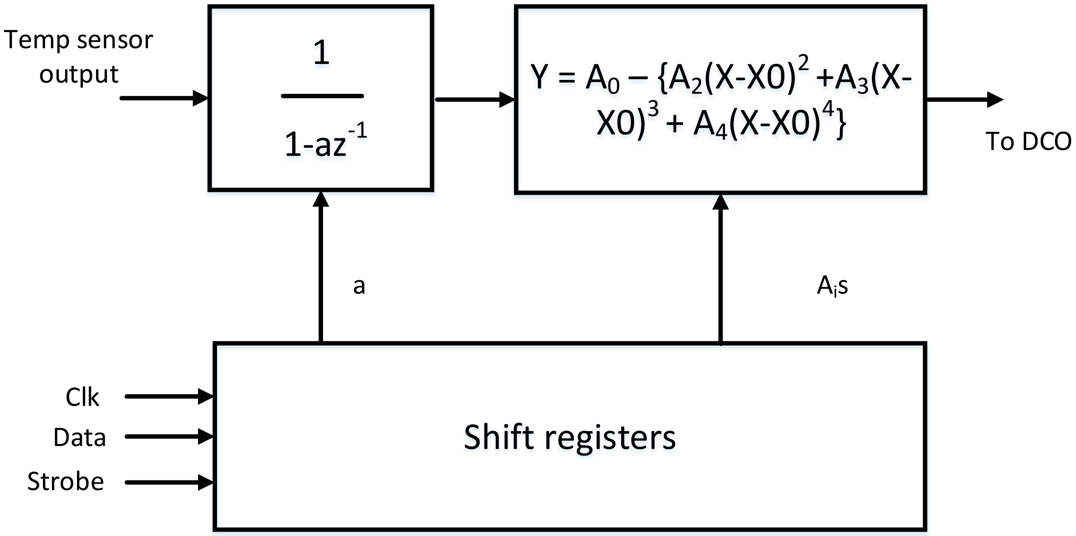


Figure 4.21: Digital signal processing to generate required DCO control

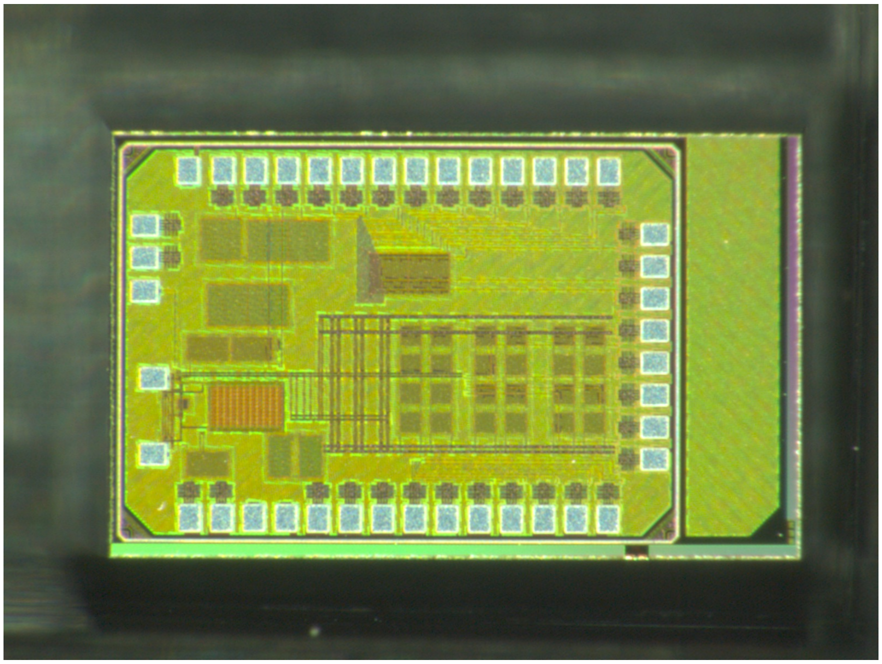


Figure 4.22: Die photo of DCO chip in prototype - I

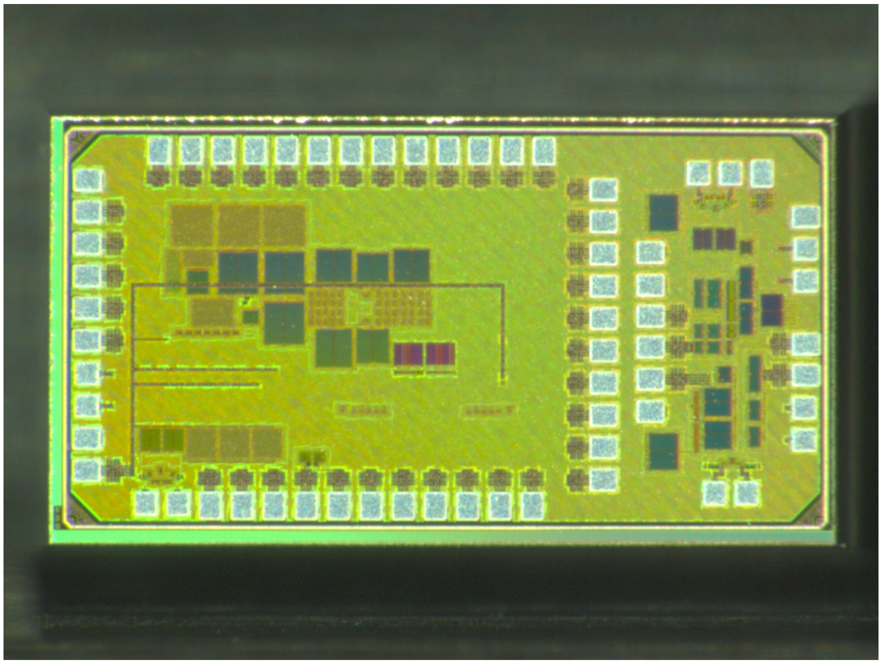


Figure 4.23: Die photo of Temperature sensor in prototype - I

Figure 4.24 shows the measured DCO transfer function across the frequency control code. The tuning range is about 250 ppm slightly less than the designed value of 300ppm but still sufficient enough to correct for temperature drifts. We also see that the transfer function is not monotonous at discrete points. Figure. 4.25 shows a zoomed out version and we clearly see a jump in frequency with a magnitude of about 2 ppm. Frequency step size for unit caps in C1 (drain side cap in the pierce structure) and C2(gate side cap in the pierce structure) are different from each other. But the dithering cap is connected only to C1. Whenever the dithering cap is completely turned off and the next cap is turned on a discontinuity arises. This will cause undesired frequency jumps and phase noise degradation. The fix for this issue is fortunately simple and is discussed later.

Figure 4.26 shows the measured phase noise of the oscillator with the temperature compensation turned on. However, it should be noted that when a frequency jump occurs during measurement the phase noise degrades from what is shown in figure 4.26.

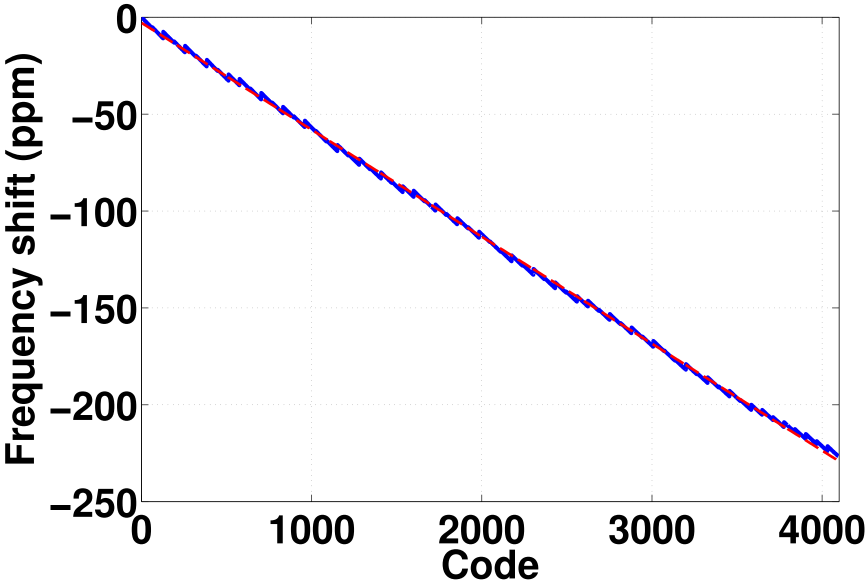


Figure 4.24: measured DCO transfer function

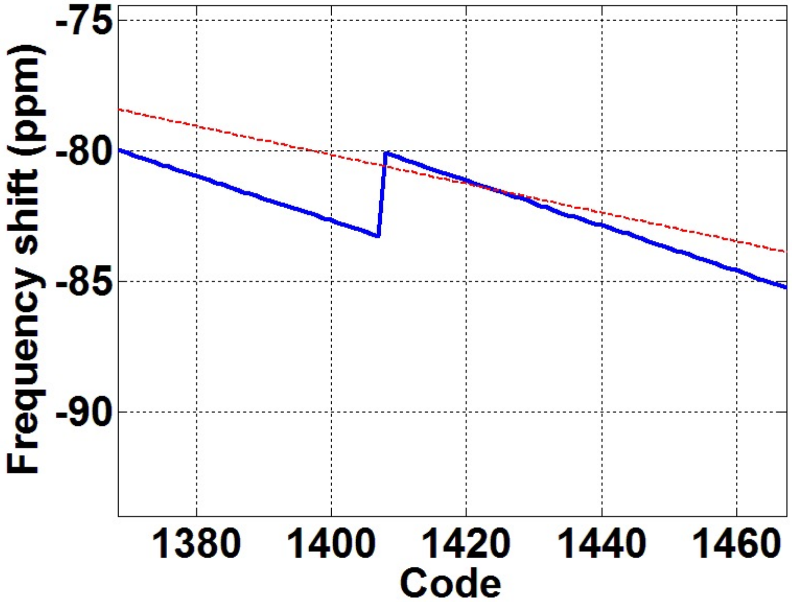


Figure 4.25: discontinuity in DCO transfer function

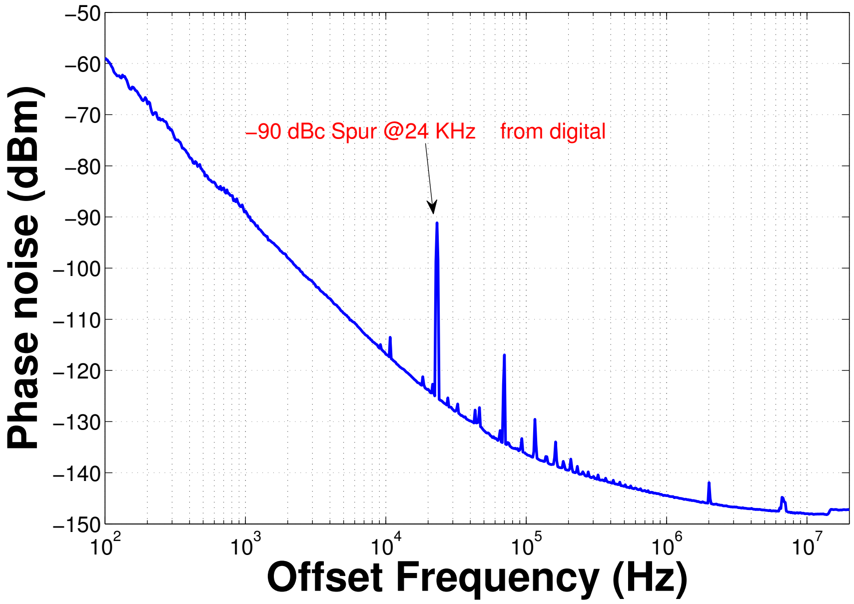


Figure 4.26: Measured phase noise of the DCO with temperature compensation

Figure 4.27 shows the Allan deviation of the FBAR oscillator.

Several anomalies were present in the temperature sensor measurements. First, the sensor was functional only when the temperature was ramping up. The sensor output was stuck at the same value when temperature was ramped down. Further, the temperature sensor needed a hardware reset to settle down to the right value. These issue were tracked down to weak operation of digital buffer at the output of the ring oscillator in the temperature sensor and a polarity inversion of the clock signal in the feedback loop. These were fixed in the next iteration of the chip. The fractional divider did not work with the intended input frequency of 750 MHz at 0.75V supply. We had to reduce the frequency to 375 MHz or increase the supply to 0.95V to get the temperature sensor to be functional. This issue was tracked down to a setup time issue in the fractional divider. Even with these issues we were able to measure the performance of the temperature sensor if we ramped the temperature up and reduced the reference clock frequency to 375 MHz. Figure 4.28 shows the measured transfer

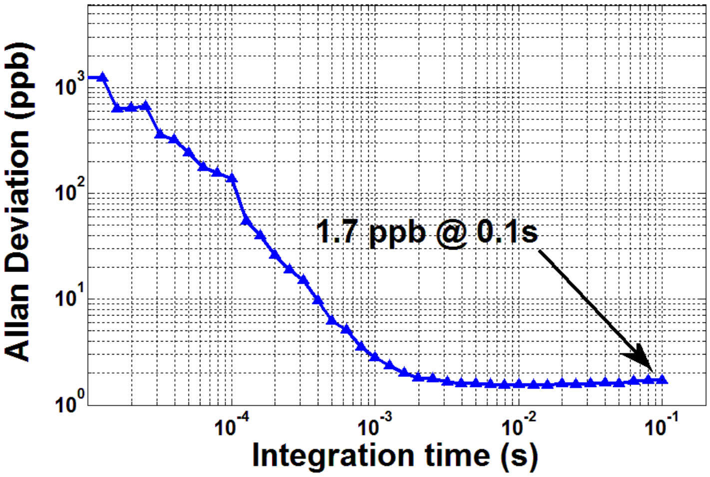


Figure 4.27: Measured Allan deviation of the FBAR oscillator

function of the temperature sensor. The gain of the temperature sensor was 6X lesser than the designed value. A factor of 3X comes from the reduction in temperature sensitivity of the sense resistance due to uncertainties in the FBAR fabrication process. Another 2X comes from the reduction in reference clock frequency from 750MHz to 375 MHz. The measured noise performance was better than 200 μK and was limited by the number of output bits

The DCO and temperature sensor were integrated at the board level. Figure 4.29 shows the measured frequency of the FBAR oscillator with and without temperature compensation. The compensated oscillator achieves a stability of ± 20 ppm far from the desired ± 5 ppm. Figure 4.30 explains this reason for this limited compensation achieved. The available gain in the control path was limited because of the gain reduction of the temperature sensor. To compensate for this reduction in gain, the turn over temperature (TOT) was artificially pushed to a higher value during the calibration process. The residual error is the difference of two parabola with different vertices and is quadratic in nature as seen in figure 4.29

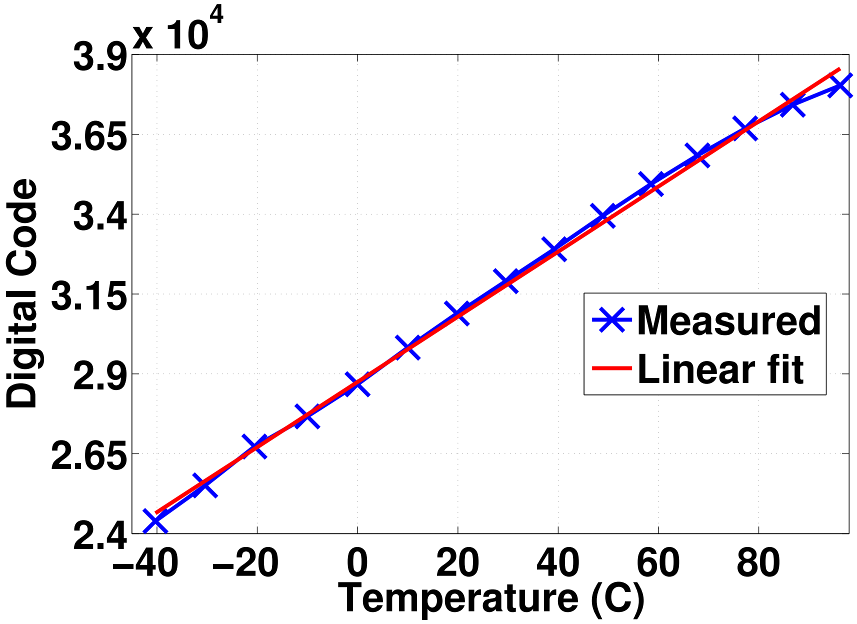


Figure 4.28: Measured transfer function of the temperature sensor

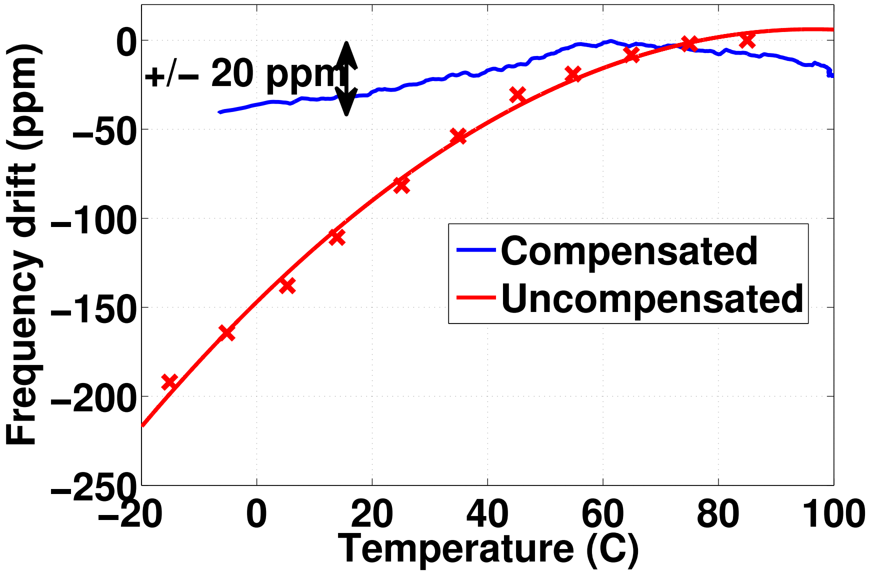


Figure 4.29: FBAR oscillator frequency with and without temperature compensation

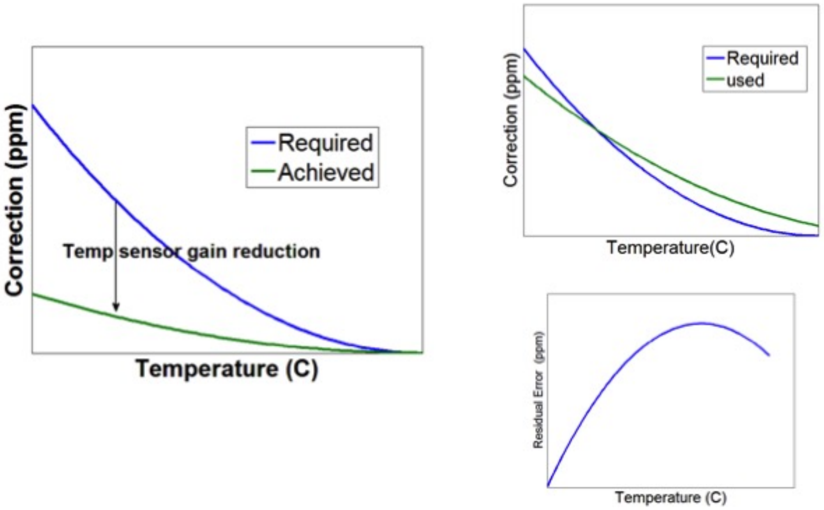


Figure 4.30: Gain reduction issue limiting achievable frequency compensation

Table 4.2 shows the measured power consumption of Prototype - I . The total power consumption is 2.95 mW significantly higher than the desired 1 mW. Temperature sensor is the most power hungry element in the system consuming more than 65 % of the total power. Power consumption of the temperature sensor needs to be addressed to enable a 1 mW FBAR frequency reference.

Table 4.2: Power consumption of prototype - I

Block	Power consumed (mW)
DCO	0.45
Temperature sensor	1.9
Digital poly gen & filtering	0.6
Total	2.95

4.6 Chapter summary

This chapter discussed the problem of stabilizing FBAR references across temperatures to enable quartz free wireless radios. A non - PLL based architecture is selected to ensure low power consumption necessary for wireless sensors. Details of the first prototype chips fabricated in 65nm TSMC process were discussed and experimental results were presented. Issues identified during the testing of the first prototype necessitated a second prototype which is discussed in the next chapter.

Chapter 5

FBAR BASED QUARTZ REPLACEMENT - PROTOTYPE - II

5.1 Goals for prototype - II

A second prototype was planned to address the issues in the first prototype. The following were the goals of the second prototype

- A temperature sensor architecture that consumed 100X lower power and a relaxed resolution of 1-2 mK.
- A monotonous DCO transfer function.
- A temperature stability better than ± 5 ppm for the FBAR reference.

5.2 Modifications in prototype - II

Figure. 5.1 shows the architecture of Prototype - II

The following were the changes made in prototype - II

- The capacitor array and dither scheme were modified to ensure a monotonous DCO transfer function,
- Temperature sensor - II - A novel temperature sensor architecture that consumes only 15 μ W was designed.
- The DCO and the temperature sensor were integrated on the same chip. As a backup plan, the old temperature sensor was also added to the chip. An external control is used to select between temperature sensor I or II. This is not shown in figure

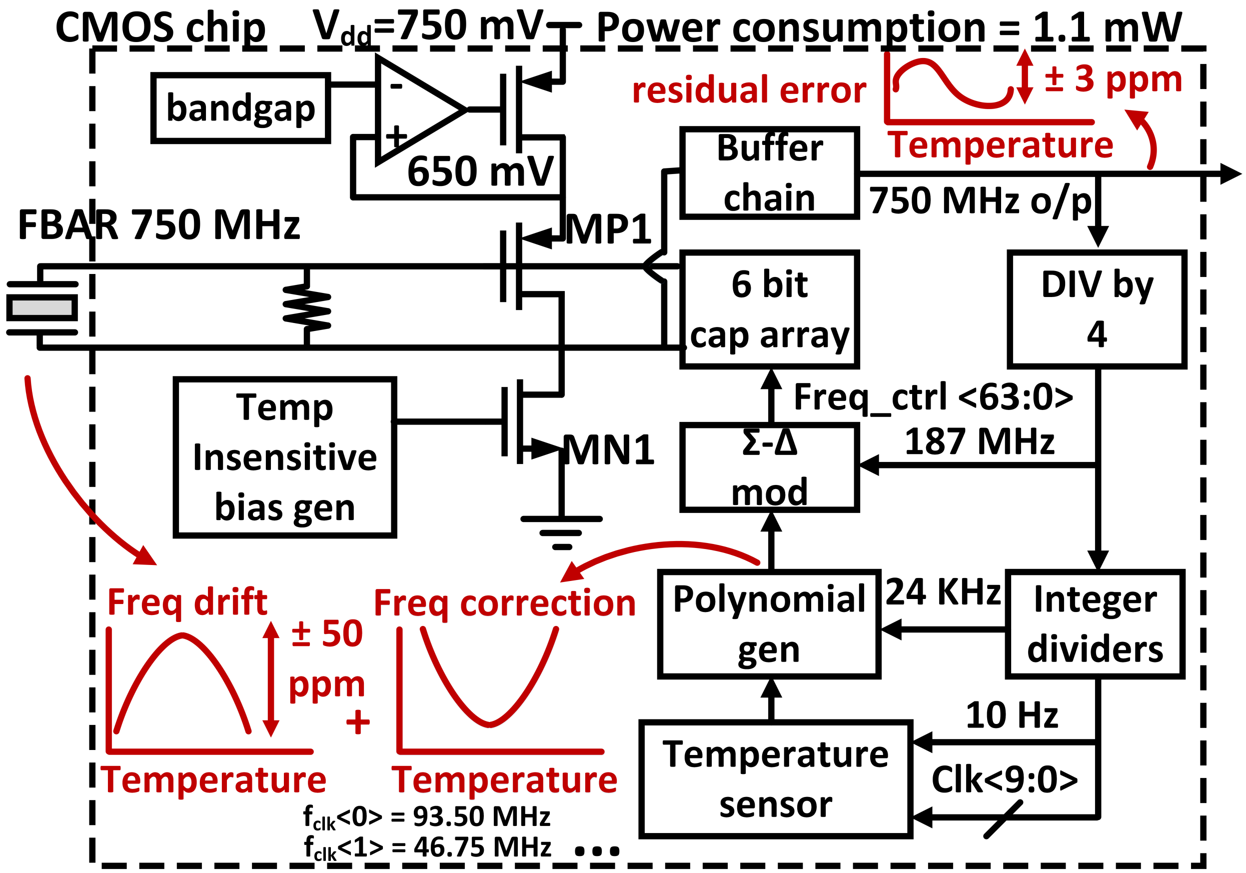


Figure 5.1: Architecture of prototype - II

- Gain in the correction path was increased to achieve a ±5 ppm stability.

These changes are discussed in detail in this section and measurement results from the second prototype is presented.

5.2.1 Capacitor array modifications

Difference in frequency sensitivities between the gate and drain side capacitances (nodes X & Y in figure.5.2) was the main reason for the abrupt frequency jump in DCO - I. This was fixed by introducing a symmetrical unit capacitor as shown in figure 5.2. Each unit capacitor in prototype - I is split into two equal halves and at every frequency step equal capacitances are added to the drain and source capacitances. Further, the dithering scheme is changed as shown in figure 5.3. This dithering scheme ensures that the dithering is dynamic and point to the last used capacitor in the array. For example, if the control has a value equivalent to 7.99, first 7 capacitors are turned on and the 8th capacitor is turned on 99 % of the time. if the control has a value equivalent to 8.01, first 8 capacitors are turned on and the 9th capacitor is turned on 1%the time as shown in figure.5.4

These two schemes ensure monotonicity by design and is not affected by mismatches or process variations.

5.2.2 Temperature sensor principle

Figure. 5.5 shows the required performance of the temperature sensor in relation to state of the art temperature sensors. The best resolution reported so far for a CMOS temperature sensor is 100 μK and the best resolution figure of merit (FOM) is 3.6 pJK^2. However temperature sensors from these works operate at a supply voltage $\geq$ 2.9V which is not compatible with our 0.75V system. We target to achieve a resolution of 1.6 mK with a figure of merit of 3.6 pJK^2 using a supply voltage of 0.75V.

The key strategy to achieve low voltage operation is to encode temperature in the time domain rather than the voltage domain. This scheme would require a time domain DAC

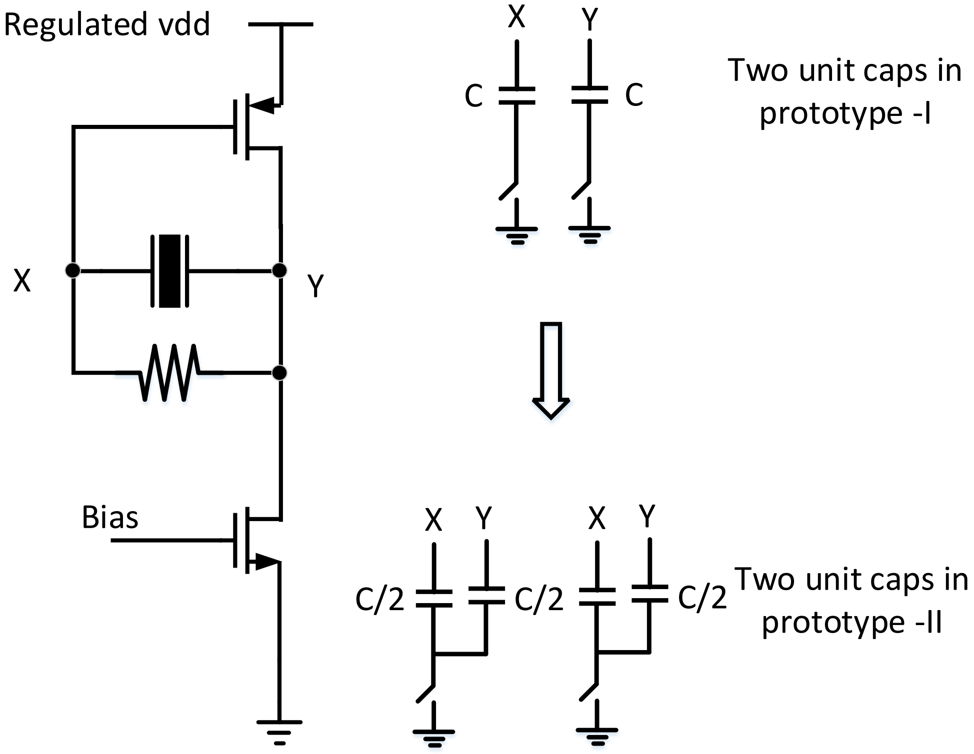


Figure 5.2: Capacitor array changes in prototype - II

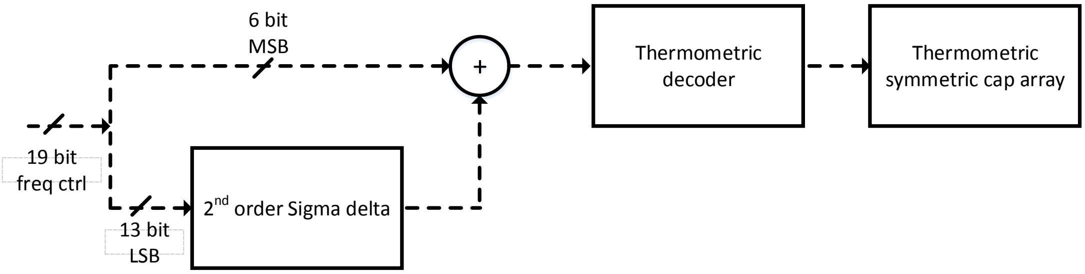


Figure 5.3: Dithering scheme in prototype - II

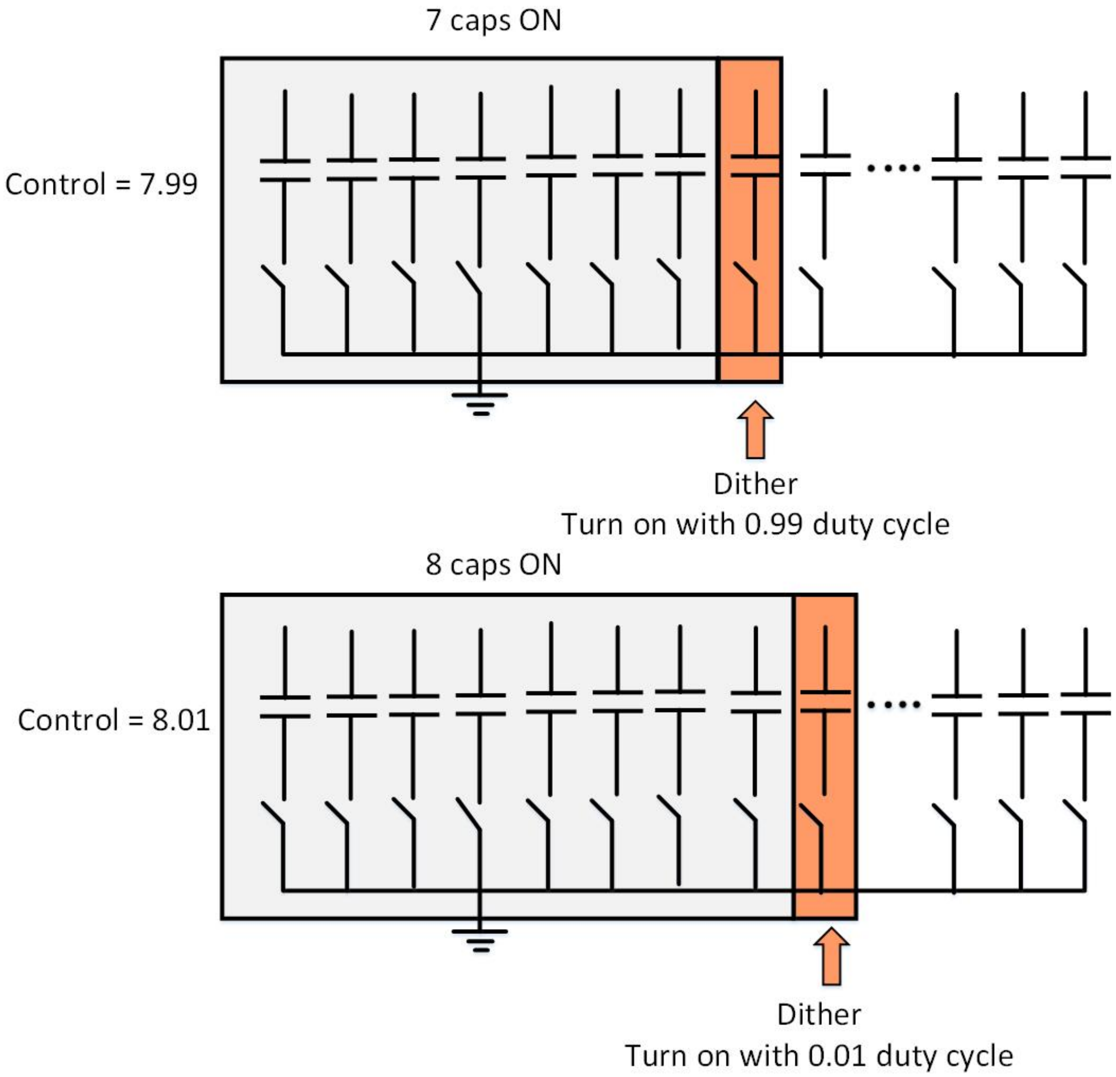


Figure 5.4: Dithering scheme in prototype - II

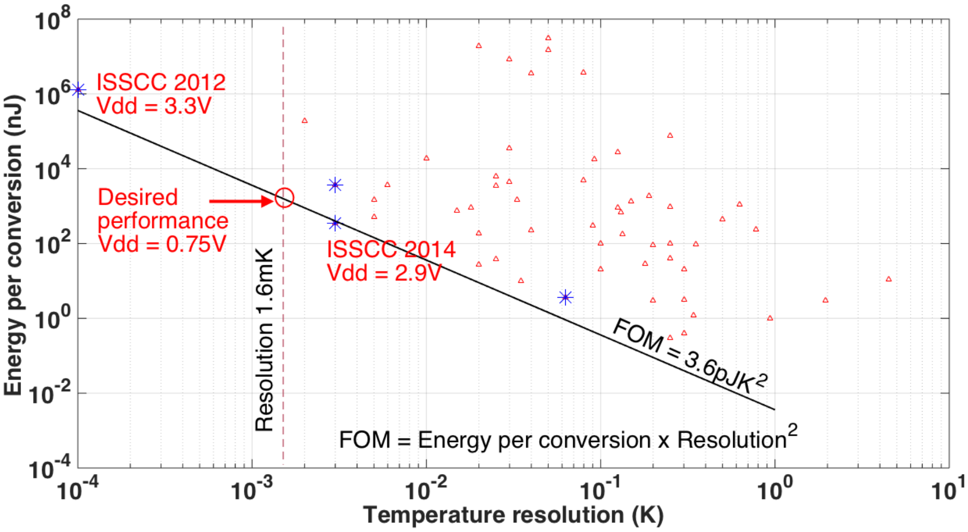


Figure 5.5: Required performance for the temperature sensor compared to the state of the art

which can easily be built using the available frequency reference from the FBAR oscillator. Figure 5.6 shows one way of achieving the temperature - duty cycle encoding.

A Wheatstone bridge is constructed using two types of resistors R_P (N-well) and R_M (p-poly). R_P has a positive temperature coefficient i.e $R_P = R_{P0}(1 + \alpha T)$ while R_M has a negative temperature coefficient i.e. $R_M = R_{M0} * (1 - \beta T)$. R_M is split into a fixed component $R_{M,fixed}$ and a variable component whose average value is controlled by the duty cycle of CLK_C.

$$R_M = R_{M,fixed} + d.R_{M,var} \tag{5.1}$$

Assume we develop a feedback loop that monitors the balance of the wheatstone bridge and modifies the duty cycle of CLK_C , d. When the bridge is balanced we can write

$$R_P = R_M = R_{M,fixed} + d.R_{M,var} \tag{5.2}$$

$$d = \frac{R_P - R_{M,fixed}}{R_{M,var}} \tag{5.3}$$

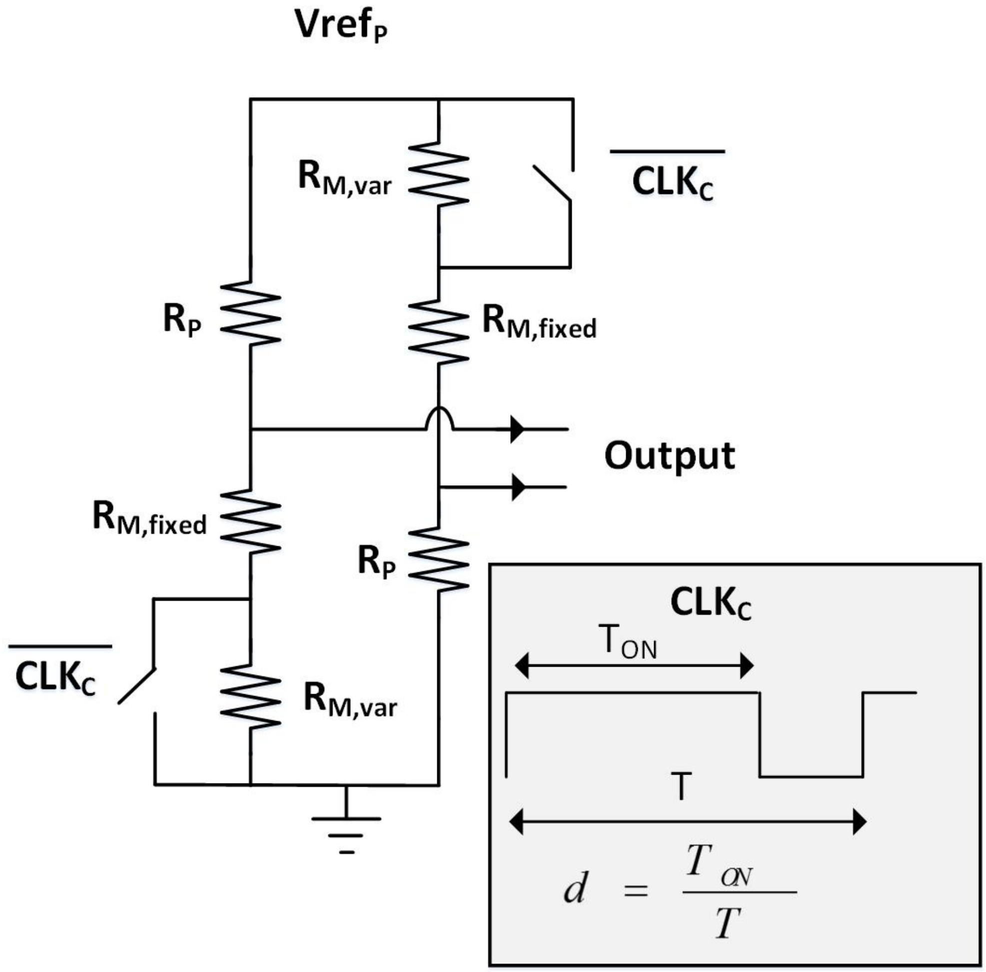


Figure 5.6: Principle behind time domain encoding of temperature

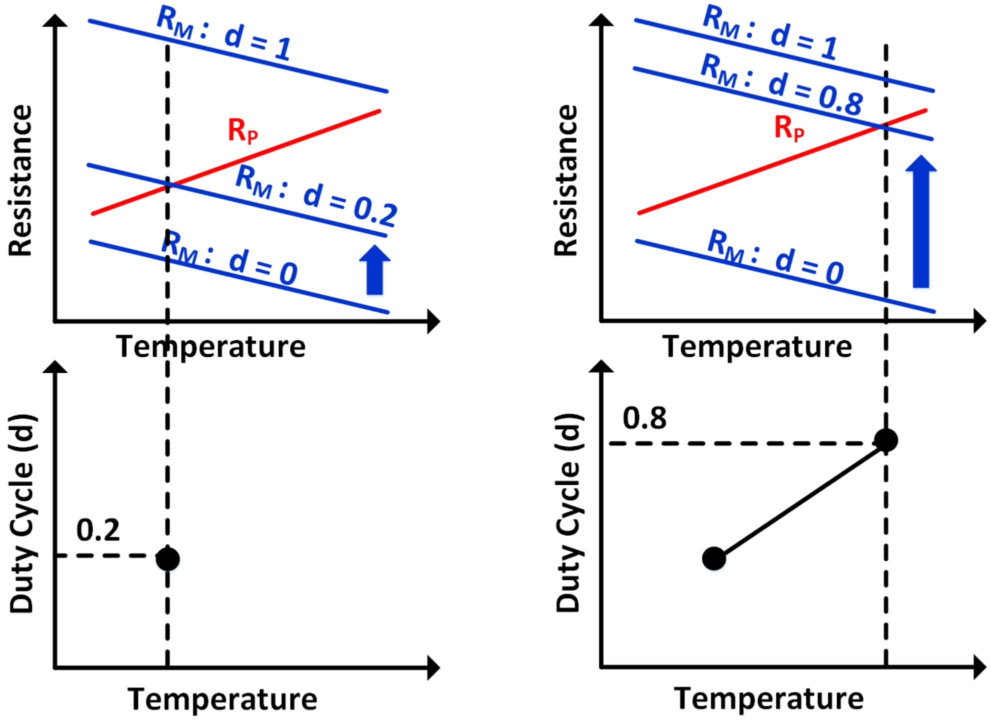


Figure 5.7: Principle behind time domain encoding of temperature

$$d = \frac{R_{P0}}{R_{M,var0}}\left(1+(\alpha+\beta)\right)T - \frac{R_{M,fixed0}}{R_{M,var0}} \tag{5.4}$$

This mechanism encodes the temperature information as the duty cycle of CLK_C. Figure 5.7 explains the concept graphically. In order to get a digital representation of the duty cycle, we introduce a digital to duty cycle converter (DDC) in the feedback loop as shown in figure 5.8

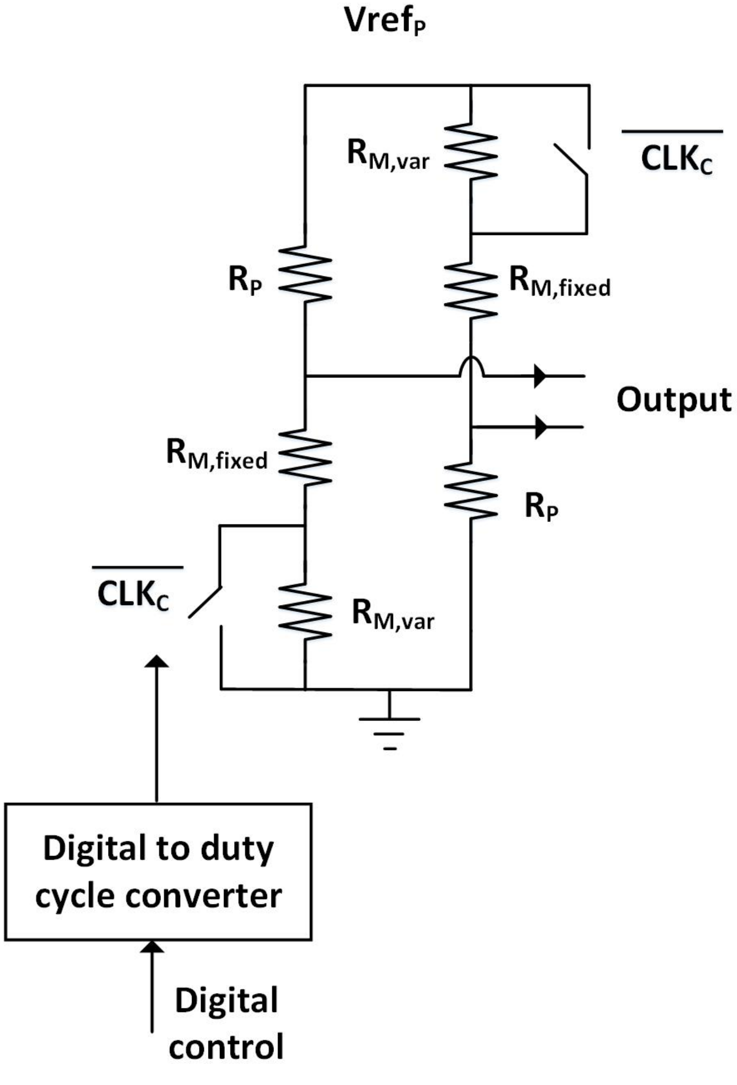


Figure 5.8: Digital to duty cycle converter is introduced in the feedback

The DDC can be built entirely from logic gates as shown in figure.5.9. The DDC exploits the divided clocks available in the system as illustrated in figure. 5.10. Upon the rising edge of 200 KHz clock the output is set to a high value. If we view the divided clocks as an asynchronous counter, the output is reset when the count reaches the control input. The output clock has a fixed frequency of 200 KHz and a duty cycle controlled by the digital control input to DDC.

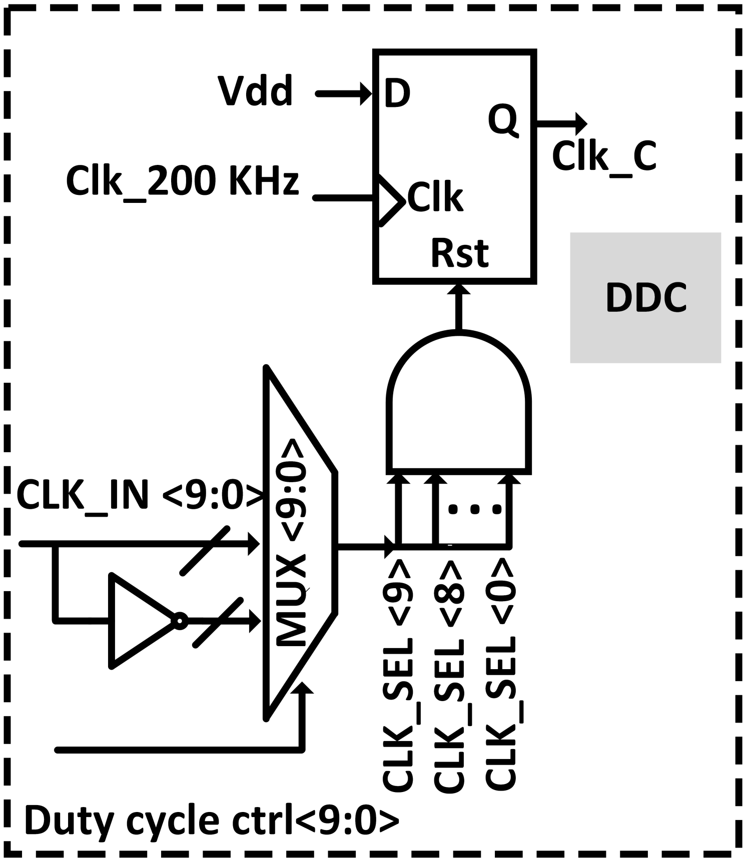


Figure 5.9: Digital to duty cycle converter block diagram

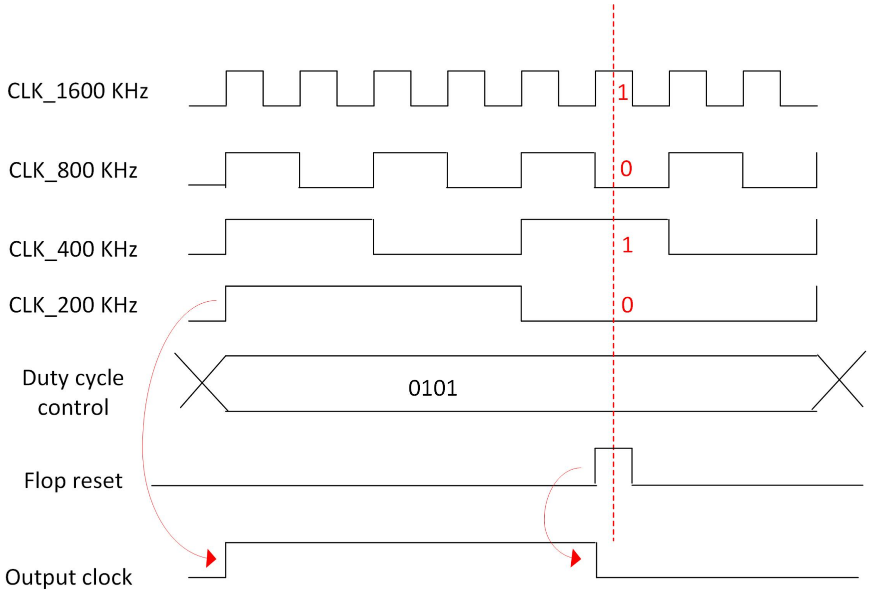


Figure 5.10: 4 bit DDC example. Actual DDC is 10 bits

5.2.3 Architecture of the feedback loop

Figure 5.11 shows how the feedback loop is closed in the temperature sensor The loop operates similar to the zoom ADC presented in [49]. An integrator monitors the Wheatstone bridge for balance. A comparator running at 200 KHz quantizes the integrator output to a 1 bit value. Input to the 'Digital to duty cycle Converter' (DDC) is adjusted based on the comparator output to balance the bridge. The loop operates in two phases.

- SAR phase
- $\Sigma - \Delta$ phase.

as shown in figure.5.12 In the SAR phase the duty cycle is digitized to a coarse 7 bit value value, (In the actual implementation a 10 bit estimate is generated. To account for comparator offsets and mismatch a guard band of ±4 is used reducing the resolution to 7 bits.) At the end of the SAR phase, the duty cycle is bounded between two values $d_{ref,1}$ and $d_{ref,2}$. The loop is them configured as a first order $\Sigma - \Delta$ loop where the duty cycle is dithered

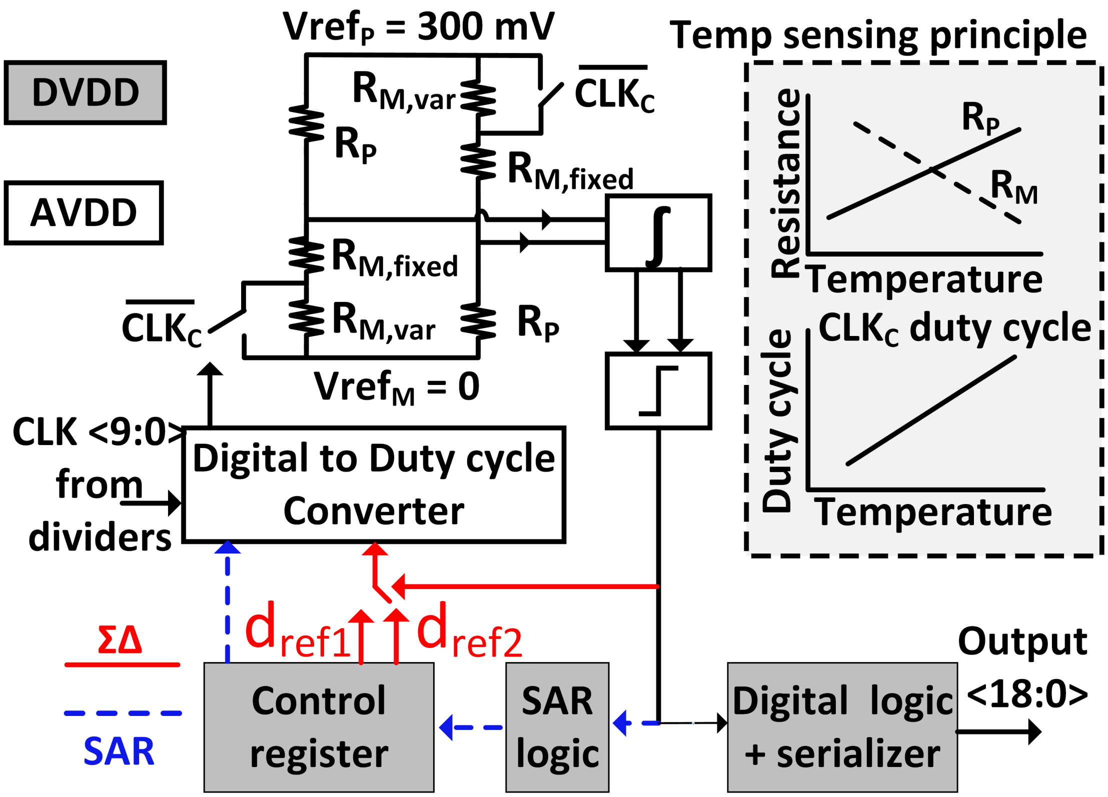


Figure 5.11: Architecture of temperature sensor

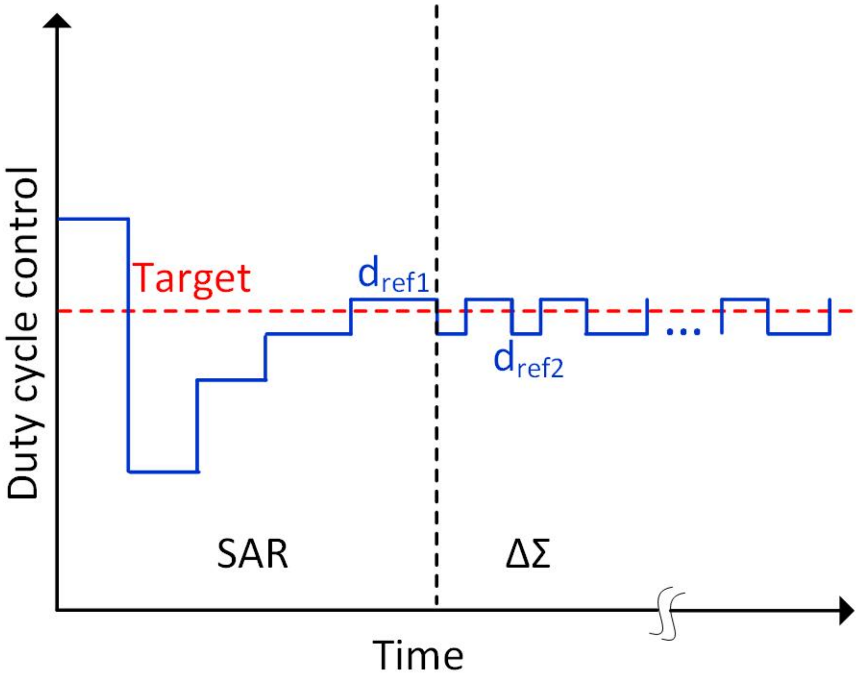


Figure 5.12: Zoom operation of the temperature sensor showing two phases

between $d_{ref,1}$ and $d_{ref,2}$ to produce a finer 19 bit estimate. Average value of the DDC control in the SAR phase gives the required digital representation of the duty cycle.

5.2.4 Circuit Schematics

Integrator

Integrator is the first block in the signal chain and is the most critical in terms of noise performance. A passive integrator structure presented in [50] is used and is shown in figure 5.13 is used in our implementation. The integrator needs to maintain a low input impedance at the input and transfers the signal current from the wheatstone bridge to the integrating capacitor. Low input impedance is achieved by using common gate input stage together with a gain boosting amplifier. Flicker noise from current sources $MN_{1,2}$ $MP_{1,2,5,6}$ are removed by using chopping. In our implementation, a reference voltage of 300 mV is used for the

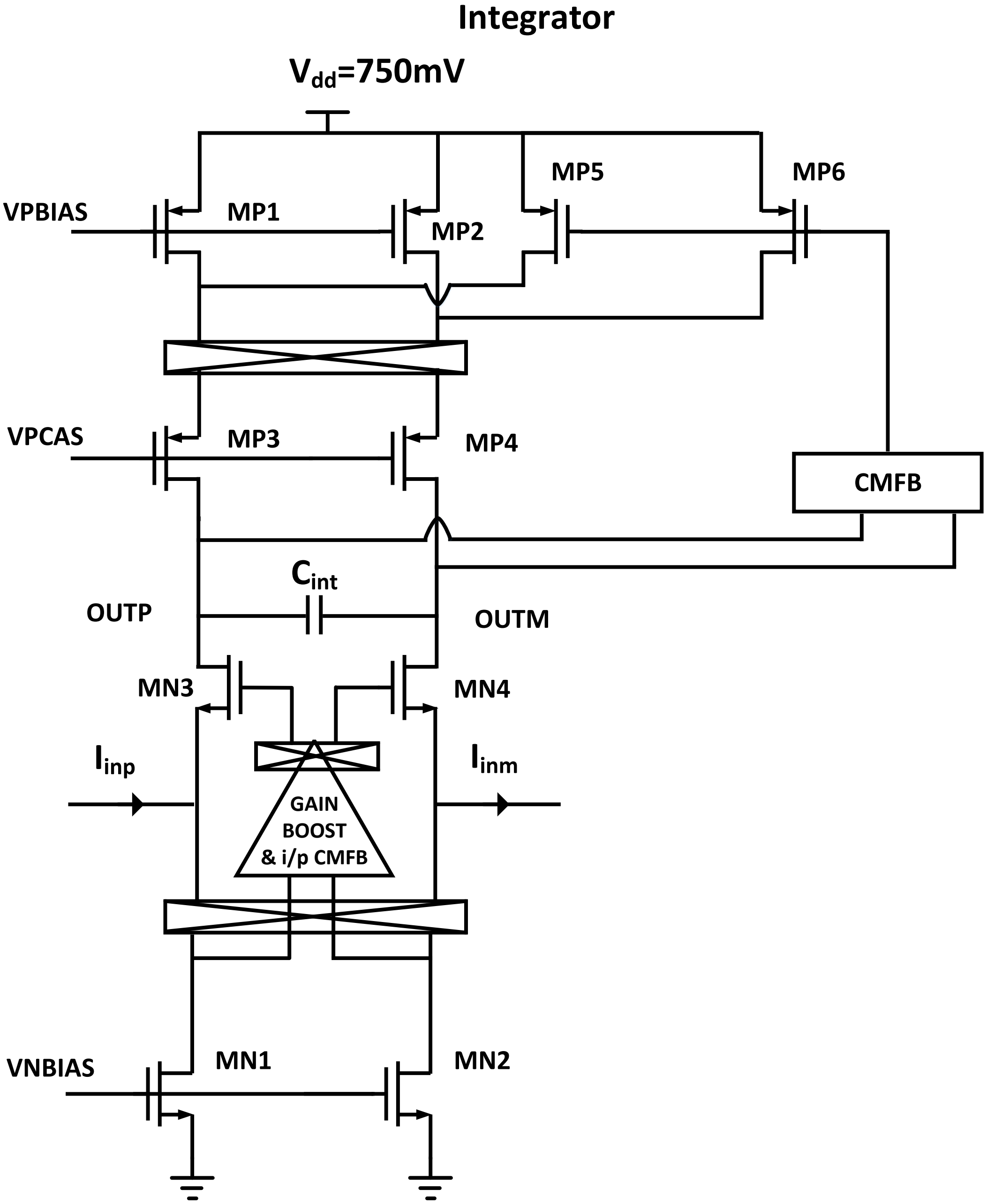


Figure 5.13: Implemented integrator

wheatstone bridge and the input common mode of the integrator is set to half the reference using a common mode feedback loop. There are 4 transistors in the stack. All transistors are biased with a V_{ds} of 150 mV across process and temperature. This is achieved by the bias generation circuit shown in figure 5.14. The cascode and the current source bias voltages are generated by feedback ensuring robust biasing across temperature and process. The integrator is biased with 3 μA per branch. The gain boost amplifier consumes 8 μA .

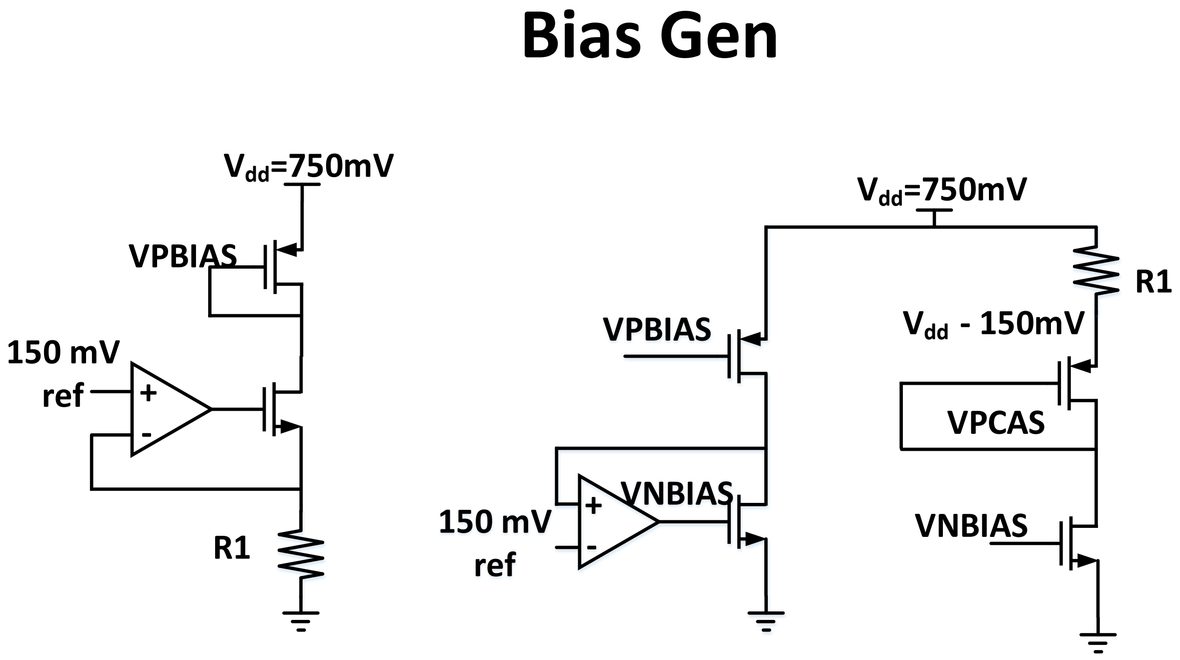


Figure 5.14: Bias generation circuit used to bias the integrator

Comparator

A dynamic comparator with a 3 stage pre amplifier similar to [50] is used . The preamplifiers consume 50nA per branch. The comparator is clocked at 200 KHz.

5.3 Experimental results

The proposed temperature sensor architecture together with the DCO was fabricated in 65nm TSMC CMOS process. Figure 5.15 shows the CMOS chip wire bonded to the FBAR resonator.

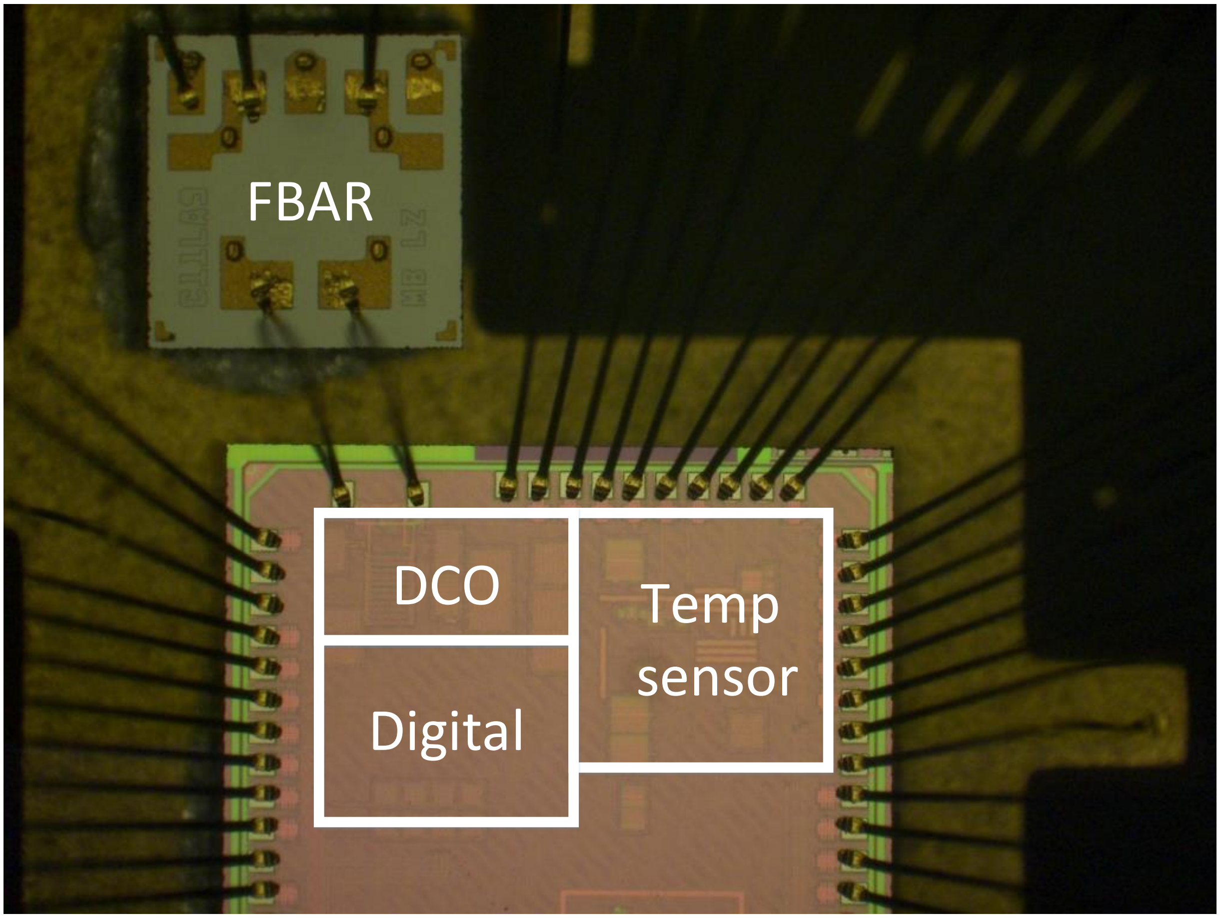


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Figure 5.15: Die photo of prototype II

Figure 5.16 shows the measured DCO transfer function. The transfer function is monotonous and has no abrupt frequency jumps as desired.

The temperature sensor was characterized by mounting the chip on a measurement PCB

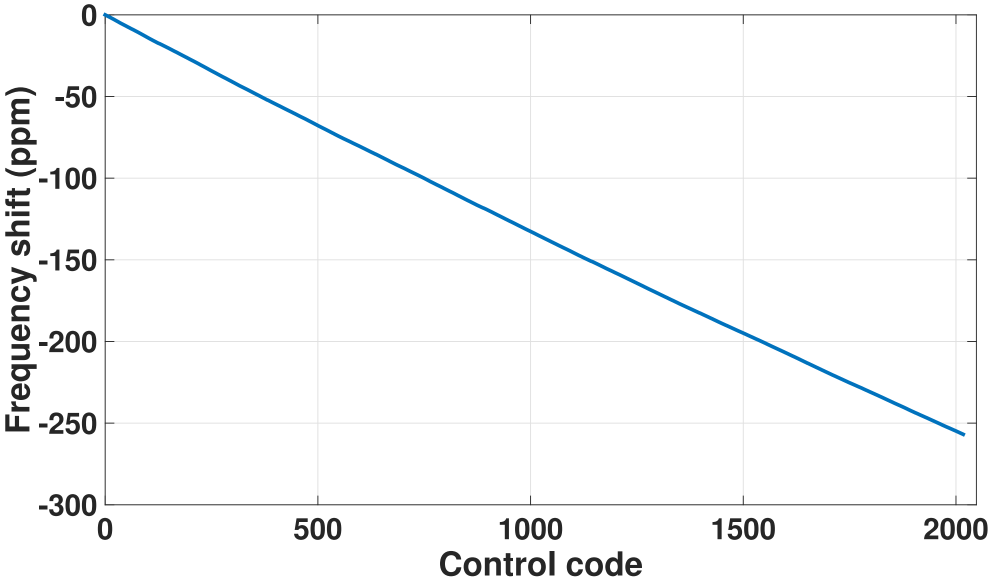


Figure 5.16: Measured DCO transfer function

. The PCB is placed inside a thermal chamber. The PCB included a precision RTD close to the CMOS chip to measure the 'true temperature'. Figure 5.17 shows the measured TDC transfer function.

Figure 5.18 shows the measured error of temperature sensor after a 4 point calibration. The error is better than ±0.1 C sufficient to achieve a ± 5 ppm frequency drift. Measurement of temperature sensor noise on the bench turned out to be very hard due to ambient temperature drifts. The issue was resolved by immersing the PCB in a oil bath and carefully removing any heat sources near the PCB that could cause a temperature drift. Output of the temperature sensor was measured continuously for about 20 minutes. Figure 5.19 shows the noise spectrum of the TDC output. Integrated noise from 0.1 Hz to 5 Hz is 1.6 mK. The temperature sensor consumes a power of 15 μW and samples at 10 Hz. The resolution figure of merit of temperature sensor can be computed by

$$FOM_{resolution} = \frac{P_{sensor} \times resolution^2}{f_{sample}} \tag{5.5}$$

This sensor achieves an FOM of 3.8 to 4.6 pJK^2 across chips. This is $\sim$ 3X better than the

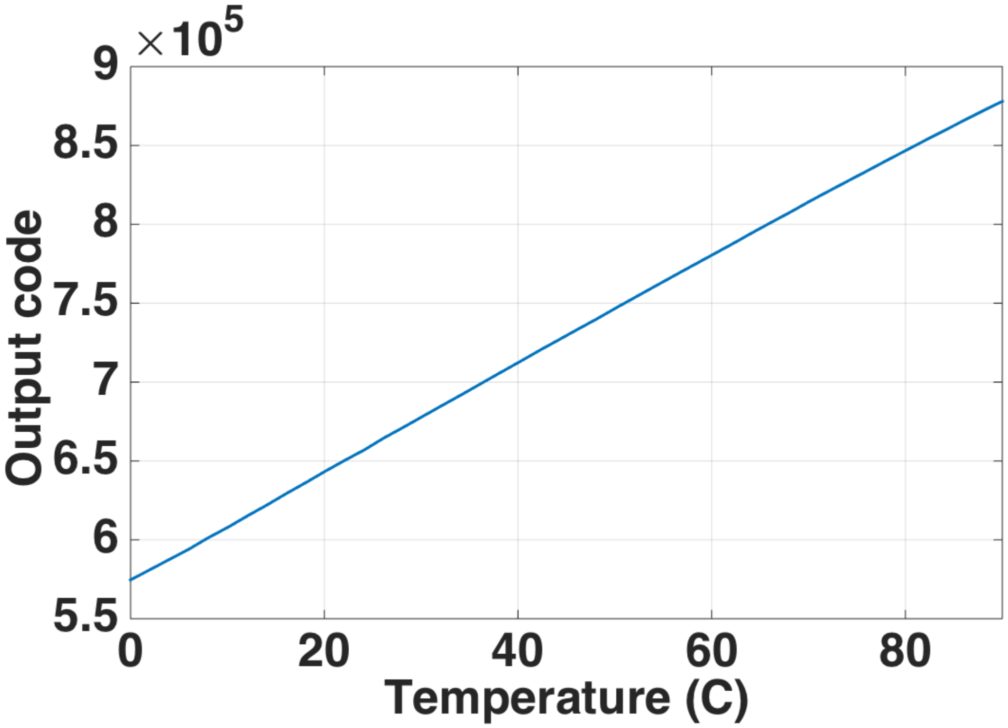


Figure 5.17: Measured temperature sensor transfer function

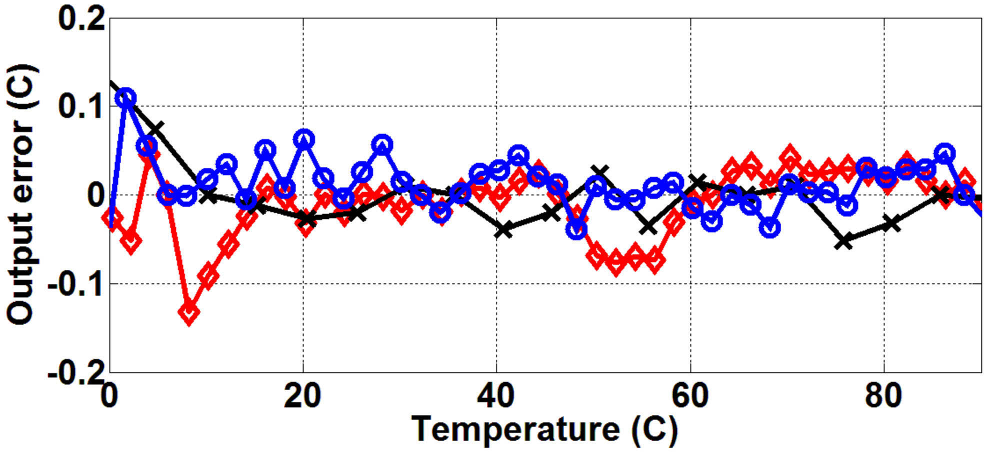


Figure 5.18: Measured error of temperature sensor across three chips after calibration

FOM reported to date for sub 1V temperature sensors.

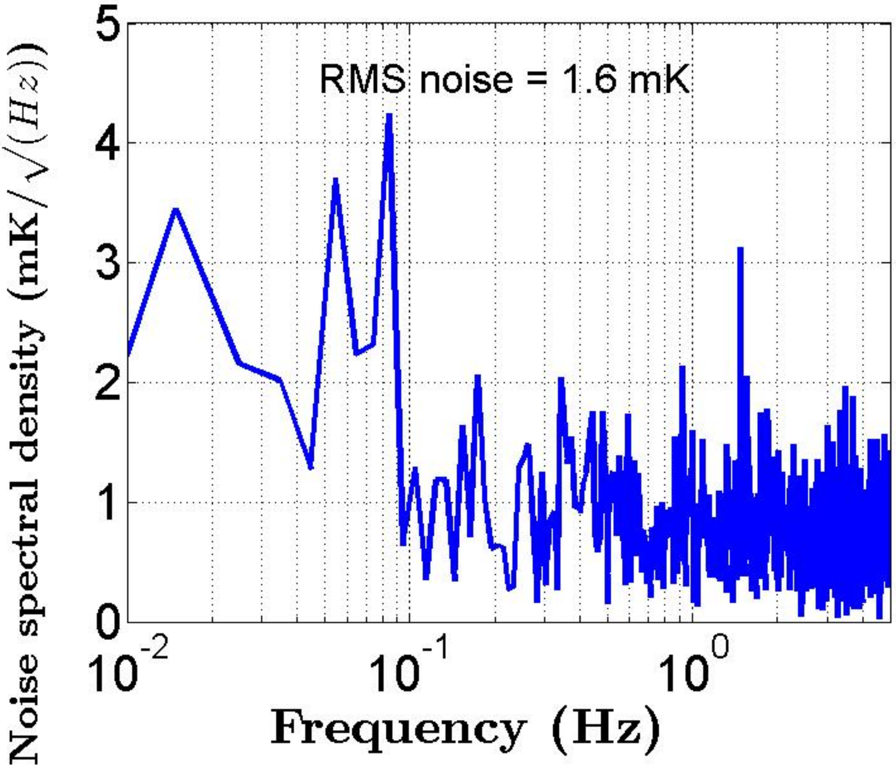


Figure 5.19: Noise spectrum of temperature sensor

System level temperature stability was measured by performing calibration at 4 temperatures. Figure 5.20 and 5.21 shows the measured temperature stability of the compensated FBAR reference. Frequency drift across temperature is less than ± 3 ppm.

Figure 5.22 shows the measured phase noise of the FBAR reference with the compensation turned on/off . The compensation was turned off by shutting down the clock to the temperature sensor and forcing a constant control code at the input of the DCO. We see that the temperature compensation does not results in any significant phase noise degradation. Spurs at 320 Hz is caused by digital IO switching from a 32X serializer for the temperature sensor output running at 10 Hz. Spur at 24 KHz is caused by the digital polynomial correction logic running at 24 KHz needed for backward compatibility with the temperature sensor

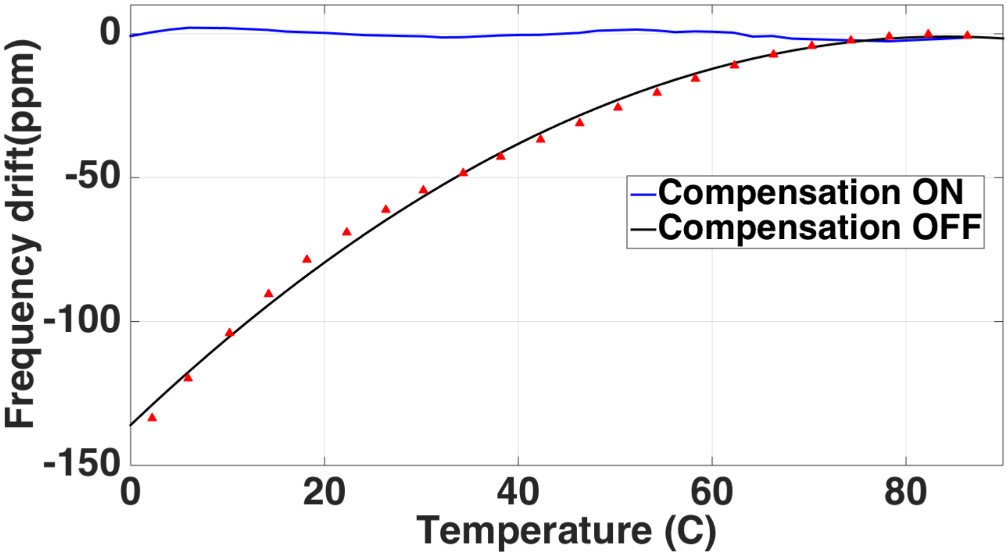


Figure 5.20: Measured temperature stability of the FBAR frequency reference with and without compensation

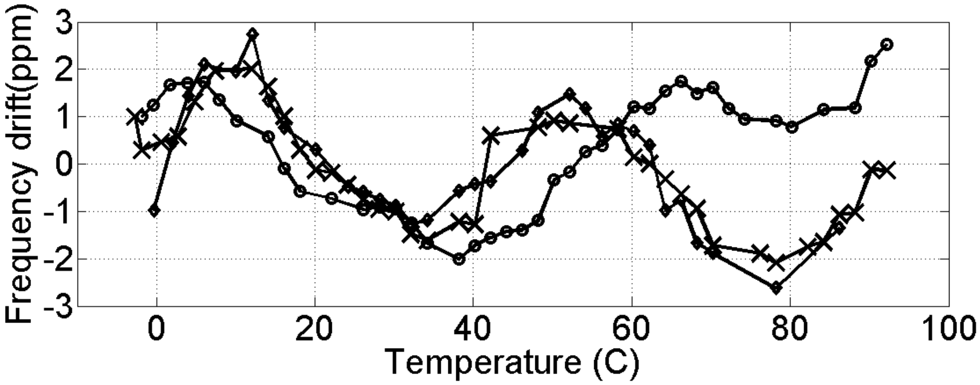


Figure 5.21: Measured temperature stability of the FBAR frequency reference after 4 point calibration

from prototype - I. Spur at 768 KHz is caused by a 32X serializer running at 32 × 24 KHz. These spurs can be removed by removing the serializers which are necessary for testing only.

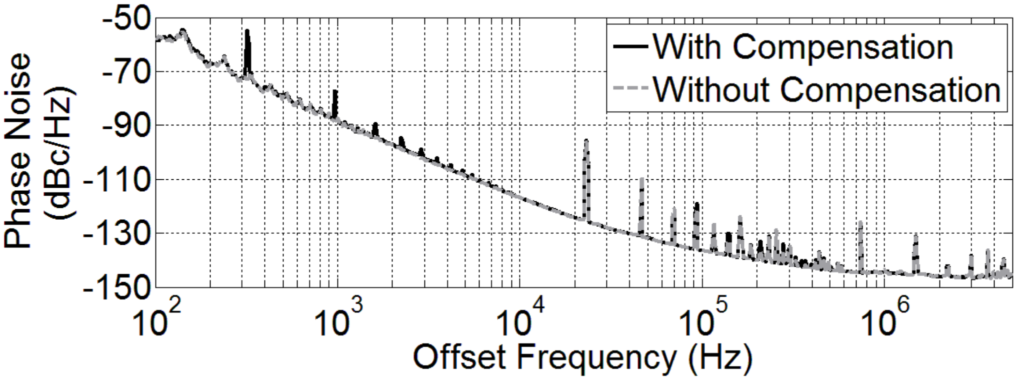


Figure 5.22: Measured phase noise of the FBAR reference with and without compensation

To illustrate that the reference does not have any abrupt frequency jumps, we measured the frequency for a time span of about 11 hours. Figure 5.24 shows the measured frequency showing only smooth variations.

Figure 5.23 shows the measured Allan deviation with and without compensation. The temperature compensated frequency reference achieves an Allan deviation of 4.7 - 8 ppb across chips at a 100mS integration time which is competitive with current MEMS frequency references. The reported FBAR frequency reference consumes a total power of 1.1 mW from a 0.75 V supply. The oscillator consumes 450 μ W, the temp sensor consumes 15 μ W, and the rest is consumed by the buffers, dividers, $\Delta - \Sigma$ modulator and the digital polynomial generator.

Figure. 5.25 compares the reported temp sensor to state of the art temperature sensors. The reported temp sensor operates from a 0.75V supply, which is lower than any CMOS temperature sensor reported to date. Figure. 5.26 also compares the FBAR frequency reference to other MEMS and quartz references. To the best of the our knowledge, this work presents the first RF frequency reference with sufficient stability (+/- 3ppm) and power (1.1mW) suitable for quartz-free standards-based wireless transceivers.

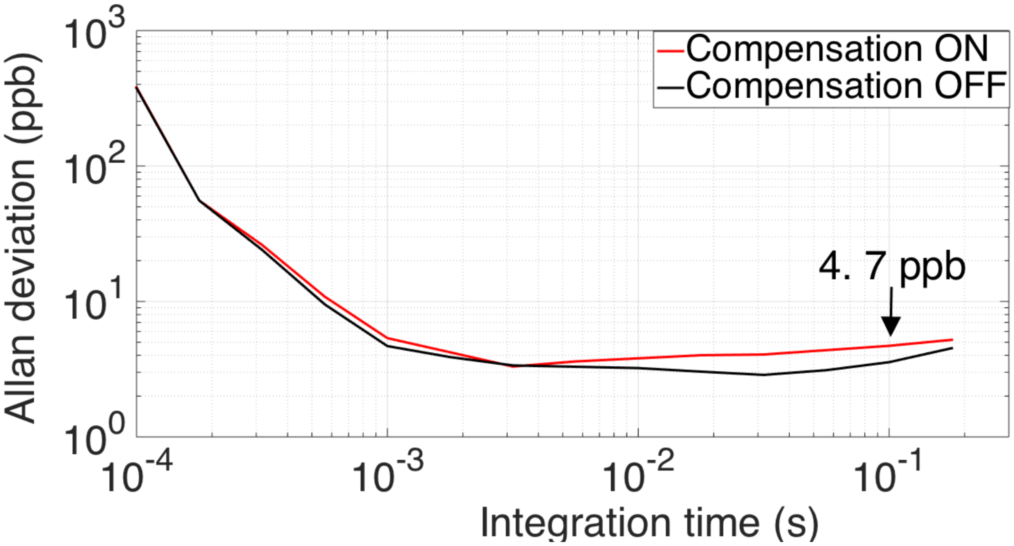


Figure 5.23: Measured Allan deviation

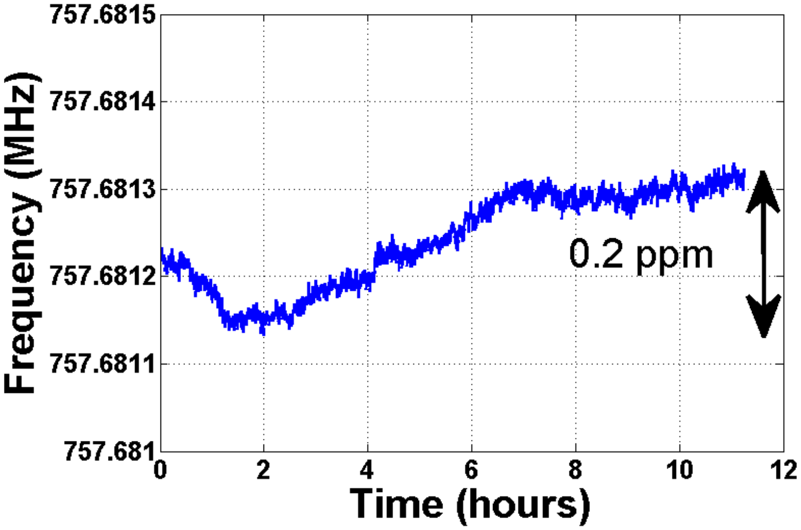


Figure 5.24: Measured frequency of the FBAR reference across 11 hours

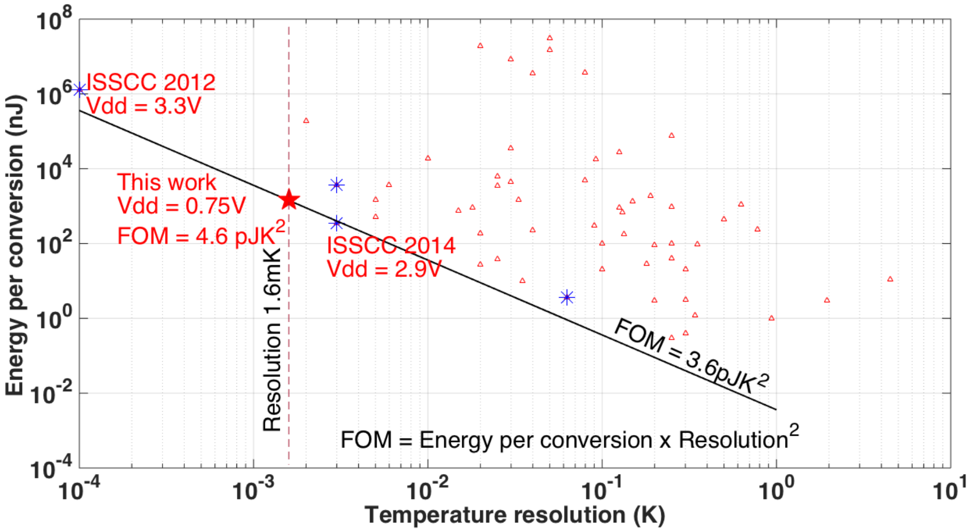
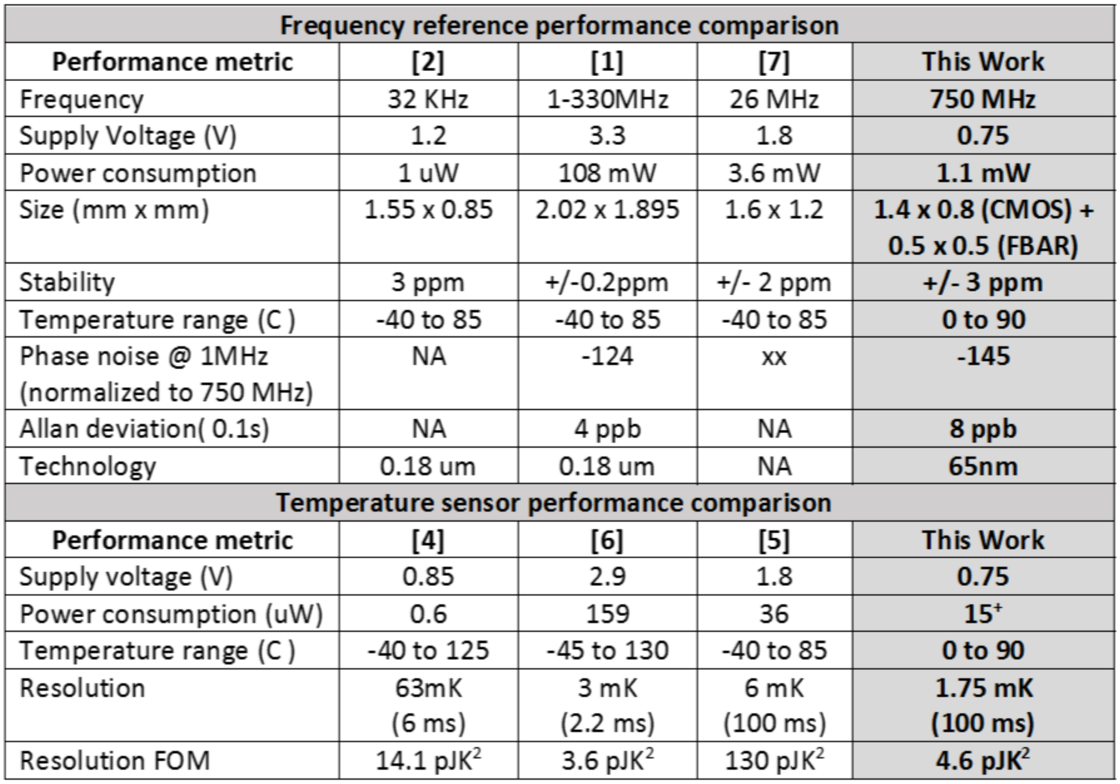


Figure 5.25: Comparison of temperature sensors

5.4 *Chapter summary and conclusion*

Issues from the first prototype were addressed in the second CMOS chip. The second prototype achieves a ± 3ppm stability and 1.1 mW power consumption. A novel temperature sensor architecture was introduced that achieve a 0.75V operation (lowest supply reported to date) and achieves a resolution 3X better than state of the art sub 1V temperature sensors.



Frequency reference performance comparison

Performance metric	[2]	[1]	[7]	**This Work**
Frequency	32 KHz	1-330MHz	26 MHz	**750 MHz**
Supply Voltage (V)	1.2	3.3	1.8	**0.75**
Power consumption	1 uW	108 mW	3.6 mW	**1.1 mW**
Size (mm x mm)	1.55 x 0.85	2.02 x 1.895	1.6 x 1.2	**1.4 x 0.8 (CMOS) + 0.5 x 0.5 (FBAR)**
Stability	3 ppm	+/-0.2ppm	+/- 2 ppm	**+/- 3 ppm**
Temperature range (C)	-40 to 85	-40 to 85	-40 to 85	**0 to 90**
Phase noise @ 1MHz (normalized to 750 MHz)	NA	-124	xx	**-145**
Allan deviation(0.1s)	NA	4 ppb	NA	**8 ppb**
Technology	0.18 um	0.18 um	NA	**65nm**

Temperature sensor performance comparison

Performance metric	[4]	[6]	[5]	**This Work**
Supply voltage (V)	0.85	2.9	1.8	**0.75**
Power consumption (uW)	0.6	159	36	**15$^+$**
Temperature range (C)	-40 to 125	-45 to 130	-40 to 85	**0 to 90**
Resolution	63mK (6 ms)	3 mK (2.2 ms)	6 mK (100 ms)	**1.75 mK (100 ms)**
Resolution FOM	14.1 pJK^2	3.6 pJK^2	130 pJK^2	**4.6 pJK^2**

Figure 5.26: Comparison of prototype - II with other temperature sensors and MEMS frequency references

Chapter 6

A 27μW SUBCUTANEOUS WIRELESS BIOSENSING PLATFORM WITH OPTICAL POWER AND DATA TRANSFER

6.1 Introduction

Barely subcutaneous sensors are implanted in a minimally invasive location just below the skin and provide a direct sensing interface to tissue, fluid, and electrophysiology to enable continuous healthcare monitoring [51]. Ease of sensor placement and aesthetics severely constrain the dimensions of the implant to the mm-scale and necessitate battery-free operation. Currently, most batteryless implanted systems use RF/inductive power and data transfer. While most wireless power transfer systems use a frequency of 13.56 MHz needing larger coils, recently, it has been shown that the optimal power transfer frequencies for mm sized coils is in the GHz range [23]. However, even when operating at the optimal GHz frequencies, power transfer efficiencies for mm sized coils are less than 0.1% [23] [22]. In this work we show that optical power transfer can achieve better efficiency for a barely subcutaneous system and demonstrate a mm scale, batteryless, optically powered implant with bidirectional optical telemetry (see Figure 6.1).

A few papers in the past have proposed optical links for either power or data transfer. [52] presents an integrated bio sensor which runs off 10nW of energy harvested from ambient light but lacks a wireless transmitter. [53] Demonstrates a 16 Mbps optical link for neural recording while transferring power using an inductive link. This system uses off-the-shelf components and the system size is of the order of cm2. [54] demonstrates a 2Mbps optical link through the cornea from an external reader to implant while being powered by a 13.56MHz inductive link in the context of an epi-retinal prosthesis. In contrast to existing

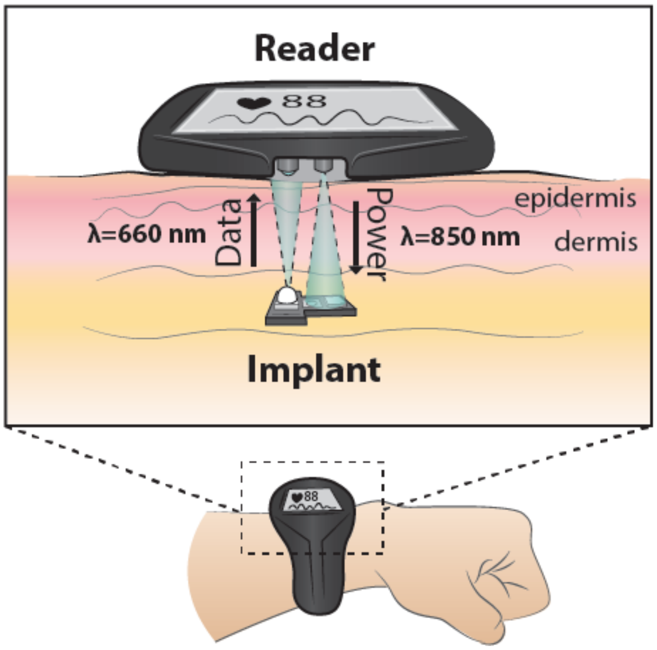


Figure 6.1: Illustration of a barely subcutaneous sensor

works, this work presents a mm-scale realization of an optically powered sensing platform that achieves bidirectional optical telemetry.

6.2 Optical power transfer

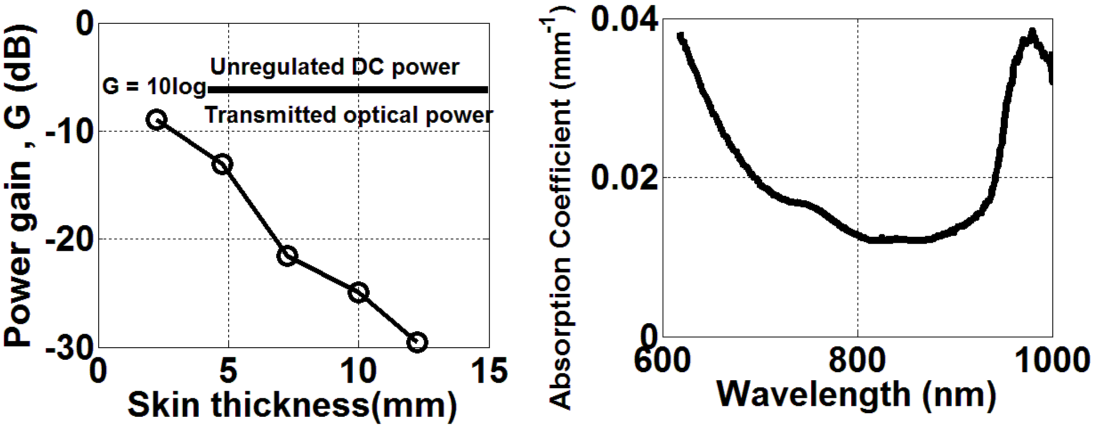


Figure 6.2: Optical path loss through pig skin and measured absorption coefficient from [55]

A barely subcutaneous implant, which is separated only by the skin barrier from the external world, opens up an alternative to inductive power transfer: optical power transfer. Human skin has a transmittance of 20% to 40% in the near-infrared wavelengths (700nm to 1000 nm) [55], which can be exploited for power and data transfer. Measurements using pig skin indicate that we can achieve power transfer efficiency (optical power to usable DC) of 4.9% using an 850nm IR emitter and 2mmx2mm silicon photodiode across a 4.75mm thick skin. Figure 6.2 shows the measured power gain (optical to unregulated DC) across multiple layers of pig skin. Though not suitable for deep implants, optical power transfer outperforms RF/inductive transfer at distances of 2-5mm which is the target reader-to-implant separation for this application. A key consideration for an optical power link is the misalignment between the source and the receiver. Figure 6.3 shows the measured efficiency loss as a function of angular misalignment. For a 10 degree tilt between the source and the receiver planes, we measured an efficiency reduction of 1dB. While the angular misalignment is relatively benign, misalignment in X-Y position is a function of the illumination cone and reader-implant separation. Fortunately, the burden of X-Y alignment can be pushed to the reader by using an array of optical transmitters covering a wider area of skin. The reader can intelligently infer the position of the implant beneath the skin and selectively activate transmitting LEDs in the transmit array.

The American National Standards Institute (ANSI) prescribes a Maximum Permissible Exposure (MPE) of 400 mW/cm2 to human skin at 850nm for long term exposure [56]. As

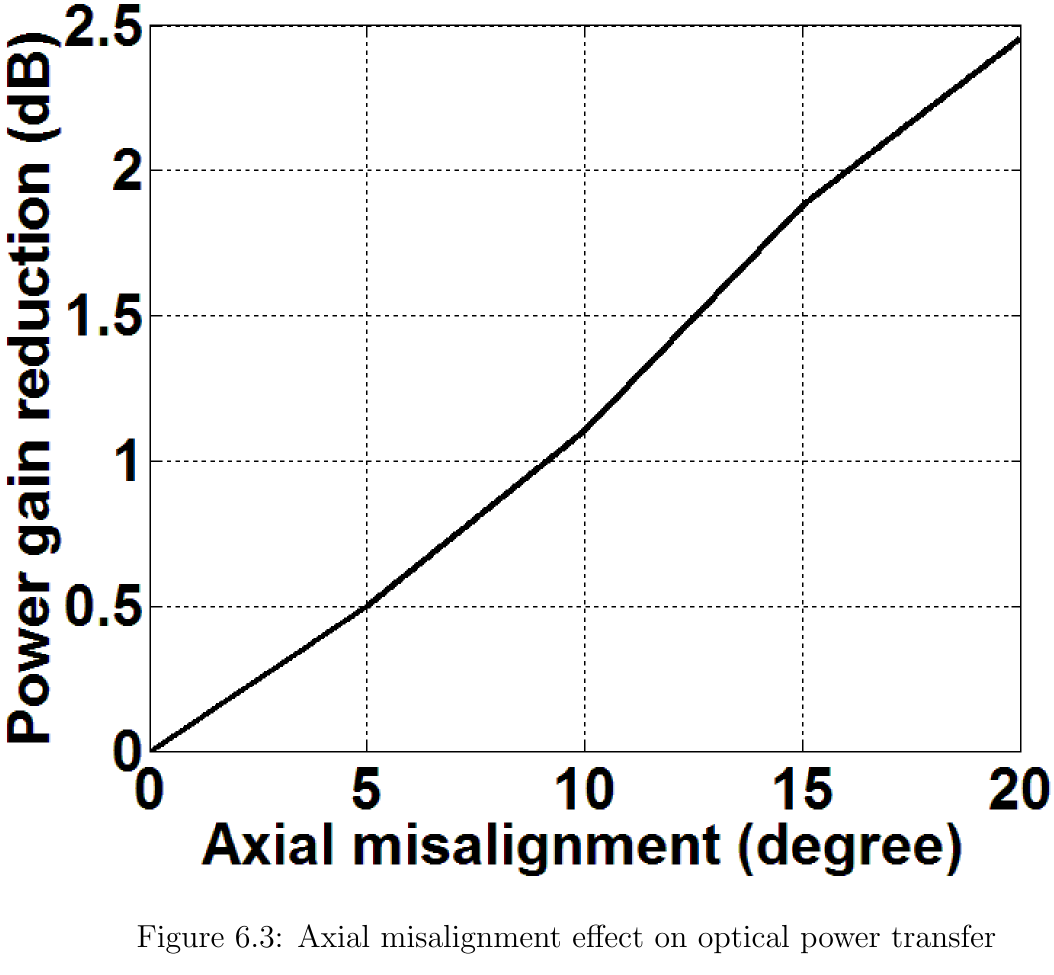


Figure 6.3: Axial misalignment effect on optical power transfer

a point of reference, direct sunlight has a power density of 100 mW/cm2 with about 50% of that power in infrared wavelengths. If we assume an illumination area of (2x2) mm2 for a miniature implant, the transmitted optical power is limited to a maximum of 16 mW. With 4.9% power transfer efficiency, up to 0.8 mW could be harvested. If we assume a conservative exposure limit of 10% of MPE, all sensing and transmission functionalities in the implant should operate within a power budget of ¡80uW, sufficient for many sensing modalities (glucose sensing, for example). The next section describes the architecture and the circuits enabling such a low power sensing platform.

6.3 Implant architecture and circuits

Figure 6.4 shows the architecture of the sensing platform. Our system runs solely from optically transferred energy from a (2x2) mm^2 silicon photodiode and achieves bidirectional optical telemetry with an external reader.

The reader transmits a modulated 850nm optical signal which provides power and data to the implant. The transmitted optical signal illuminates two photodiodes, PD1 and PD2 on the implant. PD1 is a 4 mm2 Si photodiode (Avago technologies) which harvests the optical energy and powers the entire implant. Upon sufficient illumination, this photodiode generates around 0.45V. A switched capacitor boost converter generates a 2V DC rail. A low power bandgap reference and a linear LDO operating from the 2V supply generate a regulated 1.2V.

Optical downlink data from reader to implant is detected by PD2, an on-chip 0.7mm x 0.8 mm CMOS photodiode made from an N-well/P substrate junction. A transimpedance amplifier and slicer senses the generated signal current from PD2 and converts it to a rail to rail digital signal.

Figure 6.5 shows the detailed schematic of the receiver connected to the on chip photodiode. The same optical signal which provides power to the chip also illuminates the data photodiode. The on-chip photodiode generates 1-2 uA signal current, enabling a slicer-based

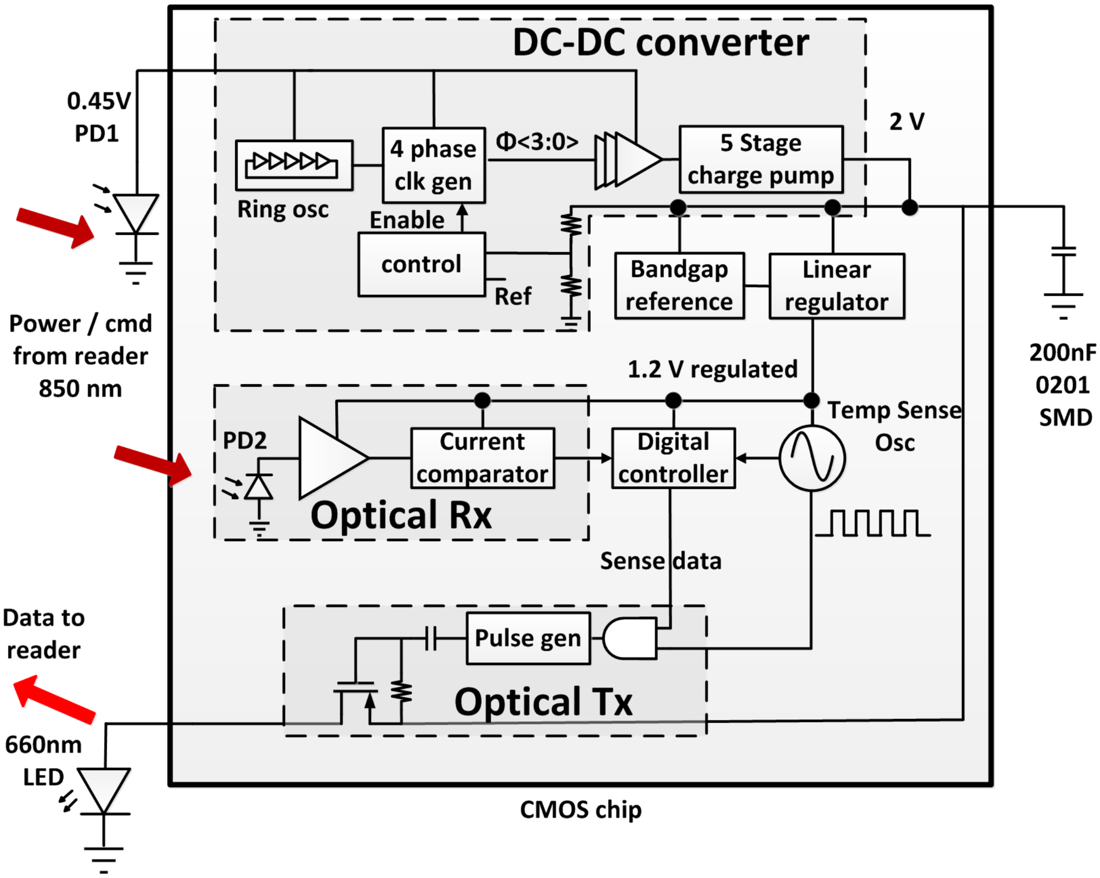


Figure 6.4: Block diagram of the subcutaneous implant

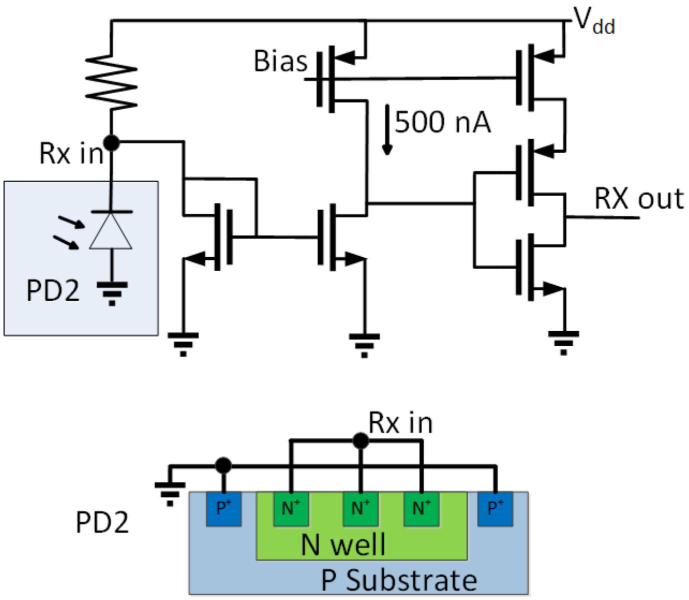


Figure 6.5: Schematic of the fully integrated optical receiver

data detection. The signal from PD2 is mirrored and compared to a reference current of 500nA. Current starved CMOS inverters following the current comparator square up the signal. The receiver consumes 1.5uA from the regulated 1.2V supply. A digital block reads the output of the receiver and interprets the commands from the reader. In this chip we use a frequency counting-based command structure as a proof of concept. The digital block consumes 2.55uW.

The implant uplinks sensed data to the reader through a 16kbps 660nm optical link using an on-implant 3.5 mm x 2 mm 660 nm LED. The transmitter is powered directly from the 2.0 V supply and consumes about 5uW while transmitting with 3% duty cycle. The proposed sensing platform can be used to measure and transmit any biological signal of interest. In this work as a proof-of-concept demo, we measure temperature and transmit it to the reader via the optical link. Temperature measurement is based on the linear frequency to temperature characteristics of a sensor oscillator. The oscillator-based temperature sensor nominally consumes 600 nW.

6.4 Implementation and measured results

All the circuits described in the previous section have been integrated in a 1.5mm x 0.9 mm CMOS IC fabricated using the IBM 130nm process (Figure 6.6). Detailed circuit characterization of the stand-alone CMOS IC was first done. An 8.1 mm x 3.2 mm prototype of the sensing platform, (Figure 6.7) housing the CMOS chip, power photodiode, PD1 and a miniature LED was then realized and tested with a companion reader board.

Figure 6.8 shows the measured outputs of the boost converter and the 1.2V regulator. Figure 6.9 shows the transmitted sensor response over temperature after two point calibration. Figure 9 shows the measured LED voltage at the optical transmitter of the implant. The reader separated from the implant by a pig skin powers up the implant and faithfully detects the optically transmitted signal from the implant (Figure 6.10). Table 6.1 shows the

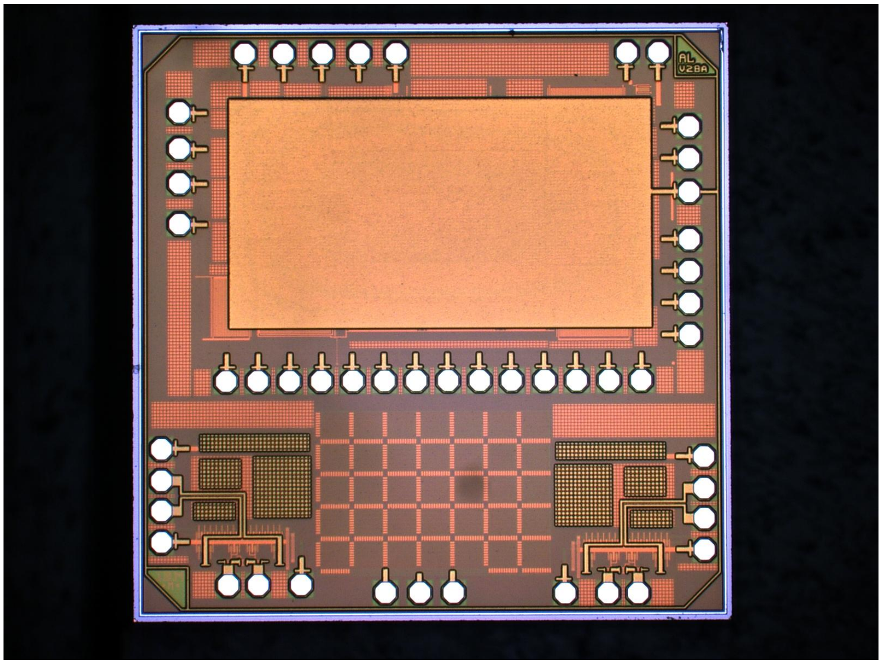


Figure 6.6: Die photo of the CMOS chip

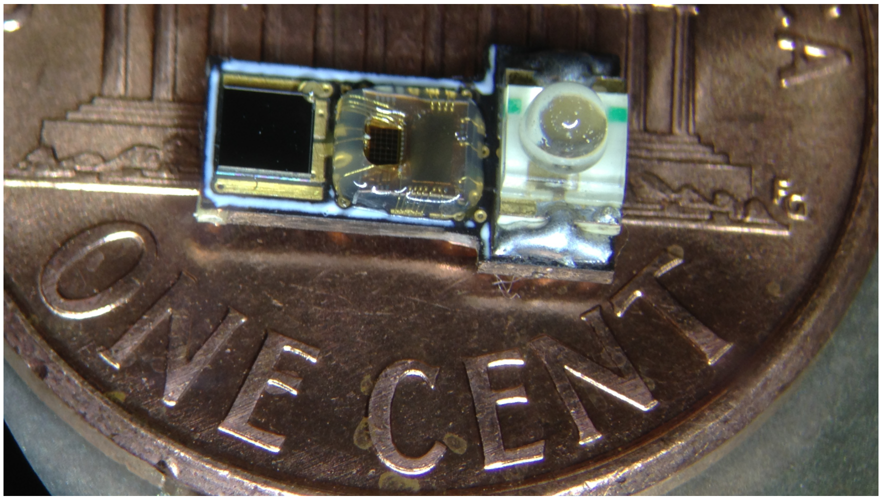


Figure 6.7: Implemented mini board with CMOS chip,LED and photodiode

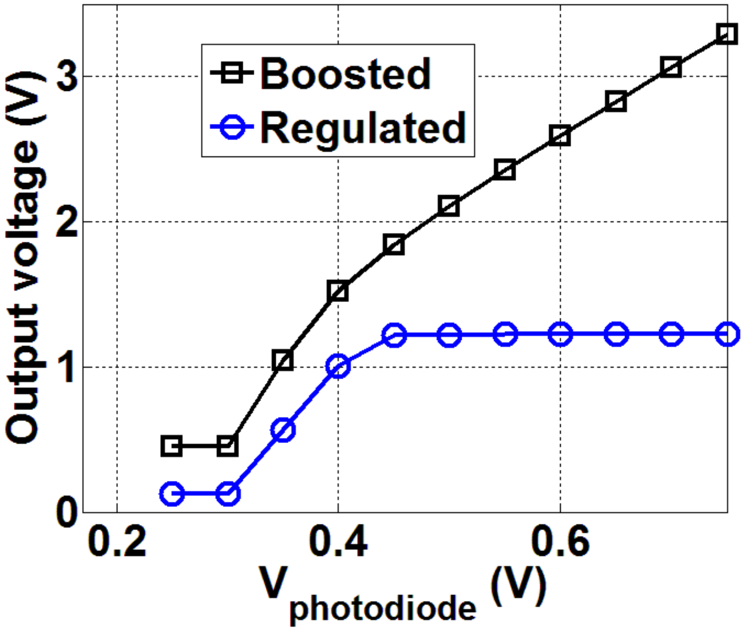


Figure 6.8: Measured power train performance

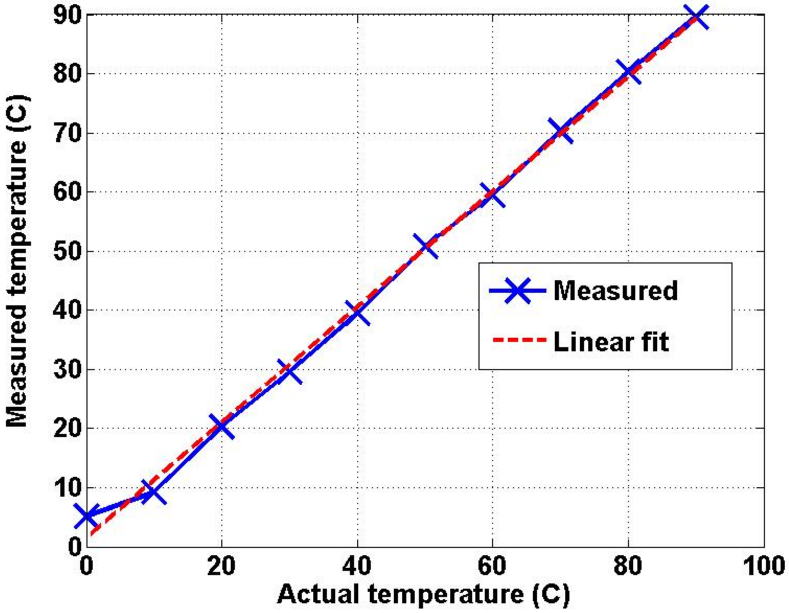


Figure 6.9: Measured temperature from the oscillator based temperature sensor

Table 6.1: Power consumption of the CMOS chip

Block	μW
Optical Rx	1.8
Bandgap + LDO	5
Digital	2.5
Optical Tx	5.3
Temp sensor	0.6
Boost converter	11.6
Total	27

Table 6.2: Performance comparison of power transfer schemes

Performance	ISSCC 2009 [23]	JSSC 2013 [22]	This Work
Coil/ photodiode size	2mm x2mm	0.5mm x 0.25 mm	2mm x 2mm
TX Power	250 mW	50 mW	13 mW
Medium	Bovine muscle	Air	Pig skin
Frequency / λ	915 MHz (RF)	1500 MHz RF	850nm optical
Tx ? Rx distance	15 mm	1mm	4.75 mm
Available power (unregulated DC)	186 uW	10.5 uW	648 uW
Efficiency (%)	0.074	0.021	4.9

power consumption of various blocks of the proposed system.

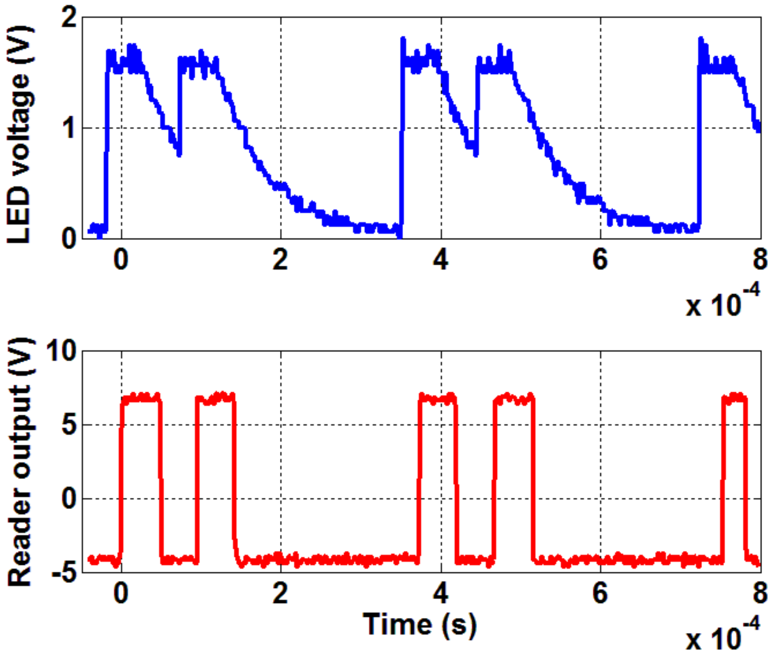


Figure 6.10: Measured outputs of LED and voltage at the reader

Table 6.2 compares optical power transfer with previous mm-scale wireless power transfer works. presented work to the best of the authors' knowledge is the first single-chip bio-sensing platform to demonstrate optical power transfer with full duplex optical telemetry.

Chapter 7

CONCLUSIONS AND FUTURE DIRECTIONS

Wireless sensors have great potential to impact human life and will likely be ubiquitous in the next decade. Miniaturizing these devices will increase their usefulness and enable them to seamlessly blend with the environment. There are several technological challenges that need to be solved. This thesis addressed the problem of miniaturizing the frequency reference needed in a radio. Thin-Film Bulk acoustic resonator (FBAR) based Quartz replacement with suitable performance for wireless radios was demonstrated. This was enabled by the introduction of a novel time-based temperature sensor architecture. Further, close-in-phase noise mechanisms in FBAR oscillator was studied in detail and a cap linearization technique to suppress AM-PM conversion is introduced. This technique will be useful for other non-FBAR high Q oscillators as well.

With the availability of very clean high frequency references available directly at radio frequencies, there is a necessity to take a re-look at radio architectures. Novel PLL free frequency synthesis architectures will be highly useful in reducing cost and power consumption in radios. Further standard CMOS compatible high - Q resonant structures such as the Resonant Body Transistors [57] might also be available for RF designers in the future. This will enable circuit designers to use multiple high Q resonators in radio design instead of the single frequency reference in current architectures.

The last chapter of this thesis demonstrated an optically powered implant. Harvesting enough energy to run circuits will become increasingly difficult as wireless devices get miniaturized. Problem of powering up highly miniature devices will demand technological improvements in multiple technical fields such as battery design, antenna design, fabrication processes, packaging etc. On the circuit design front, we will continue to see more research efforts in designing high efficiency power converters.

Summarizing, highly miniaturized wireless sensors will revolutionize the way we live our lives and circuit designers have a great role to play in making them a reality.

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