Custom High-Speed ADC for mmWave Digital Beamformers

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Abstract

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The movement towards higher data rates has placed pressure on A/D converter systems to achieve a higher sample rate and bandwidth. This thesis aims to explore and implement a nascent idea of using a reconfigurable, oversampled 1-bit converter to achieve a high signal bandwidth and lower power consumption for future use in mm-Wave 5G radios or phased array systems.

The following sections introduces the design process and architecture of a multi-stage Delta-Sigma ADC using a 2x interleaved 1-bit converter that is used in a 50-58GHz 2x2 phased-array (RX) for 5G communication system designed in TSMC 28nm CMOS. The overall phased-array system is given along with a breakdown of the ADC's system functionality with an open-loop 1-bit interleaved comparator and the closed-loop operation of a Delta-Sigma ADC.

The clock rate for the implemented chip is 4GHz with an effective sample rate of 8Gs/s with the interleaved comparators. The interface between the ADC and the digital systems has an

8x polyphase decimation filter to down sample the output of the ADC bit stream by a factor of 8. The maximum achievable SNDR for the Delta-Sigma stage was 24.7dB with a dynamic range of 27dB.

This ADC prototype aims to demonstrate the feasibility of using low-resolution ADCs for digital beamforming for future systems to save on power, area, and complexity for future applications in mm-Wave radios for faster data rates.

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Chapter 1. INTRODUCTION

Since the beginning of modern communication, data converters have been crucial in transforming data into their appropriate types for transmission or reception. The presence of data converters is ubiquitous, from cellphones to televisions, and is the main interface between the outside world and the digital world that links us to the Internet of Things (IoT) [1]. Despite being a huge factor in modern communication, innovation and performance of data converters have stagnated. At present, many commercial data converters are only capable of a few tens of megahertz of signal bandwidth while higher performance data converters are only a few hundred megahertz of bandwidth [2].

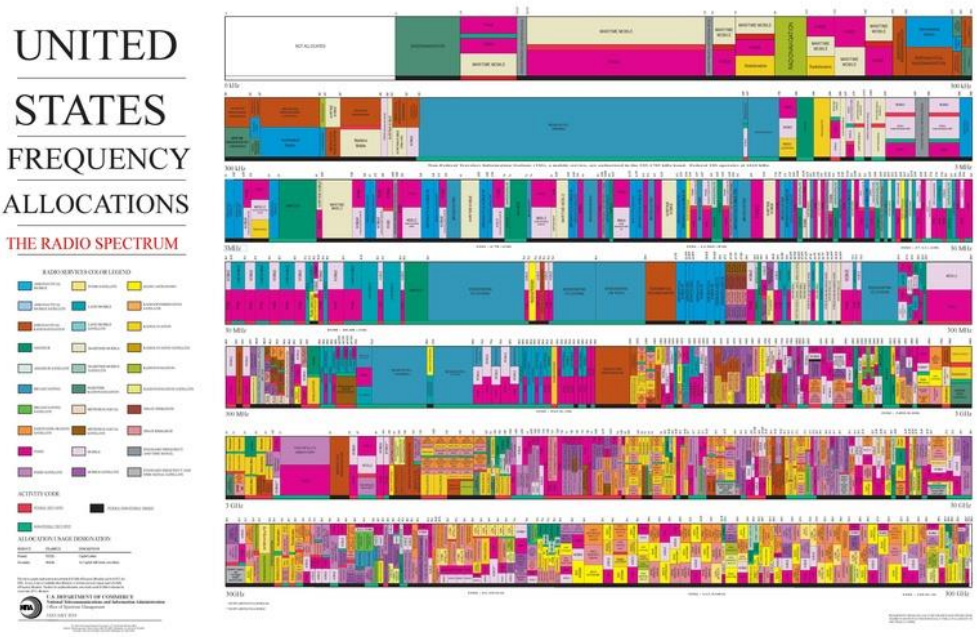


Figure 1.1.FCC frequency allocation in the United States [3]

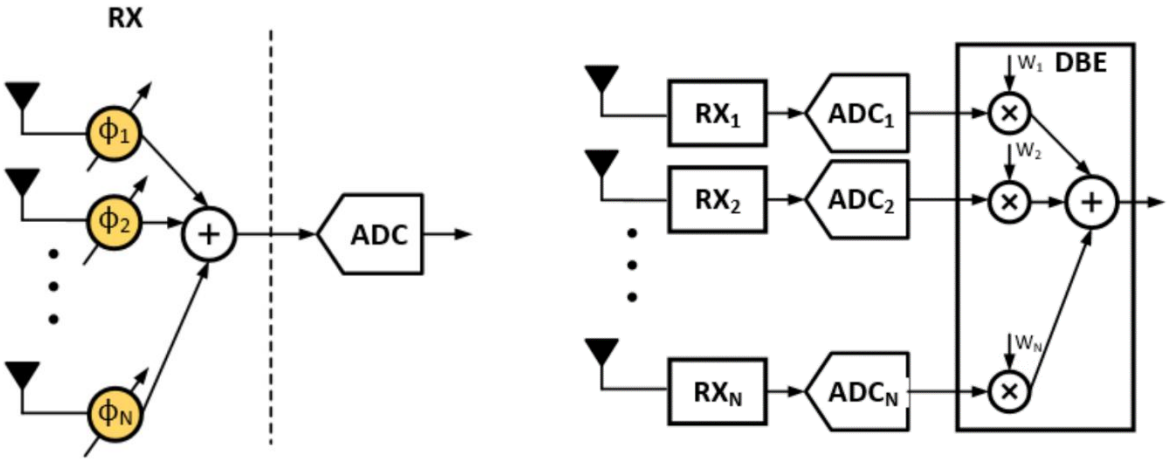
A cause of this limitation in data converters can be attributed to the limited amount of spectrum the FCC can allocate in each communication band. Currently, the communication spectrum from 0-30 GHz is already fully allocated to military usage, broadcasting, radio, WiFi,

etc. As such, present standards for frequencies below 30GHz only allow for an allocation bandwidth of a few hundred megahertz [3]. A more notable instance is the standard 2.4 GHz WiFi that has been in use for over a decade. The IEEE 802.11n standard that 2.4 GHz uses has a maximum signal bandwidth of 90 MHz from 2.412 to 2.484 GHz, and that 90 MHz bandwidth is further divided into 14 overlapping channels that are either 20 MHz or 40MHz wide depending on the modulation scheme of the data that is being received [4]. With recent advancements in scaling transistors smaller, data converters designed for the full 90 MHz signal bandwidth can be trivial when leveraging proven architectures and enhanced performance in smaller transistors. Motivation for increasing the performance data converters, as a result, has not been previously presented until now.

Current commercial focus is on the next generation of communication frequencies above 30 GHz, opening a whole new paradigm of standards and commercialization [5]. With the increase of carrier frequency, a natural increase in the signal bandwidth is also expected. What was a few hundred megahertz has now multiplied to few gigahertz wide, an increase of bandwidth of over ten times in some cases. Traditional data converters now struggle with such large increase in bandwidth requirements, and the research opportunities for gigahertz range data converters blossomed in the last several years. In particular, A/D converters (ADC) are at the forefront of interest as they are usually the limiting factors in high frequency receivers.

ADCs occupy the important role of sampling the incoming signal that the receiver picks up and discretizing the received signal for the digital backend to decode and process. As mentioned previously, the resolution and bandwidth of ADCs were determined by existing standards set by the FCC for each allocated channel. These current standards did not prove adequate motivation to

innovate ADC architectures, but now focus has shifted to developing high-performance ADCs for phased array systems in next generation communication systems.



(a) (b)

Figure 1.2. Phased array system for (a) analog beamformer (b) digital beamformer

Phased array systems are made of up of multiple receivers structured in a line or a set pattern to achieve multiple-input and multiple-output (MIMO) or beamforming. Each receiver has its own ADC in the case for MIMO, but the ADC requirements changes for phased-array beamformers. Beamforming arrays can be classified into either digital or analog arrays. Traditional analog beamformer like in Figure 1.2a arrays require one high resolution ADC that samples a reconstructed signal from multiple elements (receivers) in the array. New digital arrays, however, require one low resolution ADC for each element in the array before summing the signal together as shown in Figure 1.2b [6]. Both types of beamformers are being used today, but digital arrays are more suited for wider bandwidth and higher frequency applications due to needing low resolution ADCs.

1.1 TRADITIONAL ADC SYSTEMS

The design of ADCs is a tradeoff between resolution, speed, power, and area. This section briefly explores two traditional ADCs that have different design philosophies: the successive approximation register (SAR) and the flash converter.

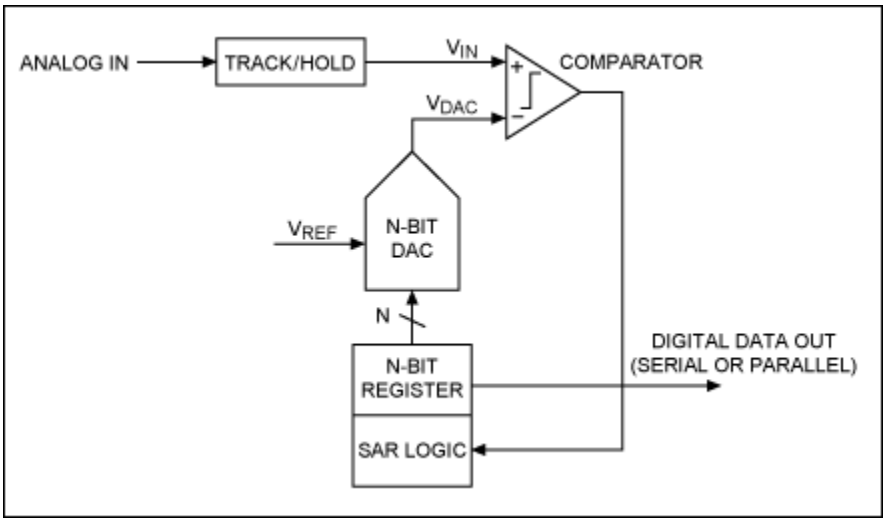


Figure 1.3. General structure of a SAR ADC [7]

SAR ADCs function like a binary search algorithm where a comparator will output either a 1 or 0 if the input signal is above or below the DAC output as seen in Figure 1.3. The output of that comparator is then stored into a bank of registers and the DAC voltage output will update accordingly. The main benefit of this system is that increasing the effective number of bits (ENOB) of the system simply requires increasing the bank of registers which is trivial in digital logic [7]. However, the DAC needs to accurately settle within a sample period and the comparator needs to be capable of resolving minor voltage differences between the input signal and the DAC voltage. These requirements increase the design complexity of the analog blocks and inherently lowers the frequency that this system can operate at [7]. As a result, SAR ADCs are great for high resolution, low bandwidth operation, and the power consumption and area usage is relatively minimal compared to other ADC structures.

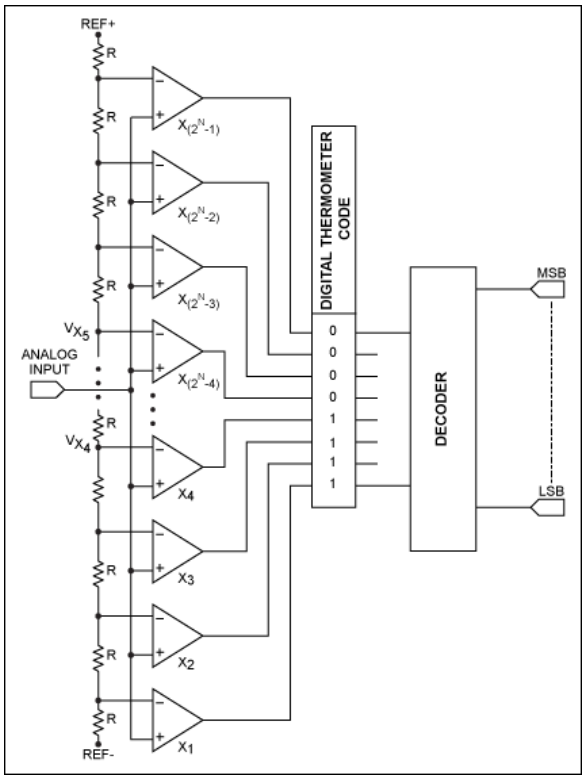


Figure 1.4. General structure of a Flash ADC [7]

On the other hand, the main purpose of flash ADCs is in low resolution, high bandwidth applications, completely in the opposite domain of SAR ADCs. Flash ADCs consist of a ladder of comparators and resistors that determine the resolution of each bit. There is usually some combinational logic at the output of the comparators that converts the thermometer code into binary code and help with error correction in the code as well. Such a simple design allows flash ADCs to excel in high-speed quantization. However, the number of comparators required is 2^N, where N is the ENOB of the system. This indicates that for each increase of ENOB, the number of comparators doubles, leading to drastic power consumption and area usage for high resolution flash ADCs [7].

1.2 MOTIVATION

With the interest for faster communication protocols and higher carrier frequencies, traditional ADC systems, like both the SAR and Flash, have difficulty meeting these new standards. Flash ADCs are great for high-speed applications but struggles with justifying a large power consumption for a high ENOB required in higher modulation schemes. On the other hand, SAR ADCs can achieve a high ENOB with low power consumption but are limited in their signal bandwidth due to settling issues. Such a requirement of high resolution and wide bandwidth ADCs bends the current paradigm of ADC design and has generated increasing research interest in solving this issue.

One common solution is the use of Delta-Sigma Modulators (DSM) as ADCs. DSM systems have been around for a while but have fallen to the wayside as they did not provide any major benefits compared to SAR or Flash architectures in the past. Yet, DSMs have re-emerged within the last decade as the primary ADC candidate for future communication standards due to their noise shaping ability that allows a high ENOB across a wide bandwidth [2]. The main goal of this thesis is to introduce the implementation of a high-speed multi-stage 1-bit DSM ADC with a signal bandwidth of 2 GHz and an effective sampling frequency of 16 GHz across 2x interleaved comparators. The following chapter goes in depth into the design and functionality of DSM to establish a foundation for the reader before introducing the system architecture and the circuit implementation.

Chapter 2. DELTA-SIGMA MODULATORS

The basic idea of DSM was first introduced as a variation of Delta modulation by Inose et. Al. in 1962 [8]. Back then, delta modulation was typically used in biomedical and speech receivers,

but the transceiver's non-linearity injected itself in the feedback loop and effected the accuracy of the quantization. DSM was supposed to fix this issue, but the idea spun into something more with DSM becoming attractive due to their insensitivity to analog components and high resolution.

2.1 Operation of delta-Sigma Modulators

Fundamentally, a DSM is a moving average filter that continuously approximates the input signal and is primarily an oversampling data converter. Figure 2.1 shows the basic structure of a DSM structure with the building blocks for a DSM structure consisting of a loop filter made up of integrator(s), a low resolution quantizer, and a D/A converter (DAC) in the feedback path. Since DSM ADCs are in the mixed-signal domain for circuits, a DSM ADC can be built in either continuous time (CT) or discrete time (DT). Typically, CT DSMs can have a much higher sampling frequency compared to DT DSMs and require lower integrator specifications but suffer to increased sensitivity to RC variations in the integrator [9] [10]. DT DSMs, on the other hand, require high bandwidth and high gain opamps for the integrators to allow for faster settling times between blocks, but are immune to the integrator's capacitor mismatches due to process variations because of this fast-settling requirement [9]. Both have DT and CT variations have their applications, but the main advantage of CT systems is their implicit anti-aliasing response that comes from the CT loop filter.

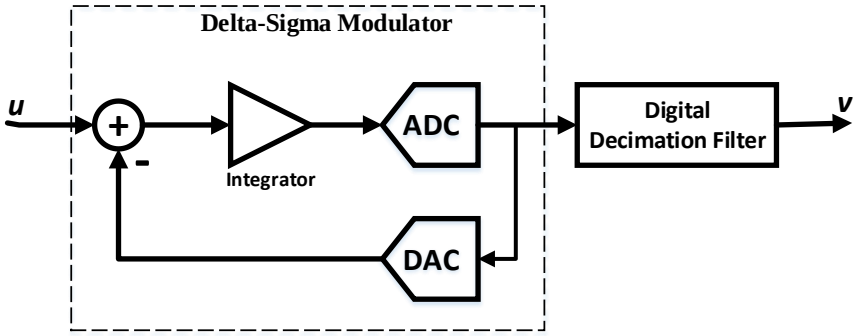


Figure 2.1. A simple Delta-Sigma modulator structure

As mentioned before, DSMs are oversampling converters. Oversampling converters differ from Nyquist converters as they sample at a frequency much higher than the Nyquist rate of $2f_{BW}$ where f_{BW} denotes the signal bandwidth. The ratio of the sampling frequency (f_S) compared to the Nyquist frequency is given by the oversampling ratio (OSR):

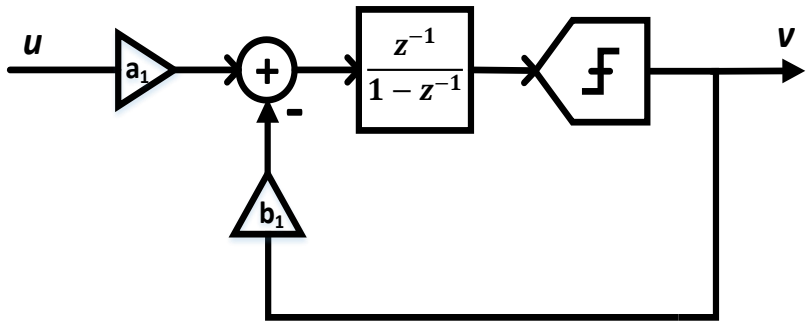
$$OSR = \frac{f_S}{f_{BW}} \tag{2.1}$$

A benefit for a high OSR is applicable to every oversampling converter where the signal-to-quantization noise (SQNR) is decreased within the signal bandwidth. The decrease of the in-band noise (IBN) is inversely proportional to the OSR given the step size (Δ) of the quantizer inside of the ADC.

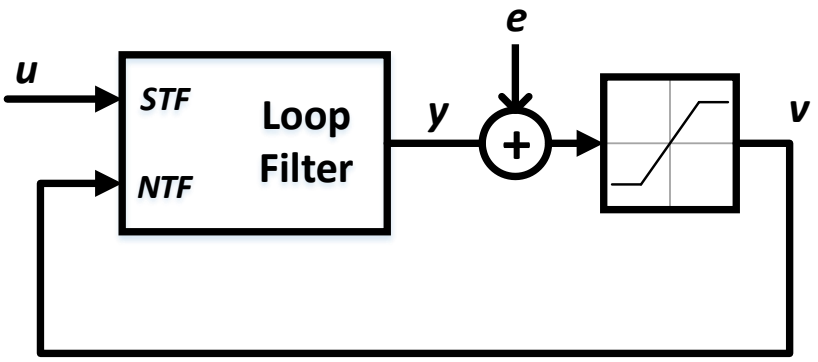
$$IBN = \frac{\Delta^2}{12(OSR)} \tag{2.2}$$

A qualitive explanation is that the quantization error for each sample is smaller now due to the small-time difference between samples, increasing the chance the sampled outputs are approximating the input signal better. These high-speed repetitive samples are combined in a decimation filter after the DSM ADC to represent the voltage level of the input signal more accurately across one down sampled data point.

A more key aspect of DSMs is its inherent ability to noise shape the quantization error. The DSM system has two closely related transfer functions, one that effects signal and one that effects noise. The signal transfer function (STF) is closely related to the pole-zero response of the loop filter and the negative feedback loop and is designed to have unity gain within the signal bandwidth as to not exacerbate non-linear effects in the system. The noise transfer function (NTF) is caused by the negative feedback and is where the noise shaping comes from. The NTF looks like a high-pass filter that pushes all the quantization noise from lower frequency out towards higher frequency.



(a)



(b)

Figure 2.2. (a) 1st order discrete-time DSM (b) a simplified model of a DSM [9].

To simplify the analysis for Figure 2.2a, the system is converted into a simpler model like in Figure 2.2b and analyzed in the ℤ-domain. The quantizer is modeled as the quantization error (e) that is being added to the output $y[n]$ and the input is defined as a continuous signal u. The entire system transfer function can now be generalized to:

$$Y(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \tag{2.3}$$

Where $Y(z)$, $U(z)$, and $E(z)$ are the ℤ-domain equivalent of the output, input, and quantization error respectively. The equations for just the STF and NTF would give:

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{2.4}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{2.5}$$

$H(z)$ is given as the common $\mathbb{Z}$-domain polynomial between the STF and NTF. Since the feedback loop effects both the NTF and STF, a characteristic of a DSM system is that the denominator in both transfer functions is the same and that the poles of the STF are the zeros of the NTF [9] [11].

Also, the OSR of the DSM keenly affects the location of poles of the NTF. Typically, the sampling frequency of the DSM is normalized to the unit circle in the $\mathbb{Z}$-domain and the location of the zeros in the NTF all lie on the unit circle. If the $OSR >> f_{BW}$, then the location of the poles is generally close to the unit circle. Having the poles closer to the unit circle, and the zeros for that matter, increases the stability of the given DSM system. Therefore, it is common for a DSM to have an OSR of at least 32 in most design specifications as the high OSR provides greater stability [9].

With noise shaping and oversampling, the performance of DSM ADCs is better than the performance of other ADC systems in a straight comparison. The signal-to-noise (SNR) ratio of a typical ADC is classified by the well-known equation in Eq. 2.6 where N is the number of bits in the quantizer of the ADC.

$$SNR = 6.02N + 1.76 + 10log(OSR)\, dB \tag{2.6}$$

While DSM still follows this equation, the noise shaping of the DSM must also be accounted into the equation. Taking the DSM in figure Figure 2.2a for instance, doubling the OSR every time results in a 9dB increase instead. The SNR of the DSM system is now:

$$SNR = 6.02N + 1.76 + 9(OSR)\, dB \tag{2.7}$$

Increasing the OSR in a DSM yields a higher SNR than what a typical ADC with the same OSR would give. However, Figure 2.2a only shows that the loop filter is made up of one integrator which makes $H(z)$, and the resulting STF and NTF, only a 1st order equation which limits the noise shaping of the system.

2.2 HIGHER ORDER DELTA-SIGMA

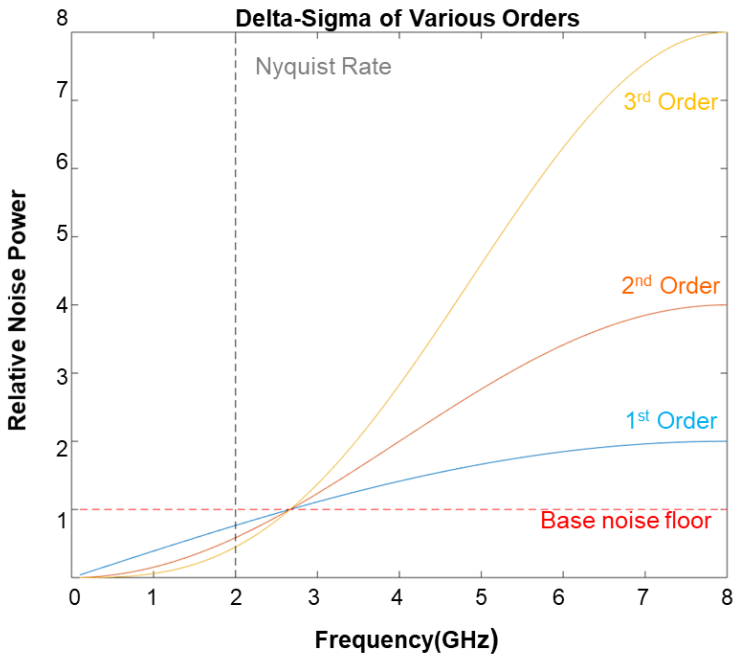


Figure 2.3. The magnitude of noise shaping of for higher order DSMs.

The use of only one integrator in Figure 2.2a DSM only allows a 9dB SNR increase each time the OSR is doubled due to the slope of the noise shaping only being 20dB/decade. While this SNR increase is still better than what a normal ADC gives, increasing the OSR even further to achieve a higher SNR is not very power efficient. Thus, the idea of nesting DSMs within each other came to be [9]. By nesting the DSM loops, the order of the loop filter increases, allowing for more aggressive noise shaping like in Figure 2.3 at the cost of adding more integrators. However, stability becomes more of a concern the higher the loop order is from the increase of poles and zeros in the system. Different system architectures were developed to alleviate stability concerns. The two most used architectures are the feedforward (FF) and the feedback (FB) methods [9] – [12].

2.2.1 *Feedback Architecture*

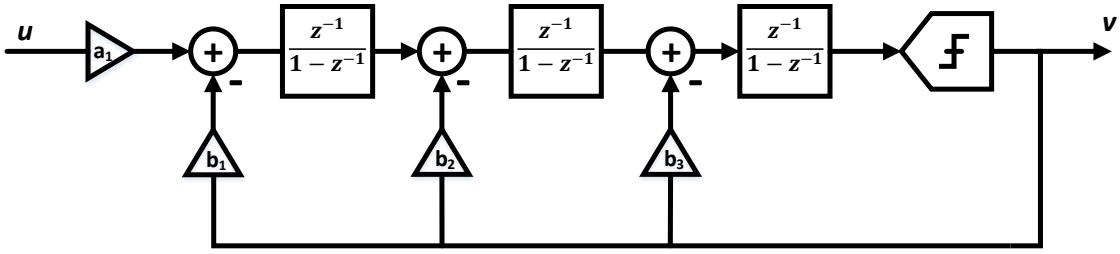


Figure 2.4. A 3rd order DSM with a feedback architecture.

The FB architecture is probably the more recognized of the two methods and is more straightforward. Additional DACs are used to connect the feedback path to the intermediate nodes between integrators as shown in Figure 2.4. The gain blocks in the feedback path control the pole-zero locations of the loop filters and are usually implemented as a resistive or capacitive ratio at the virtual short node of the integrator. The system response of the Figure 2.4 is given as

$$STF = \frac{b_1 z^{-3}}{(1-z^{-1})^3 + a_3 z^{-1}(1-z^{-1})^2 + a_2 z^{-2}(1-z^{-1})^1 + a_1 z^{-3}} \tag{2.8}$$

$$NTF = \frac{(1-z^{-1})^3}{(1-z^{-1})^3 + a_3 z^{-1}(1-z^{-1})^2 + a_2 z^{-2}(1-z^{-1})^1 + a_1 z^{-3}} \tag{2.9}$$

Looking closely, Eq. 2.8 and Eq 2.9 both satisfy Eq. 2.4 and Eq. 2.5 and both NTF and STF have the same denominator. The magnitude response of the STF rolls off as z^{-3} at higher frequencies which is great for wireless applications where a steep roll off is needed to differentiate between channels [9] [11]. The DC gain of the system can be quickly inferred to be $STF(z=1) = {b_1}/{a_1}$ which is designed to be unity. A negative aspect of the FB method is that each FB path needs a DAC to convert the quantized signal back to the continuous domain. Another concern is that each integrator contains some correlation to the input signal due to the additional FB paths and so the voltage swings at these intermediate nodes are relatively large [9].

2.2.2 *Feedforward Architecture*

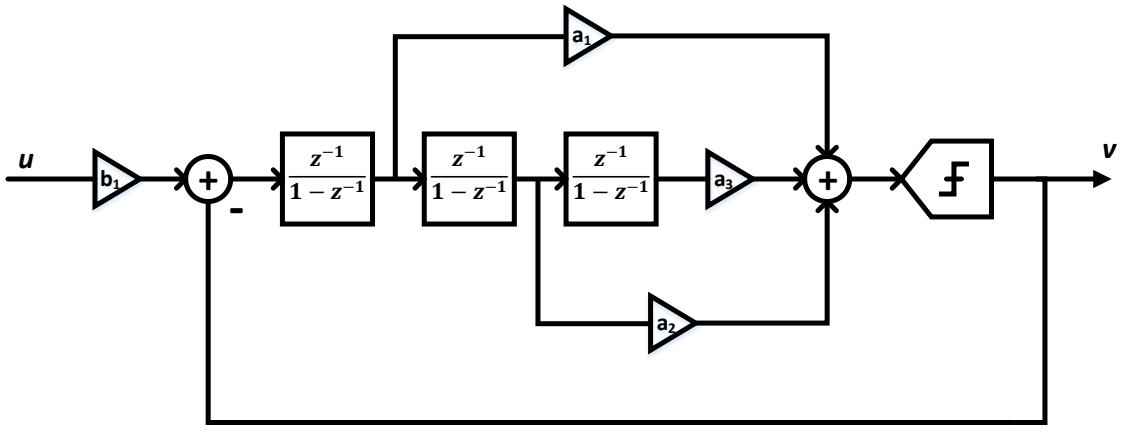


Figure 2.5. A 3rd order DSM with a feedforward architecture.

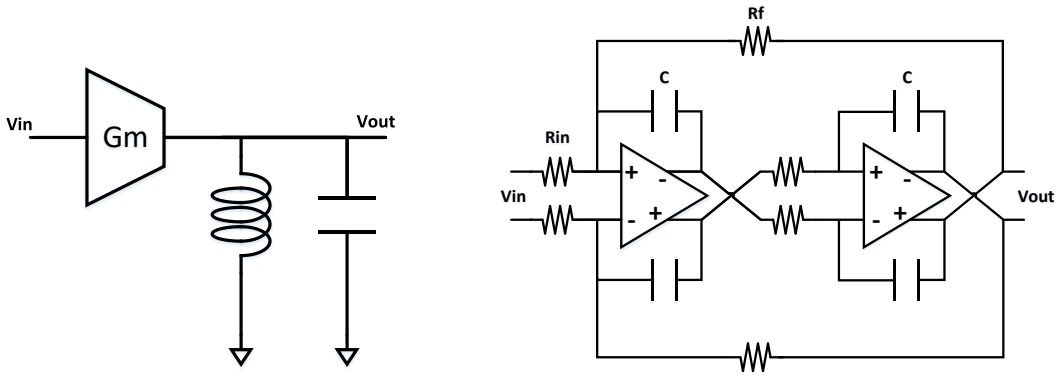
The FF structure relies on feeding the signal from the intermediate nodes to the input of the quantizer and only requires the minimum of one DAC to establish the feedback loop. The gain stages are still present in the FF paths in the loop filter, and they still control the pole-zero locations of the loop filter. Finding the STF and NTF of Figure 2.5 will still result in Eq. 2.8 and Eq. 2.9, respectively. However, the FF paths introduce additional zeros in the STF resulting in peaking in the out of band (OOB) magnitude response before rolling off as z^{-1} [9] [11]. The OOB peaking is not desirable in wireless applications as the peaking can possibly extend the bandwidth into the next channel [9] [11]. Yet, the FF structure remains the more popular of the two methods. With only one feedback loop, the output of each integrator contains only integrated noise which only has a small voltage swing. Therefore, only the first integrator in the system needs to be high performance, particularly from an output voltage swing perspective, while the subsequent integrators in the chain can have more relaxed specifications.

2.2.3 *Other Design Methods*

A less common method is combining both feedforward and feedback methods into a hybrid FF-B structure. The FF-B method aims to combine the benefits of both FF and FB methods while retaining only parts of their drawbacks. However, design and analysis of such a hybrid structure is

more complicated and less straightforward. FF-B method borders the subject of control systems instead and requires the designer to have an extended knowledge of control theory and state-space descriptions. Nevertheless, FF-B structures have gained interest with their ability to control the DSM's frequency response more accurately, particularly when combining them with FIR-DACs to create low distortion DSM ADCs [9] [13].

Another interesting technique that is commonly used is creating a local resonator within the loop filter. A resonator is created through a weak feedback around two integrators or the use of an LC tank. The main purpose of incorporating a resonator is to create a pair of complex zeros in the Ƶ-domain on the unit circle. The complex pair creates a notch, or a ripple depending on how many pairs exist, in the NTF within the passband. The notches increase the SQNR at low frequencies, but decreases the SQNR at the high end of the signal bandwidth allowing for an overall decrease of the IBN. Resonators are great for low OSR DSMs as the complex zeros allow for the optimization of the IBN across a wide signal bandwidth [9] – [12].



(a) (b)

Figure 2.6. DSM band pass topologies using (a) an LC tank (b) an active-RC resonator.

The performance of these higher order DSM is now difficult to capture with Eq. 2.6 and Eq. 2.7. The order of the DSM determines how aggressive or steep the noise shaping slope is,

further reducing the IBN. In [14], the author gives an SNDR equation for any given DSM loop order L and its OSR:

$$SNR = 6.02N + 3.01(OSR)(2L+1) - 9.36L - 2.76\,dB \quad (2.10)$$

Applying a 1st order DSM into Eq. 2.10 will give the same result as Eq. 2.7. Increasing the loop to be 4th, 5th or even 6th order to increase the DSM's resolution is possible but carries a large risk of the system being unstable. To combat this, engineers have placed DSM systems in parallel with each other, creating multi-stage DSM systems that carry a low risk of instability while still achieving high resolution.

2.3 Multi-Stage Delta Sigma

Multi-stage DSM structures relies on parallelizing multiple DSM systems to maintain a high ENOB while decreasing the risk of system instability. Since the DSM systems are parallel, the stability for each DSM stage is independent of one another, but the performance of the cascaded systems is the sum of the loop orders in each stage [9] – [12]. Another benefit that cascaded DSMs bring is inherent dithering. With quantization noise typically assumed to be white, the addition of another quantizer sampling the quantization error of another stage can be thought of as the addition of two uncorrelated noise sources. As such, cascaded DSMs typically do not need dithering blocks to decrease the spurs in the frequency spectrum [9] [11].

2.3.1 *Multi-stage Noise Shaper (MASH)*

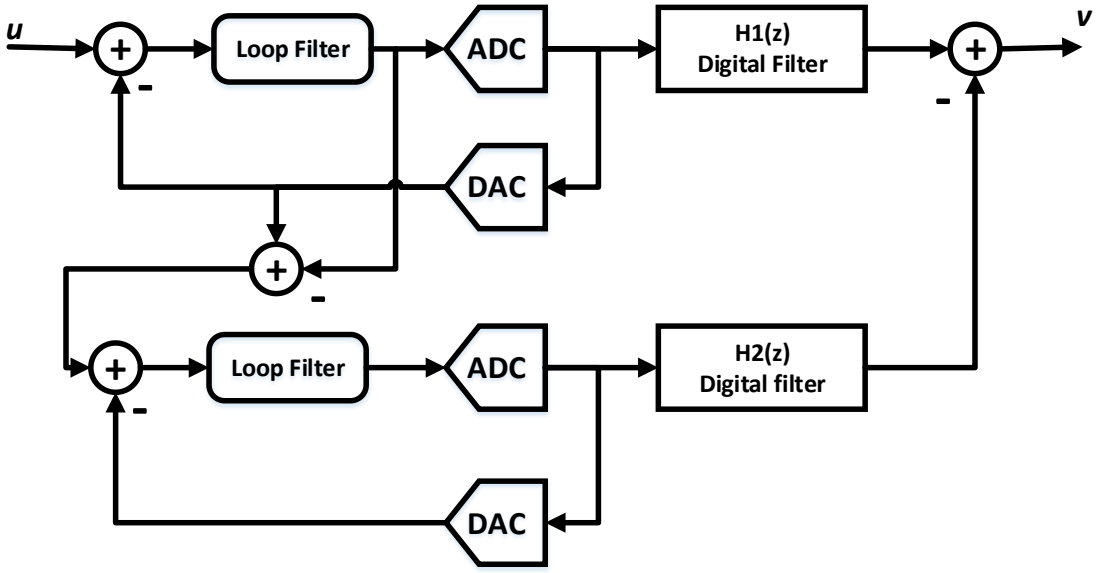


Figure 2.7. A generic 2-stage DSM multi-stage noise shaper (MASH).

The quantization error from the 1st stage is extracted and fed into the 2nd stage of the MASH. The 2nd stage samples the quantization error of the 1st stage before both stages are combined through a subtraction in the digital domain. The transfer functions of the 1st and 2nd stage are given below

$$V_1 = STF_1(z)U(z) + NTF_1(z)E_1(z) \tag{2.11}$$

$$V_2 = STF_2(z)E_1(z) + NTF_2(z)E_2(z) \tag{2.12}$$

The digital filters H_1 and H_2 are designed so that E_1 is canceled out at $V(z)$ which requires:

$$NTF_1(z)H_1 - STF_2(z)H_2 = 0 \tag{2.13}$$

The easiest way to do so is to set $H_1 = STF_2$ and $H_2 - NTF_1$ which will result in the overall system equation given below:

$$V = STF_1 \cdot STF_2 \cdot U - NTF_1 \cdot NTF_2 \cdot E_2 \tag{2.14}$$

As seen in Eq. 2.14, the quantization error is shaped by both NTF1 and NTF2, indicating that the order of the noise shaping is determined by NTF of both stages but the stability of each stage is still independent [9] [11] [12]. However, the overall MASH systems suffer heavily from

mismatch between the transfer functions of the stages. The variability of the NTF and STF from the loop filter due to imperfections from implementation or fabrication makes it difficult to satisfy Eq. 2.13. The mismatches will cause E_1 to be amplified through the loops and appear at the output, decreasing the noise performance of the system heavily. The concern of the noise leakage of E_1 makes the MASH system a high-sensitivity noise canceller and is not optimal for high sampling applications [9]. An example of a MASH system can be found in [15] where a discrete version was implemented.

2.3.2 *Sturdy MASH*

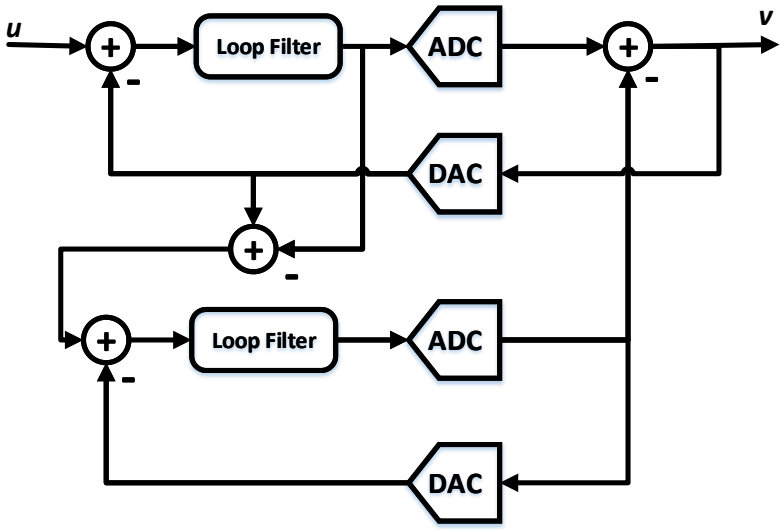


Figure 2.8. A generic 2-stage DSM Sturdy-MASH (SMASH).

The high sensitivity of MASH structures can be reduced, or mitigated, through a small modification that will eliminate the use of matching digital filters $H_1(z)$ and $H_2(z)$. The modification can be seen in Figure 2.8 where the subtraction of both stages is done in the 1st stage after the quantizer and before the point where the output v is fed back to the input. The resulting system change gives the overall transfer function

$$V = STF_1 \cdot U - NTF_1 \cdot NTF_2 \cdot E_2 + NTF_1 \cdot (1 - STF_2) \cdot E_1 \qquad (2.15)$$

A curious observation from Eq. 2.15 is that the cancellation of E_1 is now required by $NTF_1 \cdot (1 - STF_2) = 0$ or more simply $(1 - STF_2) = 0$. Such a requirement is impossible to satisfy as STF_2 must be delay-less to cancel out E_1. However, the magnitude E_1 can still be minimized through the careful design of STF_2. Selecting $STF_2 = 1 - NTF_2$ now allows E_1 to also be noise shaped through both NTFs, but locks the design of the 2nd stage to be an FF implementation. The function now yields

$$V = STF_1 \cdot U - NTF_1 \cdot NTF_2 \cdot (E_2 + E_1) \tag{2.16}$$

The transfer function now indicates that the digital matching blocks are not needed and the overall system is now a low-sensitivity noise shaper instead. The modified architecture is adequately named a Sturdy MASH (SMASH) due to maintaining the performance of a normal MASH while being robust against imperfections in the transfer functions [9].

2.4 Current Trends

The current trends for ADC designs seems to favor MASH/SMASH architectures for high resolution applications with the 1st stage usually being a high order DSM. Off shoots of the MASH architecture have also been created like the Zoom ADC [16] or incremental ADC [17] but neither are great for high-speed sampling operations due to their reliance on digital blocks within the system. As such, CT-DSMs are still the choice candidate for a high-speed operation in mm-Wave applications. The use of noise shaping and oversampling to further enhance the ENOB of a low resolution quantizer fits well with digital phased-array requirements of a low-resolution ADCs in each element. The introduction of a 1-bit 0-3 CT MASH architecture designed for digital phased array systems is now being introduced.

Chapter 3. SYSTEM ARCHITECTURE

This section aims to introduce the system design of the CT MASH DSM that was designed for a digital phased array system at mm-Wave frequencies.

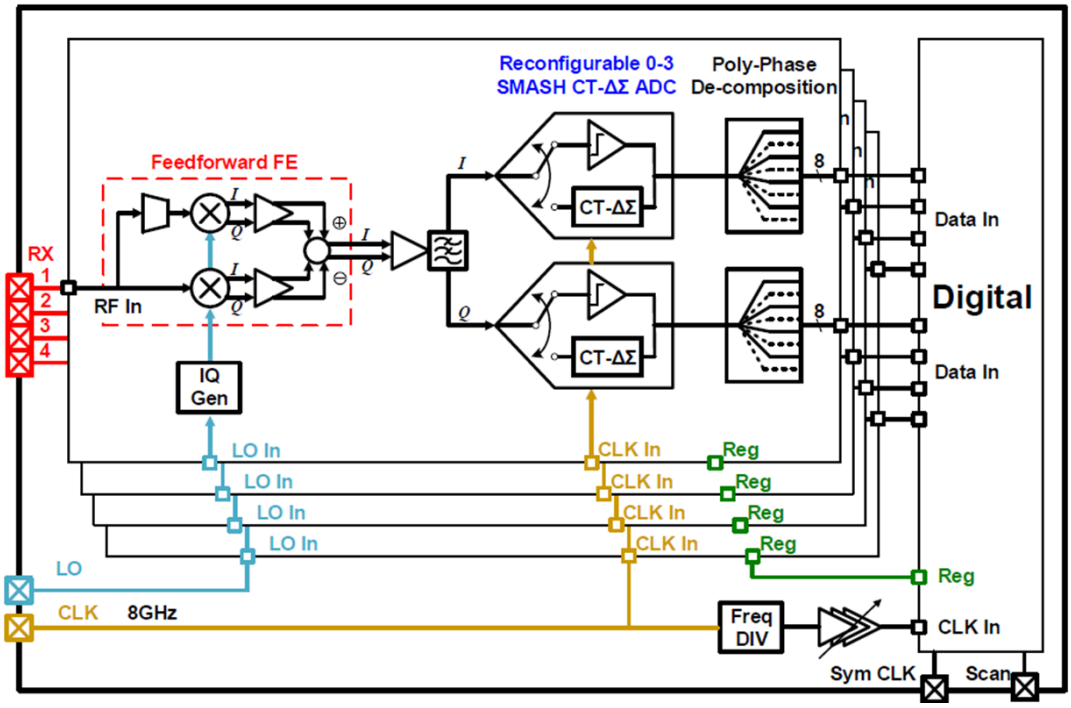


Figure 3.1. The proposed 2x2 phased array beamformer with the digital backend [18].

The overall system will consist of a 2x2 receiver array with each containing a feedforward, mixer first front end, 2 reconfigurable CT-DSM for I & Q signals, a custom digital polyphase decimation filter, and a digital backend for beamforming. A separate ADC test structure is also included for individual testing. The main purpose of this ADC is to allow for two modes, one for beamforming and another for beam searching a target receiver. Some additional research goals are to:

1. Use an oversampling 1-bit quantizer during both ADC modes
2. Allow for a configurable DSM loop during beamforming mode

The entire ADC system will consist of a 0-3 CT SMASH DSM along with a polyphase decimation filter. A breakdown of the target specification for this ADC will be given along with the architectural design of the entire ADC.

3.1 TARGET SPECIFICATION

Since this system is being designed for a mm-Wave digital phased-array system, the signal bandwidth is very wide, but the SNDR required for 16-QAM modulation is not very high. The minimum SNDR required for 16-QAM is around 15-17 dB for a bit error rate (BER) of ~10^{-4} with only a single carrier [19]. However, other aspects like the peak-to-average-power-ratio (PAPR) or accounting for margin will increase the required SNDR by quite a bit. The equation for the exact SNDR requirements is given below,

$$SNDR_{req} = SNR_{min} + PAPR + Margin + Noise\ Backoff \tag{3.1}$$

The PAPR, margin, and quantization noise backoff will vary between designs and specifications. For this ADC design, the breakdown of the required SNDR is given in the figure below.

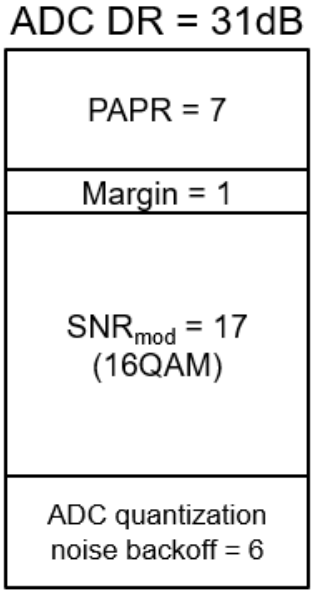


Figure 3.2. A breakdown of the required performance of the ADC in the receiver chain

The total required SNDR is calculated to be about 31 dB for the entire ADC with a 1 dB margin, a 6 dB noise backoff, and a PAPR of 7 dB. From the required SNDR, an initial architecture can be considered. Eq. 2.10 was used to generate a table with different DSM orders and varying OSR. A 3rd order DSM with an OSR of 8 was chosen as the SNDR would give around 32 dB which satisfies the required SNDR for this ADC alone.

Table 3.1. Maximum SNR of higher order DSM with varying OSR and loop order

		OSR (2^n)				
		2^1	2^2	2^3	2^4	2^5
Loop Order	1	-3.09	5.94	14.97	24	33.03
	2	-6.43	8.62	23.67	38.72	53.77
	3	-9.77	11.3	**32.37**	53.44	74.51
	4	-13.11	13.98	41.07	68.16	95.25
	5	-16.45	16.66	49.77	82.88	115.99

The subsequent list summarizes the main requirements that the ADC needs to meet:

- Signal Bandwidth: 2 GHz
- Sampling Frequency: 16 GHz
- OSR: 8
- Minimum SNDR: ~31 dB
- Decimation Rate: 8

3.2 SMASH SYSTEM

The ADC architecture chosen is a 0-3 SMASH with an FF loop in the 2nd stage and 1-bit comparators in both stages with inspiration taken from [20]. Like previously mentioned, the goal of this ADC is to allow for two reconfigurable modes and an oversampled 1-bit comparator.

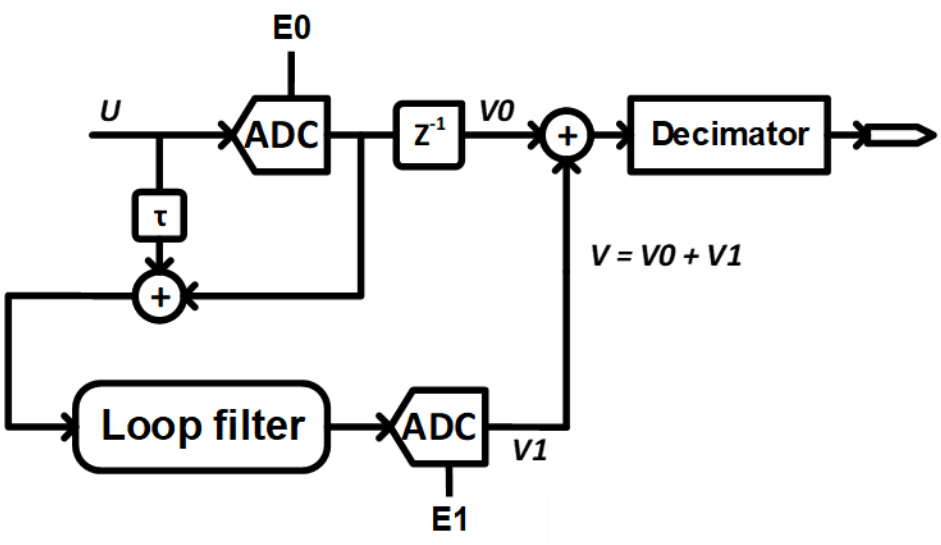


Figure 3.3. Proposed SMASH architecture for the reconfigurable ADC.

The first stage of the SMASH consists of a "0" path which is only a 1-bit quantizer in the signal path. The quantization error of the 1st stage will then be fed into the 2nd stage where a 3rd order DSM with an FF loop will quantize the error before the paths will be summed together through a full adder. The main purpose of the DSM in the 2nd path is to perform robust noise and harmonic cancellation for the 1-bit comparator, effectively enhancing the SNDR through noise shaping. The transfer function for each stage is given as:

$$V0 = U + E_0 \tag{3.2}$$

$$V1 = -E_0 \cdot STF + E_1 \cdot NTF \tag{3.3}$$

where STF and NTF are the transfer functions of the DSM in the 2nd stage. Since the loop filter is going to be an FF implementation, the FF paths control both the pole and zero locations in the filter and therefore the generalization of $STF = 1 - NTF$ can be made. Summing both stages together and substituting $STF = 1 - NTF$ into the equation yields the final transfer function below.

$$V = V0 + V1 = U + NTF \cdot (E_0 + E_1) \tag{3.4}$$

From the equation, the quantization noise of both stages will be shaped through the DSM of the 2nd stage while the signal integrity will be mostly determined through the 1-bit comparator which will have unity gain. However, this system has a 3dB SQNR penalty as the summation of incoherent quantization noise from both stages will increase the IBN.

A Ƶ-domain initial transfer function was synthesized in MATLAB using Richard Scheier's Delta-Sigma toolbox for the frequency response of the loop filter in the DSM [9]. Since the OSR of this DSM is low, the filter response was made to be a 3rd order Chebyshev response to minimize the IBN across a wide signal bandwidth.

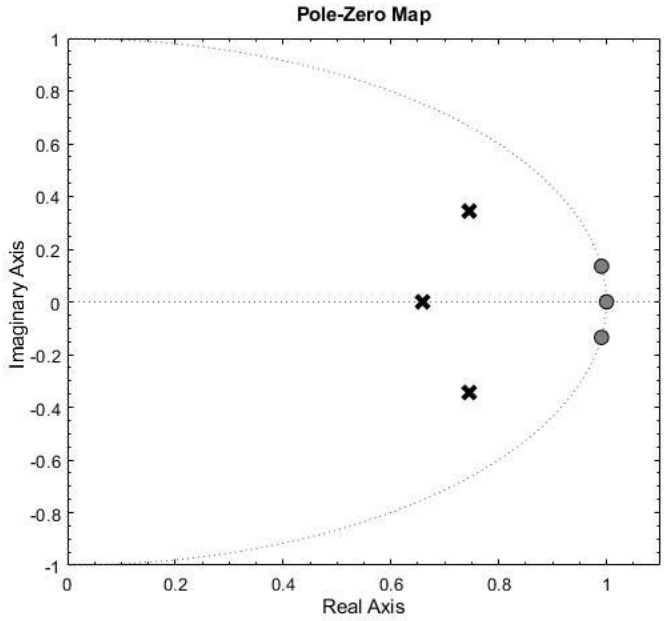


Figure 3.4. Location of the pole-zeros in the Ƶ-domain unit circle.

The zeros of the system are all on the unit circle, indicating that they are all located at DC, and the overall response will be a high-pass filter response with a null given by the angle of the complex zero pairs. Despite the complex response of the function, the real-part location of the pole-zero pairs is unchanged from a normal high-pass filter.

$$NTF_{MATLAB} = \frac{s(s^2 - 0.16s + .09)}{(s + 0.43)(s^2 - 0.43s + .18)} \tag{3.5}$$

Since the DSM is continuous time, the ℤ-domain transfer function needs to be converted into an s-domain transfer function instead.

There are many methods to do this discrete-continuous conversion, but the two popular ways are the bilinear transformation (BT) and the impulse-invariant (II) method. The BT method is computationally simple, substituting $z = e^{sT} \approx \frac{1+s(T/2)}{1-s(T/2)}$ into the discrete transfer function to convert it into its continuous-time version, with T being the sampling period. However, the substitution is only an approximation between discrete-continuous time functions and the resulting transfer function will contain frequency warping since the BT attempts to map a continuous s-plane into a finite unit circle in the ℤ-domain. The effects of frequency warping can affect the system response for low OSR DSM and must be factored in during the conversion [21]. Luckily, MATLAB already has built-in options to allow for the compensation of frequency warping for the BT method when designing a low-OSR DSM, but frequency warping is an effect that must be considered when doing so.

The II method has been traditionally the more popular method over the years due to good matching between discrete- and continuous-time transfer functions [21]. However, the method is computationally intense. The higher loop filter order for the DSM the more complex each substitution becomes. A table from [11] is given below that shows up to the 4th-order conversion between ℤ and S domains. β and α are arbitrary lengths for the feedback DAC and f_s is the sampling frequency.

$\mathcal{Z}$-domain	$\mathcal{S}$-domain equivalents with f_S (Hz) $= 1/T_S$
$\frac{1}{(z-1)}$	$\frac{w_0}{s}, \quad w_0 = \frac{f_S}{\beta - \alpha}$
$\frac{1}{(z-1)^2}$	$\frac{w_1 s + w_0}{s^2}, \quad w_0 = \frac{f_S^2}{\beta - \alpha}, \quad w_1 = \frac{1}{2}\frac{f_S(\alpha + \beta - 2)}{\beta - \alpha}$
$\frac{1}{(z-1)^3}$	$\frac{w_2 s^2 + w_1 s + w_0}{s^3}, \quad w_0 = \frac{f_S^3}{\beta - \alpha}, \quad w_1 = \frac{1}{2}\frac{f_S^2(\alpha + \beta - 3)}{\beta - \alpha},$ $w_2 = \frac{1}{12}\frac{f_S[\beta(\beta-9) + \alpha(\alpha-9) + 4\alpha\beta + 12]}{\beta - \alpha}$
$\frac{1}{(z-1)^4}$	$\frac{w_3 s^3 + w_2 s^2 + w_1 s + w_0}{s^4}, \quad w_0 = \frac{f_S^4}{\beta - \alpha}, \quad w_1 = \frac{f_S^3}{2}\frac{\beta + \alpha - 4}{\beta - \alpha},$ $w_2 = \frac{f_S^2}{12}\frac{(\beta - \alpha)^2 + 2\beta\alpha - 12(\beta + \alpha) + 22}{\beta - \alpha},$ $w_3 = \frac{f_S}{12}\frac{\beta^2(\alpha - 2) + \alpha^2(\beta - 2) - 8\alpha\beta + 11(\beta + \alpha) - 12}{\beta - \alpha}$

Figure 3.5. Z-domain to S-domain conversion through II method [11].

Such complex computation is difficult by hand, but MATLAB has several built-in functions that allow for such a complex conversion [22]. The BT with frequency pre-warping was used to convert Eq. 3.6 into an s-domain equivalent function that has similar frequency behavior in MATLAB.

$$NTF_{MATLAB} = \frac{s(s^2 - 0.16s + .09)}{(s + 0.43)(s^2 - 0.43s + .18)} \tag{3.7}$$

The equation above will be used to design the coefficients for the FF paths in the loop filter which will be explained later in the implementations section.

3.3 Polyphase Decimation Filter

A decimation filter is needed to down convert the bitstream from the ADC into a lower a frequency so the digital baseband can perform necessary computations for demodulation and beamforming. With an effective sampling rate of 16 GHz, the bitstream from the ADC is too fast even for custom digital circuits to handle. The decimation filter, therefore, was designed as a

polyphase decomposition filter that down sampled the data first, before being filtered and summed together.

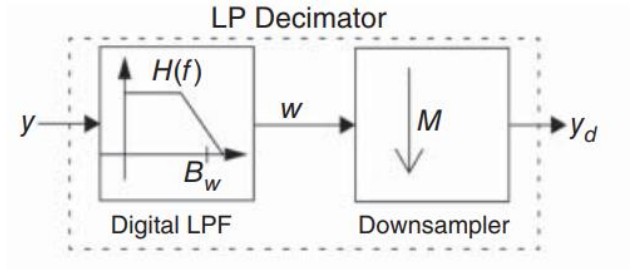


Figure 3.6. General decimation filter structure [23].

Polyphase decimation filters allow for the input to be down converted into a lower frequency first before the data is filtered through an FIR filter. Since down sampling happens first, the FIR filter only needs to be clocked at the down sampled rate which is more power efficient than traditional decimation filter designs where the filter is placed first in the signal path. The general decimation system is given in Figure 3.6. Mathematically, a normal decimator and a polyphase decimator are identical. The discrete-time Fourier Transform (DTFT) of a normal decimator is a modified sampling equation.

$$X_d\left(e^{j\omega}\right) = \frac{1}{M}\sum_{i\,=\,0}^{M-1} X\left(e^{j\left(\frac{\omega}{M}-\frac{2\pi i}{M}\right)}\right) \tag{3.8}$$

$$X_d(z) = \frac{1}{M}\sum_{i\,=\,0}^{M-1} X\left(z^{1/M} e^{-j2\pi k/M}\right) \tag{3.9}$$

Where M is the down sampled factor. The discrete time signal $X\left(e^{j\omega}\right)$ is effectively resampled at frequency M times lower than the sampling frequency, creating a convolution between an impulse train and the input signal with a resulting output sequence $X_d\left(e^{j\omega}\right)$. To prevent aliasing, a digital filter is usually included in front of the down sampler to prevent the edges of the aliased signals from superimposing on each other.

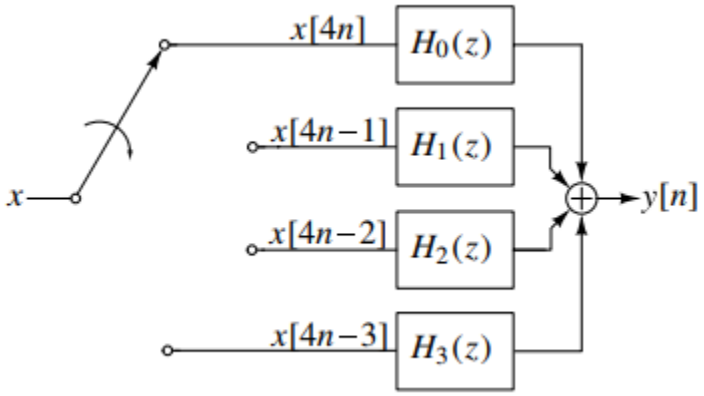


Figure 3.7. General structure of a polyphase implementation of a decimation filter [9].

A polyphase implementation of the decimation filter entails moving the down sampler in front of the filter instead. In addition, the digital filter is now broken down or "decomposed" into its polyphase components for each path, but the overall filter response will be equivalent to the original filter after the summation.

$$H(z) = H_0(z^4) + z^{-1}H_1(z^4) + z^{-2}H_2(z^4) + z^{-3}H_3(z^4) \quad (3.10)$$

In this case where the signal is being down sampled by a factor of 4, each path will see only every 4th sample coming in from the input. Therefore, the impulse response of each polyphase filter when $n = 0$ are

$$h_0 = \{h[0], h[4], h[8] \dots\} \quad (3.11)$$

$$h_1 = \{h[1], h[5], h[9] \dots\} \quad (3.12)$$

$$h_2 = \{h[2], h[6], h[10] \dots\} \quad (3.13)$$

$$h_3 = \{h[4], h[7], h[11] \dots\} \quad (3.14)$$

$$h = h_0 + h_1 + h_2 + h_3 \quad (3.15)$$

indicating that the summation of individual polyphase filter will have the same filter response as the original filter [9] [23]. A polyphase decimation filter is particularly useful for high-frequency operation as the polyphase filters only need operate at the decimated clock rate instead of at the

sampling clock rate which greatly saves power and relaxes timing requirements in the digital components.

Chapter 4. CIRCUIT IMPLEMENTATION

The following section details the design of the individual circuit blocks for the ADC and the interface between the ADC and the digital backend. The ADC, as previously mentioned, is a CT 0-3 SMASH DSM architecture that consists of an 8x polyphase decimation filter that interfaces to the digital backend. The loop filter in the DSM stage is a 3rd order capacitive feedforward structure that uses the capacitor in the third integrator as the common summing node for the feedforward paths. A local resistive feedback path was also created with the 1st and 2nd integrator to implement the Chebyshev filter response. The integrators use a 2-stage feedforward amplifier with cross-coupled capacitors to maintain stability and a large unity gain bandwidth (UGB). The comparator is a 2x interleaved sample and hold (S/H) topology that doubles the effective sampling rate from the clock. The bitstream from the comparator is combined through a DAC driver before being fed through a normal 1-bit current DAC. The data from the ADC is then decimated through a 8x polyphase decimation filter with a custom digital decimator. The 2x2 digital phased-array system was designed and implemented in TSMC 28nm HPC.

4.1 CT 0-3 SMASH SYSTEM

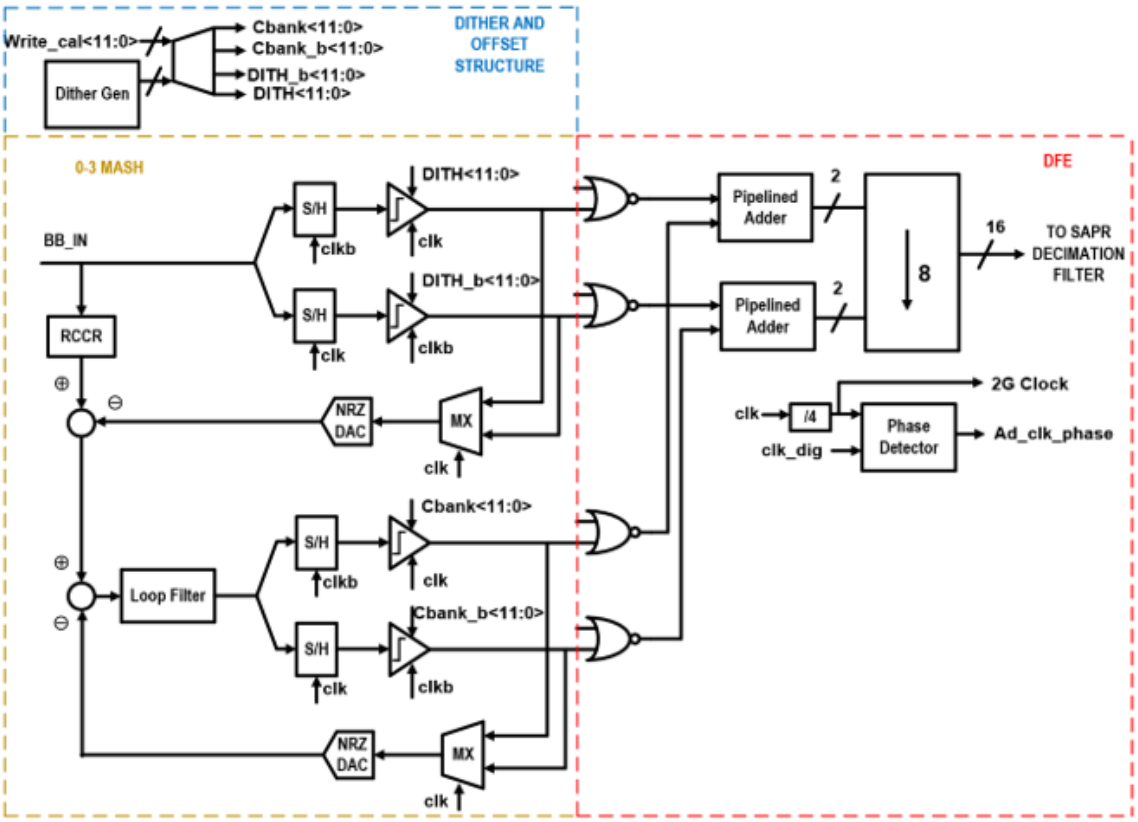


Figure 4.1. Detailed architecture of the ADC.

The overall ADC architecture is given above in Figure 4.1. The first path in the ADC consists only of a 1-bit comparator with a 1-bit current DAC, IDAC0. The second path is a 3rd order CT FF DSM stage that is used to quantize the quantization error in the first stage. In between the two paths is a passive first-order all-pass filter (APF) that is used to match the delay of the open-loop comparator and IDAC0 as well as to provides a real part resistance for the first integrator.

$$H(j\omega) = \frac{1 - j\omega\tau}{1 + j\omega\tau} \tag{4.1}$$

The APF's transfer function is given in Eq. 4.1 where τ is the time constant of the filter. The maximum group delay of the filter can be calculated by taking the negative derivative of Eq. 4.2 with respect to ω and setting that result to zero [24]. The result, Eq. 4.3, indicates that the maximum

delay is when $\tau = {}^{1}/_{\omega}$ and the APF can be designed to accommodate roughly 1.5 clock periods of delay.

$$\tau(j\omega)_{max} = \frac{1}{\omega} = \frac{1}{2\pi f} \tag{4.4}$$

If the delays are matched correctly, then the quantization error from the 1-bit comparator can be extracted through the current subtraction between the APF and IDAC0 that takes place before the first integrator.

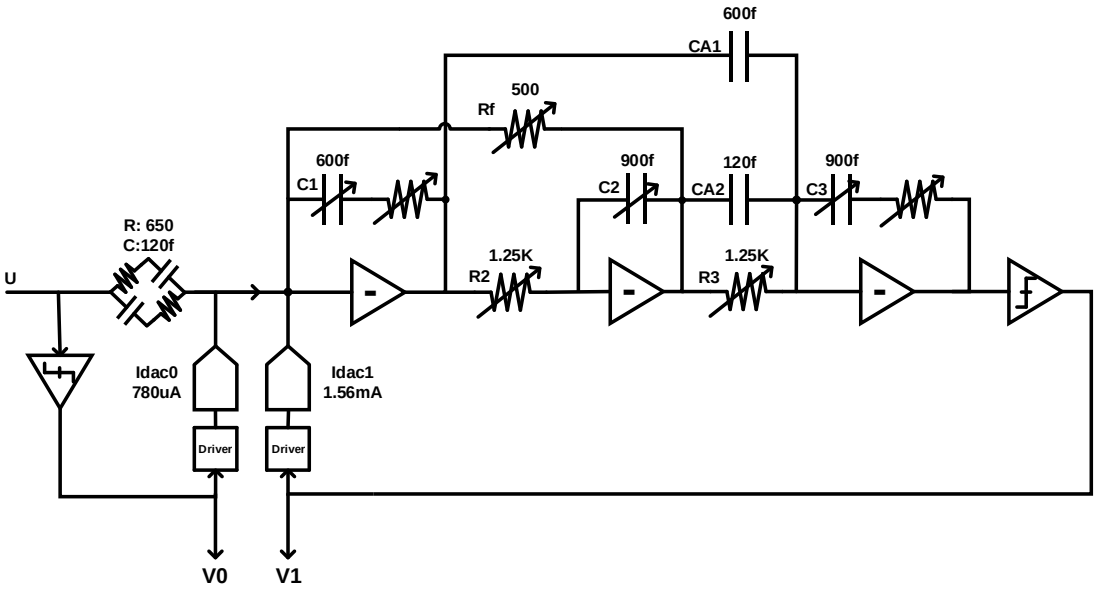


Figure 4.2. The architecture of the reconfigurable 0-3 SMASH ADC.

The 2nd stage in the ADC is a 3rd order CT FF DSM that uses capacitive FF paths in the loop filter. The loop filter in the DSM contains three integrators, in which the first two integrators have a local feedback path through the Rf resistor to form a resonator. The FF paths in this loop filter are provided by the two capacitors CA1 and CA2 and uses C3 as a common summing node.

$$STF(s) = \frac{\frac{Gm_0}{s^3 C_1 R_2 C_2 R_3 C_3} + \frac{Gm_0 C_{A2}}{s^2 C_1 R_2 C_2 C_3} + \frac{Gm_0 C_{A1}}{s C_1 C_3}}{\frac{Gm_1}{s^3 C_1 R_2 C_2 R_3 C_3} + \frac{Gm_0 C_{A2}}{s^2 C_1 R_2 C_2 C_3} + \frac{Gm_0 C_{A1}}{s C_1 C_3} + 1} \tag{4.5}$$

$$NTF(s) = \frac{1}{\frac{Gm_1}{s^3 C_1 R_2 C_2 R_3 C_3} + \frac{Gm_0 C_{A2}}{s^2 C_1 R_2 C_2 C_3} + \frac{Gm_0 C_{A1}}{s C_1 C_3} + 1} \quad (4.6)$$

The transfer functions for the DSM are given in both Eq. 4.7 and Eq. 4.8 where Gm_0 and Gm_1 are the large-signal transconductance of the current DACs from the 1st and 2nd stage, respectively. The resonator loop through Rf is not included in the analysis as the resonator only makes the pole-zero pairs complex and typically will not move the real-part location of the poles. The gain of the feedforward paths is given by a ratio between the feedforward caps and C3, and the ratios can be found by equating the NTFs in Eq. 4.4 and Eq. 3.6. The initial capacitor ratios are given below:

$$\frac{C_{A1}}{C_3} = 0.67 \quad (4.9)$$

$$\frac{C_{A2}}{C_3} = 0.18 \quad (4.10)$$

However, these ratios will change when excess loop delay and intermediate node scaling are considered, and the values of the feedforward capacitors needs to be swept around the initial values in the final design.

For excess loop delay (ELD) compensation, the proportional-integration (PI) method given in [25] was used. Resistors are added in series with C1 and C3 to form an effective short for the input signal through C1, CA1, and C3 to the quantizer. This method is the easiest to implement while requiring a moderate increase in the unity gain bandwidth (UGB) of the amplifiers [25]. Other methods require additional DACs or supporting digital circuitry which is not feasible for such a high clock frequency, nor power efficient.

The feedback DACs, IDAC0 and IDAC1, are both connected to the same current summing node before the first integrator. IDAC1 was made to have up to twice as much current as IDAC0 to properly scale the input of the DSM stage by half. This current ratio effectively changes the DC

gain of the STF in the DSM to ½ and needs to be compensated for the system to properly perform correct noise cancelation and shaping given by Eq. 4.11. The compensation is done through the pipelined full adder that combines the output of both stages. The output of the DSM is shorted into two of the inputs of the full adder, effectively achieving a digital gain of 2, and establishes unity gain across the entire signal bandwidth through the DSM 2nd stage.

4.2 FEEDFORWARD AMPLIFIER

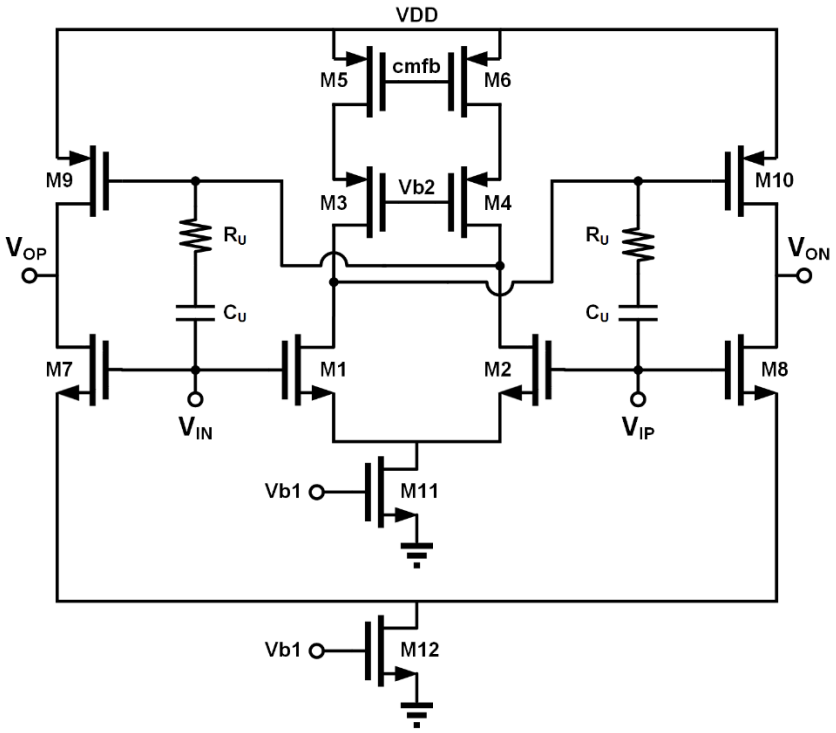


Figure 4.3. Topology of the 2-stage feedforward amplifier.

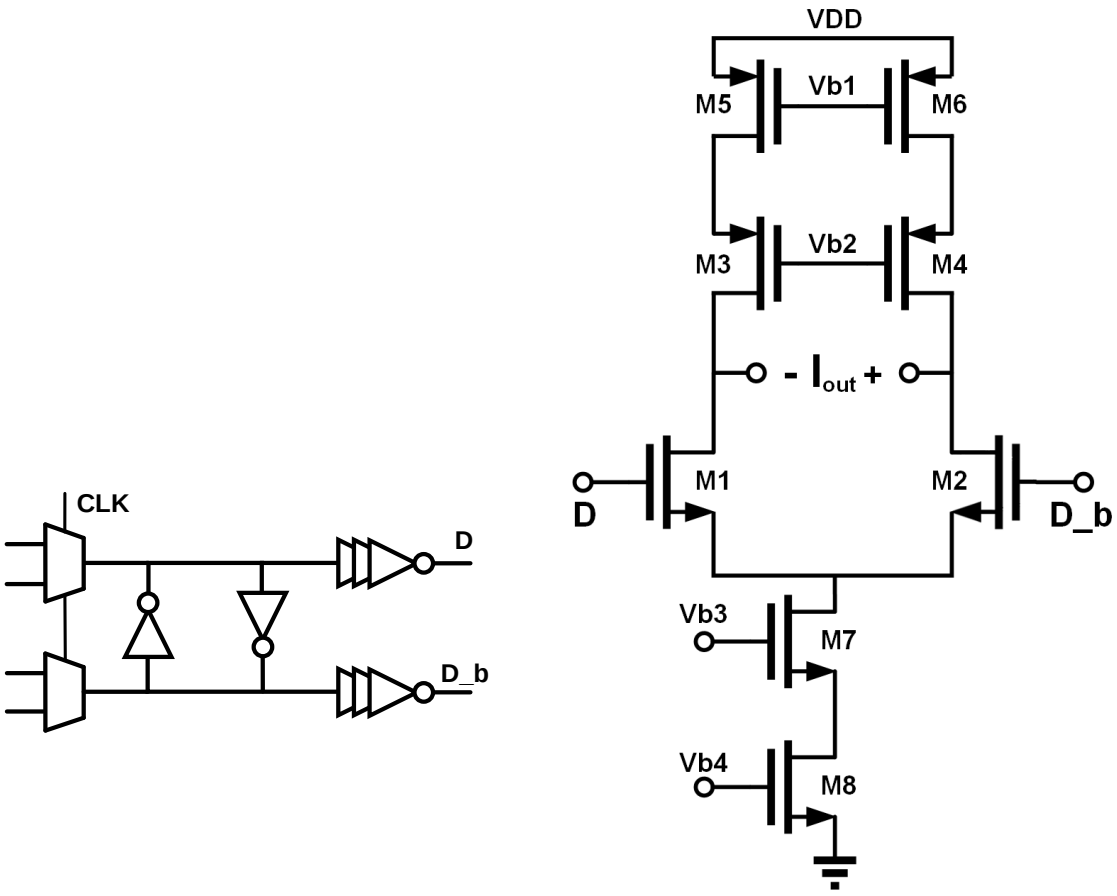
A second-order feedforward amplifier was used in the three integrators in the DSM. Feedforward amplifiers are popular in CT-DSM loop filters due to their ability to achieve high gain at higher frequencies compared to typical miller-compensated multi-stage amplifiers [26]. Also, the fact that feedforward amplifiers have bad settling times is irrelevant in a CT-DSM [9] [11]. The additional zero introduced through the feedforward path increases the UGB of the amplifier at the cost of increasing settling times. In a CT-DSM, however, the entire output

waveform is relevant unlike in a DT-DSM where the individual samples need to settle within a clock period. As such, feedforward amplifiers remain the more popular amplifier topology used in CT-DSM.

To maintain stability, the dominant pole needs to come from the first order path in the amplifier [20]. However, given the high frequency of operation that can only be achieved by burning more current. A better solution is to use cross-coupled capacitors to offset the dominant pole created between the two stages [27]. The cross-coupled capacitors create another pole-zero doublet pair which nulls the loading capacitance that the 1^{st} stage sees into the 2^{nd} stage. To lower the amount of capacitance needed, resisters were added in series.

This amplifier was designed using ultra-low voltage threshold (ULVT) RF devices and uses 2mA total, including the common-mode feedback circuitry, with a 0.95V power supply. With the addition of the cross-coupled capacitors, the lowest phase margin was 65 degrees. This amplifier managed to achieve 35dB of open loop gain and 55 GHz of UGB, which is sufficient to prevent degradation of the NTF.

4.3 CURRENT DAC



(a) (b)

Figure 4.4. Topology of the DAC (a) the DAC driver (b) current DAC cell

The current DAC used for both the 1st and 2nd stage in the ADC is just a typical current DAC topology. The top and bottom current sources were implemented as ULVT mac devices while the input switches use normal VT devices to allow for faster switching. Since the entire phased-array system is integrated into one power supply domain of 0.95V, the input switches were biased into triode, but were still able to maintain decent performance with a 16 GHz switching frequency.

The DAC driver is a simple cross-coupled inverter with buffers at the output. A 2-to-1 mux is used to drive the inverter latch and convert the interleaved bitstream from the comparator back into a 1-bit bitstream. Single-bit DACs are inherently linear so a 1-bit bitstream is desired to

maintain that linearity as any mismatch between multiple DAC elements will increase the noise floor at the input of the ADC. The only drawback of this topology is the top current sources are directly connected to the output which will inject drain noise into the input of the ADC. However, since the ADC only uses an interleaved 1-bit comparator, the quantization noise will be the most dominant factor for this ADC.

4.4 COMPARATOR W/ DITHERING SCHEME

The comparator implemented in this ADC is divided into a track and hold (T/H) and a 2-stage comparator. Due to the high effective sampling rate, the decision was made to interleave 2 comparators together. Interleaving 2 comparators halves the required clock rate from 16 GHz to 8GHz and does not require any phase shift circuitry as the comparators will operate on opposite clock edges.

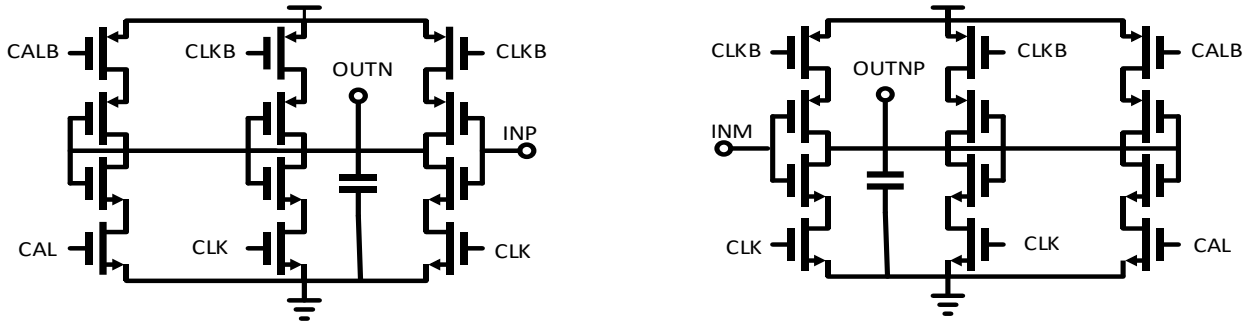
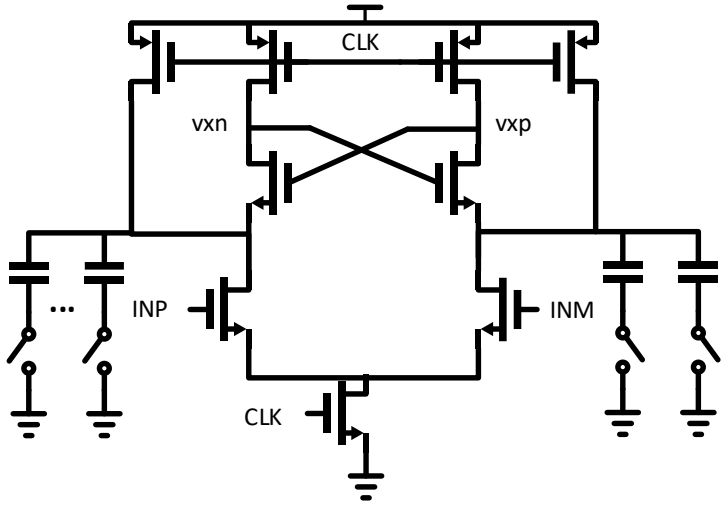


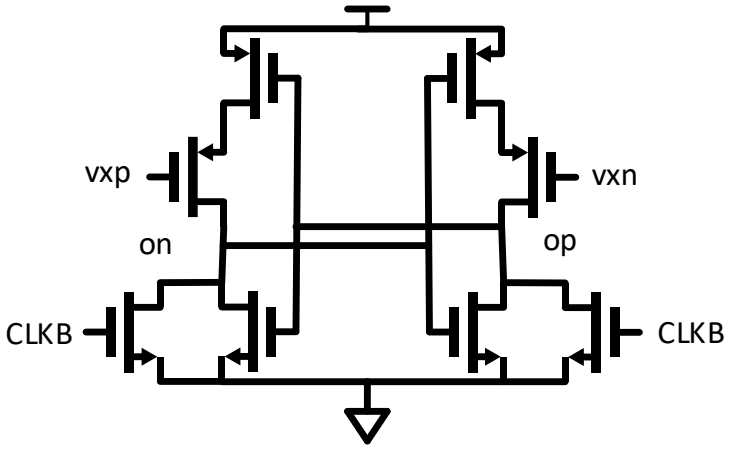
Figure 4.5. Topology of the Track-and-Hold in the comparator

The topology for the T/H is a self-biased inverter-based load given above and was taken from [28]. The DC gain of this T/H is dependent on the ratio of the transconductance of the driver stage and the impedance of the load. An additional 10.5 fF metal-on-metal (MOM) capacitor was added to decrease the switching noise of the T/H. A replica branch was also implemented to allow for the T/H to provide a similar bias and load for the comparator when doing DC offset calibration.

The T/H achieves a -3 dB DC gain with a bandwidth of 17.7 GHz. An IIP3 of 11.26 dBm was achieved along with a power consumption of 2.16mW with a nominal supply of 0.95V.



(a)



(b)

Figure 4.6. Topology of the comparator (a) the first stage (b) the second stage.

The topology of the comparator is a mesh of ideas taken from [29], [30], and [31]. The entire comparator takes half a clock cycle for amplification and the other half for latching. When the clock is high, the cross-coupled pair in the first stage amplifies the input voltages through regeneration. The output of the first stage, *vxn* and *vxp*, are then fed to a PMOS switch in the second stage where the input is latched when the clock is low. Inverters and an SR latch are used

to buffer the output of the second stage. Binary-weighted moscaps were attached to the input of the comparator to tune the DC offset as well to implement a dither path. The overall comparator achieves a decision time of 51ps while only taking 15.7ps to reset. The power consumption is 2.18mW at nominal supply of 0.95V.

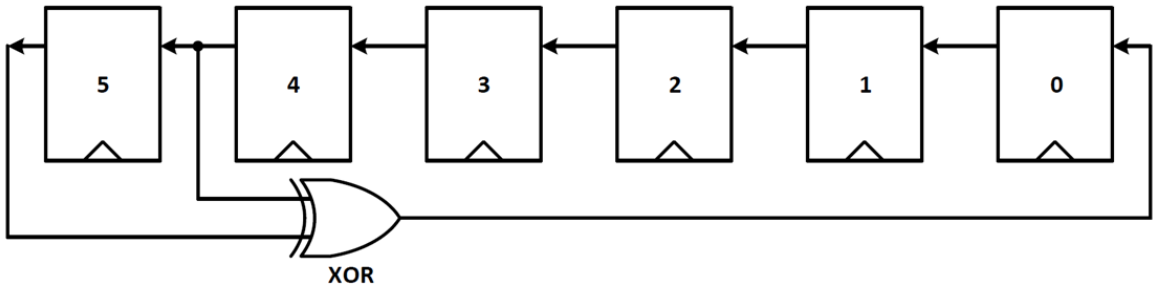


Figure 4.7. A pseudo random dither topology.

As previously mentioned, dithering was implemented in the comparators through the DC offset capacitors. When the summation occurs in the digital beamformer, the noise between the different elements needs to be decorrelated to take advantage of the array gain. The array gain occurs when uncorrelated noise and the correlated signal are summed together in the digital backend, resulting in a 3dB increase in the SNR every time the number of elements is doubled. For this reason, a pseudo random dithering sequence was created using 6 LFSRs all seeded differently between the different ADCs in the phased-array system. Doing so would decorrelate the noise between the different ADCs and array elements so that the array gain can be taken advantage of. The dithering circuitry is only needed when running the open-loop path for the 1-bit comparator since natural dithering occurs when running the entire ADC with the DSM stage.

4.5 DECIMATION FILTER

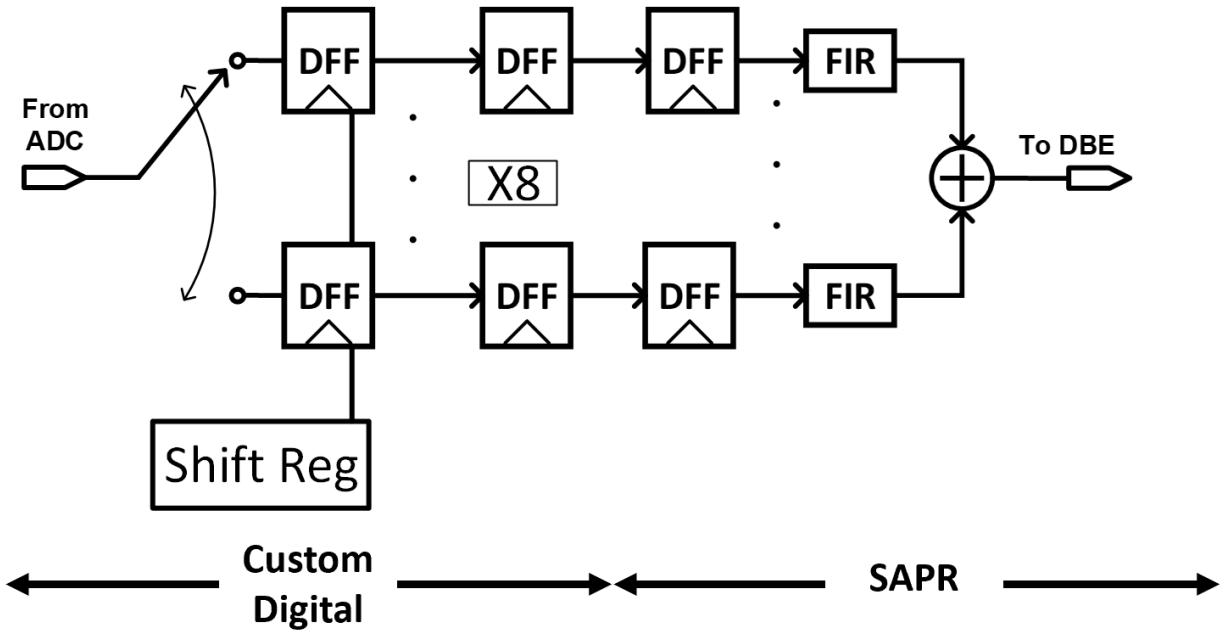


Figure 4.8. Topology of the polyphase decimation filter.

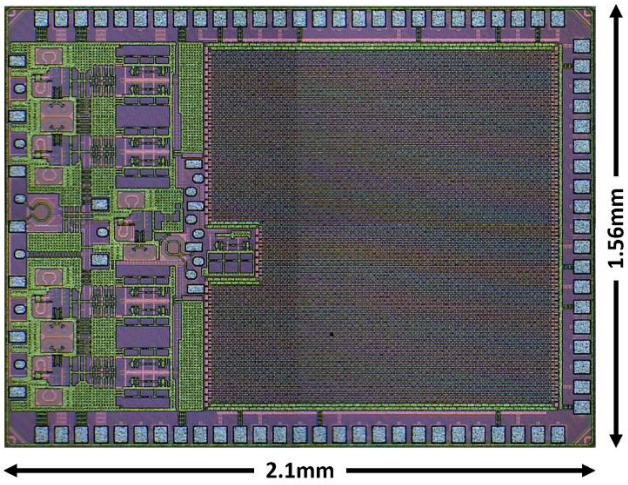
The decimation filter is implemented as an 8x polyphase decimation filter. Figure 4.8 shows custom-designed, round robin shift registers that clocks the first set of registers in the decimator, down sampling the ADC bitstream down to the Nyquist frequency of 2 GHz. Another set of custom DFFs are used to buffer the output of the decimator before the decimated bitstream goes into the synthesized DFFs and the polyphase FIR filters. The outputs of the FIR filters are summed together and sent into the digital backend for post processing.

Chapter 5. MEASUREMENTS

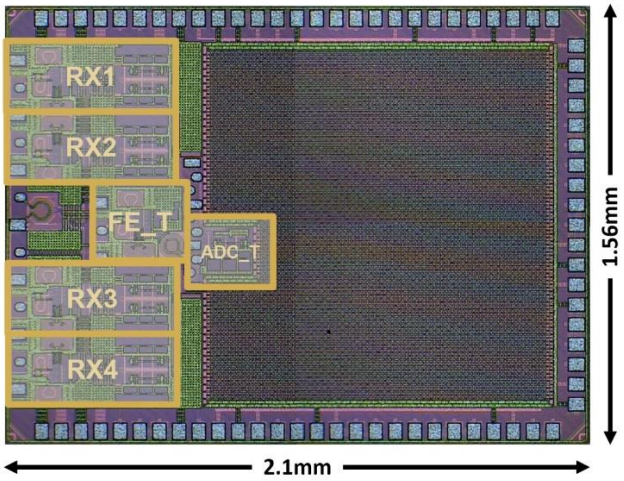
The ADC was taped out with the 2x2 V-band phased array receiver mentioned earlier, and the chip was fabricated in TSMC 28nm CMOS HPC+ technology. An individual test structure of the ADC was included onto the chip so that the performance can be characterized independently from the rest of the system.

5.1 MEASUREMENT PLAN

The input pads of the ADC test structure were wire bonded and connected to SMA connectors onto a custom designed daughter board, and the output of the ADC is stored in a 1024 address memory bank on-chip. The daughter board is attached to another custom designed motherboard through a 128-pin connector, and a raspberry pi is connected to the motherboard to move and manipulate the data on the chip.



(a)



(b)

Figure 5.1. (a) Picture of the 2x2 phased array chip (b) location of the receiver elements and test structure

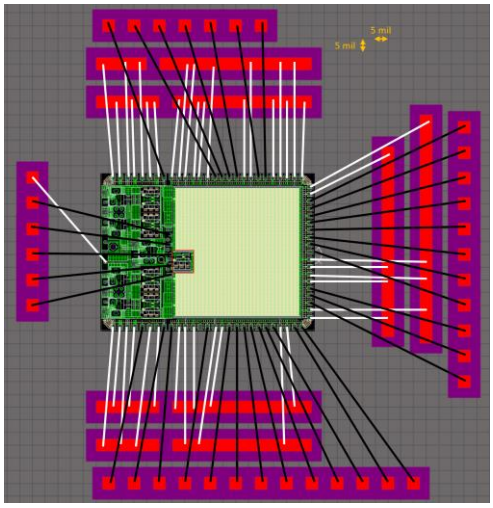


Figure 5.2. Layout of the bonding diagram from the chip to the board.

Figure 5.1b shows where the ADC test structure is in the physical chip itself and the bonding diagram of the chip is also given in Figure 5.2. With the ADC test structure, the goal is to characterize the maximum SNDR, dynamic range, signal bandwidth, and frequency response. The test structure only needs a differential signal, a clock signal, and a current bias as inputs, and requires 4 different power supply domains for the analog blocks, custom-digital blocks, synthesized digital, and the digital input pads to control the different settings on chip.

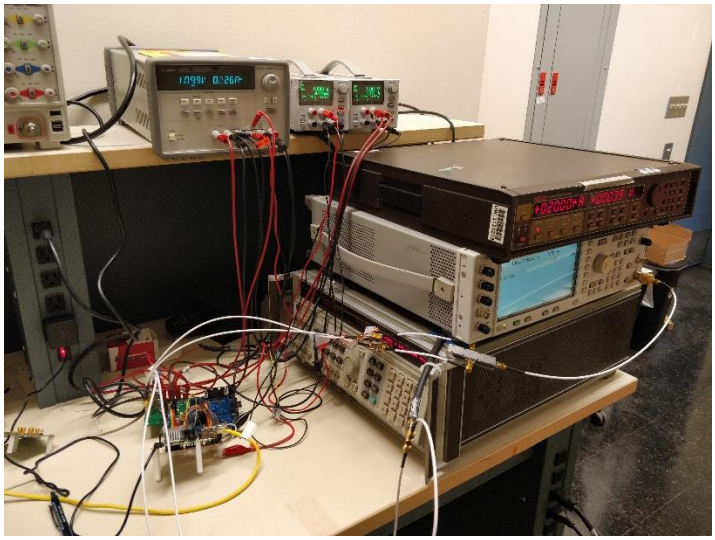


Figure 5.3. Picture of the test setup with all the equipment and board

5.2 Experimental Results

The experimental results of the ADC were taken using a 1.2V supply for the analog blocks and the die photo is previously given above in Figure 5.1a. The clock frequency was halved from 8 GHz to 4 GHz as the noise shaping was not stable, but the new clock frequency would still give an 8 GS/s bit stream with the interleaved comparators.

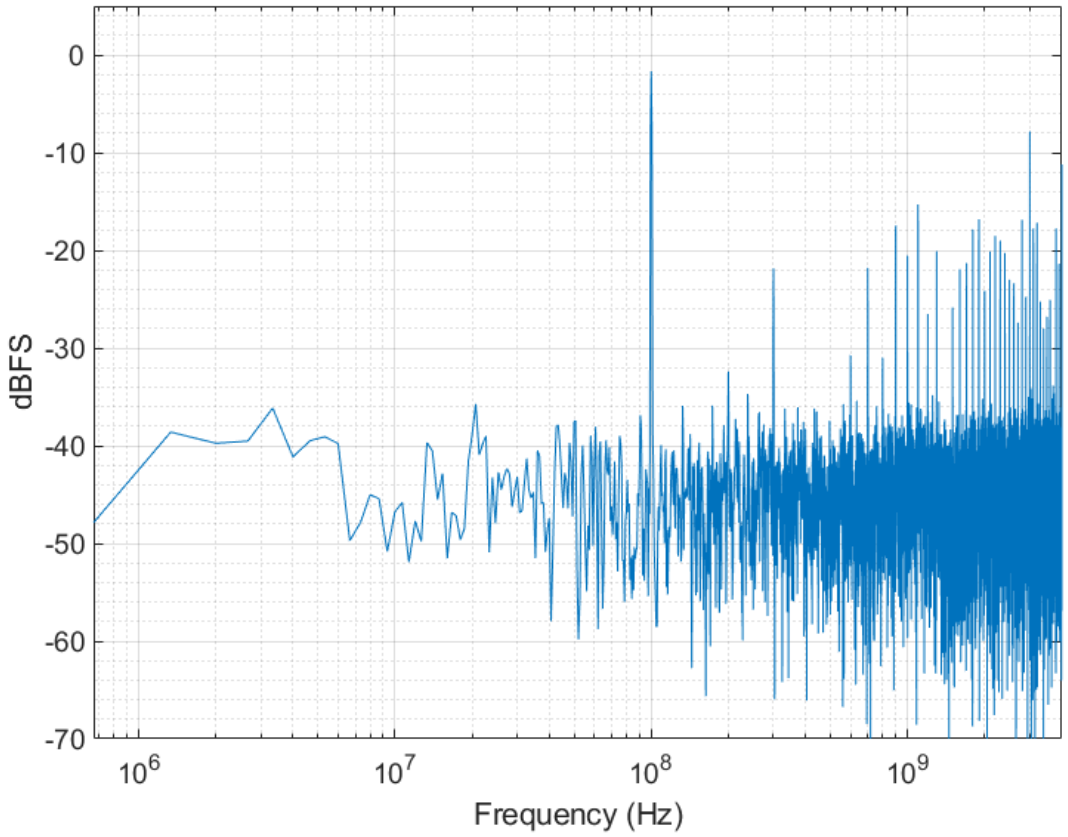


Figure 5.4. Frequency response of the open loop 1-bit comparator with a 100 MHz tone at -1.6 dBFS

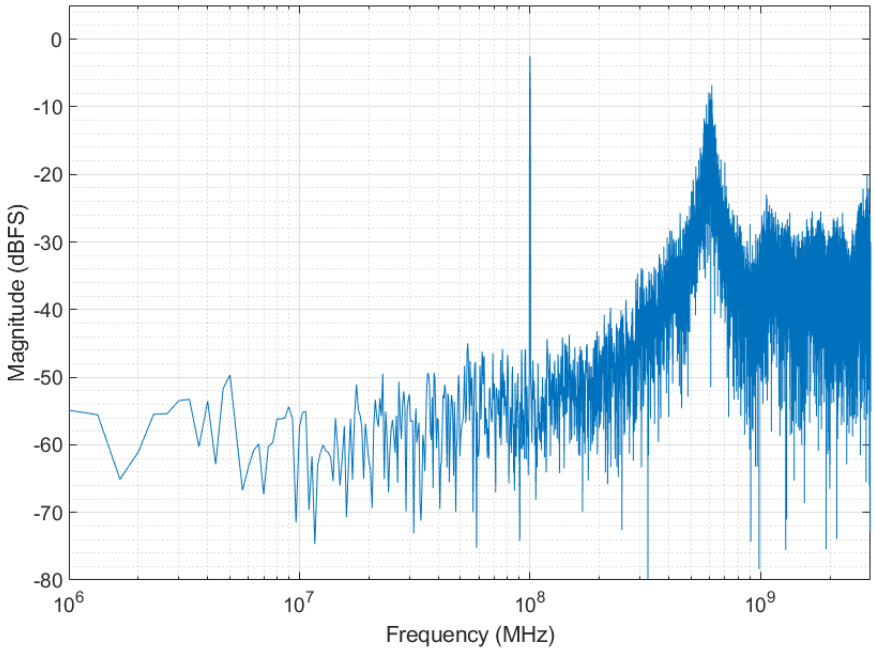


Figure 5.5. Frequency response of the DSM with a 100 MHz input tone at -2.1 dBFS

The performance of the single-bit comparator suffered heavily due to the odd order harmonics as seen in Figure 5.4 and was limited to only 16 dB of SNDR. A single tone with an input power of -2.1 dBFS and at 100 MHz was sent into the DSM stage of the ADC and the resulting spectrum can be seen in Figure 5.5. A peak SNDR of 24.7 dB was achieved with the DSM after decimating and filtering the result in Figure 5.5. Repeating SNDR measurements were taken using both the on-chip decimation filter and an ideal MATLAB filter. Both filters were configured with a passband and stopband of 200 MHz and 300 MHz respectively and used 48 quantized taps in the frequency response. Figure 5.6 shows that the ideal and on-chip filter both behave closely to each other.

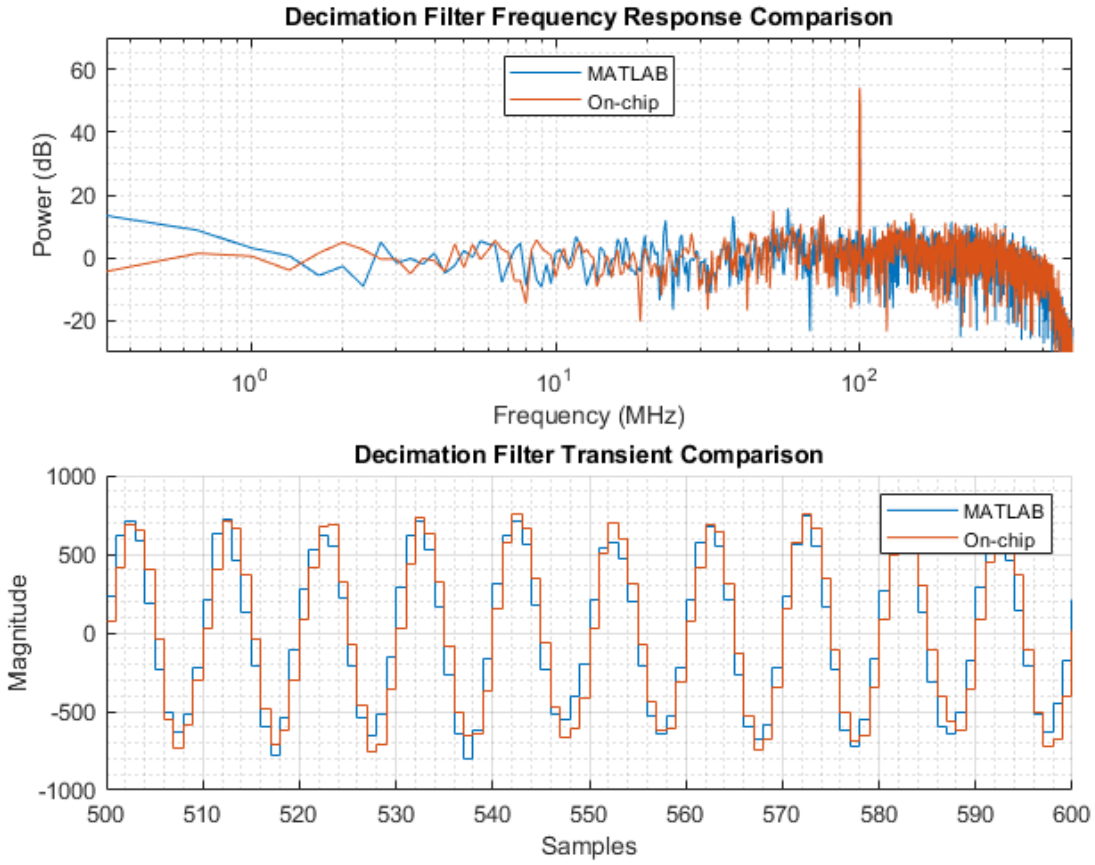


Figure 5.6. Frequency response of the MATLAB and on-chip decimation filter along with the transient response.

The dynamic range (DR) of the DSM came out to be around 27 dB as seen in Figure 5.7 with both the on-chip and MATLAB filters. The total power that the ADC burns is hard to determine due to the individual test structure nestled inside beamformer itself which results in a much higher current consumption than expected. The simulated power consumption came out to be a total of 35 mW with a breakdown of the power consumption in Figure 5.8.

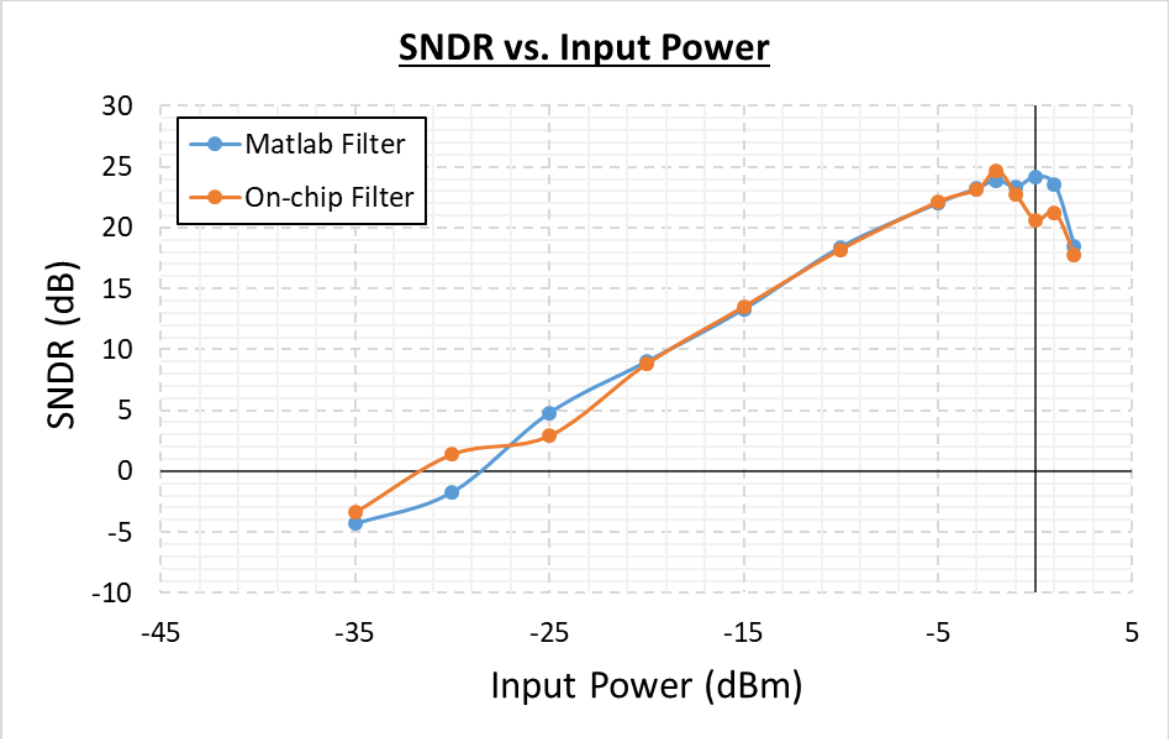


Figure 5.7. Measured SNDR vs 100 MHz input tone w/ the DSM stage.

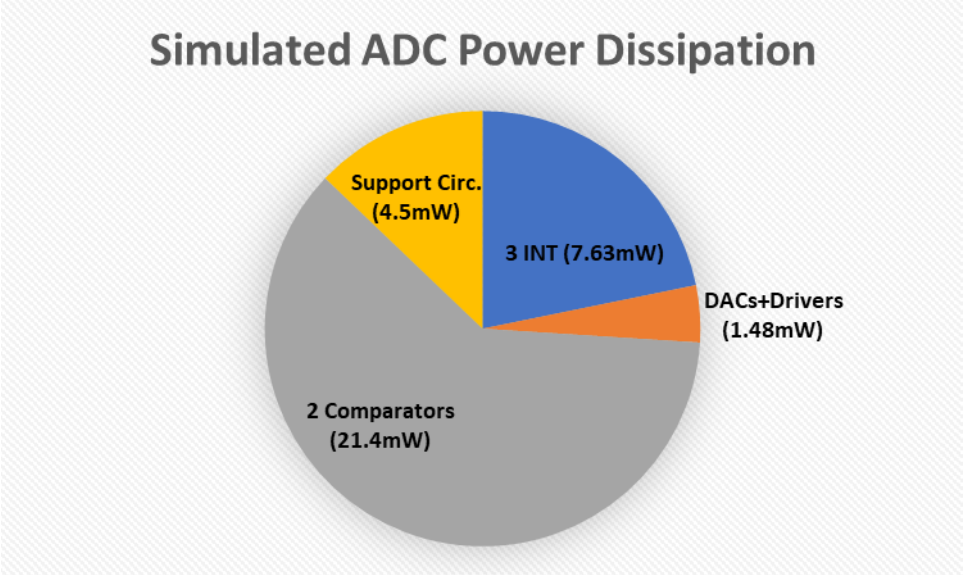


Figure 5.8. Simulated ADC power dissipation.

Chapter 6. CONCLUSION

This work introduced the design of a high-speed low-resolution ADC for V-band digital phased array systems. The ADC was implemented in TSMC 28nm CMOS HPC+ and integrated into a 2x2 digital phased array system. Measurement results show that the DSM stage can achieve an SNDR of 24.7 dB with a DR range of about 27 dB, capable of quantizing basic modulation schemes. The goal of this work is to prove that low-resolution ADCs are viable alternative for low power V-band systems while capable of achieving decent performance.

However, the measurements in the lab were limited by the multiple impairments found on the chip. Specifically, the full MASH system suffered an additional 3 dB SQNR penalty compared to running just the DSM stage by itself. The additional penalty can be seen in Eq. 3.4 where two uncorrelated noise sources E_0 and E_1 are summed together before being noise shaped. With an already low-resolution quantizer and low OSR, the additional SQNR penalty from the MASH system limits the beamformer's ability to quantize higher order modulated schemes.

Another crucial design error is the peaking effect shown in noise shaping that can be seen in Figure 5.5 which comes from comparator metastability [9] [11] [12]. Generally, the feedback loop has a half-sample delay that comes the DAC taking in the inverse clock signal that the comparator uses. The half-sample delay allows the comparator to latch correctly so that the DAC only sees a binary output from the comparator. In this case, the DAC and comparator use the same clock signal which results in the DAC seeing a signal from the comparator that is briefly metastable.

In addition, the coefficients for the taps in the decimation filter were also designed to be signed integers only. This oversight limited the stopband roll-off in the frequency response and resulted in a less than ideal filtering for the high frequency noise shaping.

In future iterations of the ADC, the overall system needs to be redesigned with the above-mentioned errors fixed to allow for an ADC that can achieve the goals outlined at the beginning of Chapter 3. A comparison table below shows the results of this ADC compared to other state of the art works on ADC designs.

Table 6.1. Comparison Table with State-of-the-Art ADC publications

	[20]	[32]	[33]	**This work**
Technology	**28nm**	**28nm**	**65nm**	**28nm**
Architecture	**CT 0-3 S/MASH**	**CT 3-1 SMASH**	**CT 4th BP**	**CT 0-3 S/MASH**
Sampling Rate	**3.2 GHz**	**1.8 GHz**	**800 MHz**	**8 GHz**
Comparator	**4-bit FLASH 2.5-bit FLASH**	**4-bit FLASH 2.5-bit FLASH**	**3-bit FLASH**	**1-bit in both paths**
Sig. BW	**45 MHz**	**50 MHz**	**24 MHz**	**100MHz**
DR [dB]	**90**	**85**	**60**	**27**
SNR [dB]	**84.6**	**76.8**	**-**	**-**
SNDR [dB]	**72.6**	**74.9**	**58**	**25**
Supply Voltage	**0.9V/2.8V**	**1.3V/1.5V**	**1.25V**	**1.2V**
Power [mW]	**235**	**80.4**	**12**	**35**

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