Multilevel Resistive Switching in a Metal Oxide Semiconductor based on MoO_3

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Abstract

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Over the years a resistive random-access memory (ReRAM) has received great attention due to its simple structure, CMOS compatible fabrication process, low-power consumption. Among other attracting memory characteristics, multilevel switching is considered as a very important feature since a single memory cell can store more than one bit of information, thereby increasing memory density. While molybdenum trioxide (MoO_3) has been widely used for many optoelectronic devices as a charge transport layer, it has not been extensively investigated as a resistive switching layer.

In this research, I have used MoO_3 as a switching layer and demonstrated a multilevel resistive switching by controlling the compliance current. In a novel lateral device architecture, I have also demonstrated a self-compliance resistive switching behavior. However, devices need to be further optimized to reduce the operating voltage in a lateral device architecture.

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I would also like to extend thanks to Dr Tadesse Ghirmai, and Dr Harry Aintablian from the research committee for accepting my invitation.

DEDICATION

I would like to dedicate this research to both my parents. All of this became possible with their vision and dedication that I was able to come this far in my educational career. Their love and support throughout all these years kept me persistent in achieving my goal.

Chapter 1

Introduction

1.1 Brief history of memory technologies

For years, the capacitive-based memory technology had been toe-to-toe with the ever-emerging market, fulfilling all the desired aspects of the ambitious and the exponentially increasing interests of its consumers [1]. The memory technology is divided into a non-volatile and volatile: a non-volatile memory promotes the retention of the previously stored contents even after the removal of the power supply while a volatile memory requires refreshment every few milliseconds to hold the contents resulting in a higher energy consumption [2-5].

Among all the existing memory technologies Dynamic RAM (DRAM), Static RAM (SRAM) and Flash memory had been playing the vital role and met diverse requirements of many different applications. Each memory technology comes with its competitive advantages and disadvantages. For example, a DRAM can achieve a very high density, but it requires the dynamic refreshing causing the data to be refreshed periodically, otherwise it cannot hold data stored in a capacitor over long period of time due to the capacitive leakage as shown in Figure 1.1(a) [6]. In a DRAM, data is recognized as 1's and 0's determined from the amount of charge stored in the capacitor, e.g., fully charged ("1") and fully depleted ("0") [7]. Conversely, a SRAM does not use the capacitor in its memory cell structure which makes it free from charge leakage issues as the DRAM, hence it does not require a periodic refreshment, resulting in a high-speed data read and write capabilities but it is a volatile memory like a DRAM memory [2, 3, 6, 8-11]. Figure 1.1(b, c) [6] illustrates the 6-transistor and 4-transistor layout configurations of SRAM's memory cell structure. The typical SRAM memory cell structure comprises of four MOSFET transistors and two pull down resistors, referred to as 4-transistor SRAM memory cell, which exhibits two stable

memory states such as logic “0” and “1” [12]. The pull-down resistors in the cell structure adds the drawback of high-power dissipation due to the constant current flow through either of the resistor which also results in the circuit design issues and limiting higher integration [13] comparatively, the 6-transistor memory cell configuration has the advantages of the reduced power dissipation and low static power due to no pull-down resistors being used in its circuitry [14]. Although, the 4-transistor memory cell structure results in the disadvantage of the high-power consumption but it has the advantage of the density which comes at the toll of manufacturing complexity [13, 15].

Flash memory is the potential competition to both DRAM and SRAM and has the advantage of non-volatile characteristic, but it has some disadvantages such as low operating speed, limited endurance, and higher writing voltage [16, 17]. Flash memory is classified into two memory configurations based on how its memory cells are organized: NOR and NAND [18]. Figure 1.1(d) [6] shows the NOR configuration of the flash memory that reads and writes the data into the memory cells individually because of the parallel arrangement of the memory cells respective to the bit lines, which also adds the capability to randomly access each memory address at any given time and has a faster read operation than NAND. Alternatively, in the NAND configuration all the memory cells are arranged in series to the bit lines as shown in Figure 1.1(e) [6] which means that it has a higher density than the NOR architecture, that is also the reason why the NAND flash memories have higher data storage capacity, smaller in size and cheaper than their counterpart NOR [3].

The cross-sectional view of the flash memory in Figure 1.1(f) illustrates the physics behind the non-volatile memory storage.

In order to allow the conduction between the drain and source, a positive voltage (V_G) is applied to the gate that will attract electrons as a charge carrier, creating a channel between the drain and source [19].

If the V_G is further increased, then the electrons forming the channel between the drain and source can tunnel through the oxide and then trapped at the floating gate where oxide layer is the insulating layer that normally blocks the transport of electrons, and the floating gate is the isolated gate between the select gate and the drain-source channel. This trapped charge is responsible for shifting the threshold voltage which is a minimum voltage needed to create a conducting path between the drain and source. The floating gate holding the trapped electrons needs a higher threshold voltage, representing the Logic 0. If there are no electrons trapped in the floating gate, then a lower threshold voltage is required, representing the logic 1. Therefore, by detecting the threshold voltage we can determine if the transistor has any electrons trapped at the floating gate or not. Since the floating gate is electrically isolated, the trapped electrons have nowhere to go and can stay there for a very long time of around 10 years or so thus, making a non-volatile memory storage [1-6, 8, 9, 20].

Figure 1.1. Memory cell structures of existing memory devices (a) DRAM with 1 transistor & 1 capacitor configuration (b) SRAM with 6 transistor configuration (c) SRAM with 4 transistor configuration (d) NOR type Flash memory cell configuration (e) NAND type Flash memory cell configuration and (f) Cross-sectional view of the Flash memory cell structure.

Each memory technology has their respective advantages and disadvantages based on their circuit designs, the comparison among each memory technology is shown in Table 1.1.

Table 1.1. illustrates the summarized comparison among DRAM, SRAM and Flash memory [21]

Feature	DRAM	SRAM	Flash
Read Speed	Medium	Fastest	Fast
Write Speed	Medium	Fastest	Low
Future Scalability	Limited	Good	Limited
Cell Density	High	Low	Medium
Non-Volatile	No	No	Yes
Endurance	Infinite	Infinite	Limited
Cell Leakage	High	Low/High	Low
Operating Voltage	Limited	Low	Limited
Complexity	Medium	Low	Medium
Memory Cell Construction	Built using one transistor and one capacitor.	Built in CMOS technology, only transistors and no capacitor.	Built in CMOS technology, uses transistors only and a floating gate component that leverages the non-volatile memory operation in the memory cell.

The existing memory technologies impose great challenges in terms of miniaturization and power consumption [22]. For example, a capacitor in the DRAMs, multiple transistors in SRAM, and a floating gate of flesh memory add significant manufacturing complexity when they are scaled down to 10 nm or beyond [23]. This is attributed to the loss of stored charge at nanoscale, which results in the degradation of the performance, reliability, and noise margin [5, 24]. Furthermore, complicated read and write operations require considerable power consumption, hindering advancement of mobile electronics [24, 25]. Therefore, next generation memory technology should guarantee a low-power consumption and a higher integration with a a simplified structure.

1.2 Next generation memory technologies

There are many new emerging memory technologies such as Magnetic RAM (MRAM), Ferroelectric RAM (FeRAM), phase-change RAM (PCM) [5]. MRAM stores data via magnetization process and is classified into two categories: Toggle Mode MRAM and Spin-Tunnel Torque (STT) MRAM. Figure 1.2(a) [26] shows the memory cell structure of a Toggle Mode MRAM technology. It is based upon the magnetic tunnel junction structure (MTJ) consisting of two ferromagnetic layers separated by a thin insulating layer that acts as a tunnel barrier [27].

Figure 1.2(b) shows the memory cell structure of a STT MRAM which is also based on one transistor and one MTJ. In both types of MRAM technologies, data is represented as the resistance state of a MTJ which can be switched between high resistance state and low resistance state upon changing the direction of magnetism of the two ferromagnetic layers in MTJ [26-28]. One of the ferromagnetic layers in MTJ is a reference layer that has a fixed magnetic direction (magnetic moment) while the other is a free layer with two possible magnetic moments. MRAM technology uses the magnetism of the electron spin to perform the non-volatile memory operation. The electron spin direction is used to switch the magnetic moment of the free layer either in the same direction as the reference layer (parallel magnetic polarization) or in a different direction than the reference layer (antiparallel magnetic polarization) to switch the resistance state of the MTJ between low resistance state and high resistance state, representing the bit log 0 and 1 respectively [29, 30].

The main difference between the two MRAM memory technologies is in terms of their memory operation i.e., Toggle MRAM uses the magnetic field that changes the electron spin which in effect changes the magnetic moment of the free layer in MTJ for programming/writing bits

while STT MRAM uses the spin polarized current (reversed direction currents) to change the spin of electrons which alters the magnetic moment of the free layer in MTJ [31-33].

Figure 1.2(c) [34] shows the basic FeRAM memory cell structure consisting of ferroelectric capacitor and a MOS transistor [35]. The FeRAM has a capacitor containing ferroelectric material as a dielectric medium that can change its polarization state respective to the direction of the applied electric field. The ferroelectric material typically has a crystalline structure having an atom at the center. This atom has two low energy states and the position of an atom between these two states determines the polarization state of the ferroelectric material. Data is stored in a polarization state and Figure 1.2(d) [34] illustrates two different polarization states of the ferroelectric capacitor: polarized-up or polarized-down. These states is controlled by applying electric field in different directions. Upon removing the electric field, the atom still remains at the same polarization state, exhibiting a non-volatile memory characteristic [35, 36].

Figure 1.2(e) [33] illustrates the cross-sectional view of the PCM memory cell structure. PCM consists of the phase change material that can be either in a crystalline or amorphous state at room temperature. The material has a lower resistance when in a crystalline state and high resistance when in an amorphous state [37, 38].

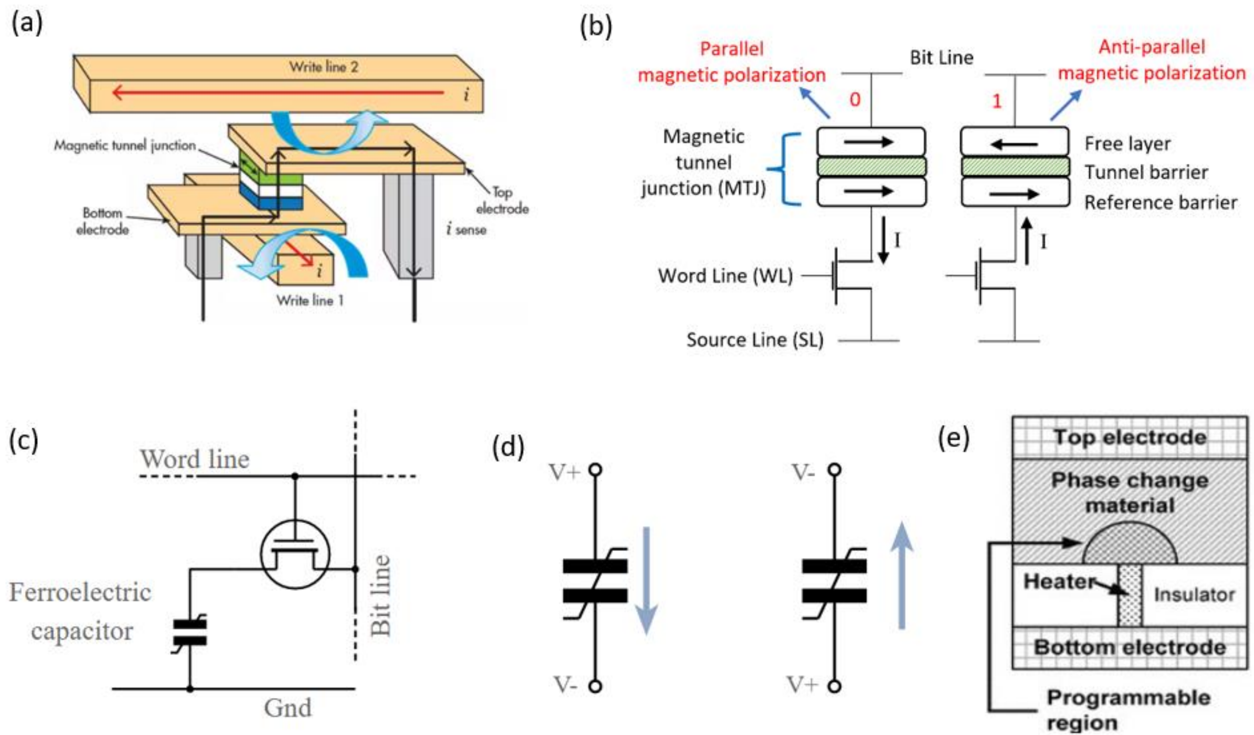

Figure 1.2. Memory cell structures of the new memory technologies (a) Toggle-MRAM memory (b) STT- MRAM memory showing the read/write operation (c) FeRAM memory (d) Ferroelectric capacitors polarization based on the applied electric field polarity, contributing to the read and write operations in the FeRAM memory cell (e) PCM memory.

1.3 Motivations

Among those emerging memory technologies, a Resistive Random Access Memory (ReRAM) has received great interest in the recent years due to its promising potential for the development of the non-volatile memory devices with fast switching, longer retention time, high storage density, and low power consumption [39-45]. In addition, ReRAM devices are relatively easy to be implemented as a multilevel switching memory where more than 1 bit of digital information can be saved in one single memory cell. Thanks to the simple read/write process, power consumption can be very low. Another advantage of ReRAM technology is that many dielectric and metal oxide materials are available as a switching layer [39-42, 46-50].

Molybdenum Oxide (MoO_3) has been very widely used as a hole transport layer for optoelectronics, but its potential as a resistive switching layer has not been explored much. In this research, I have investigated the potential of MoO_3 as a multilevel resistive switching layer and explored a novel device architecture which can be used as a sensing element.

Chapter 2

Basics of Resistive Switching Devices

In this chapter I will discuss the fundamentals of the ReRAM devices, including a typical device structure that shows a simple Metal-Insulator-Metal (MIM) configuration and the fabrication techniques involved specific to the devices prepared for this study. In addition, I will also discuss the basic terminologies associated with device characterizations.

2.1 Device fabrication

There are various fabrication methods for the ReRAM device, but the effective ones are considered to provide the lower probability against device-to-device and cell-to-cell variability which are the responsible factors towards the device performance variations, degradation, and the credibility of the acquired results [51]. Devices that realize the significant device-to-device and cell-to-cell variations never leads to the conclusive results of the ReRAM performance and resistive switching behavior.

With the choice of a fabrication technique, the electrical and mechanical properties of each layer in the stack structure can be altered, thus providing the controllability and optimization of the device switching behavior and performance [51-53].

The widely used fabrication processes for the ReRAM are the sputter deposition and thermal evaporation which are the common methods of the physical vapor deposition (PVD) [54]. As shown in Figure 2.1 [55], the sputter deposition setup consists of the vacuum chamber enclosing the closely placed parallel-plates (Cathode and Anode) plasma reactor. The process involves the bombarding of the high energy ions towards the cathode, ejecting the to be-deposited material from the target on to the wafer, placed at the anode/substrate. In a simple sputtering process, the

chamber is supplied with an inert gas usually argon which maintains the vacuum pressure around 0.1-1 torr. Sputtering is preferably used to deposit wide range of materials including metals and dielectrics [56, 57].

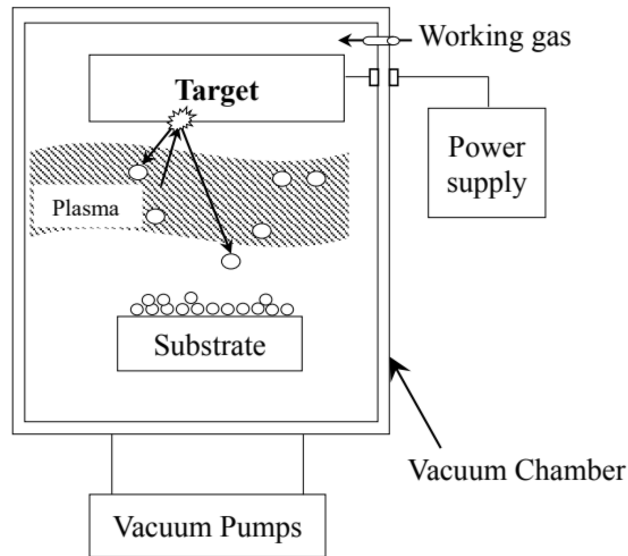

Figure 2.1. Simple parallel plate sputtering system having the target placed at the cathode and the substrate at the anode.

Similarly, thermal evaporation is also used for the deposition of the materials, but mostly metals. The material is heated to a certain temperature in a high vacuum where it is vaporized and deposited on the substrate. Figure 2.2 shows a typical the thermal evaporator chamber where the substrate/samples are located at the top of the chamber to the rotating chuck, facing downwards to the source material for coating [58, 59].

Figure 2.2. Thermal evaporator having the device samples facing downwards to the heated source material which is located at the bottom of the chamber facing upwards. photo from the clean room.

2.2 Basic device structure and resistive switching

A ReRAM has gained a great attention in the past few years among many different memory technologies due to its very simple structure where a resistive switching layer (SL) is sandwiched between two electrodes, i.e., top electrode (TE) and bottom electrode (BE) [1, 2] as shown in Figure 2.3(a). This allows ReRAM technology to be a promising candidate for a low cost and high throughput manufacturing technology [3, 60]. In a resistive memory device, data is stored in different resistive states and these states remains unchanged for a very long period of time, making ReRAM as a non-volatile memory device. For example, a ReRAM typically shows two distinctive resistive states i.e., Low Resistive State (LRS) and High Resistive State (HRS), representing data bits 1's and 0's, respectively. Each state is the result of the formation and rupture of a conductive path between the top electrode and bottom electrode based upon the application of voltage biasing at the top electrode while the bottom electrode is kept grounded [50, 61, 62].

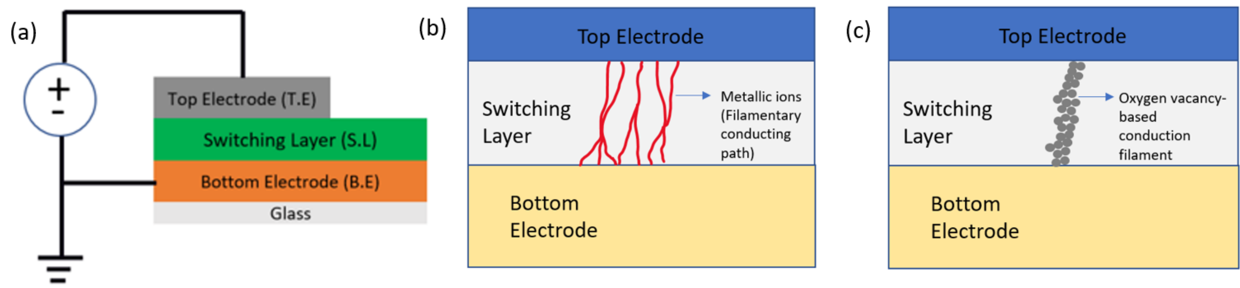

Figure 2.3. Conventional ReRAM device (a) Vertically stacked metal-Insulator-metal structure of a ReRAM device (b) Cross-sectional view of the ReRAM showing metallic filament-based conduction path between the top and bottom electrodes and (c) Cross-sectional view of the ReRAM showing oxygen vacancy-based conduction path between the top and bottom electrodes.

The dynamics and type of the formation and rupture of the conduction path between the top and bottom electrodes is determined by the switching mechanism. There are various switching mechanisms to form the conduction path in a ReRAM device, but two commonly observed models are the filamentary conducting path model and an interface-type conducting path model also referred to as oxygen-vacancy model [3]. Figure 2.3(b) illustrates the filamentary-switching model that postulates the resistive switching as a result of the formation and rupture of a metallic conductive filament in the ReRAM device known as conductive bridge RAM (CBRAM) which is also often referred to as the electrochemical metallization memory (ECM). In an oxygen-vacancy based model, resistive switching happens due to the movement of charged oxygen vacancies or oxidation/reduction of metallic elements in the ReRAM device called as OxReRAM also sometimes referred to as valence change memory (VCM) [3, 39, 62-66] as shown in Figure 2.3(c).

A ReRAM has two major switching behaviors: unipolar and bipolar switching modes. As shown in Figure 2.4(a) [65], in a unipolar switching mode, set and reset processes occur at the same voltage polarities and the magnitude of the applied voltage determines those processes. For example, a positive reset voltage (V_{reset}) takes the device from the LRS to the HRS, and a little bit

higher positive voltage (V_{set}) brings the device back to the LRS. The similar switching can take place in the negative voltage bias for a unipolar switching device [2, 3, 67-69]. In a bipolar switching mode as shown in Figure 2.4(b) [65], the resistive switching is dependent on the voltage polarity. For example, a negative bias (V_{reset}) is required for the reset process, which takes the device from the LRS into the HRS, and a positive bias (V_{set}) is required for the set process, which takes the device from the HRS into the LRS or vice versa [70].

The resistances values of each state (HRS & LRS) in either switching mode are obtained by applying a small voltage, also known as a reading voltage (V_{read}), without triggering set/reset process. Both unipolar and bipolar switching modes possess advantages and disadvantages. The unipolar switching has an advantage of providing a large distinction between resistance values in HRS and LRS states and only require a single polarity to exhibit the resistive switching, making the implementation of the read/write circuitry simple. However, it typically has a low endurance and inadequate read margin between resistance states compared to the bipolar resistive switching [2, 3, 71, 72]. A read margin often referred to as OFF/ON ratio which is the ratio of HRS to LRS.

A compliance current (I_{CC}) as noticed in the Figure 2.4(a)-(b) plays a critical role during the resistive switching operation and limits the maximum current that can conduct through the resistive switching layer. To prevent a permanent device failure due to a potentially high current during the set process, a compliance current is set in the measurement instrument to limit the amount of current during the set process [66, 73-75]. It was also reported that a slight changes to the compliance current can have a prominent impact on LRS and set/reset voltages during the resistive switching [66].

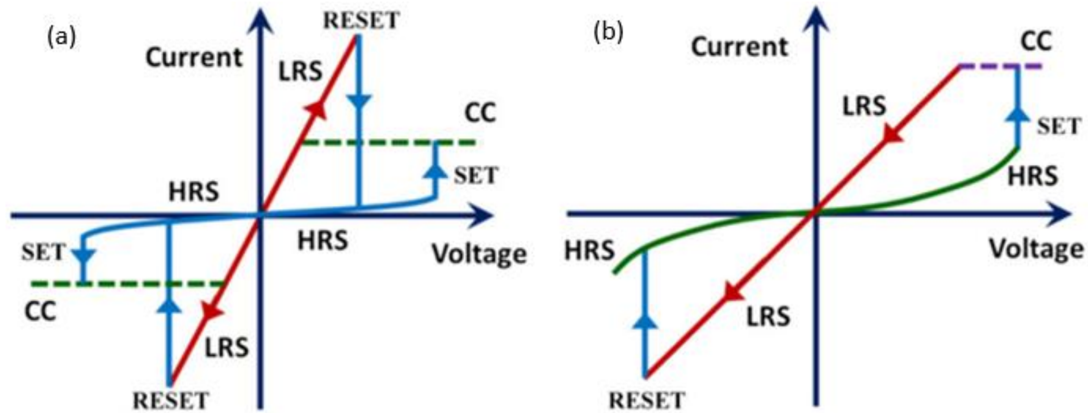

Figure 2.4. Current-Voltage (I-V) characteristic curve of a typical ReRAM device. (a) unipolar resistive switching and (b) bipolar resistive switching [5]. A compliance current is set to limit the amount of current during the set process, thereby preventing the memory device from a permanent failure due to the high current.

ReRAM devices can overcome the limit of miniaturization of current memory technologies thanks to their simple structure and operating principles. Three layouts have been widely used to implement high density ReRAM devices: (i) cross-point structure, (ii) crossbar structure, and (iii) a common bottom electrode structure [51, 76, 77]. (i) A cross-point structure is formed by sandwiching a resistive switching layer with two electrode arrays which are connected into the large contact pads as shown in Figure 2.5(a) [51]. This layout is particularly useful in a small-scale research lab where new resistive switching layers are screened and characterized. The large contact pads leverage the use of the conventional probe station or spring-loaded contacts of PCB board. (ii) A crossbar architecture consists of multiple cross-point devices, arrayed on a compact area as shown in Figure 2.5(b) [51]. Although this layout suffers from leakage current, parasitic capacitance, and cross-resistance by the adjacent cells, it can offer a very high-density memory cells if the electrode width is limited to a few nanometers. Several ReRAM companies are based on the crossbar architecture. Earlier in 2020, Crossbar Inc., along with others, formed SCAiLE (Scalable AI for Learning at the Edge), an AI consortium dedicated to combining ReRAM with

advanced acceleration hardware and optimized neural networks to create power-saving AI platform [78]. (iii) A common bottom electrode is the most common architecture and as the name implies, it uses the conductive substrate as a common bottom electrode which is completely covered by a resistive switching layer. Top electrodes are patterned to create arrays of memory cells as shown in Figure 2.5(c) [51]. The characteristics of ReRAM devices also depend on geometry and fabrication techniques.

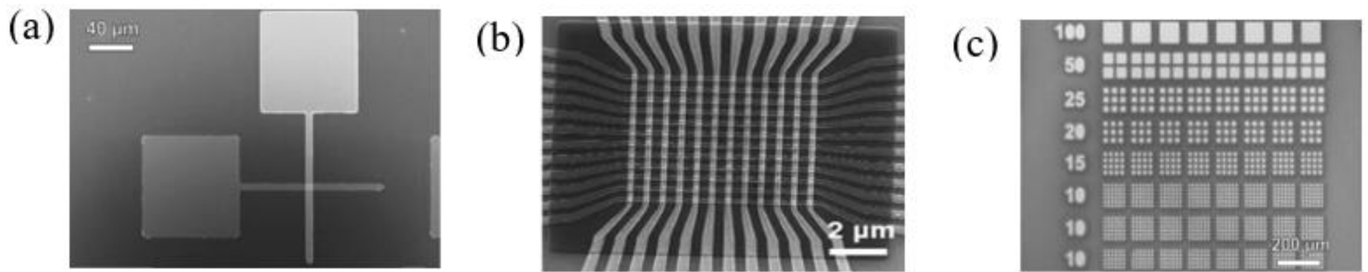

Figure 2.5. Common layouts of ReRAM devices (a) cross-point ReRAM device (b) crossbar ReRAM device having multiple interconnected cross-point devices (c) Common bottom electrode ReRAM device.

Multilevel switching has drawn a great interest particularly due to the increasing demands for high-density data storage. The programmability of multilevel resistance states allows a single memory cell to store more than 1-bit of information, hence, enabling high density and miniaturization memory cell implementation [1-3]. While a ReRAM cell can typically have two resistive states, LRS and HRS, storing only 1-bit of information, a multilevel ReRAM can have more than two levels of resistive states, hence allowing a single memory cell to store more than one bit of data [79]. Multilevel switching (MLS) provides an alternative way to increase the data storage density without further reducing the device size which becomes increasingly difficult [3, 51, 79]. Figure 2.6 shows I-V characteristic curve of a multilevel ReRAM device where different compliance currents set the ReRAM device into multi-resistive states [80]. It shows three distinct

LRS states (LRS 1, LRS 2 and LRS 3) which corresponds to the compliance currents of 200 µA, 150 µA and 100 µA, respectively and one HRS state.

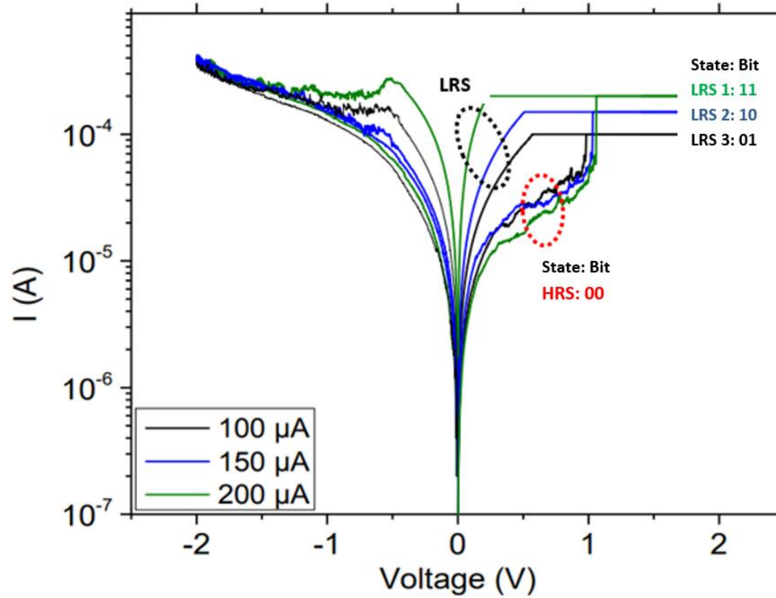

Figure 2.6. Multilevel switching in a ReRAM device represented by I-V characteristics in a semi-log scale showing 4 different states in a single cell by varying the compliance current.

A multilevel resistive memory can have 2^n distinct levels where '*n*' represents the number of bits per cell. In this example, there are four resistance levels including three LRSs and one HRS, i.e., 4 levels = 2^2, hence, this device has 2-bits per cell memory storage.

2.3 Characterization method

The characterization method involves the preset configuration of certain electrical parameters (a compliance current, voltage range, voltage sweep speed, step voltage, and so on) that defines the boundary of operation for the ReRAM device. Various techniques are used to characterize physical properties of ReRAM device such as endurance, stability, hysteresis, and OFF/ON ratio.

2.3.1 Measurement of I-V curve, endurance, and stability

Current – voltage (I-V) measurement is the most fundamental characterization method for a resistive memory device in which a voltage is applied between two electrodes and a current passing through the resistive switching layer is measured. As shown in Figure 2.7 [51], I-V measurement shows characteristics of the device: resistive switching behaviors (unipolar vs. bipolar), hysteresis, OFF/ON ratio, V_{set} and V_{reset}, resistance values for HRS and LRS. Furthermore, by measuring I-V curve multiple times, *aka*., cycling test, device stability and endurance can be characterized as well.

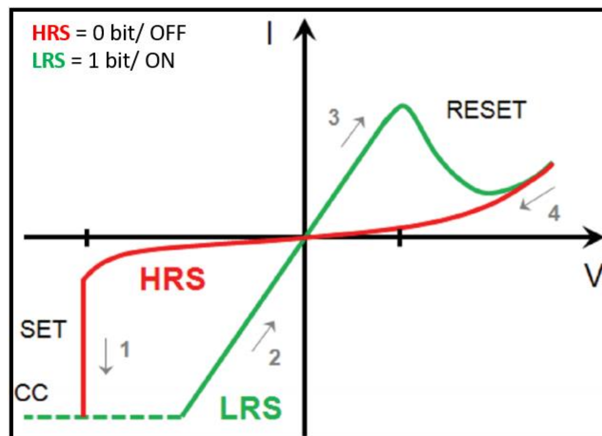

Figure 2.7. Typical I-V sweep showing bipolar resistive switching.

During the I-V measurement, a source meter is typically used to measure the I-V curve with a key set of parameters in the instrument settings. Understanding these parameters is important as they also affect the device performance. These key setting parameters are summarized in Table 2.1 [81].

Table 2.1. Summary of key parameters of I-V measurement instrument

Key setting parameters	
Sweep type	Determines whether to perform the voltage sweeping in a linearly incremental or logarithmically calculated steps.
Start/Stop voltage (Sweeping voltage)	Determines the range of voltage sweep.
Step voltage	Determines the size of the voltage increments during the linear voltage sweeping. Also, determines the data points that are generated during the voltage sweep execution.
Source range	Specifies the test instrument's voltage range used to force the sweep voltage in-order to adjust the voltage resolution and control while the sweeping process.
Compliance current	Protects the device against permanent damage caused by the excessive electric current during the set state.
Current range	Determines the instrument's range for the current measurements. This option controls the resolution of current measurements.
Speed	Determines the speed (Fast, Normal, Quiet or Custom) of the voltage sweep. This can affect switching profile as the response is not instantaneous for most resistive switching materials. The configured speed must compensate the switching rate of the device.
Time settings for the Custom speed	Determines the customized sweep settings for the measurement including the following options to optimize the sweeping operation: Delay Factor – The source waits for the specified delay time after applying the forced voltage to start making a measurement. Usually set between 0 to 100. Filter Factor – This option is used to reduce the measurement noise by applying the filter that fits the voltage sweeping measurement range. This option may also A/D Integration Time – Specifies the A/D conversion time used to measure a signal in units of Number of Power Line Cycles (NPLC). Usually set between 0.1 to 10 NPLC.

Endurance characteristics helps in determining the consistency in resistive switching [3]. Repeated transition between HRS and LRS induces a permanent damage to the materials and its performance degrades gradually. Thus, endurance is defined as the number of times a ReRAM device can be switched between HRS and LRS without losing distinguishable ratio between HRS

and LRS. Endurance is characterized by measuring a few hundred cycles of I-V curve. Then, HRS and LRS of each cycle are calculated from the measured I-V curve and plotted in a separate graph to show how well HRS and LRS hold their values over those cycles [44, 51, 82-85] as is shown in Figure 2.8 [51]. Note that R_{on} and R_{off} correspond to LRS and HRS, respectively.

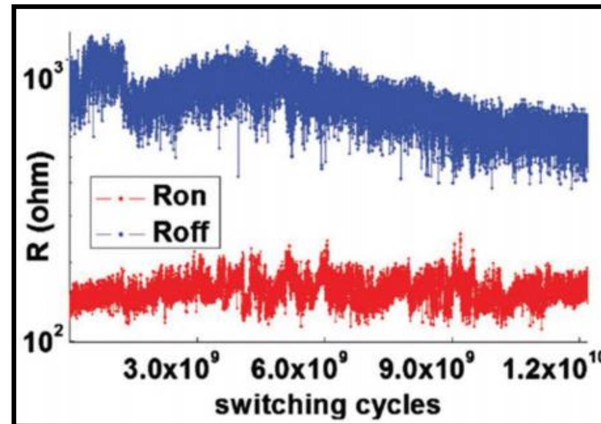

Figure 2.8. Endurance characteristics of a ReRAM device based on molybdenum oxide, using HRS and LRS data extracted from various number of I-V sweep cycles.

Data collected from the endurance test also can be used to determine the variability of the HRS and LRS over the number of cycles through the cumulative distribution, depicting the stability of the ReRAM device [51, 86-90] as shown in Figure 2.9 [51].

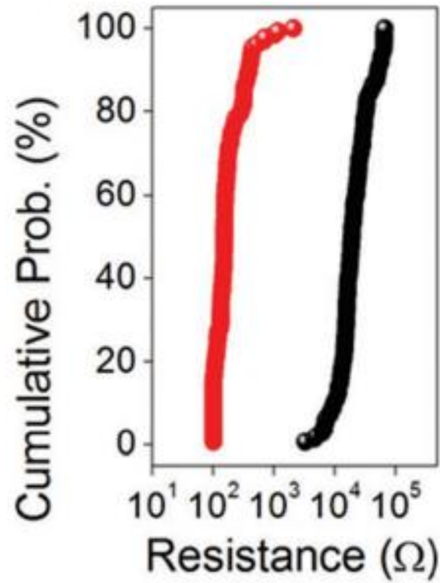

Figure 2.9. Cumulative distributions of HRS and LRS over number of I-V sweeps to analyze the ReRAM device stability. Plotting data is extracted from the endurance characteristics test.

Retention characteristics is the characterization method used to determine the length of time a device can stay in one state i.e., HRS or LRS after programing or erasing. It is evaluated by reading the existing resistive state of the device by applying a small voltage pulse without disturbing the current resistive status [43]. Figure 2.10 shows the retention characteristics of a ReRAM device with HRS (in Red) and LRS (in Black) stretched over time while maintaining the sufficient read margin between the two resistive states.

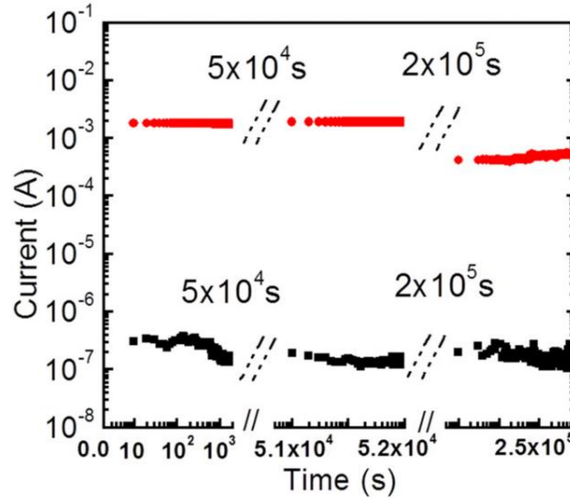

Figure 2.10. Retention characteristics of a ReRAM device, showing the stability of a resistive state i.e., HRS or LRS over the time after the reset and set transitions respectively.

Read disturb characteristics involves the continuous stressing the device by applying voltage pulses and characterizing any degradation in the resistive states. Figure 2.11 shows the read disturb characteristics of a ReRAM device with On-state and Off-states referring to the LRS and HRS respectively.

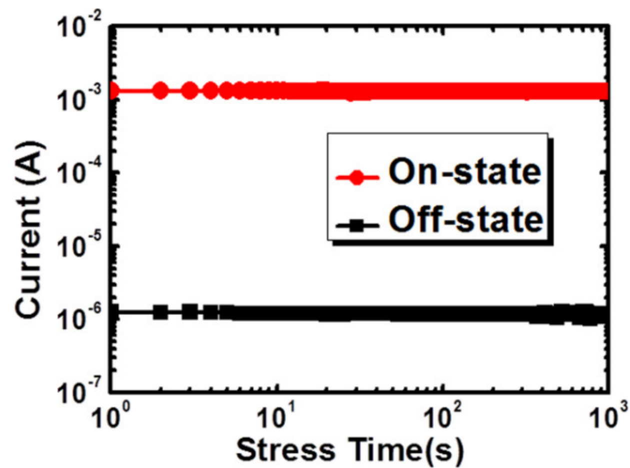

Figure 2.11.Read disturb characteristics of a ReRAM device by applying the continuous read stress pulses.

2.3.2 Forming voltage, set/reset/read voltages, and a compliance current

A ReRAM device is generally considered to realize the HRS in their pristine state. In order to activate its resistive switching behavior, a forming voltage (V_f) is often applied which is relatively higher than its normal set voltage. A forming voltage is typically required only in the initial stage of the device to supplement the atomic diffusion between the two electrodes to set the device in the high conductive state or LRS from its initial state (HRS) [91]. The conductive filament formed between the two electrodes is due to the electrical breakdown of the switching layer when a high electric field is applied between two electrodes. Forming voltage greatly effects the device performance in both positive and negative manner. When considering the positive factor, high forming voltage may result in the formation of the thicker conductive filament at the beginning, hence increasing the conductivity between the two electrodes when the device is in LRS. This initial thickness of the conductive filament leads to the power efficiency factor of the device because in the later characterization efforts, device may only require low operating switching voltages to exhibit the resistive switching behavior. The negative effect of the forming voltage involves the dramatic changes in the switching layer's film morphology including surface damage of the electrode material due to high joule heating effects and unpredictable resistance states which lowers the device success yield [91] .

A set voltage (V_{set}) switches the device resistance state from HRS to LRS. The device after the initial forming process tends to exhibit the resistive switching behavior at a lower voltage than the forming voltage, hence V_{set} is lower than the forming voltage. However, this set voltage is high enough to grow the conductive path in a resistive switching layer, switching the device from HRS to LRS.

A reset voltage (V_{reset}) switches the device resistance state from LRS to HRS. A reset voltage is responsible for rupturing/shrinking the conductive filament to reduce conductance of the resistive switching layer, hence increasing resistance of it. In a bipolar switching device, a reset voltage is usually negative while a set voltage is positive. In a unipolar switching device, the magnitude of a set voltage is higher compared to a reset voltage in the same polarity.

During the set process, there is always a concern of the uncontrolled high current conduction while the device switches from HRS to LRS and this could permanently damage the device. A **compliance current (I_{cc})** is set to limit the amount of current passing though the thin resistive switching layer. A compliance current is also used to induces the multilevel switching operation in a ReRAM and this will be discussed in the next session. A compliance current plays a pivotal role in controlling the device performance throughout the characterization processes.

A read voltage (V_{read}) is a small voltage that is applied to the device to read the current resistive status. In the I-V curve, a read voltage is typically selected near the origin to minimize a power consumption during the reading process. A read voltage also needs to be sufficiently far away from the V_{set}/V_{reset} not to trigger the set/reset process.

Once $V_{set}/V_{reset}/V_{read}$ are determined from the I-V curve, a ReRAM device is practically operated by applying a voltage pulse rather than sweeping voltages.

2.3.3 Multilevel switching characterization

A ReRAM device often exhibit a multilevel switching property in which the device can be set into many different resistive states. By operating a single memory cell with a multilevel switching technique, data storage density can be dramatically increased without increasing the number of memory cells [3, 79].

Multilevel switching can be achieved by several methods during the I-V measurement: (i) by setting a different compliance current, (ii) by applying a different reset voltage, by changing the voltage pulse, aka, Electric Pulse Induced Resistance (EPIR), in which pulse width (iii) or amplitude (iv) are varied [61, 79].

(i) Figure 2.12 [79] illustrates multilevel switching operation with three LRS and one HRS resistance levels by varying the compliance current, showing 2 bits/cell storage. Higher compliance current allows more current to conduct through the resistive layer, hence creating more conductive paths and lowering LRS (Increase in I_{LRS}). While V_{set} is relatively insensitive to a higher compliance current, reset voltage and current increase as the compliance current increases.

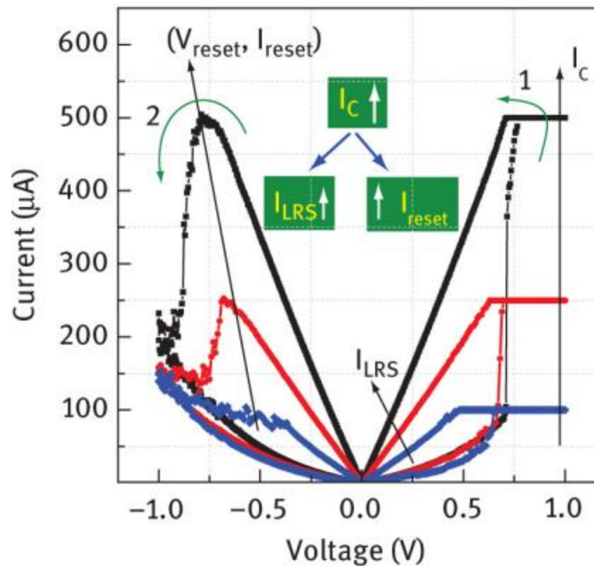

Figure 2.12. Semi-log (I-V) plot illustrating multilevel switching operation by varying the compliance current with 4 distinct levels for 2 bits/cell storage.

(ii) If we vary the reset voltage (reset voltage control method), the device can be set to have many different HRSs. As the applied reset voltage increases, the device can enter the deeper

resetting process, resulting in much higher resistive state. Hence, a multilevel switching device in this mode exhibit one LRS and several different HRSs. As shown in Figure 2.13 [79], the device exhibits three distinct HRS and one LRS, total of 4 resistance states, hence storing 2 bits per memory cell.

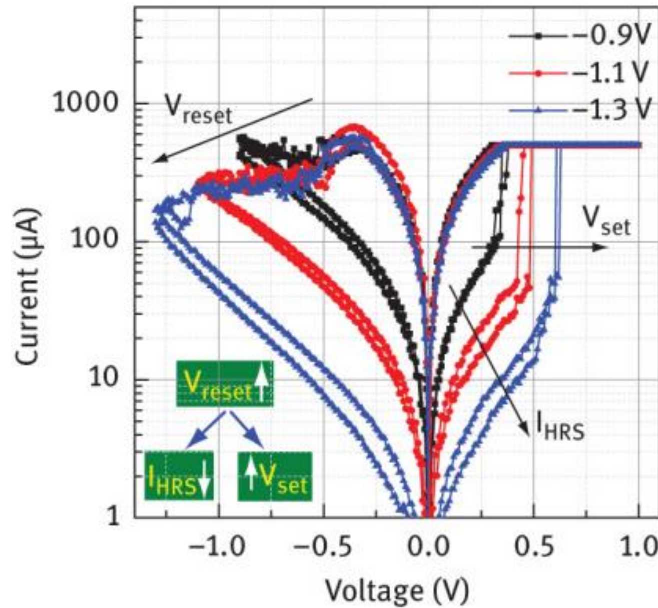

Figure 2.13. Semi-log (I-V) plot illustrating multilevel switching operation by varying the reset voltage with 4 distinct levels for 2 bits/cell storage.

(iii) When a ReRAM device use a voltage pulse for set/reset/read process, a multilevel switching can be obtained by varying set/reset pulse width. By varying the pulse width of set voltage or reset voltage, a device can have many distinct levels of LRS or HRS, respectively.

As shown in Figure 2.14 [92], by drastically varying the reset pulse width from 50 ns to 5 μs in a HfO_x-based ReRAM, three distinct HRS states were achieved. This method is similar to the reset voltage control method. Pulse width variation technique is similar to the varying voltage sweeping rate in an I-V measurement. In fact, device performance depends on the voltage sweeping speed when I-V measurement is used. Pulse width control method exhibits a higher

energy consumption due to the unwanted energy dissipation associated with the intrinsic joule heating in the switching material [79, 92] .

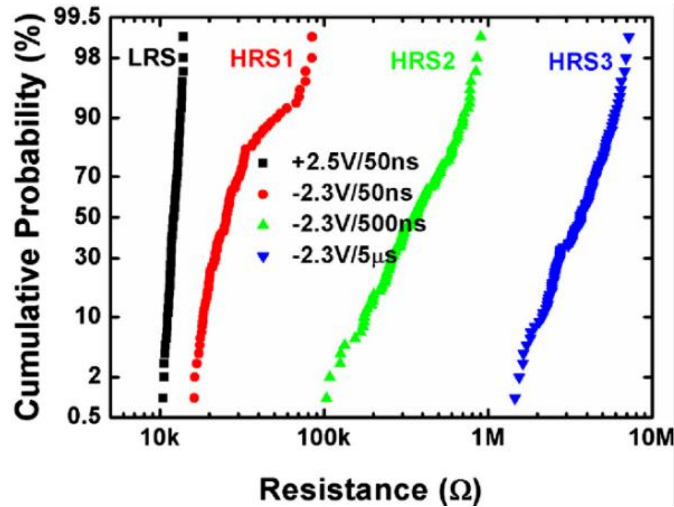

Figure 2.14. Multilevel switching operation achieved by the voltage pulse width control method. Three distinct HRS states achieved by varying the voltage pulse widths (50 ns, 500 ns, 5 µs) while the pulse amplitude is kept constant at -2.3 V.

(iv) Voltage pulse amplitude control is one of the schemes of EPIR method and is used to induce distinct LRS states by varying amplitude of the pulses [61, 92]. Figure 2.15 [61] shows the 2-bit multilevel switching operation in the ReRAM device by the voltage pulse amplitude control scheme where the device exhibits total four distinct resistance levels including three distinct LRS states (level 1, level 2 and level 3) and one HRS state upon application of the different positive voltage pulses of 1 V, 1.5 V and 2.5 V with pulse width of 50 ns and negative voltage pulse with pulse width of 1 µs respectively.

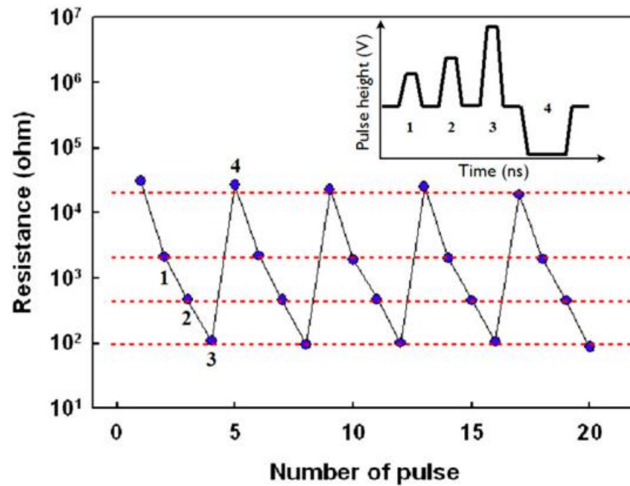

Figure 2.15. Multilevel switching operation achieved by the voltage pulse amplitude control method. Three distinct LRS states achieved by varying the voltage pulse amplitudes of the set voltage (1 V, 1.5 V, 2.5 V) while the pulse width is kept constant at 50 ns.

2.4 Summary

In this chapter, basic structure of a ReRAM device and its operating/characterization techniques are described. Its simple structure and easy operation make a ReRAM technology as one of the promising candidates for the development of the next generation non-volatile memory devices with a fast switching, longer retention time, high storage density, and low power consumption [45, 52, 93-99]. While many dielectric and metal oxide materials have been tested as a resistive switching layer, Molybdenum Oxide (MoO_3) has not been extensively researched as a resistive switching layer. Hence, my research has focused on the demonstration of multilevel switching based on the MoO_3 layer and also explored a novel device architecture for a sensing application of a ReRAM device which is presented in Chapter 3.

Chapter 3

MoO_3 -based ReRAM

This chapter includes the results and discussion of my research on MoO_3-based ReRAM devices. MoO_3 has been a widely used material, preferably as a hole-transport layer for optoelectronic devices such as solar cells and light-emitting diodes, but very rarely as a switching layer for the resistive switching devices [100-105]. It has been reported that ReRAM devices based on MoO_3 show an excellent switching uniformity, retention characteristics, good OFF/ON ratio with a potential for the multilevel switching [45, 52, 93-99].

It is also noticed that ReRAM devices based on MoO_3 have a tendency to show the enhanced memory performance when coupled with the choice of diverse electrode materials in the ReRAM structure. Most noticeable performance has been observed with the Cu and Ag as a top electrode which compliments the growth of the conduction filament in the MoO_3 switching layer during the forming process [45, 96, 97, 106].

Although the potential of multilevel switching operation is highlighted in many studies of the MoO_3 based ReRAM devices, the reports confirming the multilevel feature are scarce.

In-addition, I have also investigated the novel device architecture by fabricating the ReRAM device in a lateral structure where two electrodes are placed in parallel, parted by a switching layer [107-110].

Most of the resistive memory devices are based on the vertical structure, there have been several reports highlighted the lateral structure as a potential candidate for the diverse applications such as memory storage, neuromorphic, computing, security and sensing applications [107-109, 111-115]. The lateral structure can offer significant exposure of the

switching layer to the external environments which is important for a wide range of sensing applications [114, 115].

3.1 Stack device architecture

Stack device structure consists of three layers Au (Bottom electrode)/MoO_3 (Switching layer)/Ag (Top electrode) respectively as shown in Figure 3.1(a).

Ag is one of the commonly used active top electrode along with Cu. It is a crucial element to form a conductive bridge through the switching layer through the oxidation and reduction process [50, 51, 116-118].

MoO_3 is used as the switching layer which is a dielectric medium between the two electrodes that is responsible for the kinetics of the conduction filament formation, breakdown, and variability characteristics of the resistive switching in the ReRAM device [116].

Au is most widely used conductor and is typically used as a bottom electrode. The bottom electrode plays a critical role in the redox process by generating traps for the mobile ions or cations to promote the enhancement of the filament growth [51, 119].

The performance of the ReRAM devices is strongly affected by these layers and Table 3.1 summaries it.

Table 3.1. Functions of each layer in the ReRAM device and how each layer contributes towards the switching characteristics [42, 110, 116, 120, 121]

Layer	Function	Impacted Switching Characteristics
Top Electrode	• Controls the transport mechanism type [116].	• OFF/ON ratio • V_{set} • V_{reset}
Switching Layer	• Control forming, breakdown and variability of switching voltages and current [110, 116, 121].	• Forming voltage (V_f) • V_{set} • V_{reset} • Compliance Current (I_{cc})
Bottom Electrode	• Supplements the redox process [42]. • Generate traps for the mobile ions during the forming or set process to supplement the atomic diffusion between the top and bottom electrodes [120].	• OFF/ON ratio • V_{set} • V_{reset}

Figure 3.1(b) shows the prepared ReRAM devices fabricated on the glass substrate with three different cell sizes that are elaborated in the Figure 3.1(c). The active area of the memory cell plays a critical role towards the device performance because it affects the inherent inconsistency of the device resistive switching characteristics i.e., switching voltages and current due to the stochastic nature of the resistive switching process [51, 79, 96]. The large memory cell area may also incur multiple random weak spots that promotes the irregular geometrical formation of the conductive filament [49, 51].

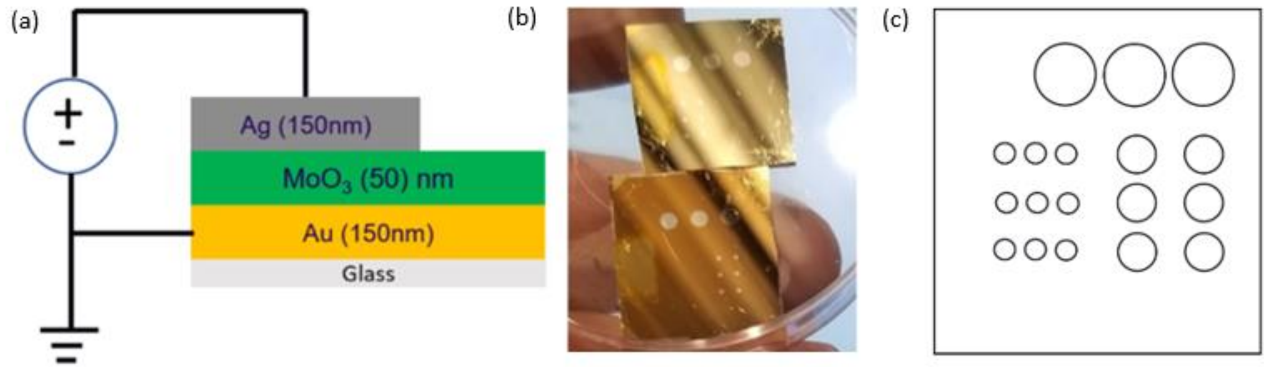

Figure 3.1. ReRAM device structure (a) Stacked metal-insulator-metal structure of a ReRAM device based on MoO_3 as switching layer (b) Actual Image of the fabricated ReRAM samples with three different cell sizes and (c) A Shadow mask design which defines the size of memory cell.

3.2 Stack Device fabrication

The fabrication process included multiple steps. The first step involved the glass substrate preparation which included cutting the glass to 1 inch by 1 inch square (1” × 1”) devices. The glass substrates then went through the cleaning process where samples were sonicated while being submerged into the Acetone solution, IPA solution and DI water for about 20 mins, 10 mins and 10 mins, respectively. The last step of the cleaning involved the plasma cleaning process where the samples were cleaned with plasma for 1 min under the pressure of $\cong 2\times10^{-3}$ torr. After the cleaning process, 150 nm thick Au film was deposited by DC sputtering process onto the glass substrates as a common bottom electrode followed by the deposition of 50 nm MoO_3 via thermal evaporation (2.6×10^{-5} torr and 0.8 Å/s deposition rate). Finally, 150 nm thick Ag was deposited through the shadow mask by using a thermal evaporator (1.2×10^{-5} torr and 1.92 Å/s deposition rate). Although the best practice is to keep maintaining the vacuum between depositing each layer, the vacuum chamber needed to be opened after MoO_3 deposition to place the metal shadow mask manually in the thermal evaporator (Angstrom Engineering, Covap II)

[51]. Table.3.2, shows all the fabrication parameters involved in the deposition process for all the stacked layers.

Table 3.2. Deposition process of stack ReRAM (Au/ MoO_3/Ag) device structure

Au Deposition (Bottom Electrode) by DC Sputterer		
Final thickness achieved	150 nm	
MoO_3 Deposition (Switching Layer) by Thermal Evaporator		
Starting Pressure	1.4×10^{-5} torr	
Rotation of chuck	19.1 rpm	
Evaporation started at	Power:	16.8%
	Pressure:	1.7×10^{-5} torr
Deposition started at	Power:	20.9%
	Pressure:	2.6×10^{-5} torr
	Rate:	0.8 Å/s
Final thickness achieved	50 nm	
Ag Deposition (Top Electrode) by Thermal Evaporator		
Starting Pressure	1.3×10^{-5} torr	
Rotation of chuck	22.1 rpm	
Evaporation started at	Power:	16.9%
	Pressure:	2×10^{-5} torr
Deposition started at	Power:	21.8%
	Pressure:	1.2×10^{-5} torr
	Rate:	1.92 Å/s
Final thickness achieved	150 nm	

3.3 I-V characteristics of a stack ReRAM device

I-V characteristics of the stack structured ReRAM device based on MoO_3 showed a bipolar resistive switching behavior. Characterization of the ReRAM device was conducted using the Keithley 4200 SCS Semiconductor Characterization system and a probe station. The dc voltage biasing was applied at the top electrode, and the bottom electrode was kept grounded at the room temperature.

The precondition of the tests included the programming of the compliance current at 0.1 A, to protect the device against the hard breakdown due to excessive current during the set process, configuring the sweeping voltages and defining the sweeping resolution via step voltage including other critical parameters discussed in Table 2.1. For I-V characteristics, the dc voltage was swept between -0.5 V to + 0.5 V and it showed a bipolar switching behavior, confirming the voltage polarity dependent resistive switching. In the pristine state, the device exhibits the HRS state which was verified when the device shows HRS at near zero voltage before performing the I-V characteristics. One cycle of I-V measurement shows a typical bipolar switching behavior (Figure. 3. 2). The set and reset voltages are around -0.26 V and +0.27 V, respectively as summarized in the Table 3.3 along with other switching parameters, implying that very small voltages can be used for writing/erasing process.

The device also reached the programmed compliance limit of 0.1 A during the set process at -0.43 V and showed a read margin (OFF/ON ratio) of 10.88, calculated by dividing the HRS by LRS to show the distinction between the HRS and LRS resistance levels. The compliance current limits the maximum current allowed for the device and is widely used to induce multilevel resistive switching [51, 79, 122].

The resistive switching behavior of MoO_3 is assumed to be based on the metallic filamentary switching model, where the application of the positive voltage at the top electrode induces the oxidation of the active electrode to produce cations. These cations form a conductive filament by conducting to the bottom electrode where a reduction process takes place. The formed conductive filament is then ruptured upon the application of the negative voltage at the top electrode, representing the reset process [1-3, 39-41, 63, 88, 120].

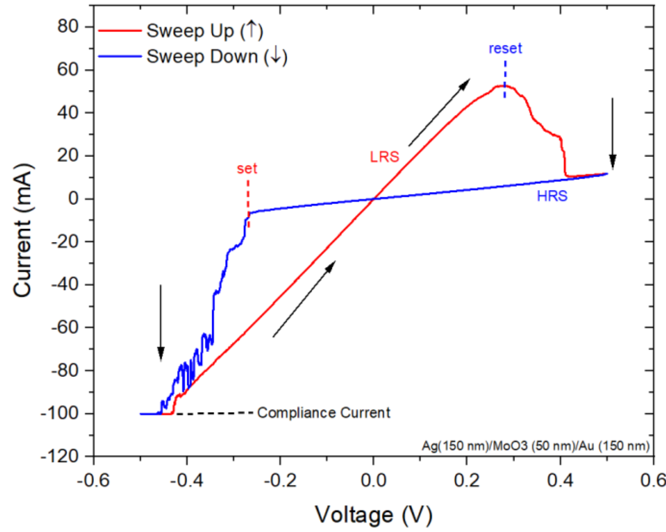

Figure 3.2. I-V characteristics of the MoO_3-based ReRAM in the stack configuration showing bipolar resistive switching.

Table 3.3. Summary of I-V characteristics obtained from Figure 3.2

V_{read} (V)	HRS (Ω)	LRS (Ω)	OFF/ON	V_{set} (V)	V_{reset} (V)	I_{set} (mA)	I_{reset} (mA)	Compliance Current (A)	Switching Mode
0.01	48.15	4.43	10.88	-0.26	0.27	-6.59	52.72	0.1	Bipolar

3.4 Multilevel switching property based on stack structure

With the multilevel switching operation *a.k.a.*, multiresolution operation, a single memory cell can exhibit enhanced storage density by storing more than 1 bit of information [3, 92, 123, 124]. There are multiple ways to induce the multilevel switching in a resistive switching device, but the conventional scheme involves the control of the resistance levels of the LRS by varying the compliance current during the set process [83, 118, 125]. In this way, memory density can be increased significantly without requiring any complicated fabrication processes to increase the number of memory cells per area [122, 126-128].

To supplement my research about the multilevel operation in a resistive switching device, I have fabricated multiple ReRAM devices in a stack structure with a configuration of Au (Bottom

electrode)/ MoO_3 (Switching layer)/ Ag (Top electrode). The devices were successfully demonstrated as a multilevel resistive memory device and are discussed in detail in the next sections.

3.4.1 Multilevel switching reported by other people

Multilevel switching property in the MoO_3-based ReRAM devices has been discussed by several researchers [39, 50, 52, 62], but with very few demonstrations [45, 94] which is summarized in Table 3.4.

Arita et al. investigated thermally oxidized MoO_3 as a switching layer in the device of Pt-Ir/ MoO_3/Pt configuration. [39]. When MoOx was paired with Cu and Tin (Cu/MoO_x/Tin), it showed two set modes and two reset modes upon the formation and rupture of the conductive filament during the over-set and over-reset processes, respectively [50].

Yoon et al. investigated the possibility of multilevel switching operation in the ReRAM device having a Pt/Cu:MoO_x/GdO_x/Pt structure by controlling the value of LRS via external load resistor during the accelerated transitions (accelerated ion migration caused by the thermal stress) between the two resistive states i.e., HRS and LRS under variable temperatures, ranging from 200 °C to 250 °C. Yoon showed that the retention period of the LRS could go over ten years at 85 °C [97].

Similarly, **Jo** et al. also reported a multilevel switching in a device of Pt/Cu/MoO_x/AlO_x/Al structure where an NMOSFET is connected to the bottom electrode. The multilevel switching was observed by controlling the resistance levels by varying compliance current which is controlled by the gate voltage (V_g) of the n-channel MOSFET. By applying a higher V_g, higher compliance current flows which results in a lower LRS. This experiment demonstrated a

versatile method to attain the target resistance levels which is a critical parameter for the multilevel switching operation [94].

Dai et al. reported the excellent retention characteristics for the ReRAM device based on the MoO_3. The device has a configuration of Au/MoO_{3-x}/Au where MoO_{3-x} thin film was deposited via atomic layer deposition (ALD) process. The device exhibited a bipolar switching properties and its operation was explained based on the oxygen filamentary transport mechanism. They showed OFF/ON ratio of more than 20, sufficient for the multilevel switching operation in the device. In addition, the device showed low operating current and voltage which is one of the key parameters in defining the good performance of a ReRAM device [98].

Kudo et al. studied the switching operation of the ReRAM device based on Pt/Cu/MoO_x/Tin structure by investigating the inner structural changes through *in situ* transmission electron microscopy (TEM). It was observed that the size of the conduction filament was increased as the compliance current was increased during the set process which explains well how we set the ReRAM device into a different LRS state by varying the compliance current [95].

Table 3.4. Summary of MoO_x-based ReRAM studies performed by other people

Reference(s)	**Structure**	**I-V characteristics**	**Observed switching properties**	**Observed performance**
Arita et al. [39]	Pt-Ir/ MoO_3/Pt	• Voltage sweeping. • Cycling characteristic.	• **Switching mode/:** Unipolar and bipolar. • **Unique switching properties:** Coexistence of unipolar and bipolar switching modes. • **Multilevel switching:** No multilevel switching reported.	• **Resistive Switching:** Low reproducibility of resistive states. • **Endurance:** low stability.
Arita et al. [50]	Cu/MoO_x/ Tin	• Voltage sweeping. • Cycling characteristics.	• **Switching mode:** Bipolar switching mode. • **Unique switching properties:** Two set and two reset switching modes	• **Resistive Switching:** Low reproducibility of resistive states. • **Retention**: Time for LRS was maintained for at least 3 hours.

		• Retention characteristics. • Endurance characteristics by varying pulse width.	during over-set and over-reset processes. • **Multilevel switching:** No multilevel switching reported.	• **Endurance:** Low, unstable resistive switching after 23rd cycle. • **Switching rate:** Slow.
Yoon et al. [45]	Pt/Cu:MoOx/GdOx/Pt	• Voltage sweeping. • Cycling characteristics by applying voltage pulses. • Retention characteristics.	• **Switching mode:** Bipolar switching mode. • **Multilevel switching:** No multilevel switching reported.	• **Resistive Switching:** Good reproducibility of resistive states. • **Retention:** Time of ten- year data retention. • **Endurance:** Stable over 10^4 cycles.
Jo et al. [94]	1T1R: (Pt/Cu/MoOx/AlOx/Al)	• Voltage sweeping. • Cycling characteristics.	• **Switching mode:** Bipolar switching mode. • **Multilevel switching:** Multilevel switching reported by varying compliance current.	• **Resistive Switching:** Reproducibility of resistive states captured only for ten cycles.
Dai et al. [98]	Au/MoO_{3-x}/Au	• Voltage sweeping. • Retention characteristics.	• **Switching mode:** Bipolar switching mode. • **Multilevel switching:** No multilevel switching reported.	• **Resistive Switching:** Uniform reproducibility of resistive states. • **Retention:** Excellent retention with the OFF/ON ratio > 20 was observed for 1400 seconds. • **Operating requirements:** Device exhibits resistive switching at low switching voltages i.e., V_{set} and V_{reset}.
Kudo et al. [95]	Pt/Cu/MoOx/Tin	• Voltage sweeping.	• **Switching mode:** Bipolar switching mode.	Device performance parameters are not specified in the research paper.

3.4.2 Multilevel operation by varying a compliance current

I investigated multilevel switching in the Au (150 nm)/MoO_3(50 nm)/Ag (150 nm) devices by varying the compliance current sequentially (20, 40, 60, 80 and 100) mA as shown in Figure 3.3. The device exhibited a reliable multilevel switching and showed five distinct resistance levels at LRS and one resistance level at HRS, resulting in total six distinct resistance levels, representing

at least 2-bit per cell storage. Higher than 2-bit multilevel switching is possible if the compliance current is adjusted for the additional intermediate resistance levels at the cost of a read margin among the distinct LRS resistances. However, it may reduce the read margin, hence negatively affecting the reliability of multilevel switching operation.

It was observed that by increasing the compliance current, LRS decreased linearly from 10.80 Ω to 4.36 Ω (Fig. 3. 3 (c)). HRS is well separated from LRS except for the compliance current of 80 mA. By excluding data at this compliance current, HRS exhibits 47.1 ± 2.2 Ω. For the switching voltages, it exhibits very consistent setting/resetting voltages (V_{set} = -0.28 ± 0.02 V and V_{reset} = 0.26 ± 0.05 V) across the various compliance currents (20 ~ 100 mA). These results are also well matched to what has been discussed by Amit et al. [79] as discussed previously in section 2.3.3.

It is also observed that the adequate OFF/ON ratio of 4 to 10 (= HRS/LRS) were maintained over the wide range of compliance currents. This could further contribute to the improved device endurance and retention characteristics which measures how long the device can maintain the distinction between the HRS and LRS until it is completely degraded i.e., when there is no obvious difference between the two states (HRS and LRS) [51, 79].

For a multilevel switching, it is equally important to discern the different LRS values accurately which is often referred as a read margin. A read margin can degrade due to many different reasons and possibly lead to the failure of device [79, 129, 130]. Table 3.5 also summarizes the LRS read margin during the successive compliance variations.

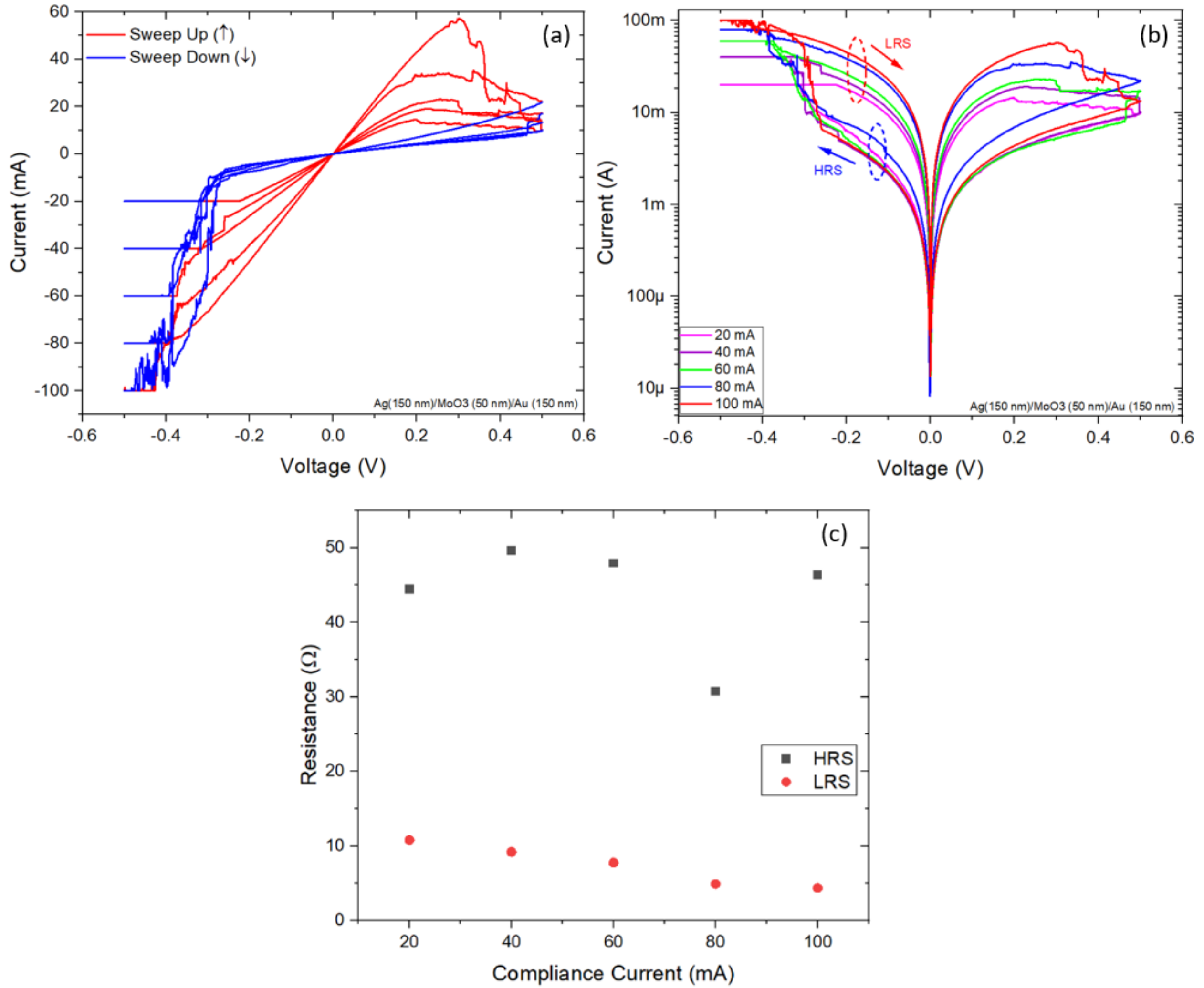

Figure 3.3. Multilevel switching operation by varying the compliance current in the stack ReRAM device having Au/MoO_3/Ag structure (a) illustrates the multilevel cell operation in a linear scale, (b) illustrates the multilevel cell operation in a semi-log scale and (c) Resistive states as a function of compliance current.

Table 3.5. Summary of I-V sweep parameters from multilevel switching operation in Figure 3.3

Resistive switching parameters								
Compliance Current (mA)	**V_{read} (V)**	**HRS (Ω)**	**LRS (Ω)**	**OFF/ON**	**V_{set} (V)**	**V_{reset} (V)**	**I_{set} (mA)**	**I_{reset} (mA)**
20	-0.005	44.42	10.80	4.11	-0.27	0.20	-10.61	14.03
40		49.60	9.20	5.39	-0.29	0.22	-9.55	18.95
60		47.90	7.75	6.18	-0.31	0.30	-9.13	22.22
80		30.71	4.91	6.25	-0.31	0.34	-11.04	35.39
100		46.36	4.36	10.63	-0.26	0.30	-6.64	57.05

LRS read margin	
Compliance current (mA)	**Read margin (Ω)**
Between 20 to 40	1.60
Between 40 to 60	1.45
Between 60 to 80	2.84
Between 80 to 100	0.55

3.4.3 Stability of MoO_3-based ReRAM device

The **endurance** characteristics is one of the critical aspects of the ReRAM device performance metrics that defines the maximum transitions (cycles) between LRS and HRS in which the device endure until the difference between the two states is indistinguishable. In other words, it represents how long the ReRAM can hold a readable margin between the HRS and LRS [51, 79, 85].

Figure 3.4 shows 6 out of 11 cycles to observe the endurance characteristics of the tested device, having slight variations among all the cycles which is possibly ascribed to the uncontrolled compositional deviation of the filament at each cycle [33]. Sweeping data from the endurance test is summarized in Table 3.6.

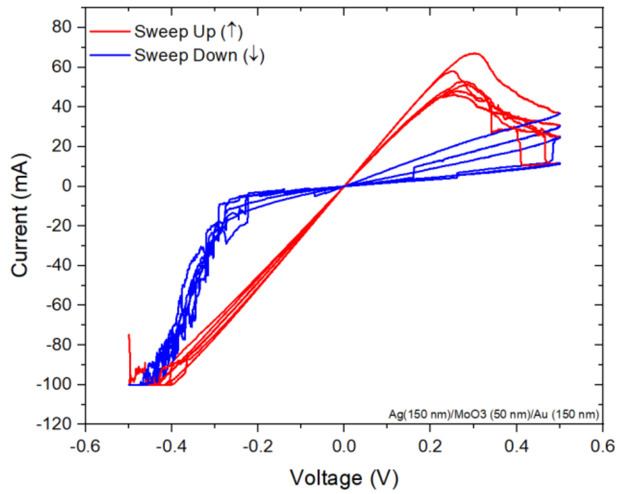

Figure 3.4. I-V sweep characteristics in linear scale showing endurance properties measured by transitioning (Cycles# 1,3,5,7,9,11) between set and reset, swept over 11 cycles.

It is also important to maintain a good OFF/ON ratio which is a measure of the read margin between the HRS and LRS resistance levels (HRS and LRS) when the device is subjected to repetitive voltage sweeping cycles during the endurance characteristics [51, 85]. In this regard, our ReRAM device showed a low to medium read margin (≅ 2 to 11) between the HRS and LRS levels whose values were measured at 0.01 V over 11 sweeping cycles as shown in Figure 3.5.

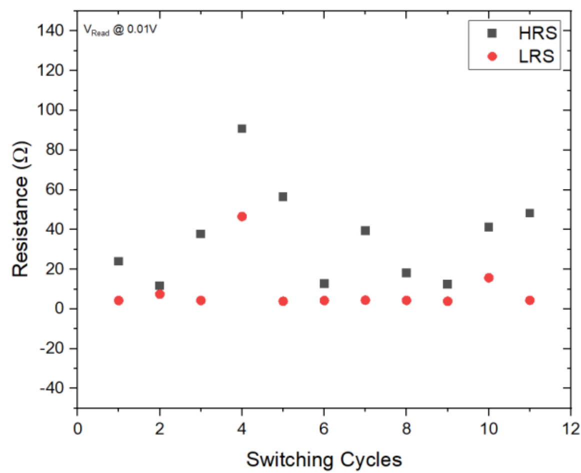

Figure 3.5. Endurance performance measured via HRS-LRS resistances read at 0.01V over 11 cycles.

The statistical analysis of the cycle-to-cycle dispersion of HRS and LRS over the 11 cycles can also be determined by plotting the cumulative distribution of the HRS and LRS resistances levels as shown in Figure 3.6. The calculated mean and the standard deviation of HRS and LRS defining the dispersion over 11 voltage sweeping cycles is around 36.00 ± 24.00 for HRS and 9.43 ± 13.00 for LRS.

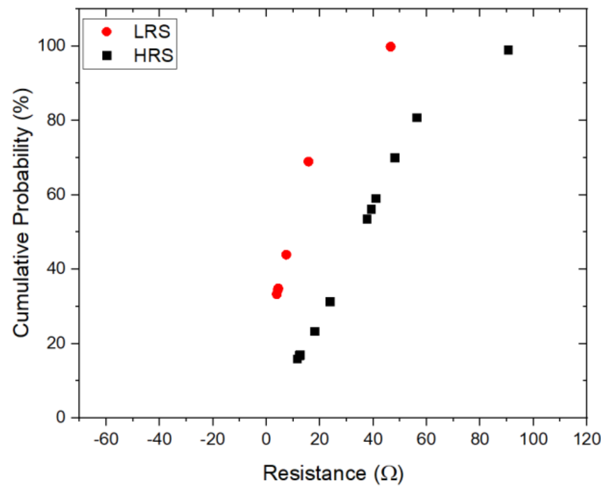

Figure 3.6. Cumulative distribution of the HRS and LRS resistance levels over 11 cycles.

The device also exhibited a minimal variation in the switching voltages (V_{set} and V_{reset}), measured for over 11 sweeping cycles as shown in Figure 3.7. The voltage difference between the set (0.22 – 0.29) V and the reset (0.15 – 0.30) V was around 0.59 V with a cycle-to-cycle variation of 0.26 ± 0.02 and 0.25 ± 0.05 respectively. This looks good for 11 cycles, but extended number of cycles is required to determine the long-term stability. The cumulative distribution of the switching voltages is shown in Figure 3.8, indicating the controlled formation and rupture of the conduction filament during the switching operation [86].

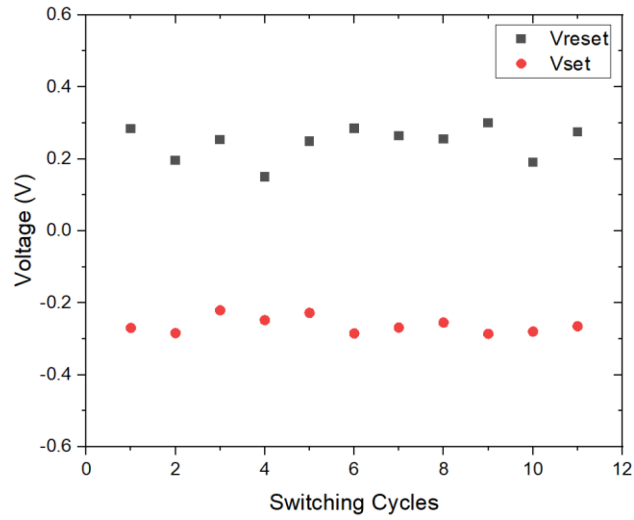

Figure 3.7. Stability of the switching voltages (V_{set}-V_{reset}) over 11 cycles.

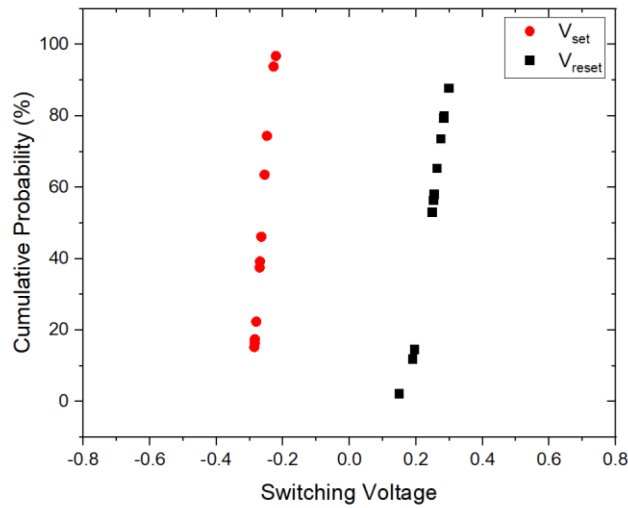

Figure 3.8. Cumulative distribution of the V_{set} and V_{reset} switching voltages over 11 cycles.

Table 3.6. Summary of sweeping parameters from the I-V measurement performed in Figure 3.4

Resistive switching parameters									
Cycle #	**V_{read} (V)**	**HRS (Ω)**	**LRS (Ω)**	**OFF/ON Ratio (HRS/LRS)**	**V_{set} (V)**	**V_{reset} (V)**	**Compliance Current (mA)**	**I_{set} (mA)**	**I_{reset} (mA)**
1		23.94	4.29	5.58	-0.27	0.28		-17.17	51.05
2		11.64	7.46	1.56	-0.28	0.20		-13.76	17.04
3		37.75	4.29	8.79	-0.22	0.25		-4.98	46.11
4		90.69	46.55	1.95	-0.25	0.15		-2.79	6.44
5		56.48	3.91	14.46	-0.23	0.25		-4.97	57.98
6	0.01	12.67	4.31	2.94	-0.26	0.29	100	-31.32	53.64
7		39.37	4.44	8.86	-0.27	0.26		-11.87	47.82
8		18.14	4.37	4.15	-0.26	0.26		-20.75	51.48
9		12.52	3.89	3.22	-0.29	0.30		-9.11	66.9
10		41.09	15.75	2.61	-0.28	0.19		-8.76	8.82
11		48.15	4.43	10.88	-0.27	0.28		-6.59	52.72
Statistics		36.00 ± 24.00	9.43 ± 13.00	6.00 ± 4.00	0.26 ± 0.02	0.25 ± 0.05		12.00 ± 8.43	42.00 ± 21.00

3.5 Lateral device architecture

ReRAM Implementation in lateral structure is illustrated in Figure 3.9. This ReRAM layout can lead to multiple opportunities in the flexible and wearable technologies and many sensing applications by exposing the larger sensing area to the external environments [107, 124].

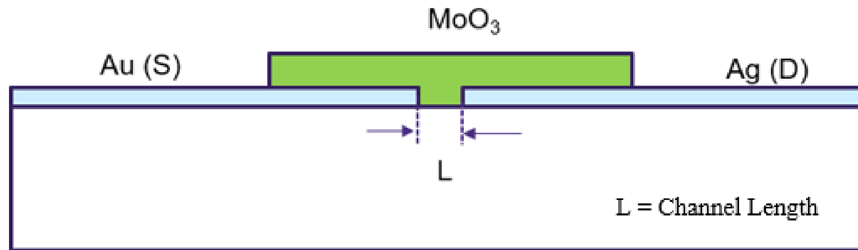

Figure 3.9. Cross-sectional view of the lateral ReRAM device based on MoO_3 as a switching layer where, L represents different lengths of the switching material between the two electrodes, forming the dielectric region.

Lateral device structure, as the name implies, has a planar arrangement of the metal-insulator-metal layers. As shown in Figure 3.10(a), there are six ReRAM memory cells

fabricated over the glass substrate with six distinct channel lengths covered by the switching layer (MoO_3) [107, 108]. The material selection of the lateral devices was the same as that of the stacked device, i.e., Au-MoO_3-Ag.

Figure 3.10(b) shows the cross-sectional view of the lateral ReRAM memory cell structure where MoO_3 (Switching layer) connects two electrodes, Au and Ag. The distance between these two electrodes defines the channel length. Only two electrodes are used for I-V measurement: Drain (D) electrode as an anode to induce the resistive switching and Source (S) as a ground.

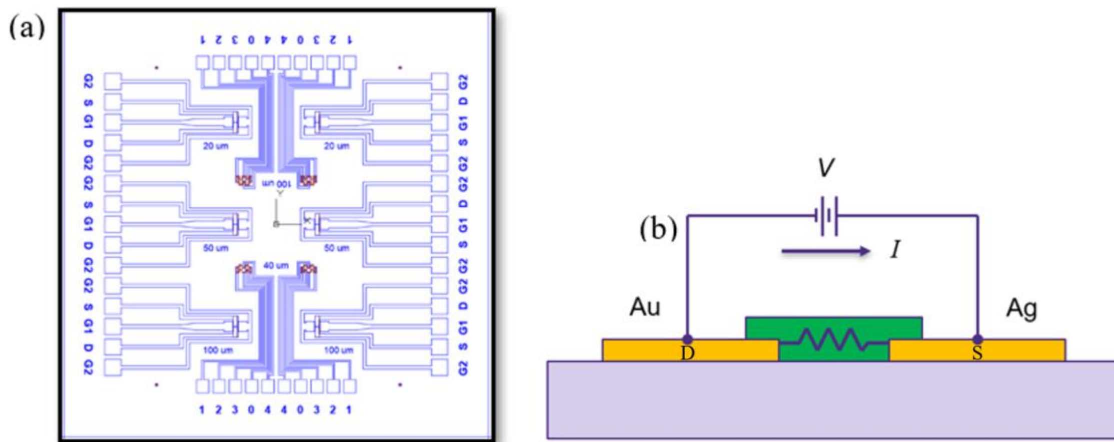

Figure 3.10. ReRAM device structure (a) Lateral ReRAM device based on MoO_3 as a switching layer with distinct channel lengths (b) Cross-sectional view of the lateral ReRAM device, resistor in the middle of the two electrodes illustrates the diverse dielectric medium channel lengths.

3.5.1 Motivation behind studying the lateral device structure

Resistive switching in a laterally structured ReRAM devices in general has not been extensively studied compared to the stacked configuration [108-110, 115]. Even though the stack ReRAM devices have shown good resistive switching characteristics [45, 98], its configuration has several limitations and challenges involving the leakage currents, parasitic capacitance and cross-resistance among the neighboring memory cells [112]. To overcome the issues involving the cross-interference among the adjacent memory cells and leverage the opportunity of scalable

and flexible integrations with the external circuitry, an alternative approach was introduced: lateral ReRAM devices [107, 115]. Furthermore, lateral device can offer additional unique opportunity as a sensing element which is generally not possible in a stacked device due to its limited sensing area [107, 108]. By utilizing a large sensing area in a lateral device, the memory device can be used as a combination of sensor/memory.

In recent studies, lateral ReRAM devices have shown the promising stability and performance and a potential in the memory storage, neuromorphic, computing, security and sensing applications [107, 108, 113, 114]. Congli He et al. reported the excellent memory characteristics of a two-terminal planar Ti/Au/Nanographene/Ti/Au graphene/SiO_2 nanogap ReRAM device, exhibiting the endurance up to 10^4 cycles, retention period of more than 10^5 seconds and switching rate of 500 ns. The device also showed the property of tunable resistance levels upon varying the reset voltages, confirming the multilevel switching operation [109].

In this research, I explored the potential of the lateral device structure in the diverse applications including memory storage, neuromorphic, computing, security and sensing applications.

3.6 I-V characteristics of a lateral ReRAM device

Figure 3.11 shows the I-V characteristics of our lateral ReRAM device, having a channel length of 4.5 μm. Due to the higher intrinsic resistance values and a long channel length, voltage sweeping at a higher range between ±210 V was required to demonstrate a resistive switching with the compliance current programmed at 0.1A.

The device exhibits a nonconventional resistive switching mode in this lateral structure having three sets (set A at -40 v, set B at 40 V and set C at -10 V) and two resets (reset A at 40 V and reset B at -40 V). The device exhibited reset (reset A) and set (set B) at around the same

voltage i.e., 40 V which makes the set/reset process difficult due to their close overlapping. The device also showed another set voltage at -10 V (set C). Two consecutive setting process means two different LRS whose values depend on the reading voltage. For example, the resistance values measured between -10V and 40V is different than when the value is measure below -10 V. This could make the read/write process more complicated.

The device also exhibits the read margin (OFF/ON ratio) of >10 which is relatively low compared to other studies [3, 131-134]. HRS and LRS were read at different read voltages i.e., 110 V and 5 V respectively due to a non-conventional resistive switching hysteresis. I-V measurement data is summarized in Table 3.7.

In addition, the device also showed a self-compliance ability due to the micrometer scale channel length which is several orders higher than the stacked device in which switching layer is typically few tens of nanometers in thickness. This is an added benefits in the lateral configuration where no external current limiting circuit is required during the set process [135-137]. Conclusively, the device showed many unique features which are not completely evaluated yet for any applications and require further studies.

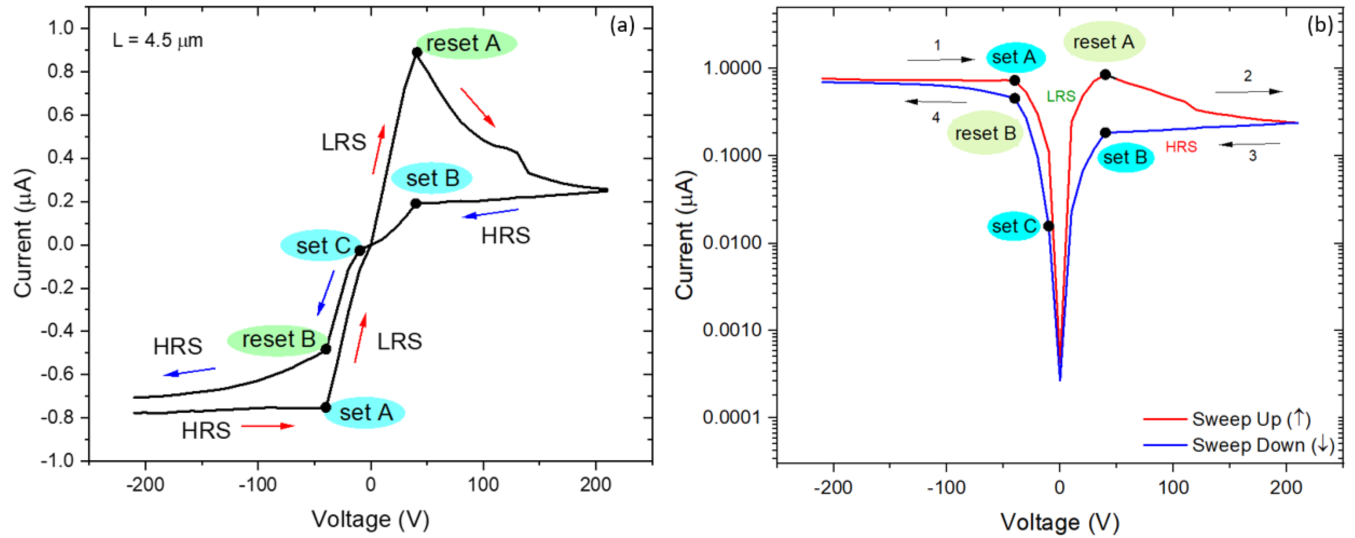

Figure 3.11. I-V curve from the 100th cycle of the endurance characteristics of a lateral ReRAM device with 4.5 µm channel length. (a) I-V sweep in a linear scale and (b) I-V sweep in a semi-log scale, showing multiple set and reset operations.

Table 3.7. Summary of switching parameters from the I-V sweep characteristics in Figure 3.8

<table>
<tr><th colspan="6">Resistive switching parameters</th></tr>
<tr><th colspan="6">Resistances</th></tr>
<tr><th>V_{read} - HRS (V)</th><th>V_{read} - LRS (V)</th><th>HRS (MΩ)</th><th colspan="2">LRS (MΩ)</th><th>OFF/ON Ratio (HRS/LRS)</th></tr>
<tr><td>110</td><td>5</td><td>436</td><td colspan="2">41</td><td>10.63</td></tr>
<tr><th colspan="6">Voltages</th></tr>
<tr><th>V_{set} A (V)</th><th>V_{set} B (V)</th><th>V_{set} C (V)</th><th colspan="2">V_{reset} A (V)</th><th>V_{reset} B (V)</th></tr>
<tr><td>-40</td><td>40</td><td>-10</td><td colspan="2">40</td><td>-40</td></tr>
<tr><th colspan="6">Currents</th></tr>
<tr><th>I_{cc} (µA)</th><th>I_{set} A (µA)</th><th>I_{set} B (µA)</th><th>I_{set} C (µA)</th><th>I_{reset} A (µA)</th><th>I_{reset} B (µA)</th></tr>
<tr><td>-0.77</td><td>-0.73</td><td>0.19</td><td>-0.02</td><td>0.86</td><td>-0.46</td></tr>
</table>

3.6.1 Stability characteristics of the lateral device

The ReRAM device was subjected to 120 repetitive voltage sweeping cycles between ±210 V with the current compliance set at 0.1 A to determine the endurance characteristics. The device endured the resistive switching properties up to 105 cycles but lost the hysteresis afterwards.

Up till 105 cycles, the device showed the continued variability in the HRS and LRS states as the number of cycles increased. After the set process at -40 V, corresponding to the Set A in the Fig. 3. 11 (a), the current rapidly increases but never reached the programmed compliance level as shown in Figure 3.12 (a) and (b) which demonstrate a self-compliance mechanism. Hysteresis varies as more cycles are added which may correspond to the progressive growth of the conductive path in the MoO_3-based dielectric medium [138, 139].

Figure 3.12(c) illustrates the relationship between the HRS-LRS resistance states and number of sweeping cycles to determine the endurance and stability of the resistive switching operation. The device showed the continued trend of decreasing HRS and LRS resistance levels, hence showing increased switching current (I_{CC}, I_{set}, I_{reset}). After 20 cycles, the read margin improved a lot, i.e., wider separation between HRS and LRS, but it degraded as more cycles were added. However, the switching voltage remained constant throughout the endurance characteristics, indicating the well-controlled transport mechanism during the switching process [86].

Figure 3.12(d) illustrates the cumulative distribution of the HRS and LRS over 105 cycles of I-V sweep to demonstrate the HRS and LRS dispersion due to the cycle-to-cycle variations. Also, the dispersion is calculated from the cycling characteristics data as 1.82 ± 1.05 for HRS and 0.41 ± 0.39 for LRS which further confirmed the varying trend in the resistive switching operation, showing lower stability. I-V measurements are summarized in the Table 3.8.

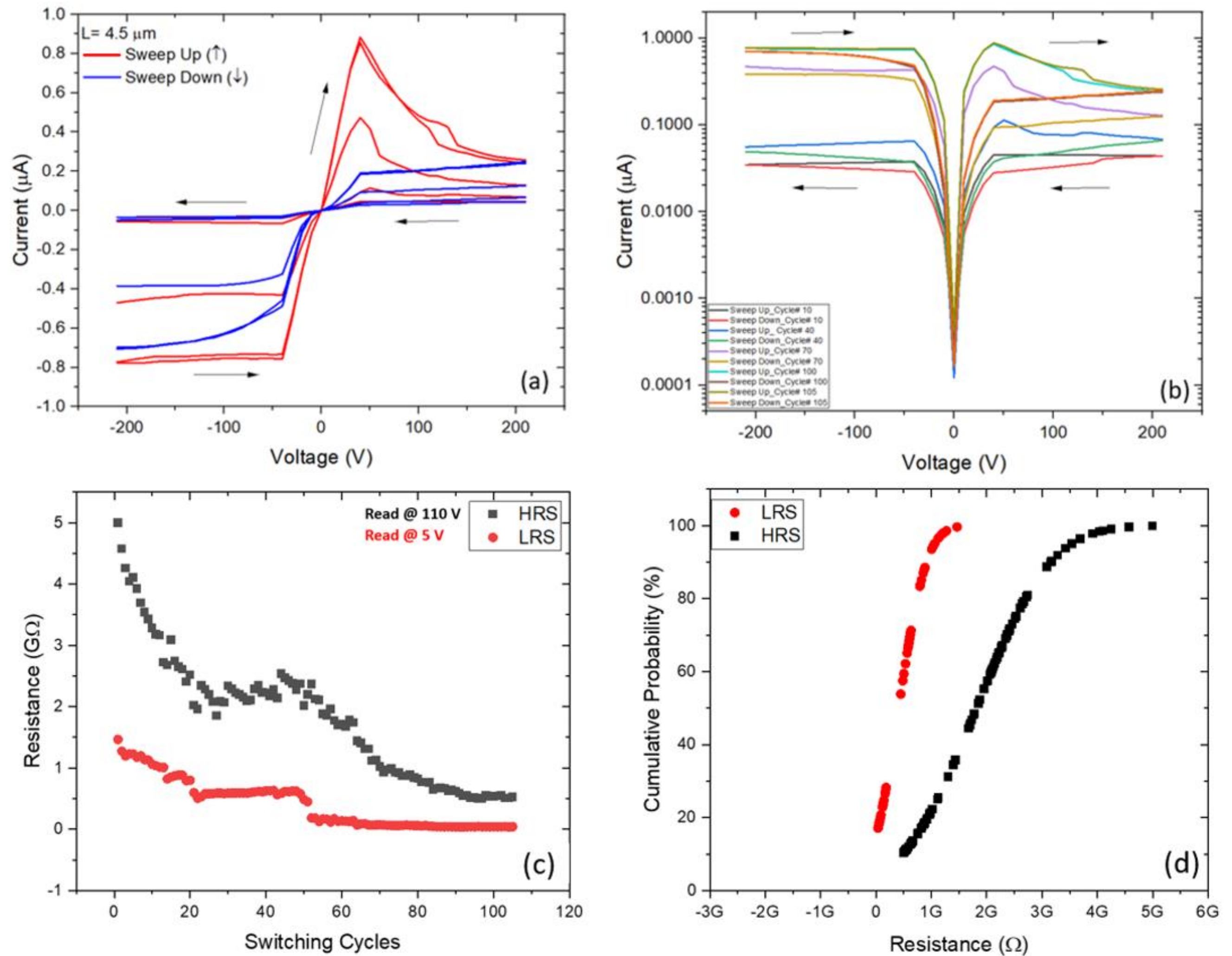

Figure 3.12. Endurance and stability characteristics of a 4.5 μm channel length lateral ReRAM device. (a) Cycling characteristics (I-V sweeps) with 105 cycles in a linear scale, (b) I-V sweep cycles in a semi-log scale, (c) Endurance characteristics with HRS and LRS over the number of sweeping cycles read at 110 V and 5 V respectively from the cycling characteristics and (d) Statistical analysis representing the cumulative distributions of the HRS and LRS.

Table 3.8. Summary of resistive switching parameters from I-V characteristics in Figure 3.9

Resistive switching parameters					
Resistances					
Cycle #	**V_{read} - HRS (V)**	**V_{read} - LRS (V)**	**HRS (GΩ)**	**LRS (GΩ)**	**OFF/ON Ratio (HRS/LRS)**
10	110	5	1.82	1.06	1.71
40			1.50	0.63	2.38
70			0.82	0.08	10.81
100			0.44	0.04	10.64
105			0.42	0.04	9.85
Statistics			1.82 ± 1.05	0.41 ± 0.39	7.00 ± 5.00
Voltages					
Cycle #	**V_{set} A (V)**	**V_{set} B (V)**	**V_{set} C (V)**	**V_{reset} A (V)**	**V_{reset} B (V)**
10	-40	40	-10	40	-40
40	-40	40	-10	40	-40
70	-40	40	-10	40	-40
100	-40	40	-10	40	-40
105	-40	40	-10	40	-40

Currents						
Cycle #	**I_{cc} (μA)**	**I_{set} A (μA)**	**I_{set} B (μA)**	**I_{set} C (μA)**	**I_{reset} A (μA)**	**I_{reset} B (μA)**
10	-0.04	-0.04	0.03	-0.01	0.05	-0.03
40	-0.06	-0.07	0.04	-0.01	0.09	-0.04
70	-0.47	-0.43	0.09	-0.02	0.47	-0.32
100	-0.77	-0.73	0.19	-0.02	0.86	-0.46
105	-0.78	-0.76	0.19	-0.02	0.88	-0.49

3.6.2 Effect of different channel lengths on the MoO_3-based resistive switching properties

Two substrates were prepared having six ReRAM memory devices fabricated on each sample and each ReRAM device had a different MoO_3-based dielectric channel length between the two electrodes. Out of twelve ReRAM devices, unfortunately, only four devices (L = 2.0, 3.0, 4.5, and 9.0) µm showed the hysteresis while others showed no observable hysteresis and one of the devices was shorted during the measurement. Also, none of the working devices showed

current reaching the programmed compliance level during the characterization process while they share the same test configuration parameters.

Endurance characteristic was conducted for 120 cycles and the devices (2.0, 3.0, and 9.0 µm) showed observable hysteresis only for several cycles while the 4.5 µm device showed the observable hysteresis for up to 105 cycles.

As was expected, it was observed that all the working devices showed the increasing span of the HRS and LRS resistances as the channel length increases as shown in Figure 3.13, and the data is summarized in Table 3.9.

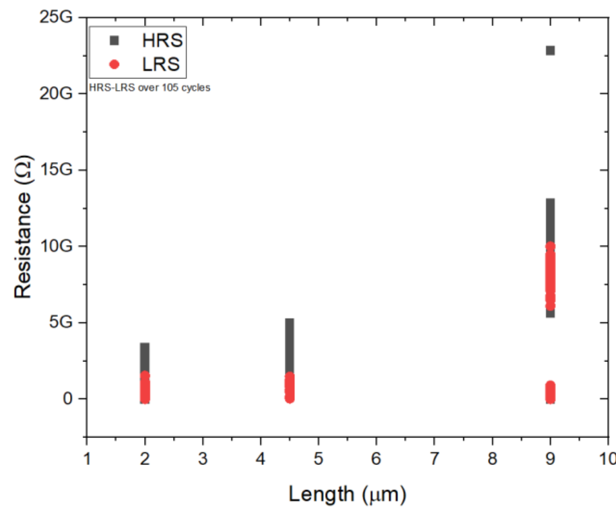

Figure 3.13. Length vs switching resistance levels (HRS and LRS) of (2.0, 4.5 and 9.0) µm lateral MoO_3-based ReRAM devices.

It is to be noted that Figure 3.13 includes the data for all the cycles including the ones with insignificant hysteresis. The main idea of presenting the Figure 3.13 is to highlight the expansion of the HRS and LRS resistance spectrum respective to the varying channel lengths.

Table 3.9. Summary of switching resistances over 105 for each dielectric length

Length (µm)	**Cycles**	**Statistics**	
		HRS (GΩ)	**LRS (GΩ)**
2.0	105	0.68 ± 1.15	0.15 ± 0.28
4.5		1.82 ± 1.05	0.41 ± 0.39
9.0		6.20 ± 5.37	5.05 ± 3.92

3.6.3 Self-compliance property of the lateral ReRAM device

As discussed before, the compliance current is set to protect the device against the excessive electric current during the forming or set process [66, 73-75, 135]. Figure 3.14(a), illustrates I-V curve of our stack ReRAM device, showing the bipolar switching behavior with reset at around 0.28 V and set at around -0.27 V. For I-V characteristics, the compliance current was set at 0.1 A and the stack device was noticed to hit the compliance level every time during the set process even at very small voltage sweeping ranges between -0.5 V and +0.5 V. This indicates that stack device, due to the very thin switching layer, requires the current limiting circuit in the practical applications to protect against the severe current overshoots for the compact electronics applications requiring minimal operating power [135, 137].

The lateral device on the other hand showed the self-compliance switching that ensures the device safety against the excessive current for any operating voltage ranges [131, 135-137]. Figure 3.14(b) shows the I-V curve of our lateral ReRAM device, showing a unique resistive switching mode with multiple set and reset voltages in either positive and negative voltage polarities when swept at a very high voltage range of ±210 V and still maintained the self-compliance property which infers to the device's intrinsic self-protection ability against any severe power operating conditions [131, 135-137, 140, 141].

The self-compliance ability makes the device best suited for most of the applications with the scalability in the diverse power operating range, increases the degree of integration, reduce the intricacy of fabrication, suppresses the unwanted interferences in the highly compact memory array architectures due to parasitic capacitance and sneak current etc., and cuts the extra cost and space requirements for the current limiting circuits in all the practical applications [51, 135-137, 142].

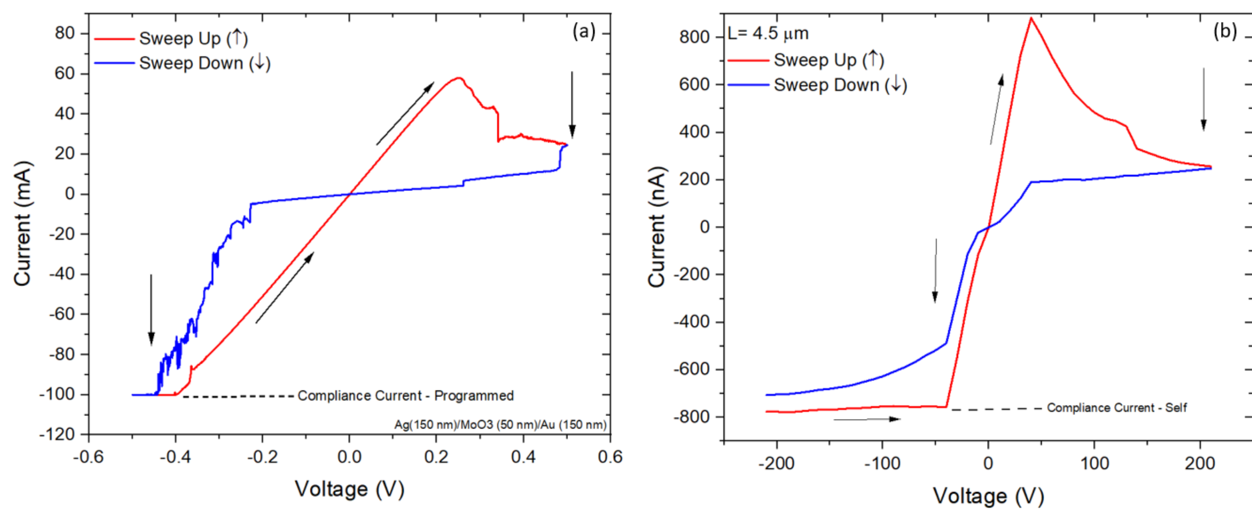

Figure 3.14. Basic I-V curves of ReRAM device. (a) I-V curve of a stack ReRAM device showing the resistive switching reached the compliance level during the set process upon the negative voltage biasing and (b) I-V curve of a lateral ReRAM device showing the self-compliance while the compliance current is configured to 100 mA during the I-V characteristics.

Although the lateral device showed the potential for the practical applications as a nonvolatile resistive switching memory device with its self-protection mechanism, a multilevel switching has not been observed in this configuration due to the lack of compliance current [3, 61, 79, 128]. Self-compliance current range over 105 sweeping cycles is illustrated in the Figure 3.15 and the measurement data is summarized in Table 3.10.

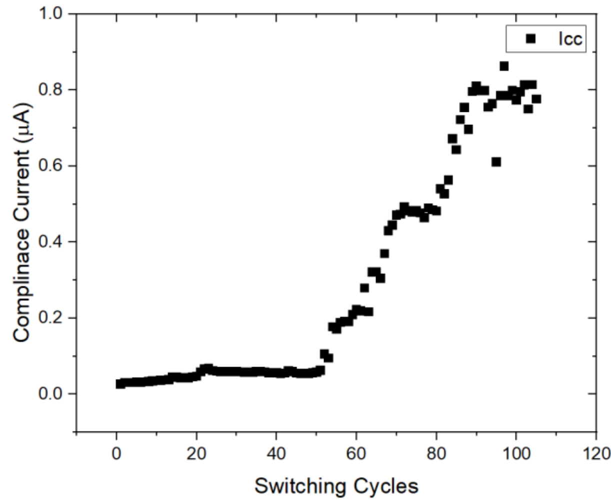

Figure 3.15. Self-compliance current range of a lateral ReRAM device with 4.5 μm channel length over the 105 sweeping cycles.

Table 3.10. Cycle-to-cycle dispersion of the compliance current in a lateral ReRAM device over 105 sweeping cycles.

Total Cycles	**Compliance Current (μA)**
105	0.30 ± 0.30

However, there can be a possibility of invoking the multilevel switching in the fabricated lateral device by adapting other techniques such as by varying the reset voltage to control the resistance levels at the HRS state or by electric-pulse-induced resistance (EPIR) method [61, 79], which requires further device characterization.

3.6.4 Application of the unique resistive switching properties observed in the MoO_3-based lateral ReRAM device architecture

The fabricated MoO_3-based lateral ReRAM device showed unique resistive switching properties e.g., multiple set and reset operations and the overlapping of set and reset operations in the positive voltage regime. These unique switching properties may become useful features for

certain applications but requires an extensive optimization to find out any potential this resistive switching behavior may offer.

3.6.5 Reasoning behind the high voltage stress during the I-V characterization process and possible improvements

I-V characterization for the lateral ReRAM devices was configured at a very high voltage stress i.e., ±210 V to observe the resistive switching behavior due to the large inheritance resistances between the source/drain electrodes in our devices. During the I-V characteristics, the sweeping voltage range was sequentially increased in the subsequent tests and none of the lateral ReRAM devices showed any sign of the forming process or hysteresis as shown in Figure 3.16, until the biasing voltage was set to ±210 V.

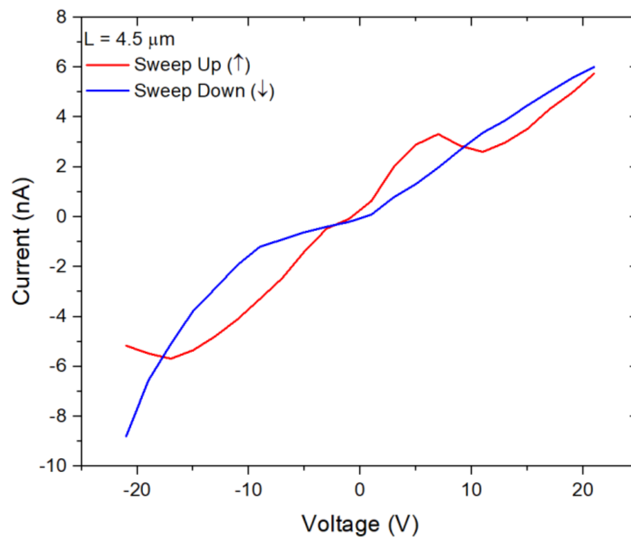

Figure 3.16. I-V sweep of a MoO_3-based lateral ReRAM at low sweeping voltage of ±21 volts.

If the channel length is further reduced to a few nanometers range, the required set/reset voltages could be significantly reduced while preserving large sensing areas at the cost of self-compliance capability [109, 110, 114].

Chapter 4

Conclusion and Future Work

In this research I have investigated the multilevel switching operation in a stack ReRAM device based on MoO_3 switching layer. The device showed the noticeable multilevel switching properties as the compliance current was varied during the set process. Different intermediate LRS resistance levels were achieved for the compliance currents at 20, 40, 60, 80, and 100 mA while no significant change was observed in the HRS other than minor sweeping fluctuations probably caused by the ambient noise. The device realized the 2-bit/cell multilevel switching operation with four distinct LRS resistance levels and one HRS resistance level.

Although the device showed the multiresolution property, it was lagging the adequate read margin, ranging between 4 to 10 during the endurance characteristics consisting of 11 sweeping cycles.

In addition, I have also investigated the switching properties of the novel lateral ReRAM device structure based on MoO_3. The lateral device showed the unique resistive switching properties with multiple set and resets in both positive and negative voltage regimes. Multiple device samples were prepared with different channel lengths to study the resistive switching operation of the lateral structure, however, only one of the samples with 4.5 µm channel length showed the observable hysteresis with the noticeable endurance of up to 105 sweeping cycles at ±210 V. Further investigation is required to determine the plausible applications of the unique switching properties achieved from the lateral ReRAM.

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