The Low-Power Interface Circuits for Energy-Constrained Sensing Applications

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Abstract

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In the emerging applications of the Internet of Things (IoT) − the vision of ubiquitous and pervasive sensing, collecting, and managing data through various sensors, communication technologies, and data analytic techniques, billions of sensors are attached to different objects. The power consumption of the analog front-end circuits in a sensor system is one of the most stringent requirements. The low-power consumption not only can be environment-friendly but also can benefit the customers economically.

This thesis presents a suite of design on the low power interface circuits for the energy-constrained sensing applications. First, an always-on input-biased sub-nanowatt millivolt hysteretic threshold detector for near-zero energy sensing applications is introduced. The threshold detector compares two pA currents generated by current mirrors biased by the mV-range input signal. With the input signal near zero at the standby mode, the threshold detector consumes near-zero energy. Positive feedback is introduced to accelerate the output signal transition and generate the hysteresis to tolerate the noise in the input signal. Designed and fabricated in a standard 65 nm CMOS process, the proposed threshold detector achieved programmable thresholds from 27 to 46.5 mV with energy per switching from 1.9 to 2.4 nJ using four control bits with a 10 Hz input. While the static power consumption is 270 pW measured at the input signal of 0.1 mV with a frequency of 10 Hz.

Second, a resistor-based highly-digital temperature sensor with a SAR-quantization embedded differential low-pass filter is presented for integrated SoC thermal detection. It has three unique features: (1) the use of a differential low-pass RC filter (DLPF) for thermal sensing, which reduces the area; (2) SAR-quantization embedded in the DLPF, which reuses the DLPF capacitor for capacitive digital to analog conversion (CDAC), eliminates the CDAC references, and utilizes the full sensing range for quantization; and (3) a highly-digital circuit architecture, which can be easily implemented using a standard digital design flow and migrated to different processes. The temperature sensor was fabricated in a 65nm CMOS technology occupying 8400 μm^2 silicon area. It achieves 0.38 °C resolution at room temperature. After a 2-point calibration, the sensor achieves a 3σ inaccuracy of ±1.2 °C from -30 to 100 °C. It consumes 35.3 μW power from a 1.1 V supply. With a 2.5 μs conversion time, the sensor achieves an 88 pJ/Conversion energy efficiency, which yields a 12.7 pJ$\cdot$K^2 resolution figure-of-merit (FoM).

Finally, we move on to another interface circuit, analog-to-digital converter (ADC). An energy-efficient, area-compact successive-approximation-register (SAR) ADC based on passive charge sharing is introduced. For each bit decision, a bit reference capacitor with capacitance β times larger than that of the bit weight capacitor and precharged to the reference level is introduced to replace the precise reference source. Closed-form analytic expressions of ADC transfer functions are derived based on charge conservation and validated by behavioral and schematic simulations. Based on the derived results, and using the bitwise passive charge sharing technique, an 11-bit segmented SAR ADC that comprises a 5-bit coarse ADC and a 12-bit fine ADC has been designed and fabricated in a 65 nm CMOS technology, occupying 0.076 mm^2. The fabricated ADC has been measured to achieve a peak SNDR of 60.6 dB and SFDR of 72 dB, and to dissipate 240 μW under 1.2 V supply at 25 MS/s, including 70 μW used by on-chip reference charge reservoir drivers, leading to a Figure of Merit (FoM) of 11.8 fJ/conversion-step at the input frequency of 2.43 MHz.

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DEDICATION

to my family

Chapter 1

INTRODUCTION

1.1 Overview

The sensor-based application is ubiquitous. Example applications can be in domestic, medical, and environmental monitorings. An optical smoke detector uses a photocell, which is an electronic light detector that generates electricity when light falls on it, to detect the smoke [2]. A potential fire disaster can be averted. A pacemaker uses electrodes to detector a patient's heart's electrical activity and then monitor and control the patient's heart to beat at a normal rate [3]. A geophone uses a wire coil that moving within a magnetic field to convert ground movement (velocity) into voltage [4]. It plays a vital role in intruder detection and perimeter security applications. Irrespective of different applications, the sensor-based applications resemble some commonalities. A generic, simplified diagram of a sensor system is shown in Fig. 1.1. Basically, a sensor system utilizes a transducer to translate the changes in a physical condition such as temperature, pressure, and acoustic to continual electrical signals that the electrical devices can recognize. As an interface circuit to bridge the physical world to the electrical devices, a transducer can not only sense the physical changes but also output the translated electrical signals. The translated continual electrical signal is usually small in amplitude (μV) and noisy. It is then filtered and amplified by the analog front-end before digitizing. The digitized signal is sent for the back-end signal processing in the digital domain. The interface circuit that converts an analog signal to a digital signal is an analog-to-digital converter (ADC).

ADC is an essential block to convert the real world analog signal to its digital representation. The advances in ADC is one of the keys to the success of the electronic systems as the information is stored, processed in the digital domain in today's electronic devices. There

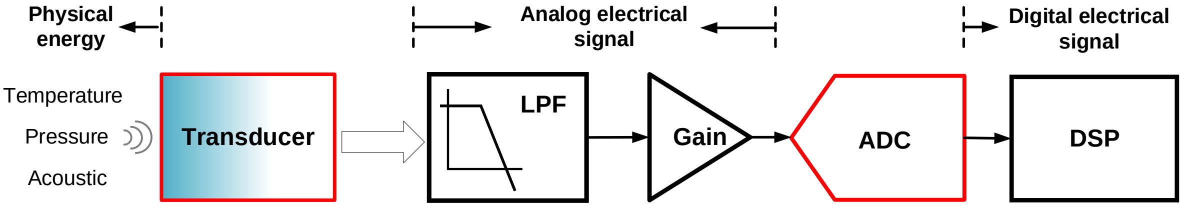


Figure 1.1: A diagram of a general sensor system.

are three metrics to evaluate the performance of an ADC: resolution (number of bits), speed (sampling rate) and power consumption. Per different applications, different resolution and speed are required. In all the application scenarios, minimum power consumption is preferred. Figure 1.2 shows the required resolution of real world signal versus its bandwidth in different applications [5]. In a sensor system, the sampling rate of an ADC is usually less than tens of MHz, this is due to the sensed signal is low in frequency. While for the communications and testing instruments, the sampling rate can be as high as tens of GHz.

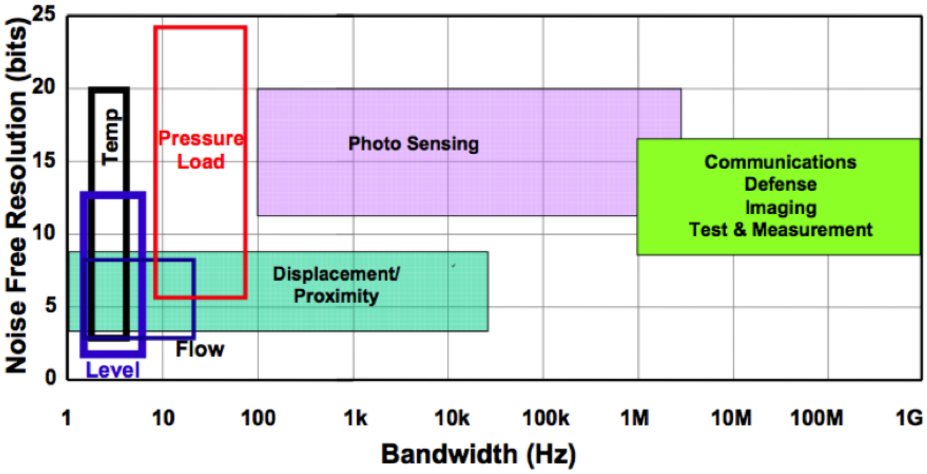


Figure 1.2: The real world signal resolution versus bandwidth in different applications.

1.2 The Power Constraints for Energy-Constrained Sensing Applications

For the battery powered sensor systems, the power consumption is a stringent specification. It can be optimized from 1) block-to-system level hardware design; 2) communication capacity and scalability between sensor nodes and gateway sensor node and; 3) signal processing. This dissertation investigates energy-efficient hardware design from block level to system architecture.

For example, in the application of unattended ground sensor (UGS) network, the sensed signals are low in amplitude (μV), noisy and sparse. State of the art sensors use active devices to continuously and actively monitor the environment and detect the external trigger. The sensors have no prior knowledge of the presence of an event. The always-on front-end active devices and the back-end radio-frequency (RF) communication links and microprocessor with high frequency await infrequent external triggers drain the charge of the battery quickly. Thus, this operation shortens the lifetime of the sensor to less than one month.

In order to extend the lifetime of the sensor nodes, event-driven sensors are preferable. Figure 1.3 shows an event-driven sensing system for UGS application. It includes a front-end stage, which is comprised of a signal collection block, amplification and filtering block, and a threshold detector circuit for event-driven detection, and a back-end stage that consists of RF communication link and a microprocessor for remote signal processing. Geophone continuously senses the acoustic and seismic wave to convert them to electrical signals, then these sensed electrical signals are amplified and noise filtered to compare with the pre-defined threshold voltage. If the amplified signals are larger than the threshold voltage, the comparator outputs digital “1” to wake up the back-end stages for remote signal processing. Otherwise, the back-end stages are in low power sleep mode. Compared with the always-on sensor, the event-driven sensor reduces the “on” time of the power consuming back-end circuits. Therefore, it can increase the sensor lifetime dramatically.

This thesis does not design the sensor front-end circuits and the ADCs for a *typical* sensing application. It focuses on the exploration of the low power techniques of the interface circuits in a sensor system targetted for *different* sensing applications. Section 1.3 lists these interface circuits that are presented in the following chapters in details.

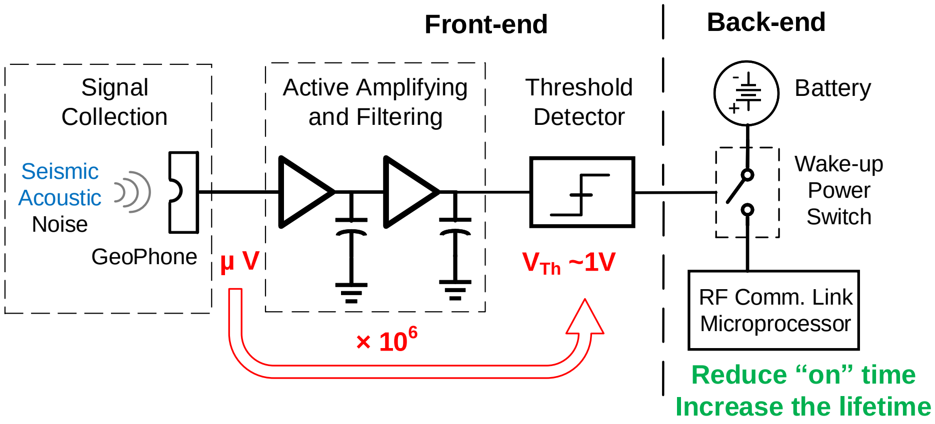


Figure 1.3: A diagram of an event-driven sensing system in unattended ground sensing (UGS) network.

1.3 *Thesis Organization*

There are five remaining chapters in this thesis, organized as follows.

Chapter 2 presents an always-on input-biased nanowatt millivolt-threshold hysteretic threshold detector for event-driven sensing applications. The threshold detector compares two pA currents generated by current mirrors biased by the mV-range input signal. With the input signal near zero at the standby mode, the threshold detector consumes near-zero energy. Positive feedback is introduced to accelerate the output signal transition and generate the hysteresis to tolerate the noise in the input signal. Simulation results in 9HP BiCMOS and measurement results in 65nm CMOS are both presented in this chapter.

Chapter 3 describes a resistor-based highly-digital thermal sensor for integrated thermal detection. It introduced a new sensing element – differential low pass filter (DLPF), to decrease the capacitance value in the sensing circuit, thus reducing both area and power consumption of the thermal sensor. The readout circuit is a successive-approximation-register

(SAR) ADC. The capacitive digital-to-analog converter (CDAC) in the SAR ADC is embedded in the DLPF, which can eliminate the CDAC reference circuits and utilize the whole dynamic range of the ADC. A 65nm CMOS prototype was fabricated and measurement results are described in this chapter.

Chapter 4 provides the analysis of bitwise and sample-wise switched passive charge sharing for SAR ADC. For each bit decision, a bit reference capacitor with capacitance β times that of the bit weight capacitor and precharged to the reference level was introduced to replace the precise reference source. Closed-form analytic expressions of ADC transfer functions are derived based on charge conservation and validated by behavioral and schematic simulations. Two elegant results for SAR ADCs with bitwise switched reference charge reservoirs (BS-RCRs) were concluded. First, a binary-weighted SAR ADC implemented with BS-RCRs is transformed into a sub-radix-2 ADC. Second, the reference error caused by finite reservoir capacitance appears in the form of bit weight error. This error is input independent and thus can be digitally corrected. However, the reference error with sample-wise switched reference charge reservoir (SS-RCR) is input dependent. A case study of an 11-bit 100MS/s SAR ADC in 65nm CMOS is presented.

Chapter 5 presents the theoretical analysis, design, and implementation of passive charge sharing based segmented SAR ADC. Closed-form analytic expressions of the reference error were derived and validated by behavioral modeling. A prototype 65nm design was measured with an energy efficiency of 11.8fJ/conversion-step that including the power consumption of on-chip reference drivers.

Chapter 6 concludes the thesis and provides recommendations for the future work.

Chapter 2

AN ALWAYS-ON INPUT-BIASED NANOWATT MILLIVOLT-THRESHOLD HYSTERETIC CURRENT-BASED THRESHOLD DETECTOR

2.1 Background and Challenges

An event-driven sensor system can extend the lifetime of the sensor by reducing the “on” time of the back-end stages as can be seen from Fig. 1.3. However, there is a big gap between the sensed signal and the threshold voltage (where the threshold voltage is the reference voltage to which the comparator is compared, do not be confused with the threshold voltage of a transistor) of the state of the art detector. The active amplifier and filters are often used to bridge this gap. The always-on high gain amplifier with a gain of 120dB and threshold detector contributes considerable power consumption to the event-driven sensor. To extend the lifetime of the sensor further, the power consumption of the front-end always-on circuits should be as low as possible. The proposed architecture of an event-driven UGS system is shown in Fig. 2.1, with passive amplification and near-zero energy, low threshold comparator replacing the active amplifier and high threshold detector in Fig. 1.3, the front-end always-on circuits consumes less than 10 nW power without event present. Thus, the proposed architecture can extend the lifetime of the sensor from one month to more than tens of months. The research of this work focuses on design low-power, low-threshold comparator.

The always-on comparator design confronts several challenges. Firstly, as an always-on component, its power consumption should be as low as possible. Nano-watt design is preferred. Secondly, the threshold voltage of the comparator should be as low as possible to reduce the passive gain amplification. The comparator output should be at the level of a power supply of the digital signal processing circuit, which is typically 1.2 V in a 65nm

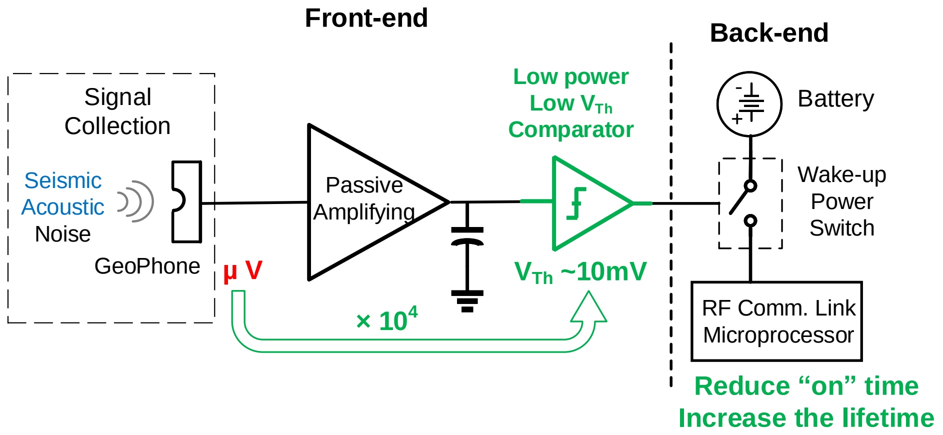


Figure 2.1: The proposed event-driven sensing architecture.

CMOS process. Thirdly, the hysteresis feature is required to avoid noise disturbing and constant switching activities. Often, the sensed signal has low frequencies in nature and high-frequency noise shall be ignored. Lastly, the design should be area efficient.

The widely used low-power comparators are dynamic latch-based. In 65 nm CMOS, to bring the power down to the range of sub-nW to tens of nW requires the use of reduced supply voltages [6, 7]. Furthermore, the dynamic comparators require a clock, which may not exist in the intended application systems, and the clock generation circuit itself is more complex and consumes much more power than the comparator itself. A line of early work has explored current comparators with hysteresis [8, 9, 10, 11]. These comparators fail to accept small-amplitude inputs and also require proper DC biasing, which consumes static power during standby mode.

2.2 Current-based Comparator with Hysteresis

In this section, a current comparator with bistable regions and the hysteresis behavior is presented. First, two branch currents are introduced for the current comparator. The characteristic of these two branch currents controlled by the input voltage is the foundation of

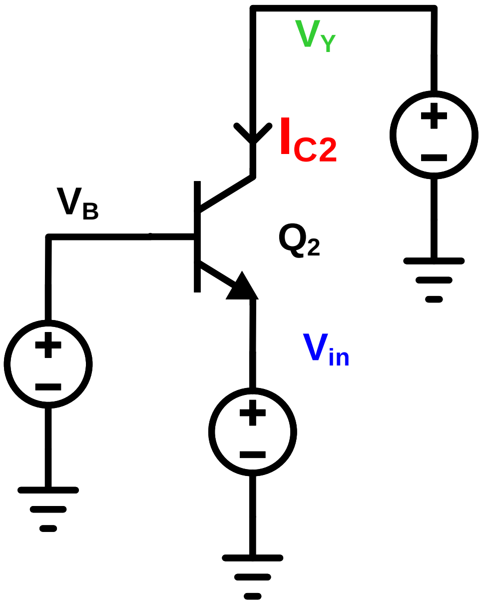


Figure 2.2: A bipolar transistor biased with independent voltage sources.

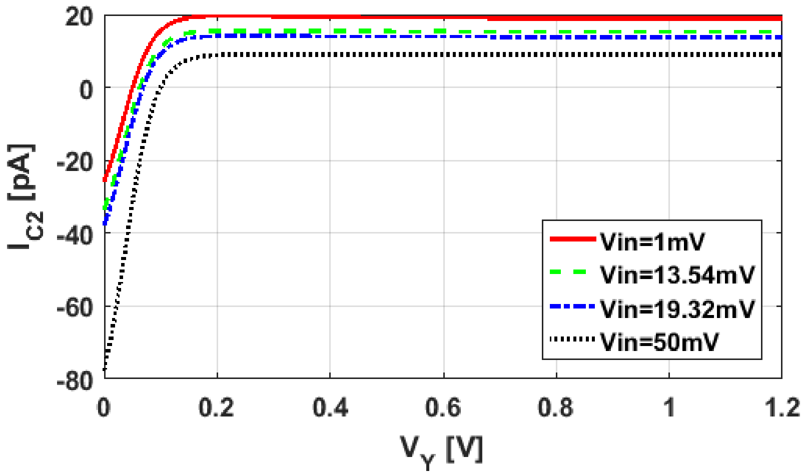


Figure 2.3: The I-V characteristic of the bipolar transistor shown in Fig. 2.2.

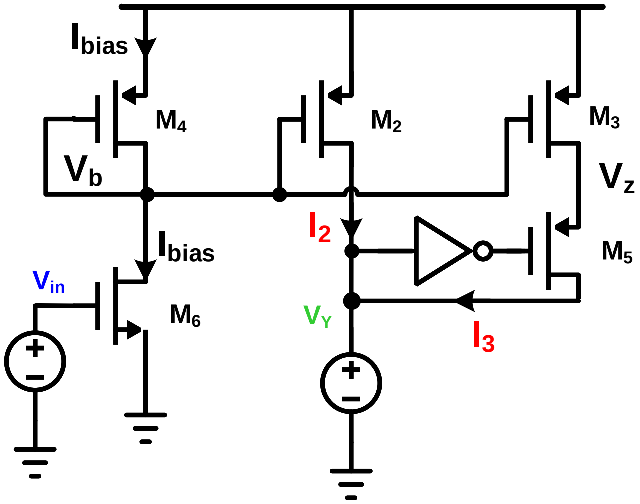


Figure 2.4: The circuit based on the PMOS current mirror in the deep subthreshold region.

the current comparator. Then, a current comparator based on these two branch currents is presented, focusing on the definition of the trip points and the stable regions.

2.2.1 I-V Characteristic of a Bipolar Transistor

The schematic of a bipolar transistor biased with independent voltage sources is shown in Fig. 2.2. Assume that the bias voltage at base V_B is fixed around 450 mV, the emitter connects to V_{in}, which is in the range smaller than 100 mV. The collector voltage V_Y varies from 0 to VDD (1.2 V). Then we obtain the current I_{C2} versus V_Y at different values of V_{in} as shown in Fig. 2.3. When $V_{CE} = V_Y - V_{in} < 0$, $I_{C2} < 0$. When $V_{CE} > 0$, the current increases exponentially as V_Y increases, and then saturated when $V_{CE} > 3V_T$, here V_T is the thermal voltage. As V_{in} increases from 1 mV to 50 mV, the current I_{C2} decreases as shown in Fig. 2.3.

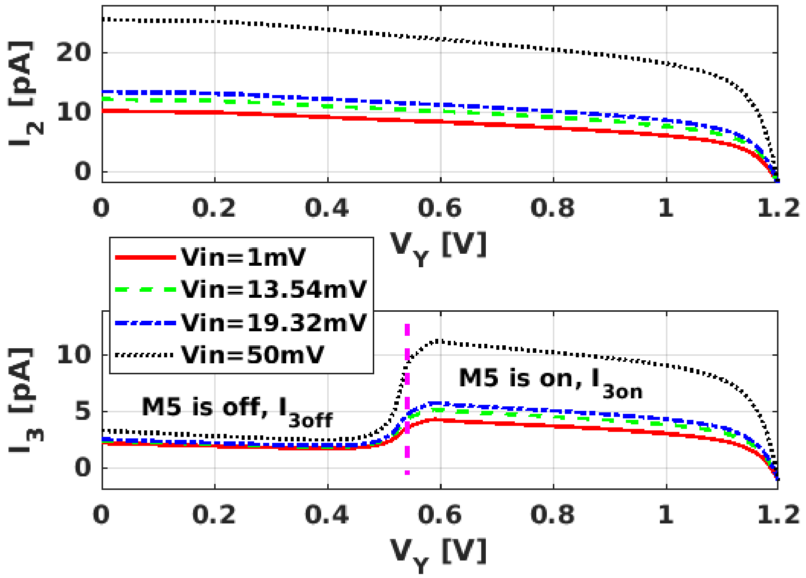


Figure 2.5: The I-V characteristic of the PMOS current mirror with a positive feedback shown in Fig. 2.4.

2.2.2 I-V Characteristic of a PMOS Current Mirror with a Positive Feedback

The schematic of a PMOS current mirror with a positive feedback is shown in Fig. 2.4, in which V_{in} and V_Y are the voltage sources same as in Fig. 2.2. I_2 and I_3 are the currents flowing through M_2 and M_3, respectively. Since V_{in} is much smaller than the threshold voltage of M_6, all the MOSFETs in the current mirror work in the deep subthreshold region. Similarly, V_Y is swept from 0 to VDD (1.2V), we can obtain currents I_2 and I_3 versus V_Y at different values of V_{in} as shown in Fig. 2.5. When $|V_{DS}|$ of M_2 decreases, current I_2 decreases too, as shown in the upper plot. An interesting characteristic of M_3 is that when V_Y is small, M_5 is off, V_Z floats to VDD. Current I_3 is the leakage current when M_5 is off. As V_Y increases to turn on M_5, current I_3 has the same trend as I_2. Current I_3 in the current mirror plays a vital role to introduce hysteresis in the current comparator. When V_{in} increases from 1 mV to 50 mV, both currents I_2 and I_3 increase.

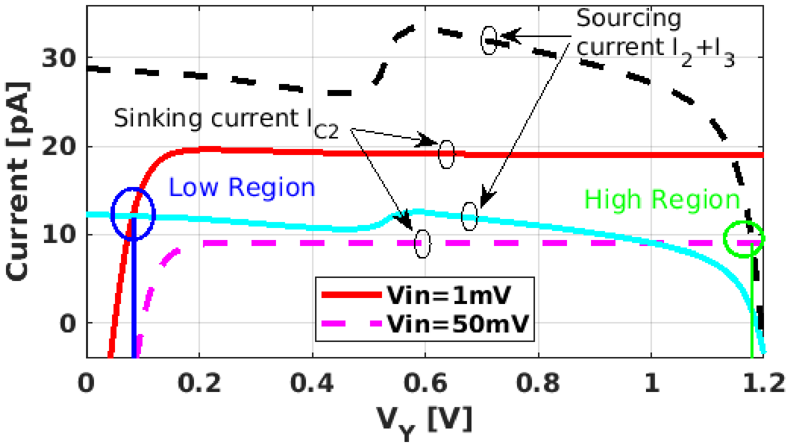


Figure 2.6: The definition of the stable regions in the current comparator.

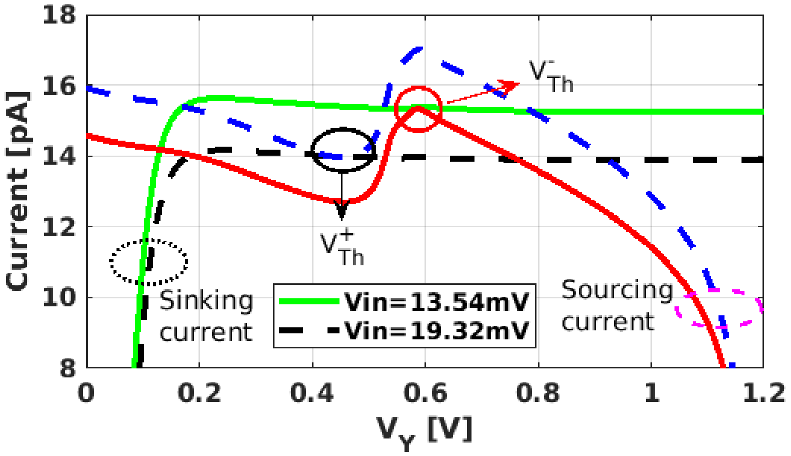


Figure 2.7: The definition of the trip points in the current comparator.

2.2.3 Current Comparator

If we combine the above two circuits and let them join at V_Y, current $I_2 + I_3$ serves as the sourcing current, and I_{C2} serves as the sinking current to net V_Y. This forms a current comparator with hysteresis. It works as follows: Start from a very small V_{in}, i.e., $V_{in} = 1mV$. In this case, there is only one intersection point of the sourcing and sinking currents. No matter where V_Y starts, it goes to a stable point where the sourcing and sinking current intersects, noted by an elliptic circle on the left of the two solid curves in Fig. 2.6 as *the low stable region, noted as* ^{l}. As V_{in} increases, sourcing current $I_2 + I_3$ increases, while sinking current I_{C2} decreases. When V_{in} increases so that I_2+I_3 and I_{C2} have exactly two intersection points, and after that the two currents have only one intersection point, the value of V_{in} at this time is *the positive trip point* V_{Th}^+, denoted as in Fig. 2.7. As V_{in} increases further, there is only one intersection point of $I_2 + I_3$ and I_{C2}, which forces the comparator to enter *the high stable region, noted as* ^{h} shown in Fig. 2.6, noted by the intersection point of two dashed curves. But when V_{in} decreases from high to low, to some value of V_{in} that there are only two intersection points of the sourcing and sinking currents, the value of V_{in} at this time is called *the negative trip point* V_{Th}^-. When V_{in} decreases further, the current comparator can only enter to the low region. When $V_{Th}^- < V_{in} < V_{Th}^+$, the sourcing and sinking currents have three intersection points, in which the middle intersection point is not a stable point. The comparator can either enters to the low or the high stable region depending on the initial value of V_Y.

2.3 Proposed Hysteretic Comparator

Figure 2.8 shows the proposed input biased mV-threshold comparator with hysteresis. PMOS transistors M_1 to M_4 constitute a current mirror with the current generated by input-biased NMOS transistor M_6. With this, the static power consumption is near zero when the input signal is near zero. The MOSFETs in the current mirror work in the deep sub-threshold region. The sourcing currents I_2 and I_3 are exponentially proportional to V_{in} through the PMOS current mirror. Bipolar transistors Q1 and Q2 form a Widlar current mirror, with the resistor replaced by the input voltage source. The Q2 emitter is connected to the input source. The sinking current I_{C2} is inversely exponentially proportional to V_{in} through the Widlar current mirror. The sinking current is at the range of pico-ampere. Thus transistors Q1 and Q2 work in the cutoff region. The input resistance of this comparator is at the range of GΩ.

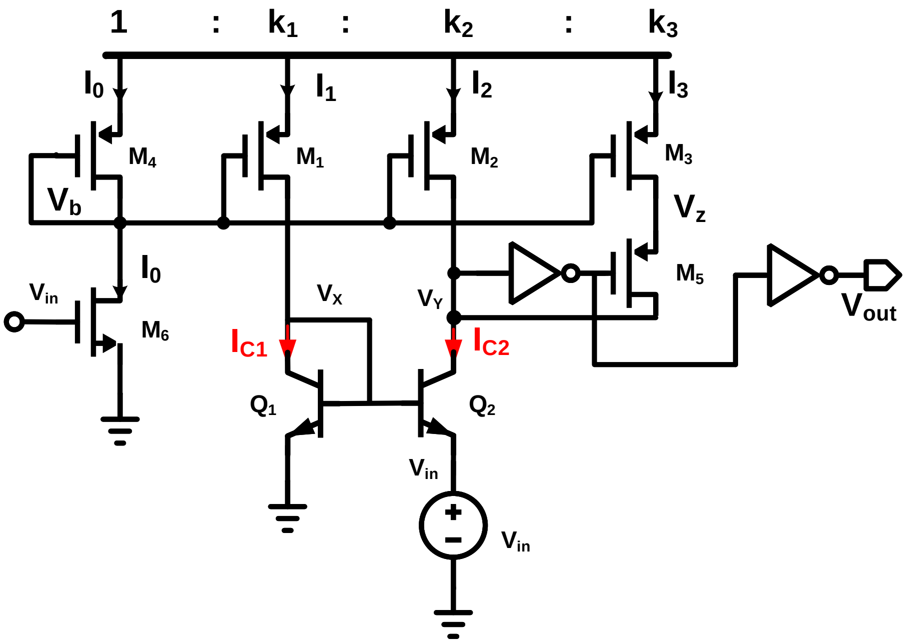


Figure 2.8: Proposed low-threshold low-power hysteresis comparator.

Hysteresis is provided by the positive feedback constructed by M$_3$, M$_5$, and an inverter. The hysteresis range is defined as $V_{Th}^{+} - V_{Th}^{-}$, which is controlled by the positive feedback current I_3. The comparator operates as follows: assume that input voltage V_{in} increases below from V_{Th}^{+}, sourcing current I_2 is increasing while sinking current I_{C2} is decreasing. Thus, V_Y increases to high gradually. As long as V_Y exceeds the threshold voltage of the NMOS transistor in the inverter, M$_5$ is on. This increases the sourcing current by $I_{3on} - I_{3off}$, which forces V_Y to the high stable region. When the input signal V_{in} decreases towards to negative trip point V_{Th}^{-}, sinking current I_{C2} through Q2 overweights sourcing current $I_2 + I_{3on}$. As long as V_Y decreases to lower than $|V_{ThP}|$ of the PMOS transistor in the inverter, M$_5$ is off, which decreases the sourcing current from $I_2 + I_{3on}$ to $I_2 + I_{3off}$. This forces V_Y to the low stable region.

2.4 Analysis of The DC Characteristics

2.4.1 Subthreshold MOSFET Model

The channel current of a MOSFET in the subthreshold region can be expressed as in (2.1)

$$\begin{aligned} I_{DS} &= 2\zeta\mu_e C_{ox}\frac{W}{L_e}V_T^2\exp(\frac{V_{GS}-V_{Th0}}{\zeta V_T})[1-\exp(\frac{-V_{DS}}{V_T})] \\ &= I_0\frac{W}{L_e}\exp\frac{V_{GS}}{\zeta V_T}[1-\exp(\frac{-V_{DS}}{V_T})] \end{aligned} \tag{2.1}$$

where $I_0 = 2\zeta\mu_e C_{ox}V_T^2\exp(-V_{Th0}/(\zeta V_T))$ is the technology current, and ζ is the subthreshold slope factor, and usually $1 < \zeta < 1.5$. Parameter μ_e is the effective carrier mobility. Parameter V_T is the thermal voltage (26 mV in the room temperature) and V_{Th0} is the MOSFET threshold voltage with the source-bulk zero biased.

We define $I_{G0} = I_0\exp(|V_{GS}|/\zeta V_T)$ as the *gate-controlled technology current*, which degenerates to the technology current when $V_{GS} = 0$. Figure 2.9 plots I_{G0} verse $|V_{DS}|$ for 65nm-process PMOS transistors with $|V_{Th0}| = 409mV$ and $|V_{GS}| = 113mV$ and $|V_{GS}| = 91mV$, respectively. We can see that the value of I_{G0} varies about two times during the entire V_{DS} region. This is due to the weakly linear V_{DS} dependence of ζ amplified by the $exp((|V_{GS}|-|V_{Th0}|)/\zeta V_T)$ term; i.e., a 10% change in ζ leads to an about 200%-300% change in I_{G0}. This is in contrast to the transistors working in the linear and saturation regions where the technology current is treated as a process-dependent parameter; i.e., not dependent on V_{DS} [12].

2.4.2 Input-Biased MOS Current Mirror

Now consider the input-biased MOS current mirror as shown in Figure 2.10. Transistors M_1 to M_4, and M_6 are all working in the subthreshold region. The bias current can be expressed as in (2.2) through M_6, and as in (2.3) through M_4

$$I_{bias} = I_{0N}(\frac{W}{L})_{M6}\exp(\frac{V_{in}}{\zeta_N V_T}) \tag{2.2}$$

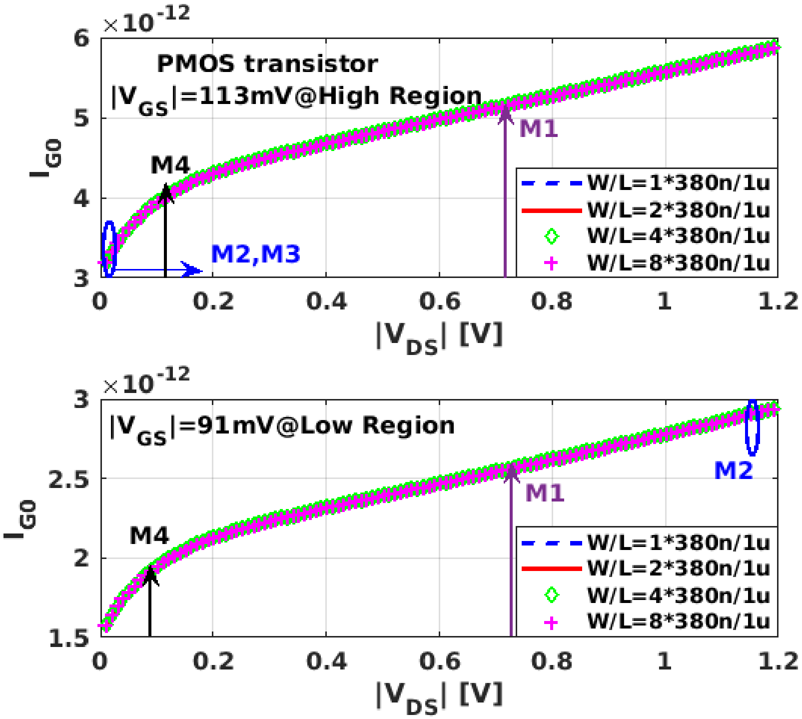


Figure 2.9: Normalized gate controlled channel current versus $|V_{DS}|$ of different size PMOS transistors at (a) $|V_{GS}| = 113mV$ and (b) $|V_{GS}| = 91mV$.

$$\begin{aligned} I_{bias} &= I_{0P,4}(\frac{W}{L})_{M4}\exp(\frac{V_{DD}-V_b}{\zeta_{P,4}V_T})[1-\exp\frac{-(V_{DD}-V_b)}{V_T}] \\ &\approx I_{0P,4}(\frac{W}{L})_{M4}\exp(\frac{V_{DD}-V_b}{\zeta_{P,4}V_T}) \end{aligned} \tag{2.3}$$

where I_{0N} and $I_{0P,4}$ are the technology currents, ζ_N and $\zeta_{P,4}$ are the slope factors, of NMOS M_6 and PMOS M_4, respectively. Both M_4 and M_6 have the same size. The aspect ratio of PMOS transistors M_4, M_1, M_2 and M_3 in the current mirror is $1 : k_1 : k_2 : k_3$ as noted in Fig. 2.10. So the mirrored currents through M_1, M_2, and M_3 can be expressed as (2.4), (2.5), and (2.6), respectively.

$$I_1 = k_1\chi_1[I_{0N}(\frac{W}{L})_{M6}\exp(\frac{V_{in}}{\zeta_N V_T})] \tag{2.4}$$

$$I_2 = k_2\chi_2[I_{0N}(\frac{W}{L})_{M6}\exp(\frac{V_{in}}{\zeta_N V_T})][1-\exp\frac{-(V_{DD}-V_Y)}{V_T}] \tag{2.5}$$

$$I_3 = k_3\chi_3[I_{0N}(\frac{W}{L})_{M6}\exp(\frac{V_{in}}{\zeta_N V_T})][1-\exp\frac{-(V_{DD}-V_Z)}{V_T}] \tag{2.6}$$

where

$$\chi_i = \frac{I_{G0,i}}{I_{G0,4}} = \frac{I_{0P,i}}{I_{0P,4}}\exp[\frac{V_{DD}-V_b}{V_T}(\frac{1}{\zeta_{P,i}}-\frac{1}{\zeta_{P,4}})] \tag{2.7}$$

Factor $\chi_i, i = 1,2,3$ are introduced to take into account the mismatches of the gate-controlled technology currents $I_{G0,i}, i = 1,2,3$ of transistors M_1, M_2, and M_3 from M_4 due to their varying V_{DS}. They can be extracted from Figure 2.9.

No matter M_5 is on or off, V_Z is close to or near to VDD. So even M_5 is off, the leakage current through M_3 also matters. Here we model the current through M_3 when M_5 is off as I_{3off}

$$I_{3off} = \alpha I_3 \tag{2.8}$$

where α is the leakage factor of M_3.

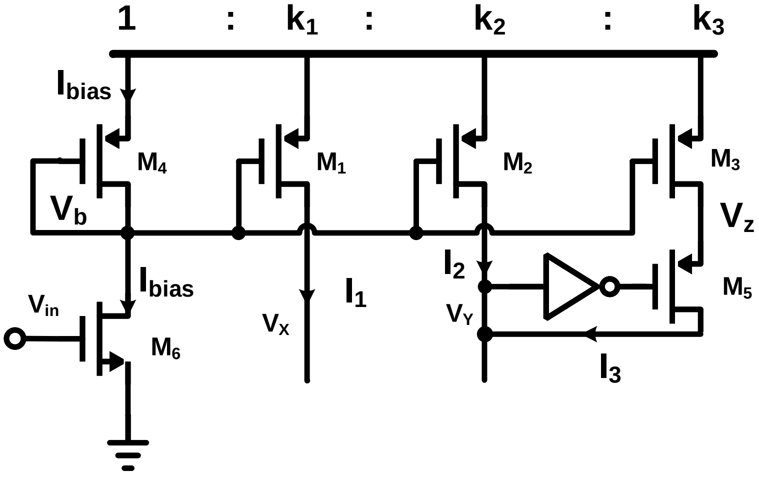


Figure 2.10: A PMOS current mirror with an input-biased NMOS current generator.

2.4.3 Input-Biased Bipolar Current Mirror

Now consider the input-biased bipolar current mirror as shown in Figure 2.11. It is a classical Widlar current mirror with the resistor replaced by the input source. The sizes of transistors Q1 and Q2 are chosen to be the same. Apply the KVL at the base and the emitter of Q1 and Q2, we have

$$V_{in} = V_{BE1} - V_{BE2} \tag{2.9}$$

The collector current I_{C1} of Q1 can be expressed as

$$I_{C1} = I_S \exp(\frac{V_{BE1}}{V_T}) \tag{2.10}$$

where I_S is the saturation current. While Q2 can be in the cutoff region or in the reverse active region depending on the state of V_Y,

$$I_{C2} = I_S \exp(\frac{V_{BE2}}{V_T}) - I_S(1 + \frac{1}{\beta_R}) \exp(\frac{V_{BC2}}{V_T}) \tag{2.11}$$

Applying the KCL at Q1 collector, we have

$$I_{C1} = \frac{\beta_1}{\beta_1 + 1}(I_1 - \frac{I_{C2}}{\beta_2}) \tag{2.12}$$

where β_1 is the current gain of Q1, and β_2 is the current gain of Q2. Applying the KCL at Q2 collector, we have

$$I_{C2} = I_2 + I_3 \tag{2.13}$$

Substitute (2.10) to (2.13) into (2.9), we obtain V_{in} as a function of I_1, I_2, and I_3

$$V_{in} = V_T ln[\frac{\frac{\beta_1}{\beta_1+1}(I_1 - \frac{I_2+I_3}{\beta_2})}{I_2 + I_3 + (1 + \frac{1}{\beta_R}) \exp(\frac{V_{BC2}}{V_T})}] \tag{2.14}$$

2.4.4 DC Trip Points

The proposed comparator has two trip points. One is the positive trip point V_{Th}^{+}, the value of V_{in} when comparator outputs from "0" to "1". The positive feedback is from off to on.

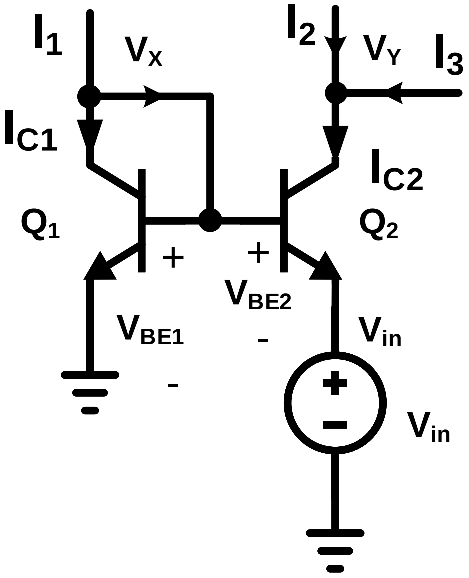


Figure 2.11: An input-biased bipolar current mirror.

At the positive trip point, V_Y is about half VDD, which is close to V_X thus $\chi_1 \approx \chi_2 \approx \chi_3$. Equation (2.14) can be simplified to

$$V_{Th}^{+} = V_T \ln[\frac{\beta_1}{\beta_1 + 1}(\frac{k_1}{k_2 + \alpha k_3} - \frac{1}{\beta_2})] \tag{2.15}$$

The other is the negative trip point V_{Th}^{-}, the value of V_{in} when comparator outputs from "1" to "0". The positive feedback is from on to off. From (2.14), we have

$$V_{Th}^{-} = V_T ln[\frac{\beta_1}{\beta_1 + 1}(\frac{k_1}{k_2 + k_3} - \frac{1}{\beta_2})] \tag{2.16}$$

The beauty of (2.15) and (2.16) is that the positive and negative trip points can be controlled by k_1, k_2, k_3, the aspect ratios of PMOS transistors in the current mirror.

2.4.5 DC Transfer Curves

The proposed comparator has two stable regions. One is when $V_{in} > V_{Th}^{+}$, the comparator stays at the high region. In the high region, variables V_X, V_Y and χ have the upper note ^{h} to denote the high region. The other is the low region when $V_{in} < V_{Th}^{-}$. In the low region, upper ^{l} is used to denote the low region. Now we quantitatively analyze these two stable regions by solving V_Y as a function of V_{in}.

In the high region, V_Y approaches to VDD, the positive feedback is on. Thus, $V_Y = V_Z$, and $\chi_2^h = \chi_3^h = \chi_{2,3}^h$. Substitute (2.4) and (2.10) into (2.12), one can obtain V_X as a function of V_{in} as shown in (2.17) by neglecting the second term in the parenthesis of (2.12).

$$V_X^h = \frac{V_{in}}{\zeta_N} + V_T \ln[\frac{k_1 \chi_1 I_{0N} (W/L)_{M6} \beta_1}{I_S(\beta_1 + 1)}] \tag{2.17}$$

Substitute (2.5), (2.6) and (2.11) into (2.13), V_Y^h as a function of V_{in} and V_X^h can be obtained as shown in (2.18). Here Taylor series expansion of $e^x = 1 + x$ is used when x approaches to 0.

$$V_Y^h = V_{DD} - \frac{\zeta_N V_T I_S}{\chi_{2,3}^h (k_2 + k_3) I_{0N} (W/L)_{M6}} \exp(\frac{\zeta_N V_X^h - (\zeta_N + 1) V_{in}}{\zeta_N V_T}) \tag{2.18}$$

Substitute (2.17) into (2.18) to obtain V_Y^h as a function of V_{in} as in (2.19)

$$V_Y^h = V_{DD} - \frac{\zeta_N V_T k_1 \chi_1 \beta_1}{\chi_{2,3}^h (k_2 + k_3)(\beta_1 + 1)} \exp(\frac{-V_{in}}{V_T}) \tag{2.19}$$

From (2.19), we can see that, as V_{in} increases, the second term approaches to zero, V_Y^h is close to VDD.

In the low region, V_Y approaches to GND, the positive feedback is off. So the leakage current I_{3off} is ignored. From (2.12) to obtain V_X^l as a function of V_{in} as shown in (2.20). Here $I_{C2} = I_2$ is used.

$$V_X^l = \frac{V_{in}}{\zeta_N} + V_T ln[(k_1 \chi_1^l - \frac{k_2 \chi_2^l}{\beta_2}) \frac{I_{0N} (W/L)_{M6}}{I_S} \frac{\beta_1}{\beta_1 + 1}] \tag{2.20}$$

Similarly, according to the KCL at node V_Y, that is (2.13), one can obtain V_Y^l as a function of V_{in} and V_X^l

$$V_Y^l = V_X^l + V_T ln(\frac{1}{\beta_R} + 1) - V_T ln[\exp(\frac{V_X^l - V_{in}}{V_T}) - k_2\chi_2^l \frac{I_{0N}(W/L)_{M6}}{I_S} \exp\frac{V_{in}}{\zeta_N V_T}] \tag{2.21}$$

Substitute (2.20) into (2.21) to obtain V_Y^l as a function of V_{in} as shown in (2.22). Equation (2.22) indicates that V_Y^l is related to V_{in}, and some process dependent constants.

$$V_Y^l = V_T ln(1 + \frac{1}{\beta_R}) - V_T ln[exp(\frac{-V_{in}}{V_T}) - \frac{k_2\chi_2^l}{k_1\chi_1^l - k_2\chi_2^l/\beta_2}\frac{\beta_1 + 1}{\beta_1}] \tag{2.22}$$

2.5 Circuit Design Consideration

2.5.1 MOSFETs in the Deep Subthreshold Region

Biased by the mV-range input signal, the CMOS current generator, and its driven MOS current mirrors are working in the deep subthreshold region with the currents in the range of pA. Inversion coefficient (IC) is a design parameter introduced to represent the degree of MOSFET channel inversion for analog circuit design, which is defined as

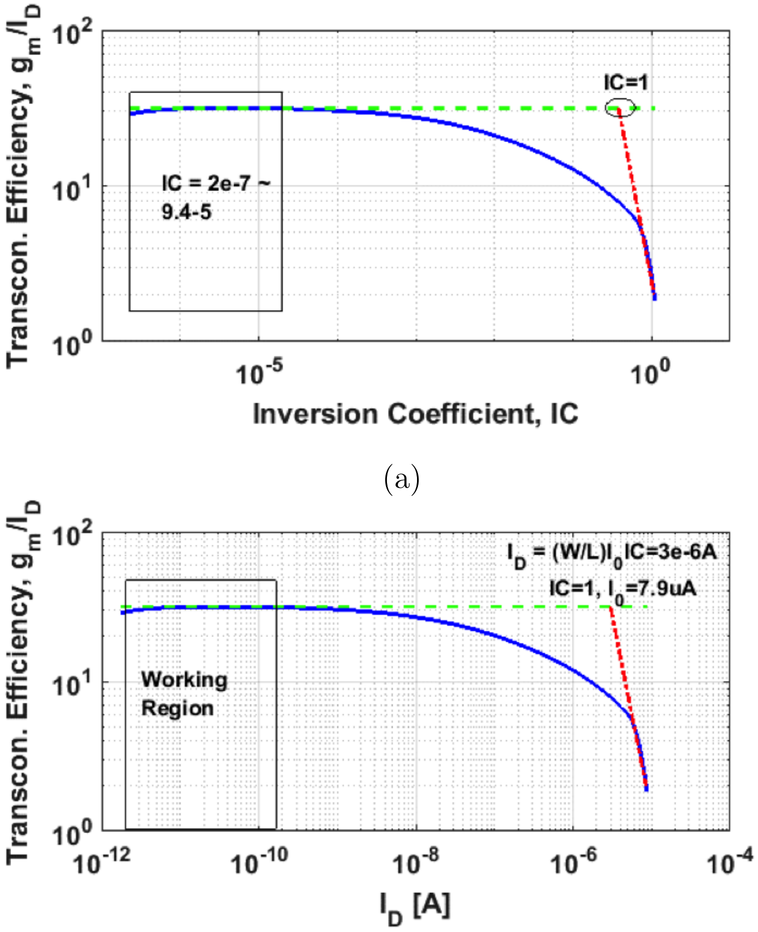
$$IC = \frac{I_D}{\frac{W}{L} I_0} \tag{2.23}$$

where I_D is the drain current, I_0 is the technology current that relates to the subthreshold factor and carrier mobility, and W/L is the aspect ratio. When $IC > 10$, the MOSFET is in the strong inversion region, when $IC = 1$, the MOSFET is in the moderate inversion region, and when $IC < 0.1$, the MOSFET is in the weak inversion region. As illustrated in Figure 2.12 (a), the ICs of MOS transistors in the proposed current mirror are designed to be in the range of 2e-7 to 9.4e-5, which we refer to as in the *deep subthreshold* region, or *deeply weak* inversion region. We note that IC in the deeply weak inversion region is several orders of magnitude smaller than the weak inversion region (IC around 0.1), which has been previously explored for ultra-low power analog design [12].

The transconductance in the subthreshold region is

$$g_m \approx \frac{I_D}{\zeta V_T} \tag{2.24}$$

As shown in Figure 2.12 (b), the transconductance efficiency g_m/I_D is much higher in the deep subthreshold region than that in other regions. This leads to higher circuit energy efficiency.



(a)

(b)

Figure 2.12: Transconductance efficiency versus bias operation point.

2.5.2 Process Variation and Mismatch

Unfortunately, MOSFET electrical characteristics in the deep subthreshold region are more subject to process variation and mismatch. Experiments show that the two main sources of mismatch among MOS devices are the transistor threshold voltage (V_{TH}) mismatch and current factor ($\mu C_{ox}\frac{W}{L}$) mismatch that is inversely proportional to the transistor area WL. For the current mirror, the current mismatch can be expressed as

$$(\frac{\sigma(\Delta I_{DS})}{I_{DS}})^2 = \frac{A_\beta^2}{WL} + (\frac{g_m}{I_{DS}})^2 \frac{A_{Vth}^2}{WL} \tag{2.25}$$

where A_β and A_{Vth} are two technology dependent parameters. From Figure 2.12, g_m/I_{DS} is at its maximum in the deep subthreshold region. Since g_m/I_{DS} is in the range of 30 to 40 in the deep subthreshold region, about 10 times bigger than that in the typical weak inversion region (IC=1, $g_m/I_{DS} = 3 - 4$). Thus mirror current mismatch is about 100 times amplification of process mismatch.

We note that the comparator threshold V_{th} is not sensitive to process variation in the first order, except logarithmically to I_1/I_2, the ratio of two currents. Three techniques are used to mitigate the effect of current mismatch. The first is by increasing transistor sizes and carefully matched layout design. The second is to select the ratio of I_1/I_2 to be greater than one. Note that

$$\frac{\Delta V_{th}}{\Delta \frac{I_1}{I_2}} = \frac{1}{\frac{I_1}{I_2}} \Delta \frac{I_1}{I_2} \tag{2.26}$$

the mirror current mismatch is attenuated by $\frac{1}{I_1/I_2}$ to affect the comparator V_{th} variation. Finally, mismatch can be calibrated as being described in Section 2.5.4.

2.5.3 Vertical Bipolar Transistors in CMOS and Bias-Dependent β

The cross-section view of a vertical NPN bipolar transistor realized in a standard CMOS process is illustrated in Figure 2.13. As shown the n+ source/drain doping layer is utilized as the emitter, the p-Well as the base, surrounded by the deep N-well as the collector. Since the N-well and P-well are lightly doped, the base and collector carrier densities are low. This leads to small β_F and β_R. For the 65-nm CMOS process we used, $\beta_F = 4.75$ and $\beta_R = 0.33$.

Another issue of a vertical NPN bipolar transistor is the bias-dependent β effect. In the classical Ebers-Moll model, β is constant. However as noted originally by Gummel and

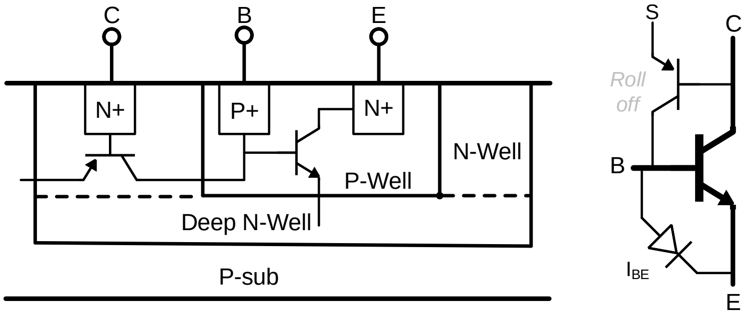


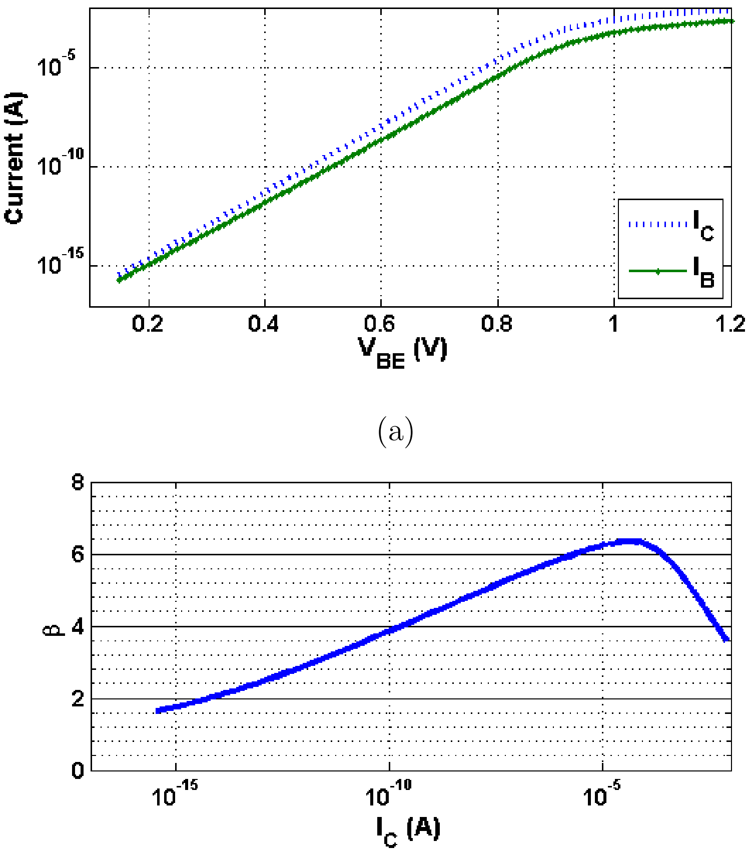
Figure 2.13: Cross-section view of a vertical NPN bipolar transistor in a CMOS process.

Poon [13], there is a parasitic PNP bipolar transistor and a parasitic leakage diode as shown in the equivalent circuit in Figure 2.13. The parasitic PNP transistor leads to the β rolling-off characteristic in the high current forward biased region. The V_{BE} dependent leakage, modeled as a diode, tends to dominate in the small current region. This leads to a smaller effective β.

Techniques have been developed to calibrate β [14] and to increase β [15] in 65nm CMOS at the expense of more silicon area. For this design, to save the silicon area, the smallest available NPN transistor in the CMOS process with size $2\mu \times 2\mu$ is used. The simulated NPN transistor collector current I_C and base current I_B versus bias voltage V_{BE} under $V_{CE} = 1.2V$ are plotted in Figure 2.14 (a). The effective β versus I_C is plotted in Figure 2.14 (b), which shows the bias-dependent β effect. In our design, bipolar transistors are working in the region with β around 3.5, where β is proportional to bias voltage V_{BE} linearly.

2.5.4 Threshold Programmability and Calibration

A simple solution to realize the programmable threshold voltage is presented in Figure 2.15. Programmable binary-weighted current mirrors replaced M_1. By enabling or disabling each branch in the binary current mirror array through digital control codes, the value k_1 varies, and then the threshold voltage varies.



(a)

(b)

Figure 2.14: DC characteristics of a vertical NPN transistor.

The aspect ratio in the current mirror is $1 : k_1 : k_2 : k_3 = 1 : (7+15) : 2 : 1$. By adjusting the aspect ratios, we can achieve a comparator threshold at the range of mV. Furthermore, these ratios could be set by the digital control logic, allowing the comparator threshold – and subsequently the input signal level to be detected – to be easily programmed.

2.6 Measurement Results

The proposed comparator was fabricated in a 1P9M 65-nm CMOS LP technology. Figure 2.16 shows the die micrograph. The active area of one comparator is 16.5 μm × 19.5

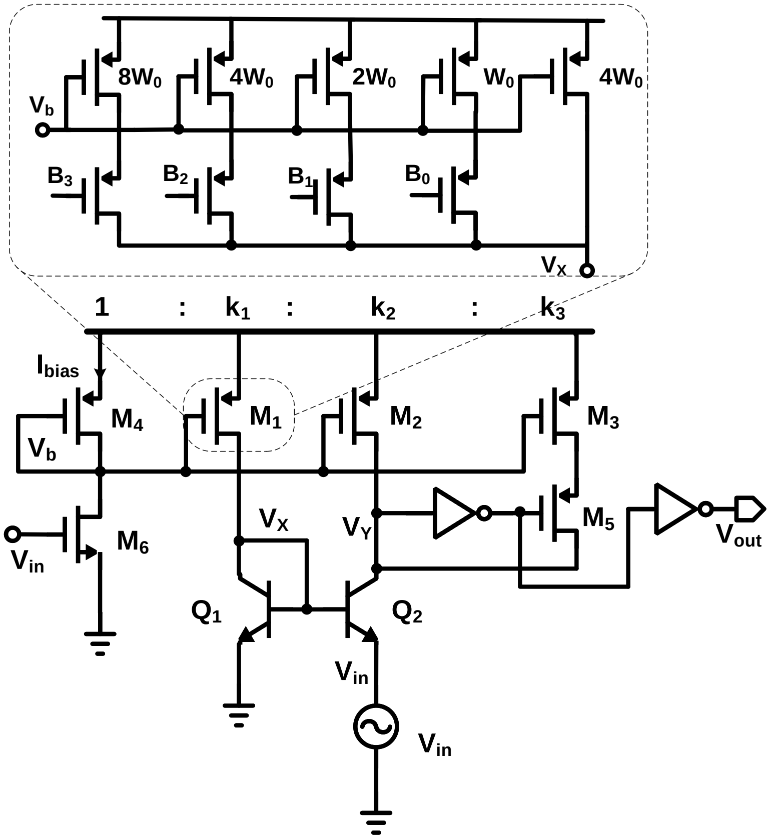


Figure 2.15: Comparator with adjustable thresholds by tuning k_1.

μm, 40% of which is used by the two vertical NPN bipolar transistors. To evaluate the impact of process variation and mismatch, eight comparators are placed in an array on a single die. A serial-to-parallel interface (SPI) is used to configure comparator threshold control bits. The comparator uses only one power supply of 1.2V, which is shared with other on-chip analog blocks without any dedicated power management and level shift circuits.

The DC characteristics of the comparator are measured by a high-precision DAC (MAX544x Evaluation Kit), and monitored by a logic analyzer (Keysight 16800 Series). By configuring the threshold control bits, the comparator thresholds are measured. The results are shown in Fig. 2.17, compared with both theoretical analysis and simulation. The comparator achieved

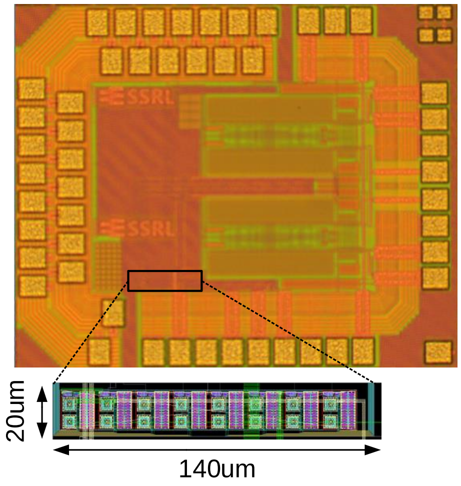


Figure 2.16: Micrograph of the die.

the threshold from 27 mV to 46.5 mV. The result of theoretical analysis considering both the finite β and off-transistor leakage effects matches well to that of simulation and measurement. Ideal analysis with infinite β causes substantial deviation from that with finite β (between 2 to 5).

Figure 2.18 shows the measured thresholds of six comparators from two chips by varying control bits. The standard deviation (1-σ) is approximately 3.0 mV, close to the 3.1 mV from Monte-Carlo simulation.

The dynamic performance of the comparator is measured using an ultra-low-distortion function generator (DS360) and a high-resolution oscilloscope (Keysight DSOX3000). The signal generator provides low-frequency sine waves (0.01 Hz 5 KHz) and on-off modulated signals with 0.1 mV resolution. The input and output of the comparator are fed into the oscilloscope. Figure 2.19 shows the measured comparator output time domain waveforms under control bits 0000 and 1111 along with the waveform of a 1Hz 50 mV sinusoidal input signal. The threshold hysteresis effect can be seen by observing the duty cycle difference between the comparator output high and low periods.

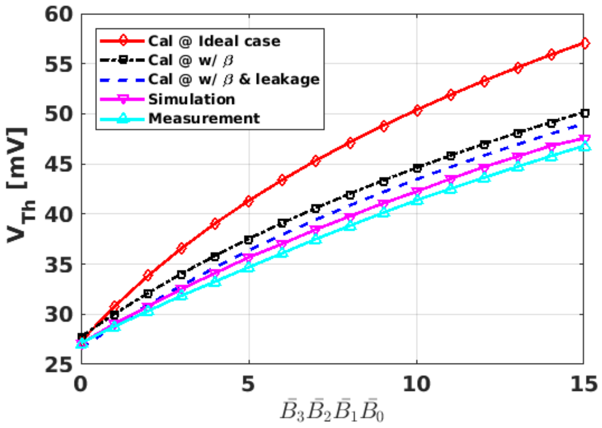


Figure 2.17: Comparator threshold V_{Th} versus control code, from calculation, simulation, to measurement.

The relationships of the measured comparator threshold versus the control code at input signal frequencies of 1 Hz, 10 Hz, and 20 Hz are shown in Figure 2.20. We can see that the worst variation is less than 1.5 mV across all control codes. Figure 2.21 shows the measured comparator threshold and hysteresis expansion as the result of increasing the input signal frequency for several comparators on the same die. We can see that the comparator stops comparison when the input signal frequency approaches 1 KHz. The measured threshold increase with the frequency is consistent with theoretical analysis as and simulation as also shown in Figure 2.21.

The comparator static power consumption is measured to be 270 pW at the 0.1 mV input signal level. The energy consumed per input-threshold detection (switching to 1.2 V output) is measured by applying the periodical stimulus with frequency of 10 Hz. The energy per switching is 1.8 nJ to 2.4 nJ, dependent upon control codes. The switching energy breakdown is approximately 87.9% for the inverter in the positive feedback loop, 5.6% for the output inverter, and 6.5% for the rest of the comparator. With the negligible leakage, the power consumption of the comparator increases linearly with the input signal frequency. Table 2.1 summarizes the comparator design. Table 2.2 compares the comparator performance with

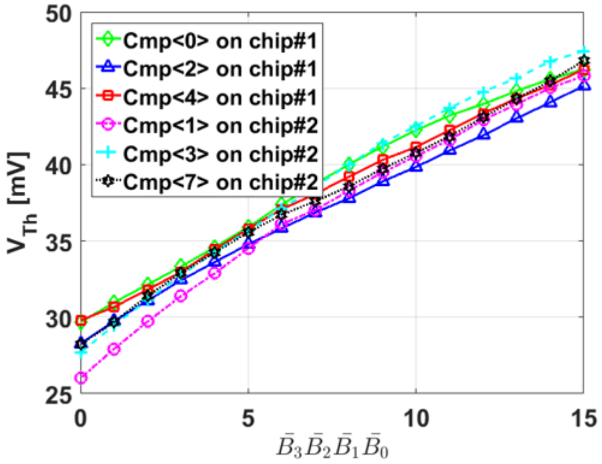


Figure 2.18: Measured V_{Th} versus control code of six comparators on same/different die(s).

that of published of the similar architecture.

2.7 Conlcusion

A programmable mV-threshold, 1.2 V-output hysteretic comparator with sub-nW power consumption was presented in this chapter. Biased by the input signal, the power consumption of the comparator is near zero in the sleep mode. A comprehensive analysis of circuit characteristics working in the deep subthreshold region has been presented. Theoretical analysis matches well with simulation and measurement. The comparator was implemented in a 65 nm CMOS technology. Measurement results have shown that the threshold of the comparator is programmable from 27 mV to 46.5 mV with switching energy from 1.9 nJ to 2.4 nJ at the 4-control bit when $f_{in} = 10Hz$. The leakage power consumption is 270 pW at the 0.1 mV input level. The proposed comparator is promising for low frequency, low threshold, and near-zero-energy event sensing.

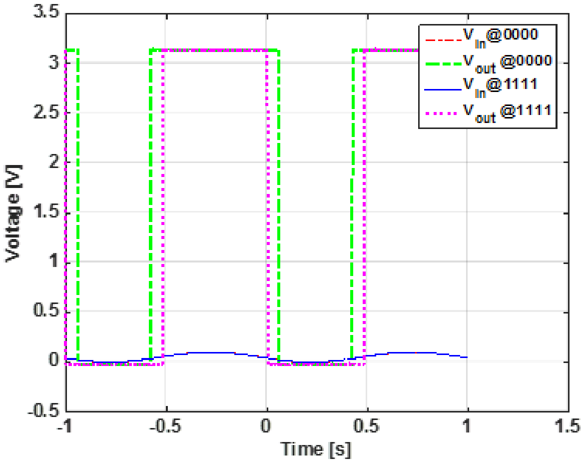


Figure 2.19: Measurement Vin (1 Hz/50mV) and Vout waveforms with codes 0000 and 1111.

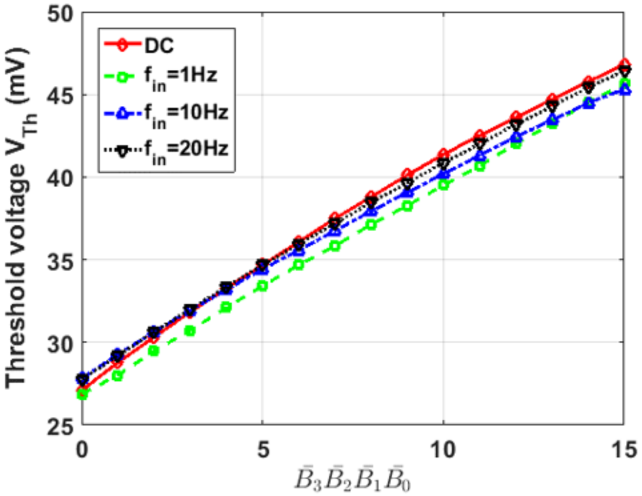


Figure 2.20: Measured V_{Th} versus control code at various input signal frequencies.

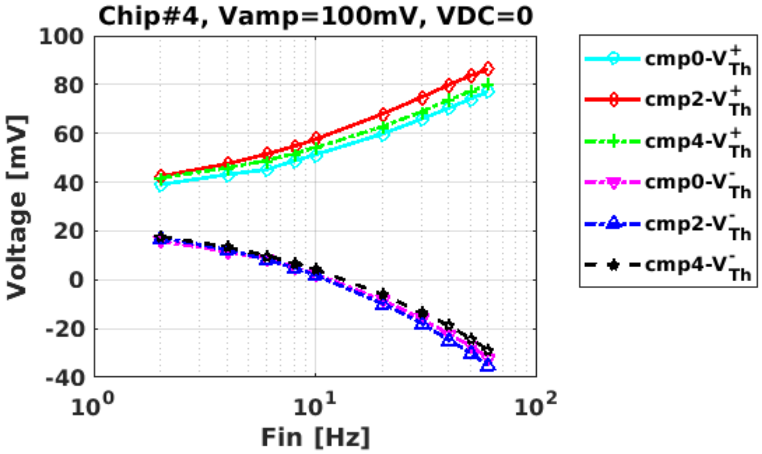


Figure 2.21: Measured V_{Th} versus input frequency across three comparators on one chip.

Table 2.1: Performance Summary

Metric	Performance
Threshold Voltage (V_{Th})	27 mV – 46.5 mV
Number of comparators on a single die	8
Threshold voltage precision (max)	$< 4.8mV$
Gate capacitance	8 fF(6.4 f+1.2 f)
Input resistance	$3.3G\Omega$
Number of cycles	> 20
Power consumption at $V_{in} = 0.1mV$	270 pW
Energy per switching @ $f_{in} = 10Hz$	1.9-2.4 nJ

Table 2.2: Performance Comparison

	[16]	This work† [17]	This work‡ [18]
Technology	0.18um CMOS	9HP BiCMOS	65nm CMOS
Supply (V)	3.0	1.0	1.2
Power (uW)	10.3@3V	684e-6	24e-3
$V_{Th}(mV)$	1415 – 1586	0 – 30	27 – 46.5
$f_{max}(Hz)$	–	160K*	1K*

†: Simulation results in a 9HP BiCMOS technology

‡: Measurement results in a 65nm CMOS technology

*: with the pre-defined amplitude of 100 mV

Chapter 3

A RESISTOR BASED SAR QUANTIZATION EMBEDDED TEMPERATURE SENSOR

3.1 Introduction and Motivation

Integrated temperature sensors are widely used in high-performance integrated circuits (ICs), especially CPUs and GPUs, to provide the thermal information, which can be used to control system clocks or used by circuit designers to develop advanced power and thermal management schemes [19]. The increase in the transistor number, the high core operating frequencies and switching activities, lead to high power density. Further, a single die usually integrates many different functional blocks, where some can be heated rapidly and may create hot spots. Without proper thermal detection, the accumulated heat may shorten the life time of a chip and cause unreliable operations or even damage the chip permanently [20]. By monitoring the die temperature with integrated temperature sensors, a microprocessor can reduce the clock frequency, the supply voltage, or both, to reduce the power consumption before the chip reaches the factory-set temperature limit [19]. Thus, integrated temperature sensors are crucial for high-performance ICs to maintain the proper thermal environment for reliable, long-term system operation.

The multi-core processor architecture prevails because high-performance computation is required for many applications. In general, each core works for a particular computation task with its own clock frequency and supply voltage. This leads to a non-uniform thermal distribution. Further, the thermal gradient among multiple cores can change for different instructions and applications [21]. Thus, multiple temperature sensors are required to enable localized measurement. For examples, three [22], ten [23], and forty [24] temperature sensors can be used in a processor. Therefore, it is desirable for integrated temperature sensors to have low power consumption and a small area. To save the power, temperature sensors are in the sleep mode for most of the time. Once activated by an enable signal, they perform several temperature measurements, then return to the sleep mode. Thus, it is important for temperature sensors to have a short conversion time (≤ 1 ms) [23, 25, 24] and latency so that the thermal management unit (TMU) can perform readout and make decision in time. For general IC thermal monitoring applications, it is sufficient to have a sensor whose accuracy is about ±1°C at the throttle and about ±3°C over the rest of the range [23, 25, 24]. It has been pointed out that "it is not necessary to have ultra-high resolution (≤ 0.05°C) temperature sensors in microprocessors, since the non-linearity associated with high-volume manufacturing will likely be much higher than resolution limits reported" [25] and [24].

Various types of integrated temperature sensors have been developed in CMOS technologies. Parasitic BJT-based bandgap sensors are the most established ones for industry-level applications [23]–[25, 26]. The linear temperature-to-voltage relationship leads to high linearity and accuracy. This physical mechanism is considered very reliable. However, BJT-based sensors need high supply voltages to bias a BJT in the forward-active region, and are thus not suitable for very low voltage operations. Further BJT sensors are mostly analog in nature, require power-consuming opamps, which are difficult to scale.

To achieve compact area and lower power consumption, CMOS transistor-based temperature sensors have been developed. These sensors use temperature-dependent carrier mobility and threshold voltage to generate temperature-dependent frequency of oscillation. A sub-threshold oscillator-based temperature sensor with an exponential temperature-to-frequency conversion was introduced to relax the reference timing constraint, and realized a 0.6 nJ/conversion energy efficiency [27]. A very compact (area is 0.004 mm^2) ring oscillator-based temperature sensor was designed in 65nm CMOS [28]. A fully integrated CMOS temperature sensor based on temperature independent/dependent current sources was developed, which uses oscillators and counters to generate a digital temperature code [29]. However, the temperature dependency of the carrier mobility and threshold voltage is less stable among different processes, which prevents its usage in the volume-production [25, 24].

On the other hand, the leakage current increases at the high temperature.

Very recently, resistor-based temperature sensors gained a lot of attention since a modern CMOS technology offers several types of resistors whose temperature coefficients are relatively constant. These temperature sensors can work at sub-1V supply voltages. A resistor-based temperature sensor was presented based on the measurement of an RC time constant [24]. A phase-domain $\Delta\Sigma$ ADC quantizes the temperature dependent phase shift generated by an RC Wien-bridge filter [30]. It is known that a $\Delta\Sigma$ ADC requires not-scalable, area and power consuming opamp circuits. A highly-digital resistor-based temperature sensor that uses a frequency locked loop (FLL) as the readout circuit achieved small area and high resolution [31]. The boosted output voltage of the poly-phase filter (PPF) -based sensing element puts extra constraints on the following stage circuit input.

This chapter presents the design and implementation of a resistor-based highly-digital temperature sensor. A differential low pass filter (DLPF) based sensing element is proposed to provide a temperature dependent phase shift. The phase shift is quantized by a successive approximation register (SAR) ADC whose CDAC is embedded into the DLPF. The embedded SAR-quantization eliminates the CDAC reference circuits and utilizes the full input range of the ADC. The proposed design was fabricated in a 65nm LP CMOS technology that occupies 8400 μm^2. It achieves 0.38 °C resolution at room temperature. After a 2-point calibration, the sensor achieves a 3σ inaccuracy of ± 1.2 °C from -30 to 100 °C. It consumes 35.2 μW power from a 1.1 V supply. With a 2.5 μs conversion time, the sensor achieves an 88 pJ/Conversion energy efficiency, which yields a 12.7 pJ·K^2 resolution FoM.

3.2 On-Chip Temperature Sensing with a Differential Low-Pass RC Filter

3.2.1 Response of a DLPF to a Complementary Clock

Figure 3.1 shows a differential RC low-pass filter (LPF) driven by a complementary periodic clock of period T with 50% duty cycle, and its output responses: differential output voltage $\text{V}_{\text{DLPF-P}}$ and $\text{V}_{\text{DLPF-N}}$. One response charges while the other response discharges at the

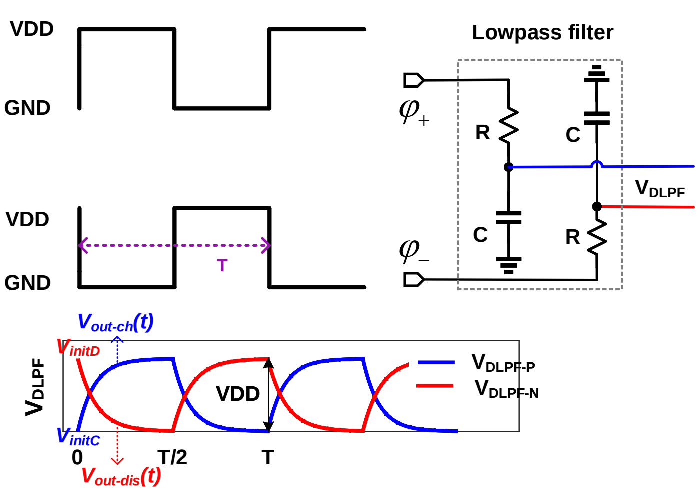


Figure 3.1: The transient response of a differential RC LPF to a complementary clock with a 50% duty cycle.

Table 3.1: Clock Period T in terms of RC Time Constant for Selected DOCP Reference Phases

t_{DOCP} or Ref. phase	$T/8$	$T/16$	$T/32$
T	$8ln(1.8393) \cdot RC$	$16ln(1.992) \cdot RC$	$32ln(2) \cdot RC$

* Calculation based on 50% duty cycle clocks.

same time, and this behavior repeats periodically. Considering one clock period $t = 0\ to\ T$, the charging response can be expressed as

$$V_{out-ch}(t) = V_{DD} - (V_{DD} - V_{initC})e^{\frac{-t}{RC}} \tag{3.1}$$

where $\mathrm{V_{DD}}$ is the high level of the input clock, while the low level is ground, and $\mathrm{V_{initC}}$ is the initial voltage at the beginning of charging. The discharging response can be expressed as

$$V_{out-dis}(t) = V_{initD}e^{\frac{-t}{RC}} \tag{3.2}$$

where $\mathrm{V_{initD}}$ is the initial voltage at the beginning of discharging.

Solving (1) and (2) with the conditions that $\mathrm{V_{initD}}$ is the final voltage at the end of charging and $\mathrm{V_{initC}}$ is the final voltage at the end of discharging when $t = T/2$, we have

$$V_{initC} = V_{DD}(e^{\frac{-T}{2RC}} - e^{\frac{-T}{RC}})/(1 - e^{\frac{-T}{RC}}) \tag{3.3}$$

$$V_{initD} = V_{DD}(1 - e^{\frac{-T}{2RC}})/(1 - e^{\frac{-T}{RC}}) \tag{3.4}$$

When $T > 10 \cdot RC$, then $\mathrm{V_{initC}} \approx 0$ and $\mathrm{V_{initD}} \approx \mathrm{V_{DD}}$.

The differential output crossing point (DOCP) is defined as the time when $\mathrm{V_{DLPF-P}}$ crosses $\mathrm{V_{DLPF-N}}$; i.e., they both reach to $\mathrm{V_{DD}}/2$. We can obtain

$$t_{DOCP} = RC \cdot ln(2/(1 + e^{\frac{-T}{2RC}})) \tag{3.5}$$

When $T/RC \to \infty$, $t_{DOCP} = RC \cdot ln2$.

Clearly the t_{DOCP} of a DLPF is determined uniquely by the RC time constant and period T. Note that we can use digital circuits to generate $T/2^i, i = 1, 2, 3, ...$ as *temperature-independent reference phases*. Then the design principle of a DLPF-based temperature sensor is to select T, R, and C for a reference phase so that $t_{DOCP} = T/2^i, i = 1, 2, 3, ...$ for a selected i. This is to select T to satisfy the following equality

$$T/2^i = RC \cdot ln(2/(1 + e^{\frac{-T}{2RC}})) \tag{3.6}$$

Let $x = e^{\frac{-T}{2^i RC}}$, then (6) is simplified to the following equation

$$x + \frac{1}{x^{2^{i-1}-1}} = 2 \tag{3.7}$$

This equation has a valid solution for $i > 2$ as when $i = 1$ *or* 2, $x = 1$, which leads to $T = 0$. Table 3.1 shows the required clock period T in terms of the RC time constant so that the DOCP occurs at a selected reference phase $T/2^i$ for $i = 3, 4, 5$. Then the temperature-induced phase difference can be measured and quantized.

3.2.2 The Choice of Sensing Resistor and Capacitor in a CMOS Process

In a typical CMOS technology, different types of resistors have different temperature coefficients (TCs), sheet resistances, and supply sensitivities. In general, a resistor that has a

Table 3.2: Characteristics of Resistors in a 65nm CMOS Technology

	k_1 †	k_2 †	sheet resistance	supply dependency
N+ diff w salicide	2.16e-3	-5.77e-6	15.5	7.73e-5
N+ diff wo salicide	1.62e-3	-1.36e-6	120	1.63e-4
N+ poly w salicide	2.15e-3	-6.08e-6	15	5.61e-5
N+ poly wo salicide	1.16e-4	5.35e-7	153	1.98e-4
Nwell under OD	2.45e-3	1.24e-5	327	3.09e-3
Nwell under STI	2.04e-3	1.57e-5	595	4e-3
P+ diff w salicide	2.36e-3	-7.1e-6	14.55	8.15e-7
P+ diff wo salicide	1.34e-3	-3.01e-7	245	9.22e-5
P+ poly w salicide	2.36e-3	-6.8e-6	15	1.41e-4
P+ poly wo salicide	-3.2e-4	1.45e-6	690	-5.11e-4

†: Simulation results based on 10 kΩ resistors with expression in (3.8)

large and relatively constant TC, a large sheet resistance, and a low supply sensitivity is preferred for temperature sensing. The relationship between resistance R and temperature $temp$ can be expressed in (3.8)

$$R(temp) = R_o \cdot [1 + k_1(temp - 27) + k_2(temp - 27)^2] \tag{3.8}$$

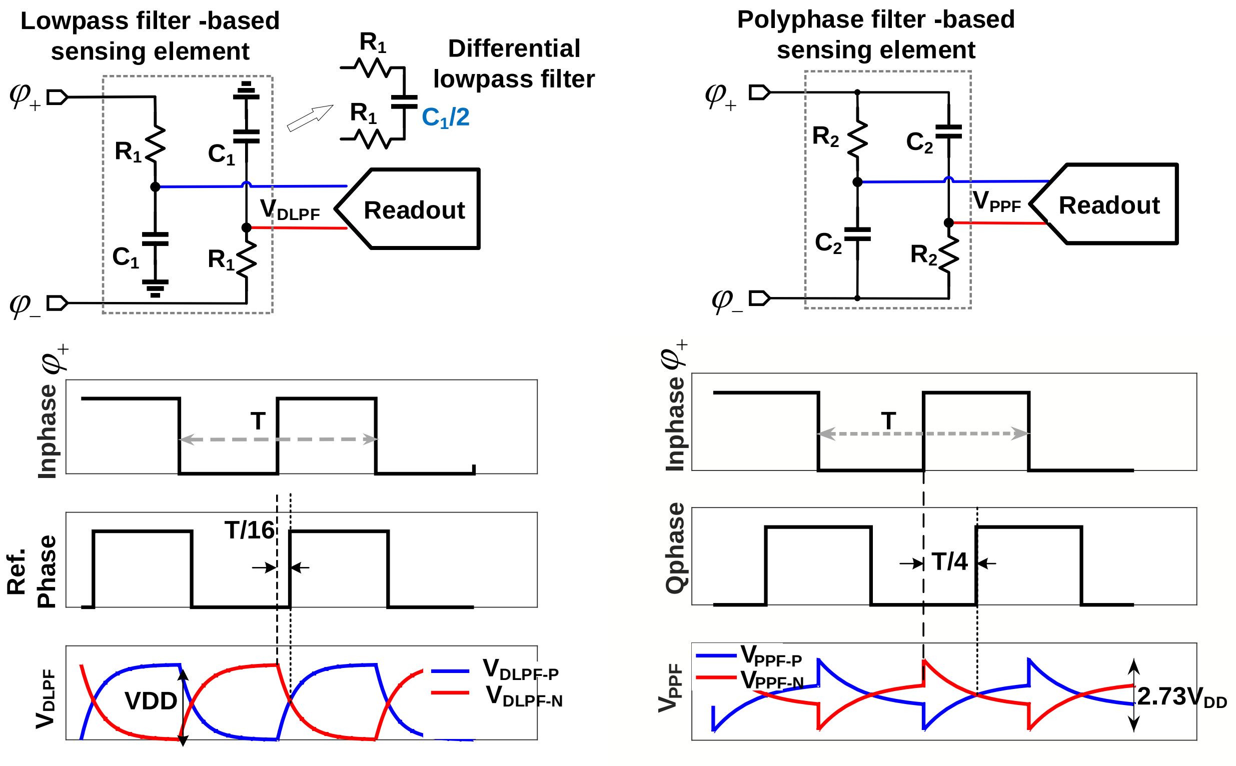
where R_o is the resistance at 27°C, k_1 is the first order TC, and k_2 is the second order TC. To achieve fine resolution and good linearity, k_1 shall be as large as possible, while k_2 should be as small as possible. From Table 3.2, we can see that the Nwell resistor under the oxide layer, the P+ diffusion resistor with salicide, and the P+ poly resistor with salicide have large first order TCs. However, the Nwell resistor has large nonlinear temperature and voltage dependency. The diffusion resistor has large parasitic and spreads more compared with the poly resistor [30]. Therefore, salicided p-poly resistors are used in this design for its large first order TC (2360 ppm/°C) and its small nonlinear temperature dependence (second order TC: -6.8 ppm/$(^\circ\text{C})^2$). Note that the salicided p-poly resistor has small sheet resistance, which can lead to a large area. In this design, the capacitor array occupies almost half of the area. There is no area penalty to use the salicided p-poly resistors since they are placed under the capacitor array.

Metal-oxide-metal (MOM) capacitor is used in this design. Compared with metal-insulator-metal (MIM) capacitor, it has following advantages. First, the MOM capacitor has slightly smaller first-order TC (-12 ppm/°C) compared with the TC (-16 ppm/°C) of the MIM capacitor. Second, the MIM capacitor requires additional fabrication masks into the process, which potentially increases the cost. Third, the capacitance density of the MOM capacitor (2.4 $fF/\mu m^2$) is slightly larger than that of the MIM capacitor (2 $fF/\mu m^2$) when more metal layers are used, there is no area penalty by using the MOM capacitor. Finally, the routing of the MOM capacitor is more flexible than the routing of the MIM capacitor that is being limited to M8 in 65nm CMOS.

The phase shift of the DOCP within a DLPF is mainly determined by the temperature dependent resistor when it is driven by a fixed cycle clock. The dynamic range of the phase shift (time difference between two extreme DOCPs) within a DLPF can be obtained by combining (3.5) and (3.6) and cancelling C,

$$t_{dyn} = \frac{T}{2^i} \cdot \frac{R(temp_H) - R(temp_L)}{R_o} \tag{3.9}$$

Here $i = 3, 4, 5, ...$, $temp_H$, and $temp_L$ are the high and low temperatures that the sensor can detect. The dynamic range is proportional to the chosen reference phase $T/2^i$ and the TC of the resistance based on (3.9). It has no relationship with the absolute value of the resistance R and the capacitance C.



(a) Proposed DLPF-based temperature sensor **(b) PPF-based temperature sensor**

Figure 3.2: Sensing element comparison: DLPF versus PPF with ideal readout circuits.

3.2.3 Comparison of DLPF and PPF -based Sensing Elements

Figure 3.2 (a) and (b) show the principle of the proposed DLPF-based and the previous PPF-based [31] temperature sensors. Both sensing elements consist of temperature-dependent salicided p-ploy resistors ($R_{1,2}$) and temperature-insensitive MOM capacitors ($C_{1,2}$). Driven by the same cycle complementary clock φ_+ and φ_-, the differential output response of V_{DLPF} and V_{PPF} charges and discharges symmetrically. The phase shift of the differential output is quantized by a readout circuit.

The difference between these two topologies lies in two aspects. First, the connection of the capacitor is different. The connection of the capacitor in the DLPF can maintain its differential output voltage V_{DLPF} in the range of $\mathrm{V_{DD}}$. The two C_1 can be merged into one

$C_1/2$ that saves the capacitance value by 4X. However, the connection of the capacitor in the PPF boosts its differential output voltage V_{PPF} to 2.73$\mathrm{V_{DD}}$. The boosted voltage improves the slope at the crossing point. But it puts extra constraints on the following stage input[31].

Second, the reference phase in the DLPF is chosen $T/16$ delay of the input clock φ_+ to have a large slope of the output voltage at the DOCP without boosting its output voltage. A smaller reference phase increases the slope of the output voltage at the DOCP. But it also decreases the dynamic range according to (3.9) and requires a higher order frequency divider to generate a smaller reference phase. Whereas, one-quarter delay of φ_+ is chosen as the reference phase in the PPF which is referred to quadrature phase, Qphase [31].

In Fig. 3.2 (a), the charging and discharging responses can be obtained from (3.1) and (3.2) with the initial condition of $V_{initC} = 0$ and $V_{initD} = V_{DD}$.

They cross each other at the time

$$t_{DOCP} = ln(1.992)R_1C_1 = \frac{T}{16} \tag{3.10}$$

Similarly, in Fig. 3.2 (b), the charging response is

$$V_{PPF-ch}(t) = V_{DD} - \frac{1}{2}(2+\sqrt{3})V_{DD}e^{\frac{-t}{R_2C_2}} \tag{3.11}$$

and the discharging response is

$$V_{PPF-dis}(t) = \frac{1}{2}(2+\sqrt{3})V_{DD}e^{\frac{-t}{R_2C_2}} \tag{3.12}$$

They cross each other at the time

$$t_{DOCP} = ln(2+\sqrt{3})R_2C_2 = \frac{T}{4} \tag{3.13}$$

If the resistors in the DLPF and the PPF have the same resistance; i.e., $\mathrm{R_1} = \mathrm{R_2} = \mathrm{R_0}$ and driven by the same cycle clock, the required capacitance in the DLPF is 2.1X smaller than that in the PPF based on (3.10) and (3.13). The switching energy of the DLPF is 5.75X lower than that of the PPF since the PPF output voltage is boosted to 2.73X $\mathrm{V_{DD}}$ and the capacitance is 2.1X greater.

The slope of the output response is its first order derivative. At its reference phase, the slope of DLPF S_{DLPF} is given in (3.14) based on (3.1) and (3.10)

$$S_{DLPF} = \frac{dV_{out-ch}(t)}{dt}|_{t=ln(1.992)R_1C_1} = 8ln(1.992)\frac{V_{DD}}{T} \tag{3.14}$$

while the slope of PPF S_{PPF} at its reference phase is given by (3.15) based on (3.11) and (3.13)

$$S_{PPF} = \frac{dV_{PPF-ch}(t)}{dt}|_{t=ln(2+\sqrt{3})R_2C_2} = 2ln(2+\sqrt{3})\frac{V_{DD}}{T} \tag{3.15}$$

Comparing (3.14) with (3.15), the slope of the DLPF is 2.1X greater than that of the PPF. The thermal noise of the resistor affects the crossing point inversely proportional to the slope S through (3.16) [32]

$$\sigma_t \propto \frac{\Delta V_n}{S} \tag{3.16}$$

Therefore, the jitter in the DLPF due to resistor thermal noise at its reference phase is

$$\sigma_{t_{DLPF}} \propto \frac{\sqrt{K \cdot \mathrm{temp}/C_1}}{S_{DLPF}} = \sqrt{\frac{K \cdot \mathrm{temp} \cdot R_0 \cdot T}{4ln(1.992) \cdot V_{DD}^2}} \tag{3.17}$$

whereas, the jitter in the PPF at its reference phase is

$$\sigma_{t_{PPF}} \propto \frac{\sqrt{K \cdot \mathrm{temp}/C_2}}{S_{PPF}} = \sqrt{\frac{K \cdot \mathrm{temp} \cdot R_0 \cdot T}{ln(2+\sqrt{3}) \cdot V_{DD}^2}} \tag{3.18}$$

where K is the Boltzman constant. From (3.17) and (3.18), we can see that with the same resistance, driven clock, and supply voltage, the DLPF has $\sqrt{2.1}$X smaller jitter at its reference phase compared with the PPF sensing element.

The dynamic range given in (3.9) is directly proportional to the reference phase. From this, the dynamic range of the DLPF is reduced by 4X compared with that of the PPF. The jitter in the DLPF is improved by 1.45X. Thus, the temperature resolution is reduced by 2.76X. It is sufficient for most of the IC thermal monitoring applications with 0.5 to 1 $°C$ resolution [23, 25, 24].

The two C_1 capacitors in the DLPF can be merged to one $C_1/2$ to form a differential LPF. With this, the total capacitance is reduced by 4X, and there is no need to match the

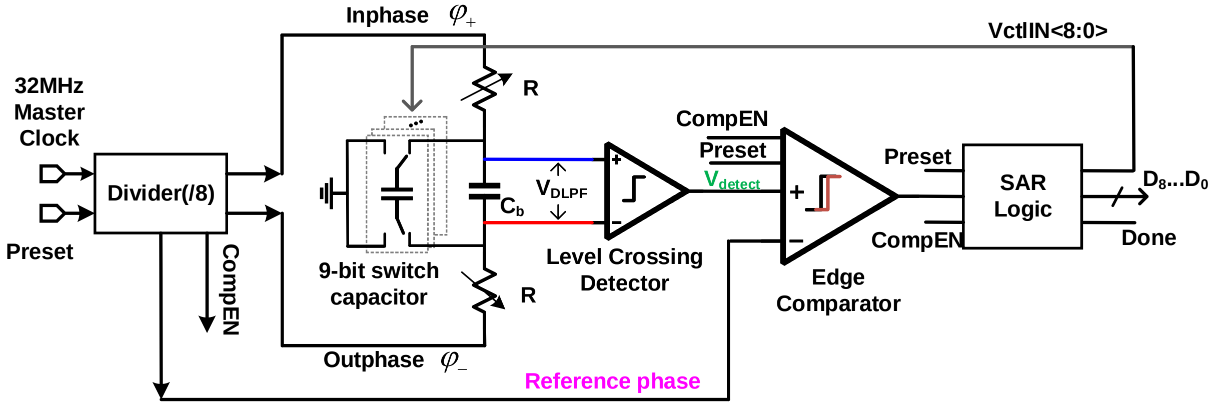
Table 3.3: Performance Summary and Comparison of DLPF and PPF -based Sensing Elements.

	DLPF-based sensing element	PPF-based sensing element
Refereence phase	T/16	T/4
Diff. output crossing point	$t = ln(1.992)R_1C_1 = \frac{T}{16}$	$t = ln(2+\sqrt{3})R_2C_2 = \frac{T}{4}$
Resistance @ room temp	$R_1 = R_0$	$R_2 = R_0$
Capacitance	$C_1 = \frac{T}{16ln(1.992)R_0}$	$C_2 = \frac{T}{4ln(2+\sqrt{3}R_0}$
Energy consumed by the driver	$2C_1V_{DD} \times V_{DD}$	$2C_2V_{DD} \times 2.73V_{DD}$
Slope @ the crossing point	$8ln(1.992)\frac{V_{DD}}{T}$	$2ln(2+\sqrt{3})\frac{V_{DD}}{T}$
Jitter@ the reference phase	$\sqrt{\frac{K \cdot temp \cdot R_0 \cdot T}{4ln(1.992) \cdot V_{DD}^2}}$	$\sqrt{\frac{K \cdot temp \cdot R_0 \cdot T}{ln(2+\sqrt{3}) \cdot V_{DD}^2}}$
Dynamic range	$\frac{T}{16}\frac{R(temp_H)-R(temp_L)}{R_0}$	$\frac{T}{4}\frac{R(temp_H)-R(temp_L)}{R_0}$

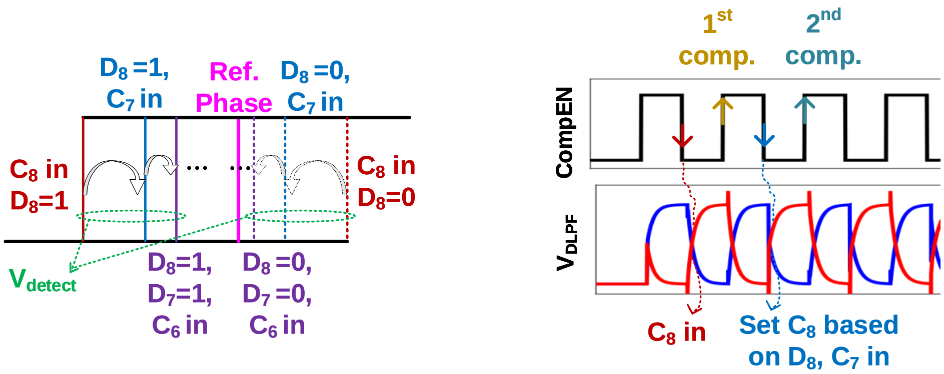
two C_1 capacitors as in the PPF-based design. The total capacitance is reduced by 8.1X compared with the capacitance in the PPF, this reducing the capacitance area by 4X. The performance comparison is summarized in Table 3.3. From the comparison table we can see that the dynamic range (resolution) is effectively used to trade off the area and power consumption.

3.3 *Proposed SAR-Quantization Embedded DLPF Temperature Sensing Architecture*

To be used for on-chip SoC thermal management, temperature sensors require a resolution of 0.5 to 1 °C [23, 25, 24] among the range of -40 to 100 °C. This specification corresponds to an 8 to 9 bit quantization, which is the most suitable for the SAR ADCs. Straightforward SAR ADC implementation requires additional area-consuming capacitor arrays, voltage reference generators, and delay-to-voltage converters (such as mixers in [30]). This work eliminates all these additional blocks by re-using the capacitor in the DLPF. We refer to this technique as *SAR-quantization embedded DLPF temperature sensing.* The phase shift in the DLPF due to the temperature-dependent resistance is quantized by successively adjusting the binary weighted capacitance in the DLPF.



(a) SAR-quantization embedded DLPF temperature sensing architecture



(b) SAR operation in time domain

(c) Set capacitor and comparison in the SAR operation

Figure 3.3: Block diagram and operation principle of the DLPF-based SAR-quantization embedded sensing .

Figure 3.3 shows the block diagram and operation principle of the proposed SAR-quantization embedded DLPF-based temperature sensor. The *Preset* signal and a 32 MHz master clock are derived from an on-chip system clock. The 32 MHz master clock is divided by 8 to generate a 4 MHz complementary clock φ_+, φ_-, the reference phase clock, which is T/16 delay of φ_+, and a *CompEN* that is generated by φ_+ and the inverse of *Preset*. These four signals have little temperature dependency. The resistors in the DLPF can be tuned from 9 to 12.5 KΩ with 8-bit non-uniform thermometer weights to compensate process variation of the DLPF and the level crossing detector. The capacitor $C_1/2$ in Fig. 3.2 (a) was implemented as a fixed base capacitor C_b and a 9-bit binary weighted capacitor array with the unit capacitance C_u of 1 fF. The dynamic range (phase shift) due to the temperature dependent resistance is about 5.2 ns from -40 to 120 °C, which can be estimated from (3.9) when T/16 reference phase is used.

The sensor is initiated by the *Preset* signal followed by the 32 MHz clock. The SAR logic performs the conventional binary searching algorithm; i.e., setting the most significant bit (MSB) capacitor C_8 to the DLPF bridge and the rest of the bits $C_7, ..., C_0$ to GND for the first comparison shown in Fig. 3.3 (b). Then, the level crossing detector detects the differential output crossing point of $\mathrm{V_{DLPF-P}}$ and $\mathrm{V_{DLPF-N}}$ and generates $\mathrm{V_{detect}}$. Then, the edge comparator compares $\mathrm{V_{detect}}$ with the temperature independent reference phase. If $\mathrm{V_{detect}}$ lags the reference phase, the edge comparator outputs digital "1"; i.e., $\mathrm{D_8} = 1$, and the MSB $\mathrm{C_8} = 256\mathrm{C_u}$ keeps connecting to the DLPF bridge. Otherwise, $\mathrm{D_8} = 0$, and $\mathrm{C_8}$ disconnects from the DLPF but to GND. Then, $\mathrm{C_7} = 128\mathrm{C_u}$ connects to the DLPF bridge for the next bit comparison. This process continues till to the least significant bit (LSB) C_0. $\mathrm{V_{detect}}$ is close to the reference phase within one LSB resolution after setting the LSB bit.

It is noted that connecting or disconnecting capacitors to the DLPF bridge disturbs the charging and discharging processes with changing the capacitance $(C_b + D \cdot C_u)$. To eliminate this disturbance and the error associated with the switch on/off activities such as charge injection and clock feedthrough, the bit capacitors to the DLPF are connected or disconnected at the falling edges of the *CompEN* signal, while comparing $\mathrm{V_{detect}}$ with the reference phase at the next rising edges, at which time the capacitance in the DLPF is unchanged and also there is no switching activity. The first two cycles are denoted in Fig. 3.3 (b). The outcome of embedding SAR-quantization in the sensing circuit is to quantize the RC phase shift due to the temperature dependent resistance through successively adjusting

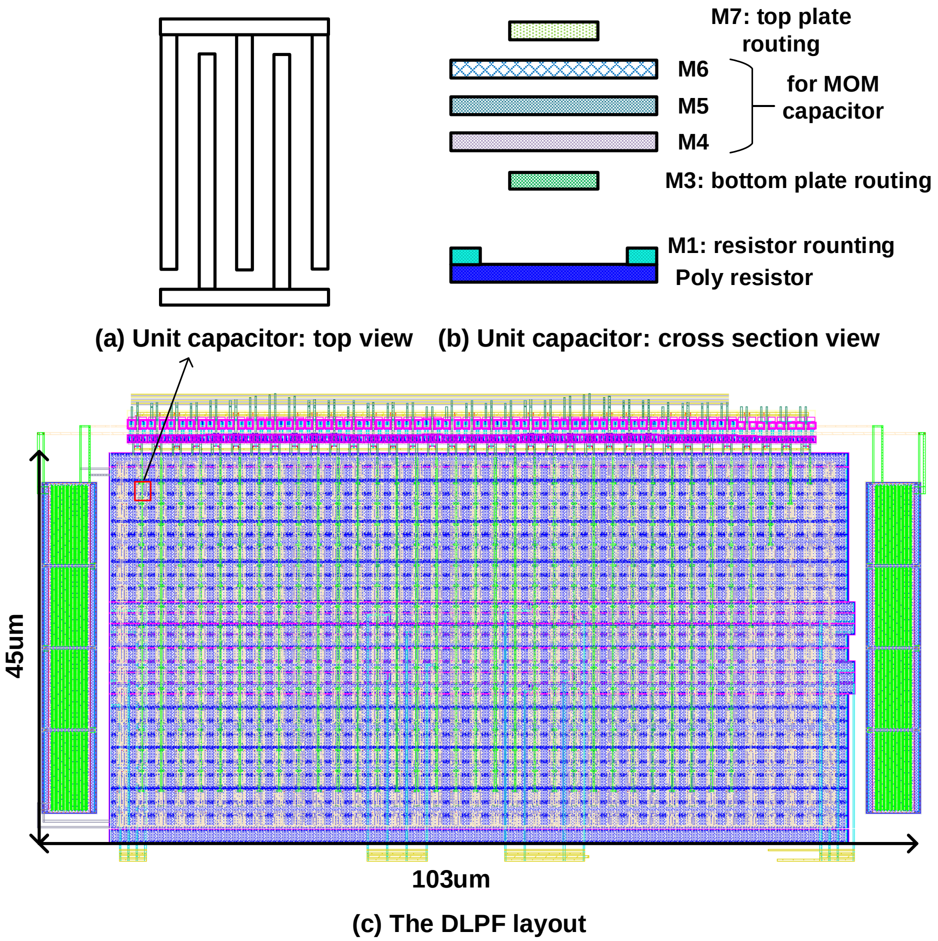


Figure 3.4: The custom designed unit capacitor and the DLPF layout.

the binary weighted capacitance in the DLPF. The digital code D can be expressed as

$$ln(1.992) \cdot R \cdot (C_b + D \cdot C_u) = T/16 \tag{3.19}$$

with R given in (3.8).

3.4 Circuit Implementation

3.4.1 DLPF-based Sensing Elements

In the DLPF, the base capacitor is a MOM capacitor from the process library provided by the foundry. The 9-bit capacitor array is a custom designed interdigitated MOM capacitor array shown in Fig. 3.4 (a) and (b). Metal layers M4, M5, and M6 are used to form unit capacitors utilizing coupling, while M3 is reserved for bottom plate routing and M7 for top plate routing. This minimizes the parasitic routing capacitance. The poly resistors in the DLPF are laid out under the capacitor array. Overlapping the MOM capacitor array and the poly resistors not only saves the area for the poly resistors but also makes it easy to meet the poly and metal density rules. The 9-bit capacitor array occupies 0.004 mm^2, which takes 47.4% of the entire core area. Thus, the width of the poly resistors is enlarged to 1.4 μm to make sure two tunable resistor ladders occupy the same area as the capacitor array. To this extent, the mismatch of the resistance is decreased by 3.44X compared with using the minimum width (0.4 μm) poly resistors. Both the resistor ladders and the capacitor array are surrounded by their dummies to decrease mismatch. The fixed base MOM capacitor is placed symmetrically at the two sides of the capacitor array as shown in Fig. 3.4 (c).

3.4.2 Level Crossing Detector

The level crossing detector is implemented as an inverter based threshold comparator shown in Fig. 3.5 for lower power consumption and good scaling capability [33]. V_{DLPF-P} crosses with V_{DLPF-N} at $V_{DD}/2$. The comparison between V_{DLPF-P} and V_{DLPF-N} is equivalent to the comparison between V_{DLPF-P} and $V_{DD}/2$. In the inverter based threshold comparator, the switching threshold voltage V_{ST} is internally decided by the sizes of M0 and M_1 in Fig. 3.5, while the comparison voltage is V_{DLPF-P}. V_{ST} is defined as the voltage at which the inverter $V_{in} = V_{out} = V_{DD}/2$. With high supply voltages, i.e., $VDD > V_{tn} + |V_{tp}|$, both M0 and M_1 work in the saturation region with V_{ST} as the input. Then V_{ST} is obtained by equaling the

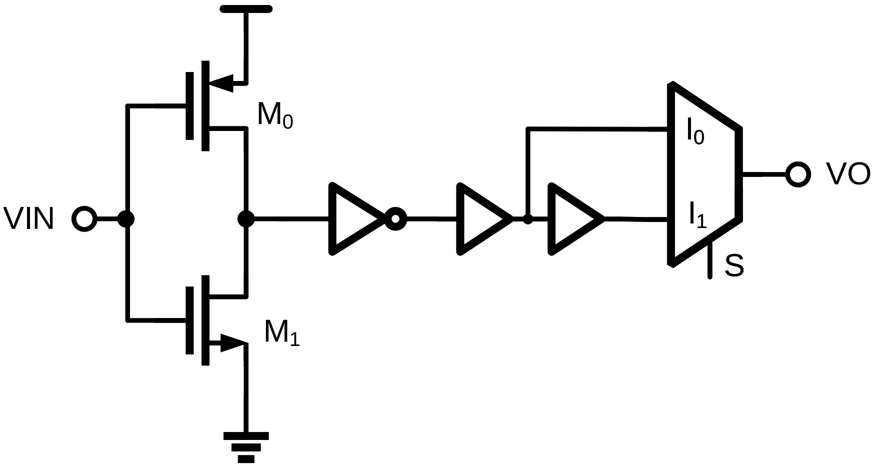


Figure 3.5: An inverter based level crossing detector.

currents through M0 and M_1 as shown in (3.20)

$$V_{ST} = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}} \tag{3.20}$$

here $\beta_n = \mu_n C_{ox}(W/L)_n$, and $\beta_p = \mu_p C_{ox}(W/L)_p$. $V_{ST} \approx VDD/2$ through optimizing the sizes of M0 and M_1 in the inverter [34, 35].

The following two buffers are added to shape the waveform and a 2:1 MUX is used to tune the delay at different supplies. The reference phase also passes through the same level crossing detector to cancel the supply and temperature dependency in the first order. Simulation results show that the delay difference between the reference phase path and the signal path is 16 ps when V_{DD} varies from 1.0 to 1.2 V at room temperature, which corresponds to 0.48 °C temperature error. The delay difference changes at a slope of 1.2 to 2.5 ps/°C from -40 to 120 °C at a 1.1 V supply, which corresponds to 0.1 °C temperature error. The simulated input referred noise is 60 μV_{rms} that translates into to 0.16 °C temperature error. From the Monte Carlo simulations, 1-σ variation of the offset delay is 172 ps that translated into a temperature inaccuracy of ±1.2 °C (3σ) after a 2-point digital calibration.

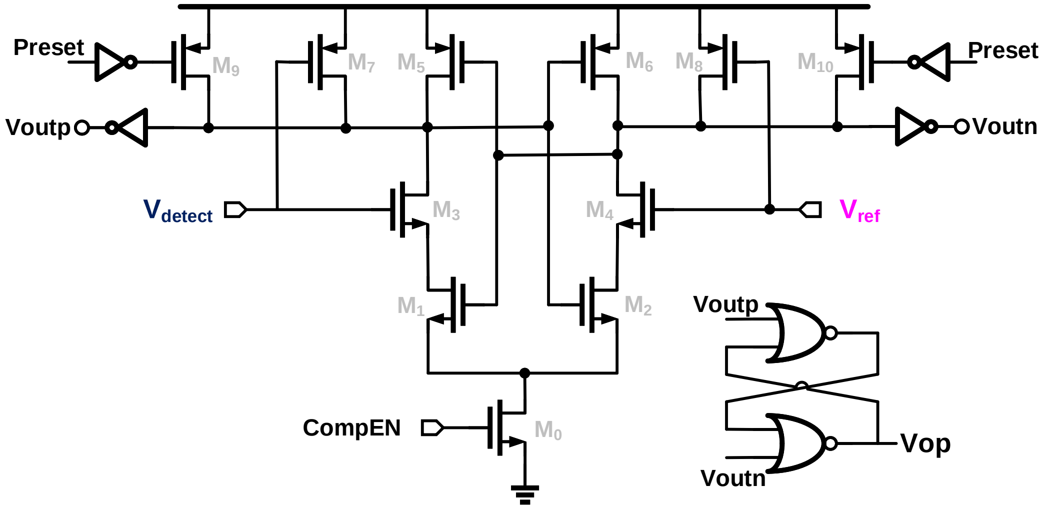


Figure 3.6: A dynamic latch based edge comparator.

3.4.3 Edge Comparator

The inputs to the edge comparator are two square wave signals: V_{detect} and reference phase V_{ref}. The edge comparator detects whether V_{detect} leads or lags V_{ref}. A dynamic latch based comparator is adopted shown in Fig. 3.6. The comparator is enabled through $CompEN$, which is before the rising edge of its two input signals. NMOS $M_3(M_4)$ and PMOS $M_7(M_8)$ are both controlled by the input $V_{detect}(V_{ref})$. When both of the inputs are low, the outputs are set to low. There is no current flow through the circuit, as M_3 and M_4 are off. If V_{detect} leads V_{ref}, then V_{outp} is set to low, Otherwise, V_{outp} is set to high. An SR latch is used to keep the outputs of the edge comparator for the whole cycle. The size of the transistors is optimized for low offset and small noise [36, 37]. The average current of the edge comparator is 90 nA from a 1.1 V supply at a 4 MHz clock. The 3σ offset and the input referred noise converted to time are 1.8 ps and 0.1 ps, respectively. These are translated into 0.048 and 2.7m °C temperature errors.

3.5 Measurement Results

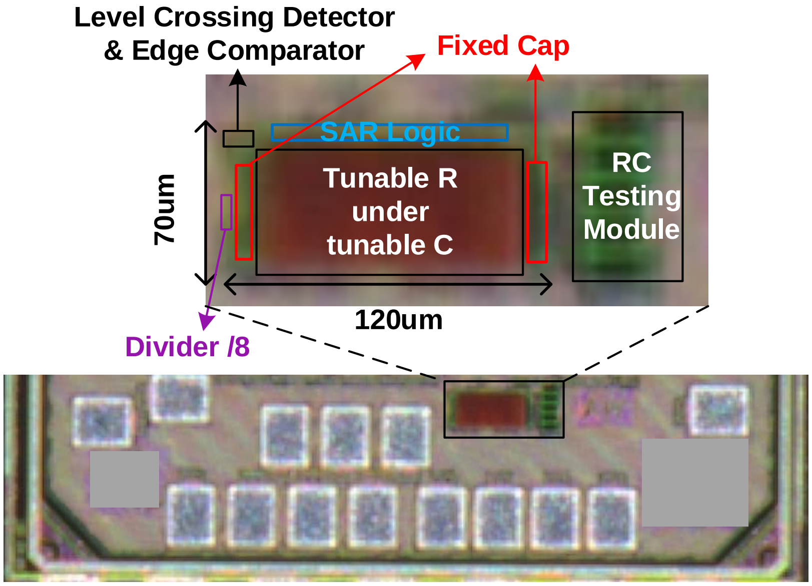


Figure 3.7: Die micrograph.

The temperature sensor prototype was fabricated in a 65nm LP CMOS technology. The die photograph is shown in Fig. 5.23 with a 0.0084 mm^2 active core area. Replicas of resistors and capacitors are placed beside the core to test the process of the fabrication. The chip has an SPI interface, which is used to connect to a micro-controller/FPGA board (PYNQ-Z1) for testing. The clock is provided by the PLL on the micro-controller, acting like the SoC master clock with noisy jitters in practice. The measurement was done by placing the test board in a temperature-controlled Tenney environmental chamber, and the PYNQ-Z1 board driven by a computer connecting to the test board is placed outside of the chamber shown in Fig. 3.8. Only one DC power supply is required to provide the supply voltage for the LDO on the testing board.

When running at the conversion time of 2.5 μs (one SAR cycle is 250 ns, nine SAR cycles and one done cycle count for one conversion), the entire temperature sensor consumes 35.2

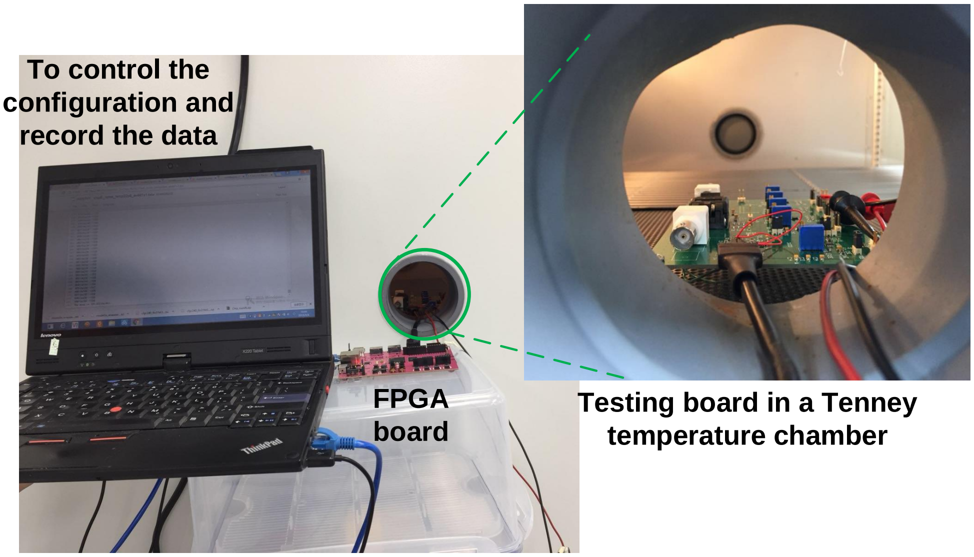


Figure 3.8: Measurement Setup.

μW under a 1.1 V supply. This yields an energy efficiency of 88 pJ/Conversion. The DLPF driver consumes 31.1 μW, which is 89% of the total power.

Twelve samples in QFN40 packages from one MPW shuttle are characterized from -30°C to 100 °C. Figure 3.11 (a) shows the measured raw digital output versus temperature. The nonlinear digits versus temperature relationship is introduced by the design formula shown in (3.19). Figure 3.11 (b) upper plot shows the temperature error after a two-point calibration over -30 to 100 °C. It clearly shows the second-order nonlinearity leads to the 3σ temperature error as much as 3.5 °C. The second-order nonlinearity is mainly from the second order temperature coefficient of the resistor shown in (3.8). This nonlinearity is very similar among sensors, therefore can be nulled. After removing the second order systematic nonlinearity, a 3σ inaccuracy of ±1.2 °C is achieved using two-point calibration shown in the Fig. 3.11 (b) lower plot. A two-point calibration is used as the D_{out} to the temperature relationship has at least three variables.

The effective resolution of the sensor at is obtained by calculating the root mean square

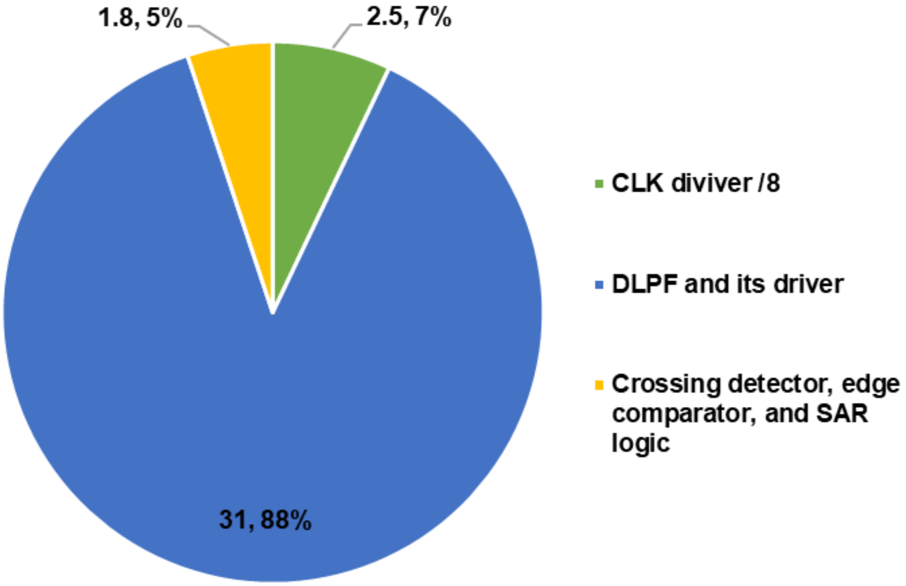


Figure 3.9: The Measured power consumption breakdown under a 1.1V supply.

(rms) value of 500 consecutive readouts at each temperature. Figure 3.12 (a) shows the temperature error of 500 consecutive readouts measured at 25°C. It shows the rms resolution of 0.38 °C. The temperature resolution is characterized at the entire temperature range from -30 to 100 °C using rms noise calculation. The result is shown in Fig. 3.12 (b). The resolution decreases with the temperature as more noise presents at higher temperatures. The supply sensitivity is characterized from 1.0 to 1.2 V at three different temperatures shown in Fig. 3.13. The temperature sensor has 2.8 °C/V supply sensitivity at 30 °C. While it increases to 7 °C/V at -30 °C. The measured results match the simulation results in Section V-B.

Table 5.1 summarizes the measured sensor performance and compares it with the state-of-the-arts. This work achieves a FoM of 12.7 pJ·K^2, which is 40X better than that of the BJT-based sensor with the similar resolution [26], The area is 5X smaller than [39], 13X smaller than [40] that use the SAR ADCs as the readout circuits. The sensor has

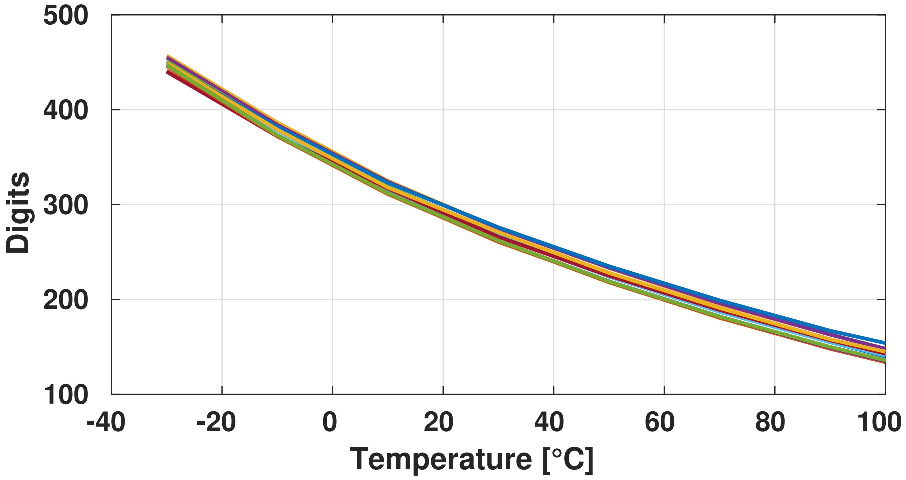
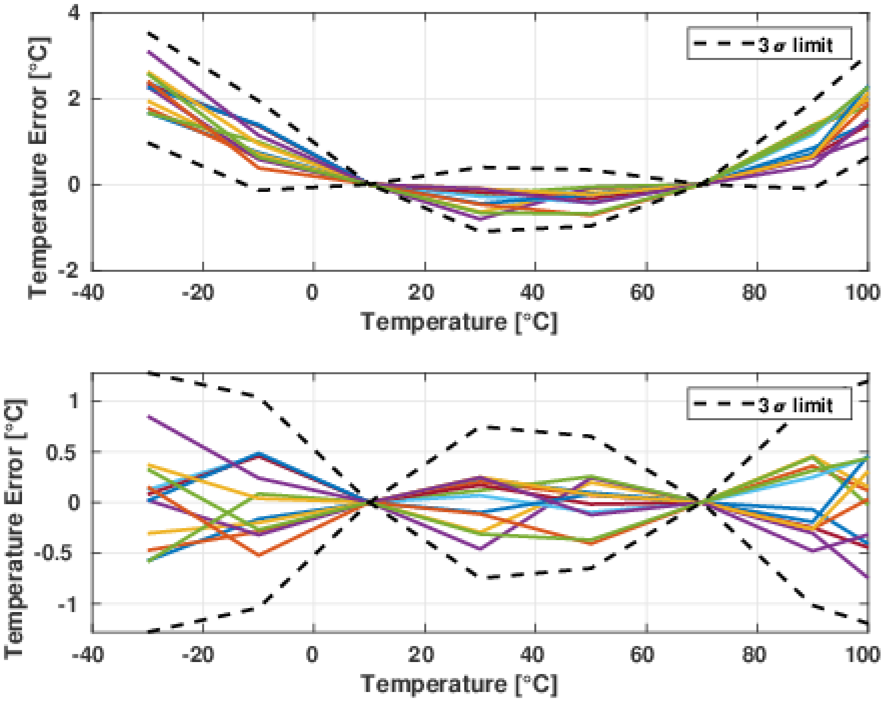


Figure 3.10: Measured sensor output digits versus temperature.

4X-400X faster conversion time than the state-of-the-arts. Figure 3.14 shows the resolution FoM benchmark of the proposed work. The energy/conversion of 0.088 nJ is achieved with smaller area and fast conversion time [1].

3.6 Conclusion

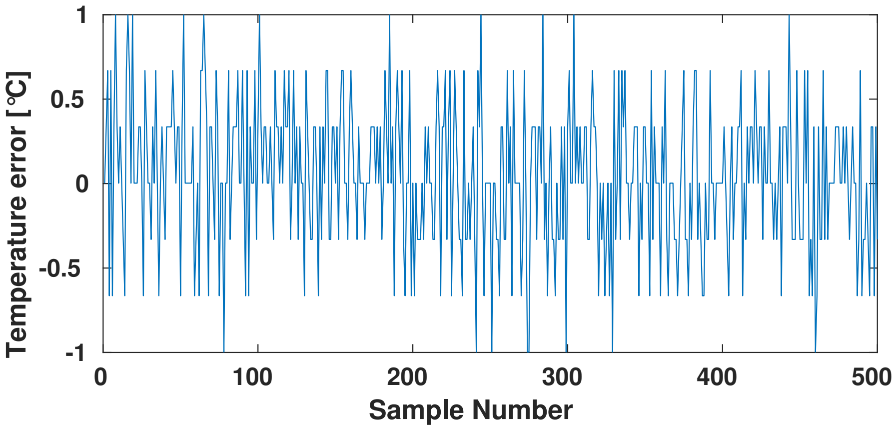
A resistor-based, area compact (0.0084 mm^2 implemented in 65nm CMOS) temperature sensor was presented. It uses a salicided p-poly resistor to sense the temperature, a differential low-pass filter (DLPF) to generate a temperature-dependent phase, which is then quantized by adjusting the MOM capacitor in the DLPF via successive approximation registration (SAR). This SAR-quantization embedded DLPF sensing architecture utilizes the full temperature-sensing range for digitization, reuses SAR capacitors, eliminates CDAC reference circuits, is much more area efficient than previous PPF and WB followed by SAR quantization architectures. Measurement results show that it achieves a 12.7 $pJ{\cdot}K^2$ resolution FoM. With a 2.5 μs conversion time, it achieves an 88 pJ/Conversion energy efficiency, which is the fastest sample rate with good energy efficiency comparing to the state-of-the-arts. Furthermore, the highly-digital architecture enables easy process migration and the



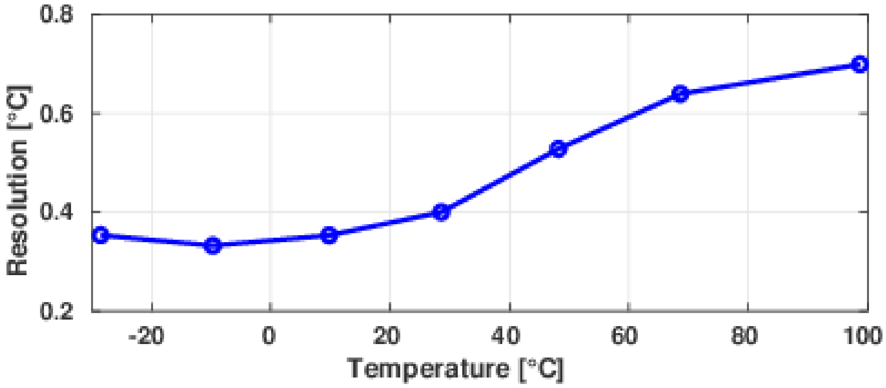
(b)

Figure 3.11: The temperature error after a 2-point calibration without and with removing the 2^{nd} systematic error.

use of a standard digital design flow.



(a)



(b)

Figure 3.12: (a) Measured temperatures error at 25°C. (b) Measured rms resolution versus temperature.

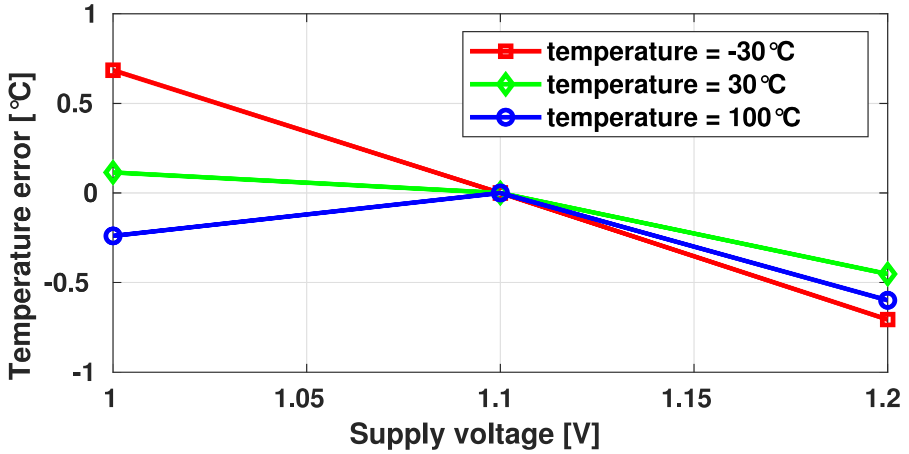


Figure 3.13: Measured temperature error versus supply at different temperatures.

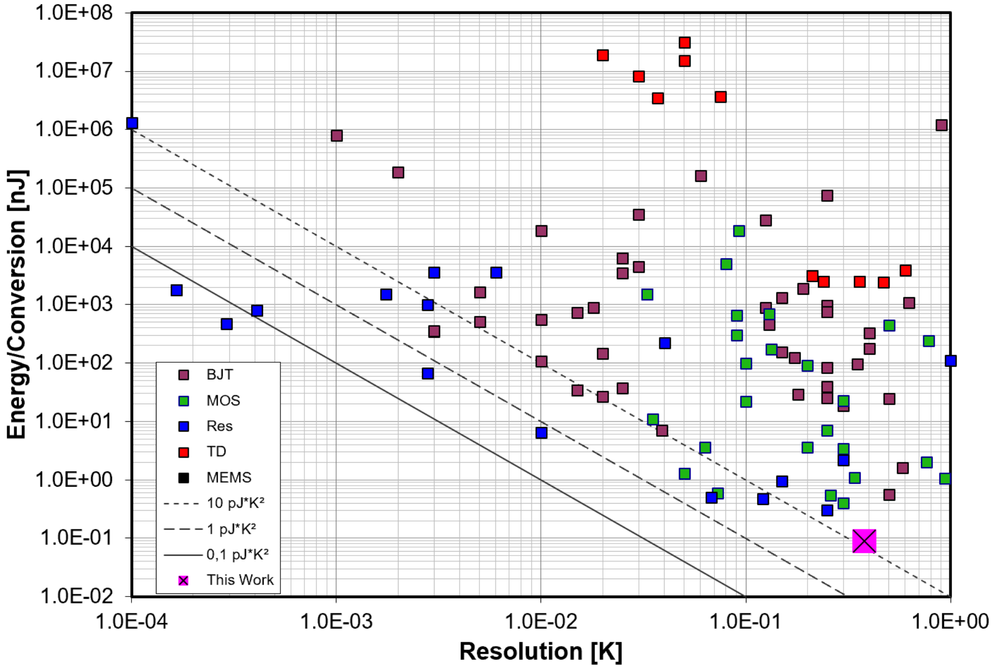


Figure 3.14: Resolution FoM benchmark of this work compared with the published temperature sensors [1].

Table 3.4: Performance Summary and Comparison with the State of the Arts.

	This work [38]	JSSC 2018 [24]	JSSC 2018[31]	ISSCC 2018 [26]	JSSC 2018 [39]	SSCL 2018 [40]
Sensor Type	**Resistor**	Resistor	Resistor	PNP/MOS	Resistor	Resistor
Readout Type	**SAR**	TDC	FLL	SAR	Flash-SAR	SAR
Technology	**65nm**	65nm	65nm	22nm	65nm	65nm
Supply [V]	**1.0∼1.2**	1.1∼1.4	0.85∼1.05	0.97∼1.3	0.6∼1.2	0.65, 1
Sup. sen. [°C/V]	**2.8**[†]	3	0.5	1.75	0.28	N/A
Power [μW]	**35.2**	12.8	68 *	50	47.2	0.488
Conv. Time [μs]	**2.5**	80	1000	32	10	10
Ene/Conv. [nJ]	**0.088**	0.9	68	1.6	0.472	0.00488
Area [mm^2]	**0.0084**	0.01	0.007*	0.0043	0.044	0.11
Temp Range [°C]	**-30∼100**	-40∼110	-40∼85	-30∼120	-45∼85	0∼100
Resolution [°C]	**0.38**	0.15	0.0025	0.58	0.121	0.61
Calibration Type	**2-point**	2-point	2-point	1-point	2-point	1-point
3σ Inaccuracy [°C]	**±1.2**	± 1.4	±0.12	±1.07	+1.6/-1	-1.1/1.5
FoM [pJ·K^2]	**12.7**	20	0.43*	540	6.9∼13.8	1.82

*: Does not include an on-chip frequency to digital converter.

†: Supply sensitivity at 30 °C

Chapter 4

ANALYSIS OF PASSIVE CHARGE SHARING SAR ADCS

4.1 Introduction

The core of Successive Approximation Register (SAR) Analog to Digital Converters (ADCs) is to convert an analog input voltage to a multi-bit digital code by sampling the input onto a bit weighted capacitor array and then deciding each bit, starting from the most significant bit (MSB) down to the least significant bit (LSB) by charge redistribution [41]. Using simple architectures and building blocks consisting only of switches, capacitors, comparators, and digital logic with no static power consumption, SAR ADCs are scalable with the digital CMOS technology. With recently introduced switching schemes achieving less switching activity [42, 43, 44], SAR ADCs have become the most energy-efficient data conversion solutions for 10-100 MHz sampling rates with 10-12 bit resolution [45, 46, 47]. Furthermore, combined with pipeline [48, 49], time interleaving [49], and noise shaping [50], SAR ADCs are being extended to applications with even higher speed up to GHz [51] or higher resolution up to 18 bits[52].

High-speed high-resolution SAR ADCs require accurate voltage references for each bit decision. With bonding wire inductance, bit switching settling to the needed accuracy often requires a very large decoupling capacitor and/or a large-bandwidth linear buffer. This reference buffer can consume power many times more than the SAR ADC itself, and is not scalable with the digital CMOS technology. To remove the power-hungry buffer, passive charge sharing was introduced [53]. One implementation of passive charge sharing [54] is to replace the reference by a sufficiently large capacitor precharged to the reference voltage acting as the reference for all bit switchings during the entire analog to digital conversion, which is referred to as *Sample-wise Switched Reference Charge Reservoir (SS-RCR)*. An improvement of SS-RCR for SAR ADCs was introduced in [55, 56, 57]. For *each bit* decision, a bit reference charge reservoir with the capacitance β times larger than that of the bit weight capacitor is used to replace the reference source. This improvement is referred to as *Bitwise Switched Reference Charge Reservoirs (BS-RCRs)*.

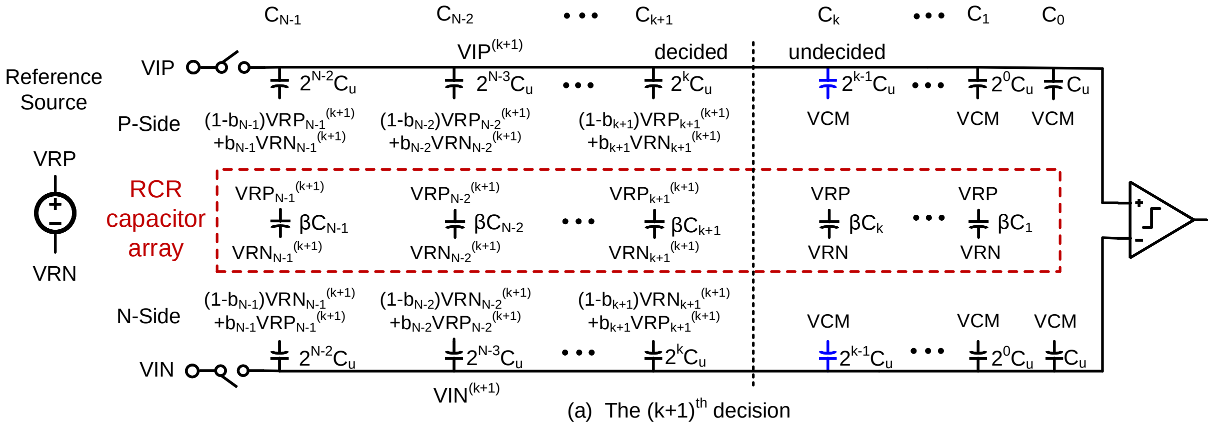
This chapter presents the analysis of bitwise and sample-wise switched passive charge sharing SAR ADCs. It has two major contributions. Firstly, we show theoretically from the principle of charge conservation that for BS-RCRs, the finite reservoir capacitance error appears in the form of bit weight error. For an N-bit binary-weighted SAR ADC, the i-th bit weight error is the bit weight attenuated by $1 + 2^{i+1-N}\beta$ where $i = N-1, \cdots, 1$. This error can be corrected digitally or by selecting a sufficiently large β. We also show that a binary-weighted SAR-ADC with bitwise switched charge reservoirs is essentially being transformed to a sub-radix-2 ADC. On the contrary, for SS-RCR, we show that the finite reservoir capacitance error appears not in the form of bit weight error, and is highly input dependent. An SS-RCR based SAR-ADC exhibits the sub-radix-2 property for some inputs and the super-radix-2 property for some other inputs. The missing level error caused by the super-radix-2 property cannot be corrected.

All the theoretical results derived in this chapter [58] have been validated by running circuit simulation. An 11-bit 100 MS/s SAR-ADC has been designed in 65nm CMOS to evaluate quantitatively the effectiveness of bitwise and sample-wise switching RCR techniques, in particular how β affects the linearity, how large β causes the settling error, and finally to validate the theory developed in this chapter.

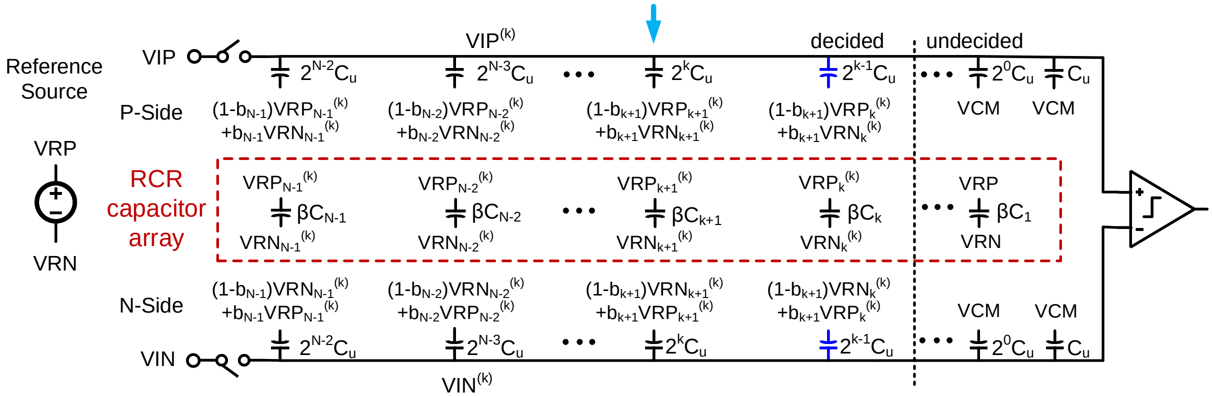
4.2 SAR Switching with Bitwise Reference Charge Reservoirs

4.2.1 VCM-based Merged Capacitor Switching

Merged capacitor switching (MCS) [43] is one of the most energy-efficient SAR-ADC bit decision methods. An N-bit SAR-ADC converts a pair of differential analog input voltages VIP and VIN with the common mode VCM to an N-bit binary codes $b_{N-1}, b_{N-2}, \cdots, b_k, \cdots, b_1, b_0$,



(a) The $(k+1)^{th}$ decision



(b) The $(k)^{th}$ decision

Figure 4.1: An N-bit BS-RCRs based SAR-ADC with top-plate sampling from the $(k+1)^{th}$ decision (a) to the k^{th} decision (b).

where bit b_i can be 0 or 1. Initially, VIP and VIN are sampled on the top plates of two (P-side and N-side) binary-weighted arrays of *bit capacitors* with capacitances $2^{N-2}C_u$, $2^{N-3}C_u, \cdots$, 2^iC_u, $\cdots$, 2^0C_u, C_u where C_u is the unit capacitance. All the bottom plates are connected to reference VCM, the common-mode voltage of high reference VRP (often VDD) and low reference VRN (often GND). The comparator first compares and outputs $b_{N-1} = 1$ if VIP $\geq$ VIN, and 0 otherwise. If $b_{N-1} = 1$ the bottom plate of the P-side (N-side) MSB capacitor is then *switched* to reference VRN (VRP), and otherwise to reference VRP (VRN). As a result of this MSB *bit switching*, the top-plate voltages change to $\text{VIP}^{(\text{N}-1)}$ and $\text{VIN}^{(\text{N}-1)}$.

In general, we use bracketed superfix k to indicate the k-th *bit switching*, $k = N-1$ down to 1. Given the top-plate voltages $\mathrm{VIP}^{(\mathrm{k+1})}$ and $\mathrm{VIN}^{(\mathrm{k+1})}$, the comparator decides b_k. The bottom plate of the P-side bit capacitor is then *switched* to reference $(1-b_k)\mathrm{VRP}+b_k\mathrm{VRN}$, and that of the N side to $(1-b_k)\mathrm{VRN}+b_k\mathrm{VRP}$, as marked in Fig. 4.1. This leads to new top plate voltages $\mathrm{VIP}^{(\mathrm{k})}$ and $\mathrm{VIN}^{(\mathrm{k})}$.

Based on the principle of charge conservation, the top-plate voltages $\mathrm{VIP}^{(k)}$ and $\mathrm{VIN}^{(k)}$ at the $(k)^{th}$ bit decision can be expressed as follows:

$$\mathrm{VIP}^{(k)} = \mathrm{VIP} + \sum_{i=k}^{N-1} \frac{1}{2^{N-i}}(\frac{1}{2} - b_i)(\mathrm{VRP} - \mathrm{VRN}) \tag{4.1}$$

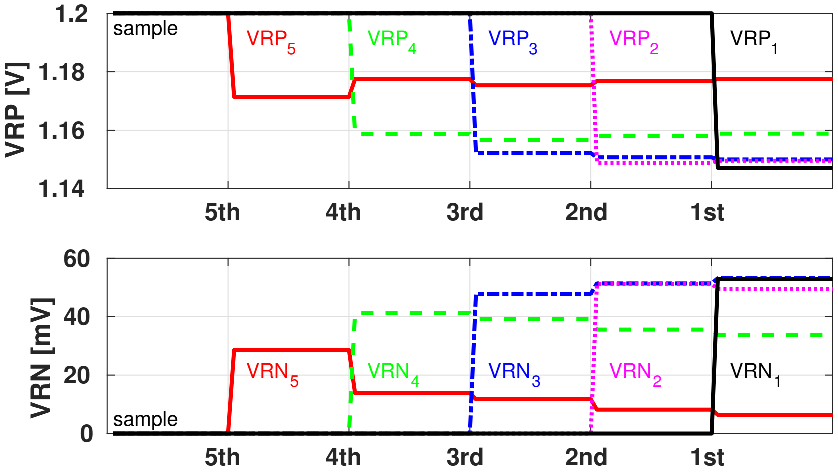
$$\mathrm{VIN}^{(k)} = \mathrm{VIN} + \sum_{i=k}^{N-1} \frac{1}{2^{N-i}}(\frac{1}{2} - b_i)(\mathrm{VRN} - \mathrm{VRP}) \tag{4.2}$$

The SAR-ADC based on the above operation is referred to as *charge redistribution SAR-ADC.*

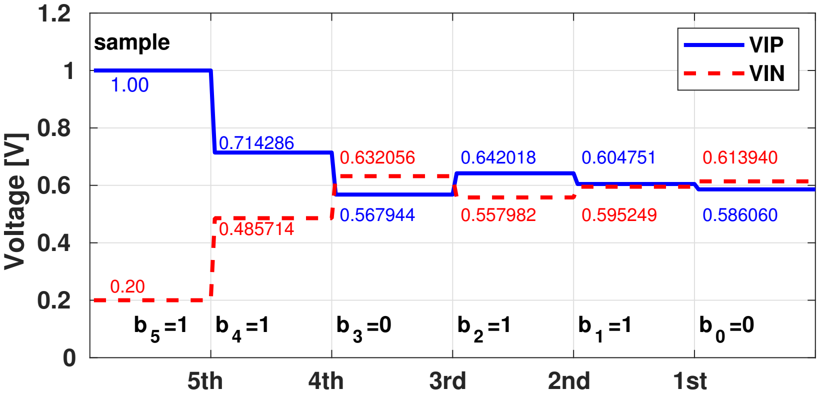
4.2.2 Bitwise-Switched Reference Charge Reservoir

Now consider for each bit decision to replace reference sources VRP and VRN with a capacitor whose top plate precharged to VRP and the bottom plate to VRN. This capacitor serves as a *reference charge reservoir.* Further, the bit reference capacitance is chosen to be β times larger than the corresponding bit weight capacitance. Shown in the middle section in Fig. 4.1 is an array of *bitwise switched ratioed reference charge reservoirs* with capacitances βC_{N-1}, βC_{N-2}, $\cdots$, βC_k, $\cdots$, βC_0, and C_T is the total bit capacitance of C_{N-1} to C_0. Since no reference sources are used for bit decision, this SAR-ADC is referred to as *passive charge sharing SAR-ADC.*

Due to charge sharing, the top and bottom plate voltages of all bit charge reservoir capacitors are not fixed at VRP and VRN. Let VRP_i and VRN_i denote the top-plate and bottom-plate voltages of the i-th bit reservoir capacitor, and $\mathrm{VRP}_i^{(k)}$ and $\mathrm{VRN}_i^{(k)}$ to denote their values at the k-th bit decision step, as shown in Fig. 4.2 (a) for the case of a 6-bit SAR-ADC with $\beta = 5$. Fig. 4.2 (b) shows that the CDAC top-plate voltages deviate from their ideal values $\mathrm{VRP} = 1.2V$ and $\mathrm{VRN} = 0V$.



(a)



(b)

Figure 4.2: CDAC reference voltages (a) and top plate voltage (b) changes at each bit decision of a 6-bit BS-RCR SAR-ADC with $\beta = 5$.

From the principle of charge sharing, as shown in Appendices A and B, the top-plate voltages $\mathrm{VIP}^{(k)}$ and $\mathrm{VIN}^{(k)}$ at the $(k)^{th}$ bit decision can now be represented as follows:

$$\mathrm{VIP}^{(k)} = \mathrm{VIP} + \sum_{i=k}^{N-1} \frac{\alpha^{(i)} C_i}{C_T} (\frac{1}{2} - b_i)(\mathrm{VRP} - \mathrm{VRN}) \tag{4.3}$$

$$\mathrm{VIN}^{(k)} = \mathrm{VIN} + \sum_{i=k}^{N-1} \frac{\alpha^{(i)} C_i}{C_T} (\frac{1}{2} - b_i)(\mathrm{VRN} - \mathrm{VRP}) \tag{4.4}$$

$$\alpha^{(i)} = \frac{2\beta}{2\beta + 1 - \frac{\sum_{j=i}^{N-1} C_j}{C_T}} = \frac{2\beta}{2\beta + (1/2)^{N-i}} \tag{4.5}$$

where the last equality in (4.5) holds if bit capacitances are binary weighted.

Note when $\beta = \infty$, $\alpha^{(i)} = 1$, (4.3) and (4.4) degenerate to (4.1) and (4.2). There is no error with infinite reference charge capacitance. Given finite reservoir capacitance with $\beta \neq \infty$, we have $0 < \alpha^{(i)} < 1$. Further $\alpha^{(i)}$ increases from the MSB ($i = N-1$) to the LSB ($i = 1$). Fig. 4.3 shows $\alpha^{(i)}$ at each bit decision of an 11-bit BS-RCR-based SAR-ADC with $\beta = 16$.

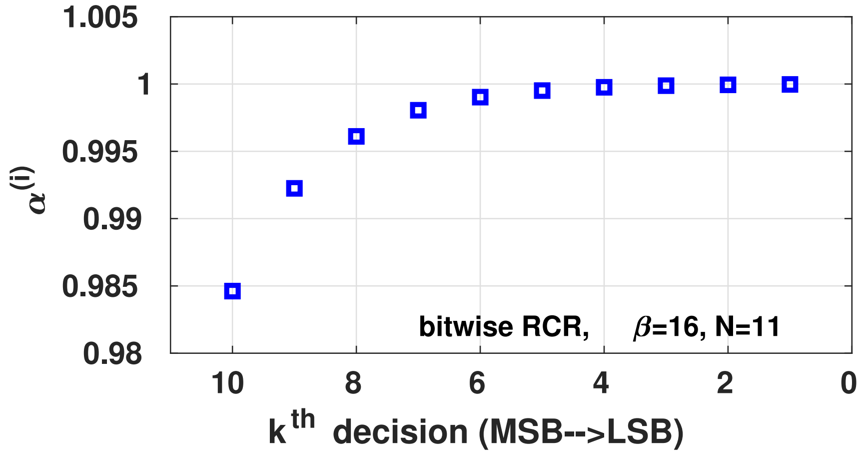


Figure 4.3: $\alpha^{(i)}$ at each bit decision of an 11-bit BS-RCR SAR-ADC with $\beta = 16$.

4.2.3 Transfer Function and Digital Error Correction

By subtracting (4.4) from (4.3) with the left hand side of the equation truncated to zero; i.e., less than 0.5 LSB, we obtain the transfer function of a BS-RCR-based SAR-ADC as follows:

$$\mathrm{V}_{\mathrm{in,diff}} = \sum_{i=1}^{N-1} \alpha^i \frac{C_i}{C_T}(2b_i - 1)(\mathrm{VRP} - \mathrm{VRN}) \tag{4.6}$$

We observe that the ratio of two consecutive bit weights has the following property

$$1 < \frac{\alpha^i C_i}{\alpha^{i-1} C_{i-1}} = \frac{2\beta + (1/2)^{N-i+1}}{2\beta + (1/2)^{N-i}} * 2 < 2 \tag{4.7}$$

With $\mathrm{VRP} - \mathrm{VRN}$ known as the full scale (FS) (analog) voltage $\mathrm{V_{FS}}$ and binary-weighted bit capacitances, (4.6) represents a sub-radix-2 expansion, also known as β-expansion, of a real number [59]. Thus a binary-weighted SAR-ADC implemented with bitwise charge reservoirs is a sub-radix-2 ADC [60]. In fact, as long as $\alpha^{(i)}$ increases from the MSB ($i = N - 1$) to the LSB ($i = 1$) then it is a sub-radix-2 conversion. On the other hand, if $\alpha^{(i)}$ decreases from the MSB ($i = N - 1$) to the LSB ($i = 1$), it is a *super-radix-2* conversion.

As an example, the transfer functions of a 6-bit BS-RCR-based SAR-ADC with $\beta = 0.5$ and $\beta = 5$ are shown in Fig 4.4. The transfer curve for $\beta = 5$ is almost ideal. The transfer curve for $\beta = 0.5$ deviates from the ideal transfer curve expanding around the middle input (differential input = 0), and reaching the maximum close to the two input ends (±FS). This exhibits the *gain* error. As a result, the effective analog input range is reduced from the full scale. Let the *full digital scale* to be the range of from code 0000 0000 000 to 1111 1111 111. Around the values of 1/2, 1/4, 3/4 of the full digital scale, where one analog input is mapped into more than one digital output codes. In terms of analog to digital conversion, some digital codes are missing, exhibiting the *missing code* error. For a given N, both the possibility of missing code occurrence and the magnitude of gain error increase with the smaller β.

Note that this BS-RCR induced error appears in the form of *bit weight* error from (4.3) and (4.4). This error can be predicted based on the given value of β and resolution of the ADC N based on (4.5). Therefore, it can be corrected based on the digital calibration through (4.8)

$$D_{out} = \sum_{i=0}^{N-1} b_i \cdot 2^i \cdot \alpha^{(i)} \tag{4.8}$$

Here $\alpha^{(i)}$ is given in (4.5). The product of $2^i \cdot \alpha^{(i)}$ represents the *actual weights* in the comparison for a binary weighted CDAC.

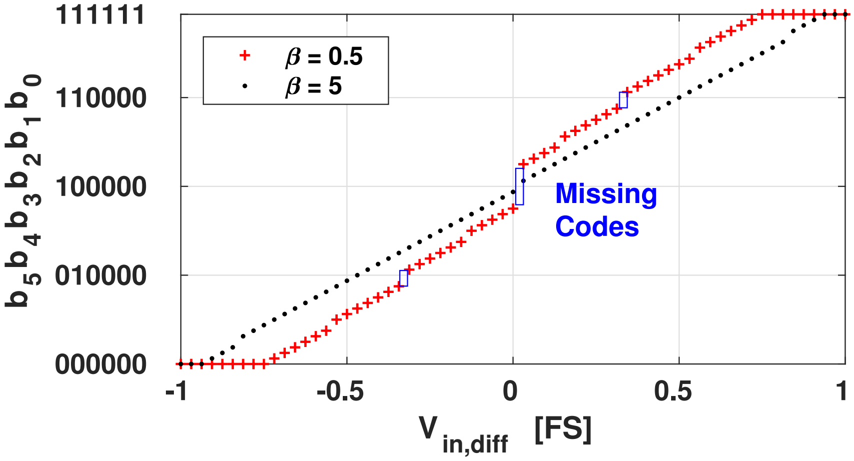


Figure 4.4: B_{out} versus $V_{in,diff}$ of a 6-bit BS-RCRs based SAR-ADC.

4.2.4 Error Control by Selecting Sufficiently Large β

Since $1 - \alpha^{(i)}$ is always positive, the maximal linearity error ε^{max} for an N-bit SAR-ADC due to finite β can be expressed as

$$|\varepsilon^{max}| = \sum_{i=1}^{N-1} \frac{C_i}{C_T}(1 - \alpha^{(i)})(\mathrm{VRP} - \mathrm{VRN}) \tag{4.9}$$

With a binary-weighted bit capacitor array, C_i/C_T can be simplified to $2^i/2^N = 1/2^{N-i}$.

To control the linearity error ϵ^{max} to be less than 0.5 LSB requires

$$\sum_{i=1}^{N-1} \frac{1-\alpha^{(i)}}{2^{N-i}} \approx \sum_{i=1}^{N-1} \frac{(1/2)^{N-i}}{2\beta \cdot 2^{N-i}} \leq \frac{1}{2^{N-1}} \tag{4.10}$$

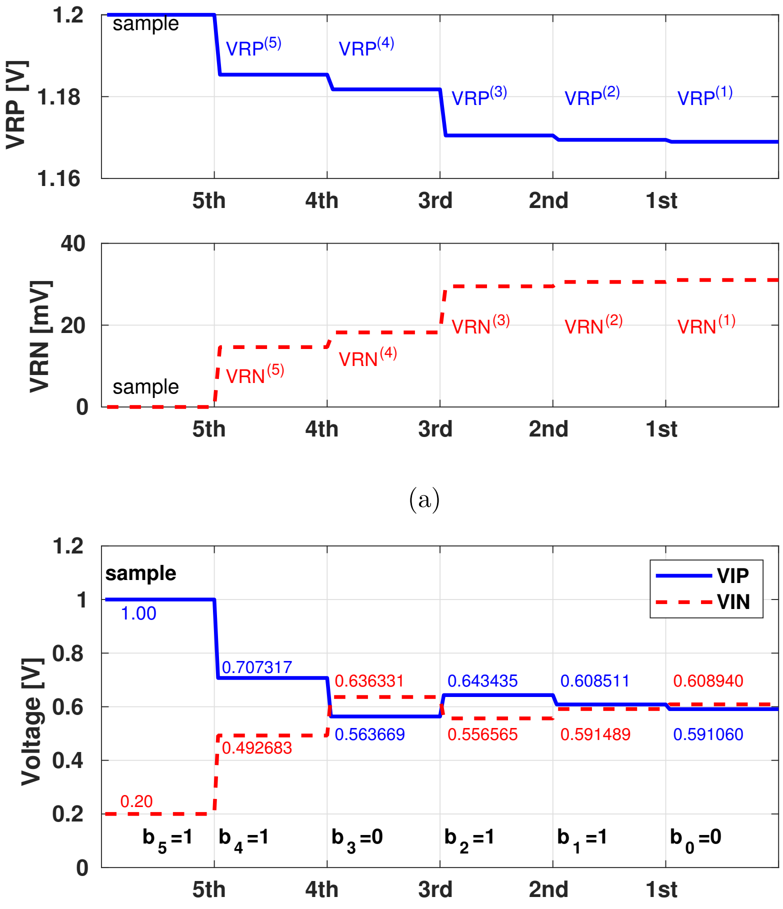
Solving this, we obtain

$$\beta \geq \frac{2^{N-1}[1-(1/4)^{N-1}]}{6} \tag{4.11}$$

Table 4.1 shows the minimal βs for an N-bit SAR-ADC with DNL $\leq$ 0.5 LSB. It has been verified through simulation. It is interesting to note that for a 2-bit or 3-bit SAR-ADC a reference reservoir capacitance can be a fraction of the corresponding bit weight capacitance without degrading the linearity.

Table 4.1: The Minimum β of An N-bit BS-RCRs Based SAR-ADC That Meets DNL $\leq$ 0.5LSB Without Digital Calibration

N	1	2	3	4	5	6	7	8	9	10	11	12
β	0	1/4	5/8	$1\frac{5}{16}$	$2\frac{21}{32}$	$5\frac{21}{64}$	$10\frac{85}{128}$	$21\frac{85}{256}$	$42\frac{341}{512}$	$85\frac{341}{1024}$	$170\ \frac{1365}{2048}$	$341\frac{1365}{4096}$



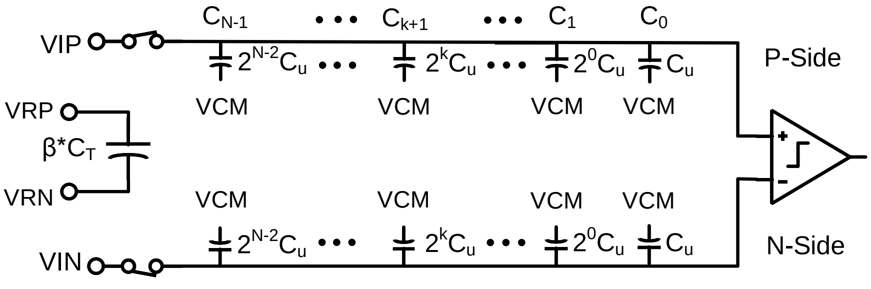
(a)

(b)

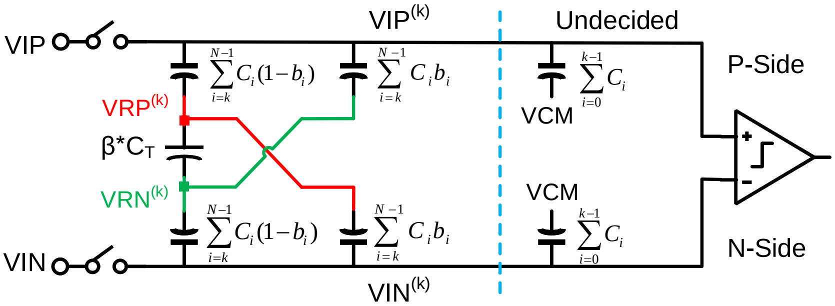
Figure 4.5: CDAC reference voltage (a) and top plate voltage changes (b) at each bit decision of a 6-bit SS-RCR based SAR-ADC with $\beta = 5$.

4.3 SAR Switching with Sample-wise Switched Reference Charge Reservoir

Instead of bitwise, if all charge reservoir capacitors are connected in parallel to form a big capacitor with capacitance $\beta(C_{N-1} + C_{N-2} + \cdots + C_1 + C_0) = \beta C_T$ with the top plate precharged to VRP and the bottom plate to VRN. This is the *sample-wise* switched charge reservoir introduced in [54]. Fig. 4.5 illustrates the waveforms of VRP$^{(k)}$, VRN$^{(k)}$, VIP$^{(k)}$ and VIN$^{(k)}$ for the case of a 6-bit SAR-ADC with $\beta = 5$. Compared with a 6-bit BS-RCR-based SAR ADC with $\beta = 5$, both the reference voltages and CDAC top-plate voltages are different from the ones in Fig. 4.2.



(a) Sampling Phase



(b) The (k)th decision

Figure 4.6: An N-bit SS-RCR based SAR-ADC with top-plate sampling.

In general, consider sample-wise reference switching at the $(k)^{th}$ decision as illustrated in Fig. 4.6 (b). From the principle of charge conservation, the analytic expressions of top-plate voltages for sample-wise switching at the $(k)^{th}$ bit decision can be derived as shown in

Appendix C and be written in the same form as (4.3) and (4.4) but with $\alpha^{(i)}$ re-defined by (4.12).

$$\alpha_{\text{sample-wise}}^{(\text{k})} = \frac{2\beta}{2\beta + \frac{\sum\limits_{i=k}^{N-1} C_i}{C_T} - [\frac{\sum\limits_{i=k}^{N-1} C_i(2b_i - 1)}{C_T}]^2} \tag{4.12}$$

We note that when $\beta = \infty$, $\alpha = 1$. For finite β, $0 < \alpha^{(k)} < 1$, and $\alpha^{(k)}$ are functions of β and N.

In contrast to bitwise $\alpha^{(k)}$ as shown in (4.5), sample-wise $\alpha^{(k)}$ depend on $b_i, i = N - 1, ..., k$; i.e., the *previous* more significant bits that have been decided. In fact the *cross* term $\sum\limits_{i=k}^{N-1} C_i(2b_i - 1)$ in (4.12) is the total capacitance of those previous bit capacitances connecting to reference plate VRN minus that of those connecting to reference plate VRP as shown in Fig. 4.6 (b). The error caused by the finite charge reservoir capacitance is thus highly nonlinear, and no longer in the form of the bit weight error. Further, it does not represent a sub-radix-2 expansion of a real number and an SS-RCR based binary-weighted SAR-ADC is not a sub-radix-2 ADC.

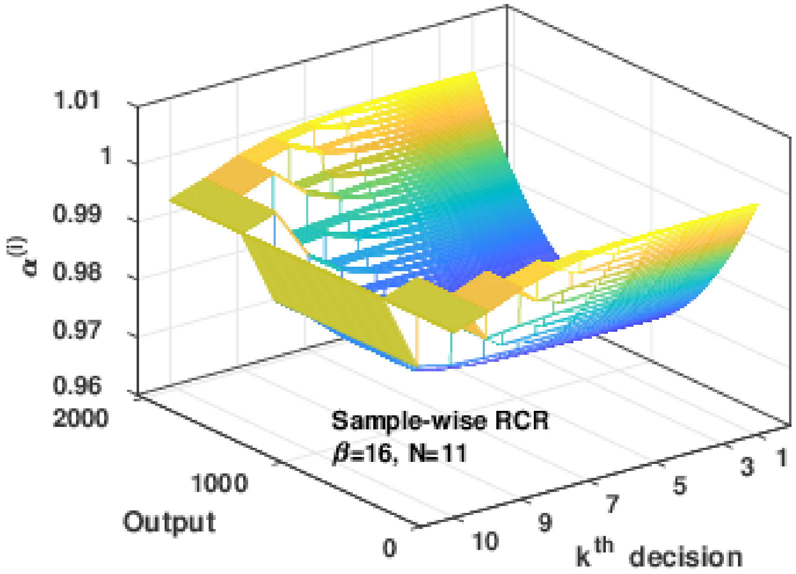


Figure 4.7: $\alpha^{(i)}$ at each bit decision of an 11-bit SS-RCR based SAR-ADC with $\beta = 16$.

Fig. 4.7 shows $\alpha^{(\mathrm{k})}_{\mathrm{sample-wise}}$ of an 11-bit SS-RCR based SAR-ADC with $\beta = 16$. For $\alpha^{(10)}_{\mathrm{sample-wise}}$, there is no previous bit. So there is only one value of $\alpha^{(10)}_{\mathrm{sample-wise}}$. For $\alpha^{(9)}_{\mathrm{sample-wise}}$, the previous bit b_{10} has two possible values 0 or 1, so is $\alpha^{(9)}_{\mathrm{sample-wise}}$ due to the term $[\sum_{i=9}^{10} C_i(2b_i - 1)]^2$ in (4.12). There are 2^9 possible values of $\alpha^{(1)}_{\mathrm{sample-wise}}$. The strong input dependency can be clearly seen by comparing Fig. 4.3 with Fig. 4.7 (a), as further shown in Fig. 4.7 (b).

One important characteristic of $\alpha^{(\mathrm{k})}_{\mathrm{sample-wise}}$ is its trend in terms of decision steps $(k)^{th}$ from the MSB to the LSB. As further shown in Fig. 4.7 (c), at the two ends of the codes (all 0s, all 1s), $\alpha^{(\mathrm{k})}_{\mathrm{sample-wise}}$ increases from the MSB to the LSB. Thus sample-wise reference switching behaviors as a sub-radix-2 conversion like bitwise reference switching. Near the middle code 10000000000, $\alpha^{(\mathrm{k})}_{\mathrm{sample-wise}}$ decreases from the MSB to the LSB. In this case, sample-wise reference switching behaviors as a super-radix-2 conversion.

As an example, the transfer functions of a 6-bit SS-RCR based SAR-ADC with $\beta = 0.5$ and $\beta = 5$ are plotted in Fig. 4.8. The transfer curve for $\beta = 5$ is almost ideal. Similar to that of bitwise reference switching, the transfer curve for $\beta = 0.5$ deviates from the ideal transfer curve expanding around the middle input point 1/2 of the full digital scale, and reaching the maximum close to the two input ends. This exhibits the *gain* error. Around the values of 1/8, 1/4, 7/8, and 3/4 of the full digital scale, one analog input is mapped into more than one digital output codes. In terms of analog to digital conversion, some digital codes are missing, exhibiting the *missing code* error.

Different from bitwise reference switching transfer curves shown in Fig. 4.4, sample-wise reference switching transfer curves shown in Fig. 4.8 show *missing analog level* errors; i.e., there exist multiple analog inputs transferred into the same digital code. *Unlike the gain error and missing code error, the missing level error cannot be corrected.*

4.4 A Case Study of An 11-bit SAR-ADCs: Behavioral and Schematic Levels

An 11-bit 100MS/s SAR-ADC has been designed in 65nm CMOS to evaluate quantitatively the effectiveness of bitwise and sample-wise switching reference charge reservoir techniques,

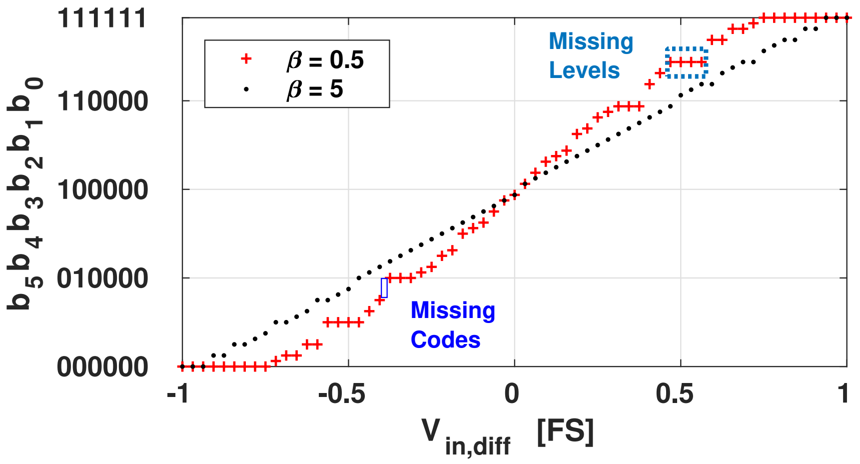


Figure 4.8: B_{out} versus $V_{in,diff}$ of a 6-bit SS-RCR based SAR-ADC with $\beta = 0.5$ and $\beta = 5$.

in particular how β affects the linearity, and to validate the theory developed in this paper.

4.4.1 SAR-ADC Architecture and Schematic Design

The ADC is implemented in the differential architecture shown in Fig. 4.9. Capacitive digital to analog converters (CDACs) are binary weighted from C_u to $2^9 * C_u$, where C_u is the unit capacitance. The reference charge reservoir capacitors are also binary weighted with capacitance β times larger than its bit capacitance. Bottom-plate sampling is used so that the ADC linearity is immune to the top-plate parasitic capacitance.

The ADC then uses VCM-based merged capacitor switching described in Section 4.2.2 to decide bits from the MSB to the LSB. Either bitwise or sample-wise switching reference charge reservoir technique is employed. The ADC uses a two-stage comparator with a dynamic preamplifier to suppress the kickback noise and latch offset [61]. A 25% duty-cycle 100 MHz is used with 25% for sampling and 75% for SAR bit decision. The SAR logic is asynchronous [62] and is the same as [42].

For comparison, an ideal 11-bit SAR-ADC is built out of this schematic ADC with capacitors, switches, comparators, delay line, and digital gates replaced by ideal elements.

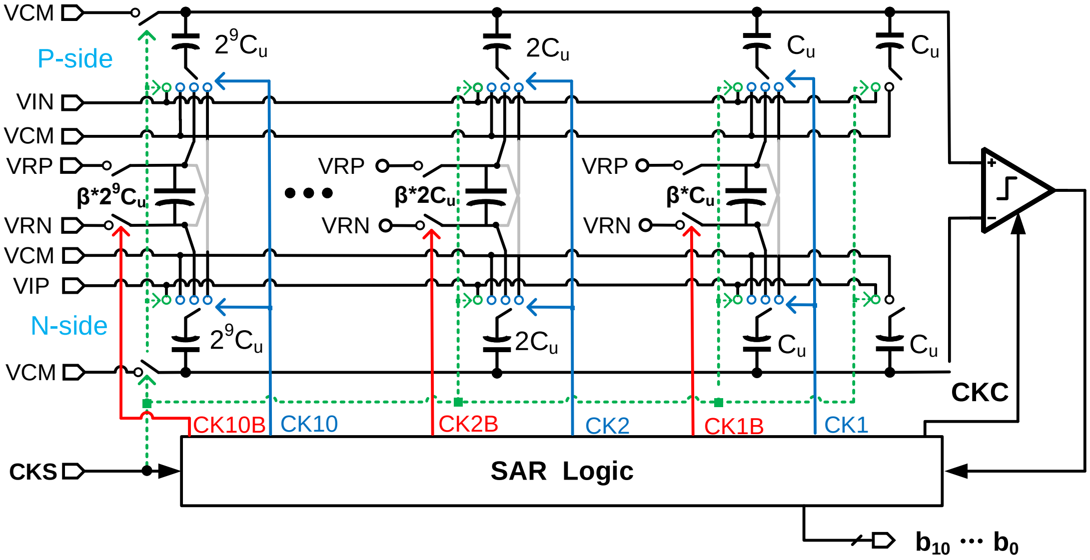


Figure 4.9: An 11-bit SAR-ADC architecture with BS-RCRs.

The linearity of the ideal ADC and schematic-level ADC are simulated using the same test benches with the same settings.

4.4.2 Effect of β on Linearity

A pair of differential input ramp signals with step 0.1 LSB are applied to obtain the static performances. A pair of differential input sinusoidal signals are applied, transient simulation was performed to obtain the dynamic performances. The performances computed include differential nonlinearity (DNL), integral nonlinearity (INL), signal to noise distortion ratio (SNDR), spurious free dynamic range (SFDR), and effective number of bits (ENOB).

Tables 4.2 and 4.3 summarize, respectively, the simulated static and dynamic performances of ideal 11-bit SAR-ADCs with BS-RCRs and SS-RCR with different βs. These have been verified to be the same as those obtained using analytic expressions (4.3), (4.4), (4.5), and (4.12). From Table 4.2, the linearity loss is less than 0.5LSB when $\beta = 256$. When β decreases to 32, the ENOB loss is 1.8 bits. From Tables 4.2 and 4.3, we see that all of the performances of bitwise switching are better than that of sample-wise switching.

Table 4.2: Behavioral Model: Static and Dynamic Performance of An 11-Bit BS-RCRs based SAR-ADC With Different βs

β	32	64	128	256
SNDR(dB)	56.74	61.38	66.70	67.66
ENOB(bits)	9.13	9.90	10.79	10.95
SFDR(dB)	59.26	65.26	72.58	81.32
DNL(LSB)	-1/0.005	-1/0.0026	-0.7/0	-0.4/0
INL(LSB)	-2.7/2.7	-1.4/1.4	-0.7/0.7	-0.3/0.3

Table 4.3: Behavioral Model: Static and Dynamic Performance of An 11-Bit SS-RCR based SAR-ADC With Different βs

β	32	64	128	256
SNDR(dB)	54.33	59.63	64.62	66.33
ENOB(bits)	8.74	9.61	10.44	10.73
SFDR(dB)	54.54	60.23	67.41	71.86
DNL(LSB)	-1/3.6	-1/1.9	-1/1	-0.5/0.5
INL(LSB)	-3.1/3.1	-1.6/1.6	-0.8/0.8	-0.4/0.4

Tables 4.4 and 4.5 summarize the simulated static and dynamic performances of the 11-bit SAR-ADC schematic design with BS-RCRs and SS-RCR with different βs, respectively. In simulation, circuit nonideal effects including clock feedthrough and charge injection introduced by MOS transistor switches as well as kickback noise from comparator and transient effects are included. Comparing Table 4.4 with Table 4.2, the ENOB loss due to circuit non-

Table 4.4: Schematic Model: Static and Dynamic Performance of an 11-Bit BS-RCRs based SAR-ADC With Different βs

β	32	64	128	256
SNDR	56.56	61.16	66.54	67.58
ENOB	9.10	9.87	10.76	10.93
SFDR	58.5	64.74	72.22	81.08
DNL(LSB)	-1/0.008	-1/0.0046	-0.7/0	-0.4/0
INL(LSB)	-2.85/2.85	-1.45/1.45	-0.75/0.75	-0.35/0.35

Table 4.5: Schematic Model: Static and Dynamic Performance of an 11-Bit SS-RCR based SAR-ADC With Different βs

β	32	64	128	256
SNDR	53.55	59.07	64.24	66.14
ENOB	8.60	9.52	10.38	10.69
SFDR	53.52	59.42	66.82	71.45
DNL(LSB)	-1/3.83	-1/1.91	-1/1	-0.5/0.5
INL(LSB)	-3.28/3.28	-1.66/1.66	-0.85/0.85	-0.43/0.43

ideality is less than 0.16 bit for BS-RCR based SAR-ADCs, and the ENOB loss decreases as β increases. Even with circuit nonideality, bitwise switching always has better linearity than sample-wise switching.

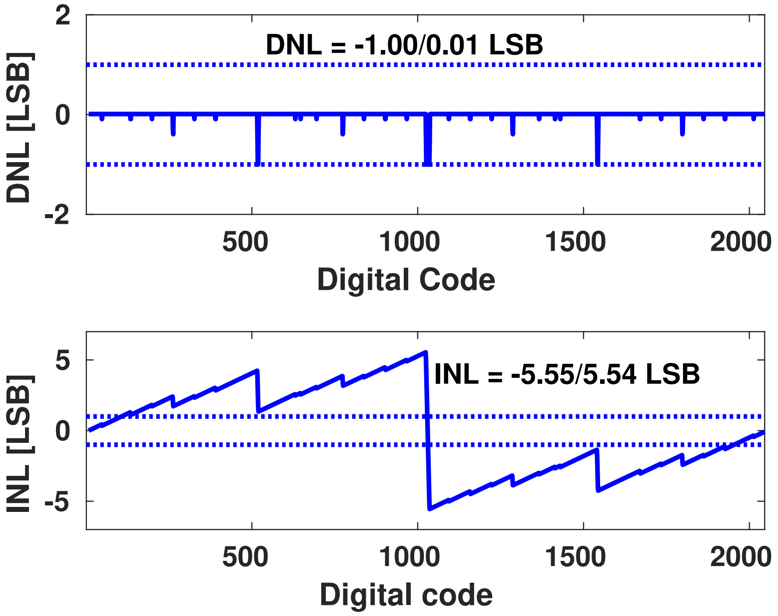
Take $\beta = 16$ for an 11-bit SAR-ADC with $C_u = 1fF$ as an example, we analyze how the sampled thermal noise on RCR capacitors and the mismatch among RCR capacitors affect the performance in both BS- and SS- based SAR ADCs. The sampled thermal noise on RCR capacitors has the form of $\sqrt{kT/C}$. Here k is Boltzmann constant, T is 300 K at room temperature, and C is the RCR capacitance. The sampled thermal noise on BS-RCR capacitor varies from 22.5 μV to 509 μV from the MSB to the LSB, while 15.9 μV thermal noise is sampled on the SS-RCR capacitor. The thermal noise is much less than the error due to charge sharing. Thus, it does not influence the performance in both BS- and SS-based SAR ADCs. Now considering the mismatch among RCR capacitors, the nmoscap is used for the RCR capacitor in the schematic-level implementation. It not only has large capacitance density (14 $fF/\mu\text{m}^2$) at VDD bias but also can be laid out beneath the CDAC to save the area. The 1-σ mismatch of a 16.8 fF nmoscap is 1.875e-17 through Monte Carlo simulation. Apply this 1-σ mismatch to all the RCR capacitors, the dynamic performance does not deteriorate in both BS- and SS- based SAR ADCs.

4.4.3 Linearity Performance with Small β and Error Correction

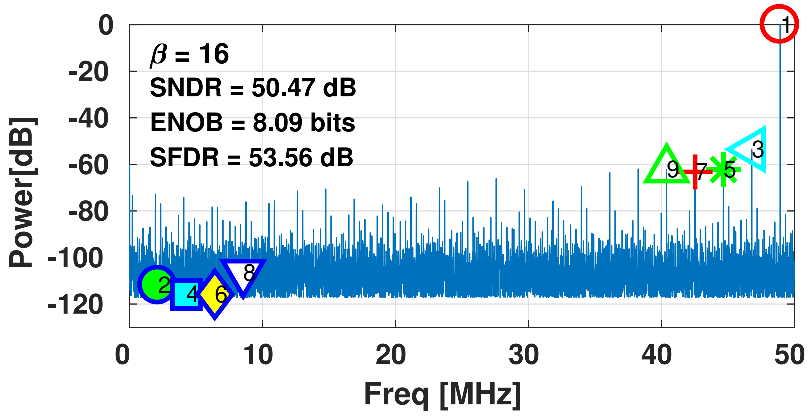
Now we show quantitatively the ADC linearity with relatively small β and the effectiveness of error correction. For $\beta = 16$, the simulated DNL and INL and dynamic spectrum performance are shown in Fig. 4.11 for a BS-RCR -based SAR-ADC. The maximal DNL error of -1 occurs near the 1/2, 1/4 and 3/4 of the full digital scale, which means missing codes at these digits. Dynamic performance shows more than 2.91-bits of resolution loss when $\beta = 16$ for an 11-bit SAR-ADC.

Fig. 4.11 shows the simulated static and dynamic performances of an 11-bit SAR-ADC with SS-RCR that has $\beta = 16$ (the total reservoir capacitance is the same as that of BS-RCRs). It can be seen that the maximum DNL is -1/7.59 LSB, much worse than that of the bitwise case. It shows both missing codes (DNL = -1 LSB) and missing levels (DNL $\geq$ 1 LSB) occure at different inputs. In particular we note that sample-wise DNL is 0 near the middle codes. This is because the super-radix-2 operation near the middle input.

After digital error correction according to (4.8), the static and dynamic performances of an 11-bit BS-RCR based SAR-ADC with $\beta = 16$ are shown in Fig. 4.12. We can see that



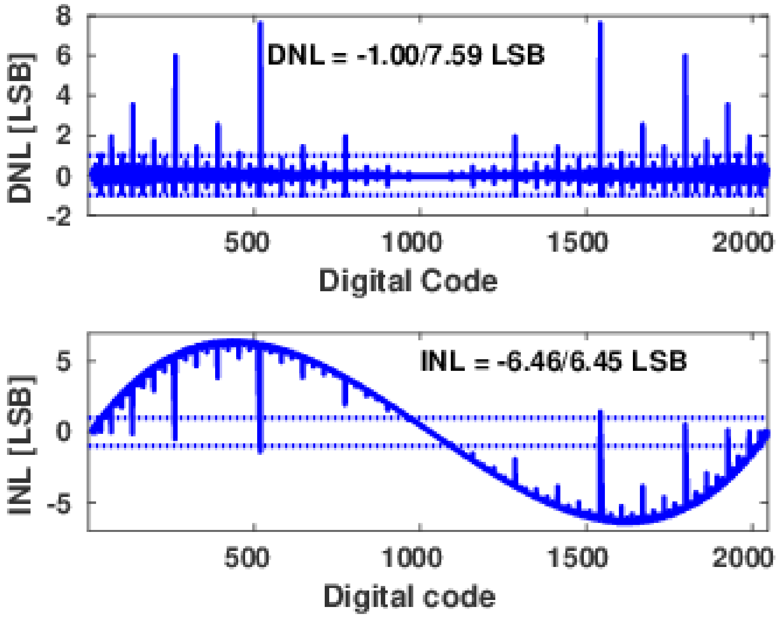
(a) The static DNL/INL performance.



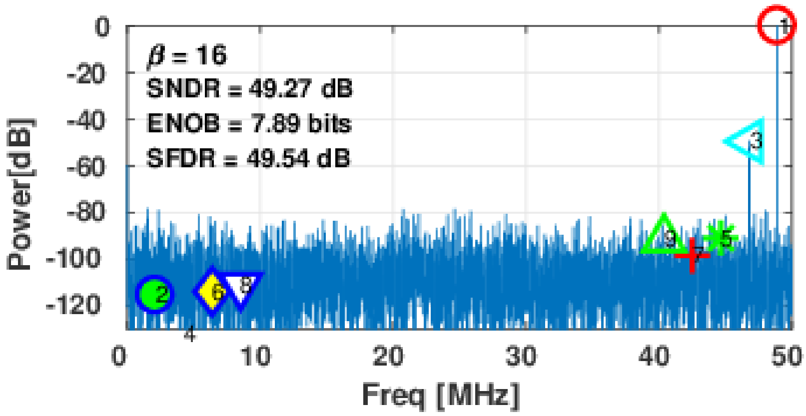
(b) The dynamic performance.

Figure 4.10: Simulated performance of an 11-bit SAR-ADC with bitwise switched RCRs @ $\beta = 16$.

the DNL and INL are both smaller than 0.55 LSB, and the ENOB can reach to 10.65 bit after error correction.



(a) The static DNL/INL performance.

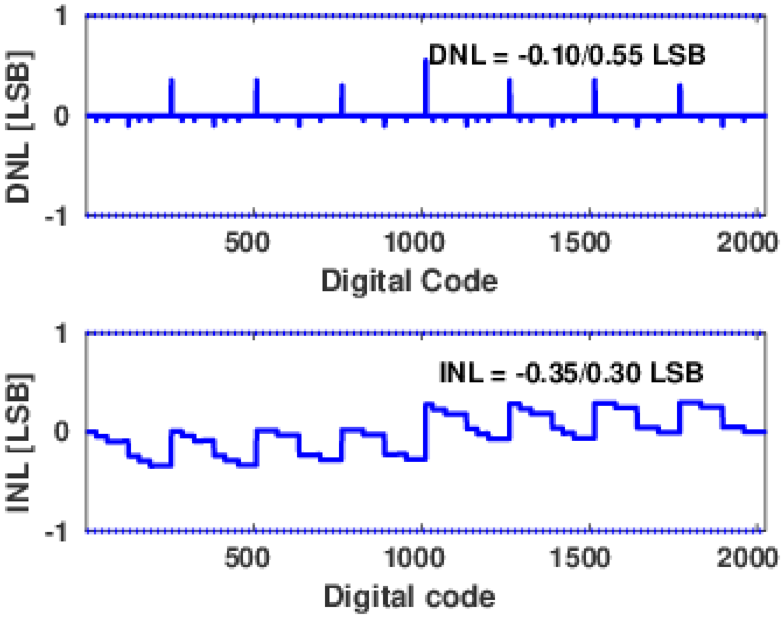


(b) The dynamic performance.

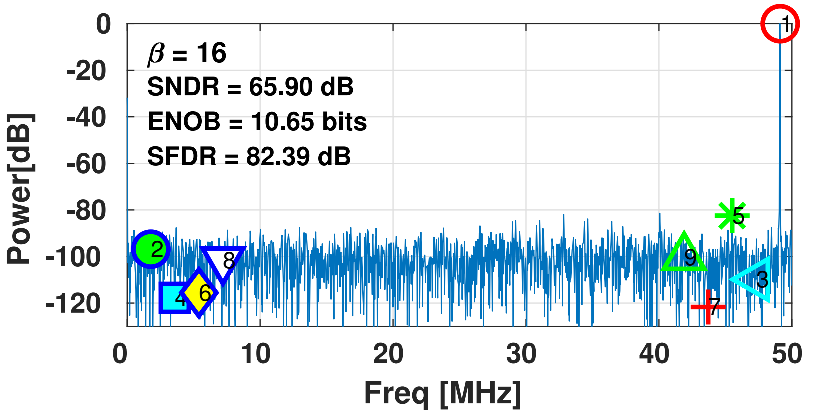
Figure 4.11: Simulated performance of an 11-bit SAR-ADC with a sample-wise switched RCR @ $\beta = 16$.

4.5 Conclusion

This chapter presented the analysis of an energy-efficient bitwise switched ratioed charge reservoir (BS-RCR) technique for reference-buffer-free SAR-ADC design. Complete theo-



(a) The static DNL/INL performance.



(b) The dynamic performance.

Figure 4.12: Simulated performance of an 11-bit SAR-ADC with bitwise switched RCRs @ $\beta = 16$ after digital error correction.

retical analysis and simulation have been performed to analyze the error due to the finite reference capacitances. It is shown that the reference error in a SAR-ADC with BS-RCRs is in the form of bit weight error, causing the gain and missing code errors, and can be digitally corrected precisely or be eliminated by using a sufficiently large β.

We have shown that a SAR-ADC with bitwise charge reservoirs is essentially a sub-radix-2 ADC. Future work includes to explore this sub-radix-2 redundancy for error correction.

The reference error for the previously published sample-wise switched reference charge reservoir (SS-RCR) technique has also been analyzed. It is shown that the SS-RCR error exhibits both the super-radix-2 and sub-radix-2 properties depends on inputs. In addition to exhibiting the gain and missing code errors, the SS-RCR technique shows the missing level errors, which cannot be corrected.

All the analyses have been validated and demonstrated using a 11-bit RCR-based SAR-ADC. Quantitative evaluation of β on ADC linearity has been presented. The effectiveness of error correction for small β has been demonstrated.

Chapter 5

DESIGN AND ANALYSIS OF PASSIVE CHARGE SHARING IN SEGMENTED SAR ADCS

5.1 Introduction

In Chapter 4, we have analyzed the reference error, which appears in the bit weight error, in a successive approximation ADC with merged capacitor switching (MCS) using either bitwise or sample-wise reference charge reservoir (RCR) [58]. To decrease the MSB associated switching energy, segmented SAR ADC was introudced [44] in 2014. In which it comprises a coarse SAR to compute several MSBs and a fine SAR ADC that loads the results from coarse SAR ADC and then computes the rest of the LSBs. The RCR technique presented in Chapter 4 can also apply to a segmented SAR ADC. However, the reference error due to finite reference charge in the fine SAR ADC is different from the one in the successive approximation ADC. Even [57] presented the analysis, design and measurement results of a 16-bit 16 MS/s SAR ADC with bitwise RCRs in 55nm CMOS. There is no closed form of expression of how the RCR capacitance to the bit capacitance ratio β affects the performance. On the other hand, the analysis of charge sharing between the bit capacitor and its RCR capacitor is different in successive switching(SS), aligned switching(AS), and detect-and-ship aligned switching (DAS-AS) within a segmented SAR ADCs.

This chapter presents the analysis, design, and implementation of RCR-based segmented SAR-ADCs. Theoretically, we have derived the analytic formula of the reference error for various RCR-based segmented SAR-ADC switching schemes. We have proved that successive decisions using bitwise RCRs and fine MSB switching using DAS-AS subsample-wise RCR yields the near smallest reference error while saving most switching energy. Therefore, it is adopted in our 11-bit segmented SAR-ADC silicon prototype. An 11-bit 25 MS/s

SAR ADC has been implemented in 65 nm CMOS. It consumes 240 μW with a FoM of 11.8 fJ/conversion-step including 70 μW used by reservoir drivers.

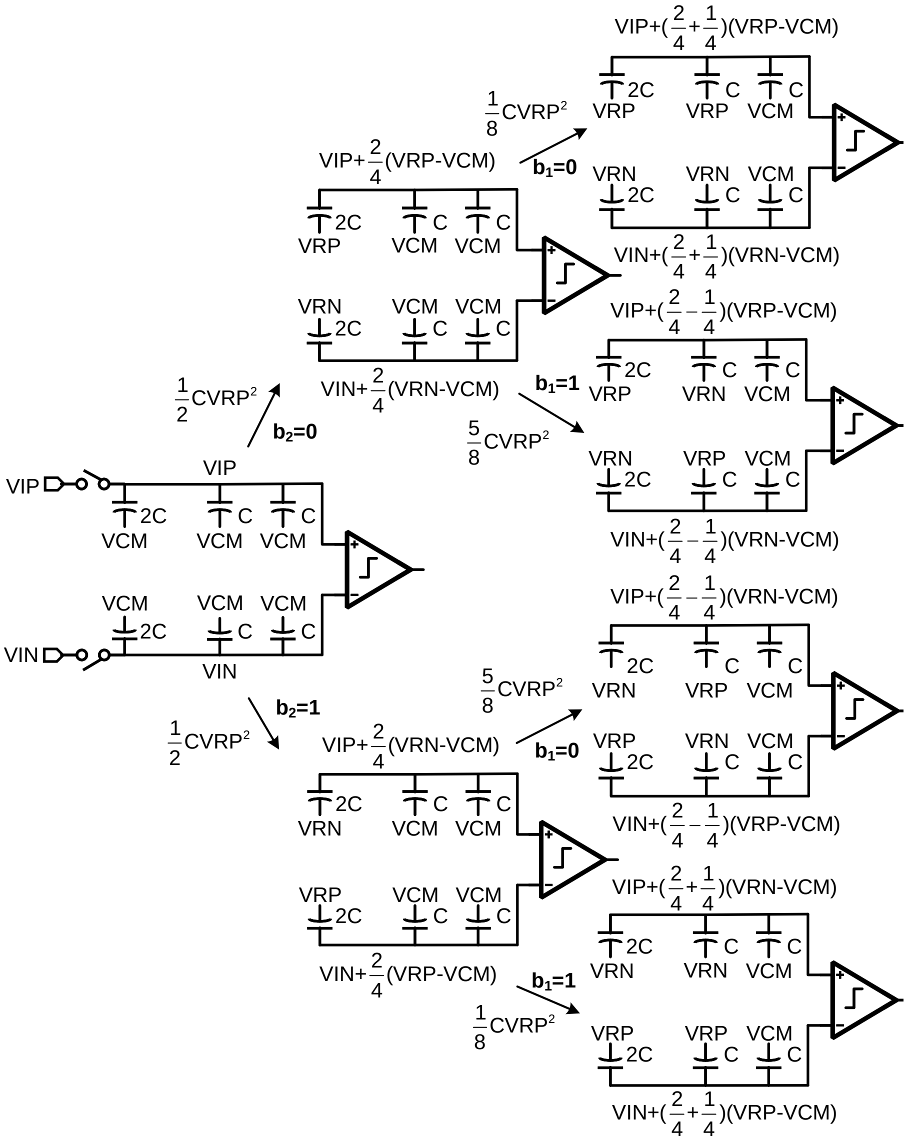
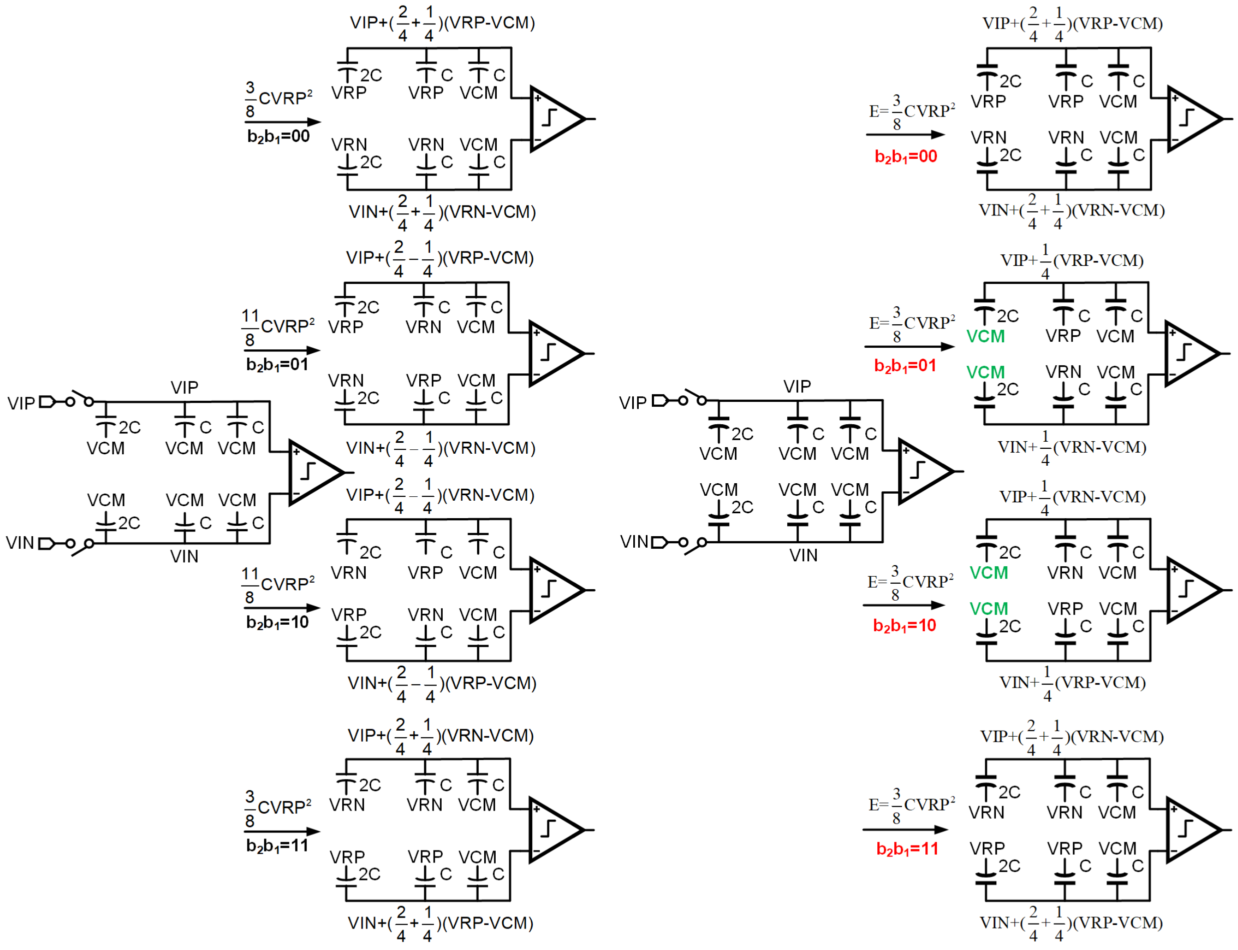


Figure 5.1: Three bit charge redistribution CDAC successive switching (SS) example.

5.2 *Charge Redistribution and Charge Sharing based SAR ADCs*

In this section, a 3-bit SAR ADC is used to illustrate three switching methods: SS, AS, and DAS-AS, and their switching energy consumption. First, reference sources are used for CDAC; this is the *charge-redistribution* SAR ADC. We then replace reference sources with precharged capacitors, known as *reference charge reservoirs*; this leads to the *passive charge-sharing* SAR-ADC.



(a) Aligned Switching (AS)

(b) Detect-and-sckip, Aligned Switching (DAS-AS)

Figure 5.2: Three bit charge redistribution CDAC AS and DAS-AS examples.

5.2.1 Charge-Redistribution SAR-ADC Switchings

Figure 5.1 illustrates the operation of a 3-bit binary-weighted differential charge-redistribution SAR ADC using merged capacitor successive switching [43]. Two reference levels are VRP (high, often VDD) and VRN (low, often GND) with the common mode voltage VCM = (VRP + VRN)/2. Initially, differential input voltages VIP and VIN are sampled onto the top plates of the p-side and the n-side CDACs, and all bottom plates are connected to VCM. Then, the comparator compares the two top-plate voltages and determines the MSB b_2. The bottom plate of the p-side CDAC MSB bit capacitor is switched to VRN if $b_2 = 1$ otherwise to VRP, while the bottom plate of the N-side MSB bit capacitor switches oppositely to VRP and VRN. In this MSB step, the bit capacitor acts as a *neutralizing* capacitance to move the top-plate voltage towards the common mode by (1/2)(VRP − VCM). The resulting top plate voltages are shown in the figure.

The process continues by comparing the two resulting top-plate voltages to obtain the second MSB, and switch the bottom plates to VRP and VRN accordingly. In case that the second MSB is the opposite of the MSB, i.e., the MSB switching is *over-neutralizing*, Then we will then switch the bottom plate of the second MSB capacitor to the opposite of the MSB (VRP and VRN), this moves the top plate voltage back by (1/4)(VRP-VCM). This is the *opposite switch*. The corresponding bit capacitor acts as an *anti-neutralizing capacitance*. In case of *under-neutralizing*, the second MSB is the same as the MSB, we switch the bottom plate of the second MSB capacitor in the same way as the MSB capacitor, and move the top-plate voltage further by (1/4)(VRP-VCM). This is the same direction switching. The bit capacitor acts as a neutralizing capacitance. For cases of $b_2b_1 = 01$ and 10, there are opposite switchings, and bottom plates of one side of the CDAC can connect to both VRP and VRN.

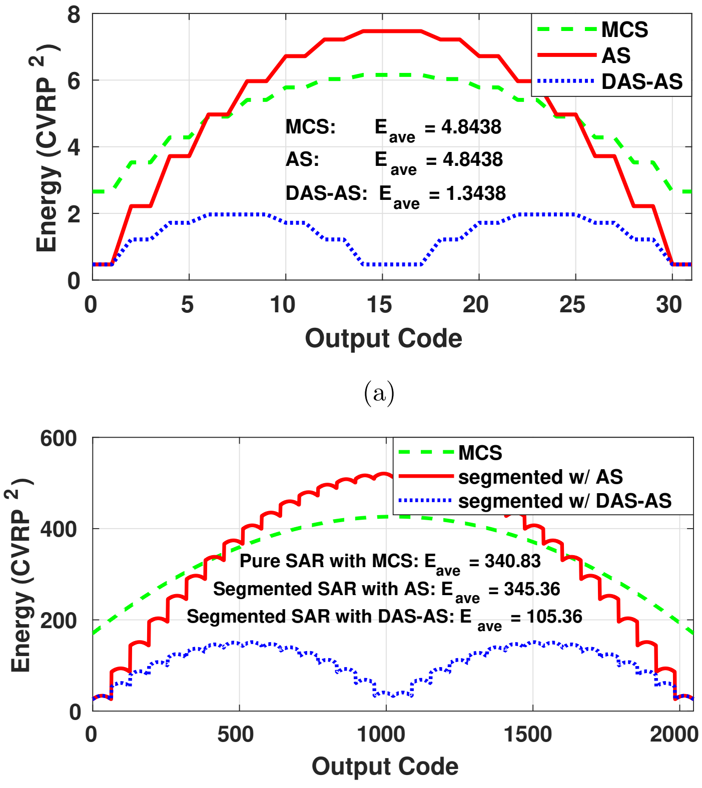
The LSB is finally obtained by comparing the resulting top-plate voltages. Hence a total of four cases of *successive switching* (SS) are shown in Fig. 5.1, where for each switching, the resulting top-plate voltage as well as the energy consumed are marked. Now consider that all digital bits are known, and all the the bottom plates of the 3-bit CDAC are switched simultaneously in one step. The four cases are illustrated in Fig. 5.2 (a). This is referred to as *aligned switching* (AS) [44].

Note that the top-plate voltages are determined by the *net neutralizing capacitance*, which is the total neutralizing capacitance subtracting the anti-neutralizing capacitance:

$$C_{net-sw} = \sum_{i=1}^{N} (2b_i - 1)C_i \tag{5.1}$$

If we are only interested in the final top-plate voltages with aligned switching, opposite switching can be avoided by switching the net neutralizing capacitance. We can represent a neutralizing bit by 1 and an anti-neutralizing bit by -1, then add all bits together. The resulting bits can be shown to be equal to the circular left shift of the original bits, where the bit same as the MSB is to switch and otherwise is to skip (no switch). For example, in case of 100, the resulting net neutralizing capacitance corresponds to number 001. Thus 2C bit switching is skipped; i.e., still connecting VCM, and only the C bit switching from VCM to VRP. This was developed as the detect-and-skip aligned switching (DAS-AS) operation [44]. Fig. 5.2 (b) shows all DAS-AS four cases.

We observe that all the three switching methods yield the same top-plate voltage but differ in energy consumption. The average energy consumed by AS is the same as that of SS. DAS-AS consumes the least energy. Fig. 5.3 (a) plots the switching energy for each code of a 5-bit SAR-ADC. Fig. 5.3 (b) plots the switching energy for each code of an 11-bit segmented SAR-ADC with a 5-bit coarse SAR-ADC. Using SS for the coarse ADC, then use DAS-AS to obtain the MSB for the fine ADC and use the SS to the remaining LSBs in the fine ADC leads to a reduction of switching energy by 69.1% compared with a SAR with SS. Here the coarse unit capacitance is 2 times larger than the fine unit capacitance in the segmented architecture.



(a)

(b)

Figure 5.3: Calculated SAR ADC switching energy. (a) 5-bit SRA ADC with SS, AS, and DAS-AS; (b) An 11-bit SAR ADC in a successive decision only SAR ADC, a segmented SAR ADC with AS, and a segmented SAR ADC with DAS-AS.

5.2.2 Charge-Sharing SAR ADC Switchings

Figure 5.4 and Figure 5.5 (a) (b) show, respectively of the decision process of a 3-bit charge-sharing SAR ADC using SS, AS, and DAS-AS schemes. For each bit decision, the reference sources VRP and VRN are replaced by charge reservoir capacitors β-times larger than the corresponding bit capacitances, precharged to VRP and VRN. This is known as *bitwise*. Figure 5.6 and Figure 5.7 show the decision process of another structure of a 3-bit charge sharing SAR-ADC where all reference capacitors connected in parallel to form a *sample-wise* charge reservoir.

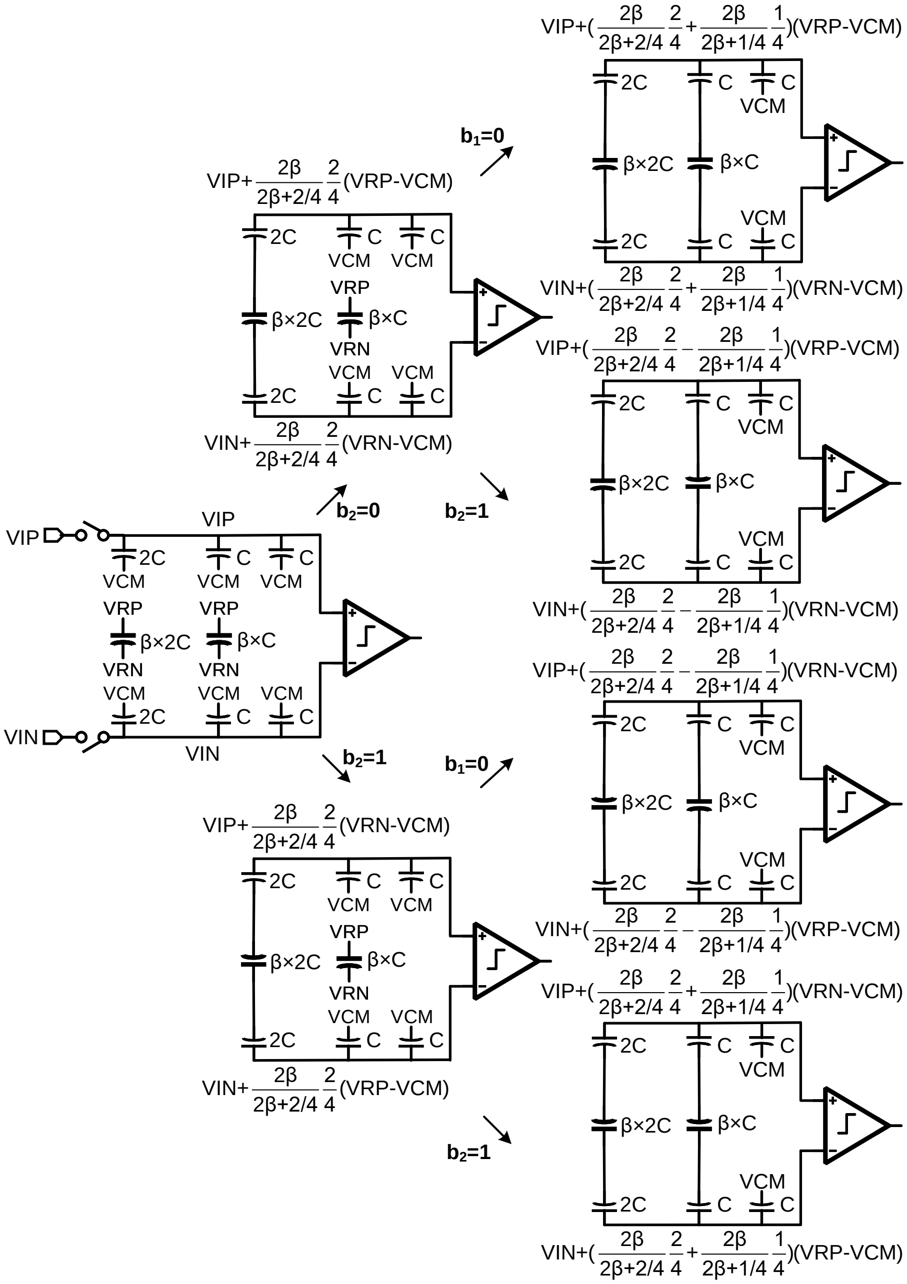
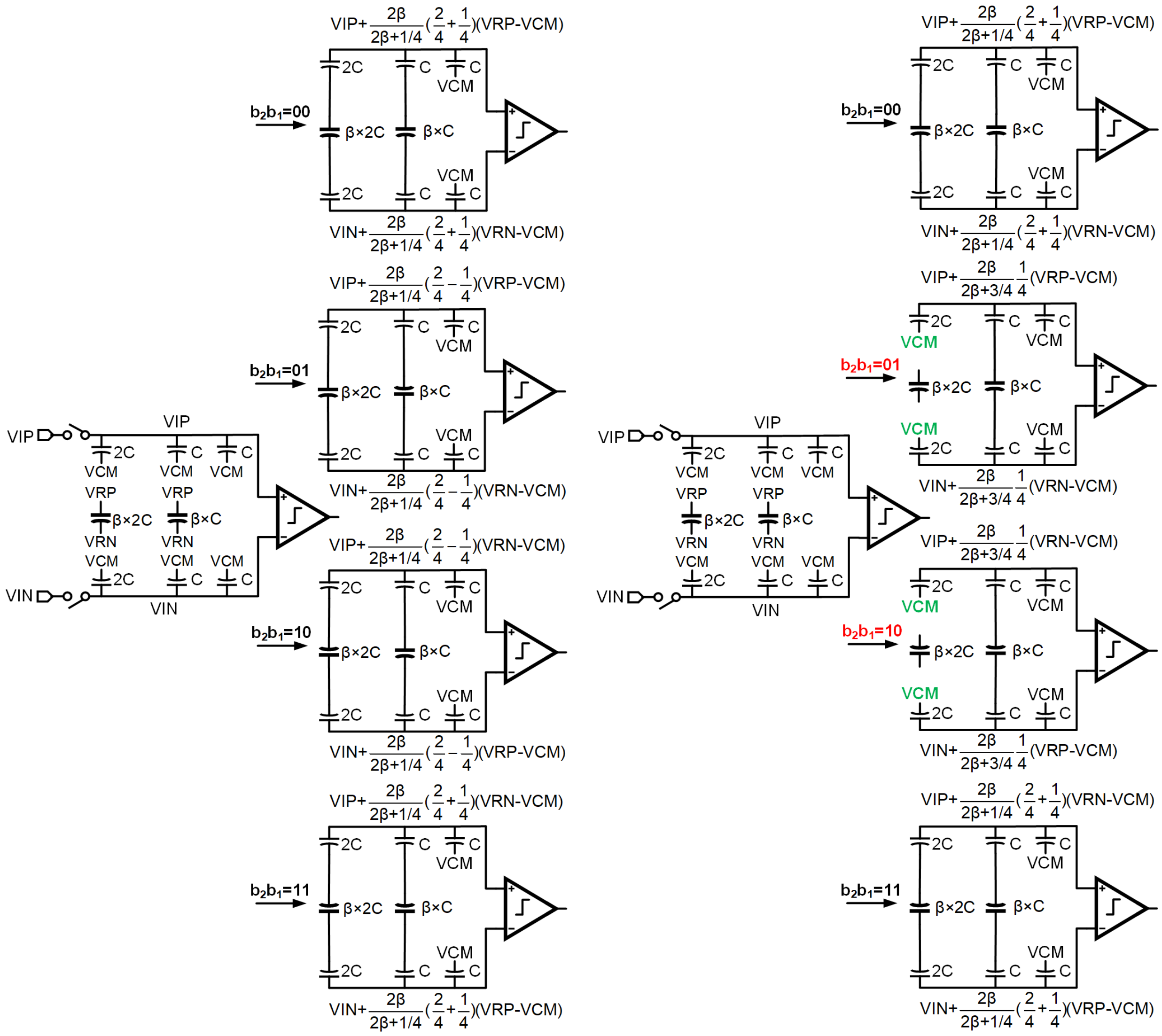


Figure 5.4: Three-bit bitwise charge sharing CDAC successive switching (SS) example.

For all three methods, for each bit switching, the resulting top plate voltages are labeled in the figures. We can see that there is a β-dependent term, referred to as α, $0 < \alpha < 1$,



(a) Aligned Switching (AS)

(b) Detect-and-sckip, Aligned Switching (DAS-AS)

Figure 5.5: Three bit bitwise charge sharing CDAC AS and DAS-AS examples.

reflecting the reference error due to finite β. When $\beta = \infty$, $\alpha = 1$. Further, we observe that with bitwise RCRs, for AS, term α is no less than that of successive switching. AS has the better linearity than successive switching. However, for DAS-AS, term α is no greater than that of successive switching. Thus DAS-AS has the worst linearity in the case of with bitwise RCRs. With sample-wise RCR, for AS, term α is no greater than that of successive switching. However, for DAS-AS, term α is no less than that of successive switching. Thus, DAS-AS scheme has the best linearity in the case of with sample-wise RCR.

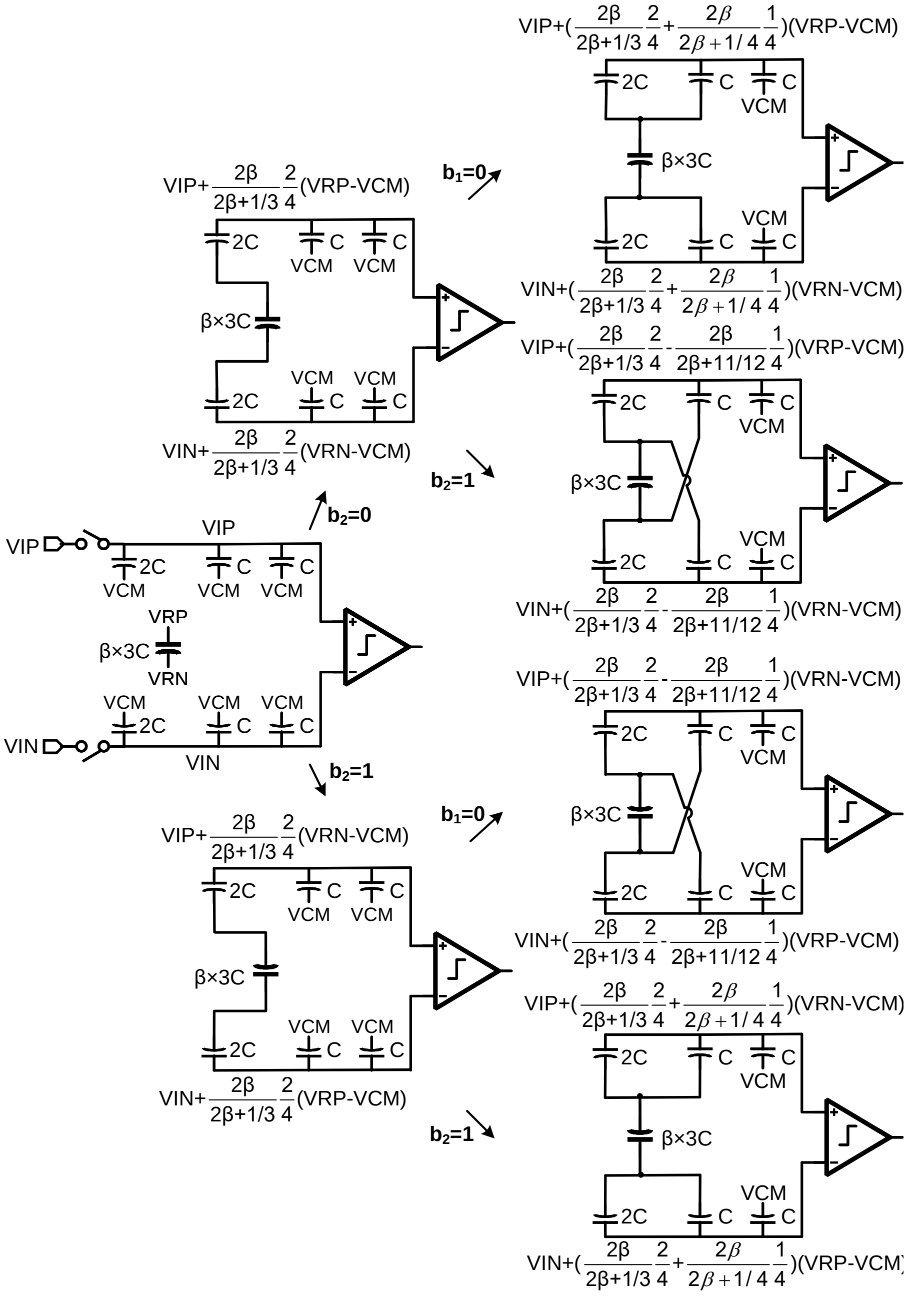
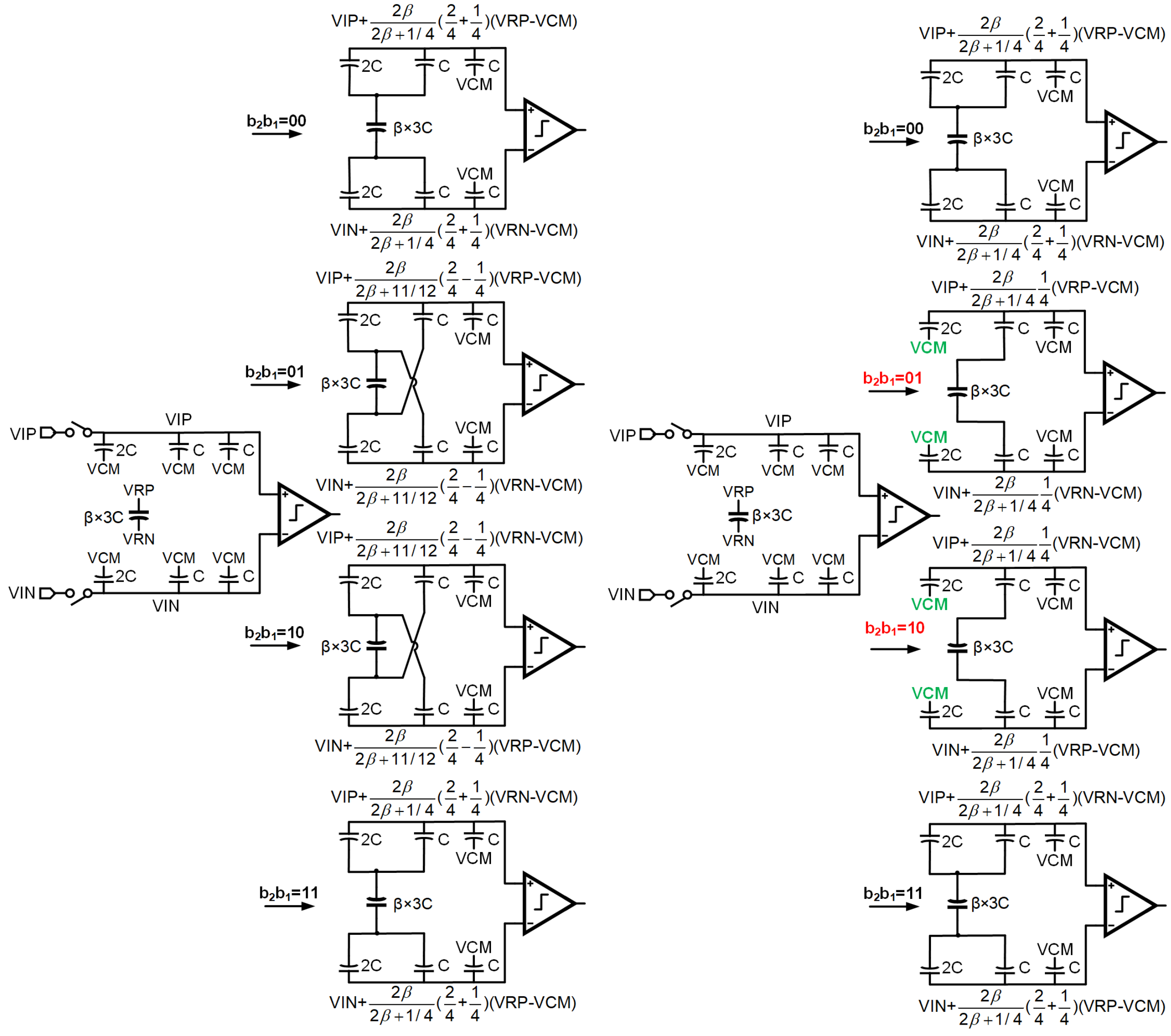


Figure 5.6: Three-bit samplewise charge sharing CDAC successive switching (SS) example.



(a) Aligned Switching (AS)

(b) Detect-and-sckip, Aligned Switching (DAS-AS)

Figure 5.7: Three bit samplewise charge sharing CDAC AS and DAS-AS examples.

5.3 *Analysis of Segmented SAR Switching with Reference Charge Reservoirs*

This section presents theoretical analysis of the SAR-ADC linearity for various switching methods for a segmented charge-sharing (N + M)-bit SAR ADC where a coarse SAR-ADC computes the N MSBs, and a fine SAR ADC computes the M LSBs. Whenever possible,

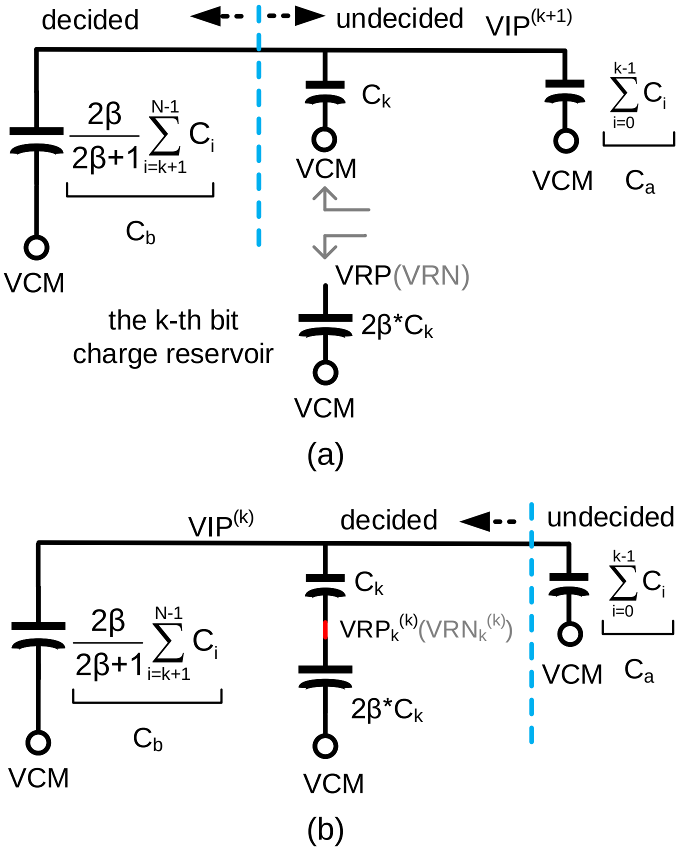


Figure 5.8: Half-circuit model and derivation of bitwise reference switching in the coarse SAR ADC. (a) The $(k+1)^{th}$ decision; (b) The $(k)^{th}$ decision.

the analysis is based on the equivalent circuit model introduced in [58] since it provides more circuit intuition. Nevertheless, all the results in this section have been derived directly using the principle of charge conservation following the same procedure as in the Appendices of [58].

5.3.1 Bitwise RCR based Coarse SAR ADC Successive Switching

The N-bit coarse SAR ADC decides each bit successively using VCM-based merged capacitor switching [43] with bitwise RCRs. We use a bracketed superfix $^{(k)}$ to indicate the k-th *bit decision*, and a subscript $_i$ to represent the i-th bit. The equivalent half-circuit model [58] for charge sharing from $(k+1)$-th to k-th bit decision is shown in Fig. 5.8. Without loss of generality we assume that the bottom plate of the k-th bit weight capacitor C_k is switched from connecting to VCM to either VRP or VRN depends on b_k. Let us assume that it is VRP. Voltage $\mathrm{VRP}_k^{(k)}$ can be obtained from the following charge sharing equation:

$$\begin{aligned}(\mathrm{VRP}-\mathrm{VCM})(2\beta C_k) = (&\mathrm{VRP}_k^{(k)} - \mathrm{VCM}) \\ &[2\beta C_K + (C_a + C_b)C_k/(C_a + C_b + C_k)]\end{aligned} \tag{5.2}$$

Then the P-side top-plate voltage change due to this charge sharing is obtained by capacitive division as

$$\mathrm{VIP}^{(k)} - \mathrm{VIP}^{(k+1)} = \frac{C_k(1-2b_k)}{C_a + C_b + C_k}(\mathrm{VRP}_k^{(k)} - \mathrm{VCM}) \tag{5.3}$$

Substituting (5.2) to (5.3) with $C_T = C_a + C_b(2\beta+1)/2\beta + C_k$, we can obtain

$$\mathrm{VIP}^{(k)} - \mathrm{VIP}^{(k+1)} = \alpha^{(k)}\frac{(1-2b_k)C_k}{C_T}(\mathrm{VRP} - \mathrm{VCM}) \tag{5.4}$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + \sum\limits_{j=0}^{k-1}\frac{C_j}{C_T}} = \frac{2\beta}{2\beta + (1/2)^{N-k}} \tag{5.5}$$

where N is the number of bits in the coarse ADC, C_T is the sum of the coarse CDAC capacitance from C_0 to C_{N-1}, and b_k is the k-th bit value being either 1 or 0. The last equality in (5.5) holds if bit capacitances are binary weighted.

Note that $0 < \alpha^{(k)} < 1$, $\alpha^{(k)}$ increases from the MSB ($k = N-1$) to the LSB ($k = 1$) and $\alpha^{(k)} = 1$ when $\beta = \infty$. Fig. 5.9 shows $\alpha^{(k)}$ at each bit decision of a 5-bit bitwise switched RCRs based coarse SAR ADC with $\beta = 16$. The term $\alpha^{(k)} \neq 1$ in (5.4) is caused by the reference error due to charge sharing between the reference capacitor and the bit capacitor. The beauty of bitwise RCRs based SAR ADCs is that the reference error is the form of linear bit weight error as shown in (5.5) and in Fig. 5.9 [58]. Bit weight error (1-$\alpha^{(k)}$) depends only on β, k and N, irrespective of the input.

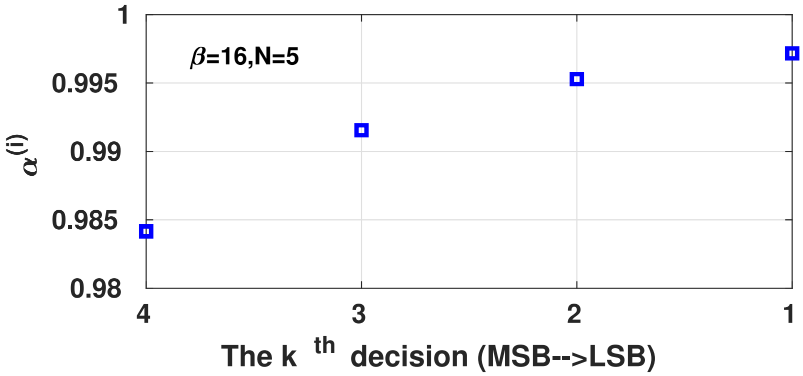


Figure 5.9: $\alpha^{(k)}$ at each bit decision for the coarse SAR ADC in a segmented architecture.

5.3.2 Fine MSB Aligned Switching and DAS Aligned Switching : Bitwise and Subsample Wise

Let C_F denote the fine ADC unit capacitance, C_{TM} the N-bit MSB capacitance, C_{TL} the M-bit LSB capacitance, and C_{TF} the total capacitance in the fine ADC.

Fine MSB Aligned Switching: Bitwise and Subsample Wise

When loading the coarse digits directly to the fine MSBs in one step, the fine CDAC top plate voltages after aligned switching can be expressed in (5.6) and (5.7)

$$\mathrm{VIP}^{(M)} = \mathrm{VIP} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}} (1 - 2b_i)(\mathrm{VRP} - \mathrm{VCM}) \tag{5.6}$$

$$\mathrm{VIN}^{(M)} = \mathrm{VIN} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}} (1 - 2b_i)(\mathrm{VRN} - \mathrm{VCM}) \tag{5.7}$$

where b_i are the digits of the N-bit fine MSBs, which are equal to coarse bits. For aligned switching, the coefficient $\alpha^{(M)}$ is extracted to the outside of the sum symbol. This is because the aligned switching is one-step operation involving N-bits.

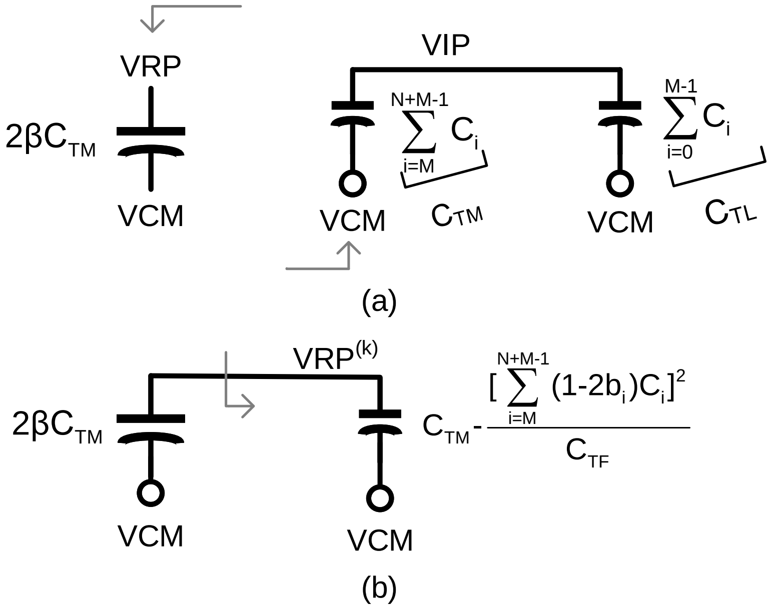


Figure 5.10: Half-circuit model and derivation of sample-wise reference switching in fine MSB. (a) Sampling phase; (b) The AS decision phase

For bitwise referenced, $\alpha^{(M)}$ can be expressed as follows:

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}}} = \frac{2\beta}{2\beta + 1 - \frac{C_{TM}}{C_{TF}}} \tag{5.8}$$

The derivation is in Appendix A based on charge conservation.

For subsample-wise referenced, the equivalent half-circuit model from the sampling phase to the aligned switching phase is shown in Fig. 5.10 [58]. Charge is conserved before and after aligned switching; i.e., .

$$(\mathrm{VRP} - \mathrm{VCM})(2\beta C_{TM}) = (\mathrm{VRP}^{(M)} - \mathrm{VCM}) \\ [2\beta C_{TM} + C_{TM} - \frac{[\sum_{i=M}^{N+M-1} C_i(2b_i - 1)]^2}{C_T}] \tag{5.9}$$

Then the p-side top-plate voltage change can be obtained based on capacitive division.

$$\mathrm{VIP}^{(M)} = \mathrm{VIP} + (\mathrm{VRP}^{(M)} - \mathrm{VCM}) \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}}(1 - 2b_i) \tag{5.10}$$

Substituting (5.9) to (5.10) with $C_{TF} = C_{TM} + C_{TL}$, we can obtain the same result as (5.6) with $\alpha^{(k)}$ defined by (5.11).

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \frac{[\sum_{i=M}^{N+M-1} C_i(2b_i-1)]^2}{C_{TF}C_{TM}}} \tag{5.11}$$

We note that coefficient $\alpha^{(M)}$ in (5.8) is input independent because both bitwise RCRs and aligned switching are input independent. $\alpha^{(M)}$ is shown in Fig. 5.11 by the dot marker curve. The last term in the denominator of (5.8) represents the ratio of the switched bit capacitance to the total capacitance. In aligned switching, the switched bits are the N-bit MSBs in the fine ADC. The subsample-wise reference coefficient $\alpha^{(M)}$ in (5.11) is input dependent because of the subsample-wise RCR. In this case, $\alpha^{(M)}$ has 2^N possible values based on the N-bit MSBs, which is shown in Fig. 5.11 by the square marker curve.

We further observe that the square term in (5.11) is less than or equal to C_{TM}. Thus $\alpha^{(M)}$ in (5.8) $\geq \alpha^{(M)}$ in (5.11). Therefore the aligned switching with bit-wise charge reservoirs always has better linearity than aligned switching with sub-sample wise charge reservoir.

Fine MSB DAS Aligned Switching: Bitwise and Subsample wise

Now we consider the fine MSBs use DAS aligned switching based on the computed coarse MSBs. If the coarse MSB is 1, then the p-side (n-side) CDAC bottom plates either connect to VCM or switch to VRN (VRP). The switched bit capacitance in the fine MSBs is:

$$C_{sw} = \sum_{i=M}^{N+M-1} C_i b_i \tag{5.12}$$

where b_i are the digits of the N-bit fine MSBs, which are obtained by left rotating coarse bits. The differential fine CDAC top-plate voltages after DAS-AS operation are given in

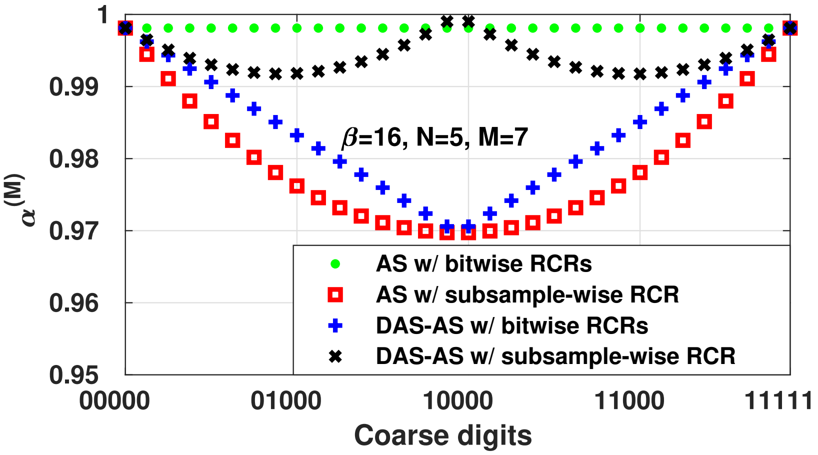


Figure 5.11: $\alpha^{(M)}$ versus coarse codes for the fine MSBs in a segmented architecture.

(5.13) and (5.14):

$$\mathrm{VIP}^{(M)} = \mathrm{VIP} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i b_i}{C_{TF}} (\mathrm{VRN} - \mathrm{VCM}) \tag{5.13}$$

$$\mathrm{VIN}^{(M)} = \mathrm{VIN} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i b_i}{C_{TF}} (\mathrm{VRP} - \mathrm{VCM}) \tag{5.14}$$

If the coarse MSB is 0, the total switched bit capacitance in the fine MSBs is:

$$C_{sw} = \sum_{i=M}^{N+M-1} C_i(1 - b_i) \tag{5.15}$$

The CDAC top plate voltages can be expressed by

$$\mathrm{VIP}^{(M)} = \mathrm{VIP} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i(1 - b_i)}{C_{TF}} (\mathrm{VRP} - \mathrm{VCM}) \tag{5.16}$$

$$\mathrm{VIN}^{(M)} = \mathrm{VIN} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i(1 - b_i)}{C_{TF}} (\mathrm{VRN} - \mathrm{VCM}) \tag{5.17}$$

For bitwise-referenced DAS aligned switching, $\alpha^{(M)}$ is given in (5.18)

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \frac{C_{sw}}{C_{TF}}} \tag{5.18}$$

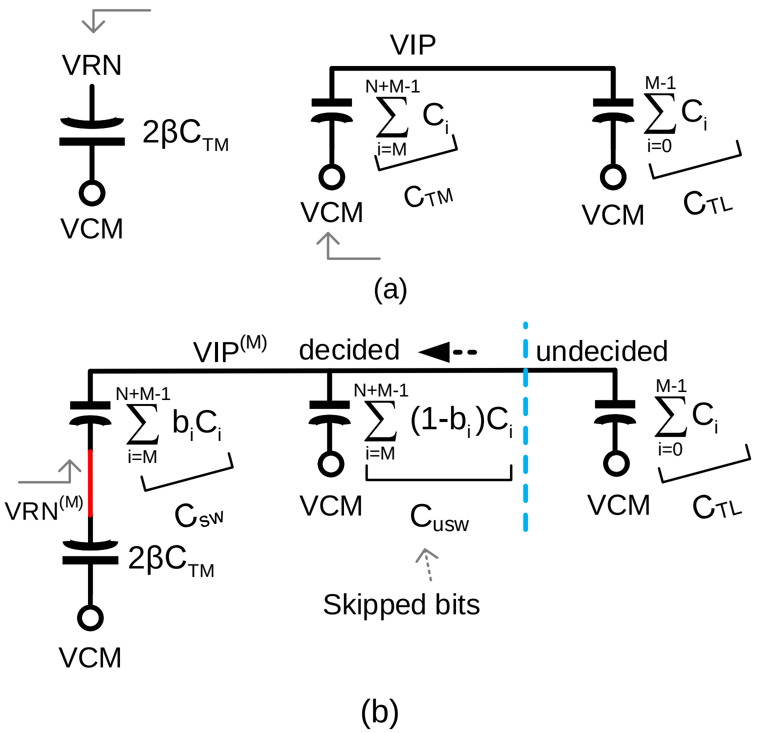


Figure 5.12: Half-circuit model and derivation of subsample-wise reference switching when coarse MSB is 1 in fine MSB. (a) Sampling phase; (b) The DAS-AS decision phase

as shown in Appendix-B based on the principle of charge sharing.

For subsample-wise referenced DAS aligned switching, there is no cross coupling between the P-side and the N-side CDACs, so the equivalent half-circuit model can be used to derive the final results directly. Fig. 5.12 shows the equivalent half-circuit model from the sampling phase to the DAS aligned switching phase. Charge is conserved before and after aligned switching; i.e.,

$$\begin{aligned}(\mathrm{VRN}-\mathrm{VCM})(2\beta C_{TM}) &= (\mathrm{VRN}^{(M)}-\mathrm{VCM})\\ &\quad [2\beta C_{TM}+(C_{TL}+C_{usw})C_{sw}/(C_{TL}+C_{usw}+C_{sw})] \qquad (5.19)\end{aligned}$$

Then the p-side top-plate voltage change can be obtained based on capacitive division.

$$\mathrm{VIP}^{(M)} = \mathrm{VIP} + (\mathrm{VRN}^{(M)} - \mathrm{VCM}) \sum_{i=M}^{N+M-1} \frac{C_i b_i}{C_{TF}} \tag{5.20}$$

Substituting (5.19) to (5.20) with $C_{TM} = C_{sw} + C_{usw}$ and $C_{TF} = C_{TM} + C_{TL}$, we can obtain the same result as (5.13) with $\alpha^{(M)}$ defined by (5.21)

$$\alpha^{(M)} = \frac{2\beta}{2\beta + \frac{C_{sw}}{C_{TM}}(1 - \frac{C_{sw}}{C_{TF}})} \tag{5.21}$$

We have $\alpha^{(M)}$ in (5.21) $\geq$ $\alpha^{(M)}$ in (5.18) by comparing (5.21) with (5.18). This is because in the DAS-AS operation, the ratio of the reservoir capacitance to the switched bit capacitance is $\beta C_{TM}/C_{sw}$ for subsample-wise RCR, greater than or equal to β for bitwise RCRs. Thus sub-sample wise referenced DAS aligned switching always has better linearity than bitwise referenced DAS aligned switching. Since C_{sw} is input linearly dependent, $\alpha^{(M)}$ in (5.18) is also input linearly dependent, while $\alpha^{(M)}$ in (5.21) is input nonlinearly dependent. $\alpha^{(M)}$ in (5.18) and (5.21) versus coarse digits are shown in Fig. 5.11 with the plus '+' marker and 'x' marker respectively.

Comparison of Four MSB Switching Methods

Now we can compare $\alpha^{(M)}$ in (5.8), (5.11), (5.18) and (5.21) by examining the last two terms in the denominator of $\alpha^{(M)}$. In DAS-AS scheme, the total switched capacitance C_{sw} expressed in (5.12) and (5.15) is mathematically equal to the term $|\sum_{i=M}^{N+M-1} C_i(2b_i - 1)|$ in aligned switching scheme shown in the last term in the denominator of (5.11). We rewrite (5.11) as

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \frac{C_{sw}^2}{C_{TF}C_{TM}}} \tag{5.22}$$

Thus $\alpha^{(M)}$ in (5.11) $\leq$ $\alpha^{(M)}$ in (5.18). Up to now we have $\alpha^{(M)}$ in (5.8) $\geq$ $\alpha^{(M)}$ in (5.11), and $\alpha^{(M)}$ in (5.21) $\geq$ $\alpha^{(M)}$ in (5.18) $\geq$ $\alpha^{(M)}$ in (5.11). Finally, we compare $\alpha^{(M)}$ in (5.8) with the one in (5.21) through comparing $1 - C_{TM}/C_{TF}$ with $\frac{C_{sw}}{C_{TM}}(1 - \frac{C_{sw}}{C_{TF}})$. As shown in Appendix-E, we have $\alpha^{(M)}$ in (5.8) $\geq$ $\alpha^{(M)}$ in (5.21) $\geq$ $\alpha^{(M)}$ in (5.18) $\geq$ $\alpha^{(M)}$ in (5.11) except

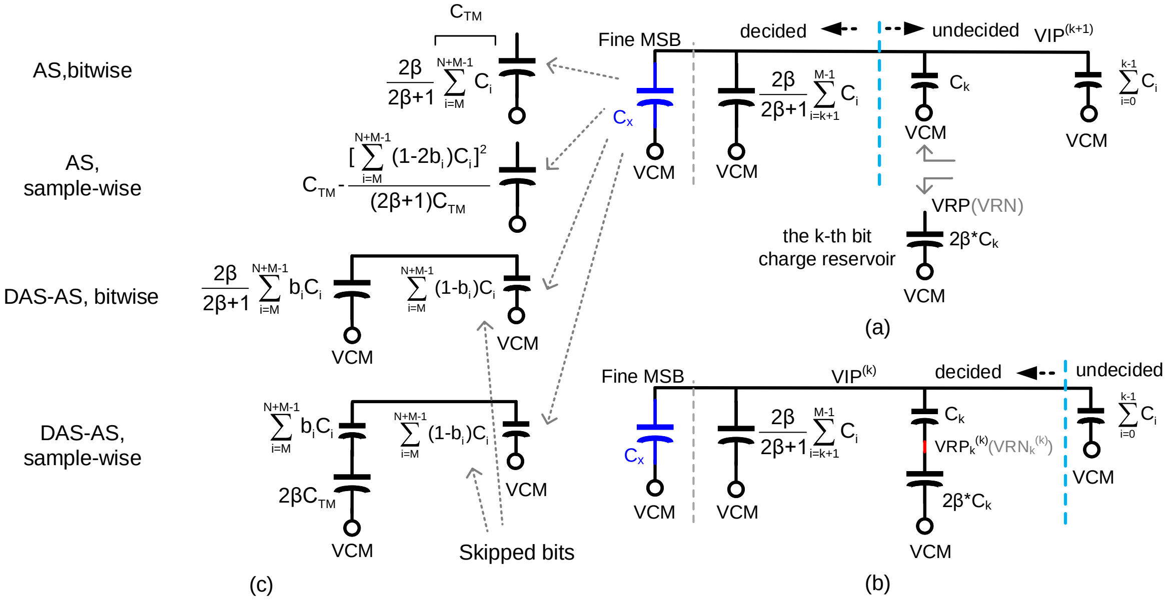


Figure 5.13: Half-circuit model and derivation of bitwise reference switching in fine LSBs. (a) The $(k+1)^{th}$ decision; (b) The $(k)^{th}$ decision; (c) C_x in 4 different switching methods.

at the middle codes. Therefore, in term of linearity, bitwise AS is better than subsample-wise DAS-AS, which is better than bitwise DAS-AS, which is better than subsample-wise AS.

5.3.3 Bitwise RCR based Fine LSB Successive Switching

Once the the N MSBs in the fine SAR-ADC are set based on the coarse ADC bits using one of the four methods, the remaining M-bit LSBs in the fine SAR-ADC can be decided by bitwise RCRs based successive switching with $k = M-1, ..., 1$. The top-plate voltages at step k can be analyzed using the equivalent half-circuit models shown in Fig. 5.13, where C_x is the equivalent capacitance for the MSBs that have been set using one of these four methods. This is exactly similar to the analysis for the bitwise switched coarse ADC in Section 5.3.1 except with an extra C_x. Hence the top-plate voltages at step k can be obtained in the same form as (5.2) re-written as follows:

$$\mathrm{VIP}^{(k)} = \mathrm{VIP}^{(k+1)} + \frac{\alpha^{(k)}C_k}{C_{TF}}(1-2b_k)(\mathrm{VRP}-\mathrm{VCM}) \qquad (5.23)$$

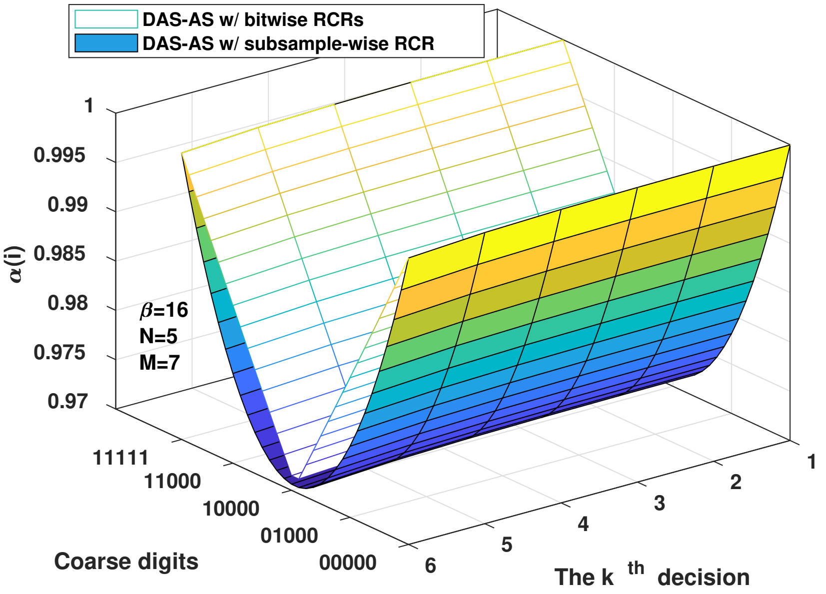


Figure 5.14: $\alpha^{(i)}$ versus coarse digits at each bit decision for the fine LSBs in a segmented architecture.

where $\alpha^{(k)}$ is given in (5.24). Substitute C_x in Fig. 5.13 (c) into (5.24), we have $\alpha^{(k)}$ for the cases of N MSBs set by aligned switching with bitwise RCRs, aligned switching with sub-sample wise RCR, DAS aligned switching with bitwise RCRs and DAS aligned switching with sub-sample wise RCR shown in (5.25) to (5.28) respectively.

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum\limits_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{(C_{TM}-C_x)(2\beta+1)}{C_{TF}}} \tag{5.24}$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum\limits_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{C_{TM}}{C_{TF}}} \tag{5.25}$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum\limits_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{[\sum\limits_{i=M}^{N+M-1} C_i(2b_i-1)]^2}{C_{TF}C_{TM}}} \tag{5.26}$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum\limits_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{C_{sw}}{C_{TF}}} \tag{5.27}$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum\limits_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{C_{sw}}{C_{TF}} \frac{2\beta+1}{2\beta\frac{C_{TM}}{C_{sw}}+1}} \tag{5.28}$$

We see that for all the four cases, $\alpha^{(k)}$ differs only in the last term in the denominator. The third term in the denominator represents the ratio of the switched bits to the fine total capacitance for the successive decided bits in the fine LSBs. It has same format as in (5.5). But the switched bits in the MSBs are different by using different switching schemes as reflected in the fourth term in the denominator for each case.

It is clear that the error increases with C_x. we can see that C_x case 2 greater than C_x case 4, greater than case 3, and greater than case 1. Hence for the fine LSB switching, AS with bitwise for MSB yields the minimal error. But since each of these has exponentially smaller weight comparing to the MSB switching, so we adopt the DAS-AS for MSB switching.

Figure 5.14 plots $\alpha^{(i)}$ versus coarse digits (from 00000 to 11111) at each fine bit decision (from k= 6 to 1) for DAS aligned switching. From Fig. 5.14 we see $\alpha^{(i)}$ is almost the same when 5-bit fine MSBs use AS or DAS-AS with subsample-wise RCR. Observe the last term in (5.28), $\frac{C_{sw}}{C_{TF}} \frac{2\beta+1}{2\beta\frac{C_{TM}}{C_{sw}}+1} \geq \frac{C_{sw}}{C_{TF}} \frac{C_{sw}}{C_{TM}}$. It has the same format with the last term in denominator of (5.26). C_{sw} is symmetric according to (5.12). It has the minimum value at coarse digits 01111 and 10000. Thus, C_{sw}^2 are minimum at 01111 and 10000. This explains why $\alpha^{(i)}$ in (5.28) has a single valley at the middle codes.

5.3.4 Static Performance of RCR-based Segmented SAR ADC

Using analytic formula derived, we can compute, simulated, and compare the static performance differential nonlinearity (DNL) and integral nonlinearity (INL) of an RCR-based 11-bit segmented SAR ADC. Figure 5.15 and Figure 5.16 upper four plots show the respective DNL and INL of a segmented SAR ADC with 5-bit coarse and 12-bit fine SAR ADC using four switching methods for the fine MSBs. With $\beta = 5$, the 5-bit coarse ADC can compute output digits correctly. These 5 digits are loaded to the 5-bit fine MSBs using one of four switching methods. As we can see, the aligned switching with bitwise RCRs in (a) yields the best static performance. This is because the reference error for the 5-bit fine MSBs is constant according to (5.8), which can be written

$$(1-\alpha^{(M)})(\mathrm{VRP}-\mathrm{VRN}) \approx 0.006(\mathrm{VRP}-\mathrm{VRN}) < \frac{1}{2^7}(\mathrm{VRP}-\mathrm{VRN}) \tag{5.29}$$

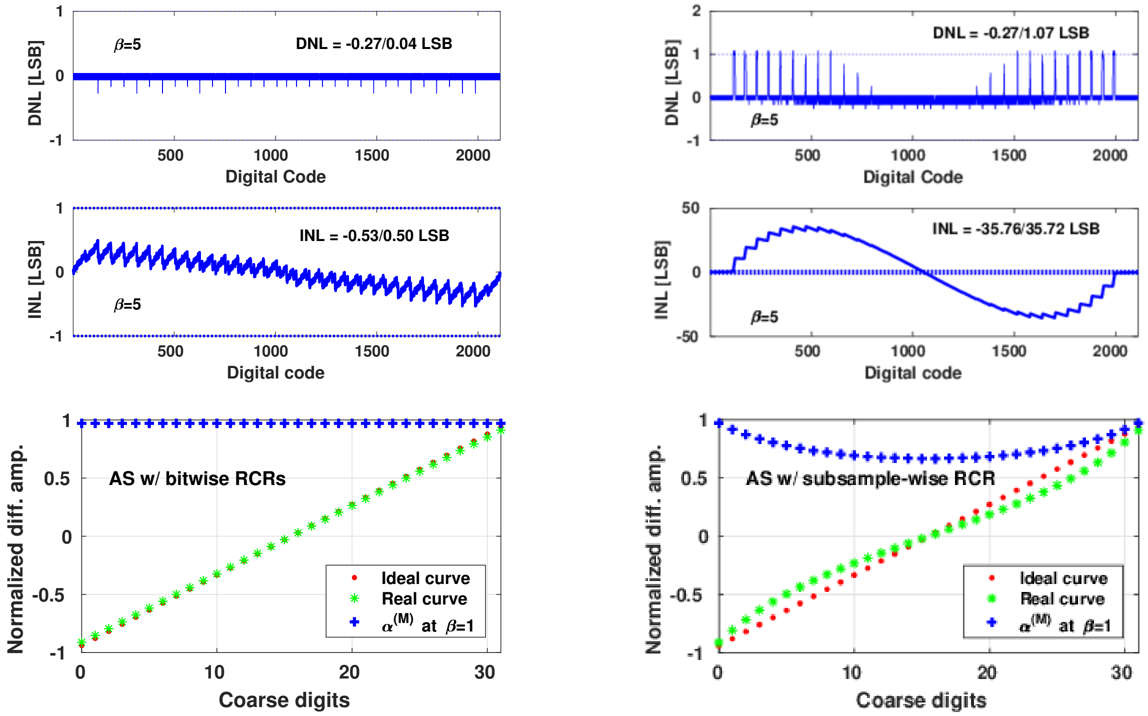
Thus, the 7-bit fine LSBs can compute results correctly. This yields the INL to be in the range of ±0.5 LSB.

The DNL and INL in Fig. 5.15 (b) and Fig 5.16 have some similarities. The segmented misaligned ADC transfer curves lead to different analog inputs mapping to the same digits, thus causing the DNL at the digits corresponding to misaligned transfer curves to be more than +1 LSB. The INL is the deviation in LSB of the actual transfer function of the ADC from the ideal transfer curve. To show the linearity of the segmented ADC is mainly decided by the *reference error introduced in the 5-bit fine MSBs.* The $\alpha^{(M)}$, normalized ideal and real transfer curves of 5-bit fine MSBs versus coarse digits are plotted in Fig. 5.15 and Fig 5.16 with the four cases. $\alpha^{(M)}$ affects the transfer curve through modulating the reference voltage in a manner of $\alpha^{(M)}(\mathrm{VRP}-\mathrm{VRN})$. Thus, the larger $\alpha^{(M)}$, the smaller reference error $1-\alpha^{(M)}$ yields better linearity. Here $\beta = 1$ is used to show this nonlinear reference modulation clearly. We see that the deviation of the real transfer curve from the ideal curve in 5-bit MSB has the same shape with the INL of the 11-bit segmented SAR ADC. To minimize the reference error, $\alpha^{(M)}$ shall be as large as possible. While for minimum switching energy associated with the MSBs switching, DAS-AS with subsample-wise RCR is a good option.

5.4 An 11-bit Segmented SAR-ADC Prototype

5.4.1 Segmented SAR-ADC Architecture

Figure 5.17 shows the architecture of the proposed RCR-based segmented SAR ADC. For simplicity, it only shows the singled-end architecture, but the implementation is differential. It consists of a 5-bit coarse SAR ADC, a 12-bit fine SAR ADC that including one redundant



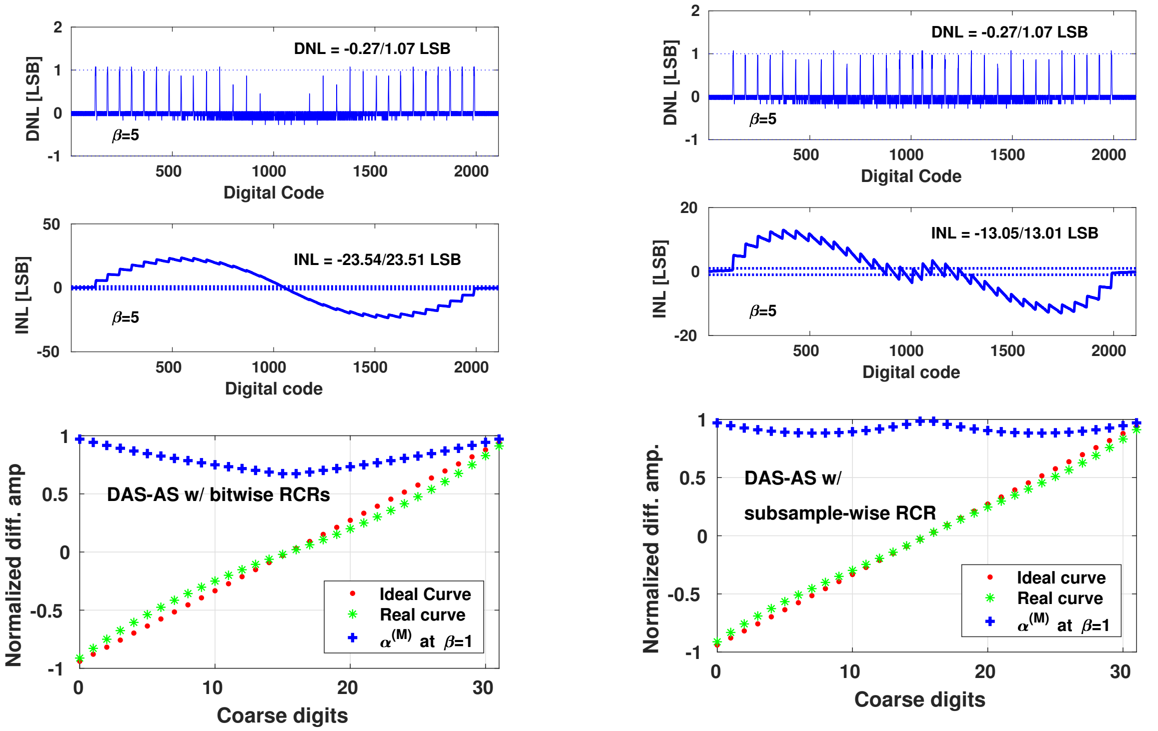
(a) Aligned switching with bitwise RCRs.

(b) Aligned switching with subsample-wise RCR.

Figure 5.15: Static performance and the fine CDAC top-plate voltage versus coarse digits of an 11-bit RCR based charge sharing segmented SAR ADC in which fine MSBs use aligned switching methods with bitwise or subsample-wise RCRs shown in (a) to (b).

bit, an AS or DAS-AS block for setting fine MSBs, and a digital error correction (DEC) block. The coarse or fine SAR ADC contains a bootstrapped sampling switch, a RCR-based CDAC, a voltage comparator [44], and a SAR logic block.

Differential inputs VIP and VIN are sampled on the bottom plates of CDAC in both coarse and fine ADCs, while the top plates are connected to VCM during the sampling phase. Simultaneously, the bit reservoir capacitor samples references VRP and VRN. In practice, VRP is set to be supply VDD and VRN is set to ground GND. Here VCM is the common-mode voltage of the differential inputs, and it also equals to half VDD. After sampling, the 5-bit coarse SAR ADC computes the 5 MSBs bit by bit using VCM-based merged capacitor switching (MCS) [43]. As the reference source, the reservoir capacitor



(a) Detect-and-skip aligned switching with bitwise RCRs.

(b) Detect-and-skip aligned switching with subsample-wise RCR.

Figure 5.16: Static performance and the fine CDAC top-plate voltage versus coarse digits of an 11-bit RCR based charge sharing segmented SAR ADC in which fine MSBs use subsample-wise switching methods with bitwise or subsample-wise RCRs shown in (a) to (b).

is inserted in between differential capacitor array successively based on the decision results. Then, the AS or DAS-AS logic block loads digits from the coarse ADC to the 5-bit fine MSBs in one step. Since the fine 5 MSBs are set at one step, one of the four switching methods: AS with bitwise RCRs, AS with subsample-wise RCR, DAS-AS with bitwise RCRs, and DAS-AS with subsample-wise RCR can be used to set 5-bit fine MSBs. Finally, the rest of 7 LSBs in the fine SAR ADC are determined successively using the VCM-based MCS switching method with bitwise RCRs. One redundant bit is included in the fine ADC to correct the error between the coarse and fine ADCs. The 5 MSBs from the coarse ADC and the 7 LSBs from the fine ADC are combined into the DEC block to derive the final 11 bit ADC output.

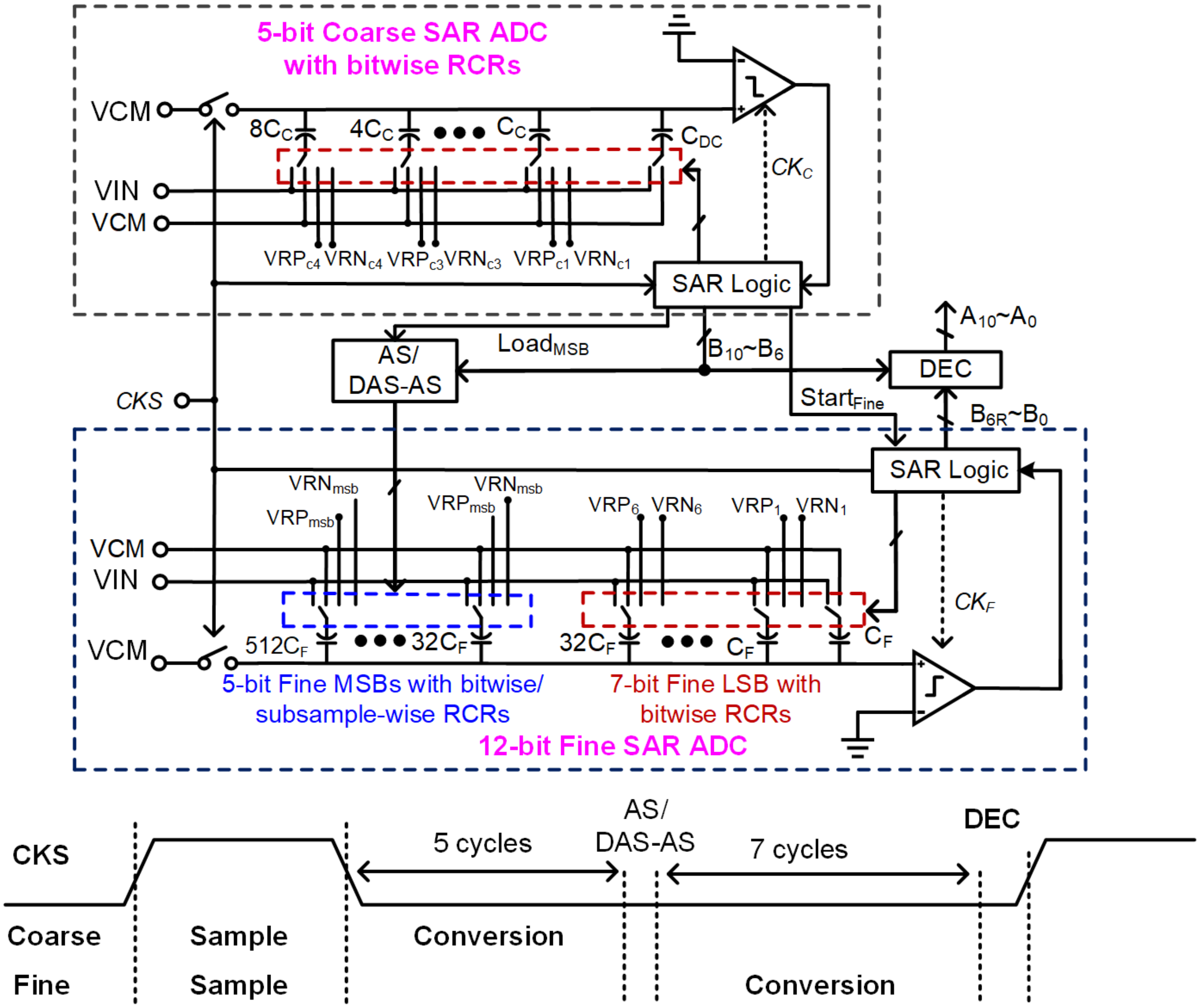


Figure 5.17: The prototype segmented SAR-ADC architecture.

5.4.2 *Charge Reservoir Capacitor Implementation*

The physical CDAC/RCR embedding capacitor cell is illustrated in Fig. 5.18 [?]. It is divided into two parts. Underneath the MOM CDAC capacitors laid the RCR capacitor. The CDAC capacitors are custom designed MOM capacitors formed from metal layers M3 to M7, utilizing both vertical and lateral coupling capacitance. Since the top plate is wrapped by the bottom plate, the parasitic capacitance of the top plate to the substrate is minimized.

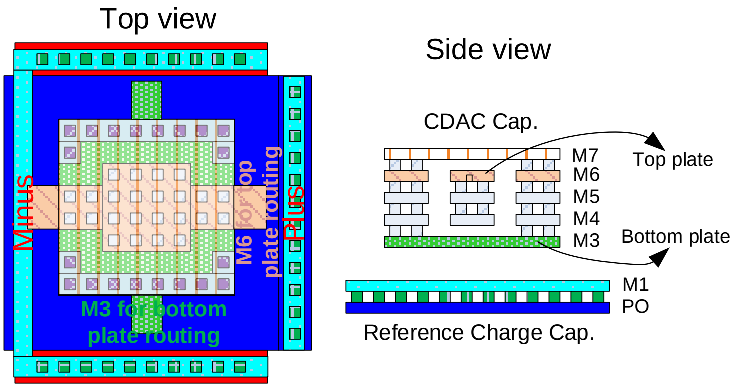


Figure 5.18: The top and cross-section side view of the CDAC/RCR capacitor embedding unit cell.

To reduce parasitic routing coupling capacitance, the CDAC array uses M6 for horizontal routing, and the bottom plate uses M3 for vertical routing. The overall capacitor array is surrounded by a dummy wall to reduce the effect of process variation. The unit bit capacitor for the coarse ADC is 2 fF, while 1 fF for the fine ADC, which yields a total sampling capacitance of 1.088 pF (single-ended).

The RCR capacitor cell is implemented as an NMOS varactor laid under the corresponding MOM CDAC cell with little silicon area penalty. NMOS varactors are used to implement RCR capacitors due to their two advantages over normal NMOS capacitors. First, working near VDD (1.2V), an NMOS varactor features a 50% higher capacitance density than a normal NMOS transistor ($12.46fF/\mu m^2$ vs $8.67fF/\mu m^2$). Secondly, an NMOS varactor has a built-in Nwell, which can provide a cleaner negative reference, VRN, for the ADC with bitwise RCRs separated from the dirty digital ground provided by the p-substrate. In our design, the capacitance ratio between each unit of the RCR capacitor to that of the MOM capacitor is around 120:1. This provides a sufficient margin for eliminating the linearity loss due to reference error.

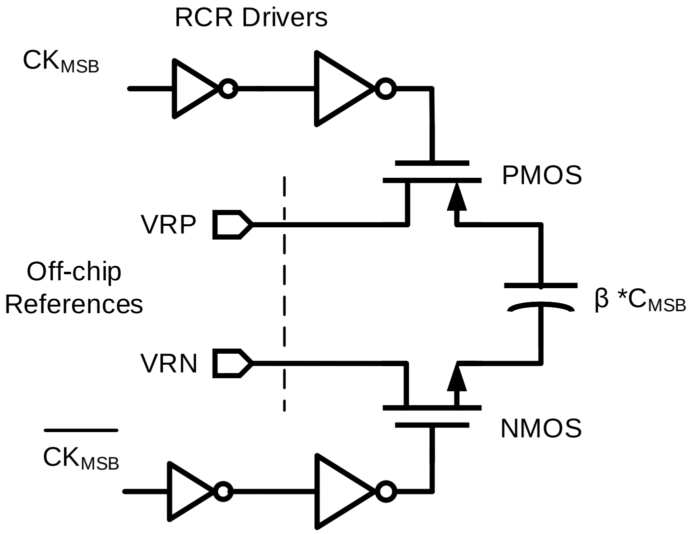


Figure 5.19: Illustration of reference driver of MSB bit.

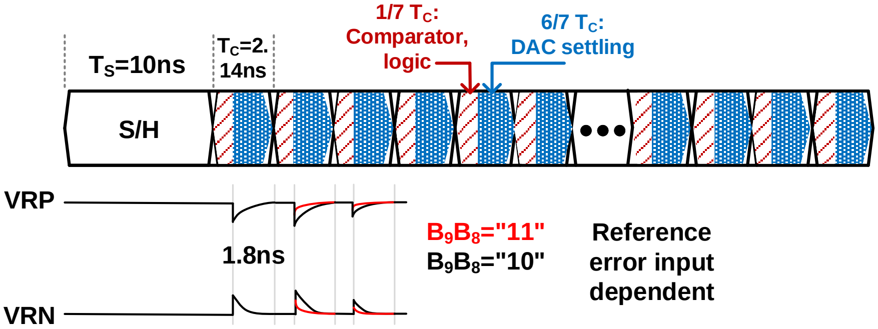


Figure 5.20: Reference buffer settling time for the SAR ADC with bitwise RCR and with on-chip reference buffer.

5.4.3 Drivers for Charge Reservoir Switches

The bitwise reference reservoir capacitance is β times larger than the bit capacitance. This would typically require large-size drivers. However note that this reservoir would only need to be re-charged at the sampling phase, when during the SAR-ADC computation, only a very small amount of charge is lost and we do not use dedicated on-chip reference drivers.

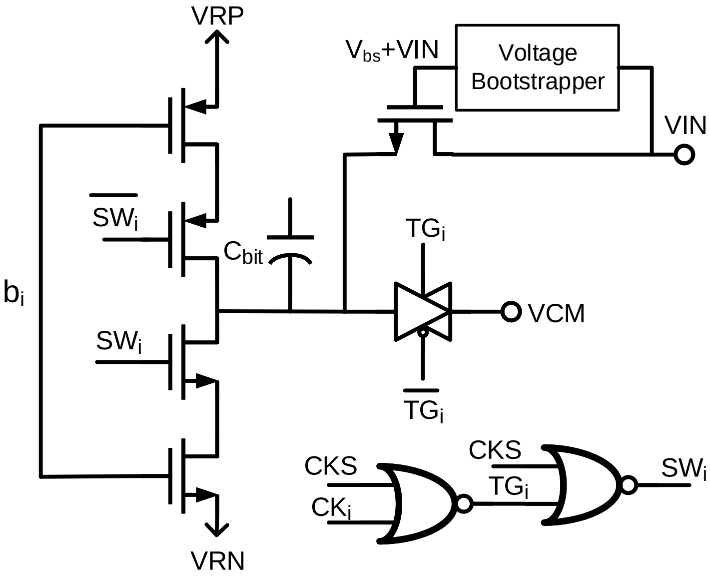


Figure 5.21: Bit capacitor bottom plate switch.

Reference charge reservoirs are re-charged during the sampling period. In this work, 25% of the 25MHz clock cycle is for sampling, which means that reference charge reservoirs need to be settled in 10ns. we use properly sized inverter-based buffer chain to turn on and turn off the switch. Fig 5.19 illustrates the drivers for the MSB bit reference charge reservoir switch. On the other hand, if we do not use charge reservoirs and use on-chip reference and reference buffer, for each bit decision, the reference buffer needs to be settled within about 6/7 bit decision cycle, which is about 1.8 ns. This is shown in Fig. 5.20.

5.4.4 Switches and Shared Bootstrapping Distributed Sampling

As shown in Fig. 5.21, the bottom plate of a bit capacitor connects to a four-way switch: connecting to VRP through stacked PMOS switches, VRN through stacked NMOS switches, VCM through CMOS transmission gate, and VIN through bootstrapped switches. Control signals TG_i and SW_i are generated through the SAR logic. As shown in Fig. 5.22 a bootstrapped switch is an NMOS transistor with the gate and source connecting a volt-

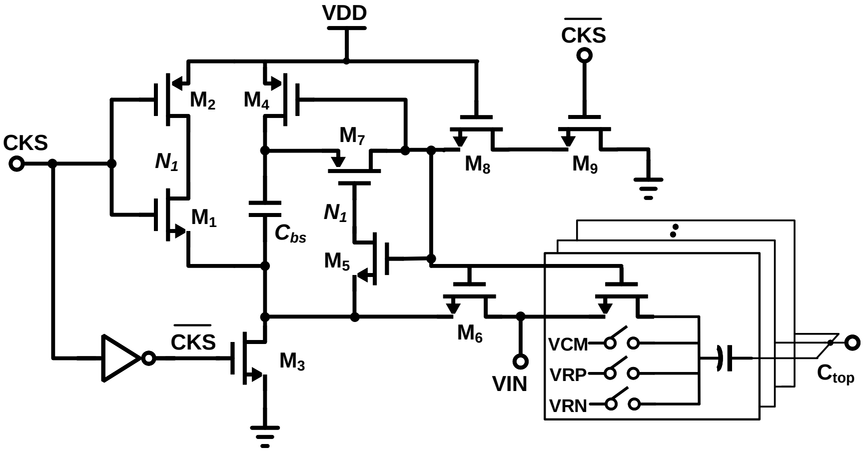


Figure 5.22: Sampling switches with a shared voltage bootstrapper.

age boostrapper that sets the gate voltage to be VIN + V_{bs}. In our design, four shared bootstrappers are used, two for the coarse SAR ADC and two for the fine SAR ADC.

Long routing wire between the bootstrapper and the bitwise sampling switches introduces large parasitic capacitance C_P. For the 12-bit fine ADC, the parasitic wiring capacitance is 12.5 fF, where the total parasitic capacitance of sampling switch NMOS transistors (singled-ended) is about 5 fF. This parasitic capacitance charge-shares the precharged V_{DD} on boost capacitor C_{bs} and boosts the gate voltage by

$$V_{bs} = \frac{C_{bs}}{C_{bs} + C_P} V_{DD}, \tag{5.30}$$

where C_{bs} is the VDD precharged capacitor in the bootstrapper. In our design, we select C_{bs} to be 250 fF for the fine ADC bootstrapper. Two shared bootstrappers instead of twenty-two are used for the fine ADC. This reduces power from 1.7 μW to 1.1 μW. For the coarse ADC, two shared bootstrappers instead of eight are used for the coarse ADC, which reduces power from 655 nW to 223 nW.

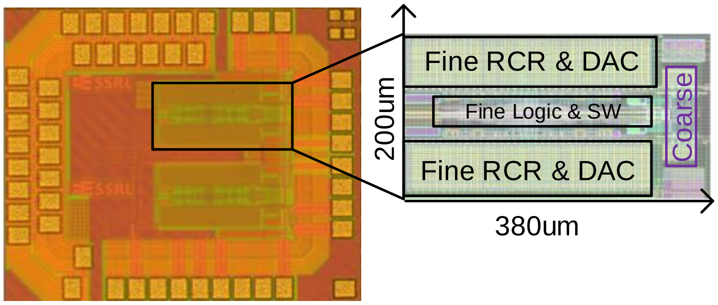


Figure 5.23: Micrograph of the die.

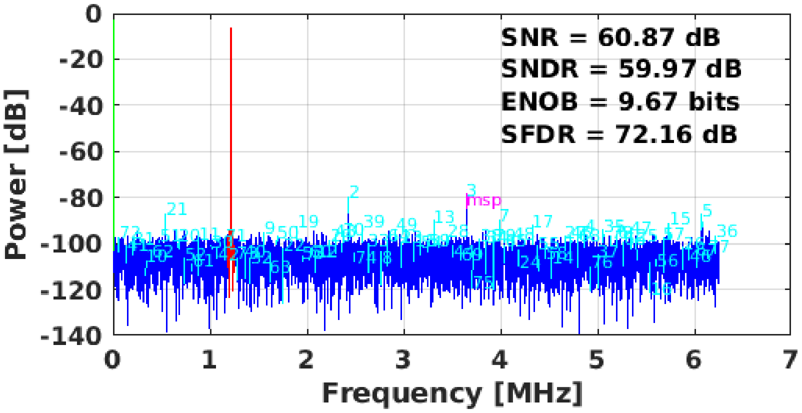


Figure 5.24: Measured FFT spectrum of the ADC, decimated by 2.

5.5 *Measurement Results*

The prototype of an 11-bit segmented SAR ADC was designed and fabricated in a 65 nm CMOS LP technology. Fig. 5.23 shows the die micrograph. The core active area is 0.076 mm^2. The layout floorplan is divided into two parts, the fine ADC is on the left and the coarse ADC on the right. All RCRs were buried underneath of the custom designed MOM capacitors. The reference does not employ any extra decoupling capacitor. Fig. 5.24 shows the measured FFT spectrum with the data decimated by a factor of 2. The measured SNR, SNDR, SFDR are 60.59 dB, 59.97 dB, and 72.12 dB, respectively. Fig. 5.25 shows the

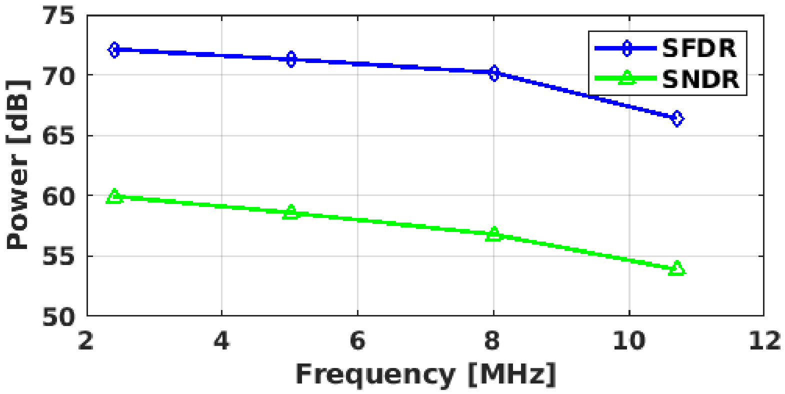


Figure 5.25: Measured dynamic performance.

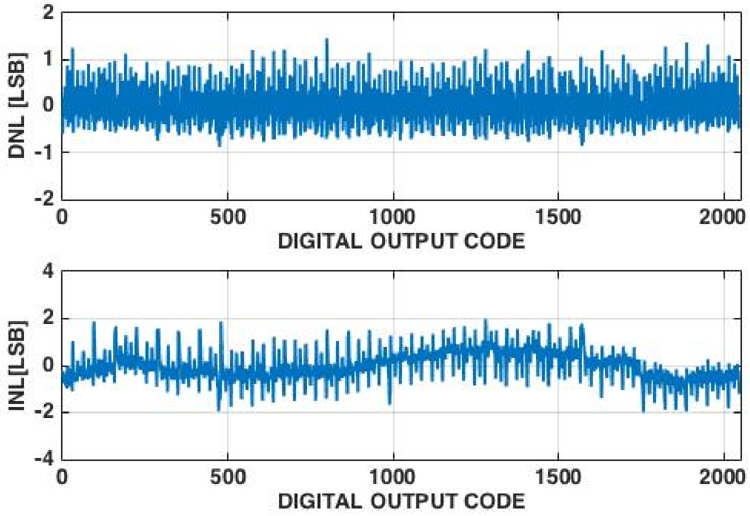


Figure 5.26: Measured static performance.

dynamic performance versus the input signal frequency at the sampling rate of 25 MHz.

The measured DNL and INL are within +1.45/-0.88 LSB and +2/-2 LSB, respectively, as shown in Fig. 5.26. The dynamic performance degradation has been debugged and confirmed to be caused mainly by the offset in both coarse and fine SAR ADC and finite sampling circuit bandwidth. The SNDR loses about 10dB as the input signal frequency varies from 2.3 MHz to 10.7 MHz. The measured total power consumption is 240 μW under 1.2V supply, in which

Table 5.1: Performance Summary and Comparison

Specs	**This work**	[63] '13	[53] '07	[47] '16
Technology	65nm	65nm	90nm	28nm
Arch.	SAR	SAR	SAR	SAR
Resolution	11b	12b	9b	12b
Sample Rate	25MHz	50MHz	0-50MHz	104MHz
ENOB	9.67	10.9	7.4	10.17
Power (mW)	0.24	2.09	0.29	1.6
Area (mm^2)	0.076	0.083	0.08	0.007
FoM(fJ/conv)	11.8*	21.9	65	13.2
On-chip Ref.	Yes	No	yes	Yes
Power	70μW		43.5μW	0.72mW

*-with low frequency input, excluding the charge reservoir driver power, the FoM is 8.4 fJ/conv.

23 μW was used by two comparators and four voltage bootstrappers, 46 μW by CDACs, 38μW by coarse SAR logic and delay lines to generate comparator clocks for asynchronous operation, 53 μW by fine SAR logic, 10 μW by DAS-FAS logic, and 70 μw by reference reservoir drivers. Table 5.1 summarizes the performance of this SAR ADC and compares with state-of-the-art SAR ADC designs. The Walden FoM is 11.8 fJ/conversion-step with on-chip reference reservoirs and 8.4 fJ/conversion-step without.

5.6 Conclusion

This chapter presented the theoretical analysis of a reference charge reservoir (RCR) technique for segmented SAR-ADC design. Theoretical analysis and simulation have been performed to analyze the error due to the finite reference capacitance. Both the analysis and simulation show that in a segmented SAR ADC, successive bit decisions in both coarse and fine SAR ADCs using *bitwise* RCRs and the MSB copy from the coarse ADC to the fine ADC using *aligned switching with bitwise RCRs*, can reduce β significantly compared with other cases without any performance loss. While the fine MSB copy using detect-and-ship, aligned switching with subsample-wise RCR can improve the performance and energy efficiency compared with successive decision only SAR ADCs with bitwise or sample-wise RCR.

An 11-bit 25 MS/s SAR ADC with the proposed RCR technique was designed and fabricated in a 65 nm CMOS technology. Bitwise reference charge reservoir capacitors were implemented as NMOS varactors laid out underneath the corresponding CDAC MOM capacitors; this leads to a compact silicon implementation. Measurement results have shown that it achieves 60 dB SNDR and 72 dB SFDR consuming 240 μW power, of which 70 μW used by the reference reservoir drivers. Without the need for power-hungry analog buffers, the proposed segmented SAR-ADC architecture with mixed subsample-wise and bitwise reference charge reservoirs is attractive for embedded low-power small-silicon-area system-on-chip applications, especially Internet-of-things devices driven by energy harvesters [64].

Chapter 6

CONCLUSION AND FUTURE WORK

Several interface circuits for energy-constrained applications have been demonstrated thoughout this dissertation. A programmable mV-threshold, 1.2 V-output hysteretic comparator with sub-nW power consumption was presented in Chapter 2. Biased by the input signal, the power consumption of the comparator is near zero in the sleep mode. The proposed comparator is promising for low frequency, low threshold, and near-zero-energy event sensing.

The threshold votlage of the comparator is relatively robust to the process and supply variation. Future directions for this work can focus on optimizing the temperature dependency of the threshold voltage. For some sensing applications, the sensor nodes are emplaced in the remote field or border area. The temperature can vary a lot in these areas. To provide constant or unchange thereshold voltage over different temperatures, one can come out a counter-balance circuit to cancel the temperature dependency since the threshold voltage is linearly related to the temperature. The proposed threshold detector was a standalone design. It can be codesigned with systematic level specification requirements. And then extending it to different event-driven sensing applications with systematic level considerations.

A resistor-based, area compact temperature sensor was introduced in Chapter 3. It uses a salicided p-poly resistor to sense the temperature, a differential low-pass filter (DLPF) to generate a temperature-dependent phase, which is then quantized by adjusting the MOM capacitor in the DLPF via successive approximation registration (SAR). This SAR-quantization embedded DLPF sensing architecture utilizes the full temperature-sensing range for digitization, reuses SAR capacitors, eliminates CDAC reference circuits, is much more area efficient than previous PPF and WB followed by SAR quantization architectures. Furthermore, the highly-digital architecture enables easy process migration and the use of a standard digital design flow.

Future directions for this work can optimize the fixed capacitor in the DLPF and the level crossing detector. The design in [38] has a relatively large fixed capacitance C_b, which increases the power consumption of clock driver. The design consideration of choosing relatively large C_b is to make sure the unit capacitance in the 9-bit CDAC is achieveable and accurate. To decrease the fixed bit capacitor C_b down to less than one hundred fF, and still use greater than 0.5 fF unit capacitance in CDAC, one can create an equivalent larger temperature slope of the resistor in the DLPF. The process, supply, and temperature variation of the level crossing detector introduces dominant inaccuracy for the proposed temperature sensor. To decrease the inaccuracy of the sensor, the reference phase path can have a same architecture that track the main path PVT variations. The proposed highly-digital architecture targets for speeding up the design in different processes. The next-step work can use digital flow to synthesize the prototype thermal sensor.

An energy-efficent segmented SAR ADC using passive charge sharing technique was described in Chapter 5. The decent results of the reference error due to finite reference charge was derived in both Chapter 4 and 5. It provides a theory guide for the designers to choose the value of reference charge reservoir capacitor based on the resolution of the ADC. The future direction can design high-speed and low resolution SAR ADC with smaller RCR capacitance to relax the CDAC settling time, while does not introduce reference error but introduce non-uniform quantization for high-speed wireline receiver applications.

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Appendix A

DERIVE PASSIVE CHARGE SHARING SAR ADCS BASED ON CHARGE CONSERVATION

A.1 Bitwise Switched RCR Charge Conservation Equations

Refer to the BS-RCR based SAR in Fig. 4.1, we consider how to find top plate voltages $\mathrm{VIP}^{(k)}$ and $\mathrm{VIN}^{(k)}$, reference top and bottom plate voltages $\mathrm{VRP}_i^{(k)}$ and $\mathrm{VRN}_i^{(k)}$, $i = N-1, ..., k+1$. There are a total of $2(N-k+1)$ variables. Below, we formulate $2(N-k+1)$ charge conservation equations.

First, the charge on the top plates of the P side bit capacitor array is conservative, i.e.,

$$\sum_{i=k+1}^{N-1}[\mathrm{VIP}^{(k+1)} - (1-b_i)\mathrm{VRP}_i^{(k+1)} - b_i\mathrm{VRN}_i^{(k+1)}]C_i + [\mathrm{VIP}^{(k+1)} - \mathrm{VCM}]\sum_{i=0}^{k} C_i = \sum_{i=k}^{N-1}[\mathrm{VIP}^{(k)} - (1-b_i)\mathrm{VRP}_i^{(k)} - b_i\mathrm{VRN}_i^{(k)}]C_i + [\mathrm{VIP}^{(k)} - \mathrm{VCM}]\sum_{i=0}^{k-1} C_i \quad \text{(A-1)}$$

Here the first term represents the total charge of the bits that have been decided, while the second term is the total charge of the bits undecided. Similarly, the top-plate of the N-side bit array charge conservation equation is

$$\sum_{i=k+1}^{N-1}[\mathrm{VIN}^{(k+1)} - (1-b_i)\mathrm{VRN}_i^{(k+1)} - b_i\mathrm{VRP}_i^{(k+1)}]C_i + [\mathrm{VIN}^{(k+1)} - \mathrm{VCM}]\sum_{i=0}^{k} C_i = \sum_{i=k}^{N-1}[\mathrm{VIN}^{(k)} - (1-b_i)\mathrm{VRN}_i^{(k)} - b_i\mathrm{VRP}_i^{(k)}]C_i + [\mathrm{VIN}^{(k)} - \mathrm{VCM}]\sum_{i=0}^{k-1} C_i \quad \text{(A-2)}$$

Second, the charge is conserved of the current bit $(k)^{th}$ reference charge capacitor βC_k from the $(k+1)^{th}$ to the $(k)^{th}$ bit decision. During the $(k+1)^{th}$ bit decision, reservoir capacitor βC_k connects to references VRP and VRN. It then connects to its bit capacitor C_k at the $(k)^{th}$ bit decision. At the reference top-plate VRP we have

$$\begin{aligned}(\mathrm{VRP}-\mathrm{VRN})\beta C_k+[\mathrm{VCM}-(1-b_k)\mathrm{VIP}^{(k+1)}-b_k\mathrm{VIN}^{(k+1)}]C_k=\\ (\mathrm{VRP}_k^{(k)}-\mathrm{VRN}_k^{(k)})\beta C_k+[\mathrm{VRP}_k^{(k)}-(1-b_k)\mathrm{VIP}^{(k)}-b_k\mathrm{VIN}^{(k)}]C_k\end{aligned}\tag{A-3}$$

Here the first term is the charge of the current bit reference charge capacitor, and the second term is the charge of the current bit capacitor. Similarly, at the reference bottom plate VRN we have

$$\begin{aligned}(\mathrm{VRN}-\mathrm{VRP})\beta C_k+[\mathrm{VCM}-(1-b_k)\mathrm{VIN}^{(k+1)}-b_k\mathrm{VIP}^{(k+1)}]C_k=\\ (\mathrm{VRN}_k^{(k)}-\mathrm{VRP}_k^{(k)})\beta C_k+[\mathrm{VRN}_k^{(k)}-(1-b_k)\mathrm{VIN}^{(k)}-b_k\mathrm{VIP}^{(k)}]C_k\end{aligned}\tag{A-4}$$

Finally, for the bits already decided, N-1 to k+1, the reference capacitors share charge when the potential of the CDAC top plate changes. At the P-side reference top plates, we have

$$\begin{aligned}(\mathrm{VRP}_i^{(k+1)}-\mathrm{VRN}_i^{(k+1)})\beta C_i+[\mathrm{VRP}_i^{(k+1)}-(1-b_i)\mathrm{VIP}^{(k+1)}-b_i\mathrm{VIN}^{(k+1)}]C_i=\\ (\mathrm{VRP}_i^{(k)}-\mathrm{VRN}_i^{(k)})\beta C_i+[\mathrm{VRP}_i^{(k)}-(1-b_i)\mathrm{VIP}^{(k)}-b_i\mathrm{VIN}^{(k)}]C_i\end{aligned}\tag{A-5}$$

Here $i=N-1,...,k+1$. The first term is the charge of the reference capacitor, and the second term is the charge of the bit capacitor. Similarly, at the N-side reference we have

$$\begin{aligned}(\mathrm{VRN}_i^{(k+1)}-\mathrm{VRP}_i^{(k+1)})\beta C_i[\mathrm{VRN}_i^{(k+1)}-(1-b_i)\mathrm{VIN}^{(k+1)}-b_i\mathrm{VIP}^{(k+1)}]C_i=\\ (\mathrm{VRN}_i^{(k)}-\mathrm{VRP}_i^{(k)})\beta C_i+[\mathrm{VRN}_i^{(k)}-(1-b_i)\mathrm{VIN}^{(k)}-b_i\mathrm{VIP}^{(k)}]C_i\end{aligned}\tag{A-6}$$

In summary, (A-1) to (A-6) are $2(N-k+1)$ charge conservation equations of an N-bit SAR-ADC with BS-RCRs from $(k+1)^{th}$ to $(k)^{th}$ bit decision.

From (A-1) to (A-6), we observe that the common mode voltages always stay at VCM.

$$\mathrm{VRP}_i^{(k)}+\mathrm{VRN}_i^{(k)}=\mathrm{VRP}+\mathrm{VRN}=2\mathrm{VCM}\tag{A-7}$$

$$\mathrm{VIP}^{(k)}+\mathrm{VIN}^{(k)}=\mathrm{VIP}+\mathrm{VIN}=2\mathrm{VCM}\tag{A-8}$$

A.2 Closed-Form Solution Derivation

Equation (A-1) can be re-written as

$$\mathrm{VIP}^{(k)} = \mathrm{VIP}^{(k+1)} + \frac{C_k}{C_T}[(1-b_k)\mathrm{VRP}_k^{(k)} + b_k\mathrm{VRN}_k^{(k)} - \mathrm{VCM}] + \sum_{i=k+1}^{N-1}\frac{C_i}{C_T}[(1-b_i)(\mathrm{VRP}_i^{(k)} - \mathrm{VRP}_i^{(k+1)}) + b_i(\mathrm{VRN}_i^{(k)} - \mathrm{VRN}_i^{(k+1)})] \quad \text{(A-9)}$$

Equation (A-9) shows the top plate voltage at the current bit k^{th} decision equals to the top plate voltage at the previous bit $(k+1)^{th}$ decision, and the changes in the current bit and the changes from the already decided bits. From (A-5) and (A-6), we can write $\mathrm{VRP}_i^{(k)} - \mathrm{VRP}_i^{(k+1)}$ and $\mathrm{VRN}_i^{(k)} - \mathrm{VRN}_i^{(k+1)}$ as a function of $\mathrm{VIP}^{(k)} - \mathrm{VIP}^{(k+1)}$ and $\mathrm{VIN}^{(k)} - \mathrm{VIN}^{(k+1)}$ respectively. Substitute them to term $\mathrm{VRP}_i^{(k)} - \mathrm{VRP}_i^{(k+1)}$ and $\mathrm{VRN}_i^{(k)} - \mathrm{VRN}_i^{(k+1)}$ in (A-9), we can obtain

$$\mathrm{VIP}^{(k)} = \mathrm{VIP}^{(k+1)} + \frac{\frac{C_k}{C_T}[(1-b_k)\mathrm{VRP}_k^{(k)} + b_k\mathrm{VRN}_k^{(k)} - \mathrm{VCM}]}{1 - \frac{1}{(2\beta+1)C_T}\sum\limits_{i=k+1}^{N-1} C_i} \quad \text{(A-10)}$$

Similarly, at the N-side we can obtain

$$\mathrm{VIN}^{(k)} = \mathrm{VIN}^{(k+1)} + \frac{\frac{C_k}{C_T}[(1-b_k)\mathrm{VRN}_k^{(k)} + b_k\mathrm{VRP}_k^{(k)} - \mathrm{VCM}]}{1 - \frac{1}{(2\beta+1)C_T}\sum\limits_{i=k+1}^{N-1} C_i} \quad \text{(A-11)}$$

The term $\mathrm{VRP}_k^{(k)}$ and $\mathrm{VRN}_k^{(k)}$ in (A-10) and (A-11), can be expressed by VRP, VRN and VCM through (A-3) and (A-4). Thus (A-10) and (A-11) can be simplified to

$$\mathrm{VIP}^{(k)} = \mathrm{VIP}^{(k+1)} + \frac{2\beta\frac{C_k}{C_T}(1/2 - b_k)[\mathrm{VRP} - \mathrm{VRN}]}{2\beta + 1 - \sum\limits_{i=k}^{N-1}\frac{C_i}{C_T}} \quad \text{(A-12)}$$

$$\mathrm{VIN}^{(k)} = \mathrm{VIN}^{(k+1)} + \frac{2\beta\frac{C_k}{C_T}(1/2 - b_k)[\mathrm{VRN} - \mathrm{VRP}]}{2\beta + 1 - \sum\limits_{i=k}^{N-1}\frac{C_i}{C_T}} \quad \text{(A-13)}$$

Substitute (A-12) and (A-13) into (A-5) and (A-6) we have

$$\mathrm{VRP}_i^{(k)} = \mathrm{VRP}_i^{(k+1)} + \frac{2\beta(1-2b_i)(1/2-b_k)C_k/C_T}{(2\beta+1)(2\beta+1-\sum\limits_{i=k}^{N-1}\frac{C_i}{C_T})}(\mathrm{VRP}-\mathrm{VRN}) \tag{A-14}$$

$$\mathrm{VRN}_i^{(k)} = \mathrm{VRN}_i^{(k+1)} + \frac{2\beta(1-2b_i)(1/2-b_k)C_k/C_T}{(2\beta+1)(2\beta+1-\sum\limits_{i=k}^{N-1}\frac{C_i}{C_T})}(\mathrm{VRN}-\mathrm{VRP}) \tag{A-15}$$

Substitute (A-12) and (A-13) into (A-3) and (A-4) we have

$$\mathrm{VRP}_k^{(k)} = \mathrm{VCM} + \frac{\beta(\mathrm{VRP}-\mathrm{VRN})}{(2\beta+1)}(1+\frac{C_k/C_T}{2\beta+1-\sum\limits_{i=k}^{N-1}\frac{C_i}{C_T}}) \tag{A-16}$$

$$\mathrm{VRN}_k^{(k)} = \mathrm{VCM} + \frac{\beta(\mathrm{VRN}-\mathrm{VRP})}{(2\beta+1)}(1+\frac{C_k/C_T}{2\beta+1-\sum\limits_{i=k}^{N-1}\frac{C_i}{C_T}}) \tag{A-17}$$

A.3 Derivation of Sample-wise Switched RCR Equations

For the SAR-ADC with SS-RCRs, there is no external sources is added during the conversion phase. So, for each bit decision, the charge conservation equation can relate to the charge at the end of the sample phase. The reference capacitance is the $\beta * C_T$, where C_T is the sum of capacitance from C_0 to C_{N-1}. At the k^{th} bit decision, the charge on the top plate of the P side bit capacitor array is conservative; i.e.

$$(\mathrm{VIP}-\mathrm{VCM})C_T = (\mathrm{VIP}^{(k)}-\mathrm{VRP}^{(k)})\sum_{i=k}^{N-1}(C_i(1-b_i)) + (\mathrm{VIP}^{(k)}-\mathrm{VRN}^{(k)})\sum_{i=k}^{N-1}(C_ib_i) + (\mathrm{VIP}^{(k)}-\mathrm{VCM})\sum_{i=0}^{k-1}(C_i) \tag{A-18}$$

The term in (A-18) at the left-hand side represents the charge at the end of sampling. The first term at the right-hand side is the charge of the CDAC that connects to VRP, the second term is the charge of the CDAC that connects to VRN, and the third term is the charge of the undecided bits. Similarly, at the N side we have

$$(\mathrm{VIN}-\mathrm{VCM})C_T = (\mathrm{VIN}^{(k)}-\mathrm{VRN}^{(k)})\sum_{i=k}^{N-1}(C_i(1-b_i)) + (\mathrm{VIN}^{(k)}-\mathrm{VRP}^{(k)})\sum_{i=k}^{N-1}(C_i b_i) + (\mathrm{VIN}^{(k)}-\mathrm{VCM})\sum_{i=0}^{k-1}(C_i) \quad \text{(A-19)}$$

Second, the charge conserved on the reference charge capacitance. At the top plate at the end of sampling to the k^{th} bit decision, we have

$$(\mathrm{VRP}-\mathrm{VRN})\beta C_T + (\mathrm{VCM}-\mathrm{VIP})\sum_{i=k}^{N-1}(C_i(1-b_i)) + (\mathrm{VCM}-\mathrm{VIN})\sum_{i=k}^{N-1}(C_i b_i) = (\mathrm{VRP}^{(\mathrm{k})}-\mathrm{VRN}^{(\mathrm{k})})\beta C_T + (\mathrm{VRP}^{(\mathrm{k})}-\mathrm{VIP}^{(\mathrm{k})})\sum_{i=k}^{N-1}(C_i(1-b_i)) + (\mathrm{VRP}^{(\mathrm{k})}-\mathrm{VIN}^{(\mathrm{k})})\sum_{i=k}^{N-1}(C_i b_i) \quad \text{(A-20)}$$

Similarly, at the bottom plate from sampling phase to the k^{th} bit decision, we have

$$(\mathrm{VRN}-\mathrm{VRP})\beta C_T + (\mathrm{VCM}-\mathrm{VIN})\sum_{i=k}^{N-1}(C_i(1-b_i)) + (\mathrm{VCM}-\mathrm{VIP})\sum_{i=k}^{N-1}(C_i b_i) = (\mathrm{VRN}^{(\mathrm{k})}-\mathrm{VRP}^{(\mathrm{k})})\beta C_T + (\mathrm{VRN}^{(\mathrm{k})}-\mathrm{VIN}^{(\mathrm{k})})\sum_{i=k}^{N-1}(C_i(1-b_i)) + (\mathrm{VRN}^{(\mathrm{k})}-\mathrm{VIP}^{(\mathrm{k})})\sum_{i=k}^{N-1}(C_i b_i) \quad \text{(A-21)}$$

Note that in the bit decision process of the SAR-ADC with SS-RCR, the common mode of the reference $\mathrm{VRP}^{(\mathrm{k})}$ and $\mathrm{VRN}^{(\mathrm{k})}$, and the common mode of the top plate voltages $\mathrm{VIP}^{(\mathrm{k})}$ and $\mathrm{VIN}^{(\mathrm{k})}$ stay at the VCM. Solving (A-18) to (A-21), we obtain

$$\mathrm{VIP}^{(k)} = \mathrm{VIP} + \sum_{i=k}^{N-1}\frac{C_i}{C_T}(\frac{1}{2}-b_i)(\mathrm{VRP}-\mathrm{VRN}) * \frac{2\beta}{2\beta + \frac{\sum_{i=k}^{N-1} C_i}{C_T} - [\frac{\sum_{i=k}^{N-1} C_i(2b_i-1)}{C_T}]^2} \quad \text{(A-22)}$$

$$\mathrm{VRP}^{(k)} = \frac{2\beta}{2\beta + \frac{\sum_{i=k}^{N-1} C_i}{C_T} - [\frac{\sum_{i=k}^{N-1} C_i(2b_i-1)}{C_T}]^2}\mathrm{VRP} + \frac{\frac{\sum_{i=k}^{N-1} C_i}{C_T} - [\frac{\sum_{i=k}^{N-1} C_i(2b_i-1)}{C_T}]^2}{2\beta + \frac{\sum_{i=k}^{N-1} C_i}{C_T} - [\frac{\sum_{i=k}^{N-1} C_i(2b_i-1)}{C_T}]^2}\mathrm{VCM} \quad \text{(A-23)}$$