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System and Analog Front-End Design for
Wireless Optogenetics and Marine Mammal Science

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Abstract

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The first part of this thesis will present a low-noise, low-power Analog Front-End (AFE) for acoustic and ocean pressure detection used in marine mammal science applications. First, the design of a test chip consisting of three AFE variations with a common two-stage amplifier will be analyzed. The primary goal for the first iteration chip was to explore tradeoffs between noise and power as well as to perform basic interfacing with a hydrophone sensor; this in preparation for the second iteration system. The measured test results of this fabricated chip are discussed in detail. Second, a deployable system built upon the test chip and improved with several features such as power-gating, variable gain, and frequency scaling will be presented. This system includes digitization of sonar and pressure signals through an 8-bit successive approximation ADC. An SPI interface was added to the design in order to be compatible with a System-on-Chip developed by a collaborative team from the University of Virginia.

In the second part of this work, a system for wireless optogenetics will be presented. First, an overview of the optogenetics science will be covered, as well as a brief description of the state-of-the-art stimulation systems used in this field. Next, a high-level overview of the proposed system will be presented followed by a detailed description of the main blocks. The last section will contain applicable metric measurements and the results obtained from an in-vivo experiment conducted using our system.

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DEDICATION

I would like to dedicate this work to my dear wife Melissa and daughter Miranda.

Chapter 1

INTRODUCTION

1.1 Sonar and Marine Wildlife

Over the last 20 years, there has been increasing concern about the impact of human-introduced noise on marine wildlife. Recent works have shown a direct link between human-produced sounds and the disruption of marine mammal communication, internal injury and even mass strandings [18]. In the past, it was thought that injury to marine wildlife could only occur tens of meters away from loud sounds such as those from military sonars. However, mass strandings of beak whales coincided with naval sonar exercises involving mid-frequency sonars (MFS) conducted tens of kilometers away [8]. Another aspect of sonar that did not agree with the observed beak whale strandings is that MFS, which operate in the 3-8 kHz range, is much lower than the whale echolocation communication, which centers at around 40 kHz [25]. A hypothesis to explain the discrepancy of the frequency bands is that the harmonics of the fundamental sonar frequency carry enough energy over long distances to affect marine animals. However, it is important to conduct research and resolve these issues as they affect policies and regulations concerning the well being of the general marine wildlife.

1.2 Cause and Effect

On March 15th and 16th, 2000, a mass whale stranding occurred on the beaches of the Bahamas, as reported in [11]. Up to 17 cetaceans were found stranded in various locations, ten were alive and were returned to the ocean but seven died due to intense auditory trauma. This mass stranding event coincided with Naval tactical mid-range frequency activity which led to an intense investigation. The National Oceanic and Atmospheric Administration (NOAA) concluded in [11] that the leading cause for the strandings and death of some of the animals was the tactical mid-range frequency sonar used by the Navy.

1.3 Impact Detection Challenges

Studying the effects of MFS on whales in uncontrolled conditions proves to be very challenging. Visually observing the behavior of these whales during sonar exercises is an ineffective method as many of these deep-diving species only surface 5% of the time [18]. Another method is to use passive acoustic monitoring, that is, to listen for whale response to sonar stimuli. This also proves inadequate as species (e.g. sperm whales [27]), become silent during sonar exposure offering no real insight of the response. Thus, without knowing parameters such as diving depth, direction and orientation, it becomes extremely hard to predict the behavior of these species in the presence of sonar.

1.4 Limitations of Early Works

Early works have presented on-animal continuous tag recording systems such as the DTAG in [18] and the compact acoustic probe (CAP) in [28]. Though these systems have been deployed and produced valuable data, they are severely limited by the high power consumption of their off-the-shelf components. Both of these systems reported a power consumption of 150 mW during recording. Another limitation of early efforts is the large area and weight of their on-board components, battery and enclosure. The total weight of the DTAG and CAP is 0.5 kg and 0.9 kg respectively. Although, large whales can carry big tags, the difficulty arises when attaching the device to the animal via a long pole or bow arrow [18]. These two constraints call for a more integrated and low-power approach.

1.5 Research Approach

This work will describe an integrated Analog Front-End (AFE) aimed to be a low-noise, low-power solution for sonar and depth detection. This design will be paired with a System-on-Chip (SoC) developed by a collaborative team from University of Virginia (UVA). The ultimate goal for the overall system is to be deployed in real experiments and to have a high degree of configurability to adjust to the environments. Aggressive performance metrics will be targeted in power consumption, noise and ease-of-use.

1.6 Thesis Organization

This thesis will consists of six chapters and two topics. The first topic will be covered in Chapters 1-4 and the second topic will be covered in Chapter 5. Chapter 2 will explain the sonar and echolocation frequency bands as well as the noise specifications. Chapter 3 contains a complete design analysis of a test chip as well as measured results and a brief discussion. Chapter 4 covers the design for a deployable system, details for the main blocks and simulated results. Chapter 5 will present a wireless system for optogenetics. Finally, Chapter 6 will summarize and conclude both topics.

Chapter 2

SIGNAL DETECTION IN THE OCEAN**2.1 Introduction**

Before starting the design process, it is useful to provide some background on the type of signals that are involved. In this chapter, an overview of the sonar and echolocation frequency bands will be covered. Also, included is a short section on the sensors that are typically used to measure pressure and sonar signals. Lastly, a section on noise will help derive a noise specification which will become the basis for the subsequent design.

2.2 Sonar, Echolocation and Hearing Sensitivity Frequency Bands

As stated in the previous chapter, MFS center at much lower frequencies than the echolocation frequency used by whales to communicate and for navigation. Typical active sonars used by the Navy center at 2.6 kHz and 3.3 kHz with a source level of 235 dB re 1 μ Pa and at 6.8 kHz and 8.2 kHz with a source of 235 dB re 1 μ Pa [11]. Beak whales produce echolocation clicks centered at about 42 kHz with source levels between 200-220 dB re 1 μ Pa and a -10 dB bandwidth of 22 kHz [32]. Other literature provides similar information. For example, the work presented in [5] describes a compressive study on echolocation signals and it states that all echolocation peak frequencies collected from a variety of beaked whales species range from 16 kHz to 66 kHz. Figure 2.1 aims to piece together the information about echolocation and sonar frequencies found thus far. Also, on this plot, is the hearing sensitivity of an average beak whale as a function of frequency.

Referring to Figure 2.1, we see that the center frequencies for the echolocation and sonar do not directly overlap, but are close enough to interfere if the fundamental tone or its harmonics carry enough energy. A whale's hearing sensitivity on the other hand, goes beyond the frequency band of their emitted echolocation clicks. For example, in an auditory study on a stranded juvenile beak whale, it was found that its auditory system

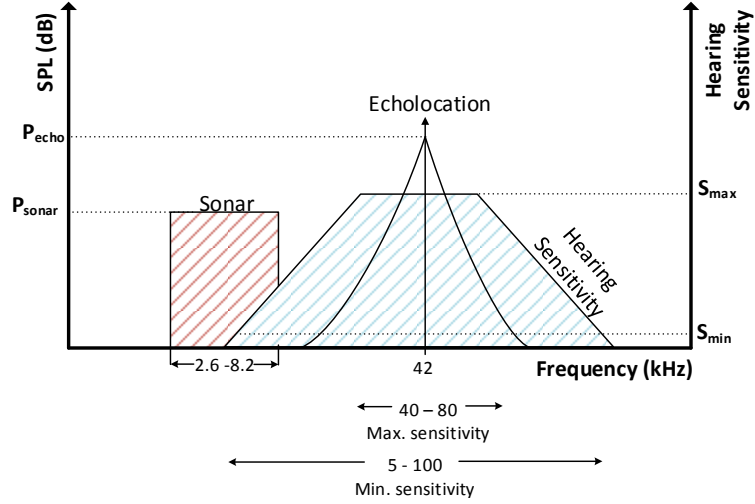


Figure 2.1: Sonar, echolocation and hearing sensitivity frequency bands

is most sensitive to frequencies between 40 and 80 kHz but goes as low as 5 kHz [6]. This study does make it clear that 5 kHz was the lowest frequency tested, suggesting that a whale's hearing sensitivity could expand to even lower frequencies.

From the information above, several insights can be gained. First, the overlap of frequency hearing sensitivity and sonar frequencies seems to be the cause for the observed hearing injury to these marine mammals. Second, even though sonar and echolocation do not directly overlap, a strong sonar signal can interfere with a whale's echolocation clicks potentially disrupting their communication. Thirdly, due to the proximity of the echolocation signal to a sonar sensing system, communication among whales is likely to saturate the electronics. Hence, echolocation suppression filtering should be included in the later stages of the proposed system.

2.3 Pressure Sensing

Measuring depth is important in order to observe a whale's diving pattern in the presence of sonar. Ocean depth measurements can be realized using a piezoresistive transducer as the

one shown in Figure 2.2 (same sensor in two forms). These Wheatstone bridge transducers offer high sensitivity, wide operating range and temperature compensation in ocean depth measurements [2]. Furthermore, these rugged sensors can sustain the intense pressures experienced in a deep dive which can reach over 3000 psi [31].

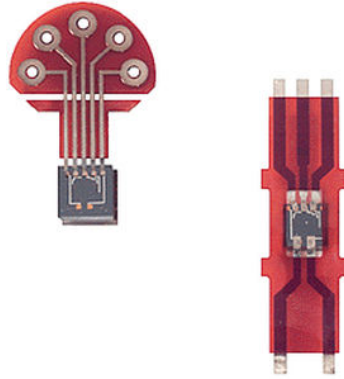


Figure 2.2: Wheatstone-based piezoresistive pressure sensor from KELLER

When measuring pressure signals, low sampling frequencies are typically desired as the water pressure changes slowly during a whale’s dive. The mean descend and ascent rates are 1.5 m/s and 0.7 m/s respectively, as reported in [24]. Previous works that have measured slow moving signals (e.g. pressure, orientation) during diving events, have used sampling frequencies below 50 Hz [18]. Also, in previous deployed prototypes preceding this work, it was found that reading ocean depth pressures every 1 second is more than sufficient. A detailed section on how to generate a 1 Hz sampling signal will be presented in Chapter 4. One advantage of ultra-low sampling frequency is that it relaxes the power consumption of the depth amplifier (covered in Chapter 4).

2.4 Sonar Detection

2.4.1 Hydrophone and Preamplifier

In a similar way that a microphone is used in air to detect sound, a hydrophone is used in water to detect sound pressure waves. When an object vibrates in water, a sound-pressure wave compresses and decompresses water molecules as it travels through the ocean[19]. The

sound-pressures emitted by MFS are typically low in amplitude therefore a pre-amplification stage is needed. All of the electrical components of the preamplifier will add noise to the signal which is already mixed with the background noise of ocean. The goal of the hydrophone-preamplifier pairs is to maximize the signal to noise ratio (SNR) so that the later stages can process the purest signal possible. The ocean background noise is out of the reach of the designer but its level determines the impact of the electrical noise from the preamplifier on the SNR.

2.5 Ambient Noise

Ambient noise is defined as “unwanted sound” [4]. For any sonar system, it is important to quantize the noise level (NL) in order to be able to detect signals in noise. The ability to gather information about the NL becomes crucial when trying to maximize the signal-to-noise ratio or SNR [22]. Ambient noise quantizations have been widely studied in the works by Wenz, Fox and Anderson described in [29], [12] [1]. These works have yielded very useful data that well characterizes the ambient noise in the ocean.

Ambient noise is an inherent characteristic of a given medium and has no specific point of source [22]. The measure of the NL is done by measuring its intensity and can be calculated as the RMS pressure of a plane wave relative to a reference pressure of $1\mu Pa$ in water ($20\mu Pa$ in air) over a 1 Hz bandwidth [26]. Acoustic intensity can be expressed by,

$$NL = 10\log(I/I_{ref}) \quad (2.1)$$

Where I is the intensity of the ambient noise referenced to $I_{ref} = 1\mu Pa$ for water. While acoustic intensity, which is the fundamental measurement of the propagation of sound [7], is of interest to acoustic engineers, it is not useful in the practical sense. Since hydrophones measure pressure and convert it into voltage, we need a measurement metric of pressure instead. This measurement is known as the Sound Pressure Level (SPL). Intensity is proportional to RMS pressure, thus a ratio of pressures is used to quantify the SPL,

$$SPL(dB re 1\mu Pa) = 20\log(P/P_{ref}). \quad (2.2)$$

As mentioned before, previous works have throughly studied the ambient noise in the ocean. A particular set of curves described in [29] (and shown in Figure 2.3) can be useful

in determining the SPL of the ambient noise which in turn can be converted into a voltage quantity. This noise voltage level can serve as the noise threshold for our AFE. The information contained within the Wenz curves gives a good indication of noise pressure level at a particular frequency. In a previous section it was determined that MFS range from 2.6 kHz to 8.2 kHz. Therefore, by looking at the Wenz curves for this frequency range, it is possible to estimate the noise pressure level, thus establishing the noise floor threshold for the sonar AFE. Based on the Wenz curves, a typical noise of 80 dB re μ Pa/ would be encountered at 1kHz. From this information and the using the sensitivity (-230 dB re 1V/ μ Pa) of a standard hydrophone, it is possible to estimate the noise floor V_{nf} for the sonar AFE,

$$[80dB + (-230dB)] \text{ re } 1\mu Pa = -150 \text{ dB re } 1\mu Pa \quad (2.3)$$

$$-150dB = 20\log_{10}\left(\frac{V_{nf}}{V_{ref}}\right) \quad (2.4)$$

$$V_{nf} = 10^{-150/20} = \frac{31nV}{\sqrt{Hz}} \quad (2.5)$$

Based on the noise floor estimation found in (2.5), it can be concluded that in order to effectively detect sonar signals, the intrinsic noise of the sonar AFE should be below this noise floor threshold. Meeting this noise specification should allow us to detect any signal that is above the noise floor. In this work, an input-referred noise of 12 nV/ \sqrt{Hz} is targeted at 1 kHz.

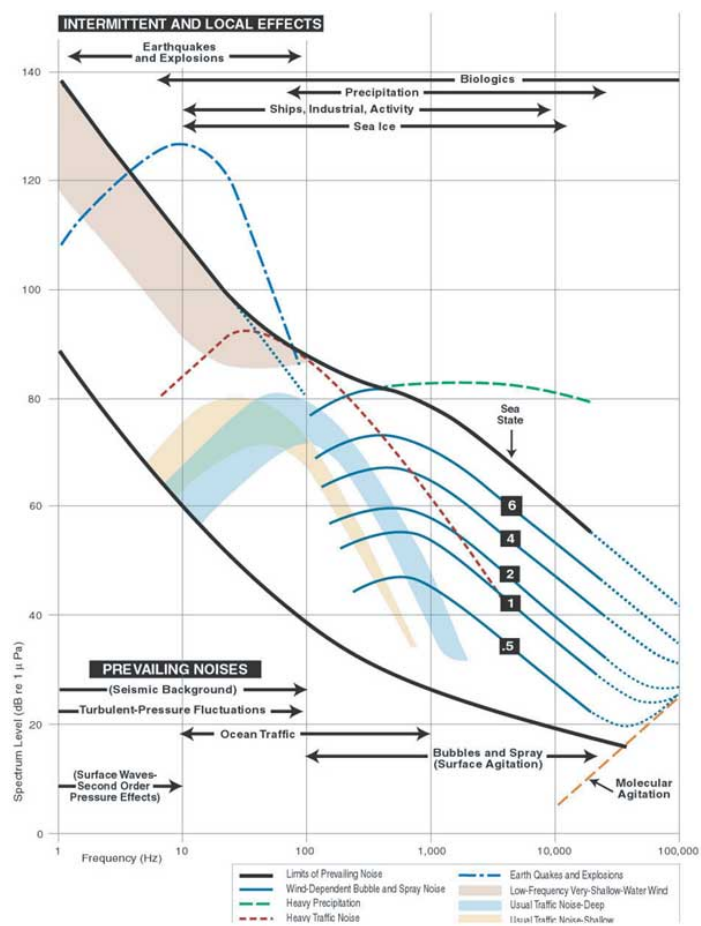


Figure 2.3: Wenz Curves showing ocean background noise vs. frequency

Chapter 3

TEST CHIP DESIGN

3.1 Introduction

Shown in Figure 3.1 are the three amplifiers designed and fabricated in the test chip. The three amplifiers called sonar, depth, and VGA were designed for low noise, low power, and variable gain, respectively. All three topologies are based on the same core two-stage amplifier with variations in bias current and capacitive feedback network values. For simplicity, the design details and results will be covered only for the sonar and VGA topologies.

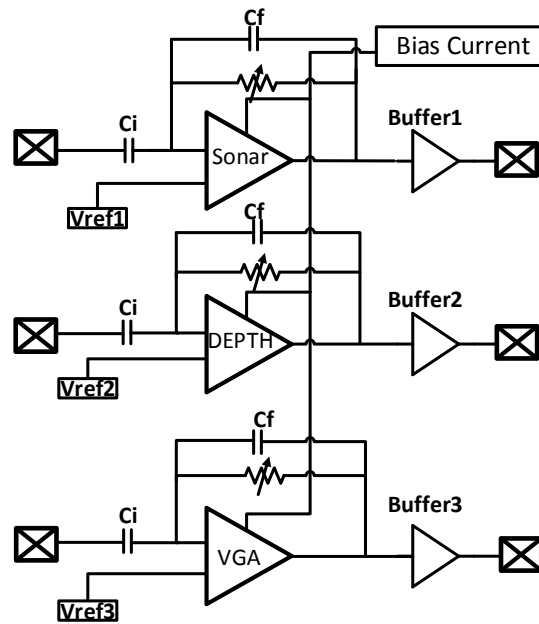


Figure 3.1: Test chip top-level diagram

3.2 Two-stage Operational Amplifier Design

In this section, we design an LNA based on a standard two-stage operational amplifier (shown in Fig. 3.2). This robust topology is used widely in analog blocks and offers good performance in noise, gain, and output swing [21].

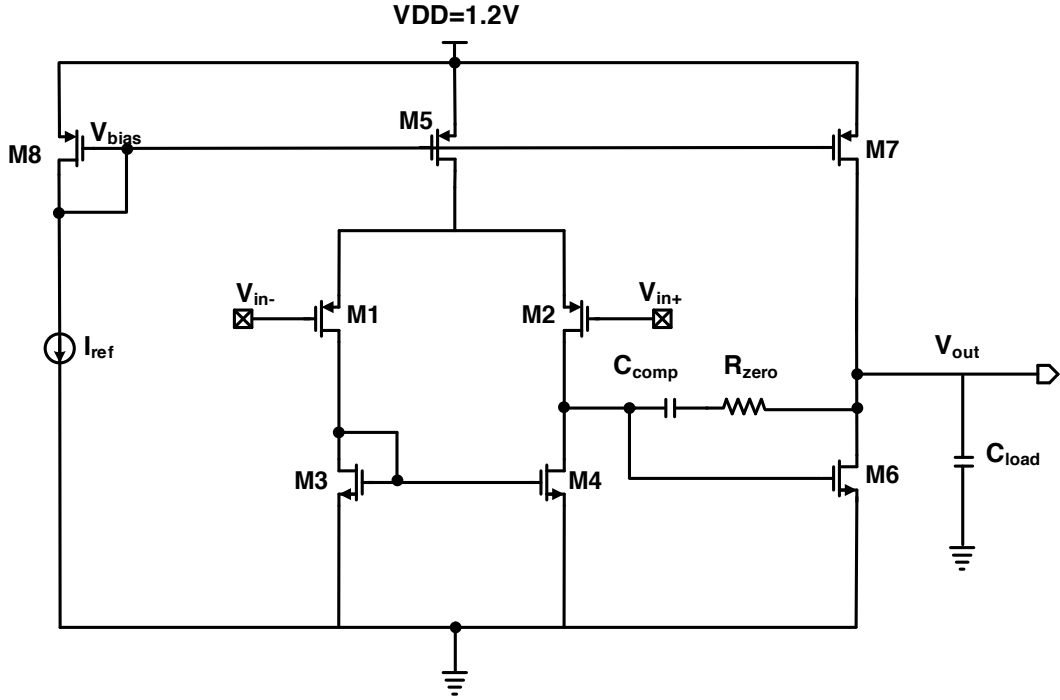


Figure 3.2: LNA transistor-level schematic

The input-referred noise voltage for this topology is derived in [21] and expressed as,

$$\overline{V_{n,in}^2} = 8kT \left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2} \right) + \frac{2K_P}{C_{ox}(WL)_1 f} + \frac{2K_N}{C_{ox}(WL)_3 f} \frac{g_{m3}^2}{g_{m1}^2} \quad (3.1)$$

From this expression, it is clear that in order to minimize the input-referred noise, it is necessary to increase the transconductance of M1 as well as the device dimensions of M1 and M3. Note that (3.1) only refers to M1 and M3 but since these are symmetrical branches, $M1=M2$ and $M3=M4$.

Next, since g_{m3} is on the numerator, we should set $g_{m3} < g_{m1}$ which can be accomplished by adjusting the aspect ratios of M1 and M3.

K_P and K_N are flicker noise, process dependent, constants for the PDK standard PMOS and NMOS, respectively. The K_P and K_N values can be estimated empirically by flicker noise simulations and using the transistor flicker noise model given by (3.2), [21].

$$\overline{V_n^2} = \frac{K}{C_{ox}(WL)} \cdot \frac{1}{f} \quad (3.2)$$

The process for finding these constants consisted of measuring the output noise voltage at 1 Hz from a single transistor with a bias current of $1\mu A$ and $1\mu m/1\mu m$ for the aspect ratio.

$$\frac{K}{C_{ox}} = \overline{V_n^2}(WL)f \quad (3.3)$$

These values were then plugged into (3.3) and the following approximated results for $\frac{K}{C_{ox}}$ were obtained,

$$\frac{K_N}{C_{ox}} = 22pV^2 \times 1\mu m \times 1\mu m \times 1Hz = 22 \times 10^{-24}V^2\mu m^2 \quad (3.4)$$

$$\frac{K_P}{C_{ox}} = 80pV^2 \times 1\mu m \times 1\mu m \times 1Hz = 80 \times 10^{-24}V^2\mu m^2. \quad (3.5)$$

Next, the value of g_{m1} can be approximated by providing a target white noise voltage at high frequencies such that the second and third term in (3.1) approach zero. Based on research on commercial low-noise operational amplifiers a target white noise voltage of $3 \text{ nV}/\sqrt{Hz}$ was chosen— similar to Texas Instruments OPA227 series. Following are the calculations for finding g_{m1} ,

$$\overline{V_{n,in}^2} = 8kT \frac{2}{3g_{m1}} \quad (3.6)$$

$$g_{m1} = 8kT \frac{2}{V_{n,in}^2} \quad (3.7)$$

$$= \frac{16 \times 1.38 \times 10^{-23} \times 300}{3 \times 10^{-9}} \quad (3.8)$$

$$= 5mS \quad (3.9)$$

Next, the product of $(WL)_{1,3}$ can be estimated by assuming low frequencies (where flicker noise dominates) and setting the following constraints:

- $\overline{V_{n,in}^2} = \frac{12nV}{\sqrt{Hz}}$
- $g_{m3} < g_{m1}$
- $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3 = \frac{W}{L}$

Thus, (3.1) can be approximated by

$$\overline{V_{n,in}^2}(1kHz) \approx \frac{2K_P}{C_{ox}(WL)_1 f} + \frac{2K_N}{C_{ox}(WL)_3 f} \frac{g_{m3}^2}{g_{m1}^2} \quad (3.10)$$

Which yields the product of WL to be:

$$LW \approx \frac{1}{1.44 \times 10^{-16}} \cdot \left(\frac{2 \times 80 \times 10^{-24}}{1 \times 10^3} + \frac{2 \times 22 \times 10^{-24}}{1 \times 10^3} \cdot \left(\frac{1}{4}\right) \right) \quad (3.11)$$

$$LW = 1.18nm^2 \quad (3.12)$$

Thus, if $L=500$ nA, $W = 2.3$ mm and $\left(\frac{W}{L}\right)_{1,2} = \left(\frac{2.3mm}{500nm}\right)$.

Based on 3.1, in order to lower the input-referred noise, it is necessary to satisfy $g_{m1} > g_{m3}$. This can be accomplished by driving M1 in weak inversion such that g_m/I_D is maximized. The following expression estimates the moderate inversion characteristic current I_S , [14],

$$I_S = \frac{2\mu C_{ox} U_T^2}{\kappa} \left(\frac{W}{L}\right) \quad (3.13)$$

Where U_T is the thermal voltage and at room temperature, it reduces to approximately 0.026 V. κ is the gate coupling coefficient and has an approximate value of 0.7 [14]. The inversion coefficient, IC , of all transistors can be found by,

$$IC = \frac{I_D}{I_S} \quad (3.14)$$

For transistors in strong inversion, $IC > 10$, moderate inversion $10 > IC > 0.1$ and weak inversion $IC < 0.1$. Note that the given expression for devices in moderate inversion, both weak and strong inversion, overestimate the transconductance [14]. Thus using the EKV model proves more adequate in this case, since it is valid in all operation regions and gives a more accurate solution. The EKV model relates I_D and g_m as follows:

$$g_m \approx \frac{2\kappa I_D}{U_T(1 + \sqrt{1 + 4IC})} \quad (3.15)$$

$$I_D \approx g_m \frac{U_T(1 + \sqrt{1 + 4IC})}{2\kappa} \quad (3.16)$$

Using the expression given by (3.16) and setting the $IC = 0.1$ for weak inversion operation of M1, a value for I_{D1} (and thus the current for M1-M4) can be finally obtained:

$$I_{D1} \approx \frac{0.005 \times 0.026(1 + \sqrt{1 + 4 \times 0.1})}{2 \times 0.7} = 200\mu A \quad (3.17)$$

Next, we find g_{m6} .

For a two-stage amplifier, for which the frequency behavior can be characterized by the non-dominant pole (f_{SP}) [14], the phase margin is expressed as

$$M_\Phi = 90^\circ \times \arctan \frac{f_{GBW}}{f_{SP}} \quad (3.18)$$

Our amplifier was designed for $f_{GBW} = 25MHz$, $M_\Phi = 70^\circ$ and $C_L = 10pF$. By using equation (3.18), we obtain $f_{SP} = 68.7MHz$. The transconductance of M6 is related to the non-dominant pole as follows,

$$f_{SP} = \frac{g_{m6}}{2\pi C_L} \quad (3.19)$$

Thus the transconductance of M6 reduces to

$$g_{m6} = 2\pi f_{GBW} C_L \tan(M_\Phi) \quad (3.20)$$

$$= 2\pi \times 25 \times 10^6 \times 10 \times 10^{-12} \times \tan(70) = 4.3mS \quad (3.21)$$

With knowledge of g_{m6} we can find the value for the compensation capacitor

$$C_C = K \frac{g_{m1}}{g_{m6}} C_L \quad (3.22)$$

Where K is the separation factor between the second pole and the gain bandwidth product [20],

$$K = \frac{f_{SP}}{f_{GBW}} \approx 2.7 \quad (3.23)$$

Thus, (3.23) evaluates to $C_C = 27pF$. The addition of the compensation capacitor creates a RHP zero. In order to eliminate this zero or move it to the LHP, a method suggested in [21] is applied,

$$R_Z \approx \frac{C_L + C_C}{g_{m6} C_C} = \frac{10 \times 10^{-12} + 27 \times 10^{-12}}{4.3 \times 10^{-3} \times 27 \times 10^{-12}} = 318\Omega. \quad (3.24)$$

Table 3.1 shows the operating points for transistors of the two-stage op-amp. As we can see, the areas of M1 and M2 are quite large, this directly helps reduce the input-referred noise. Also, note that in order to satisfy $g_{m3} < g_{m1}$, a high g_m/I_D was required; this could only be met by driving M1 and M2 in weak inversion.

Table 3.1: Operation points of the LNA core transistors

Device	W/L (μm)	$I_D(\mu\text{A})$	Inversion Coefficient	$I_D/g_m(V^{-1})$
M1, M2	2300/0.5	200	0.1	23.5
M3, M4	200/10	200	3.8	10.9
M5	400/4	400	18.0	5.7
M6	100/0.7	209	0.42	20.8
M7	200/4	209	18	5.7
M8	10/4	10	19.1	5.6
M9	10/4	10	15.7	6.1

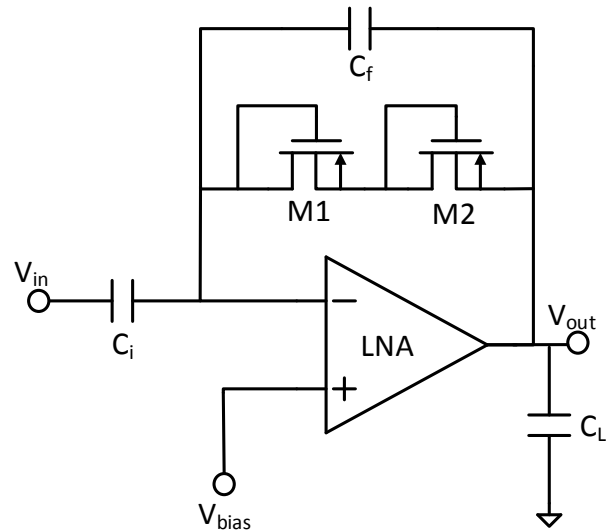


Figure 3.3: Schematic for sonar AFE

3.3 Sonar AFE

Having designed the core LNA, we can now design the front-end amplifier. The chosen AFE amplifier is the simple capacitive feedback topology shown in Figure 3.3. The reason for using capacitors instead of resistors was to avoid the high resistive thermal noise given by the fundamental equation,

$$\overline{V_{n,in}^2} = 4kTR \quad (3.25)$$

Another reason for choosing the mentioned topology is that the gain can be easily set by a simple capacitor ratio,

$$A_v = C_i/C_f \quad (3.26)$$

Equation (3.26) holds true as long as $C_i, C_L \gg C_f$. For the first iteration, the ratio of C_i/C_f was chosen to be $40pF/5pF$ yielding a gain of only 18 dB.

Another consideration when choosing the AFE topology was the frequency response. A band-pass response is needed for mid-frequency sonars (3-8 kHz) while rejecting DC. This presented a challenge due to the extremely high RC constant required for a sub-kHz corner frequency. Realizing this RC constant with an on-chip resistor would occupy a prohibitively large area, therefore the decision was made to use pseudoresistors instead. Figure 3.3 shows two diode connected PMOS transistor (M1 and M2) that function as pseudoresistors and which can achieve resistances in the order of $10^{11}\Omega$. With a negative V_{GS} , the parasitic p-n-p bipolar junction transistor gets activated and makes M1 and M2 behave as diode-connected BJT. Using the high resistance provided by the pseudoresistors, the low frequency cutoff can now approximated by,

$$f_L = \frac{1}{2R_{inc}C_f} \quad (3.27)$$

Where R_{inc} is the incremental resistance of the pseudoresistors and C_f is the feedback capacitance. In Figure 3.4 we see that for small voltages across M1 and M2 the resistance is close to $250M\Omega$ and decreases for larger voltages drops across them. This becomes

the detrimental aspect of pseudoresistors, namely that we cannot accurately control the resistance. In Figure 3.5, as expected, we see a very small amount of current (less than 5pA) through M1 and M2 due to the high resistance path. One major concern for using pseudoresistors in LNAs is flicker noise. This effect was reduced by using PMOS devices as they offer one to two orders of magnitude less noise than NMOS transistors as long as $|V_{GS}|$ does not greatly exceed V_{TH} [14].

Another aspect to consider is how much noise is introduced with the capacitive feedback. Based on equation (3.1), the flicker noise on the two-stage amplifier reduces as the areas of $M_{1,2}$ and $M_{3,4}$ are increased. However, as the the area of the input pair increases, the input capacitance C_{in} also increases. The input-referred noise of the sonar AFE relates to the input-referred noise of the two-stage op-amp as follows [14],

$$\overline{V_{n,AFE}} = \left(\frac{C_i + C_f + C_{in}}{C_i} \right) \overline{V_{in,op}} \quad (3.28)$$

Where C_i and C_f are the input and feedback capacitors, respectively, and C_{in} is the capacitance looking into the gate of M1. Thus increasing the size of the input pair, increases C_{in} and the capacitive divider, ultimately attenuating the signal and contributing to the input-referred noise of the overall AFE. Therefore, from (3.28) it is clear that maximizing C_f reduces the noise contributed by the capacitive feedback.

As an additional point, V_{bias} in Figure 3.3 was provided externally for this test chip.

3.4 VGA AFE

In the preceding section, the sonar AFE achieved a gain 18 dB by using 40 pF for C_{in} and 5 pF for C_f . However, from equation (3.28) we see that in order to suppress the input-referred noise caused by the capacitive attenuation, C_f should be minimized and C_i maximized. In this section a variable gain amplifier (VGA) AFE, able to achieve higher gains than the sonar AFE, is presented. Figure 3.6 shows a gain-configurable topology that uses NMOS switches to control the amount input capacitance C_i . The closed-loop voltage gain can be

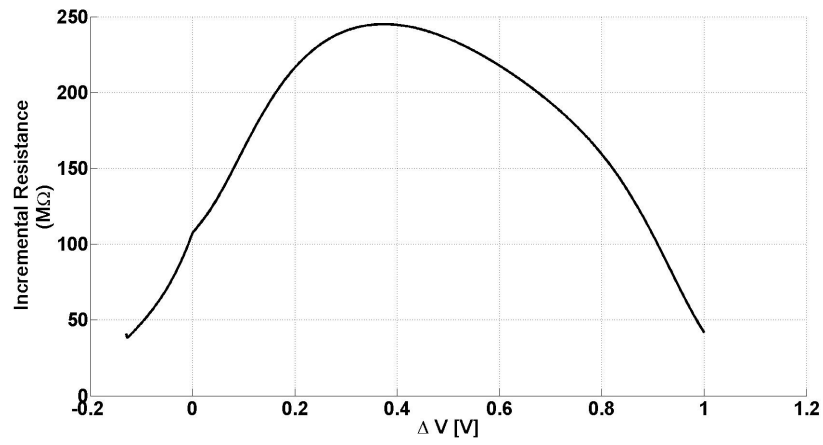


Figure 3.4: Incremental resistance of two series pseudo elements

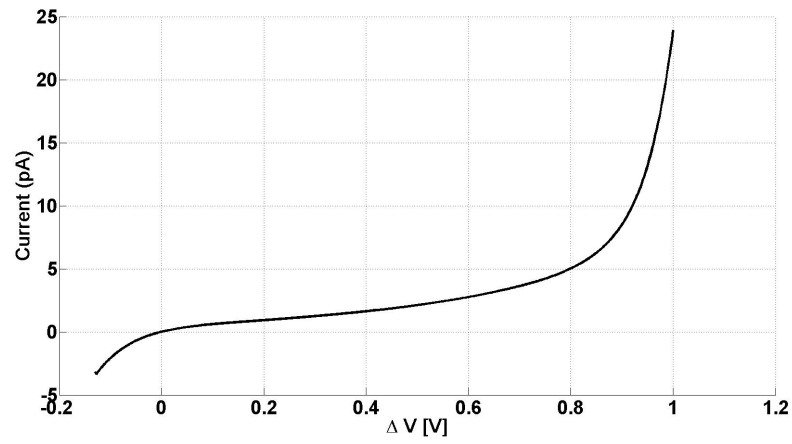


Figure 3.5: Current-voltage relation of pseudo elements

calculated by,

$$A_{V(CL)} = \frac{C_{i,tot}}{C_f} \quad (3.29)$$

Where $C_{i,total} = C_0 + C_{i1} + C_{i2} + C_{i3}$. The capacitor values used in the high-gain mode of

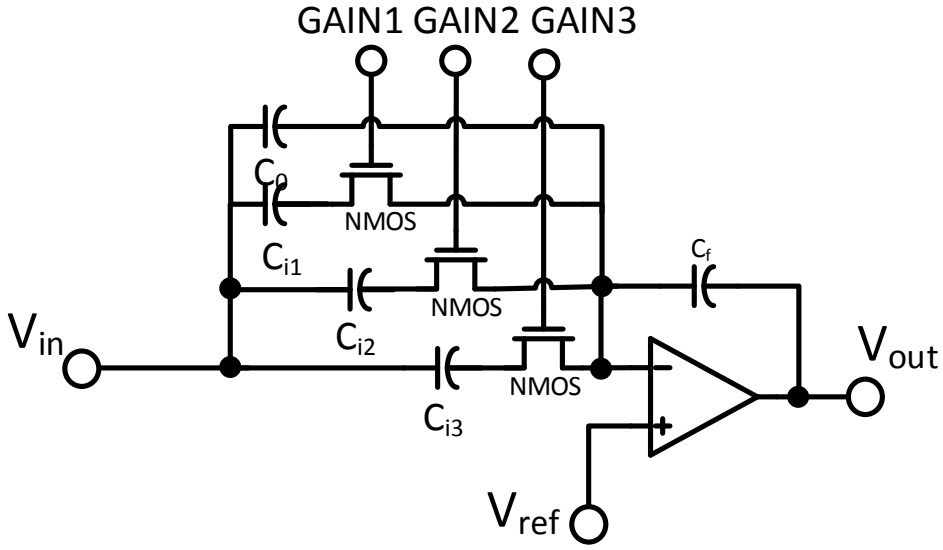


Figure 3.6: Schematic for VGA AFE

the VGA are 5, 5, 20, 30 pF. Thus, the maximum achievable closed-loop gain is:

$$A_{V(CL)} = \frac{5pF + 5pF + 20pF + 30pF}{1pF} = 60V/V = 35.6dB \quad (3.30)$$

3.5 Simulated Noise Results

Figure 3.7 shows the simulated input-referred noise of the two-stage core amplifier. The spot noise at 1 kHz is $7.3nV/\sqrt{Hz}$ lower than the target noise of $12nV/\sqrt{Hz}$ set in section 3.2. At 100 kHz, where the thermal noise dominates, the noise is $2.9nV/\sqrt{Hz}$, this agrees well with the design target of $3nV/\sqrt{Hz}$. It is worth noting that trying to meet the noise specification was a highly iterative process due to the tradeoffs involved (i.e. bandwidth,

power etc.). Therefore, even though the design and resulting values do not match exactly, they come to a fair approximation.

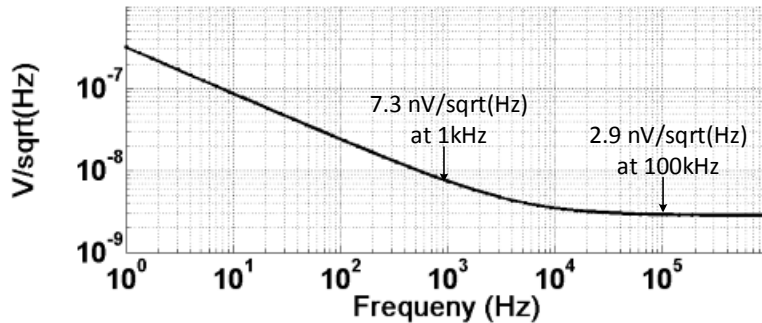


Figure 3.7: Simulated input-referred noise of the core amplifier

3.6 Measured Results

The test chip described in the previous sections was fabricated in standard 130 nm IBM CMOS process (see Figure 3.16). The measured noise and frequency response results for the sonar and VGA AFEs will be presented in this section. Also a power breakdown and the results from the sonar AFE interfaced with a ceramic hydrophone will be covered.

3.6.1 Noise

The output noise and frequency responses were measured with an Agilent's Dynamic Signal Analyzer (model 35670A). This equipment has a low intrinsic noise of about $30nV/\sqrt{Hz}$ which was sufficiently below the output noise of our amplifiers. The frequency range capability of this instrument is from mHz-51 kHz which covers the desired frequency range.

Sonar Amplifier

As mentioned in the previous section, the sonar AFE was designed to have the best noise performance of all three AFEs. However, the closed loop gain for the sonar configuration

was only 18 dB. This low gain was not sufficient to suppress the noise from later circuit stages (e.g. current biasing and pad buffer). Figure 3.9 shows the measured and simulated output noise voltage for the sonar amplifier. The measured data shows $770nV/\sqrt{Hz}$ at 10 kHz but the simulated data shows $146nV/\sqrt{Hz}$ at the same frequency. This 5x difference in the noise is due to the following two design errors:

1. The gain of the AFE was erroneously based on the assumption that the overall noise of the system would be equal to the intrinsic noise of the two-stage amplifier. Thus this incorrect assumption led to a prohibitively low closed-loop gain which ultimately resulted in poor noise performance for the sonar AFE.
2. Failing to perform a top-level noise simulation (as shown in Figure 3.8) prevented us from detecting the high noise contributed by other circuit blocks. The additional noise sources came particularly from the output pad buffer and the current bias circuit— both of which had either small device sizes and/or low bias currents.

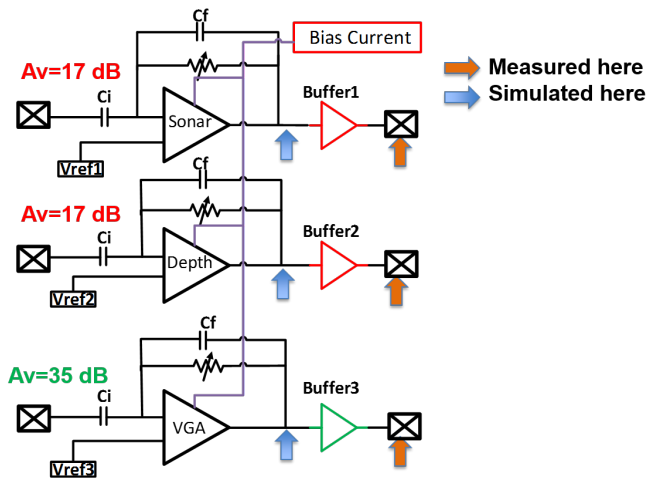


Figure 3.8: Diagram showing where simulation and measurements were taken

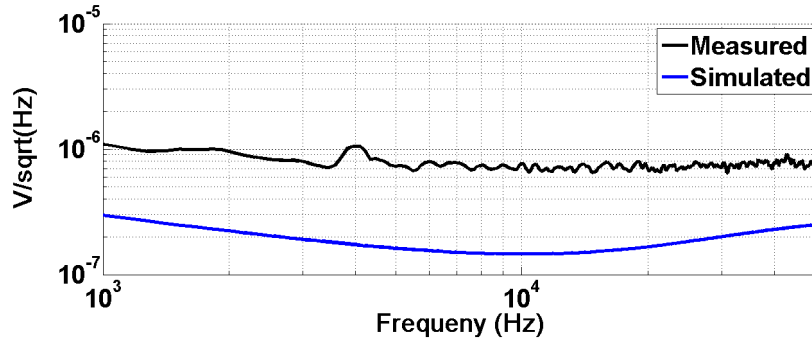


Figure 3.9: Output noise voltage for the sonar AFE

High-Gain Mode VGA

Figure 3.10 shows the total output noise of the VGA in high-gain mode. In this mode, all of the NMOS switches are in the ON position producing a gain of 60 V/V, or 35 dB. In a sharp contrast to the sonar AFE case, the simulated and measured noise profiles are in good agreement. At 10 kHz, the output noise is $992nV/\sqrt{Hz}$ which when divided by a linear gain of 60 V/V yields an input-referred noise of $16.5nV/\sqrt{Hz}$. This result comes close to the target value of $12nV/\sqrt{Hz}$ set in section 3.2.

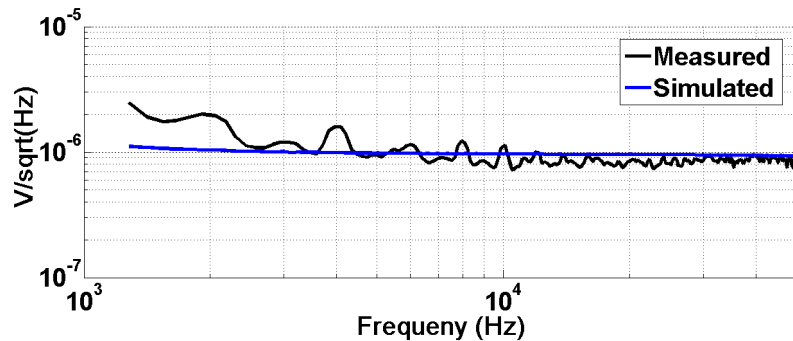


Figure 3.10: Input-referred noise for high-gain mode VGA AFE

3.6.2 Frequency Response

In this section the frequency response results for the sonar and high-mode VGA will be presented.

Sonar AFE

Figure 3.11 shows the simulated and measured mid-frequency gain of about 18 dB. These values are in agreement with the gain set by the capacitor ratio of $C_i/C_f = 40pF/5pF$.

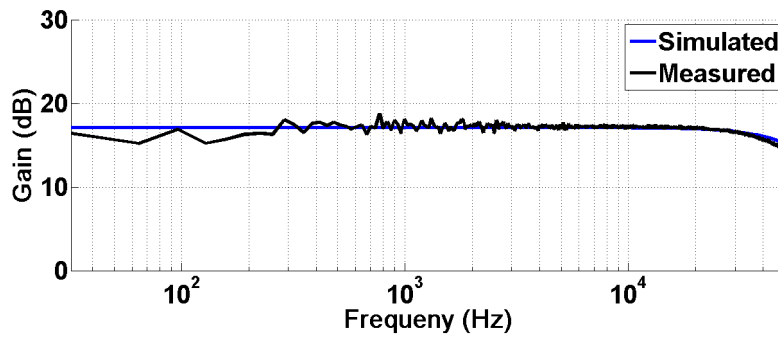


Figure 3.11: Frequency response for sonar AFE

High-Gain Mode VGA AFE

The frequency response of the VGA in high-gain mode is shown in Figure 3.12. The mid-frequency gain of the simulated and measured plots closely agree. The expected mid-frequency gain set by the capacitor ratio $C_i/C_f = 60pF/1pF = 60 V/V = 35.5 dB$ close agrees with the simulated and measured values.

Measurements Summary

Table 3.2 shows a summary of the noise and frequency responses collected from the test chip measurements. In terms of power, the sonar amplifier consumes over 2x compared to the other variations. However, the low gain prevented this amplifier from achieving the noise target of $12nV/\sqrt{Hz}$. In terms of input-referred noise, it is clear that having a large gain

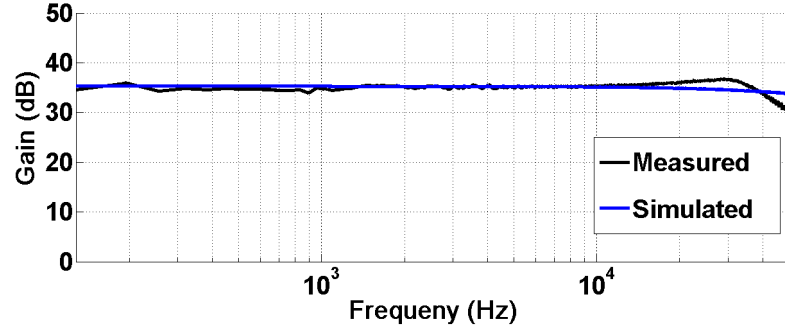


Figure 3.12: Frequency response for VGA AFE

Table 3.2: Measured power, gain and noise summary for the test chip

	Power (μ W)	Gain (dB)	Output Noise (nV/\sqrt{Hz})	Input-referred Noise (nV/\sqrt{Hz})
Sonar	760	17.8	770	100
Depth	290	17.8	800	103
VGA (Low-gain Mode)	290	5	975	195
VGA (High-gain Mode)	290	35.7	992	16.5

suppresses the noise from adjacent blocks. The VGA in high-gain mode achieves an input-referred noise of $16.5nV/\sqrt{Hz}$ getting the closest to the target value. The measured and simulated cut-off frequencies could not be conclusively compared due to frequency range limitations of the used instrument.

3.6.3 Current Consumption

The current consumption for the individual AFEs is shown in Figure 3.13. As expected, the power of the sonar AFE is over 2x higher than the other two AFEs. This is due to the high reference current needed to satisfy the transconductance for M1 set in section 3.2. This current, however, is aimed to be reduced to a level closer to that of the VGA in the

next iteration.

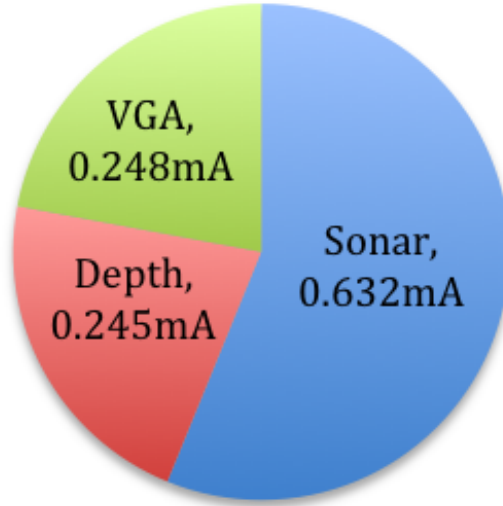


Figure 3.13: Test chip current consumption

3.6.4 Hydrophone and Sonar AFE Audio Test

One of the goals with the test chip was to verify the compatibility of the fabricated AFEs with the hydrophone sensor. Figure 3.14 shows the audio test results where a sinusoidal sound wave was generated (using a speaker) and picked up by a ceramic hydrophone which was connected to the sonar AFE. Figure 3.15 shows the simple setup used for this test. The amplitude of the input Sine wave was 66 mV and 406 mV at the output of the sonar AFE. The measured gain approximates the designed gain of 18 dB. The difference is likely due to the fact that the ceramic hydrophone is small and could only harvest part of the acoustic energy.

$$A_v = 20 \log \left(\frac{406 \text{ mV}}{66 \text{ mV}} \right) = 15.8 \text{ dB} \quad (3.31)$$

Figure 3.16 shows the die micrograph of the test chip. Fabricated in standard 130 nm IBM technology, this chip measures 2 mm x 0.7mm.

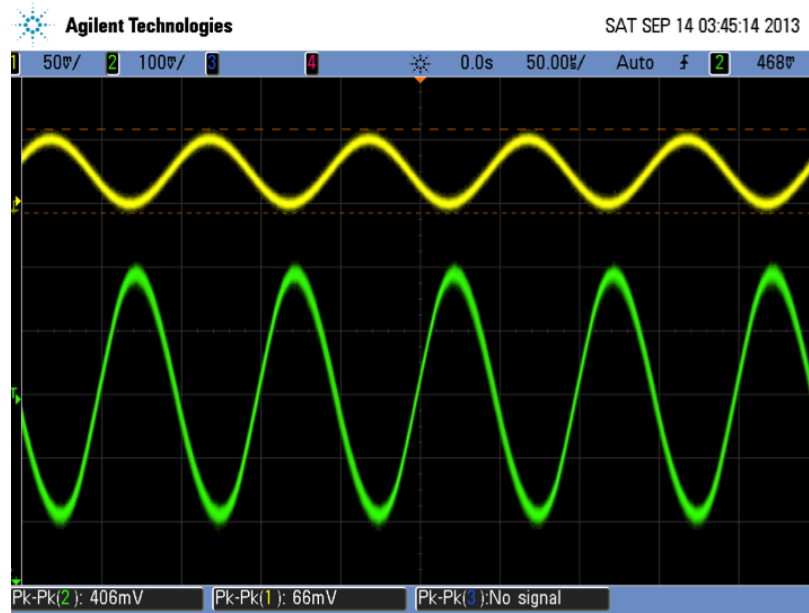


Figure 3.14: Hydrophone and sonar AFE sound test waveforms

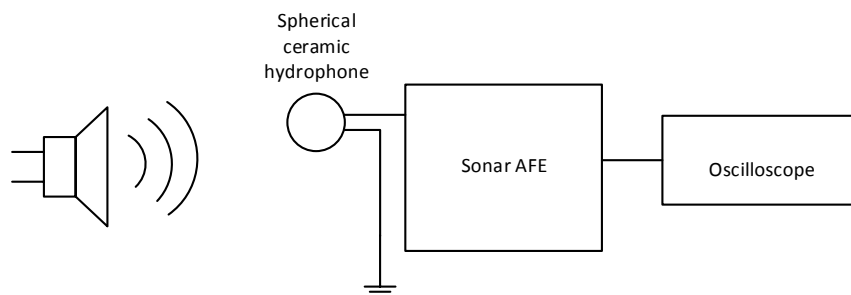


Figure 3.15: Test-bench setup for audio test using a ceramic hydrophone

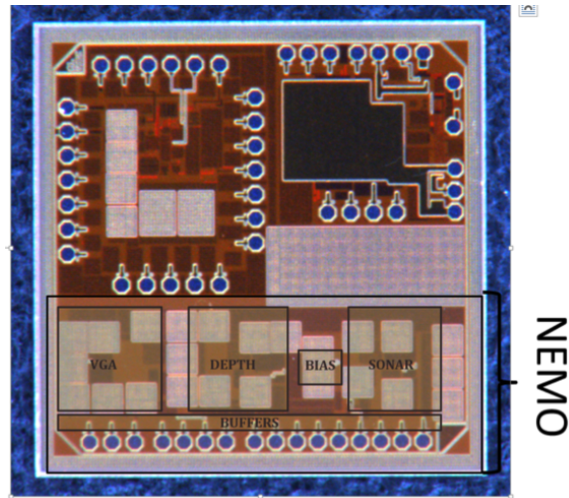


Figure 3.16: NEMO test chip die photo

3.7 Result's Discussion and Test Chip Summary

The test chip iteration offered good insight on the aspects of the design that worked well and the ones that did not. Despite achieving good noise performance in the core two-stage amplifier, not enough attention was given to the gain of the sonar and depth AFEs resulting in a large amount of noise from other sources. Fortunately, the variable gain amplifier topology showed that with at least 35 dB of gain, the noise from subsequent stages gets sufficiently suppressed. Therefore, we need enough gain in the first stage such that the overall AFE noise approaches the intrinsic noise of the core amplifier.

In terms of power consumption, Table 3.2 shows that even though the sonar front-end consumes over 2x the power of the VGA, the input-referred noise ends up being 5x higher. Thus, the noise performance is not governed merely by the amount of power provided to the amplifier, but rather by careful design of the transconductances and device sizes as suggested by equation (3.1).

In summary, by learning from the test chip results, the changes needed on the next chip iteration are clear, namely to increase the AFE gain as much as allowed by the chip area and to reduce the power by systematically optimizing for transconductances and device sizes.

Chapter 4

DEPLOYABLE CHIP DESIGN

4.1 Introduction

In this chapter, an overview of the deployable chip will be presented. From the previous chapter, conclusions were drawn on the modifications needed in order to achieve the specifications defined in Chapter 2. In addition to noise and power improvements, the second iteration of this chip has several deployable features including,

- Block power gating for low-power mode
- Frequency scaling for depth pressure detection (1- 5Hz)
- Signal digitization through an 8-bit SAR ADC
- Inclusion of an SPI slave for automated control from an external SPI master
- Dual clock for power and accuracy flexibility

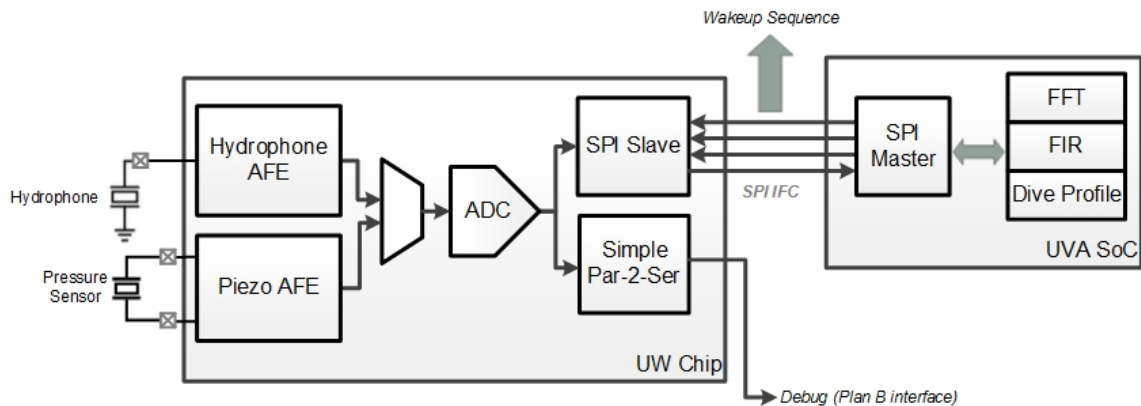


Figure 4.1: Deployable system-level block diagram

Figure 4.1 shows a simplified block diagram of the overall deployable system. This figure shows two AFEs, one to detect sonar signals through a hydrophone and the other to detect depth pressure through a piezoresistive sensor. In a typical experiment, the two signals would be continuously muxed and sampled by an 8-bit SAR ADC. Note that the sonar signal is to be sampled at a rate of about 100 kHz where as the depth pressure data would be sampled only about every second. Once digitized, the data would be transferred via SPI protocol to a System-on-Chip (SoC) developed by a collaborative team from the University of Virginia (UVA). Figure 4.2 is a detailed top-level block diagram that depicts the entire block chain. The following sections will contain descriptions on the improved sonar AFE, depth AFE, anti-aliasing filter, divider, sample and hold and clock generation blocks.

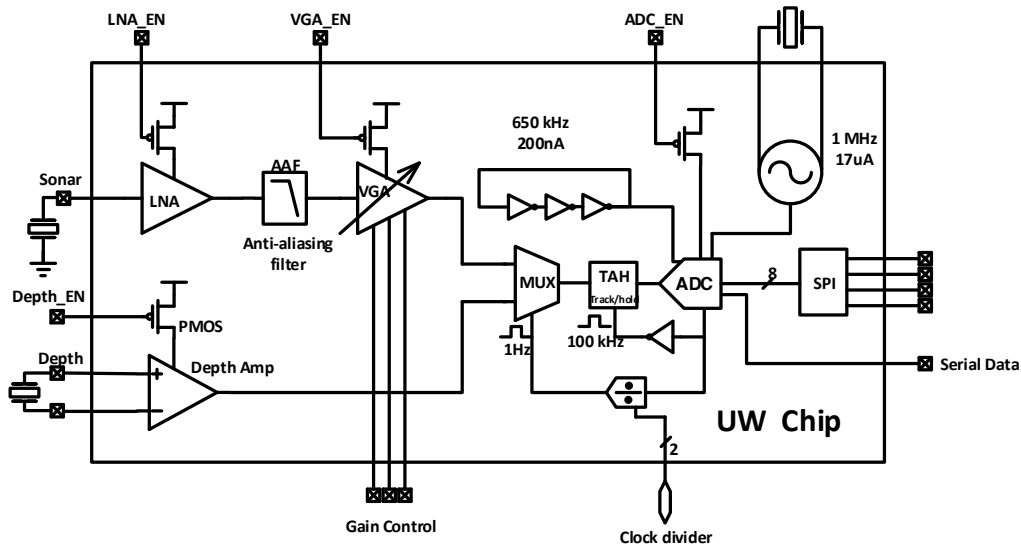


Figure 4.2: Deployable system top-level block diagram

4.2 Improved Sonar AFE

From the test chip results, it was concluded that two main modifications are needed for the sonar AFE. First, more gain is needed in order to avoid noise from other circuit blocks.

Second, the power consumption of the sonar AFE should be reduced as much as possible while still satisfying the noise specifications. The ladder can be accomplished by carefully designing the sizes and transconductance of the input devices.

For the first modification, two gain stages were cascaded. The first stage has a static gain of 40 dB and the second stage is a variable gain stage that achieves anywhere from 0 - 40 dB of gain for a total maximum gain of 80 dB. This second stage was based on the VGA covered in the last chapter. Recall that the gain for a capacitive feedback amplifier is given by

$$A_{V(CL)} = \frac{C_i}{C_f} \quad (4.1)$$

Where C_i is the input capacitance and C_f is the feedback capacitance. The strategy for increasing the gain was to allocate sufficient area to allow for hundreds of picofarads of input capacitance. Figure 4.3 shows the two gain stages used to boost up the gain of the sonar AFE.

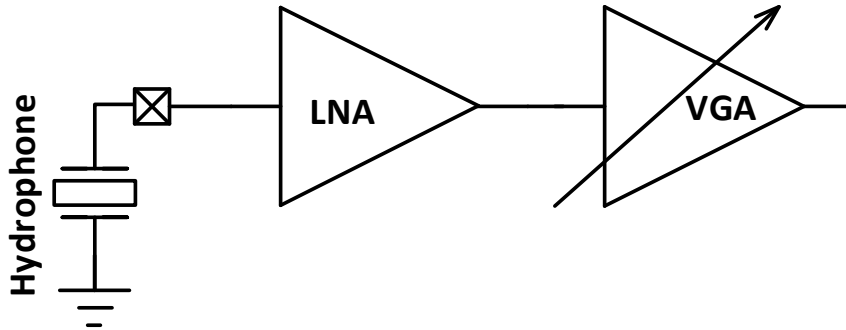


Figure 4.3: Top-level diagram of two cascaded gain stages

4.3 Pressure Amplifier

Figure 4.4 shows the schematic of the pressure transducer used in this system. This piezoresistive Wheatstone bridge operates under the a constant current excitation which eliminates

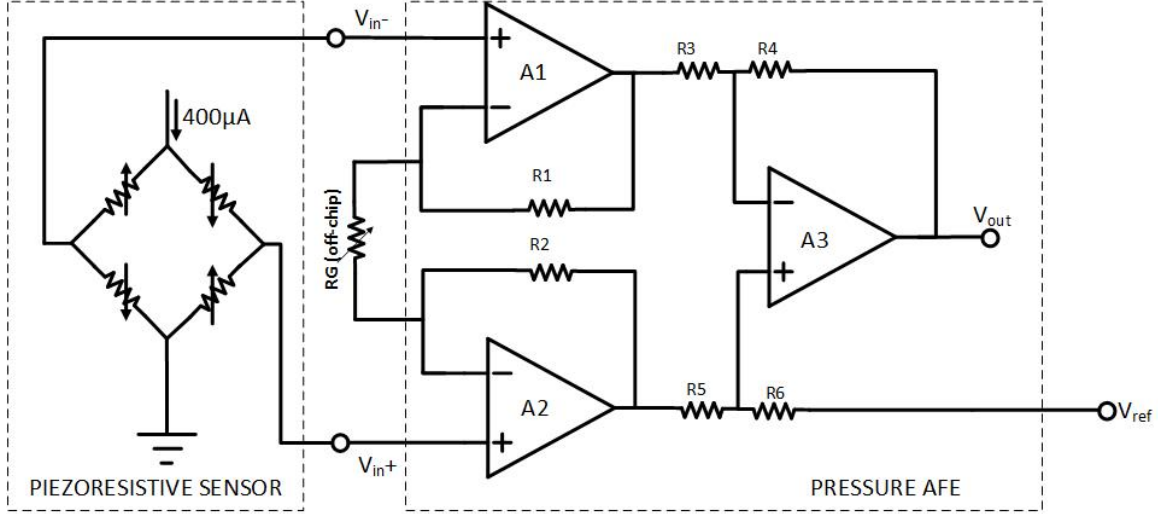


Figure 4.4: Instrumentation amplifier used for pressure depth detection

the effects of lead-wire resistance and the necessity of calibrating each unit with the lead wires attached [13]. In order to ensure high common-mode rejection ratio and high input impedance, an instrumentation amplifier is used (see Figure 4.4). This versatile amplifier has the capability to measure low-level bridge voltages and currents without loading the signal source. While A1 and A2 gain the differential signal, A3 subtracts the input signals providing a single output. The transfer function of this circuit equals to:

$$\begin{aligned}
 V_{out} = & V_{in}^+ \left(1 + \frac{2R_2}{R_G} \right) R_6 \left(\frac{R_3 + R_4}{(R_5 + R_6)R_3} \right) - V_{in}^- \left(1 + \frac{2R_1}{R_G} \right) \left(\frac{R_4}{R_3} \right) \\
 & + V_{ref} R_5 \left(\frac{R_3 + R_4}{(R_5 + R_6)R_3} \right)
 \end{aligned} \tag{4.2}$$

If $R_1 = R_2 = R$ and $R_3 = R_4$ equation (4.2) simplifies to:

$$V_{out} = (V_{in}^+ + V_{in}^-) \left(1 + \frac{2R}{R_G} \right) + V_{ref} \tag{4.3}$$

In this design, R_G and V_{ref} will be provided off-chip to have a greater level of flexibility during testing.

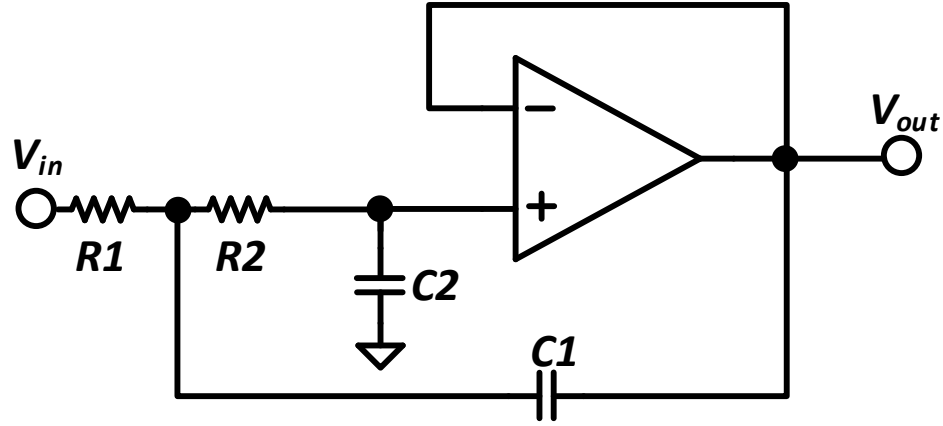


Figure 4.5: Sallen-Key low pass filter schematic

4.4 Low-Pass-Filter for Antialiasing and Echolocation Suppression

In order to avoid aliasing when sampling the sonar signal, a second order Sallen-Key low pass filter is implemented (shown in Figure 4.5). The goal of adding this anti-aliasing filter is to introduce a second pole that causes a steeper roll-off and thus avoiding any higher than necessary frequencies to be sampled by the ADC. The transfer function for the second order unity-gain low-pass filter is

$$H(s) = \frac{\omega_0^2}{s^2 + 2\alpha s + \omega_0^2} \quad (4.4)$$

$$(4.5)$$

Where ω_0 is the undamped natural frequency, α is the attenuation and $Q = \omega_0/2\alpha$ is damping ratio. This low-pass filter has no zeroes and it has two poles located in the complex s-plane:

$$s = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \quad (4.6)$$

By choosing a second-order Butterworth filter, which offers a maximally flat bandpass response [30], Q can be set to $1/\sqrt{2}$. Also, since there are four unknowns (C_1, C_2, R_1 , and R_2) but only two parameters (Q and f_0), the resistor and capacitor ratios need to be fixed to each other as follows,

$$R_1 = mR_2, \quad (4.7)$$

$$R_2 = R \quad (4.8)$$

$$C_1 = nC_2, \quad (4.9)$$

$$C_2 = C \quad (4.10)$$

Therefore, f_0 and Q can be expressed as,

$$\omega_0 = 2\pi f_0 = \frac{1}{RC\sqrt{mn}} \quad (4.11)$$

and

$$Q = \frac{\sqrt{mn}}{m+1} \quad (4.12)$$

From (4.7) and (4.9), $Q = 1/\sqrt{2}$ can be satisfied by setting $m = 1$ and $n = 2$. After considering the tradeoffs between component area and cutoff frequency, the following values for R and C are chosen:

$$R_1 = R_2 = 187k\Omega \quad (4.13)$$

$$C_1 = 100pF \quad (4.14)$$

$$C_2 = 50pF \quad (4.15)$$

yielding a cutoff frequency of $f_0 = 12kHz$.

4.5 Digital Blocks

The digitization of the sonar and pressure signals is performed by an 8-bit successive approximation analog-to-digital converter (SAR ADC). The SAR-ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital-to-analog converter (DAC) and a logic control unit. This section will focus on the S/H as this was the author's design and will defer the rest of the ADC design to literature found in [16].

4.5.1 Sample and Hold

A sample and hold is an essential block of the ADC. It is inserted before the ADC's comparator to keep the comparator's input constant while the ADC is performing the successive approximation. There are two main categories of S/H circuits: open-loop and closed-loop architectures. In this work, an open-loop architecture will be used in order to optimize for high-precision while performing fair in terms of speed.

Figure 4.6 shows a single transistor sampling switch. The ON-resistance for this switch operating in the triode region is

$$R_{ON} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{gs} - V_{th})} \quad (4.16)$$

From (4.16) we can see that as V_{in} approaches $V_{dd} - V_{th}$, the ON-resistance is highly non-linear and will approach infinity. Thus, this is the reason why NMOS devices are effective switches for low input voltages but not for high voltages. Similarly, PMOS devices are effective switches only for high voltages.

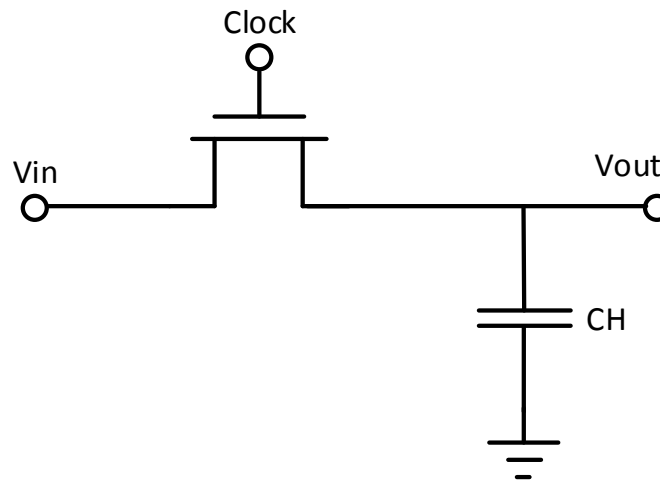


Figure 4.6: Single MOS sampling switch

To avoid this issue, we can connect a PMOS and an NMOS in parallel as shown in Figure

4.7, forming a transmission gate. The control signal for the PMOS device is achieved by using a simple inverter to invert the gate signal of the NMOS. One advantage of using a PMOS and an NMOS of equal sizes is that the charge injection will cancel each other when the switch turns off. Figure 4.8, shows the R_{ON} resistances of an NMOS, PMOS and transmission gate as a function of V_{in} . As shown by this plot, the parallel resistance is relatively flat compared to the individual resistances – this allows for full-rail transitions.

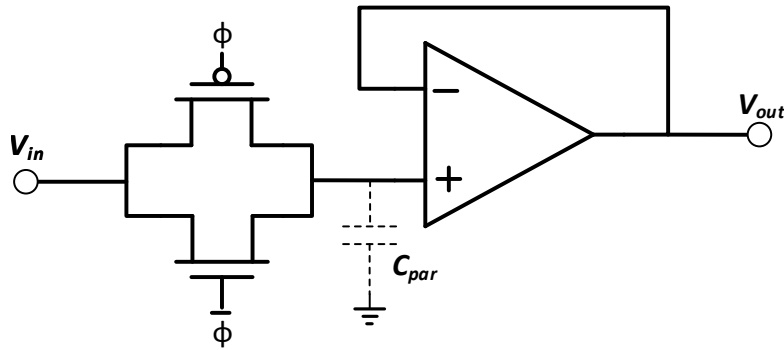


Figure 4.7: S/H schematic

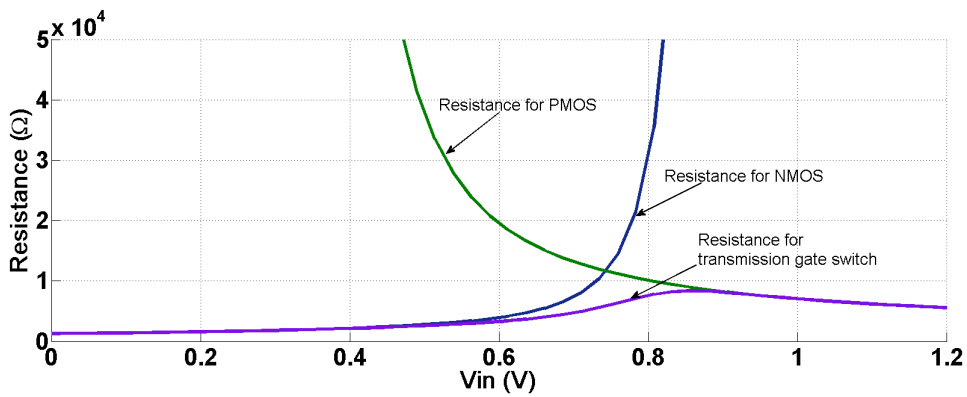


Figure 4.8: S/H ON resistance

S/H Operation

The operation of the S/H circuit, shown in Figure 4.7, consists of two modes: the sample and hold mode. During the sample mode, the transmission gate is ‘ON’ and a hold capacitor charges up to V_{in} which causes V_{out} to track V_{in} . During the ‘hold’ mode, the transmission gate is ‘OFF’ and the hold capacitor retains the charge of V_{in} just before the switch closed and thus this voltage will appear at the output. For a typical sample and hold circuit, an explicit hold capacitor is used. However, in this case, the parasitic input capacitance (C_{par}) of the buffer used is relatively large (3 pF) and can be used as the hold capacitor. In order to verify that the parasitic capacitance can function as the hold capacitor, we must compute the track-mode bandwidth which is defined as

$$TBW = \frac{1}{R_{ON}C_H} \quad (4.17)$$

Where R_{ON} is the ‘ON’ resistance of the MOS switch and C_H is the hold capacitor [23]. From Figure 4.8, the parallel R_{ON} has a maximum value of about $8k\Omega$ yielding a bandwidth of

$$TBW = \frac{1}{8k\Omega \times 3pF} = 6.6MHz \quad (4.18)$$

The sampling frequency of the ADC, based on a 1 MHz clock reference, is about 100 kHz, thus we can conclude that using the parasitic as the hold capacitor will satisfy the bandwidth of the ADC. Figure 4.9 shows a sinusoidal input signal and the corresponding output after the S/H block.

4.5.2 Clock Generation

One of the objectives for this work was that the system consume low-power in order to extend the on-the-field experiments. When considering what type of low-power clock generator to implement, the easiest solution was to have a simple ring oscillator. A ring oscillator can be operated with as little as $1\mu W$ at 1 MHz in modern CMOS technologies. The drawback of a ring oscillator is that it is highly dependent on temperature variations. This can bring potential issues as the system will be exposed to temperature changes as high as $30^\circ C$ during

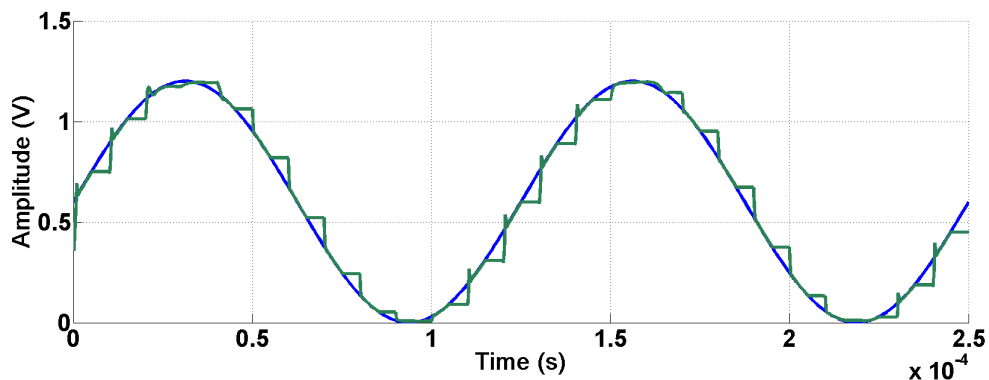


Figure 4.9: S/H input and output plots

Table 4.1: Characteristics and performance of the on-chip clocks

Clock	Frequency	Power Cons.	$CLK_SEL(HIGH)$	$CLK_SEL(LOW)$
Crystal	1 MHz	21.6 μW	OFF	ON
Ring Osc.	650 kHz	240 nW	ON	OFF

a whale's dive – this can cause a frequency variation of over 50%. Therefore, after carefully considering the tradeoffs, the decision was made to include an additional clock source based on a crystal oscillator which offers high resilience to temperature changes. Figure 4.10 shows how both clock sources are connected. The power to the two oscillators will be controlled by PMOS headers. When a low-power mode is needed, the ring oscillator can be activated by setting 'CLK_SEL' to high which in turn will deactivate the crystal oscillator. If a more accurate clock signal is required, 'CLK_SEL' should be set to low, cutting the power to the ring oscillator and activating the crystal oscillator. Table 4.1 shows the key characteristics of the implemented clock generation block.

4.5.3 Divider

As mentioned in previous sections, the pressure data needs to be sampled very rarely compared to the sonar data. To put it into perspective, one single sample of pressure data per

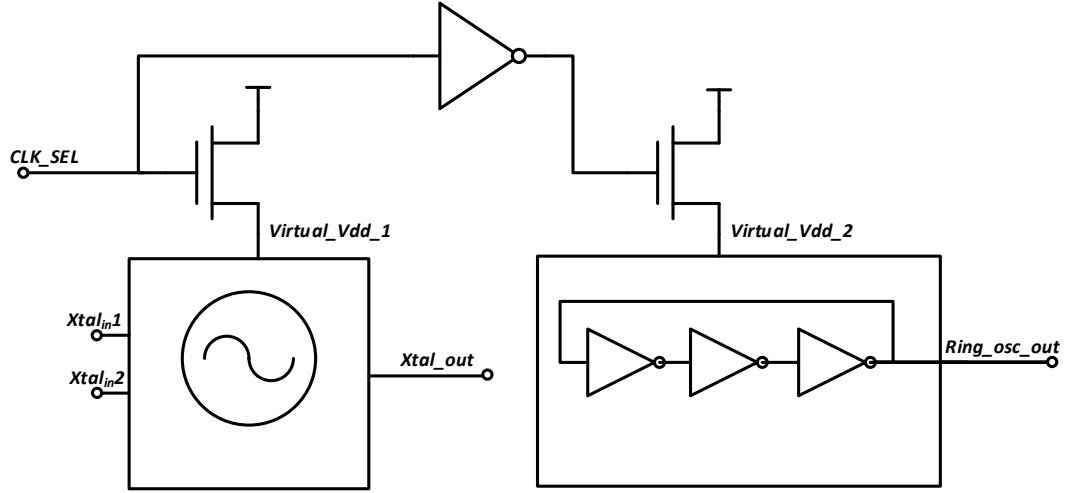


Figure 4.10: Ring and crystal oscillators

every 100 thousand samples of sonar data approximately. To achieve this level of frequency division, a ripple counter is implemented with 17 positive-edge triggered flip-flops as shown in Figure 4.11. If a 1 MHz crystal reference clock is used, then the sampling frequency signal coming from the ADC, f_{samp} is about 100 kHz and the frequency division scale can be expressed as

$$f_{Div} = \frac{f_{samp}}{2^N} \quad (4.19)$$

Where N is the number of DFFs in the chain, f_{samp} is the sampling frequency of the ADC and f_{div} is the divided signal that enables pressure reading. In order to have flexibility on how often the pressure signal is sampled, the following three options are implemented:

$$f_{Div<15>} = \frac{100kHz}{2^{15}} = 3Hz \quad (4.20)$$

$$f_{Div<16>} = \frac{100kHz}{2^{16}} = 1.5Hz \quad (4.21)$$

$$f_{Div<17>} = \frac{100kHz}{2^{17}} = 0.76Hz \quad (4.22)$$

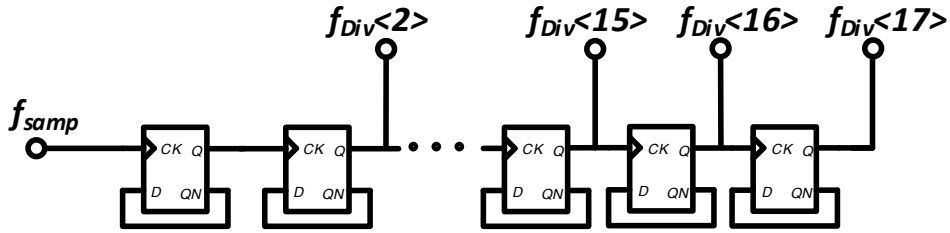


Figure 4.11: Divider flip-flop chain

To create narrow pulses and avoid needless sampling the pressure data we use a reset. The reset consists of a single DFF with a positive-edge reset controlled by the $f_{samp}/2$ signal. In a typical operation, the user would choose the desired division scale, represented by the control to the mux depicted in Figure 4.12, then the system would sample either at 3, 1.5 or 0.76 Hz and reset a short time later according to the $f_{samp}/2$ signal. Ultimately, the output signal of this block, f_{press_cont} will be the control to the mux shown in Figure 4.2 which controls whether the sonar or depth signal is sampled.

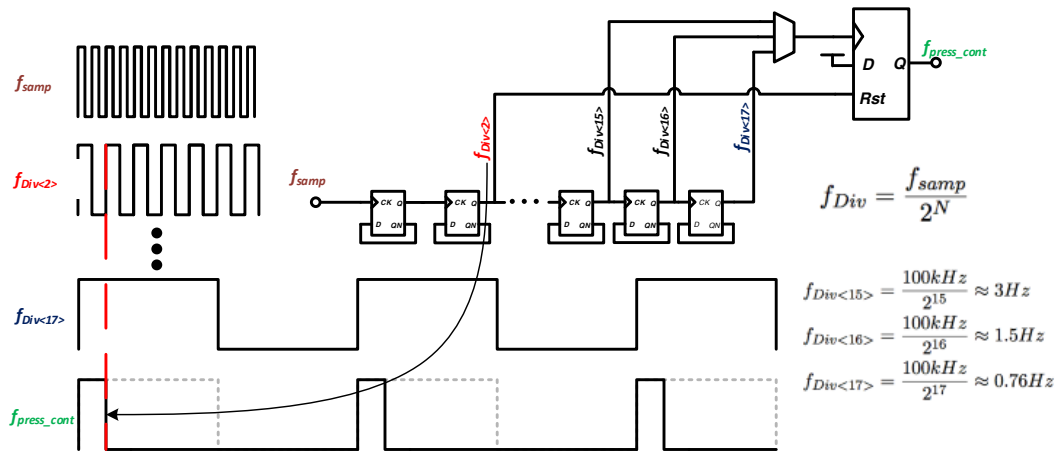


Figure 4.12: Divider logic

4.6 Simulated Results

This section will present the system layout and will outline a brief test plan. Also, simulated results for noise, frequency response and power consumption will be presented.

4.6.1 Layout and test plan

Figure 4.13 shows the 40-pin deployable system submitted for fabrication. This chip contains enough pads for two modes of operation: 1) test mode: in this mode, the knobs for the gain, frequency division, clock selection and power gating will be controlled manually to verify their functionality. 2) deploy mode: once the chip functionality has been verified in the test mode, this system will be connected to the SPI master on the SoC to control the mentioned knobs digitally. If the tests yield good results, this system would be ready for an on-field deployment.

4.6.2 Noise

Figure 4.14 shows the input-referred noise of the sonar AFE simulated at the top-level. The RMS voltage is $1.17\mu V_{rms}$ for 1-10 kHz and the spot noise at 1 kHz is $17.7nV/\sqrt{Hz}$. The resulting spot noise is slightly higher than the $12nV/\sqrt{Hz}$ targeted in section 3.2. The reason for this discrepancy is that even though the gain is high enough to suppress the noise from blocks further down the chain, the components connected directly to the input pair of the LNA contribute to the noise total. Figure 4.16 shows the noise contributors at 6 different frequencies. At very low frequencies (1 Hz), the gain is not high enough to suppress the noise from the buffer; this problem was encountered in the test chip. As the frequency increases, the gain also increases as shown in Figure 4.17, and the noise from the buffer is completely suppressed (around 50 Hz). As the frequency increases even further, the current thermal noise from the pseudo-resistors – from the VGA initially since it's closer to the output – starts to dominate. Finally, around the lowest spot noise (12kHz), there are only two contributors remaining, namely the drain current thermal noise from the input pair of the LNA and the thermal noise from the N-Well resistors. Thus, the resulting flicker noise profile seen in Figure 4.14 is not as simple as the $1/f$ encountered in the core amplifier.

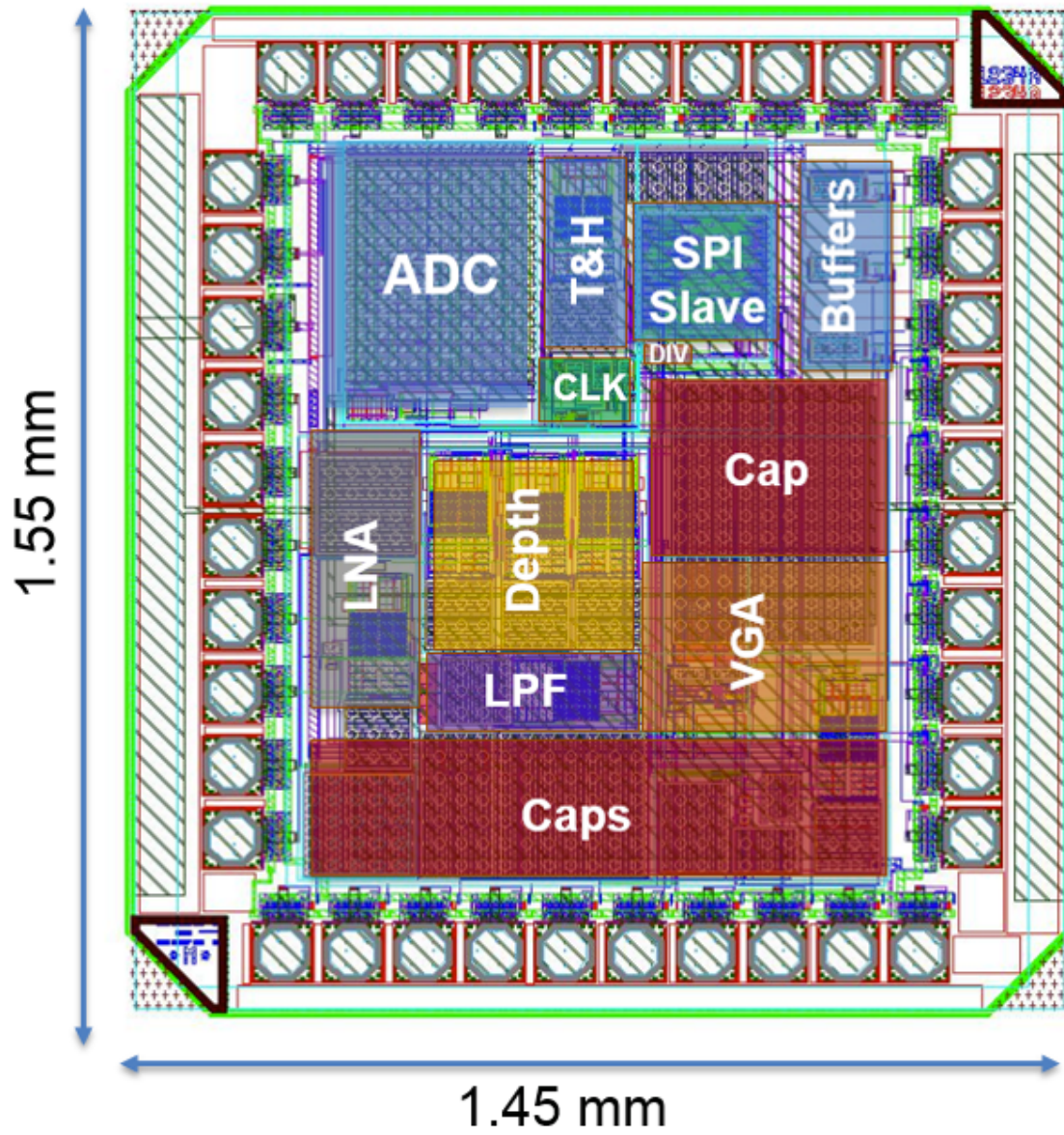


Figure 4.13: Complete system layout

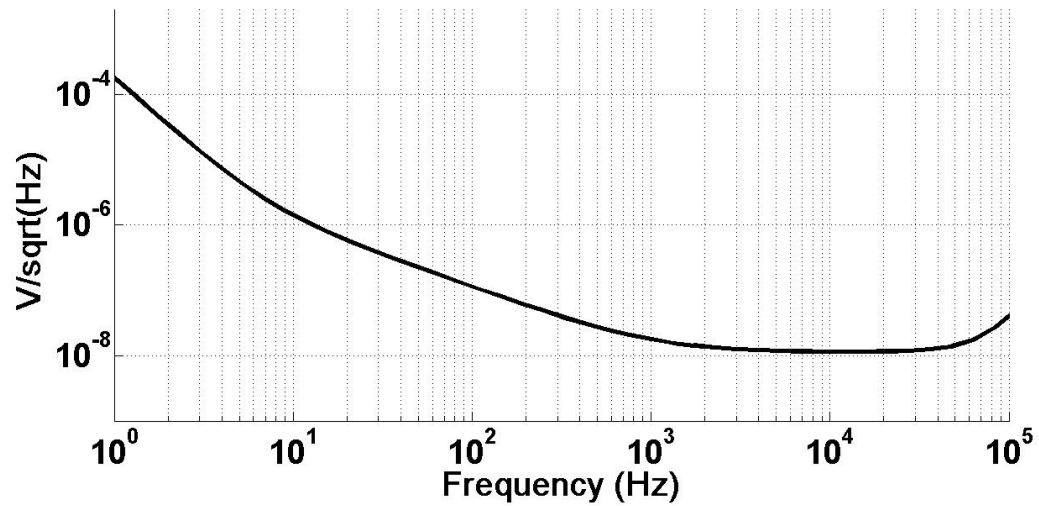


Figure 4.14: Sonar AFE input-referred noise

That is because, as explained, there are multiple noise contributions from different sources and each of these sources contributes a combination of thermal and flicker noise. A direct comparison can be seen in Figure 4.15, where the input-referred noise from the AFE is plotted along the noise from the two-stage amplifier.

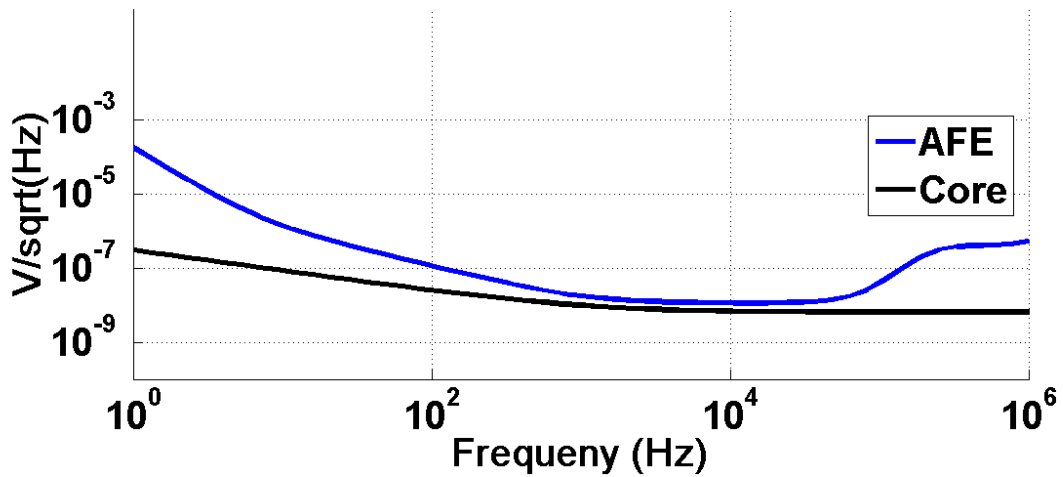


Figure 4.15: Noise comparison between the two-stage core amplifier and the complete sonar AFE

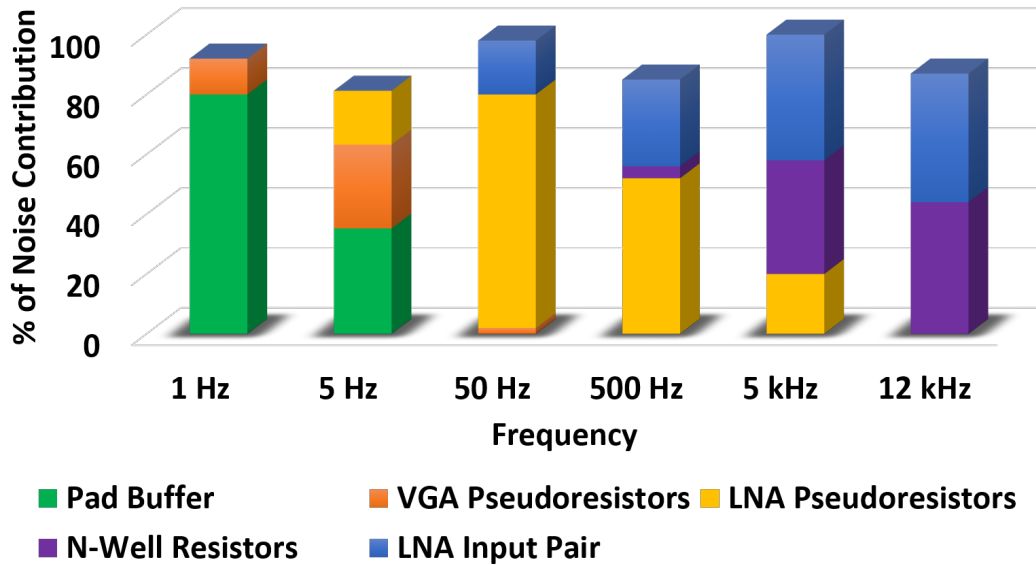


Figure 4.16: Noise contributions by different circuit blocks

4.6.3 Frequency Response

Figure 4.17 shows the sonar AFE frequency response. A maximum gain of 80 dB is achieved by the two cascaded gain stages. The first stage, contributes a static gain of 40 dB, while the second stage achieves a maximum gain of 40 dB. For the VGA, there are 3 NMOS switches that control the amount of input capacitance thus there are 8 possible step gain values that can be achieved by varying the switch configurations. The high-pass -3dB frequency corner is at 750 Hz and the low-pass is at 10.75 kHz yielding a -3dB bandwidth of 10 kHz. This bandwidth is centered closely on the sonar frequency band. A -40 dB roll-off is achieved by the 2nd order Sallen-Key LPF which helps attenuate the echolocation frequency which centers at 42 kHz.

4.6.4 Power Consumption

The pie chart shown in Figure 4.18 breaks down the current consumption of the entire deployable system. As expected, the Sonar AFE amplifier consumes the majority of the power at 44% since low-noise was targeted. The VGA and the instrumentation-based depth

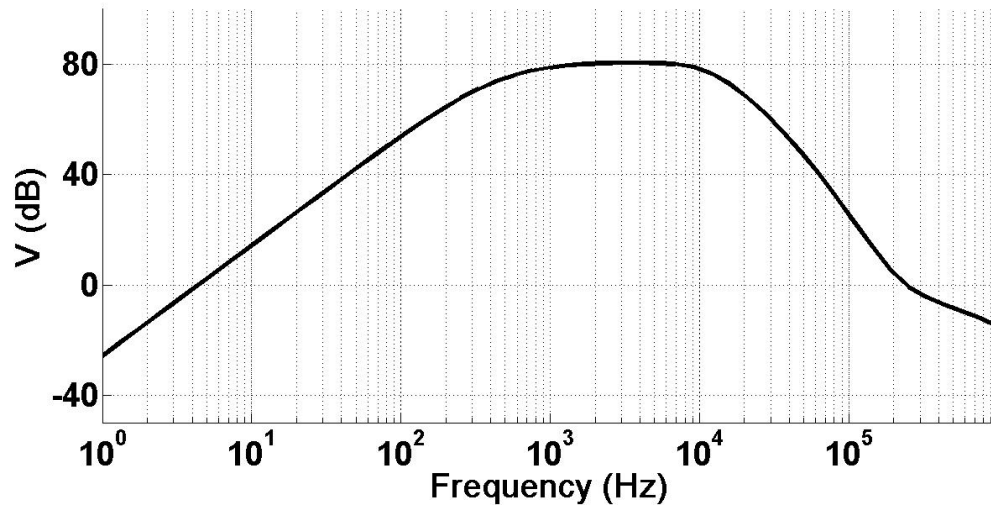


Figure 4.17: Sonar AFE frequency response

amplifier consume about the same amount at 15% and 17%, respectively. The rest of the system is mainly mixed signal and consumes a combined 25 % of the total current. In all, a total power consumption of $524\mu\text{W}$ is achieved for the entire system.

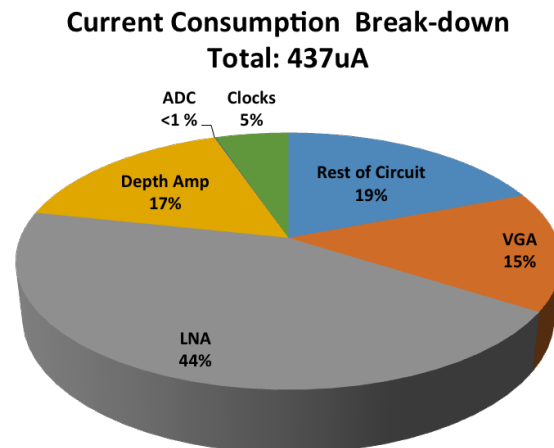


Figure 4.18: Current consumption breakdown

Chapter 5

WIRELESS SYSTEM FOR OPTOGENETICS**5.1 Introduction**

This chapter describes a low-cost, easy-to-use wireless system used in optogenetics. The motivation for this work is to find an alternative for traditional laser systems normally used in neurostimulation. These systems are not only expensive and cumbersome to use, but due to the necessary optic fiber for light delivery, they prevent researchers from conducting experiments with freely-moving animals.

5.2 Optogenetics Technology

According to Karl Deisseroth, conceptor of this field, “Optogenetics is a technology that allows a targeted, fast control of precisely defined events in biological systems as complex as freely moving animals. By delivering optical control at the speed (millisecondscale) and with the precision (cell type-specific) required for biological processing, optogenetic approaches have opened new landscapes for the study of biology, both in health and disease” [10]. The simple idea behind optogenetics is that through the insertion of a special gene such as channelrhodopsin, a neuron becomes photosensitive and can be activated or silenced by shining light upon it.

By combining the advanced field of genetics with optical methods, optogenetics allows for precise control over the neuropathways of the brain. Using this approach, researchers are able to conduct experiments with freely-moving animals in order to advance their quest for finding treatments for common neurological disorders including epilepsy, Parkinson’s and Alzheimer’s disease. Clear advantages of neuron selectivity exist in comparison to pharmacological or electrical stimulation methods. For example, a behavior study on primates conducted in [9] directly compared optogenetics with electrical microstimulation. This study concluded that optogenetics offers the ability to directly record the effects of optogenetic

stimulation during the stimulation, something that is extremely difficult to achieve using electrical microstimulation.

5.3 Laser Systems: State of the Art

Illumination of target neurons is generally achieved using optic fibers or a focus laser beam through a microscope [17]. The light source usually consists of a laser system as the one shown in Figure 5.1. Although these methods permit an accurate positioning of the illumination spot, in-vivo experimentation is severely hindered due to the tethering of the animal. In general, optogenetic-purposed laser systems have the following drawbacks:

- Optic fiber tethering prevents experimentation on freely moving animals
- Cannot adapt to natural or social experiments as mice like to chew on the fibers
- High cost. Each system can cost between \$5k and \$10k

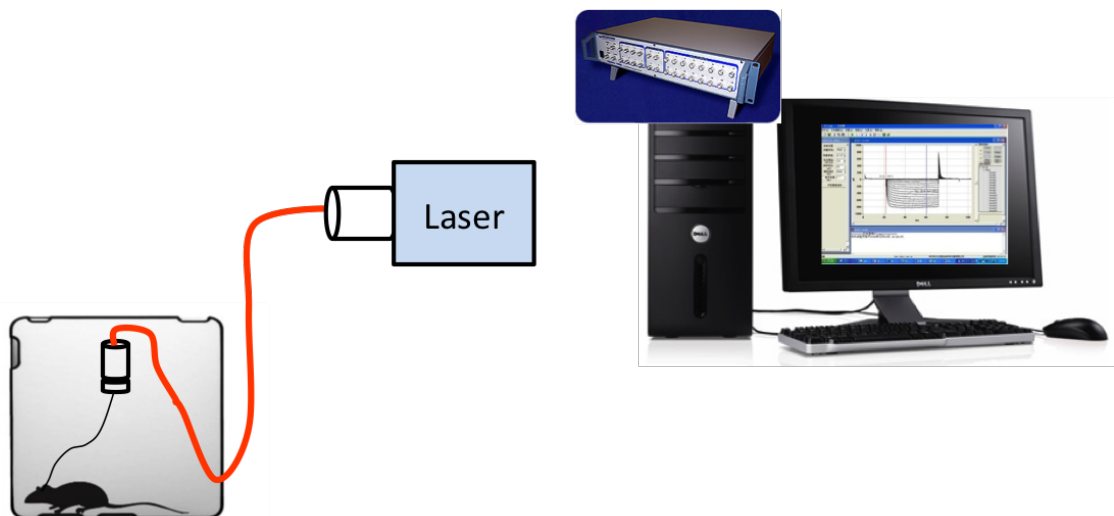


Figure 5.1: Typical laser system and optical fiber for light delivery to the brain

5.4 Telemetric System

We designed a fully autonomous telemetric brain stimulation system named Neurofly. This system is comprised of three main components: receiver implant board, transmitter base station and graphical user interface (GUI). The base station connects via universal serial bus (USB) to any Windows enabled computer and has bidirectional communication (at 2.4 GHz) with the implant. The GUI provides full control over all the functionalities of the system including accelerometer programming, LED pulse sequence control and real time data plotting. Following is a more detailed explanation of all three components.

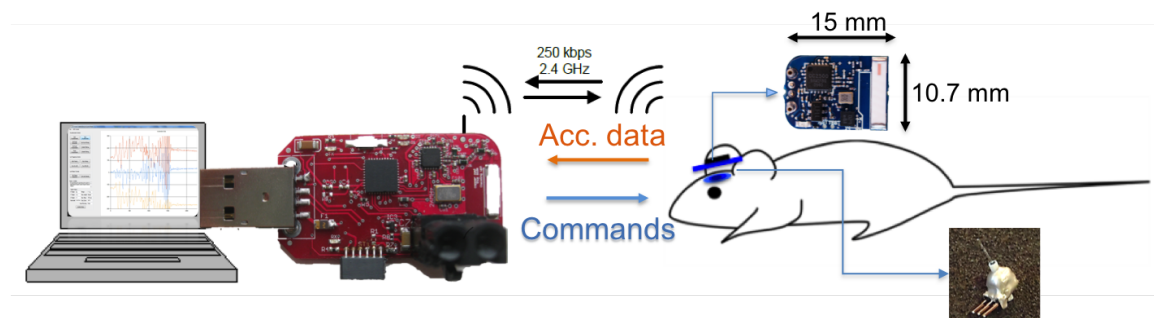


Figure 5.2: Top-level wireless system overview

5.4.1 Implant Board

The implant board is a small battery-operated device measuring 10.7 mm x 15 mm x 0.6 mm and weighting 1.7 grams (including the battery). This board is based on an evaluation tool by Texas Instruments (TI EZ430-RF2500) specifically tailored to be implanted on the head of a mouse. The main modules on the implant board shown in Figure 5.3 are: MSP430 microcontroller (MCU), accelerometer sensor, radio transceiver, dual voltage regulator, chip antenna and LED driver. The implant board is attached to the skull of the animal by force connecting two male pins located on the surface of the animal's head to two female pin receptors on the board. The connection serves two purposes: to provide power to the LED and to mechanically support the implant.

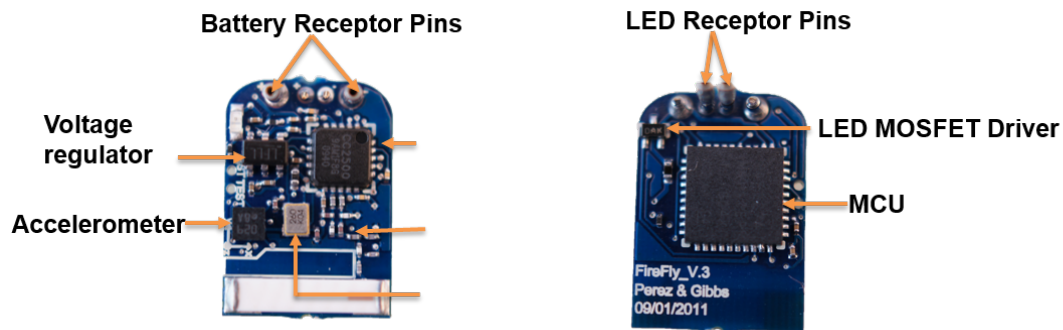


Figure 5.3: Top and bottom view of wireless implant

Regulator

The first voltage output on the dual voltage regulator is used to provide exclusive power to the implanted LED. The second voltage output is used to power the rest of the system including the MCU, radio and accelerometer. The motivation for using this scheme is to isolate the noise produced by the fast switching times of the LED which can go as low as 3 ms.

LED Driver

After testing several LED drivers, we decided to use a simple N-FET transistor as a switching mechanism for driving the implanted LED. This not only minimizes the part count on the implant, but also provides a fast and reliable way for pulsing the LED. The LED driver configuration consists of connecting the LED and N-FET transistor by a current control resistor. A signal line is connected from the MCU to the gate of the transistor providing a high voltage (3 V) to allow current flow from the drain to the source and a low voltage (0 V) to stop the current flow.

Accelerometer

To facilitate a close loop system, where stimulation on the mouse's brain is based on behavioral and electrophysiological events, we have integrated a miniature, fully programmable

3-axis accelerometer sensor chip (BMA250 from Bosch Sensortec). An accelerometer has been used in previous studies using wireless devices on moths [15]. This sensor has an acceleration dynamic range of 2g/4g/8g/16g (g = acceleration due to gravity) and a low-pass filter bandwidth of 8Hz - 1kHz; both features can be controlled via the GUI. The current draw of this miniature sensor is $139\mu A$ in normal mode operation and has a power supply range of 2.4-3.6 V.

Implant Battery Current Distribution

The battery current is distributed as shown in Figure 5.4. This current breakdown corresponds to when the implant circuitry is powered by a 45 mAh lithium ion battery and the stimulation LED is at 90% DC. The average current drawn is roughly 42 mA which would allow the battery to last for about 1 hour.

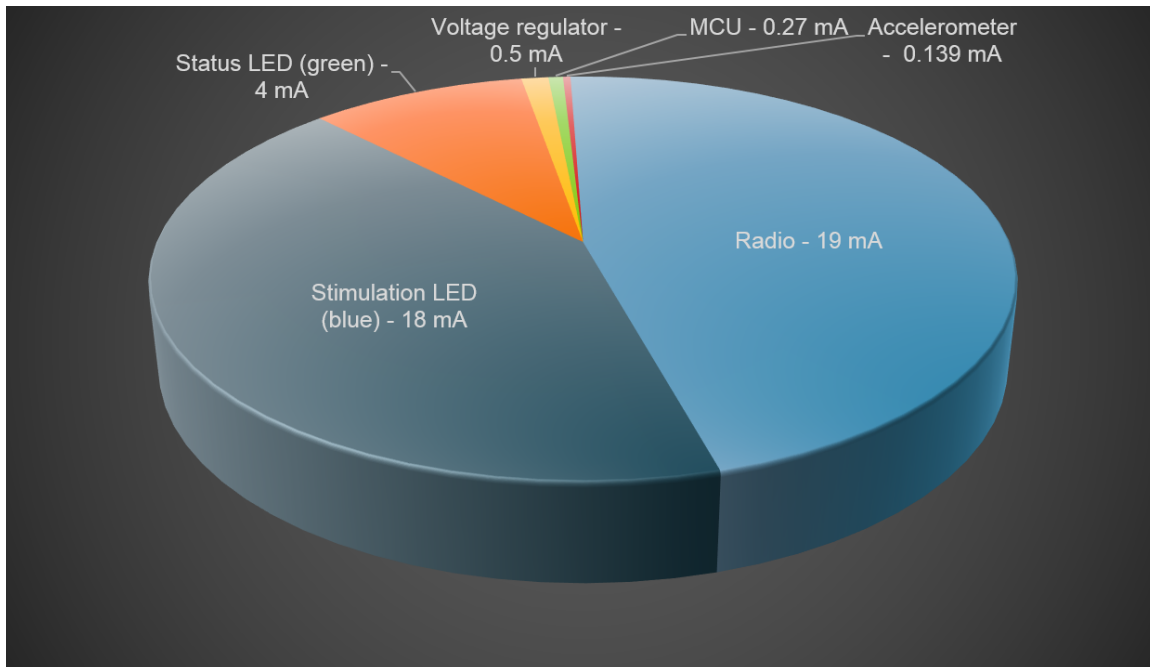


Figure 5.4: Implant current consumption breakdown with stimulation LED at 90% DC

5.4.2 Base Station

The base station is also a modified version of the evaluation tool from TI (EZ430-RF2500) and has most of the same basic components as the implant. It connects to any PC via USB and uses a USB to serial converter (RS232) to stream data back and forward between the PC and base station. This device is equipped with a triggering mechanism that allows the synchronization of the LED pulsing with an external device such as video tracking recording. The trigger mechanism consists of applying a 3.3 V between the triggering terminals either manually or automatically (see the large black component on the base station—Figure 5.2). The base station incorporates the capability of charging the used 45 mAh lithium ion battery. The MCU was uploaded with a sequence code that detects the voltage of the battery and charges it accordingly. If the battery voltage is below 2.4 V, the base station fast charges the battery using the manufacturers suggested 0.5 C ($C = 45 \text{ mA}$). When the battery reaches 4.2 V (maximum voltage) the system tops-off the battery with a small amount of current. The status LEDs will tell the user the stage in the charging sequence: Solid red indicates fast charging and blinking red indicates top-off stage.

5.4.3 Graphical User Interface

The graphical user interface is written in Visual C++ and uses the .NET 3.5 framework to provide graphing and communication services between the implant and the user. The software is compatible with most Windows-based PCs and was written to allow use by any PC user without the need for special run-time engines from 3rd party suppliers. The software has an event-driven architecture to allow for direct user inputs, and a 10 ms second timebase to provide graphical updates and communication via a virtual COM port on a USB. The interface provides control over the wide variety of accelerometer features. The user can enable or disable acceleration recording independently from the pulsing sequence. Using the GUI, the user can specify the sensitivity of the acceleration recording by setting the acceleration dynamic range anywhere between $\pm 2g$ to $\pm 16g$. Data filtering can also be applied to the streaming data by selecting what movement frequencies the accelerometer should sample. The filtering range is from 8 Hz to 1 kHz. When sampling at higher rates

is not needed, the user can extend battery life by sampling less often. The GUI also serves as a graphing platform by plotting the acceleration of a subject in real time as well as the pulsing status. This facilitates the ability of correlating the acceleration behavior to the pulsing of the LED. Moreover, the data graphed in real time can be zoomed in, copied or saved for later use. A pulsing sequence can be preprogrammed before an experiment using the GUI. The pulsing sequence dialog in Figure 5.5 shows 20 rows, each with two columns for setting a single period of the pulsing pattern. The column on the left specifies the number of milliseconds that the LED will be on where the column on the right specifies the number of milliseconds that the LED will be off. Checking the include checkbox specifies the final pulsing sequence on the LED.

The screenshot shows the 'Set Pulse Sequence' dialog box. It contains a table with 8 rows, each representing a pulse period. Each row has an 'Include' checkbox, a slider, and two numerical input fields for 'on' and 'off' durations. Below the table are fields for 'Pulse Pattern', 'Repetitions', 'Single Sequence Length', and 'Total Sequence Length', along with 'Cancel' and 'Set' buttons.

Include	Slider	On (ms)	Slider	Off (ms)
<input checked="" type="checkbox"/>	[Slider]	15	[Slider]	44
<input checked="" type="checkbox"/>	[Slider]	54	[Slider]	79
<input type="checkbox"/>	[Slider]	1	[Slider]	1
<input type="checkbox"/>	[Slider]	1	[Slider]	1
<input checked="" type="checkbox"/>	[Slider]	14	[Slider]	9
<input type="checkbox"/>	[Slider]	1	[Slider]	1
<input type="checkbox"/>	[Slider]	1	[Slider]	1
<input type="checkbox"/>	[Slider]	1	[Slider]	1

Pulse Pattern: [15, 44] [54, 79] [14, 9]

Repetitions: [Slider] 47

Single Sequence Length: 215

Total Sequence Length: 10105

Buttons: Cancel, Set

Figure 5.5: GUI pulse sequence control

5.4.4 Communication Protocol

The communication protocol for the system allows full-duplex communication between the PC and the wireless implant. The two main links are 1) between the PC and base station and 2) between the base station and implant. The device utilizes an interrupt-driven architecture to allow for maximum power savings.

Basestation Link

Communication between the PC and base station can be initiated by either device at any time. The physical layer of the link utilizes RS232 communication between the microcontroller and an intermediate chip which converts the data to a USB compatible data stream which can be read by the PC. When the base station initiates communication, it simply sends the data in a continuous stream to the PC. Each packet is encoded in an ASCII bit stream with a data type start/stop bit on the ends of the packet. The PC stores the data in its receive hardware buffer for later processing. A 10 millisecond system clock in the PC is used to periodically check the receive buffer for new data, which is then processed. When the PC initiates communication, it sends one character at a time, waiting for that character to be bounced back in confirmation before sending the next character. Each character is stored on the microcontroller in a buffer. When a sync character is received it copies the data into a commands queue for transmission to the implant.

Implant Link

The wireless link between the base station and implant is carried out using the CC2500 2.4 GHz low power radio from Texas Instruments. The device uses the SimpliciTI software framework to carry out the high-level communication strategy using a two node star network topology. In this configuration, the implant acts as the master, utilizing an internal system clock to initiate a communication event. When the clock ticks, the sensor is sampled and all the data is packetized and transmitted. After transmission the device returns to its default receive mode state to listen for a response. The base station is also normally in receive mode. When it receives a data packet from the implant, it records the data and

then immediately sends a reply. The reply may be a null command, or it may be a new command from the user or contain additional configuration data. After transmission, the base station then processes the packet received, transmitting it back to the PC. The implant is normally in receive mode and when it receives a reply from the base station it records the new command and any associated data and carries out the instruction.

5.5 System metrics

5.5.1 Packet loss

Figure 5.6 shows the packet error percentage as a function of the distance between the base station and implant board. The method for gathering these data consisted of obtaining a base packet transmission when the two transceivers were in close proximity to each other. As the distance between the two transceivers increased, the new packet count was compared to the base packet count and the difference was converted into a percentage. At 10 meters away, the maximum advertised distanced, the packet loss is roughly 9%. Although this can be considered undesirably high, the acceleration data was not impacted due to the high sampling rate (around 250 kHz).

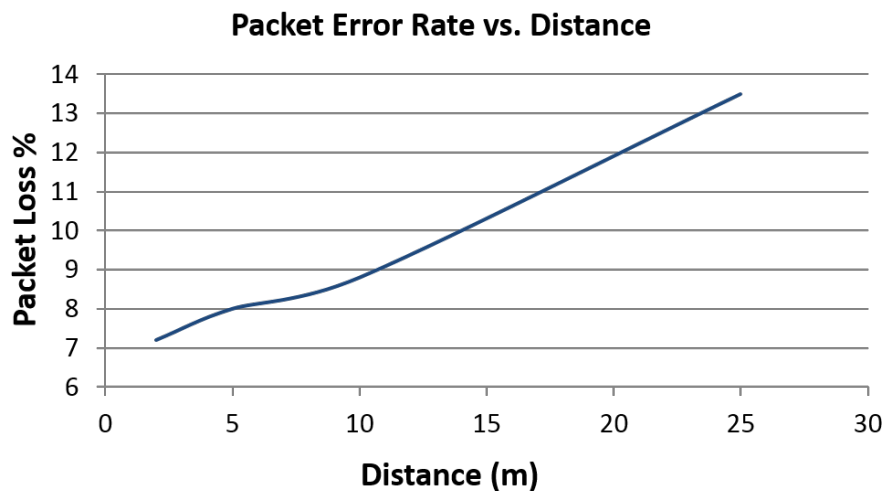


Figure 5.6: Plot of packet loss vs. distance

5.5.2 Optical power vs. Battery Time

A minimum optical power of $1\text{mW}/\text{mm}^2$ is needed to get activation in ChR2 mice, according to [3]. Therefore it is important to verify that this system has enough optical throughput to drive behavior in optogenetic mice. In Figure 5.7, a plot of the optical power output vs. battery life is presented. On that figure we see that for a 100% duty cycle (DC), the battery depletes at a fast rate but also the output power is higher than the minimum required for activation. Lowering the DC to 90% yields an optical power throughput close to the threshold and the battery lasts about 10 minutes of continuous light. This, however, is an overestimation of the optical power needed in a typical experiment where the light pulses would not only be heavily duty cycled but also would occur with long time intervals in between sessions.

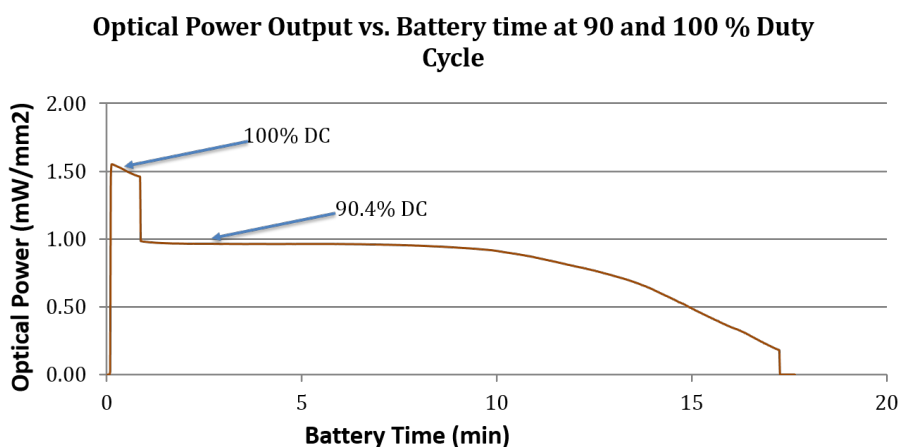


Figure 5.7: Optical power vs. time

5.6 Optogenetic Stimulation

Three ChR2 mice were used for in vivo optogenetic stimulation. Figure 5.8 shows one of the mice with the implant attached to its head. The anchor for the implant attachment is a surgically inserted LED with compatible pin receptors. The LED, which contains an optic fiber tip, was inserted in the motor cortex part of the mice's brain. The results of



Figure 5.8: CR4 mouse with head anchored implant board

the experiment are shown in Figure 5.9. The optical pulses were manually generated every 30 to 45 seconds and the real-time acceleration was observed on the same time axis. From Figure 5.9, it is clear that the light pulses directly correlate with the physiological response of the subject.

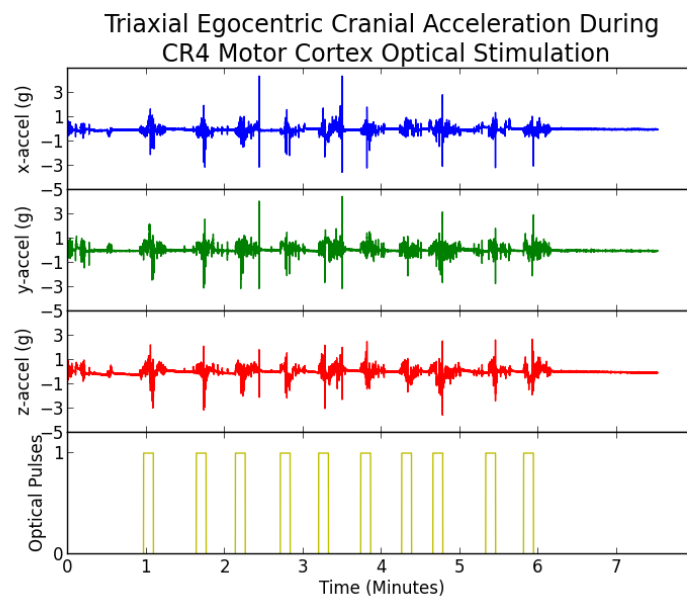


Figure 5.9: Transient X, Y, Z mouse head acceleration and optical pulses vs. time

Chapter 6

CONCLUSION

6.1 Research Summary

In the first part of this work, the design of a low-noise AFE for acoustic detection and behavior monitoring in marine mammal science has been demonstrated.

As discussed in Chapter 2, this research was motivated by the need to further understand how mid-frequency sonars affect marine mammals. It was shown that ocean ambient noise determined the noise specification for the proposed system.

Chapter 3 presented the design of a test chip which was fabricated in standard 130 nm CMOS process. The main purpose for a test chip was to learn about the tradeoffs between noise and power as well as to verify compatibility with a ceramic hydrophone sensor. Test results yielded crucial insights on the importance of high gain and top-level noise simulations to detect noise generated by devices further down the system chain.

Chapter 4 described the design of a deployable system with improved noise performance and power as well as signal digitization by analog-to-digital conversion. Adjustable features such as variable gain and frequency scaling were described. Power-gating was included on the most power-hungry blocks to achieve a low-power mode for the system. It was shown that DC offsets could be rejected by realizing a sub-kHz high-pass corner achieved using pseudoresistors. Also, it was demonstrated that echolocation signal effects could be minimized by a -40 dB/decade roll-off implemented using a 2nd order Sallen-Key low-pass filter. Simulated results showed that the band-pass frequency response was centered on the sonar band and that the input-referred noise was close to the initial target. Lastly, an analysis was included to explain the system-level noise deviation compared to the intrinsic noise of the core two-stage amplifier.

In the second part of this work (Chapter 5), a system for wireless optogenetics was presented. It was shown that this research was motivated by the need of a wireless, easy-

to-use and low-cost solution as an alternative to laser systems. First, an overview of the system introduced its main components. Next, the section on the telemetric system included detailed descriptions on the implant board, base station, GUI and communication protocol. Lastly, it was demonstrated that this system successfully achieved neurostimulation in an in-vivo experiment involving the motor cortex of the brain. This chapter concluded with a plot showing a direct correlation between the wirelessly-controlled light pulses and the physiological response of the mouse.

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