

# The Open-Source BlackParrot-BedRock Cache Coherence System

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**Abstract**

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Hardware-based cache coherence is employed nearly universally in modern shared-memory multicore processors due to its power, performance, and area efficiency. During the development of shared-memory processors, researchers proposed programmable controllers to support both cache coherence and message passing designs. Despite the flexibility afforded by programmability for post-design protocol changes or runtime selection of communication paradigms, such systems were never widely adopted. Hardware-based fixed-function designs provided excellent performance and area efficiency, as well as an easy to use shared-memory programming model that alleviated programmers of explicit cache and data-movement management. Combined with the rapid advancement of integrated circuit design technologies, single-chip shared-memory multicore processors with hardware-based cache coherence became the dominant design.

However, in the decades since the first shared-memory multicore processors emerged, the computing landscape has changed dramatically. Transistor density and power scaling have slowed or collapsed while the diversity and application of computing systems has increased significantly. It is no longer

clear whether design decisions adopted by and retained from early multiprocessor designs are correct today.

This dissertation revisits the topic of programmable cache coherence engines in the context of modern shared-memory multicore processors. First, the open-source BedRock cache coherence protocol is described. BedRock employs the canonical MOESIF coherence states and reduces implementation burden by eliminating transient coherence states from the protocol. The protocol's design complexity, concurrency, and verification effort are analyzed and compared to a canonical directory-based invalidate coherence protocol. Second, the architecture and microarchitecture of three separate cache coherence directories implementing the BedRock protocol within the BlackParrot 64-bit RISC-V multicore processor, collectively called BlackParrot-BedRock (BP-BedRock), are described. A fixed-function coherence directory engine implementation provides a baseline design for performance and area comparisons. A microcode-programmable coherence directory implementation demonstrates the feasibility of implementing a programmable coherence engine capable of maintaining sufficient protocol processing performance. A hybrid fixed-function and programmable coherence directory blends the protocol processing performance of the fixed-function design with the programmable flexibility of the microcode-programmable design. Commentary and analysis are provided to illuminate the practical architectural and microarchitectural design and implementation challenges of cache coherence systems, both with and without programmability. All three designs are available open-source, providing researchers with an easy-to-use platform for further investigation. Collectively, the BedRock coherence protocol and its three BP-BedRock implementations demonstrate the feasibility and challenges of including programmable logic within the coherence system of modern shared-memory multicore processors, paving the way for future research into the application- and system-level benefits of programmable coherence engines.

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# Acronyms

**AI** Artificial Intelligence.

**ASIC** Application-Specific Integrated Circuit.

**BP** BlackParrot.

**BP-BedRock** BlackParrot-BedRock.

**CCE** Cache Coherence Engine.

**CISC** Complex Instruction Set Computer.

**DMA** Direct Memory Access.

**DRAM** Dynamic Random-Access Memory.

**DSA** Domain-Specific Accelerator.

**E** Exclusive (cache coherence state).

**EDA** Electronic Design Automation.

**F** Forward (cache coherence state).

**FPGA** Field Programmable Gate Array.

**FPU** Floating-Point Unit.

**FSM** Finite State Machine.

**GPR** General Purpose Register.

**HLS** High-Level Synthesis.

**I** Invalid (cache coherence state).

**I/O** Input / Output.

**ILP** Instruction-Level Parallelism.

**ISA** Instruction Set Architecture.

**LCE** Local Cache Engine.  
**LLC** Last-Level Cache.  
**M** Modified (cache coherence state).  
**ML** Machine Learning.  
**NoC** Network-on-Chip.  
**O** Owned (cache coherence state).  
**PA** Physical Address.  
**PC** Program Counter.  
**PIPT** Physically-Indexed, Physically-Tagged.  
**PPA** Power, Performance, and Area.  
**RAM** Random-Access Memory.  
**RISC** Reduced Instruction Set Computer.  
**S** Shared (cache coherence state).  
**SoC** System-on-Chip.  
**SRAM** Static Random-Access Memory.  
**SWMR** Single-Writer, Multiple-Reader.  
**TLP** Thread-Level Parallelism.  
**ucode** Microcode.  
**VA** Virtual Address.  
**VIPT** Virtually-Indexed, Physically-Tagged.

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# Chapter 1

## Introduction

Computer processor architecture has historically been driven by three primary factors: power, performance, and area (PPA). However, as computers proliferate through every aspect of life, the programmability, security, and adaptability of computer systems have also become first-class design considerations. Across varied domains, shared-memory multicore processors emerged as the dominant processor architecture underlying nearly all general-purpose computer systems in use today. Furthermore, these processor designs are employed with increasing frequency in domains traditionally reliant on less complex processors, rapidly overtaking microcontroller-based systems.

Regardless of domain, the architecture of shared-memory multicore processors has largely remained constant since the earliest multicore processors were introduced commercially about two decades ago. This dissertation revisits one of the design choices employed nearly universally in shared-memory multicore processors: the use of hardware-based cache coherence mechanisms. In the rest of this chapter, [Section 1.1](#) motivates revisiting the design choice of hardware-based cache coherence, [Section 1.2](#) describes the primary questions addressed by this research, [Section 1.3](#) outlines the contents of this dissertation, and [Section 1.4](#) briefly lists published materials derived from the research described in this dissertation.

### 1.1 Motivation

As computer systems spread into all areas of modern life, the performance and adaptability of computer processors becomes increasingly important. The rapid adoption and application of computing systems in diverse domains ranging from mobile consumer devices to datacenters, supercomputers, industrial systems, healthcare, and autonomous vehicles combined with the explosive growth of edge computing, artificial intelligence (AI), and machine learning (ML) has brought about a period of extreme demand for computer processors. Across domains and applications, the processor architecture of choice for the majority of computer systems remains shared-memory multicore processors, whether as the primary computational element or as the host processor for powerful domain-specific accelerators. However, as new system demands emerge, driven by emerging applications and the novel use of computing systems in new environments and domains, it is not entirely clear whether existing systems and processor architectures will be capable of meeting those demands. The research described in this dissertation is motivated by a confluence of factors driving change in computing systems, including rapidly changing application and domain demands, the rise of open-source computer architectures and hardware implementations, and the breakdown of

fundamental technology scaling laws that have drastically altered computer architecture’s design scaling assumptions.

First, emerging applications and the application of computing systems across an ever growing set of domains is driving the need for computer processors to become both more adaptable and specialized. Artificial intelligence and machine learning applications demand novel computational hardware capable of implementing the key algorithms with greater power and performance efficiency than general purpose processors can provide. At the system level, this places additional demands on the flexibility and adaptability of existing processor architectures that are now taking on the role of host processors to domain-specific accelerators. The emergence of computing systems across a wide variety of domains such as healthcare, industrial, automotive, and edge computing further expands the set of features and functionality that computing systems must provide, and that traditional processor architectures must accommodate, integrate, or interface with. The research in this dissertation investigates how to improve the adaptability and flexibility of the cache coherence subsystem found in modern shared-memory multicore processors.

Second, the rapid growth of open-source hardware and processor architectures, driven largely by the introduction of the RISC-V Instruction Set Architecture (ISA) [9], has democratized computer processor design. No longer limited to using closed source ISAs, computer architects are able to leverage the RISC-V ISA to design and implement novel processors for any domain. The RISC-V ISA provides an extensible architecture, allowing architects to introduce domain-specific instructions or interfaces directly into the architecture in a structured manner, preserving comparability with general-purpose software infrastructure and tools while enabling application-specific, high-performance functionality. A key contribution of this dissertation is the design and implementation of a fully open-source RISC-V shared-memory multicore processor that researchers and computer designers can use to build systems of the future.

Third, over the past two decades the fundamental technology scaling laws relied upon by computer architects have stalled or broken down. Moore’s Law [94], [95], which effectively provided architects with an increasing number of transistors to implement ever complex designs has stalled and slowed significantly. Dennard scaling [38], which stated that the power consumed by transistors decreased as they became smaller, has failed, resulting in decreased power- and energy-efficiency in processor designs. Collectively, the breakdown of these laws drove computer processor designers to shift from creating faster single-core designs to constructing single-chip multicore processors and from focusing solely on general-purpose CPU architectures to leveraging domain-specific accelerator processors and system heterogeneity. However, since the shift to multicore processors occurred, their design has largely remain unchanged.

Prior to the introduction of single-chip shared-memory multicore processors, computer architects developed multi-processor systems comprising multiple processor chips connected via communication networks and having access to shared global memory. System architects explored the use of both message passing and shared memory mechanisms to create large scale systems capable of executing parallel and concurrent programs. Shared-memory systems began relying on cache coherence mechanisms, and some early systems investigated the use of programmability to support both message passing and shared memory architectures on the same system, based on application needs. However, most system architectures relied on either message passing or shared memory with shared-memory systems being implemented primarily on top of hardware-based cache coherence mechanisms. When the shift from single-core to multicore processors occurred in the early 2000s, these newly developed shared-memory multicore processors adopted the use of hardware-based cache coherence mechanisms underneath the shared-memory system.

Today, shared-memory multicore processors rely nearly universally on fixed-function hardware-based cache coherence systems. These systems demonstrate strong protocol processing performance and the use of cache coherence to provide shared memory in multicore processors is unlikely to change in the foreseeable future [86]. However, hardware-based cache coherence systems are inflexible and unable to rapidly adapt to emerging application- or system-specific demands. As shared-memory multicore processors, and computing systems in general, are employed in a growing set of domains, the ability to adapt to domain-specific needs becomes more important. While programmability within the cache coherence and shared-memory systems was explored in the past, these investigations occurred when the computing and technology landscape was significantly different than the one that exists today. Therefore, this dissertation revisits programmability within the cache coherence system of modern shared-memory single-chip multicore processors.

## 1.2 Thesis Overview

This dissertation hypothesizes that programmability can be introduced to the cache coherence system without introducing significant performance or area overheads in modern shared-memory multicore processors. Given the significant changes in the computing landscape since the topic was last investigated in depth, the widespread deployment of computing systems throughout all aspects of society and industry, and emerging trends demanding more flexible and adaptable systems, it is an apt time to revisit programmable coherence engines. Addressing this hypothesis, the research described herein investigates the design, architecture, implementation, and trade-offs of a programmable coherence directory controller, using a bottom-up, architecture-first approach guided by the following questions:

- Q1** What is an appropriate cache coherence protocol for a small- to medium-scale shared-memory multicore processor with efficient in-order processor cores and private data and instruction caches?
- Q2** What are the key architectural design decisions required for a programmable coherence directory controller to be performance and area competitive with a hardware-based fixed-function controller?
- Q3** Is it possible to design a coherence controller that achieves the flexibility benefits of a programmable controller and the power, performance, and area benefits of a fixed-function controller?

Investigating these three questions led to the development of a complete cache coherence protocol and system implemented within the BlackParrot 64-bit RISC-V shared-memory multicore processor. [Chapter 3](#) addresses [Q1](#), describing the BedRock coherence protocol, which is a practical, easy to implement coherence protocol for small- to medium-scale shared-memory multicore processors. BedRock emphasizes reducing protocol complexity over maximizing request concurrency and utilizes a space-efficient directory organization. [Chapter 4](#) addresses [Q2](#) with BP-BedRock, a BlackParrot-based implementation of the BedRock coherence protocol. BP-BedRock provides two implementations of the cache coherence directory: one that is fixed-function hardware and another that is microcode programmable. Applying lessons learned from prior work and new innovations, BP-BedRock shows that it is possible to build a programmable coherence engine that is performance competitive with a fixed-function design, with only minimal area overhead. These investigations lead to [Q3](#), which is addressed in [Chapter 5](#). A hybrid fixed-function and programmable coherence engine design combines the best aspects of the fixed-function (performance) and pro-

programmable (flexibility) coherence engines. Collectively, the research described in this dissertation demonstrates the feasibility of cache coherence engines that include programmability and provides researchers with a fully-open source architecture and implementation for use in future research.

### 1.3 Dissertation Outline

The rest of this dissertation is organized as follows. [Chapter 2](#) contains background discussion on cache coherence, open-source hardware development, and the BlackParrot RISC-V processor design. [Chapter 3](#) describes the design of the BedRock cache coherence protocol. [Chapter 4](#) details the design and implementation of BedRock within a multicore BlackParrot processor design, which is called BlackParrot-BedRock (BP-BedRock). BP-BedRock provides two implementations of the coherence directory: one constructed from fixed-function hardware and another that is microcode programmable. [Chapter 5](#) explores the integration of the programmable and fixed-function coherence directories into a unified, hybrid coherence engine capable of both efficiently executing the coherence protocol and providing useful programmability to system programmers to implement system-specific functionality. [Chapter 6](#) describes relevant related work in the areas of cache coherence protocol design, approaches to implementing cache coherence systems, programmability within the coherence system, and open-source hardware and multicore RISC-V processor design. Lastly, [Chapter 7](#) concludes the dissertation and provides a brief discussion of potential future work.

### 1.4 Published Materials

The following list provides publications related to this dissertation. Some parts of this dissertation have been published as peer-reviewed, pre-print, or technical papers.

- D. Petrisko, F. Gilani, M. Wyse, D. C. Jung, S. Davidson, P. Gao, C. Zhao, Z. Azad, S. Canakci, B. Veluri, T. Guarino, A. Joshi, M. Oskin, and M. B. Taylor, “Blackparrot: An agile open-source RISC-V multicore for accelerator socs,” *IEEE Micro*, vol. 40, no. 4, pp. 93–102, 2020. DOI: [10.1109/MM.2020.2996145](https://doi.org/10.1109/MM.2020.2996145)
- M. Wyse. “The bedrock cache coherence protocol and system v1.1.” (2022), [Online]. Available: [https://github.com/black-parrot/black-parrot/blob/master/docs/bedrock\\_protocol\\_specification.pdf](https://github.com/black-parrot/black-parrot/blob/master/docs/bedrock_protocol_specification.pdf)
- M. Wyse, D. Petrisko, F. Gilani, Y.-M. Chueh, P. Gao, D. C. Jung, S. Muralitharan, S. V. Ranga, M. Oskin, and M. Taylor, *The blackparrot bedrock cache coherence system*, 2022. arXiv: [2211.06390](https://arxiv.org/abs/2211.06390) [cs.AR]

# Chapter 2

## Background

In this chapter, brief overviews of shared-memory multicore processor architecture, cache coherence, and the BlackParrot multicore processor are provided. [Section 2.1](#) presents an architectural model of a shared-memory multicore processor that is used as a reference architecture throughout the rest of this dissertation. [Section 2.2](#) describes the fundamental problem of cache coherence, the importance of cache coherence protocols, and the relationship between cache coherence and memory consistency. [Section 2.3](#) concludes the chapter with a description of the BlackParrot processor, an open-source processor that can be configured as a shared-memory multicore, within which BP-BedRock is implemented.

### 2.1 Shared-Memory Multicore Processors

Driven by the breakdown of transistor density, power, and manufacturing scaling in the early 2000s, computer architects shifted focus from designing increasingly larger and more complex single-core processors to designing tightly-integrated single-chip shared-memory multicore processors. These processors shifted design focus from maximizing Instruction-Level Parallelism (ILP) and single-core clock frequency to exploiting Thread-Level Parallelism (TLP) via parallel and concurrent algorithms.

A high-level diagram of a canonical shared-memory multicore processor with a directory-based cache coherence system is shown in [Figure 2.1](#)<sup>1</sup>. This type of multicore comprises two or more processing cores with private caches interconnected by a Network-on-Chip (NoC), which is further connected to the last-level cache (LLC) and main memory by way of the cache coherence directory. As with single-core designs, each core in a multicore processor is capable of performing load, store, or atomic read-modify-write operations to any physical address in the system and has one or more levels of private hardware data caches. The private cache attached to each core services memory requests issued by the core by forwarding those requests to the cache coherence directory. Every level of cache in the system serves to reduce memory access latency and increase effective memory bandwidth of the shared main memory.

Multicore processors allow programmers to exploit Thread-Level Parallelism (TLP) through concurrent execution of cooperating threads within a single program address space. Multicores enable

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<sup>1</sup>Other shared-memory multicore processor organizations are possible and employed in real systems. The canonical design chosen illustrates the design concepts while remaining representative of small- to medium-scale multicore processor designs.

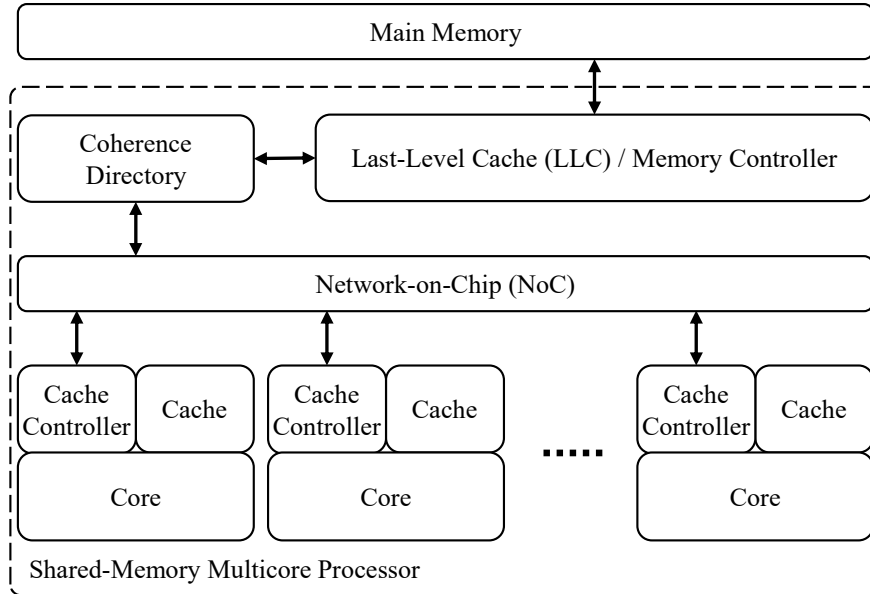


Figure 2.1: Canonical Shared-Memory Multicore Processor Architecture

efficient execution of concurrent algorithms and cooperating or synchronizing tasks, however they rely on the assumption that every cooperating thread executing on the individual cores always sees the *correct* value when loading any memory location, regardless of how many cores may be accessing the location. However, since multiple hardware threads of execution may exist and execute concurrently, with each processor core having private data caches to improve execution performance and memory access latency, it becomes possible for multiple copies of an arbitrary piece of memory data to exist within the entire system. For example, if two threads of execution running on independent cores within the multicore both access a shared memory location, each core will fetch and store a local copy of that memory location in its hardware cache to reduce the access latency of any successive read or write operations. A situation may arise where both cores then write all or a portion of the bits associated with the memory location or a group of consecutive memory locations that have been cached locally by many caches. Therefore, a mechanism and ordering rules are required to guarantee that any particular read or write of memory data returns the correct value to a thread of execution, accounting for any and all local hardware caching and updates that any given core and thread of execution make to the location.

## 2.2 Cache Coherence

Coordinating the read and write access of memory data across multiple processor cores and their private caches is a complex problem that multicore processor architects have been working on for decades. More concretely, defining the semantics of a multicore processor’s memory system and the visibility of load and store operations can be described using the two cooperating mechanisms of *memory consistency* and *cache coherence*.

”Memory consistency is a precise, architecturally visible definition of shared memory correctness” [96]. It defines the semantics for visibility and ordering of memory operations, as observed at the level of programs, instructions, and threads of execution for the shared memory system. Memory consistency defines the allowable ordering of operations across all accesses and all memory locations

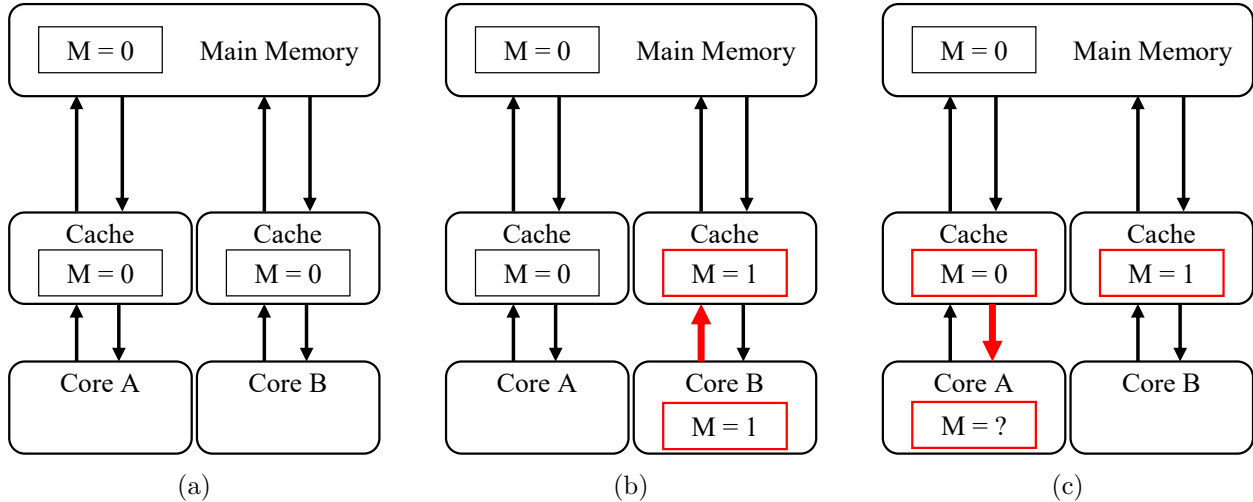


Figure 2.2: The Cache Coherence Problem

in the system. A detailed discussion of memory consistency is beyond the scope of this dissertation.

Cache coherence, on the other hand, defines the ordering and outcomes of read and write operations made by more than one processing element to a single memory location in a system employing private data caches that hold local copies of memory data. In many systems, cache coherence defines protocols and mechanisms upon which a full memory consistency model is constructed. Typically, the memory consistency model is visible to the programmer through the hardware-software interface of the machine’s Instruction Set Architecture (ISA) while the cache coherence protocol and mechanisms remain completely invisible to programmer’s and software. The rest of this section describes the fundamental problem of cache coherence using a two invariant model that is sufficient to fully define the allowable access properties and data value changes for a memory location.

### 2.2.1 The Cache Coherence Problem

The cache coherence problem, as alluded to above, occurs when multiple private copies of a single memory location can exist within a system at the same time. In a shared-memory multicore processor with private local caches per core this is easily possible. Figure 2.2 depicts the cache coherence problem. As above, consider two independent cores, core A and core B, executing programs that access a single shared memory location M. Initially, assume M has a value of 0 and both core A and core B have loaded location M, creating a copy of the location in each core’s private data cache, as shown in Figure 2.2a. Caches reduce memory access latency by storing copies of memory data closer to the processor core, and if a memory location is cached then a load or store operation only needs to manipulate the value of the location in the cache storage rather than incurring the high latency cost of a round trip access to memory. Next, assume core B modifies its cached copy of location M to have a value of 1, as shown in Figure 2.2b. Since core B’s cache has a copy of location M, the store operation from the core hits in the cache and updates only the copy of location M in core B’s cache. Lastly, as shown in Figure 2.2c, core A executes a load operation for location M. When this occurs, the question is what value should core A receive in response to its load operation?

This example illustrates the fundamental problem of incoherence. Whenever multiple agents, in

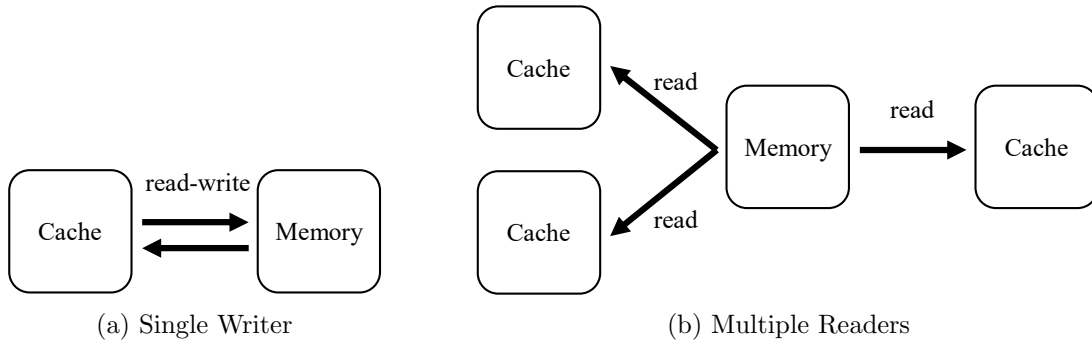


Figure 2.3: Cache Coherence Single Writer Multiple Reader (SWMR) Invariant

this case caches, can access a shared memory, there may exist multiple copies of memory locations stored in different parts of the system, and those copies can easily be manipulated such that the stored value is no longer the same across all copies. In the example above, determining the value returned by core A’s load of location M requires understanding how changes to the value of a shared memory location propagate from cache to cache or between memory and caches. Intuitively, a programmer likely expects that the load from core A will return a value of 1, which is the most recently written value to the location M, even though that write was performed by core B. Managing incoherence and solving the cache coherence problem requires defining the semantics, ordering, and observed values for load and store operations to a single shared memory location that can be cached in multiple locations throughout the system.

### 2.2.2 Cache Coherence Defined

Defining *cache coherence* is an important step when implementing a shared-memory multicore processor. Informally, ”a memory scheme is coherent if the value returned on a LOAD instruction is always the value given by the latest STORE instruction with the same address” [24]. This definition from Censier and Feautrier, while informal, is easy to understand for most programmers and architects. However, it does not precisely define the allowable ordering or observable values of a memory location as multiple agents (cores, caches) operate on the location.

More formally, cache coherence can be defined using two invariants that specify the allowable read and write access permissions any agent has for a memory location and how the observable value of the memory location changes as access permissions change [96].

#### Single Writer Multiple Reader Invariant

The *Single Writer Multiple Reader (SWMR)* Invariant, depicted in Figure 2.3, states that at any given time for a particular memory location either exactly one agent may have read and write permissions for the location or one or more agents may have read-only permissions for the location. This rule ensures that at any given time during execution, there is always at most one agent that is allowed to modify the value of a particular memory location. Further, that modification can only occur at times when no other agent can access the location. In practice, this rule implies that if a core and its cache have write permissions for a memory location then that memory location will be cached only in that core’s cache and no other cached copies of the data will exist in the system being managed by the coherence protocol. Likewise, memory locations that are cached in more than one private cache are guaranteed to be in a read-only state and the value of every copy of the

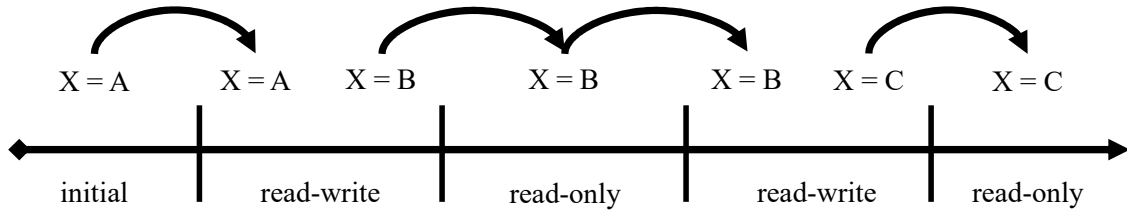


Figure 2.4: Cache Coherence Data Value Invariant

location is guaranteed to be identical.

### Data Value Invariant

The *Data Value Invariant*, depicted in Figure 2.4 defines how a memory location’s data value changes are observed in relation to read-only and read-write epochs during execution. The SWMR invariant effectively defines two types of epochs, one that is read-only (Multiple Readers) and one that is read-write (Single Writer). The data value invariant then says that starting from some initial system state, the observable value of a memory location at the start of any epoch is equivalent to the value of that memory location at the end of its last read-write epoch. Consecutive read-write epochs are possible when two agents perform writes to the memory location one after the other. The transfer of write-permissions from the first agent to the second demarcates the end of the first agent’s read-write epoch and the start of the second agent’s read-write epoch.

Informally, the data value invariant simply says that the value of a memory location cannot invisibly change between epochs. Further, there is a precise, serialized ordering of epochs that is observed during execution. The realized ordering of epochs depends on the actual timing of execution across the multiple threads of execution and processor cores, so while there may be many possible epoch orderings, every allowable ordering obeys the data value invariant and there is a well-defined transfer of values between epochs.

## 2.3 BlackParrot

BlackParrot [107] is an open-source, industrial-strength 64-bit RISC-V multicore processor that aims to become the default open-source Linux-capable RISC-V multicore used by the world. BlackParrot features a modular, tiled design, and a BlackParrot multicore processor instance is composed by selecting the appropriate number of each type of available tile and connecting them with appropriate networks. BlackParrot multicore processors implement the BedRock cache coherence protocol (Chapter 3) [133] to maintain cache coherence throughout the cacheable memory regions defined by in system. In this section, a brief overview of BlackParrot is provided, describing the types of BlackParrot tiles, the interconnection networks used between them, the BlackParrot address space, and the cache engine interface used between coherent caches and cache controllers. This section’s overview focuses on the design aspects relevant to the BP-BedRock coherence system implementation. Additional details on the BlackParrot design can be found in the documentation and code at <https://github.com/black-parrot/black-parrot><sup>2</sup>.

Figure 2.5 depicts a canonical BlackParrot multicore processor design. At the heart of the multicore is an array of BlackParrot core tiles, called the core complex. The number of core tiles in the

<sup>2</sup>The open-source BlackParrot code repository maintains the most up-to-date implementation of the processor. In the event of differences between this document and the published code, the code takes precedence.

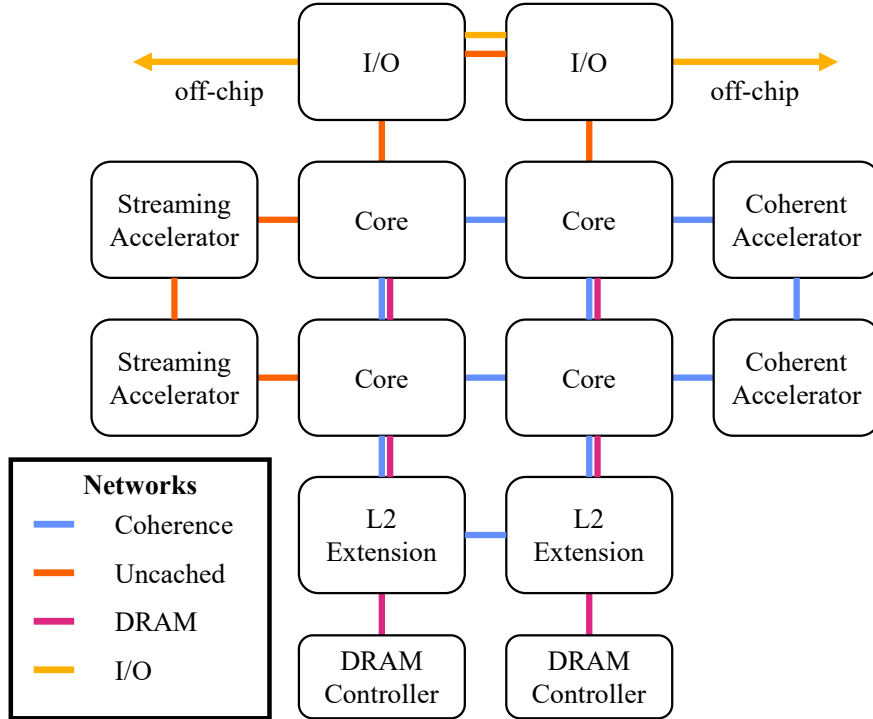


Figure 2.5: BlackParrot Tiled Multicore Processor

core complex is configurable and supports most common organizations. The remaining tile types surround the core complex in 1-dimensional complexes. Along the North side of the core complex are the I/O tiles, which connect off-chip to the East and West. Accelerator tiles are arranged along the West and East of the core complex. To the South of the core complex are the memory controllers and optional L2 extension tiles.

### 2.3.1 BlackParrot Multicore Tiles

Figure 2.6 provides a detailed view of the core, I/O, and L2 extension tiles. There are four different networks that connect the various tiles: Coherence, Uncached, DRAM, and I/O. The type of network required for each tile is determined by the functionality of the tile and the type of memory operations it handles. Note that the coloring of the networks in Figure 2.6 matches that of Figure 2.5.

#### Coherence and Uncached Networks

The Coherence network implements the full BedRock coherence protocol and its Request, Command, Fill, and Response networks. These networks are 2-D mesh networks with point-to-point ordering and Y-X dimension-ordered routing. Each of the four BedRock coherence protocol networks is carried on a separate physical network. The width of the networks is parameterizable, with 64-, 128-, and 256-bits being common widths. This network runs between the core, L2 extension, and coherent accelerator tiles.

The Uncached network is a subset-extension of the Coherence network comprising only the Request and Command BedRock networks from the Coherence network mesh that are extended out to the

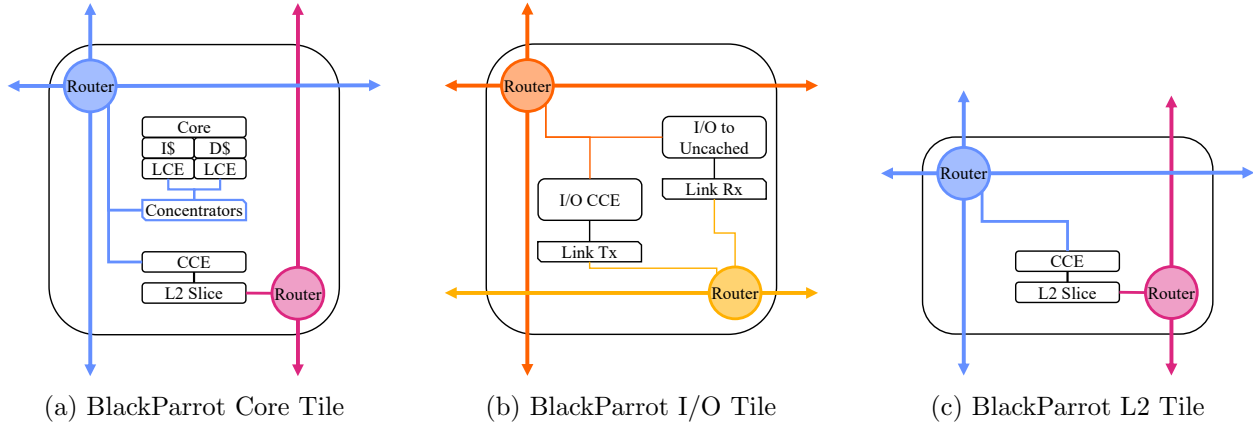


Figure 2.6: BlackParrot Multicore Tiles

I/O and streaming accelerator tiles. These tiles only support uncached load and store operations, and therefore do not utilize the Fill or Response BedRock networks.

### DRAM Network

The DRAM network supports both cacheable and uncacheable memory load and store operations. It is constructed as a set of vertical physical networks that run through the core complex columns and then South through the optional L2 extension tile and into the memory controller. The width of all DRAM networks is parameterizable, with 64-, 128-, and 256-bits being common widths. Memory accesses are only issued by the coherence directories (CCEs) found in the core and L2 extension tiles. A memory access request may originate in a core, accelerator, or off-chip via an I/O tile, and requests are routed through the Coherence and Uncached networks to a CCE, which then issues the operation to memory over the DRAM network.

### I/O Network

The I/O network is a horizontal network that connects a BlackParrot multicore to the external world. It supports uncached operations. The I/O network is bi-directional and supports both outbound and inbound paired command/response channels. Typically, each channel is implemented as its own physical network. The width of all I/O network channels is parameterizable, with 64-, 128-, or 256-bits being common widths.

### Core Tile

Figure 2.6a shows the contents of a BlackParrot core tile. Each tile comprises a single BlackParrot processor core with private L1 instruction and data caches, cache controllers (LCE) attached to each L1 cache, a coherence directory (CCE), a slice of L2 the distributed L2 cache, and connections to the Coherence and Memory networks. The Coherence network is a 2-D network that spans the core complex and reaches out to coherent accelerator and L2 extension tiles. The Memory network is a 1-D vertical network that connects each column of core tiles to a memory controller at the South border of the multicore.

The BlackParrot L1 caches maintain cache block state and data using three distinct memories, called the data, tag, and stat memories. The data memory stores the cache block data. The tag

memory stores the address tags and coherence state of for every cache block. The stat memory maintains replacement metadata, such as pseudo-LRU bits, for every cache set and dirty bits for every cache block. The L1 caches have parameterizable cache block width, associativity, sets, and fill widths. The fill width is a multiple of the cache’s internal SRAM bank width and determines the width of writes to the cache’s data memory. If the fill width is smaller than the cache block width, writing a complete cache block into the data memory takes multiple cycles.

BlackParrot’s L1 caches are virtually-indexed, physically-tagged (VIPT). Caches may be 2-, 4-, or 8-way associative and have a block size of 64, 128, 256, or 512 bits. The private L1 caches rely on banked SRAMs to store data. The width of each bank must be at least 64-bits and is computed as the cache block width divided by associativity. The cache fill width, or the width that data can be supplied to the cache must be a multiple of the cache bank width. BlackParrot implements the RISC-V Sv39 virtual-memory system with 4 KiB memory pages. There are therefore 12-bits available for the L1 cache block byte offset and cache set index bits, and it is typically assumed that exactly 12-bits are used for these two fields. The number of cache sets and block size are closely related and determined by the formula:  $\log_2(4KiB) = \log_2(sets) + \log_2(blocksize)$ . The number of cache sets must be a power-of-two. The default BlackParrot L1 cache organization is 64-sets, 8-way associative, 512-bit blocks, with a total capacity of 32 KiB.

The BlackParrot L1 caches are blocking and support one request at a time for all cacheable requests and uncacheable loads. The L1 caches are non-blocking for uncacheable stores, and the number of outstanding uncacheable stores is limited by a request credit counter in the LCE. The L1 cache is capable of executing atomic read-modify-write operations on 32- or 64-bit data words that are cached in a valid block with read-write permissions. The L1 cache may also issue atomic read-modify-write operations to the LCE, which are treated similar to uncacheable requests by the LCE.

The Coherence network instantiates each of the four BedRock coherence networks: Request, Command, Fill, and Response. Each of the four coherence networks is carried on a separate physical network. As explained in the BedRock coherence protocol specification [133], only the Fill network is bi-directional. This means that the Request, Command, and Response network input and output links connect either to the CCE or the LCE concentrators. The concentrators are used to to multiplex the coherence network connections to the two LCEs. The CCE connects directly to the Request input, Command output, and Response input coherence networks. The Fill network connects to a bi-directional concentrator since the LCEs must both send and receive Fill messages.

The L2 cache is non-inclusive of the L1 caches, and logically acts as a memory-side DRAM buffer. The coherence directory (CCE) manages a subset of physical memory, and the L2 cache only stores blocks from the same subset or slice of physical memory. An address hash or swizzle is used to efficiently utilize the entire L2 cache regardless of memory access patterns. The L2 cache slice connects to the Memory network that runs vertically through the core complex to access DRAM.

## I/O Tile

Figure 2.6b details the BlackParrot I/O tile. Each I/O tile acts as a bridge between the I/O network that runs East and West at the top of the multicore to provide off-chip connections with a 2-D Uncached network that interfaces with the core complex. The Uncached network is simply a subset of the Coherence network that only supports uncached requests. In BlackParrot, all of the I/O address space is considered uncached, however it is possible for an off-chip device to perform uncached access to BlackParrot’s DRAM address space. In this situation, software is responsible for



Figure 2.7: BlackParrot Physical Address Space

maintaining coherence between the off-chip and DRAM domains. In practice, off-chip I/O access to cacheable DRAM addresses is used to load software or data for execution into BlackParrot’s DRAM prior to the processor cores beginning execution.

Each I/O tile includes an I/O CCE module that converts uncacheable request messages issued by an LCE over the BedRock coherence/uncached network into BedRock I/O network commands, and then converts the I/O network responses to uncacheable commands that are sent back to the requesting LCE. There is also an external I/O to BedRock network converter that accepts uncacheable memory commands from off-chip sources, converts them to uncacheable requests on the BedRock coherence/uncached network, and then receives the uncachable commands satisfying the requests and converts them back to I/O network response messages for the off-chip device.

### L2 Extension Tile

If a row of L2 extension tiles are present, the Coherence and Memory networks are extended from the core complex to the L2 tiles. Figure 2.6c depicts the contents of the L2 extension tiles. Each tile contains a slice of the distributed L2 cache and a coherence directory (CCE) that manages that slice of physical memory, in the same manner that the L2 and CCE operate in a core tile. The L2 extension tiles are simplified core tiles that omit the BlackParrot core, private caches, LCEs, and concentrators. Additionally, there is no need to route the BedRock Fill coherence network since this network is only used to carry messages between LCEs, and does not connect to the CCE.

### Accelerator Tiles

Accelerator tiles may be streaming or coherent. A streaming tile is capable of performing only uncached memory operations and typically contains an accelerator IP block and a simplified LCE-like module that connects with limited functionality to the BedRock Request and Command coherence networks. A coherent accelerator tile typically contains an accelerator IP, a private L1 cache, and an LCE that participates in the full BedRock coherence protocol.

## 2.3.2 BlackParrot Address Spaces

BlackParrot divides its address space into cacheable and uncacheable regions. Figure 2.7 depicts this address space at a high-level. The address space is divided into three sections: uncacheable local memory, cacheable DRAM, and uncacheable global memory. The default physical address width in BlackParrot is 40 bits.

### Uncacheable Local Memory

Uncacheable local memory is a 2 GiB region of memory, starting at address 0, that contains mappings for devices found on BlackParrot tiles. These include bootroms, configuration links, and the Core Local Interrupt Controller (CLINT). This region supports only uncacheable accesses and

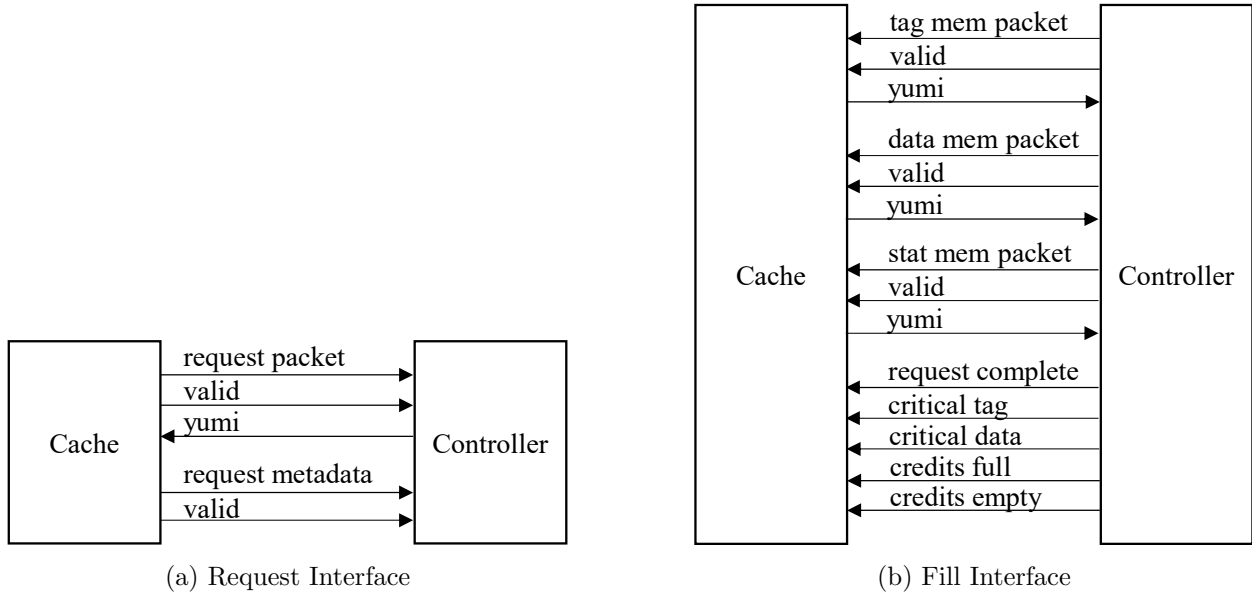


Figure 2.8: BlackParrot Cache Engine Interface

is not managed by the BedRock coherence protocol. The BlackParrot Platform Guide found in the BlackParrot documentation provides a more detailed breakdown of the local memory region.

### Cacheable Global Memory

Cacheable global memory is a 2 GiB region of memory, starting at address `0x00_8000_0000`, that maps to a cacheable portion of DRAM. This region of memory is managed using the BedRock cache coherence protocol, and is striped by cache line across the L2 cache slices and coherence directories of the core and L2 extension tiles. The region supports both cacheable and uncacheable accesses, and all accesses are serialized at the coherence directories. Performing an uncacheable access to the region results in the targeted cache block being recalled and written back, if dirty, from all caches that contain a valid copy of the block, prior to the request being issued to memory.

### Uncacheable Global Memory

Uncacheable global memory occupies the remainder of the address space, beginning at address `0x01_0000_0000`. These addresses may map to uncacheable DRAM or off-chip memory.

### 2.3.3 BlackParrot Cache Engine Interface

BlackParrot employs a flexible cache engine interface that connects each cache to an attached cache engine or controller. [Figure 2.8](#) shows the cache engine interface found in BlackParrot. The interface comprises an cache to controller request interface and a controller to cache fill interface. The cache engines are responsible for servicing misses, invalidations, and coherence transactions. The interface is latency insensitive and supports both coherent and non-coherent caches. In a BP-BedRock multicore, the cache engine interface connects the private, coherent L1 caches of each core with a dedicated Local Cache Engine (LCE). The LCE services all cache requests and maintains cache coherence for the attached cache by participating in the BP-BedRock coherence system. [Section 4.2](#) provides a detailed overview of the BP-BedRock LCE implementation.

## Cache Request and Metadata Interface

The cache engine request interface, shown in [Figure 2.8a](#), carries cache miss requests and associated metadata from the cache to the controller. In BP-BedRock, the cache can issue cacheable and uncacheable load and store miss requests, and atomic read-modify-write requests. A request includes the operation type, address, size, data for uncacheable stores and atomic operations, and a hit bit to indicate if the target cache block is cached in a valid state by the cache. The request packet utilizes a valid-then-yumi handshake<sup>3</sup>. The cache presents a request packet and raises the `valid` signal when it has a new cache request for the controller. The controller consumes the packet by raising the `yumi` signal, which depends on the `valid` input signal.

Request metadata is provided to the controller using a valid-only handshake in the cycle following the request packet handshake. The controller must be ready to accept the metadata information in the cycle following its consumption of the request packet. The request metadata includes whether the cache block including the request address is dirty and, depending on context, a way ID to use as either the replacement way or the way of a cache block hit for the request address.

## Cache Fill Interface

[Figure 2.8b](#) shows the cache fill interface that allows the controller to read and write the cache's data, stat, and tag memories while servicing cache requests. The cache fill interface also includes request completion and credit signals to help with flow control and critical word first behavior.

In general, a cache request may result in many transactions on the fill interface as the controller reads and writes the cache's memories. The cache fill interface comprises three valid-then-yumi interfaces to access the data, stat, and tag memories, and a set of request completion signals. Each of the cache's three memories has a separate, independently operating, interface, which enables flexibility in the cache engine implementation. Each of these interfaces supports read and write operations so the controller can examine and update the current state of the cache.

Three request completion signals are used by the controller to indicate when important phases of a cache request transaction complete. A request complete signal is raised to indicate that the request has been fully completed. The critical tag and data signals support critical word first behavior for cache misses. Each is raised for a single cycle when the critical data word and its associated tag are written to the cache's data and tag memories, respectively. Two credit signals are provided by the cache controller to help with flow control and hazard detection.

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<sup>3</sup>valid-then-yumi is also called valid-then-ready in [121]

## Chapter 3

# BedRock

The BedRock Cache Coherence Protocol defines a family of cache coherence protocols and the system components required to implement a specific coherence protocol. The BedRock protocols are directory-based invalidate protocols using the standard MOESI coherence states. Protocol variants are defined for the MI, MSI, MESI, MOSI, MOESI, MESIF, and MOESI state subsets. BedRock relies on a complete coherence directory to precisely track the coherence state of every cache block managed by the coherence system. The coherence directory is the point of serialization for all coherence transactions, and coherence is enforced using the *Single-Writer, Multiple-Reader (SWMR) Invariant* and *Data-Value Invariant*. A BedRock coherence system is constructed from three components: cache controllers (Local Cache Engines), coherence directories (Cache Coherence Engines), and coherence networks.

The canonical BedRock protocol presented in this chapter is well-suited for small to medium size shared-memory multicore processors. An initial implementation of BedRock within the BlackParrot 64-bit RISC-V multicore processor [107] is described in depth in [Chapter 4](#). Although BedRock has been influenced by the design needs and implementation practicalities of BlackParrot, this chapter presents BedRock agnostic to system implementation decisions.

This chapter’s description of BedRock assumes readers are familiar with the basics of cache coherence protocols. Nagarajan et al. provide an excellent overview [96] for those unfamiliar with the topic; Chapters 2 and 8 cover the basics of cache coherence and directory-based coherence protocols, respectively, and are highly relevant to the following presentation of BedRock. To the extent possible, this chapter adopts the terminology from [96] to remain consistent with the majority of published cache coherence literature.

The rest of this chapter is organized as follows. [Section 3.1](#) describes the BedRock coherence system components. [Section 3.2](#) presents the family of BedRock cache coherence protocols using both high-level overviews and detailed tabular specifications. [Section 3.3](#) discusses the incorporation of uncached and atomic accesses within the BedRock protocol. [Section 3.4](#) describes verification of the MESI variant of BedRock using the CMurphi [106] model checker software. [Section 3.5](#) compares BedRock to a canonical directory-based coherence protocol. Additionally, [Appendix A](#), [Appendix B](#), [Appendix C](#), and [Appendix D](#) provide full listings of the coherence protocol and state transition tables for all defined subsets of BedRock.

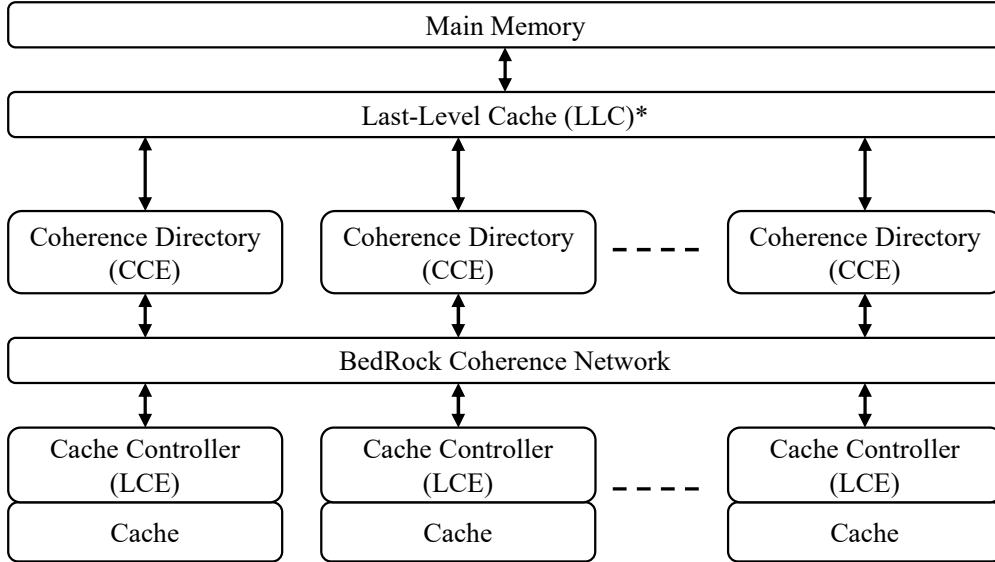


Figure 3.1: Canonical BedRock Coherence System Organization

### 3.1 System Components

BedRock defines both a coherence protocol and the system components required to implement the protocol. This section introduces the three major system components in a BedRock system: cache controllers, coherence directories, and the coherence networks.

Figure 3.1 depicts a canonical BedRock coherence system. Each cache controller (LCE) manages a single cache participating in the coherence protocol. Each coherence directory manages a disjoint subset of the physical address space and contains coherence directory storage to track all cached blocks from that subset. The controllers and directories are connected via the BedRock coherence network. The coherence directories also connect to main memory, with an optional (indicated by an asterisk) memory-side, non-inclusive Last-Level Cache (LLC) between the directories and the main memory. The LLC does not participate in the cache coherence protocol, is logically considered to be part of main memory, acting as a memory bandwidth amplifier for the higher-level caches. BedRock places no constraints on the organization of the LLC, but its implementation must provide a block-based access interface consistent with the cache block size of the BedRock system.

#### 3.1.1 BedRock Coherence Networks

The BedRock Coherence Networks carry coherence protocol messages between the cache controllers and coherence directories. The BedRock coherence protocol comprises four distinct coherence networks to carry Request, Command, Fill, and Response messages. Figure 3.2 depicts the BedRock coherence networks and their connections to the cache controllers and coherence directories. The implementation of these networks is system specific, and independent of the BedRock coherence protocol. The protocol requires each network to provide error-free message delivery and that all networks operate independently from each other. Each network may be a physical or virtual network and totally ordered, point-to-point ordered, or unordered, provided the preceding requirements are satisfied.

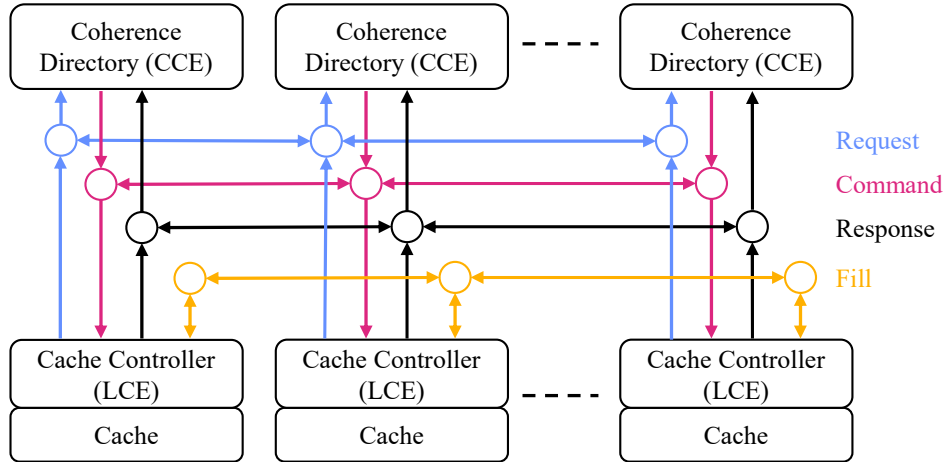


Figure 3.2: BedRock Coherence Networks

### Request Network

The Request network carries messages from a cache controller to a coherence directory. Coherence requests are initiated when a cache miss occurs due to the cache having insufficient permissions to complete the requested operation. This includes attempting to write to a read-only block and attempting to read or write a block that is not cached (i.e., the cache has no permissions for the block). The Request network may fill up and exert backpressure on the cache controllers. Backpressure may temporarily prevent a cache controller from issuing new requests, but new requests will eventually send as the coherence directory drains and processes older requests from the network. The network has no ordering constraints. All requests are eventually serialized by the network and arrive as a single request stream at each coherence directory.

### Command Network

The Command network carries coherence commands from the coherence directory to the cache controllers. The Command network has no ordering constraints and only requires that commands are processed in a timely manner after arriving at the cache controller. A cache controller may not delay processing a command in order to send a new coherence request.

### Fill Network

The Fill network carries cache to cache data transfers between the cache controllers. The Fill network has no ordering constraints and only requires that messages are processed in a timely manner after arriving at the cache controller. A cache controller may not delay processing a fill message in order to send a new coherence request.

### Response Network

The Response network carries messages from the cache controller to the coherence directory in response to commands issued by the directory or forwarded from another cache controller. Responses include invalidation acknowledgements, writeback responses with or without data, and coherence transaction acknowledgements. The Response network has no ordering constraints. Each response message sent by a cache controller is in response to a single command or fill network message. The

coherence directory must process responses in a timely manner to prevent deadlock in the coherence system. The directory must also prioritize processing responses over processing new requests or issuing additional commands.

## Network Priority

The coherence networks described above are ordered in priority, from highest to lowest, as follows:

1. Response
2. Fill
3. Command
4. Request

When a cache controller or directory receives a message it may only cause a message of higher priority to send. Requests may cause the directory to send Commands, and Commands cause the cache controllers to send Fills or Responses. Fills cause the cache controllers to send Responses.

The cache controller and coherence directory must favor processing higher priority messages over lower priority messages to avoid deadlocking the protocol. Enforcing a priority ordering of the coherence networks helps guarantee deadlock-free operation of the protocol and is commonly used by many other protocols. Readers are referred to Sections 8.2.3 and 9.3 in [96] for more information on deadlock avoidance.

### 3.1.2 Cache Controller - Local Cache Engine (LCE)

The cache controller in BedRock is called a Local Cache Engine (LCE) and manages coherence transactions for a single cache. The associated cache may be a private or shared cache, but is assumed to be a write-back cache that is inclusive of any higher-level caches in its hierarchy. The cache controller interfaces with its associated cache and with the BedRock coherence network. It may be tightly integrated into the cache pipeline or it may be more loosely coupled and interact with the cache over a well-defined interface that allows the controller to read and write cache block metadata and data.

Each cache controller manages coherence transactions for its associated cache. It issues new requests when a cache miss occurs and responds to coherence commands that arrive on the Command network. The associated cache is only allowed to access a block using the block's current permissions and may not change the permissions on a block unless directed by the coherence directory. Any operation that requires a change in permissions results in the controller issuing a new request. This includes cache block invalidations, which are detected and initiated by the coherence directory while processing coherence requests. A cache controller may have multiple cache requests outstanding at any given time as long as each request is associated with a unique cache block, however controllers should not issue multiple requests for the same cache block. The maximum number of outstanding requests per controller is a property of the specific BedRock implementation.

The cache controller must respond in a timely manner to coherence commands. Most coherence commands generate a single response message while a few messages generate no response. Cache to cache transfer commands may generate one or both of a single fill message to another controller and a single response to the directory, depending on the specific command. The cache controller must not stall command or fill message processing in order to issue a new coherence request. The

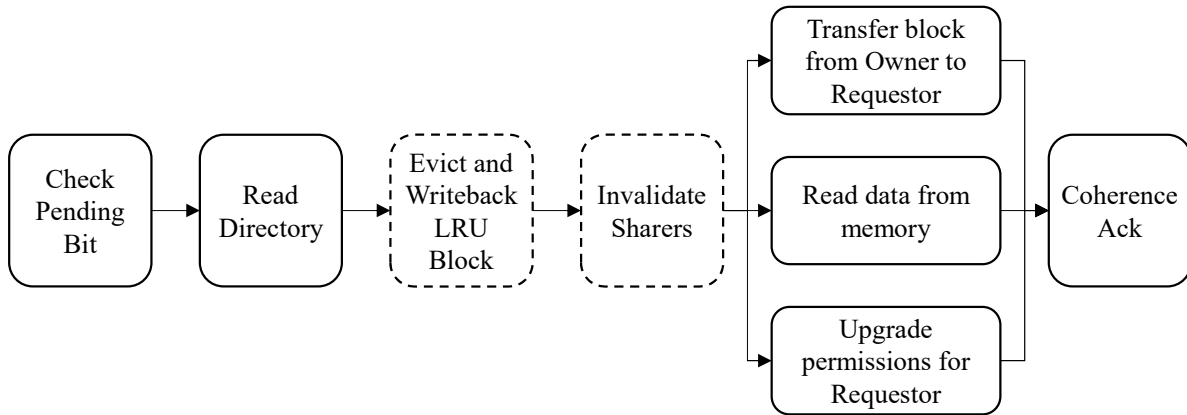


Figure 3.3: Canonical BedRock Coherence Directory Request Processing Flow

BedRock system and protocol allow the request network to fill and block new requests from sending, but the command and fill networks must be processed as they arrive independent of the request network status.

### 3.1.3 Coherence Directory - Cache Coherence Engine (CCE)

The BedRock coherence directory is called the Cache Coherence Engine (CCE) and is responsible for maintaining coherence for a disjoint subset of the physical address space. A BedRock system may have one or more coherence directories. If multiple coherence directories exist, management of the address space is divided evenly among all coherence engines with the physical address space striped across directories at the cache set granularity. All cache blocks that map to the same cache set in a cache controller are managed by exactly one coherence directory. The BedRock coherence directory must be a complete directory that can precisely track the coherence state of all cache blocks under its management. All state transitions within the coherence protocol, including the eviction and replacement of cache blocks at the cache controllers, are controlled by the directory.

The coherence directory must process response messages in a timely manner to prevent deadlock in the coherence protocol. The directory may stall additional requests and apply back-pressure on the request network while it processes the current request. The directory is also able to issue memory commands to fetch cache blocks or perform writebacks. The directory must either process memory responses as they arrive or provide sufficient buffering between the memory command and response channels to avoid stalling when issuing memory commands. A canonical system that processes requests in-order, as described below, must either block and wait for a memory response after each memory command or provide buffering for two memory command and response pairs per directory. The two memory operations that may be required for each coherence request are for cache block eviction writeback and either an additional writeback or a memory fetch.

#### Abstract CCE Request Processing Flow

The coherence directory processes coherence requests as they arrive. Each request results in one or more coherence commands being sent to the cache controllers. Request processing concludes when a coherence acknowledgment message is received at the directory from the controller that initiated the request. [Figure 3.3](#) depicts the canonical, high-level request processing flow for the coherence directory. As requests arrive, the directory is read to determine the current coherence

state of the requested cache block. If an eviction is required to make room for the newly request block a writeback command is issued to the requesting LCE. The writeback response is forwarded to memory if the cache responds with dirty cache block data. Next, any other caches with the block in the shared state are invalidated, as required by the specific request type. Then, the directory either initiates a memory read for the block, commands a cache to cache transfer from the current block owner to the requester (with a possible writeback to update memory), or responds with upgraded permissions if the requesting cache already has a copy of the target block. Finally, the directory waits for a coherence acknowledgment message to complete the transaction.

A simple directory implementation may execute the processing flow serially, stalling to wait for responses from every issued cache controller or memory command. Optimized coherence engine implementations may introduce concurrency both within a single request and across multiple requests. For example, an advanced implementation of the coherence directory may include logic to process responses in parallel to issuing commands, thereby avoiding unnecessary serialization in the processing flow. Regardless of implementation details, all requests are serialized relative to one another at the directory.

### 3.1.4 Uncacheable and Atomic Accesses

Any practical system must also be capable of processing uncacheable and atomic accesses to both cacheable and uncacheable memory. However, how these requests are handled and whether coherence is enforced for them is implementation specific. In general, atomic operations to cacheable memory should occur coherently while uncacheable operations to cacheable memory may or may not be coherent, depending on their use within the system. [Section 3.3](#) discusses one approach to keeping both uncacheable and atomic accesses to cacheable memory coherent within an implementation of the BedRock protocol and system.

### 3.1.5 System Assumptions

To facilitate discussion of the BedRock protocol's function, the following assumptions are made, unless explicitly stated otherwise, for the remainder of this chapter's description of the protocol.

1. The coherence networks require no specific ordering properties and may be completely unordered.
2. The coherence networks guarantee that messages are delivered error-free.
3. Each coherence network operates independently of the other networks.
4. Each cache controller manages a single cache that is inclusive of all higher-level caches in its hierarchy, if any exist.
5. Each cache block is managed by a single coherence directory and all cache blocks that map to the same cache set are managed by the same coherence directory.

## 3.2 Coherence Protocol

BedRock's cache coherence protocol is a four-phase, directory-based, invalidate protocol featuring the common MOESIF coherence protocol states. BedRock was designed assuming a full-duplicate

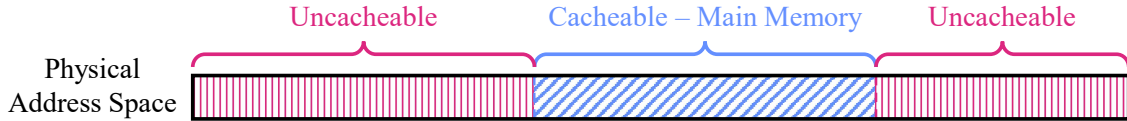


Figure 3.4: Canonical Address Space Layout and Cacheability Properties

State	Name	Valid	Dirty	Owned	Not-Excl	RW	Encoding
I	Invalid	✗	✗	✗	✗	–	000
S	Shared	✓	✗	✗	✓	R	001
E	Exclusive	✓	✗	✓	✗	RW	010
F	Forward	✓	✗	✓	✓	R	011
M	Modified	✓	✓	✓	✗	RW	110
O	Owned	✓	✓	✓	✓	R	111

Table 3.1: BedRock Coherence State Properties

tag directory organization<sup>1</sup>. The coherence protocol functions similarly to a standard directory protocol [96], however the coherence directory has complete control over all coherence state transitions in the protocol. In BedRock, the cache controllers may only use a cache block with its current permissions. Any change to permissions, including invalidation, must be requested from and directed by the coherence directory. BedRock’s other major difference from canonical directory protocols is its use of four transaction phases and four coherence networks, including a dedicated network for cache to cache data transfers.

### 3.2.1 Address Space Properties

BedRock defines a coherence protocol that is enforced for the cacheable region of the physical address space. Figure 3.4 depicts a canonical address space, with a single cacheable region backed by main memory (e.g., DRAM) and multiple uncacheable regions. Typically, the cacheable region of physical memory consists of the system’s installed DRAM address space (or a subset thereof). Without loss of generality, the rest of this chapter assumes this system model and that cacheable memory accesses are allowed only to cacheable memory. Extending the cacheable address space to cover a differently sized memory region or multiple regions requires the coherence directory to have knowledge about these ranges (or to trust the cache controllers to only issue cacheable access requests for cacheable memory). Uncacheable accesses are allowed to any physical address, and the handling of uncacheable accesses to cacheable memory is implementation specific. The implications of handling uncacheable accesses in BedRock is discussed in Section 3.3.

### 3.2.2 Coherence Protocol States

Every cache block in the BedRock protocol exists in a stable coherence state: *Invalid (I)*, *Shared (S)*, *Exclusive (E)*, *Modified (M)*, *Owned (O)*, or *Forward(F)*. Adopting the terminology of [96], each coherence state is described using four well-defined properties: **validity**, **dirtyness**, **exclusivity**,

<sup>1</sup>Any directory organization that provides complete knowledge of the system’s coherence state could be used with BedRock.

Message	Abbreviation	Description
Read Miss	ReqRd	Request cache block after a load miss
Read Miss (Non-Exclusive)	ReqRd-NE	Request cache block after a load miss with hint to not provide block in E state
Write Miss	ReqWr	Request cache block after a store miss

Table 3.2: BedRock Request Network Messages

and **ownership**. Table 3.1 summarizes the mapping of properties to coherence states for the BedRock coherence protocol with exclusivity encoded as its negation (not-exclusive indicates the block may be shared and cached in one or more caches) and validity as the logical OR of the remaining three properties. A **X** indicates the property is false, **✓** indicates the property is true. The **RW** column indicates if a block is read-only (**R**) or read-write (**RW**). A cache block is writable if the not-exclusive property is false (i.e., a single cache has ownership and write permissions) and the state is Valid. The **Encoding** column is a direct, three-bit encoding of the coherence state properties {*dirty, owned, not-exclusive*}, usable by hardware implementations.

### 3.2.3 Protocol Messages

As described above, the BedRock coherence protocol relies on the Request, Command, and Response networks to carry coherence protocol messages between the cache controllers and coherence directories. This section describes the messages carried on each of the coherence networks in detail. The messages for each network are presented in a separate table. Each table lists the message name, its abbreviation as used throughout the remainder of this document, and a description of the message’s functionality.

#### Request Network

Table 3.2 lists the Request Network message types that a cache controller may send to the coherence directory. Read requests are issued when the cache encounters a cache miss on a load operation, and write requests are issued when the cache encounters a cache miss on a store operation. Read requests may encode an optional Non-Exclusive hint to inform the coherence directory that there is no benefit in providing the cache block in the Exclusive coherence state instead of the standard Shared coherence state. This hint is useful when a cache knows that it will never need write permissions for a block and allows the directory to issue the block with read-only permissions instead of read-write permissions. Instruction caches typically issue non-exclusive read requests because the cache does not have the ability to perform writes and modify instruction memory. BedRock does not call a non-exclusive read request an instruction fetch request because this type of request may be issued by any cache controller and for either data or instruction memory locations.

A cache controller is not allowed to re-issue a coherence request until the existing request has been processed by the directory and resolved at the cache controller. A write request for a specific cache block may be issued after a read request for the same block, but multiple write or read requests for the same block from the same controller are not allowed.

Readers familiar with directory-based cache coherence may notice that BedRock does not contain a separate Upgrade request message. Upgrades exist in some protocols to indicate that write

Message	Abbreviation	Description
Invalidate	INV	Invalidate cache block specified by address
Data	DATA	Provide data and coherence state for block specified by address and wake up cache to complete request
Set State	ST	Modify state of cache block specified by address
Set State & Wakeup	STW	Modify state of cache block specified by address and wake up cache to complete request
Writeback	WB	Command cache to writeback block specified by address
Transfer	TR	Command cache to transfer cache block specified by address to another cache
Set State & Writeback	ST-WB	Modify coherence state and then command a writeback of cache block specified by address
Set State & Transfer	ST-TR	Modify coherence state and then command cache to send cache block specified by address to another cache
Set State & Transfer & Writeback	ST-TR-WB	Modify coherence state, command cache to send cache block specified by address to another cache, and then command a writeback of cache block specified by address

Table 3.3: BedRock Command Network Messages

permissions are needed for a cache block that the cache controller currently has cached with read-only permissions. BedRock omits this message type because it introduces a race into the coherence protocol between the cache issuing the upgrade and any other cache issuing an upgrade or write request for the same block. Instead, BedRock requires the LCE to issue a Write request to acquire write permissions for a block cached with read-only permissions. Section 8.8.1 of [96] explains this type of coherence protocol race in detail.

## Command Network

Table 3.3 lists the Command Network messages that the coherence directory may send to the cache controllers. Command messages are used to modify the state of cache blocks currently cached at a cache controller, provide new cache blocks to a cache, and evict blocks from a cache when a replacement is required to make room for a newly requested block. Every command generates a response of some form from the cache controller.

Command messages are divided into a group of base commands and compound commands. The base commands include Invalidate (INV), Data (DATA), Set State (ST), Set State & Wakeup (STW), and Transfer (TR). Each of these commands instructs the LCE to perform a single indivisible operation. Invalidate orders the LCE to set the specified cache block’s state to Invalid (I), thereby revoking access permissions of the block from the LCE and its cache. A Data (DATA) command provides an LCE with cache block data and coherence state in response to a coherence request. Set State (ST) and Set State & Wakeup (STW) modify the coherence state of the specified cache block. STW also indicates that the coherence request is resolved and execution can resume, which is used to implement permission upgrades. Transfer (TR) commands direct an LCE to initiate a

Message	Abbreviation	Description
Data	DATA	Provide data and coherence state for block specified by address and wake up cache to complete request

Table 3.4: BedRock Fill Network Messages

cache-to-cache transfer of the specified block by sending a message on the Fill network.

The Set State & Writeback (ST-WB), Set State & Transfer (ST-TR), and Set State & Transfer & Writeback (ST-TR-WB) messages are compound messages constructed from the Set State (ST), Transfer (TR), and Writeback (WB) command primitives. Semantically, the compound messages perform the indicated primitives in the order listed. That is, a ST-TR-WB causes the cache controller to perform a set state operation, followed by a transfer, and lastly a writeback. These operations must happen "atomically" at the cache controller, in that no other operation or command should occur between any component of the compound command. Abstractly, the compound messages are similar to atomic read-modify-write operations or transactions in that the actions taken must be all-or-none, although there is no possibility that the operations will not happen in the coherence protocol.

BedRock utilizes compound messages to reduce network traffic and enhance coherence system performance. They are sent as a single message across the network, and the main benefit of these compound messages is that it simplifies protocol correctness when using unordered networks. On an unordered network it would be possible for a sequence of ST, TR, and WB commands to arrive out of order at the cache controller, requiring protocol redesign or transient states to handle these race conditions. Races make the protocol significantly more complex and is in conflict with the design goal of simplifying the coherence system. The cache controllers must process coherence commands, including compound compounds, as atomic operations. This guarantees that the coherence state of every block at the cache controller is only visible in one of the stable MOESIF states at all times. In practice this means that coherence commands need to be serialized with cache accesses such that a cache access cannot see a block's metadata or data in different states during its lifetime.

## Fill Network

[Table 3.4](#) lists the Fill Network messages that a cache controller may send to another cache controller. Currently, the Fill network carries only Data (DATA) messages that send a full cache block and its associated state and tag to the destination controller. The state and tag portions of the message are provided by the coherence directory in an arriving Transfer command. Unlike the other coherence networks, the cache controller must support both sending and receiving messages on the Fill network.

The cache controllers must process coherence fill messages as atomic operations. This guarantees that the coherence state of every block at the cache controller is only visible in one of the stable MOESIF states at all times. In practice this means that updates to the cache data and metadata from fill messages must be serialized with cache accesses such that a cache access cannot see a block's metadata or data in different states during its lifetime.

Message	Abbreviation	Description
Invalidate Ack	InvAck	Response to an Invalidate command
Coherence Ack	CohAck	Response to finish coherence transaction
Writeback	DirtyWB	Response to Writeback command with cache block data
Null Writeback	NullWB	Response to Writeback command with no data

Table 3.5: BedRock Response Network Messages

## Response Network

Table 3.5 lists the Response Network messages that the cache controller may send to the coherence directory. Responses triggered by the receipt of a Command message. STW and DATA commands result in a Coherence Acknowledgment (CohAck) being sent back to the directory. Invalidate (INV) commands trigger an Invalidate Ack (InvAck) to the directory while Writeback (WB) commands trigger either Writeback (DirtyWB) or Null Writeback (NullWB) responses. Only DirtyWB messages carry data on the Response Network. The Response network is the highest priority network. Messages on the response network receive priority over command and request messages for processing by the coherence directory, and response messages do not cause any other messages to be sent.

### 3.2.4 Coherence Transactions and Tracking Coherence State

The BedRock coherence protocol relies on the concept of a **coherence transaction** to define the concurrency behavior of the protocol. A coherence transaction encompasses the total duration of a coherence request, beginning with the cache controller issuing a Request message to the directory and ending when the coherence directory receives the Coherence Acknowledgment (CohAck) response from the cache controller. At the cache controller, a coherence transaction begins when it issues a coherence request to the coherence directory. The coherence transaction completes when the controller receives either a STW command or a DATA message (on the Command or Fill network) and issues a CohAck response to the coherence directory. At the coherence directory, a coherence transaction begins when it starts processing a new coherence request message. The coherence transaction completes when the directory receives a CohAck response message from the cache controller that initiated the coherence request.

### 3.2.5 Protocol Assumptions

The BedRock protocol makes the following assumptions that must be enforced to ensure correct operation of the coherence protocol.

1. The coherence directory controls all coherence state transitions, with the single exception that a cache controller may silently upgrade a block from Exclusive (E) to Modified (M) on a write operation.
2. The cache controllers must not issue a duplicate coherence request until the original outstanding request is resolved.
3. The cache controllers must process all coherence commands atomically.

### 3.2.6 Coherence Protocol Tables

This section presents BedRock’s MOESIF cache coherence protocol in tabular form for both the cache controller and coherence directory [116]. The tables use a notation of ”Action/Next State” to describe the behavior of the controllers. Given the current coherence state for a cache block, as indicated at the start of the row, an entry in the table describes the action taken by the controller and the next coherence state of the block at the controller for the event indicated by the column header. If no action is required, a — is written in place of the action. Blank entries indicate that the event listed in the column header cannot occur for the state given at the start of the row. Additional tables for the other protocol variants in the MOESIF family can be found in the [Appendix A](#) and [Appendix B](#).

#### Cache Controller Protocol Table

[Table 3.6](#) presents the cache controller protocol table for the BedRock MOESIF protocol. A cache controller may experience Cache Action and Coherence Message events. Cache Actions are cacheable load and store operations. Coherence Messages are the arrival of a BedRock Command message.

Each ”Action/State” entry indicates a message sent in response to the command and the next state of the target block at the cache controller. The Action may be a response message sent to the directory or a command messages sent to another cache controller (as directed by the arriving command from the directory). Some entries in the table have a next coherence state of X that indicates the next coherence state is not known *a priori* by the cache controller. In these situations, the arriving command provides the correct coherence state, which is applied to the block by the cache controller. The specific next state is determined by the coherence directory.

#### Coherence Directory Protocol Table

[Table 3.7](#) presents the coherence directory protocol table for the BedRock MOESIF protocol. The coherence directory experiences two types of coherence events: new Coherence Requests from the cache controllers and cache block replacements (a Directory Action) that are initiated by the coherence directory while processing a coherence request. Replacements occur when a cache block in the target cache set of a coherence request must be evicted to make room for the newly requested cache block.

Each ”Action/Next State” entry provides the messages sent by the directory to cache controllers to complete processing of the request and the next state of the target block at the coherence directory. The coherence state superscripts attached to some messages in the table indicate a coherence state associated with the message or compound message component. For example, a  $ST^F$ - $TR^S$ -WB message instructs a cache controller to set the target cache block’s state to F, forward that same block to another controller with the S state, and lastly send a writeback to the coherence directory.

Replacements are only required for blocks that may be dirty (cached in the E, M or O states). Cache blocks in the S or F state are clean and do not require a separate invalidation or writeback message prior to the new cache block arriving and overwriting the existing block. The block being replaced may be freely used by the cache until it is overwritten or the invalidation and writeback occurs. Dirty blocks must be either invalidated or downgraded to a read-only state to prevent a write racing with the completion of the coherence request. Typically, dirty blocks are invalidated to conceptually align with the PUT procedure found in canonical directory-based coherence protocols.

State	Cache Action		Coherence Message												
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB					
I	ReqRd	ReqWr		CohAck/X											
S	Hit	ReqWr	InvAck/I		CohAck/M										
E	Hit	Hit/M				NullWB/E		NullWB/X	DATA/X					DATA, NullWB/X	
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X					DATA, DirtyWB/X	
O	Hit	ReqWr			CohAck/M	DirtyWB/O	DATA/O	DirtyWB/X	DATA/X						
F	Hit	ReqWr			CohAck/M		DATA/F		DATA/X						

Table 3.6: BedRock Cache Controller Protocol Table - MOESIF

Directory State	Coherence Request						Directory Action	
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	Replacement		
I	DATA to Req/E	DATA to Req/S	DATA to Req/M					
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M				
E	ST <sup>F</sup> -TR <sup>S</sup> -WB to Owner/F	ST <sup>F</sup> -TR <sup>S</sup> -WB to Owner/F	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I		
M	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I		
O	TR <sup>S</sup> to Owner/O	TR <sup>S</sup> to Owner/O	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M	ST <sup>I</sup> -WB to Req/I		
F	TR <sup>S</sup> to Owner/F	TR <sup>S</sup> to Owner/F	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M			

Table 3.7: BedRock Coherence Directory Protocol Table - MOESIF

Event	Current State	Next State
Load	I	S, E
Store	I, S, O, F	M
Store (Silent Upgrade)	E	M
Other Load	E	F
	M	O
Other Store	S, E, M, O, F	I

Table 3.8: BedRock Cache Controller Next State Table - MOESIF

### 3.2.7 Coherence State Transitions

This section describes the possible coherence state transitions at the cache and directory controllers for the BedRock MOESIF protocol. Each table describes the coherence state transitions for a single cache block given a current starting state and a cache or coherence event that causes a state transition. Events that do not cause a change in the coherence state at the controller are not listed.

#### Cache Controller State Transitions

[Table 3.8](#) enumerates the possible coherence state transitions as observed by the cache controller for a single cache block as loads and stores occur in the coherence system targeting that block. The Current State column lists the current cache coherence state of the target block and the Next State column provides the next state of the block at the cache controller. The Event column lists the type of load or store event. Events that do not cause a change in the coherence state are not listed (e.g., Load to block in S remains in S).

The first three rows correspond to actions taken by the controller itself, while the last two rows of Other Load and Other Store correspond to load and store actions initiated by some other cache controller. A Store (Silent Upgrade) occurs when the cache performs a store operation on a block cached in the E state. This state has read and write permissions but is considered clean, therefore the store must transition the block to the M state to indicate a write has occurred. This is called a Silent Upgrade since the cache controller does not need to notify the coherence directory of the write because it already has write permissions for the block.

#### Coherence Directory State Transitions

[Table 3.9](#) describes the possible coherence state transitions at the coherence directory for a single cache block as load and store misses are processed. For each event, corresponding BedRock request network message type, and current state of the coherence directory, the resulting next state of the block at both the directory and cache controller that initiated the event are listed. This table fully enumerates the possible state transitions for the MOESIF protocol, covering the cross-product of events and current directory states. In accordance with the SWMR Invariant, a store operation always results in a single cache owning the block and receiving write permissions.

As seen in the table, even when using a MOESIF protocol, the requesting cache will only ever receive a cache block in the S, E, or M states. The O and F states are used when load requests target cache blocks in either the M or E states, respectively. These states allow a single cache

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load	ReqRd	I	E	E
		S	S	S
		E, F	F	S
		M, O	O	S
Load (Non-Excl)	ReqRd-NE	I, S	S	S
		E, F	F	S
		M, O	O	S
Store	ReqWr	I, S, O, E, M, F	M	M

Table 3.9: BedRock Coherence Directory Next State Table - MOESIF

controller to retain ownership permissions for read-only cache blocks and allow a read miss to be completed with a cache to cache transfer rather than a LLC or main memory access.

Note that an event may cause the owner cache to change during the transaction, even if the block’s state at the directory does not change For example, one cache performing a write to a block that another cache already has write permissions for (i.e., cached in M) results in the state remaining in M but changes ownership of the block.

### 3.3 Uncacheable and Atomic Operations

This section describes the handling of uncached and atomic read-modify-write accesses in BedRock, using the same assumptions and canonical address space layout presented in [Section 3.2](#).

#### 3.3.1 Uncacheable Accesses

Uncacheable accesses may target both uncacheable and cacheable memory regions. Uncacheable accesses to uncacheable memory are not a concern for the BedRock coherence protocol because the protocol enforces coherence only for cacheable memory. Uncacheable accesses to uncacheable memory can either bypass the coherence directory or the directory can be augmented to forward the requests and responses to and from memory, respectively. Thus, the only changes required to support uncacheable accesses to uncacheable memory are to add appropriate request and command message types for the BedRock networks and modify the system to handle these requests, assuming that the accesses will travel on the existing BedRock networks. Endpoints that do not participate in coherence must only implement the Request and Command BedRock networks.

Uncacheable accesses to cacheable memory must participate in the BedRock coherence protocol to guarantee coherence within the system. An uncacheable access targeting a cacheable block of memory first must invalidate, and write back, the block from all cache controllers that have it cached. Then, the uncacheable access may me issued to memory with the response from memory being forwarded back to the requesting cache. This access must also be serialized with all coherence requests to the target cache block. Serializing the request is easily enforced using the existing way group and pending bit mechanisms of the coherence directory that serialize cacheable accesses.

BedRock must be modified to support the uncacheable request message types and corresponding command message types that deliver uncacheable load data or store complete confirmation to the requesting cache controller. The coherence directory must also be modified to detect an uncacheable request targeting cacheable memory and invoke the invalidation and writeback routines for the target cache block.

### 3.3.2 Atomic Read-Modify-Write Operations

Atomic read-modify-write style operations, atomics for short, are important operations for multicore processors. Consequently, a multicore processor’s memory system, including the coherence system, must support these operations. In the context of the canonical BedRock coherence system, there are two possible locations that atomics can be executed — at the LLC/memory or within the cache controller managed inclusive cache hierarchy. An atomic to uncacheable memory is assumed to be executed at the LLC/memory while an atomic to cacheable memory is executed by either the LLC/memory or the cache controller’s cache hierarchy. This is the target model used by BedRock in BlackParrot [107].

BedRock easily supports atomic operations targeting cacheable memory and executed by the cache controller’s inclusive cache hierarchy with very minimal modification to the existing cache controller. A cache executing an atomic simply needs write permissions for the target cache block. Once it has write permissions it must complete the read-modify-write sequence as a single, uninterruptible action. The simplest way to accomplish this is for the cache to perform a write request for the target block then briefly ”lock” the block while the cache completes the read-modify-write operation. After the atomic executes, the block is unlocked and any coherence commands that arrived targeting the block are processed. Although this seems to violate the spirit of BedRock in that the cache controller momentarily ignores a command from the directory, it is an effective way to implement atomics in practice. As long as the block is locked for only a very short time, there is no risk of deadlocking the coherence protocol. From the point of view of the coherence directory, a controller locking a block for a few cycles is equivalent to the coherence network taking a few extra cycles to deliver a coherence command. Since BedRock does not depend on the coherence networks delivering messages within specific latencies, the few cycles of delay from locking has no impact on correctness, so long as this delay is short and the cache controller resumes processing commands in a timely manner.

Executing atomics at LLC/memory is similar to performing an uncached memory access. The cache controller issues an atomic request with data that must be forwarded to memory for use in the read-modify-write operation, and memory responds with data if the atomic has a return value or an atomic complete message if there is not return value. The memory response is then forwarded to the requesting cache controller on the BedRock command network. This type of operation requires adding a few new message types to the BedRock request and command networks to support atomic requests and atomic data or complete commands. Atomics targeting cacheable memory and executed by the LLC/memory must follow a procedure similar to a regular uncached access to cacheable memory that invalidates and writes back the target cache block from all cache controllers possessing a copy of it. This forces any cache currently using the block to refetch it from memory, and these requests will be serialized by the coherence directory to guarantee the Data Value Invariant holds. Thus, the coherence directory must be modified in a similar manner as it was for uncacheable requests to detect atomic accesses to cacheable memory and enforce serialization of these requests using the existing way group and pending bit mechanisms.

Protocol	Cache Count					
	2	3	4	5	6	8
BedRock	0.1s	0.21s	3.1s	47s	8.9m	15.2h
Traditional	0.1s	0.35s	19.9s	10.4m	9.9h	175d
Speedup	1.0x	1.6x	6.4x	13.3x	66.6x	1230x

Table 3.10: BedRock CMurphi Verification Time and Speedup - MESI

### 3.4 Protocol Verification

The BedRock cache coherence protocol is similar to, yet subtly different from, commonly understood directory-based protocols (e.g., Section 8.3 of [96]). Therefore, it is important that the protocol itself is shown to be correct, especially since it is implemented by the BlackParrot multicore. BedRock’s MESI protocol has been verified correct using CMurphi [106], an improved version of the Murphi [40] model checking framework. The BedRock verification model is available in the BlackParrot GitHub repository.

BedRock’s CMurphi description assumes that only a single cache block and a single coherence directory are modeled. These assumptions are valid because, by definition, cache coherence is constrained to a single memory location, BedRock’s coherence directories operate independently from one another in a multi-directory system, and every cache block is managed by a single directory. The model uses unordered networks.

Table 3.10 shows the verification time required by CMurphi for BedRock and a traditional MESI coherence protocol, averaged over three runs for each configuration. Verification time for the traditional MESI protocol at 8-caches is a best-fit estimate, as it would take 175 days to complete! Both protocols are verified correct without error by CMurphi for all other configurations. CMurphi explores considerably fewer states and completes verification significantly faster for BedRock, up to 66x faster for a 6-cache system. The verification speedup is a direct consequence of BedRock’s design decisions eliminating protocol races and transient states, which greatly reduces the necessary state-space that must be explored and verified.

### 3.5 Protocol Analysis

BedRock is similar to, but subtly different from, a traditional directory-based coherence protocol. In order to better understand the design tradeoffs of directory-based coherence protocols, this section presents a comparison of the BedRock protocol to a canonical directory protocol. First, a canonical MOESIF directory-based coherence protocol is presented through state transition tables in Subsection 3.5.1. Next, a discussion of transient states and coherence networks and messages is presented in Subsection 3.5.2 and Subsection 3.5.3, respectively. Lastly, Subsection 3.5.4 presents state transition diagrams for both protocols and Subsection 3.5.5 presents mathematical models for each protocol, enabling direct comparison of the complexity inherent in each protocol.

Event	Current State	Next State
Load	I	S, E
Store	I, S, O, F	M
Store (Silent Upgrade)	E	M
Other Load	E	F
	M	O
Other Store	S, E, M, O, F	I

Table 3.11: Canonical Cache Controller Next State Table - MOESIF

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load	GetS	I	E	E
		S	S	S
		E, F	F	S
		M, O	O	S
Store	GetM	I, S, O, E, M, F	M	M

Table 3.12: Canonical Coherence Directory Next State Table - MOESIF

### 3.5.1 Stable State Transitions

Table 3.11 and Table 3.12 describe the cache and directory coherence state transitions, respectively, for a canonical directory-based coherence protocol. The cache controller state transitions are identical to the BedRock protocol. The directory state transitions are very similar to BedRock, with BedRock’s ReqRd and ReqWr messages corresponding to the canonical protocol’s GetS and GetM messages, respectively. The canonical protocol does not have a direct equivalence to BedRock’s ReqRd (Non-Excl) message, although it could easily be added, for example by a special GetS message variant that would have similar or identical semantics to ReqRd (Non-Excl).

The similarity of these tables is expected and intuitive since both protocols rely on the same set of stable protocol states and these states have the same semantics in each protocol. The state transitions between the stable states of a coherence protocol depends only on the set of stable states and the possible events. In canonical stored-program [97], or *von Neumann*, multicore processor architectures utilizing hardware-based cache coherence systems, the set of possible events is effectively only load and store operations. Complex memory operations include load-reserved/store-conditional (LRSC) and atomic read-modify-write (AMO, Atomic RMW) are constructed as special load and store operations or pairs, but the primitive events remain loads and stores. Thus, the canonical protocol described and BedRock are effectively equivalent when viewed at this level because they employ the same set of stable states (MOESIF) and have the same set of possible events (load or store).

The similarity of these protocols at this level also illustrates the importance of understanding the

details of a given coherence protocol when determining its advantages, disadvantages, objectives, and non-objectives. The degree to which transient states are employed or the number and ordering of coherence networks required are properties of the protocol's implementation. These details are important in practice because they directly correlate with the complexity, cost, and performance of a coherence protocol's implementation.

### 3.5.2 Transient States

Transient states exist in canonical directory-based coherence protocols to handle race conditions or provide additional transaction concurrency within the protocol. Unlike a canonical protocol, BedRock does not expose any transient states in the coherence protocol. BedRock is able to realize a protocol without exposed transient states due to its assumptions that only a single coherence transaction per way group may be active at any time and that each cache controller must not issue duplicate coherence requests. The cache controllers may access cache blocks with their existing permissions, but must request new permissions from the directory as needed. Coherence commands are processed atomically by the cache controllers to guarantee that cache accesses only ever see a cache block in a single stable and consistent state. The coherence directory updates the stable state of a cache block as it issues messages to change the state of the block. Since the directory only processes one request per way group at a time there is no need to expose transient states in the protocol. Implementations may define mechanisms to track the transient behavior of the request processing flow (e.g., invalidations completed, waiting for coherence acknowledgment) in order to enable concurrent processing of independent requests, but at the protocol level all blocks will be in a consistent and stable state at all times.

Canonical protocols also vary in the number and types of transient states defined in the protocol. Simple canonical protocols have fewer transient states and allow less concurrency across transactions targeting the same cache block. This manifests as stall conditions in protocol processing that blocks new requests from targeting a cache block that already has one or more active transactions. A major drawback of transient states is that verification effort typically grows super-linearly or exponentially with the number of protocol states, including both stable and transient states. Thus, while transient states allow more per-block concurrency, the verification complexity cost limits the amount of concurrency that architects are willing to add in practice. As will be seen in [Chapter 4](#) and [Chapter 5](#), concurrency across cache blocks can be realized through coherence engine implementation decisions that do not alter the coherence protocol specification.

### 3.5.3 Coherence Networks and Protocol Messages

BedRock utilizes four coherence networks instead of the three networks used by the canonical protocol. In BedRock, only the Fill network is bi-directional. The Request, Command, and Response networks are all uni-directional and carry messages between the cache controllers and the coherence directory. In contrast, canonical protocols utilize uni-directional request and forwarded request networks with a bi-directional response network.

BedRock assumes that there may only be one active coherence transaction per way group, that the directory controls cache block replacements, that all response messages return to the directory, and that all networks are unordered. These design constraints necessitate the use of a coherence acknowledgment message from cache to directory to close the transaction and requires a fourth coherence message class and network with higher priority than the canonical directory protocol's response network to carry the coherence acknowledgment message. The fourth network is necessary

BedRock Network	BedRock Message	Canonical Protocol Message
Request	ReqRd	GetE
	ReqRd-NE	GetS
	ReqWr	GetM or Upgrade
Command	Inv	Inv
	DATA	Data from Dir or Owner
	STW	Data from Dir (ack=0)
	WB	No direct equivalence
	TR	Fwd-GetX
	ST-WB	No direct equivalence
	ST-TR	Fwd-GetX
	ST-TR-WB	Fwd-GetX
Fill	DATA	Data from Owner
Response	InvAck	Inv-Ack
	CohAck	No direct equivalence
	DirtyWB	PUTM, PUTO
	NullWB	PUTS, PUTE, PUTF

Table 3.13: BedRock and Canonical Directory Protocol Message Equivalency

to accommodate transactions involving cache to cache transfers, which require four phases or hops: Request to directory, Command to owner, Fill from owner to requester, Response to directory.

Table 3.13 presents a comparison of the message types in BedRock and those used in a canonical protocol. The corresponding message types of the traditional protocol are found in Tables 6.4, 8.3, 8.4, 8.5, and 8.6 of [96]. A Fwd-GetX message corresponds to a Fwd-Get message with state specified by X, where X is one of the MOESIF states as applicable for a specific instance of the message (e.g., Fwd-GetS or Fwd-GetM). The PUT messages have also been extended to cover all of the MOESIF states. As seen in the table, many BedRock messages have direct equivalences in the traditional protocol. However, a few important differences are worth discussing.

First, BedRock carries coherence messages on four networks instead of three, so there is not a one-to-one correspondence to the three networks of the traditional protocol, which are called Request, Forwarded-Request, and Response. The Request network is similar in each protocol as they carry coherence requests from cache controller to coherence directory. BedRock’s Command network is similar to the Forwarded-Request network as both networks carry messages from the coherence directory to the cache controller. BedRock’s Response and Fill networks carry messages similar to the traditional protocol’s Response network. BedRock requires four networks to maintain priority between messages in the protocol due to the use of coherence acknowledgment messages and directory-controlled cache block replacements.

Second, there is no cache controller Replacement message that can be issued on BedRock’s Request

network. Unlike a traditional protocol, the coherence directory, not the cache controller, is responsible for performing cache block replacements to make room for new cache blocks in the cache controller. The cache controller provides a replacement way "hint" to the coherence directory with each read or write request. The coherence directory then finalizes the selection of a replacement way, writing back any dirty cache block data as required by issuing a WB message over the Command Network. BedRock's directory-controlled replacements eliminate a common race between PUT and Fwd-Get messages in the traditional protocol. Thus, one view of the WB message is that it is a directory-initiated PUT and that PUT messages are from directory to cache rather than cache to directory as in the traditional protocol.

Third, the ST-WB message has no direct equivalence in the traditional protocol. ST-WB can be viewed as a directory-initiated PUT message for a dirty cache block. The intent of these messages is to downgrade the permissions of a particular cache block, writing back the dirty block, and then modifying the coherence state of the block. ST-WB is commonly used to combine an invalidate and writeback sequence into a single command/response pair since the DirtyWB or NullWB response serves as an acknowledgment of both the writeback and invalidation actions.

Lastly, the traditional protocol does not require a CohAck message to close a coherence transaction. This message is required to enforce correct serialization of coherence requests targeting the same cache block at the directory controller when using unordered networks. The use of an explicit coherence transaction acknowledgment disallows concurrent transactions to the same block and enables the removal of many transient states from the coherence protocol required to handle races at the cache controller.

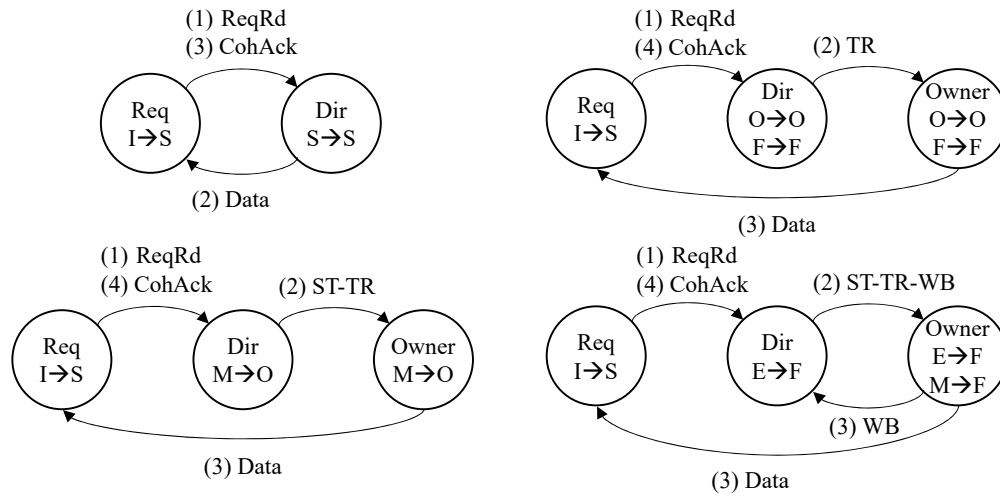


Figure 3.5: BedRock I→S Transitions

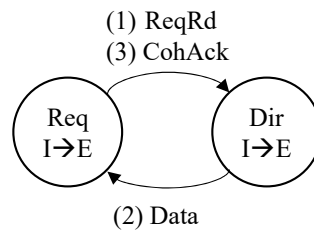


Figure 3.6: BedRock I→E Transitions

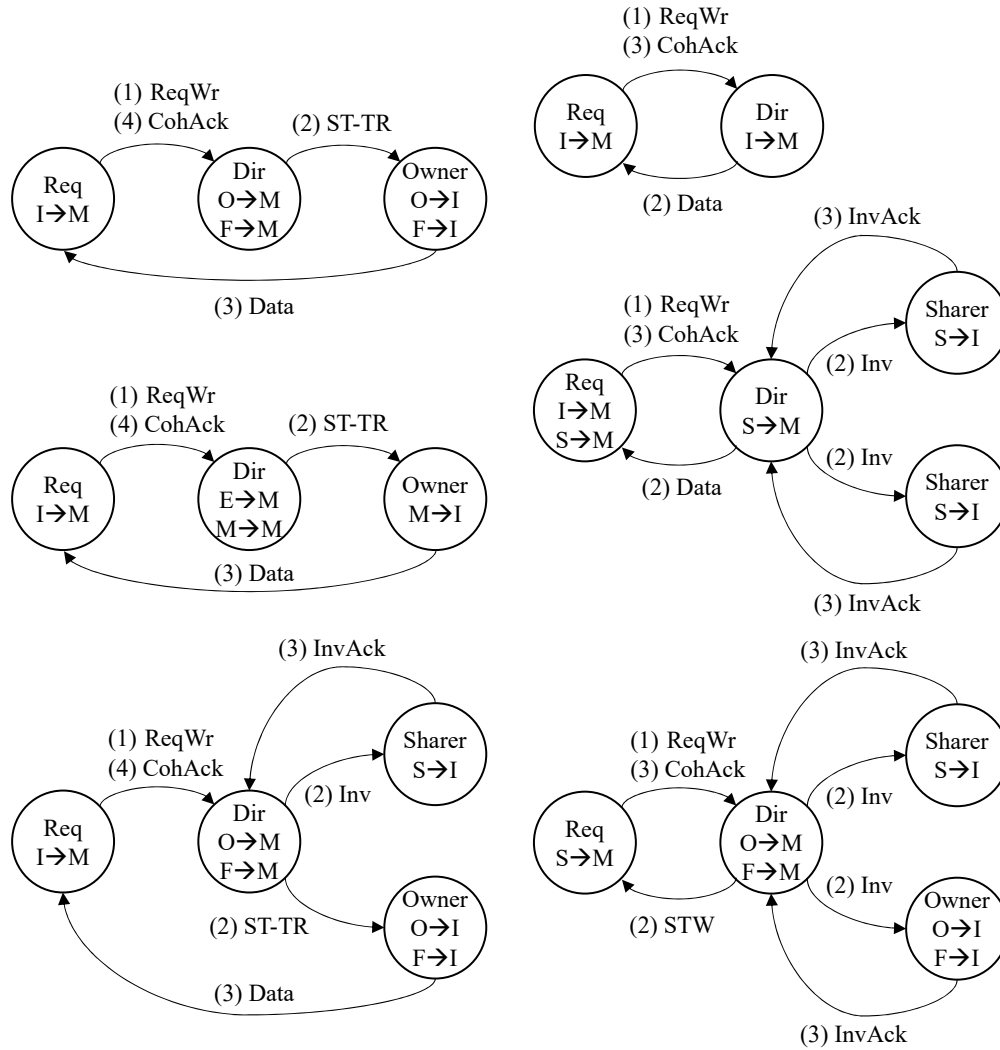


Figure 3.7: BedRock I/S→M Transitions

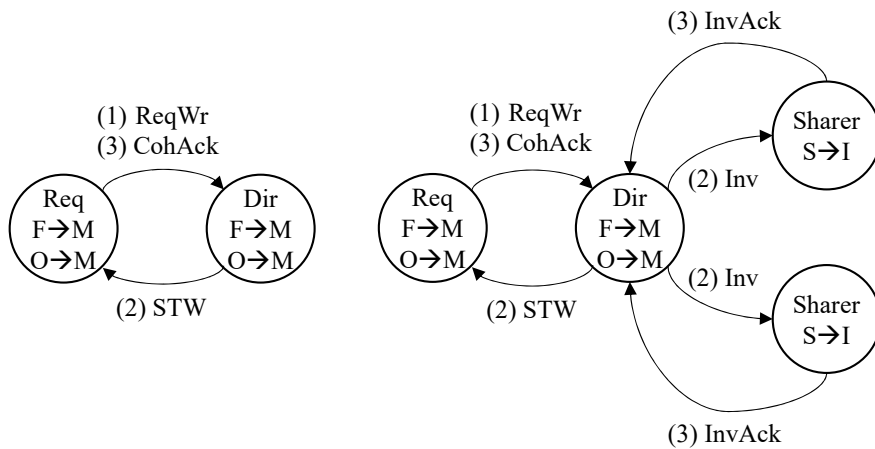


Figure 3.8: BedRock F/O→M Transitions

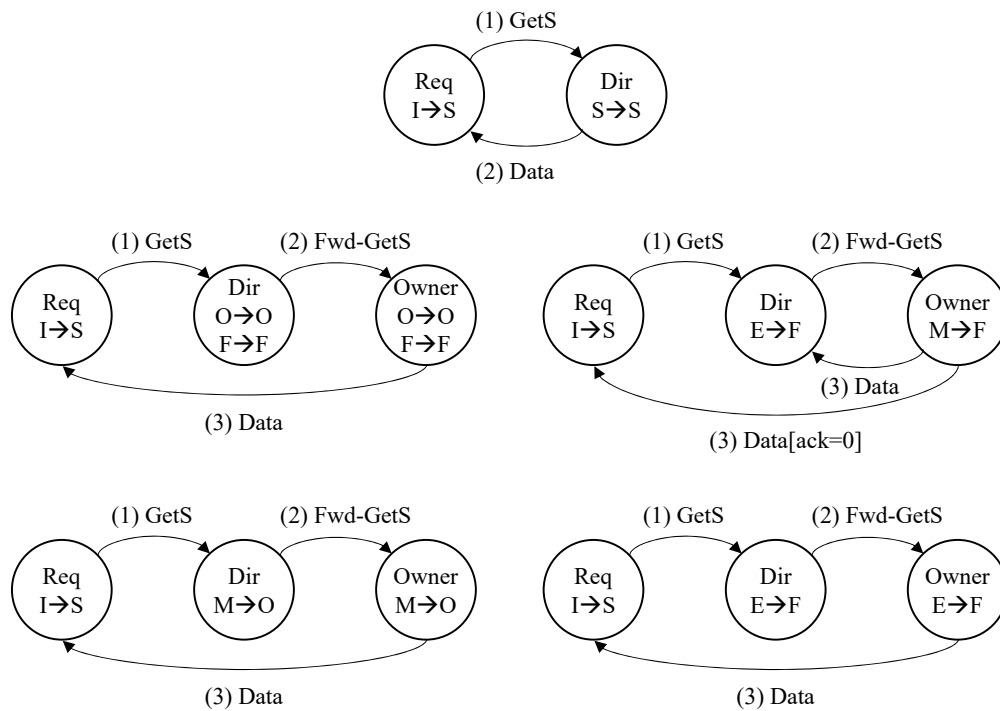


Figure 3.9: Canonical I→S Transitions

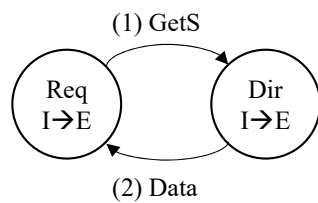


Figure 3.10: Canonical I→E Transitions

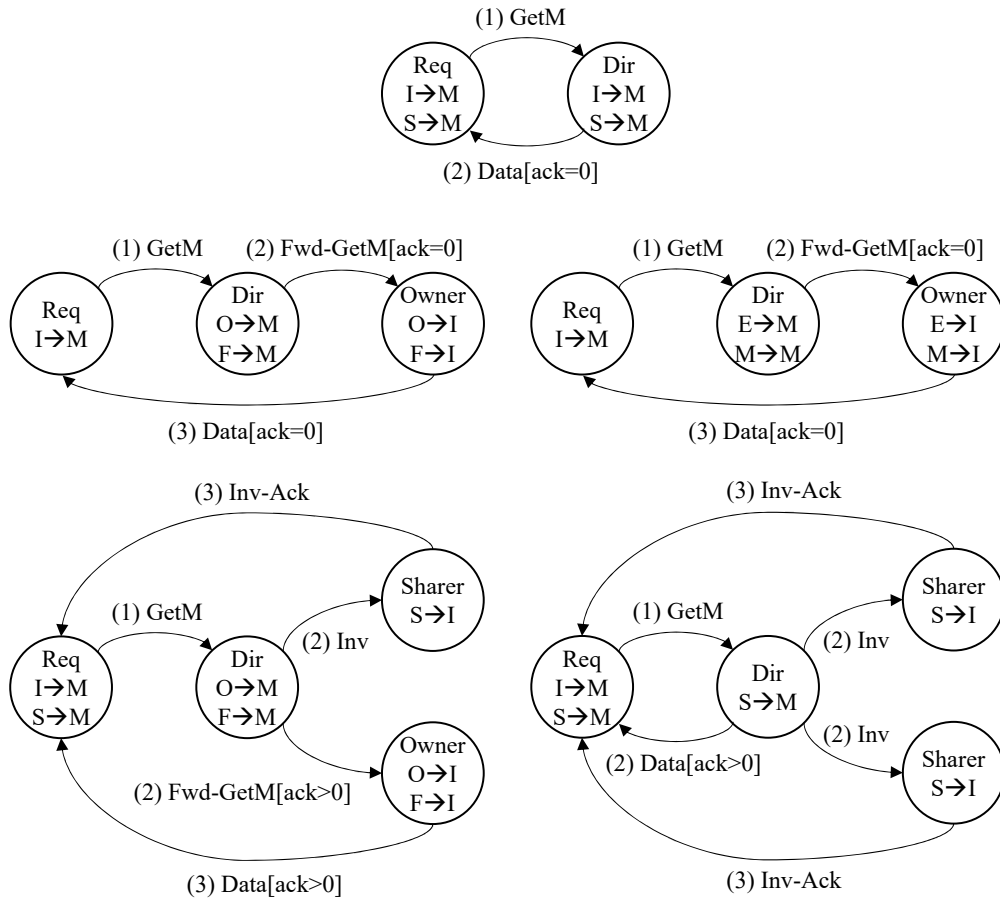


Figure 3.11: Canonical I/S→M Transitions

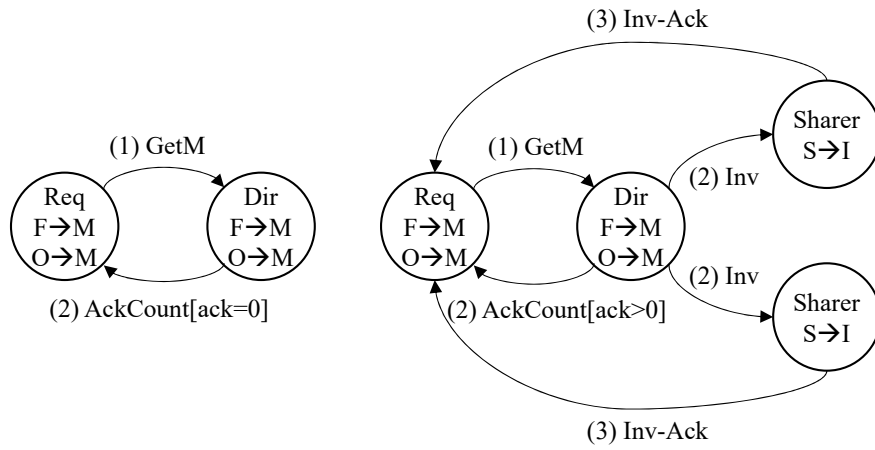


Figure 3.12: Canonical F/O→M Transitions

### 3.5.4 Coherence State Transition Diagrams

The preceding sections outline how BedRock differs from a canonical directory protocol in terms of stable state transitions, transient states, coherence networks, and protocol messages. In this section, state transition diagrams are presented for both BedRock and the canonical protocol to further illustrate the subtle differences in how specific events are handled given initial cache block and coherence directory state.

In the state transition diagrams, arrows represent messages and circles represent caches or the directory. Each arrow is labeled with a number and the message name. The number indicates the sequence of messages in the depicted transaction. Each circle may be the directory (Dir) or a cache. A cache may be either the requester (Req), the current owner of the cache block (Owner), or a sharer with read-only permissions (Sharer).

#### BedRock Protocol

Figure 3.5, Figure 3.6, Figure 3.7, and Figure 3.8 present the possible state transitions for the BedRock protocol. These diagrams clearly illustrate the role that the coherence directory plays in orchestrating and completing all coherence requests. All commands are issued by the coherence directory and all responses are sent from the caches to the directory. Additionally, every transaction is closed by the cache sending a coherence acknowledgment (CohAck) response to the directory, which informs the directory that the transaction is complete. The coherence ack is required since BedRock assumes unordered networks are used to implement the protocol.

Read requests that transition the requester from the Invalid (I) state to the Shared (S) state require either three or four phases. The first phase occurs when the requesting cache issues a request to the directory. The second phase is always the directory issuing one or more commands to caches. In the simplest case, the directory reads the requested block from memory and sends a data command to the requester. In cases where the block has an owner, the directory sends some combination of set state, transfer, and writeback commands as a single compound command message to the cache block owner, directing the owner to send the cache block data to the requester. If the directory records the block in the Exclusive (E) state, a writeback must be commanded to ensure that memory and the caches have consistent state. A writeback and the cache to cache transfer can be performed concurrently as the third phase of the transaction. The final phase of all transactions is the coherence acknowledgment phase.

A read request for a block currently in the Invalid (I) state in the directory results in a three-phase transaction comprising the request, data command to the requester from the directory, and the coherence acknowledgment to close the transaction.

Write requests transition the requester from Invalid (I), Shared (S), Owned (O), or Forward (F) states to Modified (M). These requests also require either three or four phases to complete. At the protocol level, commands issued to the requester, sharers, and owners, can, in most cases, occur in the same phase and concurrent to one another. The simplest transactions require three phases. The first phase occurs when the requesting cache issues a request to the directory. The second phase comprises the directory sending data or a coherence state update to the requester, possibly overlapped with the the directory commanding other caches to invalidate the target block. The third phase is the coherence ack from the requester to the directory. The four phase write transactions involve cache to cache transfers, similar to the four phase read request transactions. The second and third phases of these transactions involve the directory commanding the current

owner to perform a cache to cache transfer followed by the data being transferred from the current owner to the requester.

### Canonical Protocol

Figure 3.9, Figure 3.10, Figure 3.11, and Figure 3.12 present the possible state transitions for a canonical directory protocol. As implied by the use of only three coherence networks, the canonical directory protocol requires a maximum of three phases for all coherence transactions. Every transaction begins with the requester sending a coherence request to the coherence directory. Next, the coherence directory either replies directly to the requester with the requested cache block or upgraded permissions or forwards the request to the current cache block owner. The third phase of a transaction comprises data and invalidation messages traveling from other caches to the requesting cache on the response network.

For read transactions, two phases are required when the cache block data is sourced from memory while three phases are required to source cache block data from another cache. In these transactions, the third phase comprises a single data message. Similarly, only two phases are required for write transactions that source cache block data from memory via the directory or only require upgraded permissions from the directory while three phases are required to perform cache to cache transfers or to accumulate invalidations from the other sharer caches. Unlike read transactions, three-phase write transactions may involve multiple response messages being sent to the requesting cache. These messages include both the cache to cache data transfer as well as invalidation acknowledgment messages to inform the requester that all other caches in the system have relinquished permissions for the target block.

### Comparing Protocols

BedRock and the canonical directory protocol differ in a few important ways, which are illustrated by the protocol transition diagrams. First, BedRock's assumption of unordered networks necessitates the use of a fourth coherence network and an additional transaction phase for all transactions relative to the canonical protocol. This manifests as a second message from cache controller to coherence directory for every transaction in the form of the coherence acknowledgment response. A canonical protocol implemented using unordered networks may not necessitate the introduction of an additional coherence network or transaction phase, but it would require additional transient states in the protocol to manage race conditions that become possible when point-to-point ordering is not guaranteed by the coherence networks. The fourth phase does not necessarily add any latency to the transaction from the point of view of the requesting cache, since the requested block can be used as soon as the cache data (DATA) or set state and wakeup (STW) message arrives. The coherence acknowledgment message from requester to directory can be sent immediately after the cache processes the third-phase message and its transit over the response network occurs concurrently with the requester resuming execution. Subsequent transactions targeting the same block and originating from other caches may experience small processing delays if they arrive at the coherence directory prior to the coherence acknowledgment returning from the first requester. However, implementations may be able to recover concurrency or hide the coherence acknowledgment latency by overlapping initial processing of the subsequent transaction with waiting for the coherence acknowledgment to return.

Second, BedRock's decision to centralize state management at the directory results in the requesting cache controller receiving exactly one message to resolve every coherence transaction. This greatly

Event	Cache State Transition	Directory State	Mathematical Model
Load	I → S	S	$Req + Dir + Mem + Data + Ack$
	I → S	F, O	$Req + Dir + Cmd + Fill + Ack$
	I → S	E, M	$Req + Dir + Cmd + Fill + Ack$
	I → E	I	$Req + Dir + Mem + Data + Ack$
Store	I → M	I	$Req + Dir + Mem + Data + Ack$
	I, S → M	S	$Req + Dir + Max(Inv + InvAck, Mem + Data + Ack)$
	I → M	E, M	$Req + Dir + Cmd + Fill + Ack$
	I → M	F, O	$Req + Dir + Cmd + Fill + Ack$
	I → M	F, O	$Req + Dir + Max(Inv + InvAck, Cmd + Fill + Ack)$
	S → M	F, O	$Req + Dir + Max(Inv + InvAck, Cmd + Ack)$
	F, O → M	F, O	$Req + Dir + Cmd + Ack$
	F, O → M	F, O	$Req + Dir + Max(Inv + InvAck, Cmd + Ack)$

Table 3.14: BedRock Protocol Mathematical Model - MOESIF

simplifies the protocol specification and implementation at the cache controllers. There is no need for the cache controller to include complex logic to determine the next action to take or how many messages to wait for before closing a transaction, rather the single command or fill provides permissions, and if needed, cache block data that satisfies the request. The controller must only then respond with a coherence acknowledgment concurrent to completing the cache’s request.

Third, the coherence directory in BedRock is the recipient of all response messages. In BedRock, the coherence directory exclusively manages the state transitions of the target cache block in all caches, simplifying the implementation of the cache controllers. Additionally, the directory implementation can control the degree of concurrency among invalidating sharers and fulfilling the request by either directly providing data and permissions or commanding a cache to cache transfer. However, the canonical protocol is unable to realize this type of intra-transaction message concurrency. In contrast, the canonical protocol requires the cache controller to manage the accumulation of response messages such as invalidations in order to determine when the requested cache block can safely enter a stable state. The complexity of managing protocol races at the cache controllers can be seen in the canonical protocol’s specification tables for the cache controller [96]. Requiring the cache controller to accumulate all responses, including invalidation acknowledgments, may introduce latency to the transaction as the requester waits for the possibly large number of messages.

### 3.5.5 Mathematical Models

Using the protocol tables and processing diagrams, it is possible to derive mathematical models of the BedRock and canonical coherence protocols. Table 3.14 provides mathematical formulae describing coherence transactions for the BedRock protocol. Table 3.15 provides mathematical formulae for the same coherence transactions but in the canonical directory protocol. These models

Event	Cache State Transition	Directory State	Mathematical Model
Load	$I \rightarrow S$	S	$Req + Dir + Mem + Data$
	$I \rightarrow S$	F, O	$Req + Dir + FwdGet + Data$
	$I \rightarrow S$	E, M	$Req + Dir + FwdGet + Data$
	$I \rightarrow E$	I	$Req + Dir + Mem + Data$
Store	$I \rightarrow M$	I	$Req + Dir + Mem + Data$
	$S \rightarrow M$	S	$Req + Dir + Mem + Data$
	$I, S \rightarrow M$	S	$Req + Dir + Max(Mem + Data, Inv + InvAck)$
	$I \rightarrow M$	E, M	$Req + Dir + FwdGet + Data$
	$I \rightarrow M$	F, O	$Req + Dir + FwdGet + Data$
	$I, S \rightarrow M$	F, O	$Req + Dir + Max(Inv + InvAck, FwdGet + Data)$
	$F, O \rightarrow M$	F, O	$Req + Dir + AckCount(0)$
	$F, O \rightarrow M$	F, O	$Req + Dir + Max(AckCount(N), Inv + InvAck)$

Table 3.15: Canonical Directory Protocol Mathematical Model - MOESIF

follow directly from the transaction processing diagrams shown above.

Examining the formulae, it is clear that BedRock incurs additional latency per transaction to transmit the coherence acknowledgment (CohAck) message from the requester to the directory due to the extra transaction phase required by the protocol’s assumption of unordered networks. However, the mathematical models are otherwise effectively equivalent for the two protocols. All commands issued from the BedRock directory can be issued and processed concurrently in the system, as can response messages such as writebacks or invalidations from the owner or sharers, respectively, to the directory. Likewise, commands issued from the directory in the canonical protocol can be executed concurrently in the system. In the most complex transactions, the overall latency is likely determined by the relative costs of these concurrent operations. For BedRock this means that the latency incurred at the directory is typically the worst-case latency of receiving responses to the various commands it has issued while for the canonical protocol the requester experiences the worst-case latency of receiving responses. Thus, BedRock demonstrates a tradeoff in protocol design that can reduce the latency experienced at the cache controllers at the expense of latency incurred by the coherence directory.

These models demonstrate that at the highest level descriptions of the two protocols, it is not clear which may perform better in a given implementation. The impact of particular command and response latencies may manifest differently at the cache controllers and coherence directories in each of the protocols. In BedRock, the requester does not incur the CohAck latency as a cost prior to using the block since this message can be sent concurrently to the cache using the block. In the canonical protocol, the directory does not incur the cost of processing certain response messages as they are sent directly to the requesting cache controller. Further, the latencies experienced for certain phases depends on the amount of contention and sharing for the requested cache block. The models reveal the importance of implementation decisions in determining actual protocol performance. While different protocols exhibit unique latency savings or costs, whether those costs

manifest in a real system depends on the realized protocol implementation.

### 3.6 Conclusion

The BedRock cache coherence protocol presented in this chapter is an easy to implement directory-based cache coherence protocol that is well-suited for small- to medium-scale shared-memory multicore processors. The preceding description of BedRock provides a complete specification of the protocol in tabular form along with a description of the necessary system components, coherence states, coherence networks, and coherence messages required by the protocol. BedRock's emphasis on reducing protocol complexity results in a race-free protocol that requires significantly less verification effort than a canonical directory-based protocol. Additionally, removing races from the protocol results in a simple and straightforward cache controller protocol specification and the elimination of transient states from the entire protocol. A comparison of BedRock to a canonical directory-based protocol shows that BedRock requires an additional transaction phase and may provide less per-block transaction concurrency compared to the canonical protocol. However, since the cache coherence directory explicitly manages all coherence state transitions in the system and is the destination of all response messages, the cache controllers are not required to wait for messages from other caches except during cache to cache transfers. The specification and analysis of BedRock reveal that the design tradeoffs of cache coherence protocols are not always straightforward and different choices may be appropriate for different systems.

## Chapter 4

# BlackParrot-BedRock

Cache coherence protocols define the semantics of how access permissions for a particular block (or word) of memory are acquired and relinquished throughout execution. However, the protocol itself provides little insight into the actual performance and implementation implications of the realized protocol in a shared-memory multicore processor design.

A primary contribution of this dissertation is the open-source implementation of the BedRock cache coherence protocol within the BlackParrot shared-memory multicore processor, called BlackParrot-BedRock (BP-BedRock). In this chapter, the architecture and microarchitecture of BP-BedRock is described in detail. First, [Section 4.1](#) describes the on-chip network protocol underpinning the BedRock coherence networks. Next, [Section 4.2](#) describes the design of the cache coherence controller or Local Cache Engine (LCE). [Section 4.3](#), [Section 4.4](#), and [Section 4.5](#) detail the architecture and microarchitecture design of BedRock’s cache coherence directory and the fixed-function and programmable directory controllers. Lastly, [Section 4.6](#) and [Section 4.7](#) compare the two coherence directory controller designs by examining protocol processing performance and area and resource implementation costs.

The implementation of BP-BedRock is written in SystemVerilog[65], fully open-source, and available at <https://github.com/black-parrot/black-parrot>.

### 4.1 BP-BedRock Stream Protocol

In an effort to reduce implementation complexity, all BedRock coherence network and BlackParrot memory network protocol messages are carried across on-chip networks utilizing a common message format and handshaking protocol called the BP-BedRock Stream protocol. [Figure 4.1](#) depicts the signals found in the BP-BedRock Stream message protocol. Every protocol message comprises one or more message *beats* that transmits both header and data information in parallel. The message handshaking uses a *ready&valid*[121] protocol that exchanges the header and data information from manager (sender) to subordinate (receiver) during the cycle in which both the sender asserts the single-bit *valid* signal and the receiver asserts the single-bit *ready\_and* signal.

[Listing 4.1](#) shows the SystemVerilog macro code used to define the header component of a BP-BedRock coherence network message. Each header comprises a message type, a write sub-operation if necessary, the address associated with the message (or transaction), a message size, and a network-opaque payload that is customized for each particular protocol network.

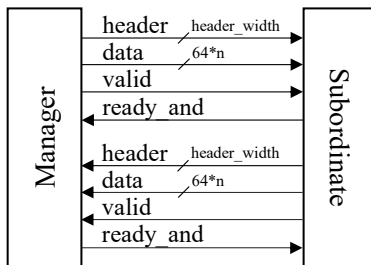


Figure 4.1: BP-Bedrock Stream Protocol

```

#define declare_bp_bedrock_header_s(addr_width_mp, payload_mp, name_mp) \
  typedef struct packed \
  { \
    payload_mp          payload; \
    bp_bedrock_msg_size_e size; \
    logic [addr_width_mp-1:0] addr; \
    bp_bedrock_wr_subop_e subop; \
    bp_bedrock_msg_u     msg_type; \
  } bp_bedrock_`name_mp`_header_s;
  
```

Listing 4.1: BedRock Message Header Macro

The message type field is a union that holds a protocol network-specific message type, as described in [Section 3.2](#) for the BedRock coherence networks or a read, write, or atomic type for a memory network message. The write sub-operation field specifies whether a write request message on the request network is a standard write operation or the type of atomic operation that generated the request. The address field is typically either a cache block- or data word-aligned (32b- or 64b-aligned) address for the block containing the address that caused a cache miss and initiated a coherence transaction. Valid message sizes are between 1 and 128 bytes, by powers of two. The payload field is network-specific. For some networks, this field carries metadata about the transaction while on other networks it contains information that augments the other fields and informs the message receiver how to process a particular message. For example, command network messages that initiate cache to cache data transfers use the payload field to define the which cache is the destination of the transfer and the coherence state that the block for the transfer destination.

### 4.1.1 Stream Pumps

The BP-BedRock implementation of the Stream protocol relies heavily on modules called Stream Pumps to interface protocol processing logic with the protocol network interfaces. Stream pumps are implemented for both message send and receive, or output and input, respectively. Both types of stream pumps provide minimal message buffering to manage backpressure and to decouple the network interface and protocol processing logic. Stream pumps also act as a *gearbox* that can convert message data widths between the network interface and protocol logic, allowing the protocol logic to operate with whichever per-beat data width is most optimal while allowing the on-chip network implementation to be independently sized for system-level power, performance, and area considerations.

The key logical benefit of stream pumps is in the interface they expose to the protocol processing logic. The stream pump generates *new*, *last*, *critical*, and *address* signals in addition to message

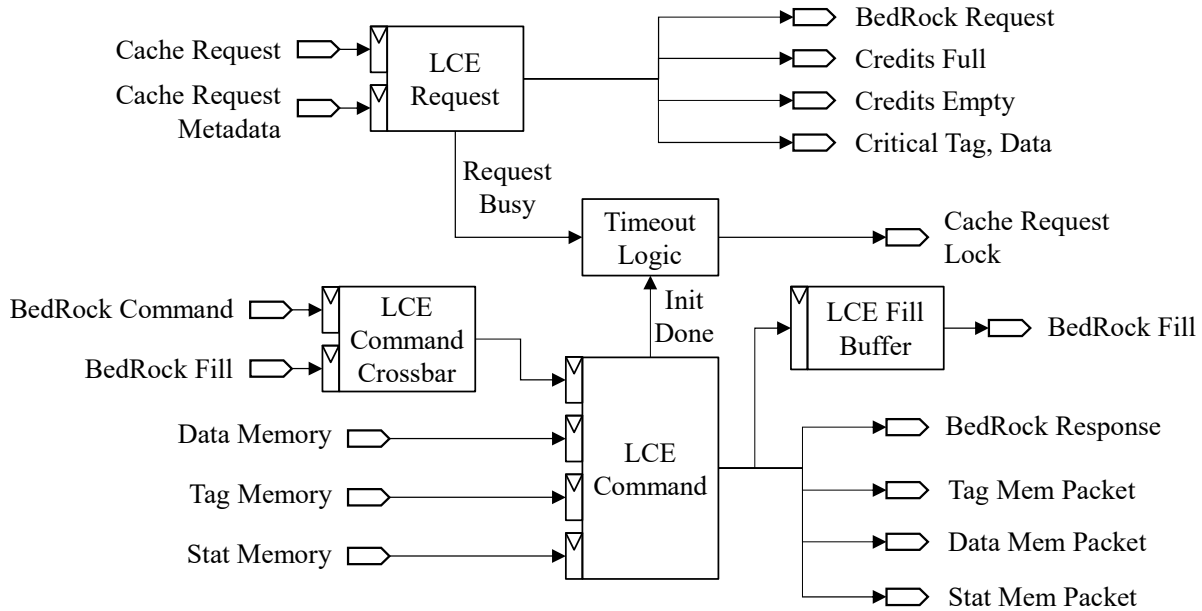


Figure 4.2: BP-BedRock LCE Block Diagram

header and data signals that can be examined by the protocol processing logic to easily take action at important points in messaging processing. The new signal is asserted on the first beat of a message, the last signal is asserted on the final beat of a message, and the critical signal is asserted on the beat of the message that contains the data specified by the message’s address. In multi-beat messages that use a word-aligned address, the critical signal may be asserted on any beat. The critical signal enables easy implementation of *critical-word-first* data return for caches, which is a commonly desired performance optimization. The address signal provides the effective per-beat, data channel width-aligned address for every beat in the message, which is incredibly useful when interacting with cache or memory data storage elements. Addressing utilizes a message-size aligned wrapping computation, similar to the WRAP burst type defined in the AMBA AXI4 protocol[7].

## 4.2 Local Cache Engine (LCE)

The cache coherence controller in BedRock is called a Local Cache Engine (LCE). In BP-BedRock there is one LCE attached to each private L1 cache in the multicore processor. The LCE processes cache requests and manages cache coherence for the cache by participating in the BP-BedRock coherence system. As discussed in [Section 2.3](#), the cache and LCE are connected through the cache engine interface, and the LCE connects to the BedRock coherence network using the BedRock Request, Command, Fill, and Response networks.

[Figure 4.2](#) shows a block diagram for the BP-BedRock LCE design. The LCE has two concurrently executing finite state machines (FSM) that are responsible for processing cache requests from the attached cache and coherence network messages arriving at the LCE. The two state machines are called the Request FSM and Command FSM, and each FSM is implemented in a separate SystemVerilog module. The top-level LCE module instantiates the Request and Command modules. The LCE also includes timeout logic to guarantee forward progress of the BP-BedRock coherence system as a whole and arbitration logic for the cache fill interface ports. The Fill and Command networks are multiplexed into a single interleave stream of commands through the LCE Command

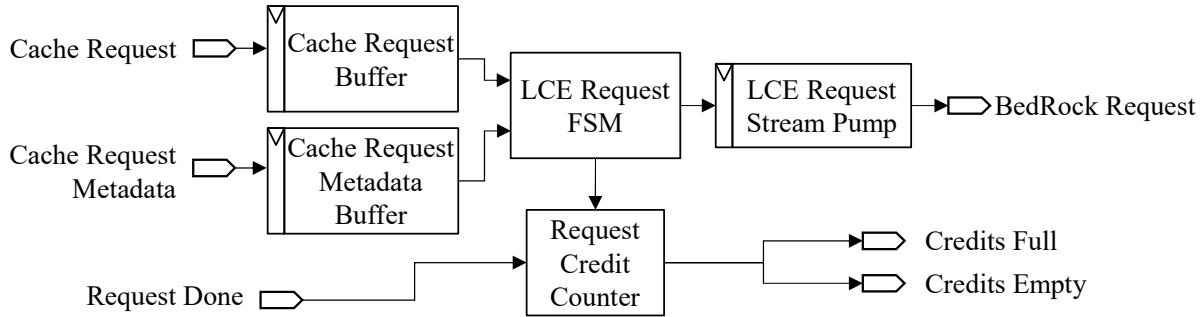


Figure 4.3: BP-BedRock LCE Request Block Diagram

Crossbar before being processed by the Command FSM.

The BP-BedRock LCE supports cacheable, uncacheable, and atomic read-modify-write operations to lower levels of the memory hierarchy. As discussed in [Section 2.3](#), the BP-BedRock L1 caches are blocking for cacheable requests, uncacheable loads, and atomics, and non-blocking for uncacheable stores. The LCE implementation supports identical behavior. [Figure 4.4](#) and [Figure 4.6](#) provide state machine diagrams for the two LCE state machines and are explained in detail below. The initial states for each FSM are shaded blue. States with pink outlines may require more than a single cycle to execute, depending on the type of request or message being processed by the state machine.

Depending on execution behavior, the type of message or event being processed, or resource contention, it is generally possible for any state to take one or more cycles to execute. States outlined in black are expected to take a single cycle to execute under ideal no-contention execution, while states outlined in pink/magenta are commonly expected to take more than one cycle to execute.

#### 4.2.1 Request Processing

The BP-BedRock LCE Request logic processes cache requests arriving on the cache engine request interface. Each cache request results in a single BedRock Request message sent from the LCE to a CCE. [Figure 4.3](#) shows the organization of the LCE Request processing module in the LCE. Cache requests and their metadata arriving from the BlackParrot L1 cache are buffered and then processed by the LCE Request FSM. The request processing state machine consumes one credit per request issued and limits the total number of outstanding requests to a design-parameterized credit limit. Backpressure is applied to the L1 cache via the cache request buffers and the credit-based flow control, and if the LCE is unable to accept a new cache miss request the BlackParrot cache pipeline will stall and attempt to replay the access at a later cycle. In the current BP-BedRock implementation, this counter only limits the number of uncacheable stores, as all other operations are blocking and limited to one per LCE.

The request state machine is a multi-cycle FSM, and is depicted in [Figure 4.4](#). The state machine waits for new requests from the cache in the Ready state. Non-blocking uncached store operations are issued from the Ready state as soon as the request and its metadata are available. All blocking requests proceed to the Send Request state, which issues the appropriate LCE Request message to the CCE before transitioning to the Wait for Done state, which waits for a signal from the cache indicating the cache miss has been resolved and a new cache miss may be processed. The backoff state is used to apply backpressure to the L1 cache when the LCE is already processing a cache request.

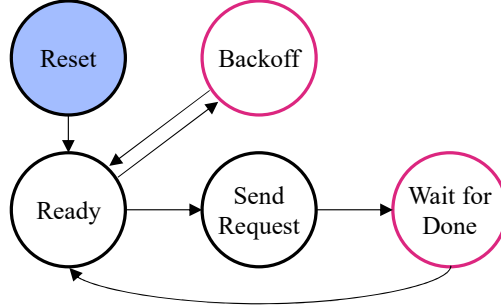


Figure 4.4: BP-BedRock LCE Request FSM

Cache Request	Occupancy (cycles)	Initiation Interval (cycles)	Description
Cacheable Load, Cacheable Store	$2 + N$	–	Block-based cache miss, send cacheable miss request
Uncacheable Load	$2 + N$	–	1, 2, 4, or 8-byte load, send uncached load request
Uncacheable Store	1	1	1, 2, 4, or 8-byte store, send uncached store request
Uncacheable Atomic	$2 + N$	–	4 or 8-byte atomic read-modify-write, send uncached amo request

Table 4.1: BP-BedRock LCE Request State Machine Occupancy

### Request Occupancy

Table 4.1 describes the request state machine’s no-contention occupancy and throughput for each possible cache request, both given in cycles. The occupancy is the number of cycles required to process a cache request, beginning with the cycle that the cache request is valid and available for processing by the state machine. The initiation interval describes the achievable throughput for consecutive non-blocking operations, as the number of cycles required to issue an additional request of the same type.

In the request state machine, uncacheable stores have an occupancy of one cycle, and all other operations have an occupancy of two plus  $N$  cycles. Uncacheable stores require a single cycle to issue the request header and data on the outbound network via the request stream pump, and uncacheable store requests can be issued in consecutive cycles with an initiation interval of one cycle, or one request every cycle. Cacheable requests, uncacheable loads, and uncacheable atomics all require two cycles to receive the request from the cache and issue the coherence request message via the request stream pump. These requests require an additional  $N$  cycles of waiting for the transaction to complete before a new transaction can be processed.

The BlackParrot L1 cache provides the request metadata in the cycle following the request packet, however the BP-BedRock LCE actually supports receiving the metadata as soon as the same cycle as the request packet. This one cycle of latency is accounted for by registering the valid cache

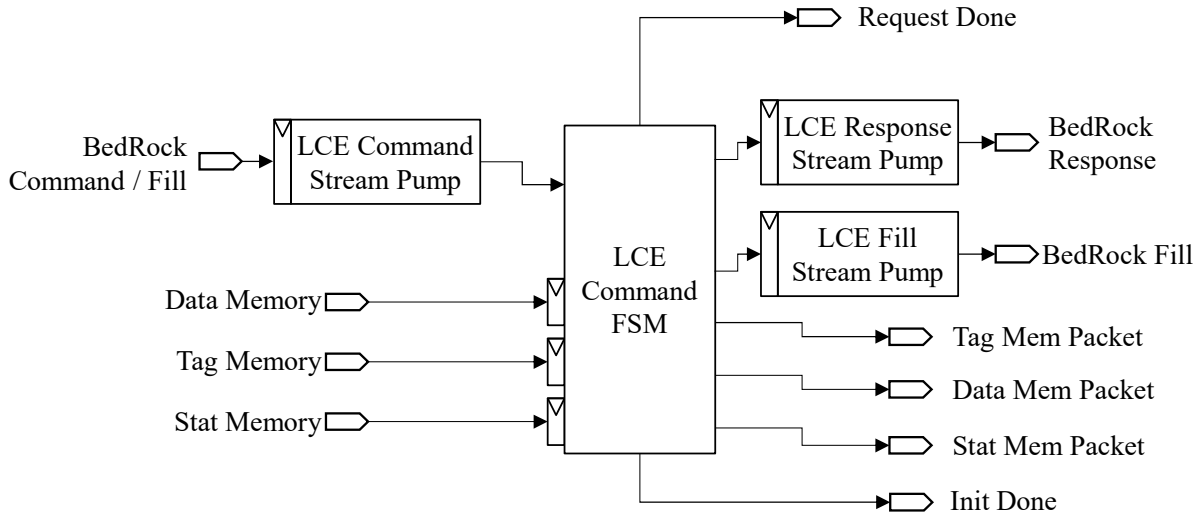


Figure 4.5: BP-BedRock LCE Command Block Diagram

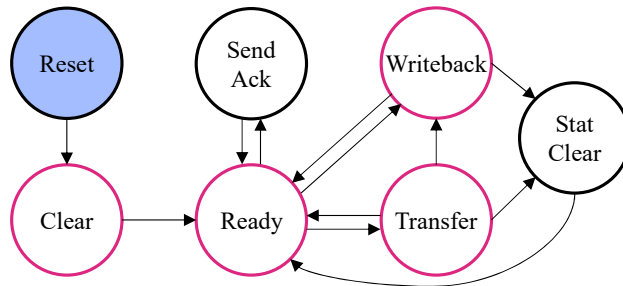


Figure 4.6: BP-BedRock LCE Command State Machine

request in the Ready state and then both receiving the valid metadata and sending the outbound coherence request in the Send Request state in the same cycle. Thus, the extra cycle of occupancy is a consequence of the BP-BedRock L1 cache design.

#### 4.2.2 Command Processing

The BP-BedRock LCE Command logic is responsible for processing all BedRock Command and Fill network messages arriving at the LCE. Figure 4.5 depicts the organization of the LCE Command module implementation. This module includes the LCE Command state machine, stream pumps for sending BP-BedRock Response and Fill messages, a stream pump for receiving Command and Fill messages, and signals that implement the cache fill interfaces with the associated BlackParrot L1 cache.

The BP-BedRock LCE Command state machine is a multi-cycle state machine responsible for processing all BedRock Command network messages arriving at the LCE. Figure 4.6 shows the states and possible state transitions in the command FSM. At system startup, the command FSM first clears the cache's tag and stat memories, ensuring that all cache blocks are invalidated, LRU and replacement information is reset, and all dirty bits are cleared. The state machine then transitions to its ready state and waits for BedRock Command and Fill messages from the CCE or other LCEs. The command state machine is more complex than the request state machine, due to the variety of command messages carried on the BedRock Command network. There are three broad command

message classes that are processed by the state machine.

The first class of messages resolves coherence miss requests previously issued by the request FSM. These messages consume cache block or word data and respond with coherence acknowledgment messages to the CCE.

The second class of message is responsible for coherence protocol management, such as updating the state of a cache block currently present in the cache, initiating writebacks of dirty cache blocks, or performing cache to cache block transfers. Whether any or all of these actions occurs is determined by the command arriving at the LCE, however the state update always happens first, followed by the transfer, and lastly, the writeback. Processing these compound commands is handled atomically by the LCE, and performing the state update first ensures that any future accesses to the target cache block performed by the cache are serialized with the command.

The third class of messages resolves previously issued uncached load and store requests. These commands are processed exclusively in the Ready state, but may take multiple cycles to process. The arrival of either type of command results in the command module raising a request completion signal to the request module, which maintains the credit-based flow control logic.

## Command Occupancy

[Table 4.2](#) details the no-contention state machine occupancy, in cycles, to process BedRock command and fill messages. All arriving commands and data are buffered by the command stream pump. The command state machine begins processing commands as soon as the stream pump output is valid. The state machine is ready to process the next command immediately following completion of the previous command.

In general, all commands have a base cost of one cycle coming from initial processing in the Ready state. Sending a coherence acknowledgment or a null writeback response requires an additional cycle. Sending a cache to cache transfer on the fill network requires  $N$  cycles, as does consuming incoming data from a data command or fill network message. The value of  $N$  is equal to the cache block width divided by the cache fill width and is the number of message beats required to transmit a complete cache block. A few commands require a final cycle to update the cache's stat memory, which tracks whether a cache block is clean or dirty.

The Sync command is used at system startup by the CCE to confirm that all LCEs are ready to execute the coherence protocol. The LCE increments a sync counter when the command is received and then responds with a Sync Ack response message. Processing a Sync command takes a single cycle. The Set Clear command invalidates all cache blocks in a single cache set, which is specified by the command address, and has an occupancy of one cycle. The state machine issues set clear operations to both the tag and stat memories, but sends no response to the CCE. The Set Clear command is currently unused by the BP-BedRock coherence protocols.

Set State and Set State & Wakeup commands modify the coherence state of a cache block and have a base cost of one cycle to write the tag memory. Set State & Wakeup requires a second cycle to send the coherence acknowledgment response message.

Data, Transfer, and Set State & Transfer commands all require one plus  $N$  cycles to process and send responses. Data commands require  $N$  cycles to consume the arriving cache block data and write it to the cache before sending a coherence acknowledgment message to the CCE. Transfer and Set State & Transfer commands require one cycle to read the cache's data memory and write

Message	Occupancy (cycles)	Description
Sync	1	Increment sync received counter, send sync ack response
Set Clear	1	Invalidate all blocks in cache set specified by address
Set State	1	Write state to tag memory
Set State & Wakeup	2	Write state to tag memory and send coherence ack response
Writeback (clean)	2	Read stat memory, send null writeback response
Writeback (dirty)	$2 + N$	Read stat memory, read data memory, and send writeback response
Set State & Writeback (clean)	2	Write tag to tag memory, read stat memory, and send null writeback response
Set State & Writeback (dirty)	$2 + N$	Read stat memory and write state to tag memory, read data memory, and send writeback response
Invalidate	1	Invalidate block by writing state I to tag memory
Data	$1 + N$	Write tag and coherence state to tag memory, data to data memory, signal request complete, and send coherence ack response
Transfer	$1 + N$	Read data memory and send fill data message to another LCE
Set State & Transfer	$1 + N$	Write state to tag memory, read data memory, and send fill data message to another LCE
Set State & Transfer & Writeback (clean)	$2 + N$	Write state to tag memory, read data memory, send fill data message to another LCE, and send null writeback response
Set State & Transfer & Writeback (dirty)	$2 + (2 * N)$	Write state to tag memory, read data memory, send fill data message to another LCE, read stat and data memory, and send writeback response
Uncached Data	1	send data to cache and request complete to request FSM
Uncached Store Done	1	sink command and send request complete to request FSM

Table 4.2: BP-BedRock LCE Command State Machine Occupancy

the cache’s tag memory, if needed, plus  $N$  cycles to transfer the cache block data on the outbound fill network via a stream pump.

The uncached commands finalize uncached load and store requests. Both commands have an occupancy of one cycle in the best case. Uncached Store Done commands inform the LCE that the a previously issued uncached store request has been committed to memory, and require a single

cycle to process and send a request completion signal to the request state machine. Uncached data commands provide uncached load data to the cache alongside sending a request completion signal to the request state machine.

Writeback commands take either two or two plus  $N$  cycles, depending on whether the cache block is clean or dirty, respectively. One cycle is required to read the cache's stat and data memories. If the block is clean, a single cycle is then required to send the null writeback response. A dirty block requires  $N$  cycles to send the writeback of the block plus an additional cycle to update the cache's stat memory.

The remaining commands are effectively combinations of their components. Their occupancies can be computed using the general rules above and are shown in the table. These commands perform a combination of modifying the cache block state, sending a cache to cache transfer, and writing back a cache block to the CCE or sending a null writeback response. The order of operations matches the names of the commands, for example Set State & Transfer & Writeback commands first update the state of the target cache block before performing a cache to cache transfer and lastly performing a writeback, whether a null or dirty writeback.

### 4.2.3 Address Alignment

The BP-BedRock LCE assumes that addresses and data are aligned, but the alignment requirements depend on the interface and message type. All data sent or received by the LCE is sent with little-endian ordering where the least significant byte of the load or store data is placed into the least significant byte of the data message. The data channel width of all four BP-BedRock coherence networks is the same at all LCEs. On the cache request interface, all addresses and data are aligned to the size of the request for both cacheable and uncacheable requests. On the BP-BedRock networks, uncached request and command messages require addresses and data to be naturally aligned to the size of the operation. All other messages are block-based and require that addresses and data are aligned to the coherence network data channel width.

The LCE implements critical-word first behavior and issues the coherence miss request by aligning the cache request address to the data channel width. Arriving Fill and Data commands are expected to return data beginning with the data channel width-aligned sub-block of cache block data that contains the coherence miss request address. In other words, cache block data may be left-rotated to make the data channel width-aligned sub-block containing the requested data the first data beat of the message. The width of the data channel is always at least 64-bits, which guarantees that the cache request data will arrive in the first data beat. If the data channel width is less than the cache block width, more than one data beat is required to send or receive data. Data is transmitted in data channel width sub-blocks, wrapping at the cache block boundary.

## 4.3 Coherence Directory

The BP-BedRock implementation of the BedRock cache coherence protocol [133] relies on a full-duplicate tag directory to track coherence state of every block cached by every cache participating in the coherence system. BP-BedRock includes multiple coherence engine implementations that utilize a single coherence directory implementation. The directory is constructed from multiple directory segments, and there is one directory segment per cache type in the system. BP-BedRock's cache types are instruction, data, and optional coherent accelerator caches. Figure 4.7 shows a block diagram of the coherence directory. All inputs are routed to each directory segment with minimal

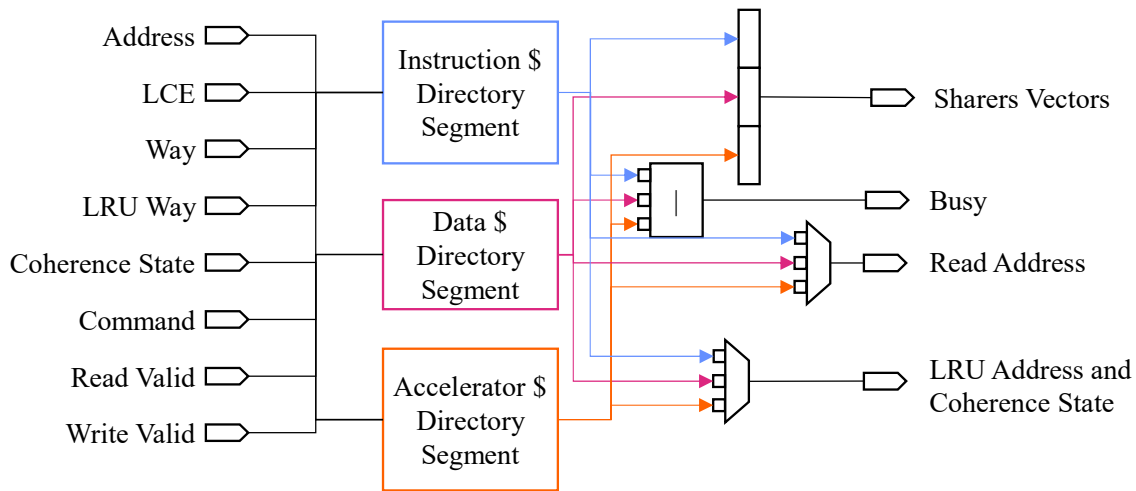


Figure 4.7: BP-BedRock Coherence Directory Architecture

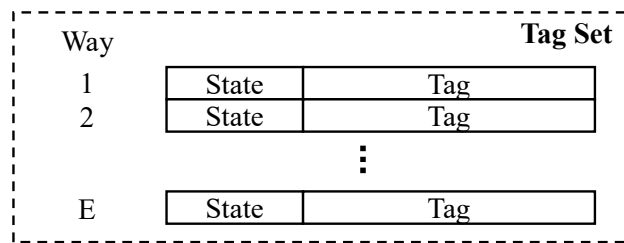


Figure 4.8: BP-BedRock Tag Set

modification, and each segment’s outputs are either combined or multiplexed to the output ports of the coherence directory. If no coherent accelerators are present in the design, the accelerator cache directory segment is not instantiated.

### 4.3.1 Tag Sets and Way Groups

BP-BedRock relies on the concepts of tag sets and way groups to track coherence state and enforce ordering among related coherence transactions. A tag set is the collection of address tag and coherence state for each cache block (way) within a single cache set of a single cache. All of the tag sets in the system are grouped into way groups that provide coherence transaction ordering for related addresses.

#### Tracking State - Tag Sets

The coherence state of every block cached in the system is tracked using the concept of a tag set, which is depicted in Figure 4.8. A tag set is simply the collection of address tag and coherence state for each cache block (way) within a single cache set. The pair of address tag and coherence state is called a Tag Set Entry. The cache controller (LCE) has one tag set per cache set in the cache it manages, and typical implementations integrate the tracking of coherence state into the existing address tag metadata associated with each cache block. The coherence directory tracks all of the tag sets for every cache set at each cache controller in the coherence system. The directory’s collection of tag sets comprises the full-duplicate tag directory.

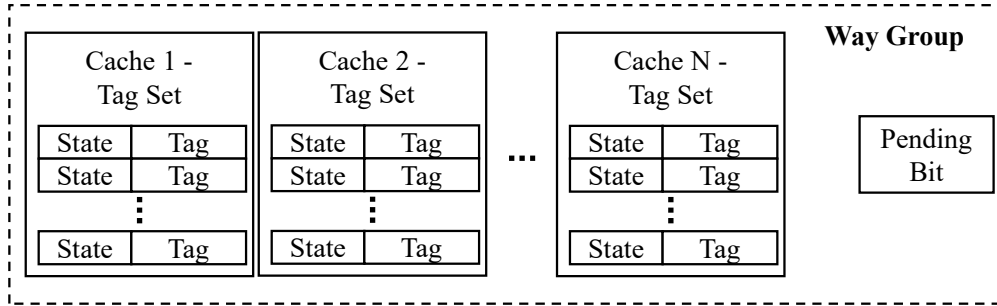


Figure 4.9: BP-BedRock Way Group

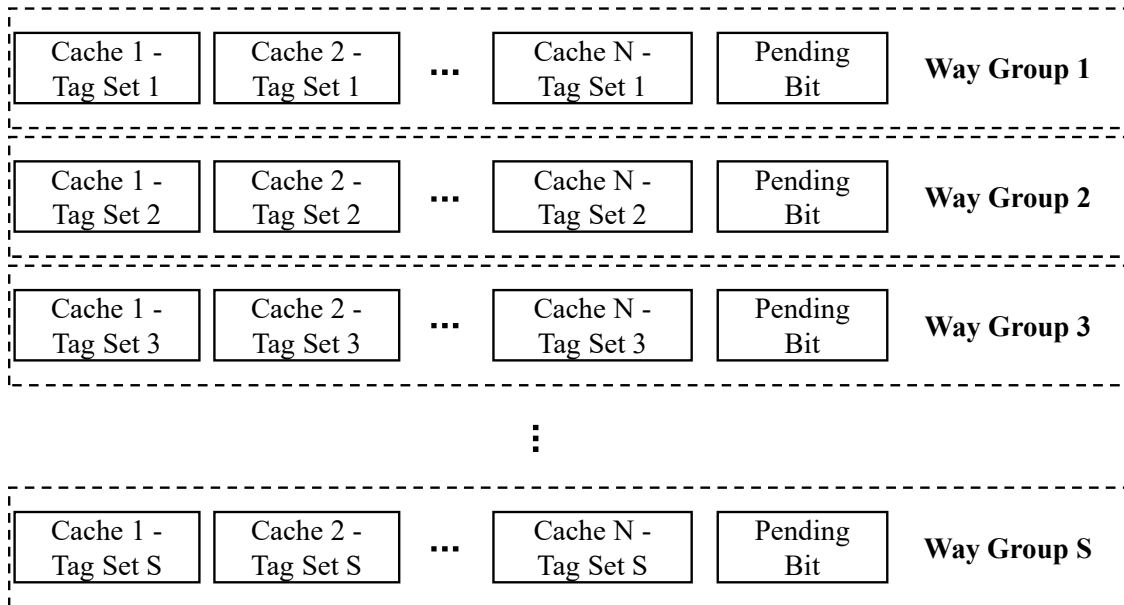


Figure 4.10: BP-BedRock Way Groups

At all times, the tag sets tracked at the coherence directory are considered to be the *golden* copies of the tag sets, which hold the current state of the coherence system across all cached blocks. The directory updates its tag sets during request processing, primarily when sending commands that change the coherence state of blocks at the cache controllers<sup>1</sup>. In contrast to the directory, the cache controllers maintain *shadow* copies of the tag sets that are read-only by the cache controller<sup>2</sup>. The cache controller tag sets are updated by coherence commands received by the controller.

### Ordering Transactions - Way Groups

Figure 4.9 depicts the contents of a way group, which contains one tag set from every cache controller in the coherence system and a Pending Bit. In a BP-BedRock system where every cache controller has the same organization and there are S sets per cache, there are S way groups at the coherence directory with way group X including tag set X from every cache controller. In other words, a cache

<sup>1</sup>Since the BP-BedRock networks guarantee message delivery, the state updates at the directory occur when the directory sends coherence commands

<sup>2</sup>The sole exception to this read-only property is a silent upgrade from E to M to record that a write occurred and a cache block has become dirty.

Virtual Address	Virtual Tag	Page Offset	
Physical Address	Physical Tag	Page Offset	
Cache Address	Physical Tag	Set Index	Block Offset
Way Group Indexing	Physical Tag	Way Group Bits	Block Offset

Figure 4.11: BP-BedRock Address Breakdown

block that maps to cache set X (equivalently, tag set X), is a member of way group X. [Figure 4.10](#) shows the way groups of a canonical system with N caches, S sets per cache, and S way groups.

The pending bit in each way group is used to enforce transaction ordering for requests that target the same way group. This bit is set when the coherence directory begins processing a coherence request targeting a cache block belonging to the associated way group and is cleared when the coherence acknowledgment (CohAck) message for the transaction is received by the directory. Each way group allows for a single active coherence transaction at a time. Any newly arriving request at the coherence directory must check the pending bit of the target way group and stall if the bit is set. Coherence transactions targeting separate way groups are, by definition, independent, and may be processed concurrently because all cache blocks that map to the same cache set are a member of the same way group. Thus requests to a single way group have no possibility of causing any coherence state change to a block in any other way group.

### Mapping Addresses to Way Groups

[Figure 4.11](#) shows how addresses are deconstructed at various stages of a memory access in BP-BedRock. A program issues a virtual address, which contains a tag and page offset. This address is translated to a Physical Address containing a physical tag and a page offset that is identical to the virtual address' page offset. The cache is accessed by further dividing the page offset field into set index and block offset fields. In the event of a cache miss, the LCE issues a miss request containing the physical address to the CCE that is responsible for the address.

A subset of the set index bits, called the way group bits with width  $\log_2(\text{waygroups})$ , is used as the input to a hash module that maps an address to a single way group. The hash module implements a semi-generic hash bank function that takes an address and constant number of banks as inputs and outputs a bank and index. Hash bank functions are commonly used to distribute addresses across cache banks, but in BP-BedRock one is used to spread addresses across CCEs. In BP-BedRock, the number of banks is the number of CCEs and the input address is the way group bits. The hash function then provides the ID of the CCE responsible for managing coherence for the address as the bank output. The index output provides a CCE-local index for the way group, which is used by the CCE but unused by the LCE. The hash function ensures that way groups are spread evenly among the CCEs, and the number of way groups managed by any given CCE will differ by at most one from the number of way groups managed by all other CCEs.

### Number of Way Groups

Every physical address maps to exactly one way group that is managed by exactly one CCE. The total number of way groups in a BP-BedRock system is equal to the *minimum* number of

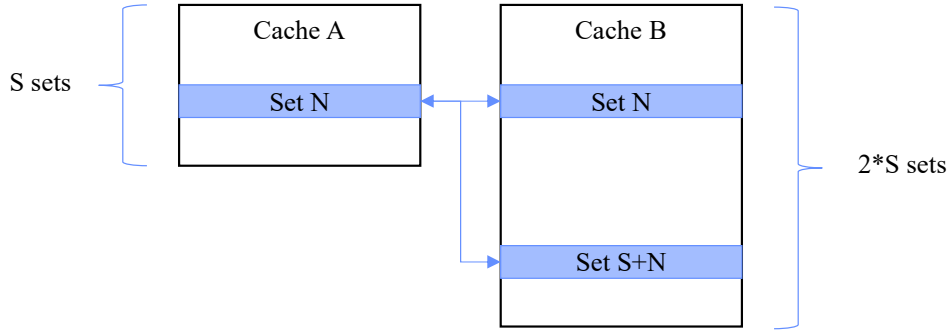


Figure 4.12: Mapping Cache Blocks to Cache Sets

Property	Value
Tag Set Entry Width	$CoherenceStateWidth + AddressTagWidth$
Tag Set Width	$TagSetEntryWidth * CacheAssociativity$
Tag Sets Per Row	2
Tag Sets Per CCE	$\lceil TagSetsPerCache / NumCCE \rceil$
Rows Per Set	$\lceil NumCaches / TagSetsPerRow \rceil$
SRAM Rows	$RowsPerSet * TagSetsPerCCE$
SRAM Size	$TagSetWidth * TagSetsPerRow * SRAMRows$
Entry Read Latency	2
Way Group Read Latency	$RowsPerSet + 1$

Table 4.3: BP-BedRock Directory Segment Properties

cache sets across all cache types participating in coherence. There are three types of caches that participate in coherence: L1 instruction and data caches attached to each BlackParrot core and coherent accelerator caches. Addresses are related if they may map to the same cache block in *any* cache participating in the coherence system.

Figure 4.12 illustrates how cache blocks in two caches with different organizations may be related. Cache A has S sets and Cache B has 2\*S sets. A cache block that maps to set N in Cache A may map to either set N or S+N in Cache B. Conversely, a block that maps to either set N or S+N in Cache B will map to set N in Cache A. Therefore, the collection of related cache blocks (equivalently, addresses) in Cache A and B is the collection of blocks that map to set N in Cache A. Therefore, the number of way groups in BP-BedRock is computed as the *minimum* number of cache sets across all cache organizations in the coherence system<sup>3</sup>.

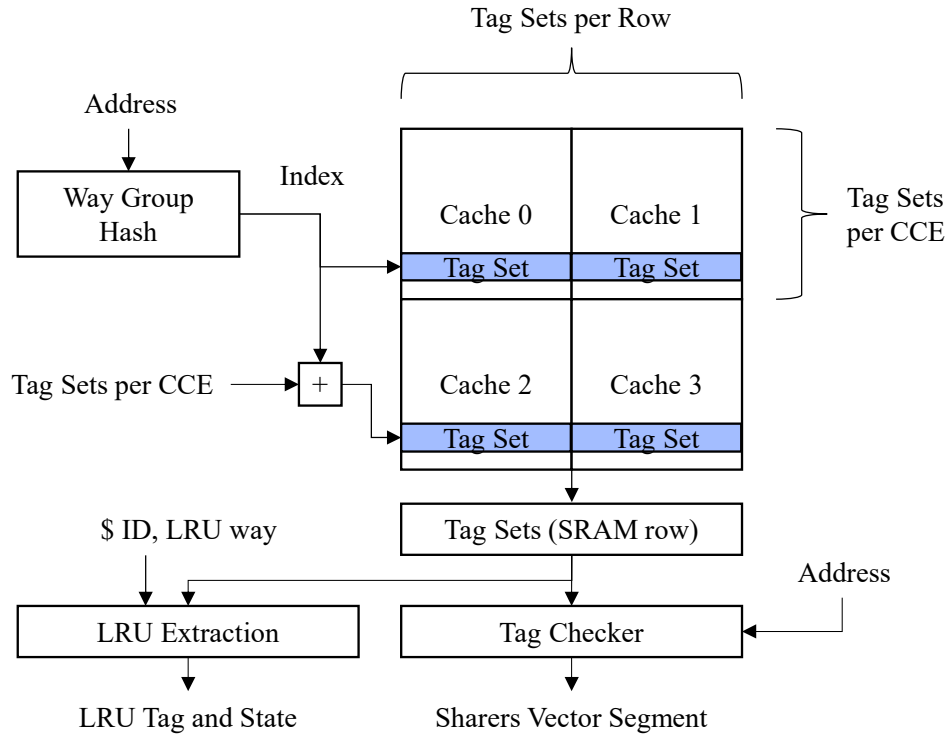


Figure 4.13: BP-BedRock Coherence Directory Segment

## 4.3.2 Coherence Directory Segment Architecture

### Directory Segment Storage

Figure 4.13 shows the organization of a BP-BedRock directory segment and Table 4.3 describes the properties of a segment. Each segment stores a subset of all tag sets for all caches of a single type. The Tag Sets of all caches are spread evenly across the CCEs, and each directory segment allocates enough storage for  $TagSetsPerCCE$  sets for each cache it tracks. The tag sets of all caches tracked are stored as shown in Figure 4.13. The tag sets of a single cache stored in sequential rows, and each row stores tag sets of a single cache set from one or more caches. If the number of tag sets per row is less than the number of caches being tracked by the directory segment, additional blocks of  $TagSetsPerCCE$  rows are added to the directory to track all caches. The directory segment SRAM is a single-ported synchronous read-write memory.

The number of tag sets per row is a parameter of the directory segment, but it must be a power-of-two, which greatly simplifies the directory lookup logic. Prior physical design analysis has shown that a value of two tag sets per row is PPA-efficient for BP-BedRock. If the tag sets per row is not an even divisor of the total number of caches tracked by the segment, the last group of directory rows will not be fully utilized. For example, if the total number of caches tracked by the segment shown in Figure 4.13 was only three, the section of directory rows outlined by the Cache 3 label would be unused. In this case, the selection of two tag sets per row minimizes unused storage space in the directory SRAM, and in the worst case the unused space is exactly the amount required to track a single cache. The location of a cache’s tag set is easily computed using the cache’s (LCE’s)

<sup>3</sup>Note that the number of sets in any cache must be a power-of-two, and there is a power-of-two relationship between the number of cache sets in any two caches.

	Cache 0	Cache 1	Cache 2	Cache 3
Sharers Hits	0	1	0	1
Sharers Ways	-	2	-	6
Sharers States	-	S	-	S

Figure 4.14: BP-BedRock Sharers Vectors

ID bits. The least significant bits determine the cache’s position within a row, and the remaining bits index a lookup table that provides the row within the directory memory. The lookup table is computed at compilation and provides fast-access with minimal hardware overhead.

### Directory Operations and Access

A small FSM controls each directory segment. Each segment supports reading a single tag set entry and reading all tag sets from all caches for a single cache set. Reading the tag sets across all caches is also called a way group read. Supported write operations are clearing an entire physical SRAM row, writing the coherence state to a single tag set entry, and writing the tag and coherence state to a single tag set entry.

The directory segment organization provides single cycle writes and multiple cycle reads. Write operations are immediately processed and initiated to the directory memory by the FSM, and a new write can be processed every cycle. Reading a single tag set entry requires two cycles. The read address is computed and presented to the directory memory in the first cycle, and the memory produces the read data in the second cycle, from which the requested tag set entry is extracted and output. Way group reads require two or more cycles, depending on the number of caches being tracked by the segment, and generate the LRU information and Sharers Vectors as outputs. A way group read is initialized by the FSM in the cycle that it receives the read command, and valid read data emerges from the memory beginning in the second cycle. As read data emerges, it is sent to both the LRU Extraction and Tag Checker modules for processing. The directory output becomes valid one cycle after the last read data emerges from the directory memory, and is valid for at least one cycle and until the next read or write operation occurs. The total latency of a way group read is equal to the number of *RowsPerSet* + 1.

### Tag Checker and Sharers Vectors

The Tag Checker module processes directory rows during way group reads, and produces the Sharers Vectors. The Sharers Vectors are a collection of three vector outputs containing a cache hit bit, coherence state, and cache way for each cache tracked by the segment. As discussed above, each directory row contains a full tag set from one or more caches. The tag checker examines each tag set and determines if the cache block containing the directory read address is present in any tag set entry within the tag set. If a matching block is found, the tag checker sets the cache hit bit for that cache and outputs the cache way within the tag set that the hit occurred in and the currently recorded coherence state of the matching block. [Figure 4.14](#) depicts an example Sharers Vectors output for the directory segment of [Figure 4.13](#), where a read to address A found the block containing A cached in a valid coherence state in caches 0 and 2. Cache 0 has the block in way 6

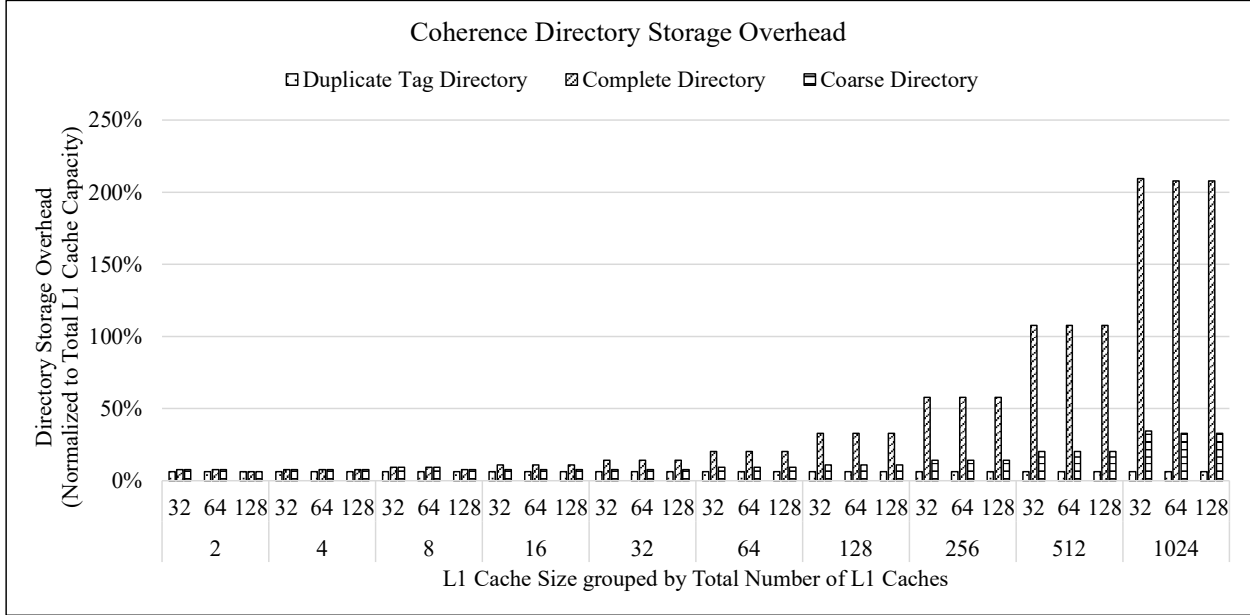


Figure 4.15: Coherence Directory Storage Overhead Comparison

and state S, and cache 2 has the block in way 2 and state S.

### LRU Extraction

The LRU extraction module processes directory rows during way group reads, and extracts the tag set entry at the LRU way for the specified LCE. If the directory segment requires multiple rows to store all cache’s tag sets for a single cache set, the LRU Extraction module outputs the LRU information only for the row containing the requesting LCE’s tag set. The module determines when to output valid information using the cache (LCE) ID and a row count provided by the directory.

### 4.3.3 Coherence Directory Storage Overhead

BP-BedRock utilizes a standalone duplicate tag coherence directory, but this is not the only choice of directory organization that could have been made. Here, BP-BedRock is compared to standalone complete [96] and coarse [130] directories to understand how the coherence storage directory overheads scale as the size of the system scales.

The analysis assumes 8-way associative L1 caches with 64-byte cache blocks, which are the defaults for BP-BedRock, with private instruction and data caches per core. The system uses 28-bit physical address tags and 3-bit coherence states. The number of caches is swept from 2 to 1024 by powers of two and L1 cache size is varied from 32 KiB, to 64 KiB, to 128 KiB. BP-BedRock’s duplicate tag directory stores the cache block tag and coherence state bits for every cache block in every L1 cache in the system. A standalone complete directory must store the cache block tag, coherence state, and owner ID bits in addition to a complete sharers bit vector for every cache block. The size of the sharers vector scales linearly with the number of caches in the system as each bit represents the presence of the cache block in a single cache. The coarse directory requires similar information as the complete directory per entry, however the sharers vector is encoded as one bit per N caches, where the bit is set if any of the corresponding N caches contains the block. In this analysis, a

coarse vector bit can represent eight caches at most, i.e., there is an 8:1 encoding of sharers to bits.

A directory's storage overhead, assuming coherence is maintained across the L1 caches in the design using a standalone directory design, can be computed as

$$Overhead = \frac{\lceil (\frac{Directory\ Bits}{8}) \rceil * Total\ L1\ Cache\ Blocks}{Total\ L1\ Cache\ Capacity} \quad (4.1)$$

where *Directory Bits* is the number of bits required per directory entry as determined by the type of directory employed. Equation 4.2, Equation 4.3, and Equation 4.4 list the formulae for computing the number of directory bits for a duplicate tag, complete, and coarse directory, respectively.

$$Directory\ Bits = Tag\ Bits + State\ Bits \quad (4.2)$$

$$Directory\ Bits = Tag\ Bits + State\ Bits + Owner\ Bits + Sharers\ Vector\ Bits \quad (4.3)$$

$$Directory\ Bits = Tag\ Bits + State\ Bits + Owner\ Bits + Coarse\ Vector\ Bits \quad (4.4)$$

Figure 4.15 and Table 4.4 show that BP-BedRock's duplicate tag directories have a constant storage overhead of 6.25%, which is less than both the complete and coarse directories. The coarse directory is able to achieve fairly low storage overheads up to about 64 caches. However, with larger numbers of caches, the size of the coarse sharers vector continues to grow as cache counts increase since each bit represents a maximum of eight caches. This overhead can be lessened by allowing each bit to represent a greater number of caches, however this coarsens the directory's sharers knowledge and results in more coherence messages to manage the coherence state of a block, many of which may be unnecessary when a block is cached by one or a small number of caches covered by each bit. The complete directory's overhead is modest through 16 caches, but becomes excessive at larger cache counts as the number of bits per sharers vector grows linearly with the cache count.

The constant storage overhead of BP-BedRock's duplicate tag directory is greatly beneficial for the physical design of BP-BedRock, where a slice of the coherence directory is instantiated on each multicore tile and the multicore is constructed by instantiating tiles in a 2D mesh. The constant overhead results in a fixed directory size per tile, regardless of core count, which enables the use of a hierarchical, tile-based backend design flow for ASIC implementations.

Caches	Cache Size	BP-BedRock	Complete	Coarse (8:1)
2	32 KiB	6.25%	7.81%	7.81%
	64 KiB	6.25%	7.81%	7.81%
	128 KiB	6.25%	6.25%	6.25%
4	32 KiB	6.25%	7.81%	7.81%
	64 KiB	6.25%	7.81%	7.81%
	128 KiB	6.25%	7.81%	7.81%
8	32 KiB	6.25%	9.38%	9.38%
	64 KiB	6.25%	9.38%	9.38%
	128 KiB	6.25%	7.81%	7.81%
16	32 KiB	6.25%	10.94%	7.81%
	64 KiB	6.25%	10.94%	7.81%
	128 KiB	6.25%	10.94%	7.81%
32	32 KiB	6.25%	14.06%	7.81%
	64 KiB	6.25%	14.06%	7.81%
	128 KiB	6.25%	14.06%	7.81%
64	32 KiB	6.25%	20.31%	9.38%
	64 KiB	6.25%	20.31%	9.38%
	128 KiB	6.25%	20.31%	9.38%
128	32 KiB	6.25%	32.81%	10.94%
	64 KiB	6.25%	32.81%	10.94%
	128 KiB	6.25%	32.81%	10.94%
256	32 KiB	6.25%	57.81%	14.06%
	64 KiB	6.25%	57.81%	14.06%
	128 KiB	6.25%	57.81%	14.06%
512	32 KiB	6.25%	107.81%	20.31%
	64 KiB	6.25%	107.81%	20.31%
	128 KiB	6.25%	107.81%	20.31%
1024	32 KiB	6.25%	209.38%	34.38%
	64 KiB	6.25%	207.81%	32.81%
	128 KiB	6.25%	207.81%	32.81%

Table 4.4: Coherence Directory Storage Overhead Comparison

#### 4.4 Fixed-Function CCE (FSM CCE)

The BP-BedRock Fixed-Function CCE (FSM CCE) is a hardware-based finite state machine (FSM) implementation of the BedRock Cache Coherence Engine (CCE). The FSM CCE implements the BedRock MOESIF cache coherence protocol with full support for coherent uncacheable loads and stores to cacheable memory and uncacheable access to uncacheable memory. The FSM CCE is the default coherence engine employed by BP-BedRock. [Figure 4.16](#) shows a block diagram of the FSM CCE. The FSM CCE has an LCE Request state machine and Memory Response state machine that work together to execute the BedRock coherence protocol. The CCE includes Speculative Bits to

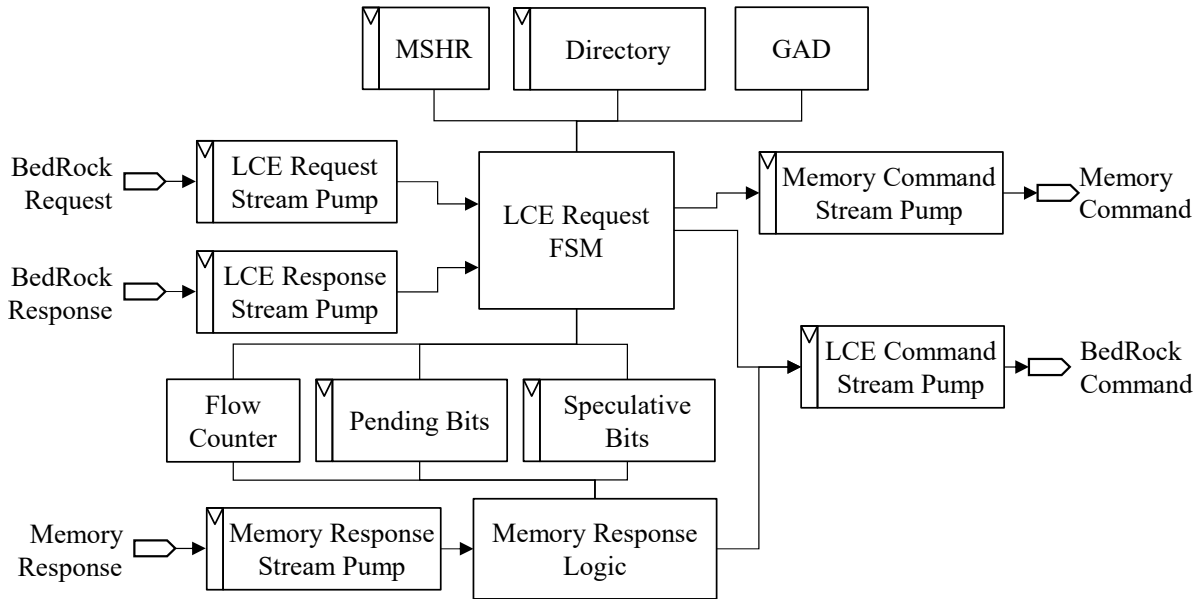


Figure 4.16: BP-Bedrock FSM CCE Block Diagram

track speculative memory reads issued during request processing, Pending Bits to enforce coherence transaction ordering for each way group, and a Flow Counter to provide network flow control on the memory network. The LCE Request state machine instantiates the BP-BedRock coherence directory and a GAD module that processes the output of the coherence directory for use by the state machine logic. It also includes a Miss Status Handling Register (MSHR) that accumulates state during request processing. The remainder of this section describes these modules in detail before describing the functionality of the two state machines.

In this section, the terms cache and LCE are used interchangeably to reference a pair of LCE and attached cache. Strictly speaking, the cache processes requests from the BP-BedRock cores (or coherent accelerators) and issues miss requests to the LCE, while the LCE participates in the coherence protocol and maintains coherence for the cache by manipulating its state. Practically speaking, from the point of view of the CCE the LCE and its attached cache are a single entity<sup>4</sup>.

#### 4.4.1 GAD (Generate Auxiliary Directory Information)

The BP-BedRock coherence protocol implementation enforces cache coherence for all requests that target cacheable memory. As the LCE Request state machine processes a request to cacheable memory it first reads the coherence directory to determine the state of the target cache block. In order to facilitate efficient control flow in the request FSM, the directory first processes the tags and coherence state stored in its memory into the Sharers Vectors and LRU Information, as explained in Section 4.3. This information is then further processed by the Generate Auxiliary Directory Information, or GAD, module for use by the request FSM.

The GAD module consumes the Sharers Vectors and LRU Information and outputs a set of flag bits that can be used for efficient control flow decisions; the owner, location, and coherence state of the target cache block, if an owner exists; and the cache way of the target block within the

<sup>4</sup>A non-BP-BedRock implementation of the BedRock coherence protocol may implement the cache and LCE as a single module.

Output	Description
Replacement Flag	Cache block in replacement way of requesting LCE needs to be evicted to make room for requested block
Upgrade Flag	Cache block exists in a read-only coherence state at requesting LCE
Cached Shared Flag	Block is cached in S in at least one other LCE
Cached Exclusive Flag	Block is cached in E in at least one other LCE
Cached Modified Flag	Block is cached in M in at least one other LCE
Cached Owned Flag	Block is cached in O in at least one other LCE
Cached Forward Flag	Block is cached in F in at least one other LCE
Owner LCE	LCE ID of cache block owner
Owner Way	Cache way of block at owner LCE
Owner Coh State	Coherence state of block at owner LCE
Req Addr Way	Cache way of block in requesting LCE

Table 4.5: BP-BedRock GAD Outputs

requesting LCE’s cache if it is already cached in a valid coherence state. The GAD module takes a single cycle to execute, but greatly reduces the complexity of control flow decisions in the request FSM.

Table 4.5 describes the outputs of the GAD module. There are seven single bit output flags that are used by the request FSM to make efficient control flow decisions when determining the specific actions required to maintain coherence. Five of these flags (Cache \* Flag) are set if the requested cache block is cached in the specified MOESIF coherence state in *any* cache other than the requesting cache. The Upgrade Flag is set if the requesting cache already has a valid copy of the requested cache block in a read-only state and the LCE request is a write-miss, indicating the cache needs read-write permissions for the block. The Replacement Flag is set if the replacement (LRU) way provided by the requesting cache is in a valid and possibly dirty state. This flag is also overloaded for uncacheable accesses to mean that the cache block containing the address in the uncacheable request exists in any valid state at the requesting cache block.

The Owner outputs from the GAD module provide the LCE ID, cache way, and coherence state of the requested cache block at the LCE that currently owns the block, if such an LCE exists. In the MOESIF protocol, a block cached in any of the E, M, O, or F states has a specified owner. If a block has an owner, the CCE is able to perform a cache-to-cache transfer of the block rather than performing a memory read of the requested block. Cache-to-cache transfers are often significantly lower latency than memory reads, which improves the overall performance of the BP-BedRock multicore system.

The Req Addr Way specifies the cache way of the target cache block within the requesting LCE’s cache. This is used in combination with the `upgrade_flag` when a cache is requesting write permissions for a block that it has cached in a read-only state. The Req Addr Way is also used for uncached requests when the block must be evicted from the requesting cache.

### 4.4.2 Pending Bits

The Pending Bits track outstanding coherence transactions for each way group managed by the CCE and serialize coherence requests targeting the same way group. There is one pending bit per way group. Each pending bit is implemented as a small counter, and a way group's pending bit is considered set if the counter is non-zero and unset if the counter is zero. When a new coherence request arrives at the CCE, the pending bits are checked and request processing begins only when the pending bit is not set. The pending bits serialize all coherence requests targeting the same way group.

The Pending Bits module implements independent read and write ports. Both ports require an input address that is sent through a hash function to determine the local way group index at the CCE. A write operation increments or decrements the pending bit counter by one, and a clear operation resets the counter to zero. Read operations output a single bit that is set if the counter is non-zero and unset if the counter is zero. Write to read forwarding is supported for concurrent read and writes.

The CCE increments the pending bit when it begins processing a new request targeting a cacheable block of memory and whenever a memory command is issued during request processing. Pending bits are decremented when memory responses are consumed, when coherence acknowledgment responses are received, and when the CCE finishes processing uncached requests to coherent memory. Uncached requests do not generate coherence acknowledgment messages and are considered complete when the CCE sends the load data or store complete command to the LCE.

### 4.4.3 Speculative Bits

The Speculative Bits record information about speculative memory reads issued to memory. When the CCE processes a new coherence request it may issue a speculative memory read of the target cache block in an effort to reduce the total request latency observed by the LCE. There is one Speculative Bits entry per way group. Each entry includes a coherence state, a speculative bit, a squash bit, and a forward-modified bit. At startup, all bits are cleared and the coherence state is set to Invalid.

The CCE sets an entry's speculative bit when it issues a speculative memory read for the way group, and clears the bit at the end of the request processing flow once it has determined the next coherence state and source of the cache block. The speculative memory read message payload contains the ID of the LCE whose request caused the memory read, the cache way the block will occupy, and the CCE's best guess of the final coherence state for the cache block.

When the CCE resolves the state and source of the block it may also set the other three fields of the entry. The squash bit is set if the speculative memory read is not needed to fulfill the request. This happens when the block will be provided by a cache to cache transfer or the requesting LCE already has the block and only needs upgrading coherence permissions. The forward-modified bit and coherence state field are set if the request will be fulfilled with the block read from memory, but the coherence state required differs from the state issued in the payload of the memory message. When the memory response returns and is processed, the CCE will observe the set forward-modified bit and replace the coherence state in the message payload with the coherence state stored in the speculative bits entry. If neither the squash or forward-modified bits are set, the CCE will forward the speculative memory read response to the LCE recorded in the payload as a Data command to fulfill the request.

Field	Source	Description
Msg Type	LCE Request	Request message type
Msg Sub Op	LCE Request	Request message sub-operation
Msg Size	LCE Request	Request message size
LCE ID	LCE Request	Requesting LCE ID
Address	LCE Request	Physical address of request
LRU Way ID	LCE Request	Replacement way from requesting LCE
LRU Address	Directory	Physical address of block in LRU way at requesting LCE
LRU Coh State	Directory	Coherence state of block in LRU way at requesting LCE
Way ID	GAD	Cache way of block in requesting LCE
Owner LCE	GAD	LCE ID of cache block owner
Owner Way	GAD	Cache way of block at owner LCE
Owner Coh State	GAD	Coherence state of block at owner LCE
Flags	Multiple	Control flow flags
Next Coh State	FSM	Next coherence state of requested block

Table 4.6: BP-BedRock MSHR State

#### 4.4.4 Miss Status Handling Register (MSHR)

The FSM CCE contains a Miss Status Handling Register (MSHR) that accumulates information related to the current LCE request. [Table 4.6](#) shows the fields of the MSHR, their source within the FSM CCE, and a brief description of each field. The information stored in the MSHR come from the LCE Request being processed, the coherence directory, the GAD module outputs, and the FSM logic. The MSHR is referenced throughout the FSM CCE's LCE request processing flow. Most fields are self-explanatory, and the rows of the table are ordered from top to bottom in approximately the order that the fields are populated. The first set of fields come from the LCE Request message header and include the requesting LCE, the request address, and the specific request message type and size. The cache way to use for a replacement, if required, is provided by the LRU Way ID field. Most of the remaining fields are generated by reading and processing the directory, indicated by the Directory and GAD sources. These include information about the owner LCE, if one exists, the address and coherence state of the block in the LRU way of the requesting cache, the cache way of the requested block in the requesting cache, and a subset of the control flow flags. The final field of the MSHR stores the next coherence state for the requested block at the requesting LCE.

[Table 4.7](#) describes the control flow flags present in the MSHR. These flags are used to make efficient control flow decisions in the FSM CCE. The first set of flags come directly from the LCE Request message that is being processed. These indicate if the request is a write or read request, cached or uncached, atomic with or without a return value, and whether or not the Non-Exclusive hint bit is set in the request message. The cacheable address flag is derived from the LCE Request message address and is set if the requested address is in the cacheable memory address space. The null writeback flag records whether the last LCE writeback response message was a null writeback or a

Flag	Source	Description
Write Not Read	LCE Request	Write Miss or Uncached Store request message type
Uncached	LCE Request	Uncached request message type
Non Exclusive	LCE Request	Non-Exclusive bit set in LCE Request
Atomic	LCE Request	Atomic operation request message type
Atomic No Return	LCE Request	Atomic no return bit set in request
Cacheable Address	FSM	Request is to a cacheable address
Null Writeback	LCE Response	LCE Response message is a Null Writeback
Pending	FSM	Pending bit was set in last pending bit read
Speculative	FSM	Speculative bit was set in last speculative bits read
Cached Shared	GAD	Block is cached in S in at least one other LCE
Cached Exclusive	GAD	Block is cached in E in at least one other LCE
Cached Modified	GAD	Block is cached in M in at least one other LCE
Cached Owned	GAD	Block is cached in O in at least one other LCE
Cached Forward	GAD	Block is cached in F in at least one other LCE
Replacement	GAD	Cache block in replacement way of requesting LCE needs to be evicted to make room for requested block
Upgrade	GAD	Cache block exists in a read-only coherence state at requesting LCE

Table 4.7: BP-BedRock MSHR Flags

data-carrying writeback. The pending bit is set whenever a pending bit module read occurs, and indicates if the specified way group has an open coherence transaction. The speculative bit is set whenever the speculative bits module is read, and indicates if there is an unresolved speculative memory read outstanding for the specified way group. The remaining flags are generated by the GAD module as explained above in [Subsection 4.4.1](#).

#### 4.4.5 Memory Response Logic

The memory response logic processes BP-BedRock Memory Response messages returning to the CCE from the L2 cache or the I/O devices. Every memory command issued by the CCE results in a single memory response back to the CCE. [Figure 4.17](#) depicts a logical representation of the memory response logic as a three state FSM. In BP-BedRock, this state machine is implemented without any explicit encoding of the three discrete states shown in the figure. Logically, as each memory response arrives at the FSM CCE, it either forwards the message to the appropriate LCE or sinks the response from the memory network. Every memory response with an address in the cacheable memory address space also decrements the pending bit counter of the associated way group when it is consumed by the CCE. Memory responses are divided into speculative and non-speculative responses, as indicated by the speculative bit in the message header payload. This bit is set for all memory response messages generated by speculative memory read commands.

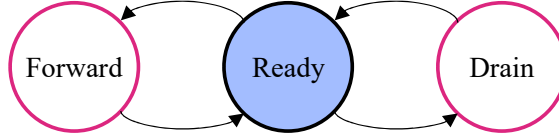


Figure 4.17: BP-Bedrock FSM CCE Memory Response Abstract State Machine

Message	Occupancy (cycles)	Description
Read	$N$	Cache block read data; forward to LCE
Write	1	Cache block writeback complete; sink message
Uncached Read	$N$	Uncached load data; forward to LCE
Uncached Write	1	Uncached store committed to memory; send Uncached Store Done to LCE

Table 4.8: BP-BedRock FSM CCE Memory Response State Machine Occupancy

If the response is speculative, the response logic reads the speculative bits to determine if the LCE Request FSM has completed request processing and resolved the speculation. The response logic stalls until speculation has been resolved, and then processes the response according to the speculative bits entry. As explained in [Subsection 4.4.3](#), there are three outcomes to speculation. The memory response may be squashed because it was not needed, it may be forwarded unmodified to the specified LCE using the coherence state supplied in the response message payload, or it may be forwarded to the specified LCE using the coherence state stored in the speculative bits entry. Squashing a memory response is achieved by draining the entire message from the memory response stream pump and sinking it in the CCE without sending any message to an LCE. Forwarding a memory response sends a BedRock Command message on the outbound command network to the LCE specified in the memory response message’s header payload data.

Non-speculative memory responses are either forwarded directly to the LCE specified in the response message header payload or are sunk at the CCE, depending on the message type. Uncached load (`uc_rd`) and cached block read responses (`rd`) are forwarded directly to the BedRock command network using multi-beat data command messages. Uncached store responses (`uc_wr`) are consumed by the response logic and transformed into a single-beat uncached store done command, which is sent to the LCE that initiated the store operation. Cacheable write (`wr`) responses inform the CCE that a cache block writeback to memory has completed. The memory response logic sinks write responses as they arrive without sending any command messages to an LCE.

### Memory Response FSM Occupancy

[Table 4.8](#) provides the no-contention memory response logic processing occupancies for the supported memory response message types. Write and Uncached Write responses each require a single cycle to process, which includes writing the pending bit and sending a command message, if required. Uncached Read and Read responses each require  $N$  cycles to process. The number of cycles required to send the BedRock command message is determined by the the data width of the BedRock network channels and the cache block size in the coherence system.

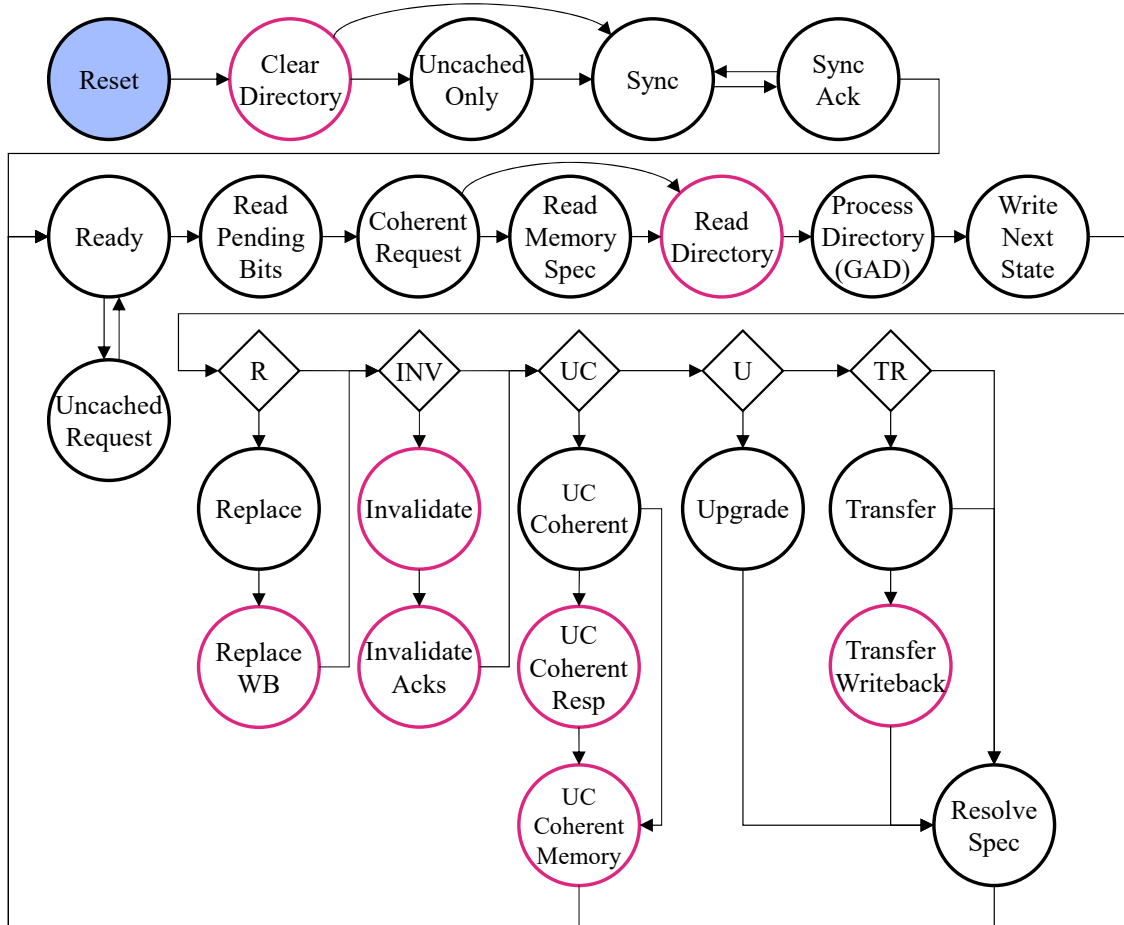


Figure 4.18: BP-Bedrock FSM LCE Request State Machine

#### 4.4.6 LCE Request FSM

The LCE Request FSM processes BP-BedRock LCE Request messages, and is depicted in [Figure 4.18](#). The Ready state, highlighted in blue, is the state machine’s initial state. The CCE processes a single request at a time, and the request state machine runs without interruption. Every request is classified as either coherent or uncacheable based on the request address. All requests that target cacheable memory are coherent requests and invoke the cache coherence protocol. Requests to cacheable memory may be either cacheable or uncacheable, as issued by the LCE. Requests targeting uncacheable memory are limited to uncached load, store, and atomic operations, and are processed outside the coherence protocol.

An uncached request to uncacheable memory is received in the Ready state, which sets the request address, message type, and a few flags in the MSHR. The FSM then moves to the Uncached Request state which issues the uncached access to memory. Uncached stores may require additional cycles to issue message data to memory, which is handled by the Send Uncached Data state. The state machine returns to the Ready state after the memory command has been sent.

Cached and Uncached Requests to cacheable memory participate in the coherence protocol and require the CCE to read the directory and possibly adjust the coherence state of one or more LCEs. All requests to cacheable memory move through an initial set of states that read the

pending bits, optionally issue a speculative memory read, read and process the directory, and update the coherence state of the requested block at the requesting LCE. The CCE first reads the pending bits to check if there is an active coherence transaction for the target way group. Once the previous transaction completes, the state machine consumes the request and increments the target way group’s pending bit to open a new coherence transaction. Cacheable requests then issue a speculative memory read, which reduces total processing latency for requests that will be fulfilled from memory by overlapping the memory read with request processing. All requests next read the coherence directory, process the output using the GAD module, and determine the next state of the targeted block at the requesting LCE. The initial request processing finishes by updating the coherence directory with the block’s next coherence state.

After the initial request processing completes, the request state machine branches to execute only those steps necessary to complete the request and maintain coherence. These decisions are represented by the diamonds in the state machine diagram. Each diamond has a latency of zero cycles and the next state selection occurs as each step completes. All coherent requests may require a cache block replacement and invalidations. Cacheable requests may require replacing the block specified in the LRU Way ID field of the MSHR to make room for the requested block, while uncacheable requests may require evicting the cache block containing the requested address and found in the cache way given by the Way ID field of the MSHR. Both types of requests may require invalidating the target cache block from all non-owner LCEs.

Cacheable requests are resolved by upgrading the coherence permissions of the block at the requesting LCE, initiating a cache to cache transfer of the block from the current owner to the requester, or fulfilling the cache block request from memory. Regardless of the action required, all cacheable requests are finalized in the resolve speculation state, which updates the speculative bits entry for the target way group. The speculative bits entry update communicates the action to take in the memory response state machine when processing the speculative memory read response. After the requesting LCE receives the necessary cache block data and coherence state, it sends a Coherence Acknowledgment response to the CCE. The CCE immediately sinks the coherence acknowledgment message and decrements the target way group’s pending bit. Processing coherence acknowledgments happens outside of the request state machine because

Uncacheable requests to cacheable memory are resolved by first invalidating and possibly writing back the target cache block from the LCE that owns the block, if one exists and if the block may be dirty. The state machine then forwards the dirty writeback to memory, if needed, before issuing the uncached load or store operation to memory.

### **LCE Request FSM Occupancy**

Table 4.9 provides the no-contention, best-case processing occupancy for each state in the request state machine. As discussed in Section 4.3, the coherence directory is organized such that the read latency of a given directory segment is equal to the total number of directory rows required to store the tag sets for all caches plus one cycle to initiate the first read. In BP-BedRock, where two cache’s tag sets are stored per directory row, the directory read latency is equal to the number of cores divided by two plus one cycles. Each directory segment stores the tag sets for a single cache type, and each core has one instruction and data cache. Therefore, there are two directory segments, and each segment tracks exactly  $C$  caches, where  $C$  is the number of cores.

The remaining states that require multiple cycles to execute involve message send and receive operations. An LCE request may require the CCE to invalidate all LCEs with target block in the

State	Occupancy (cycles)	Description
Read Directory	$(C/2) + 1$	One cycle setup, plus one cycle per two cores
Replacement Response	1 or $N$	One cycle for null writeback, $N$ for dirty writeback
Invalidation Commands	$S$	One cycle per Sharer
Invalidation Response	$S$	One cycle per Sharer
Transfer Writeback Response	1 or $N$	One cycle for null writeback, $N$ for dirty writeback
Uncached INV/WB Response	1 or $N$	One cycle for null writeback, $N$ for dirty writeback
Uncached Coherent Memory Command	1 to $N$	One cycle per data beat for store, or one cycle for load
Send Uncached Data	$N - 1, \max$	One cycle per data beat
All other states	1	

Table 4.9: BP-BedRock FSM CCE Request FSM State Machine Occupancy

Shared (S) state, which requires  $S$  cycles to send the invalidations and  $S$  cycles to consume the invalidation acknowledgment responses. If  $S$  is large, it is possible for the first invalidation responses to arrive while the final invalidation commands are being issued, in which case the request CCE is able to perform both a command send and response sink in the same cycle, thereby overlapping invalidation send and receive.

All states that wait for writeback responses from an LCE require either one or  $N$  cycles, where  $N$  is the number of data beats required to transmit the cache block data. Uncached store commands, whether targeting cacheable or uncacheable memory require at most  $N$  cycles to consume the uncached store request and convert it to an uncached memory write message.

States not listed in [Table 4.9](#) require a single cycle to execute under no-contention, best-case conditions. These states collectively perform reads or writes to the pending or speculative bits, issue header-only command or memory messages, or write the coherence directory, which are all single-cycle operations.

[Table 4.10](#) provides the no-contention, best-case processing occupancy for various cacheable LCE requests given an initial coherence state for the target cache block. These occupancies are computed by progressing through the state machine in [Figure 4.18](#) and summing the latency of each state visited. All requests assume that a cache block replacement is not required. The addition of a replacement adds either two or  $1 + N$  cycles to the processing latency for null and dirty writebacks, respectively.

From the request state machine diagram, all requests have a base processing cost of  $8 + (C/2)$  cycles to move from the Ready state through the Write Next State state, which includes reading

Request	LCE State	Directory State	Occupancy (cycles)	Notes
Read	I	I	$8 + (C/2)$	Block from Memory
		S	$8 + (C/2)$	Block from Memory
		E (clean)	$10 + (C/2)$	Transfer and Writeback
		E (dirty)	$9 + (C/2) + N$	Transfer and Writeback
		M, O, F	$9 + (C/2)$	Transfer
Write	I	I	$8 + (C/2)$	Block from Memory
		S	$8 + (C/2) + (2 * S)$	Block from Memory
		E, M	$9 + (C/2)$	Transfer
		O, F	$9 + (C/2) + (2 * S)$	Invalidate and Transfer
Write	S	S	$9 + (C/2) + (2 * (S - 1))$	Invalidate and Upgrade
		O, F	$9 + (C/2) + (2 * (S - 1))$	Invalidate and Upgrade
Write	O, F	O, F	$9 + (C/2) + (2 * S)$	Invalidate and Upgrade

Table 4.10: BP-BedRock FSM CCE Request Occupancy

and processing the coherence directory, and then to resolve the speculative memory read. Read and write requests targeting a cache block in the Invalid state are fulfilled using the block from memory and require no additional cycles. Invalidating all caches in the S state requires a total of  $(2 * S)$  cycles. Issuing a Set State and Wakeup command (STW) to upgrade the cache block from read-only to read-write permissions at the requesting LCE requires a single cycle. The only remaining special case is a write request issued when the block is in the Shared (S) state at the directory and in the Shared state at the requesting LCE. In this case, the requesting LCE is not invalidated, slightly reducing the cost of invalidations.

Applying the formulae from Table 4.10, the no-contention request processing occupancy at the CCE in an eight-core BP-BedRock multicore design is between 12 and 27 cycles. Directory reads require four cycles ( $(C/2) = 4$ ), and there are at most seven sharer caches ( $S \leq 7$ ) that must be invalidated to complete any given transaction. Direct substitution into the derived formulae provide best-case estimates for request processing occupancy.

#### 4.4.7 Memory Consistency Model

BP-BedRock’s coherence protocol belongs to a class of protocols that are called *consistency-agnostic*. These protocols support the implementation of many different memory consistency models on top of the provided coherence protocol that maintains coherence for each shared-memory location. Importantly, cache coherence is maintained for each memory location and defines the semantics and ordering for accesses to a single location or address. Additionally, most consistency-agnostic cache coherence protocols, including BedRock, operate invisibly to the programmer. Memory consistency defines the allowable orderings for memory accesses across all memory locations and is visible to the programmer. Due to the presence of microarchitectural optimizations such as cache write buffers or support for inter-access concurrency, it may be possible for certain memory

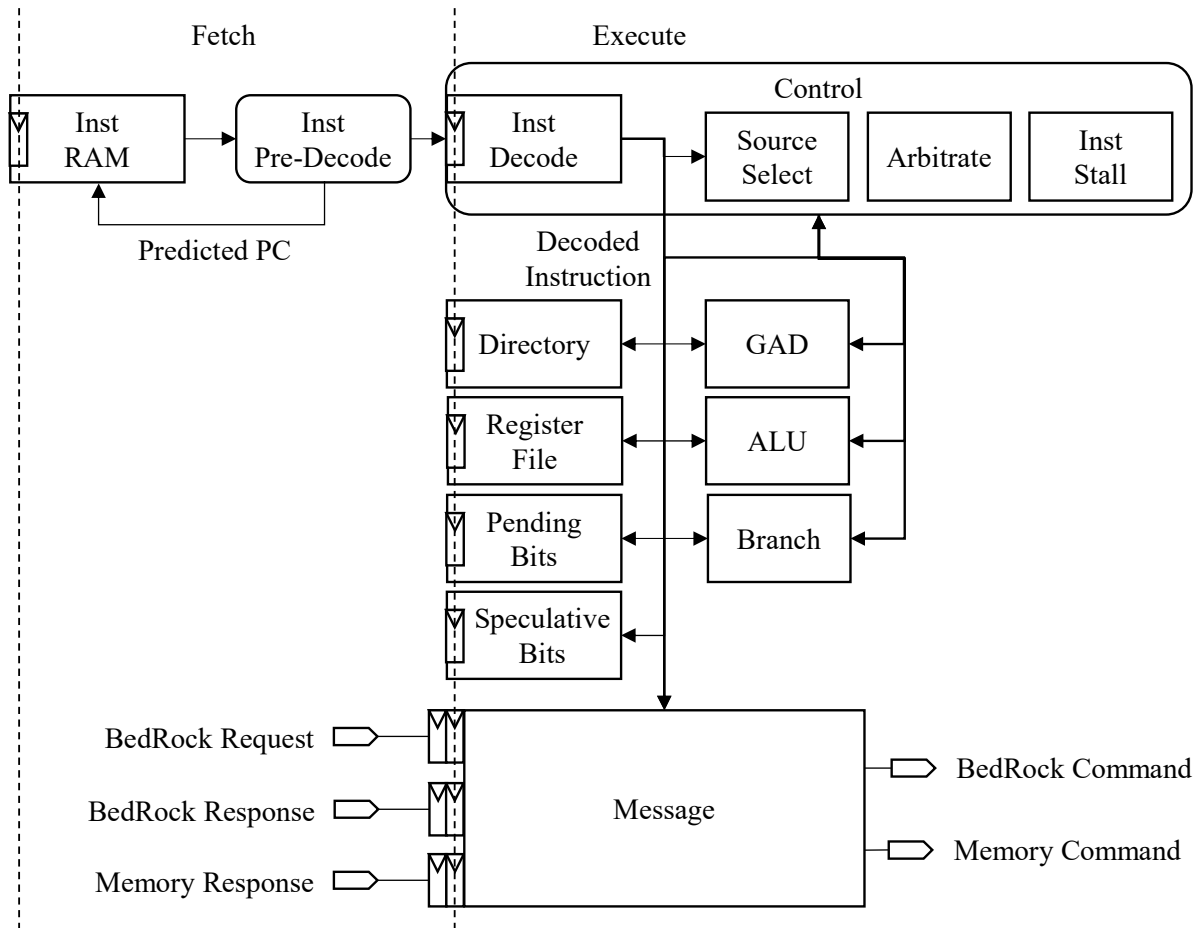


Figure 4.19: BP-BedRock Microcode-Programmable CCE Block Diagram

accesses to be observed in an order that either differs from the given program order or that differs among observers (i.e., caches and cores) in the system.

The current BP-BedRock implementation realizes a memory consistency model called Sequential Consistency (SC). In this model, the execution and memory accesses of each processor core are observed in the order given by the program. Further, the execution of all operations across all processors is simply an interleaving of each processors sequentially consistent execution. All BP-BedRock multicore processors, whether using the FSM CCE described in this section, the microcode-programmable CCE described in the following section, or the hybrid coherence engine described in [Chapter 5](#), implement the SC memory consistency model. Readers are referred to the literature for additional details and formalizations of memory consistency. Nagarajan et al. provide an excellent overview for those with backgrounds in computer architecture [96].

## 4.5 Microcode-Programmable CCE (ucode CCE)

The BP-BedRock microcode-programmable CCE (ucode CCE) is an experimental BedRock cache coherence engine implementation featuring a user-programmable coherence engine. The ucode CCE implements a two-stage fetch-execute pipeline with 64-bit general purpose registers and datapath, specialized coherence protocol processing logic, and a custom instruction set architecture. [Fig-](#)

Figure 4.19 shows a block diagram of the BP-BedRock ucode CCE. The programmable CCE re-uses a number of modules from the FSM CCE, including the Coherence Directory, GAD, Pending Bits, and Speculative Bits that are explained in Section 4.4. The functionality of the ucode CCE attempts to match that of the FSM CCE. The programmable nature of the ucode CCE allows it to execute any variant of the BedRock coherence protocol simply by changing the microcode that it executes. BP-BedRock includes microcode for the MOESIF, MESI, MSI, and EI protocols, along with variations of the MESI and MOESIF protocols that implement the speculative memory fetch behavior of the FSM CCE. This section details the implementation and instruction set of the ucode CCE and provides details on the modules that are unique to its design.

Op	Format	Function	Pseudo-Op
nop	nop	$r0 = r0 + 0$	✓
add	add ra rb rd	$rd = ra + rb$	
addi	addi ra imm rd	$rd = ra + imm$	
inc	inc rd	$rd = rd + 1$	✓
sub	sub ra rb rd	$rd = ra - rb$	
subi	subi ra imm rd	$rd = ra - imm$	
dec	dec rd	$rd = rd - 1$	✓
not	not rd	$rd = !rd$	
lsh	lsh ra rb rd	$rd = ra \ll rb$	
lshi	lshi ra imm rd	$rd = ra \ll imm$	
rsh	rsh ra rb rd	$rd = ra \gg rb$	
rshi	rshi ra imm rd	$rd = ra \gg imm$	
and	and ra rb rd	$rd = ra \& rb$	
or	or ra rb rd	$rd = ra   rb$	
xor	xor ra rb rd	$rd = ra \oplus rb$	
neg	neg rd	$rd = \sim rd$	

Table 4.11: BP-BedRock ucode CCE Base ISA - ALU

Op	Format	Function	Pseudo-Op
bi	bi tgt	$pc = tgt$	✓
beq	beq ra rb tgt [pt]	$pc = tgt$ if $ra == rb$	
bne	bne ra rb tgt [pt]	$pc = tgt$ if $ra != rb$	
blt	blt ra rb tgt [pt]	$pc = tgt$ if $ra < rb$	
bgt	bgt ra rb tgt [pt]	$pc = tgt$ if $ra > rb$	✓
ble	ble ra rb tgt [pt]	$pc = tgt$ if $ra \leq rb$	
bge	bge ra rb tgt [pt]	$pc = tgt$ if $ra \geq rb$	✓
beqi	beqi ra imm tgt [pt]	$pc = tgt$ if $ra == imm$	
bneqi	bneqi ra imm tgt [pt]	$pc = tgt$ if $ra != imm$	
bz	bz ra tgt [pt]	$pc = tgt$ if $ra == 0$	✓
bnz	bnz ra tgt [pt]	$pc = tgt$ if $ra != 0$	✓
bs	bs rspc rb tgt [pt]	$pc = tgt$ if $rspc == rb$	
bss	bss rspca rspcb tgt [pt]	$pc = tgt$ if $rspc_a == rspc_b$	
bsi	bsi rspc imm tgt [pt]	$pc = tgt$ if $rspc == imm$	

Table 4.12: BP-BedRock ucode CCE Base ISA - Branch

Op	Format	Function	Pseudo-Op
mov	mov ra rd	$rd = ra$	
movsg	movsg rspc rd	$rd = rspc$	
movgs	movgs ra rspc	$rspc = ra$	
movfg	movfg flag rd	$rd[0] = flag$	
movgf	movgf ra flag	$flag = ra[0]$	
movpg	movsg param gpr	$gpr = param$	
movgp	movgs gpr param	$param = gpr$	
movi	movi imm rd	$rd = imm$	
movis	movis imm rspc	$rspc = imm$	
movip	movis imm param	$param = imm$	
clm	clm	clear <i>MSHR</i>	
clf	clf	clear <i>MSHR.flags</i>	✓
ldflags	ldflags ra	$MSHR.flags = ra[0+ : num\_flags]$	✓
ldflagsi	ldflagsi imm	$MSHR.flags = imm[0+ : num\_flags]$	✓

Table 4.13: BP-BedRock ucode CCE Base ISA - Data Movement

Op	Format	Function
sf	sf flag	$flag = 1$
sfz	sfz flag	$flag = 0$
andf, orf	op flag1 flag2 gpr	$rd = flag1 \text{ op } flag2$
nandf, notf	op flag1 flag2 gpr	$rd = flag1 \text{ op } flag2$
notf	notf flag gpr	$rd = \sim flag$
bf	bf tgt flag [flag...] [pt]	$pc = tgt$ if all specified flags == 1
bfnof	bfnof tgt flag [flag...] [pt]	$pc = tgt$ if all specified flags == 0
bfz	bfz tgt flag [flag...] [pt]	$pc = tgt$ if any specified flag == 1
bfnz	bfnz tgt flag [flag...] [pt]	$pc = tgt$ if any specified flag == 0

Table 4.14: BP-BedRock ucode CCE Coherence ISA - Flag

Op	Format	Function
rdp	rdp addr=a	$pf = pending\_bits[addr]$
rdw	rdw addr=a lce=1 lru_way=w [src=ra]	produce sharers, lru info, etc.
rde	rde addr=a lce=1 way=w [src=ra] dst=rd	$rd = addr, sh\_st[lce] = state$
wdp	wdp addr=a p=0,1	$pending\_bits[addr] + / - 1$
clp	clp addr=a	$pending\_bits[addr] = 0$
clr	clr addr=a lce=1	clear directory row
wde	wde addr=a lce=1 way=w [src=ra] state=s [state]	$dir[addr, lce] = [tag, state]$
wds	wds addr=a lce=1 way=w [src=ra] state=s [state]	$dir[addr, lce].state = state$
gad	gad	execute GAD unit

Table 4.15: BP-BedRock ucode CCE Coherence ISA - Directory

Op	Format	Function
wfq	wfq queue [queue...]	wait for message on queue(s)
pushq	pushq queue cmd addr=a lce=1 way=w [src=ra] wp=0,1 spec=0,1	push message to queue
popq	popq queue [wp]	dequeue message, write pending bit
poph	poph queue rd	capture message header
specq	specq spec_cmd addr_sel [state]	speculation bits operation
inv	inv	send invalidations

Table 4.16: BP-BedRock ucode CCE Coherence ISA - Queue

### 4.5.1 Instruction Set Architecture (ISA)

The ucode CCE executes a custom instruction set architecture (ISA) designed to efficiently execute the BedRock coherence protocol. The ISA is divided into a *Base ISA* and a *Coherence ISA*. The Base ISA includes standard, general-purpose RISC ISA instructions such as arithmetic, branching, and data movement operations. The Coherence ISA includes the BedRock-specialized instructions that enable efficient execution and processing of the BedRock coherence protocol. The Coherence

ISA instructions are divided into Flag, Directory, and Queue operations, and include operations to perform coherence directory reads and writes, message send and receive, and complex coherence protocol control flow execution.

Across the ISA, all branch instructions are tagged with a static taken/not-taken prediction bit and the branch mispredict penalty is one cycle. Directory read and queue operations may take more than one cycle to execute depending on functional unit conflicts and latencies, while all other instructions execute in a single cycle.

## Base ISA

The Base ISA comprises ALU (Table 4.11), Branch (Table 4.12), and Data Movement (Table 4.13) instructions. Many of the instructions in these groups are commonly found in general-purpose RISC instruction sets. The ALU instructions include basic arithmetic and bitwise operations. The Base ISA tables describe each op, its microcode format, the operation's function, and whether it is implemented in hardware or is a software pseudo-operation. Pseudo-operations are indicated by a ✓ symbol and are available for the programmer to use in the microcode. These operations are transformed into hardware operations by the microcode assembler, which allows for a richer programmer interface while reducing hardware implementation complexity.

## Flag Instructions

Flag instructions can set or clear flags, perform logic operations on pairs of flags, and make control flow decisions based on the state of a programmer-selected set of flags. Table 4.14 lists the available flag instructions. The most important of these are the flag-based branch instructions (bf, bfz, bfnz, bfnz). Each flag-based branch examines a set of programmer-selected MSHR flags, encoded in a bitmask within the instruction, and branches the microcode PC to the supplied target PC if the branch condition is met. A single flag-based branch instruction is able to replace a sequence of regular branch instructions, thereby accelerating common protocol processing control flow decisions.

## Directory Instructions

Directory instructions, listed in Table 4.15, accelerate directory read, write, and processing operations by invoking the coherence directory and GAD modules. Directory way group reads require only  $1 + (C/2)$  cycles to execute, compared to tens or hundreds of cycles that would be required by a general-purpose implementation of the same routine using for loops. Pending bit and directory entry reads require one and two cycles, respectively. Directory writes execute in a single cycle. The GAD module executes in a single cycle, compared to a cost of tens of instructions to implement equivalent logic in general-purpose RISC code. Additionally, the flag outputs of the GAD module never need to be recomputed by the microcode program, saving many additional cycles for every flag-based branch instruction.

## Queue Instructions

Queue instructions enable efficient sending and receiving of coherence protocol and memory messages and are listed in Table 4.16. The ucode CCE is able to send and receive messages with a cost of one cycle per message header or data beat. The invalidate (inv) instruction further accelerates coherence protocol processing by invoking a small hardware-implemented state machine within the ucode CCE's message unit to efficiently send invalidation commands to all caches with a Shared (S) copy of the specified cache block at a rate of one message per cycle. A general-purpose RISC

routine for invalidations would require at least a few instructions per invalidation sent if executed in a tight for loop.

## **Programming the CCE**

The CCE is programmed at the microcode level. A custom assembler applies a limited set of instruction transformations to map available software pseudo-ops into hardware-implemented microcode instructions. BP-BedRock's MOESIF protocol microcode is only 125 instructions, which includes support for uncacheable access to both cacheable and uncacheable memory and system initialization.

### **4.5.2 Fetch - Instruction RAM and Predecode**

The Fetch stage of the ucode CCE includes the Instruction RAM and Predecode modules. The Instruction RAM module contains the microcode instruction memory, the fetch program counter (fetch PC), and next PC logic. After system reset, an external configuration bus loads the CCE microcode into the instruction memory and then transitions the CCE into its microcode execution mode. Once regular execution begins, a new instruction is fetched every cycle unless the Execute stage raises the stall signal. If a stall occurs, the previously fetched instruction is held valid on the output of the instruction memory.

The instruction RAM module outputs the fetched instruction and the fetch PC, which are fed to the Instruction Predecode module. The predecoder determines if the instruction is a branch instruction, whether the instructions predict taken bit is set, and the branch target encoded in the instruction. It then outputs a predicted fetch PC that is either the current PC plus one or the branch target. The instruction RAM uses the predicted fetch PC to fetch the next instruction, unless the execute stage reports a branch misprediction. Branch mispredictions unconditionally redirect the fetch PC to the resolved PC provided by the Branch module in the Execute stage.

### **4.5.3 Execution Control**

The Instruction Decode, Source Select, Arbitrate, and Instruction Stall modules make up the Execute stage's control logic. Collectively, these modules create the necessary control signals for the ucode CCE's functional units, arbitrate access to functional units shared by the microcode and the Message unit, and detect execution hazards.

#### **Instruction Decode**

The Instruction Decode unit expands the narrow microcode instruction into a much wider decoded instruction that contains functional unit control signals. The decode module also contains the current instruction and PC registers. Instruction Stalls cause the current instruction to be replayed in the next cycle, and branch mispredictions cause a single cycle bubble in execution while the Execute stage waits for a new instruction to be fetched. The output of the decoder is the decoded instruction and the current Execute stage PC.

#### **Source Select**

The source select module routes operands to the ucode CCE's functional units based on the current instruction. A source operand may come from the general purpose registers, MSHR fields, inbound network message fields, or directory outputs, depending on the specific instruction being executed.

This module primarily exists to centralize the source selection logic and de-clutter the BP-BedRock implementation code.

## Arbitration

The arbitration unit controls access to the coherence directory, pending bits write port, and speculative bits read port. In a given cycle, each of these three resources may be used by either the microcode instruction or the message unit. Conflicting use of a resource results in the current instruction stalling and the message unit winning arbitration.

## Instruction Stall

The Instruction Stall unit controls whether the current instruction executes and commits or must be replayed in the following cycle. Stalls occur due to functional unit hazards and when attempting to send or receive BedRock messages when the target network is either busy or does not have a valid message available for processing, respectively. The unit takes the decoded instruction as input, examines its control signals, and stalls execution if any of the possible stall conditions are met. The stall signal is routed to the Fetch stage to retain the previously fetched instruction, and to the instruction decoder to replay the current instruction in the next cycle. Functional unit hazards arise when the Message unit and the current microcode instruction attempt to use the same functional unit. To ensure forward progress and provide higher message processing throughput in the coherence protocol, the message unit has priority over the microcode instruction.

### 4.5.4 Register File

The Register File stores the internal state of the ucode CCE. There are four registers stored in the register file that hold the CCE's Miss Status Handling Register (MSHR), eight 64-bit general purpose registers (GPRs), a coherence state register, and an auto-forward control register. The MSHR register is identical to the one in the FSM CCE and is described in [Subsection 4.4.4](#). Registers are primarily written directly by microcode instructions, but the LRU Address and LRU Coherence State fields of the MSHR are also written by the directory during way group reads. The eight 64-bit general purpose registers are used by the microcode program to store temporary variables and values during execution. The coherence state register is a special register that holds a default coherence state that can be applied to coherence or memory commands and used as a source operand by microcode instructions. The auto-forward control register is a single bit register that controls whether the ucode CCE's Message unit will automatically process memory response messages. This bit is set by default, but can be disabled for debugging purposes or to allow the microcode full control over memory response processing.

### 4.5.5 Functional Units

The ucode CCE includes a handful of Functional Units that execute operations requested by the current microcode instruction. The Coherence Directory, Pending Bits, Speculative Bits, and GAD modules are all re-used without modification from the FSM CCE design, and are described in [Section 4.4](#).

## Branch

The Branch unit resolves branches and validates the Fetch stage's speculative fetch. The branch unit takes the current instruction's two operands, branch operation, valid bit, predict taken bit, PC,

and branch target as inputs. It then computes the result of the branch operation and determines if a misprediction occurred by comparing the branch outcome to the predict taken bit. Mispredictions result in a single cycle bubble in the execute stage and redirect the Fetch stage to the proper fetch PC. The next fetch PC will either be the current Execute stage PC plus one or the branch target, depending on the outcome of the branch comparison.

## ALU

The Arithmetic Logic Unit (ALU) is a simple, 64-bit wide ALU supporting addition, subtraction, logical shifts, and bitwise operations. The supported bitwise operations are AND, OR, XOR, NAND, NOR, and negation. The ALU also supports logical negation of a single operand. The hardware ALU is purposefully simplistic to reduce complexity. Additional common operations are supported at the software level by the assembler. Software supported operations include increment, decrement, add immediate, subtract immediate, and shift immediate.

## Message

The Message unit is responsible for sending and receiving all BedRock network messages. The message unit can write the pending bits, read the speculative bits, and write the coherence directory. It also contains the memory credit flow counter that limits the number of outstanding memory commands issued by the CCE. The message unit has two state machines to process memory response messages and send or receive messages according to the execution of microcode instructions.

The memory response state machine is effectively identical to the memory response FSM of the FSM CCE. It processes arriving memory response messages, reads the speculative bits if the response is speculative, and then squashes the message, forwards the message to the appropriate , or sinks the response at the CCE. The memory response state machine can be disabled by clearing the auto-forward control register stored in the register file.

The other state machine sends and receives messages based on the currently executing instruction. This state machine is activated by a push or pop instruction, and the instruction specifies the network, message type, and message information required.

### 4.5.6 Uncached-Only Mode

The ucode CCE contains logic sufficient to support uncached requests immediately following system reset. This logic is implemented primarily in the Message unit, which consumes LCE request messages and forwards them to memory as uncached loads or stores. Memory responses are auto-forwarded from the memory network to the LCE command network. Very minimal processing occurs in the uncached-only mode, and it is meant to support system debugging. The CCE exits uncached-only mode when commanded to by a mode change via the configuration bus. The external configuration device must guarantee that it is safe to transition from uncached-only to normal mode, and must ensure that the microcode program required by the ucode CCE has been loaded into the instruction memory.

### 4.5.7 LCE Request Processing

The ucode CCE's microcode programs implement a similar execution flow as the FSM CCE. Arriving requests trigger a coherence directory read before the microcode examines the outputs to determine whether any replacement, invalidations, upgrade, transfer, or memory read is required

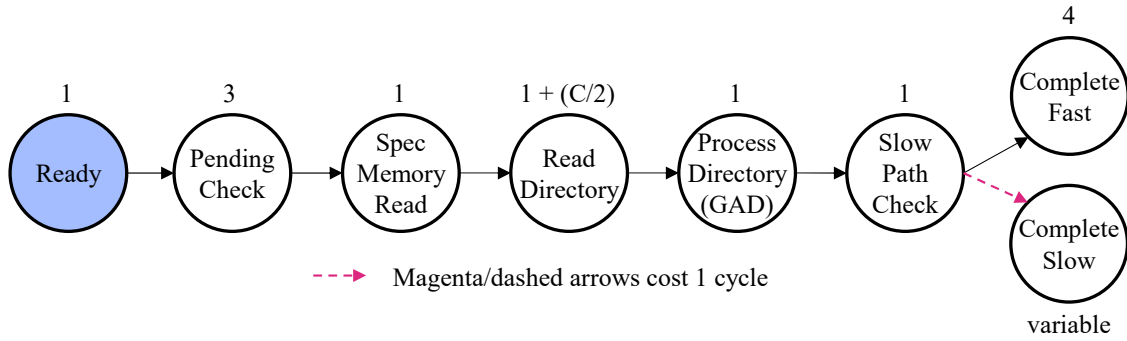


Figure 4.20: BP-BedRock MOESIF Microcode Processing Flow - Initial and Fast Path

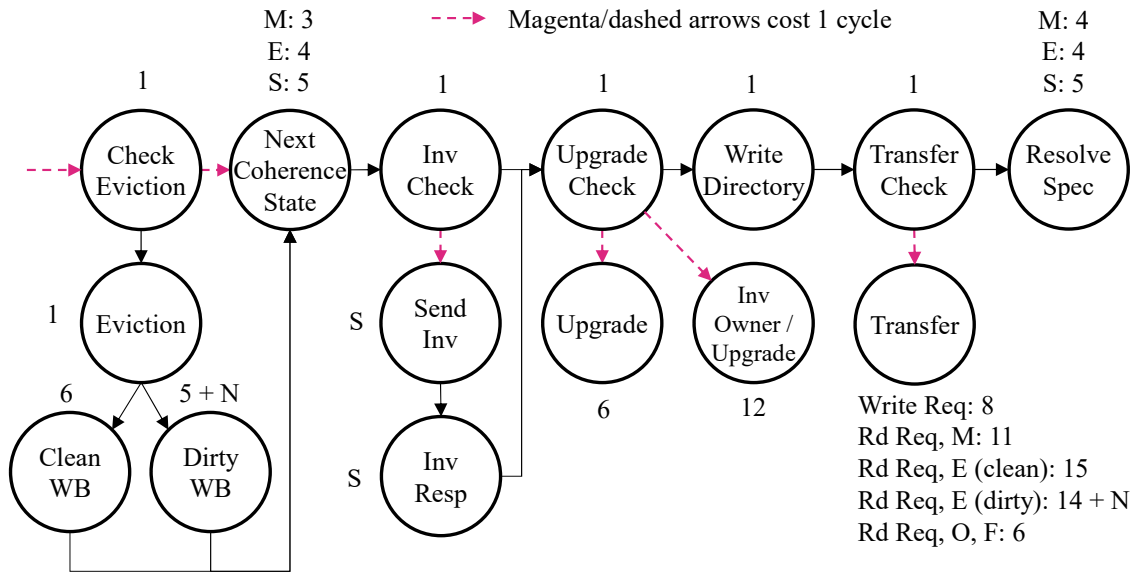


Figure 4.21: BP-BedRock MOESIF Microcode Processing Flow - Slow Path

to complete the request. This section describes the processing flow of the MOESIF cache coherence protocol microcode implementation.

### LCE Request Processing Diagrams

Figure 4.20 and Figure 4.21 depict the MOESIF protocol microcode processing flow. Each circle represents one or more microcode instructions and is called a subroutine. Transitions between subroutines are colored either black or magenta/dashed, with black transitions having no cost and magenta/dashed transitions having a cost of one cycle due to a branch misprediction penalty. The best-case, no contention occupancy in cycles is shown as a number of expression adjacent to each subroutine. The occupancy is typically one cycle per instruction, however certain instructions require multiple cycles to execute, as noted above. Most subroutines have a fixed-cost occupancy, but the value may depend on the specific type of request.

Figure 4.20 shows the initial subroutines executed by the MOESIF protocol for all coherence requests. The microcode is optimized to handle load requests to blocks in the Invalid state (not cached anywhere in the system), which is called the *Fast Path*. All other requests are handled by the *Slow Path*. A fast path request is fulfilled by a memory access, which is issued speculatively

and as soon as possible, before the directory read occurs. The directory read latency depends on the number of Cores (C), as explained in [Table 4.9](#) and [Subsection 4.4.6](#). Following the directory read, a single cycle is required to confirm the request does not require the slow path for processing before finalizing the past path processing.

Slow path requests follow the same initial processing as fast path requests, but then branch to the processing flow shown in [Figure 4.21](#). Note that the magenta arrow between "Slow Path Check" and "Slow Path Completion" subroutines in [Figure 4.20](#) is the same arrow that enters the "Replacement Check" subroutine in [Figure 4.21](#). A request processed by the slow path either targets a block that is already cached somewhere in the system, requires a cache block replacement at the requesting LCE, or is a write request. The occupancy of the *Compute Next Coherence State* and *Resolve Speculation* subroutines depend on the coherence state of the requested block that will be assigned to the requesting LCE. Invalidations require S cycles to send the invalidation commands and another S cycles to receive the invalidation responses. Writebacks during cache block replacement or from a transfer require N cycles to forward the N cache block data beats from the LCE response to the memory network. The *Transfer* subroutine occupancy depends both on the type of request (read or write) and the coherence state of the current block owner. Request processing completes after performing an Upgrade, Transfer, or Resolving Speculation.

### LCE Request Processing Occupancy

[Table 4.17](#) lists the processing occupancy in cycles for subroutines found in the MOESIF coherence protocol microcode program. The cycle counts assume best-case, no-contention execution of the microcode program. Most rows in the table correspond directly to the subroutines shown in [Figure 4.20](#) and [Figure 4.21](#). Routines named starting with *Skip* correspond to performing one of the *Check* subroutines followed by a horizontal transition in [Figure 4.21](#).

[Table 4.18](#) details the request processing occupancy for the MOESIF coherence protocol implementation. The occupancy cycles shown in the tables are derived directly from the MOESIF protocol processing flow diagrams. Given a request type, the current state of the block at the LCE, and the state of the block at the coherence directory, the processing occupancy of the request can be computed by starting at the *Ready* subroutine in [Figure 4.20](#) and progressing through the two diagrams. All requests assume that a cache block replacement is not required. The addition of a replacement adds either six or  $5 + N$  cycles to the processing latency for null and dirty writebacks, respectively.

All requests have a best processing cost of  $8 + (C/2)$  cycles to move from Ready through directory read and processing and then execute the slow path check. The slow path check branch is predicted taken to the fast path, which requires an additional four cycles to finish processing exclusive read requests for invalid blocks. All other requests incur a branch mispredict penalty of one cycle between the slow path check and the *Replacement Check* subroutine in [Figure 4.21](#). Slow path requests then perform a replacement, if required, compute the next coherence state of the requested block for the requesting LCE, and invalidate the requested block from any LCE with the block in the Shared (S) state as needed. Request processing is then finalized by performing a cache block upgrade if the requestor already has a valid copy of the block, a cache to cache transfer if another cache owns the block, or simply resolving the speculative memory access if the block will be filled from memory.

Routine	Occupancy (cycles)	Notes
Ready through Directory Read	$7 + (C/2)$	Ready through Process Directory (GAD)
Fast path Completion	4	Load request to block in I
Branch to slow path	2	1 cycle branch mispredict penalty
Skip replacement	2	1 cycle branch mispredict penalty
Replacement (Dirty)	$7 + N$	Dirty writeback
Replacement (Clean)	8	Null writeback
Compute Next State	3 to 5	Next state of M (3), E (4), S (5)
Skip invalidations	1	Branch predicted taken
Invalidation	$2 + (2 * S)$	Invalidation commands and responses
Skip upgrade	1	Branch predicted taken
Upgrade	7	No owner
Upgrade (Owner in O/F)	13	Invalidate Owner
Write Directory	1	Write tag and state to directory
Skip Transfer	1	Branch predicted taken
Transfer (Read, O/F)	7	Owner in O or F
Transfer (Read, M)	12	Owner in M
Transfer (Read, E and clean)	16	Owner in E and clean
Transfer (Read, E and dirty)	$15 + N$	Owner in E and dirty
Transfer (Write)	9	Write request
Resolve Speculation	4 or 5	Next state of E, M (4), S (5)

Table 4.17: BP-BedRock ucode CCE Subroutine Occupancy - MOESIF

## 4.6 FSM and ucode CCE Performance Comparison

The fixed-function and microcode-programmable CCEs implement the same coherence protocol using two very different approaches. Therefore, it is important to compare the performance of the two designs to fully understand the implications of using a programmable protocol processing engine. In this section, the performance of the two BP-BedRock coherence engines is compared by first examining the best-case no-contention request processing occupancy in the two coherence engine designs before evaluating the impact of request processing occupancy at the application level.

### 4.6.1 Comparison of ucode and FSM CCE

Table 4.19 presents the request processing occupancy for both coherence engines for BedRock's MOESIF protocol. Processing occupancy, given in cycles, is the number of cycles required in a best-case, no-contention execution to process a coherence request. Three constants are used in the processing occupancy computations:  $C$  is the number of cores in the multicore processor,  $N$

Request	LCE State	Directory State	Occupancy (cycles)	Notes
Read Excl	I	I	$12 + (C/2)$	Block from Memory
Read NE			$26 + (C/2)$	Block from Memory
Read	I	S	$26 + (C/2)$	Block from Memory
		E (clean)	$36 + (C/2)$	Transfer and Null Writeback
		E (dirty)	$35 + (C/2) + N$	Transfer and Dirty Writeback
		M	$32 + (C/2)$	Transfer
Write	I	O, F	$27 + (C/2)$	Transfer
		I	$23 + (C/2)$	Block from Memory
		S	$24 + (C/2) + (2 * S)$	Block from Memory
		E, M	$27 + (C/2)$	Transfer
Write	S	O, F	$28 + (C/2) + (2 * S)$	Invalidate and Transfer
		S	$24 + (C/2) + (2 * (S - 1))$	Invalidate and Upgrade
Write	O, F	O, F	$30 + (C/2) + (2 * (S - 1))$	Invalidate and Upgrade
		O, F	$24 + (C/2) + (2 * S)$	Invalidate and Upgrade

Table 4.18: BP-BedRock ucode CCE Request Occupancy - MOESIF

is the number of data beats required to send a full cache block across the coherence network data channels, and  $S$  is the number of caches holding a block in the Shared (S) coherence state, called the sharers. The data presented are the number of cycles that the coherence engine is busy processing a single request. The numbers presented assume that a cache block eviction (replacement) is not required. Occupancy provides insight into the maximum achievable throughput of the coherence engine designs. The request occupancy does not include the time required to process memory responses, which are handled by a separate state machine in both designs that operates concurrent to request processing. Network time is also excluded as the time for messages to transit networks is the same for both designs.

The FSM CCE has a base request processing occupancy of  $7 + (C/2)$  cycles, incurred by all requests. During this initial processing, the request is consumed, the directory is read and processed, and the directory entry for the requesting cache is updated with the final next state for the block. Then, depending on the specific request and state of the target block in the system, the FSM executes only those steps required to complete the transaction. The key performance advantage of the FSM-based design is that control flow decisions are effectively free; in any given state, the next state is computed concurrently with the protocol processing occurring in the state. Thus, after executing the initial processing, the added cost to complete a request is simply the cost of the remaining states visited. The worst-case request, in terms of occupancy, is a write request to a block in the O or F state, which is owned by a single cache but shared by many caches and may be present in every single cache in the system. Additionally, a cache block replacement adds either two or  $1 + N$  cycles of processing time for clean and dirty blocks, respectively.

Request	LCE State	Directory State	FSM CCE Occupancy (cycles)	ucode CCE Occupancy (cycles)
Read Excl	I	I	$8 + (C/2)$	$12 + (C/2)$
Read NE				$26 + (C/2)$
Read	I	S	$8 + (C/2)$	$26 + (C/2)$
		E (clean)	$10 + (C/2)$	$36 + (C/2)$
		E (dirty)	$9 + (C/2) + N$	$35 + (C/2) + N$
		M	$9 + (C/2)$	$32 + (C/2)$
		O, F	$9 + (C/2)$	$27 + (C/2)$
Write	I	I	$8 + (C/2)$	$23 + (C/2)$
		S	$8 + (C/2) + (2 * S)$	$24 + (C/2) + (2 * S)$
		E, M	$9 + (C/2)$	$27 + (C/2)$
		O, F	$9 + (C/2) + (2 * S)$	$28 + (C/2) + (2 * S)$
Write	S	S	$9 + (C/2) + (2 * (S - 1))$	$24 + (C/2) + (2 * (S - 1))$
		O, F	$9 + (C/2) + (2 * (S - 1))$	$30 + (C/2) + (2 * (S - 1))$
Write	O, F	O, F	$9 + (C/2) + (2 * S)$	$24 + (C/2) + (2 * S)$

Table 4.19: BP-BedRock CCE Request Occupancy Comparison - MOESIF

The ucode CCE incurs execution overheads relative to the FSM-based CCE primarily due to its inability to execute protocol processing and control flow in the same instruction and the fact that each control flow decision requires a separate instruction. As described in [Subsection 4.5.7](#), the MOESIF microcode program includes a fast path to process regular reads for blocks in the Invalid state. This path has an execution overhead of only four cycles compared to the FSM-based coherence engine. The fast path is effectively a single basic-block of microcode, and therefore can be executed at a rate matching that of the FSM-based engine. However, all other requests must branch to the full path, which is capable of performing replacements, invalidations, and cache to cache transfers. The base occupancy for both paths is only one cycle greater than the FSM-based engine at  $8 + (C/2)$  cycles. Requests processed by the full path have occupancy overheads between 15 to 25 cycles. Significant overheads are incurred for subroutines that require multiple control flow decisions. In particular, determining the proper next coherence state for the block, resolving the outcome of the speculative memory access, and initiating cache to cache transfers all add significant latency to request processing. Additionally, a cache block replacement adds either seven or  $6 + N$  cycles of processing time for clean and dirty blocks, respectively.

As noted in [Section 4.4](#), the no-contention request processing occupancy at the CCE in an eight-core BP-BedRock multicore design is between 12 and 27 cycles. The microcode-programmable engine’s occupancy overheads of 15 to 25 cycles effectively results in occupancy overheads of approximately 100% relative to the fixed-function coherence engine for such a design. However, the manifested impact of this overhead on application or system performance may still be minimal, depending on the frequency of cache coherence operations and transactions during execution.

#### 4.6.2 Splash-3 Application-Level Performance

To compare the impact of coherence engine design on system performance, a collection of benchmarks from the Splash-3 [\[110\]](#) suite were run on an FPGA-based 8-core BP-BedRock systems with the FSM-based and microcode programmable coherence engines. The BP-BedRock FPGA designs instantiate an 8-core BlackParrot multicore with 32 KiB L1 instruction and data caches, a 512 MiB shared L2 cache, 2 GiB of HBM-based main memory, and a core clock frequency of 50 MHz. The benchmarks were compiled for the RISC-V ISA using `gcc` targeting a Linux environment, and

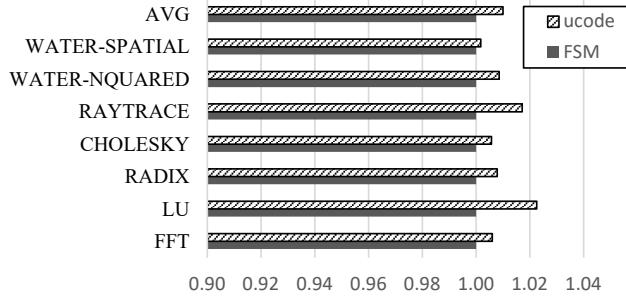


Figure 4.22: BP-BedRock Splash-3 Normalized Execution Time - 8 core

invoked to execute on all 8 available processor cores. The programs were run in a Linux-based OS environment constructed using BuildRoot [18] and Busybox [19] with Linux kernel v5.15 [124] and OpenSBI v1.0 [101]. The FFT, LU, RADIX, and CHOLESKY programs are smaller kernel programs, while the remaining three programs are larger application programs. Readers are referred to [110] and [131] for more details on the synchronization and memory characteristics of these programs. Wall-clock execution time for all benchmarks ranged between tens of seconds and tens of minutes.

Figure 4.22 shows total execution time measured using the `time` utility for each benchmark, averaged over three runs, and normalized to the FSM-based multicore design. Despite having a 15 to 25 cycle best-case processing occupancy overhead, the ucode CCE-based design experiences a very small performance degradation, being within 1% of the hardware-based coherence engine’s performance on average, and only 2.3% slower at worst. Intuitively, this result makes sense as any program with reasonably good cache utilization and low miss rates will only invoke the coherence system on a cache miss. If misses are infrequent, the overall impact of the programmable coherence engine’s increased processing occupancy latencies will be small, which follows directly from the standard average memory access time computation. This result indicates a promising path forward for further exploration of programmable coherence engines. Careful design of the protocol processing paths can keep a programmable coherence engine competitive with a fixed-function engine, while the flexibility of a programmable system can unlock exciting new system features.

## 4.7 FSM and ucode CCE Area Comparison

BlackParrot, including BP-BedRock, has been silicon validated using GlobalFoundries 12nm Fin-FET process and FPGA validated in an 8-core configuration for each coherence engine using a Xilinx Ultrascale+ VCU128 development platform[41]. Table 4.20 provides area and resource utilization overheads for ASIC and FPGA-based designs using the ucode CCE, normalized to designs using the FSM CCE. The more efficient ASIC implementations show the introduction of programmability into the coherence system comes at a small area cost of only 4.08% extra die area for the entire multicore and a 4.28% increase per BlackParrot Tile. Each BlackParrot Tile comprises a BlackParrot core, its 32 KiB L1 D\$ and I\$, a 64 KiB slice of the distributed L2 cache, the on-chip networks and routers to connect tiles, and an instance of the BP-BedRock coherence engine and directory. All SRAM macros are hardened in the ASIC flow. The area overheads of the ucode CCE designs are largely due to the addition of the microcode instruction SRAM. In the FPGA implementations, the logic utilization increases by only 6.32% and 7.08% for the entire multicore and per tile, respectively, when using the ucode CCE. Each programmable CCE additionally requires a single 18 Kib block

Design	Component	Resource	Overhead
ASIC	Multicore		4.08%
	Tile	Die Area	4.28%
	CCE		31.08%
FPGA	Multicore	Logic LUTs	6.32%
		BRAM	1.54%
	Tile	Logic LUTs	7.08%
		BRAM	1.54%
	CCE	Logic LUTs	66.19%
		BRAM	1 per CCE

Table 4.20: BP-BedRock ucode CCE Resource Overheads

RAM resource, which amounts to a 1.54% increase in 18 Kib block RAM resources<sup>5</sup>. Additionally, both coherence engine implementations meet the same design target frequency in both the ASIC and FPGA implementations.

## 4.8 Conclusion

In this chapter, a complete, fully open-source implementation of the BedRock cache coherence protocol within the BlackParrot 64-bit RISC-V shared-memory multicore processor, called BP-BedRock, is described. BP-BedRock provides a fully functional implementation of the BedRock protocol including its Local Cache Engines (LCE), Cache Coherence Engines (CCE), and coherence networks. The coherence directories in BP-BedRock are complete duplicate-tag directories and rely on an innovative directory segment architecture to provide constant-sized coherence engines and directory storage, regardless of the number of cores in the tiled multicore design. The coherence directory storage overhead in BP-BedRock is a constant 6.25% relative to the capacity of the coherent L1 caches. Two coherence directory implementations are provided, one that is hardware-based and fixed-function and a second that is microcode programmable. An analysis of the two coherence engine designs show that it is possible to introduce programmability into the cache coherence system of modern shared-memory multicore processors with minimal area and performance overheads. The key to realizing programmability at low overheads is the use of highly-specialized coherence processing modules and instruction set extensions that offload the core of the coherence protocol processing from general purpose code. Consequently, the microcode programmable coherence engine implementation has only single-digit percentage area and resource costs at the multicore design level while incurring only a 1% average (2.3% worst-case) performance overhead for the Splash-3 benchmarks. Using programmability to implement the cache coherence protocol has an area or resource overhead of 4-7% at the multicore tile level.

<sup>5</sup>36 Kib block RAMs are counted as two 18 Kib block RAMs for this analysis.

# Chapter 5

## Hybrid CCE

The two coherence directory implementations of BedRock presented in [Chapter 4](#) demonstrate the tradeoffs involved in introducing programmability into the cache coherence system at the coherence directory. While the fixed-function directory offers superior performance, the programmable engine can be leveraged to introduce system-specific functionality. Despite architectural and microarchitectural optimization, the microcode-programmable coherence engine is unable to match the coherence protocol processing performance of the fixed-function coherence engine.

In this chapter, a hybrid fixed-function and programmable coherence engine architecture (Hybrid CCE) is described that attempts to preserve the protocol processing performance of the fixed-function coherence engine and the system-dependent flexibility of the programmable engine with minimal cost and overhead. First, [Section 5.1](#) describes the baseline coherence protocol processing architecture of the hybrid coherence engine, including key learnings that are incorporated from the fixed-function coherence engine described in [Chapter 4](#). Next, [Section 5.2](#) introduces a programmable pipeline to the hybrid CCE architecture, drawing from the learnings of implementing the microcode-programmable coherence engine described in [Chapter 4](#). [Section 5.3](#) presents a performance analysis and comparison of the hybrid coherence architecture by comparing its processing occupancy latencies and microbenchmark performance to that of the fixed-function and programmable architectures. [Section 5.4](#) presents a comparison of resource utilization for the hybrid coherence engine architecture to that of the fixed-function and programmable coherence engines.

### 5.1 Fixed-Function Protocol Processing Architecture

In [Chapter 4](#), a fixed-function coherence engine architecture is presented that correctly implements the BedRock cache coherence protocol. The FSM CCE architecture employs specialized hardware to accelerate coherence protocol operations, but its initial design relies on one large and complex state machine to handle LCE request and response message processing and memory command issue. Therefore, the first step in defining the hybrid coherence engine is to revisit the fixed-function coherence protocol processing logic architecture. [Figure 5.1](#) presents the outcome of this design iteration. The hybrid CCE's coherence protocol functionality is decomposed into a set of independent pipes. All pipes execute concurrently and manage a single type of incoming protocol or memory message. Memory response messages are processed by the Memory Response Pipe, LCE Response messages are processed by the LCE Response Pipe, and LCE Request messages are

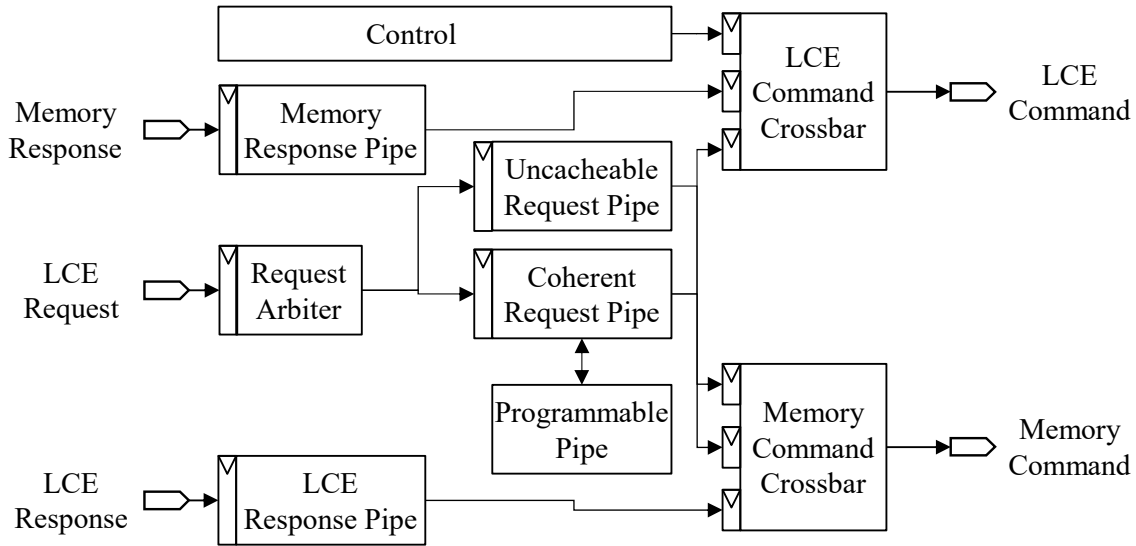


Figure 5.1: Hybrid CCE Block Diagram

processed by either the Uncacheable Request Pipe or the Coherent Request Pipe after first being classified by the Request Arbiter block. The rest of this section describes the functionality of each processing pipe and the other major modules in the coherence engine.

### 5.1.1 Coherence State Management

Figure 5.2 shows the three coherence state blocks in the hybrid CCE and their interaction with the various functional pipes in the design. As with the FSM and ucode CCE designs, the three pieces of coherence state used to implement the coherence protocol are the coherence directory, pending bits, and speculative bits. The pending bits are used to enforce intra-way-group ordering of requests. They are written by the memory response, LCE response, and coherent request pipes and read by the pending queue. New coherence requests and outgoing memory commands increment the associated pending bit while LCE and memory responses decrement the associated pending bit. The coherence directory is used exclusively by the coherent request pipe to track and manage the coherence state of all cache blocks in the coherence system. The speculative bits are written by the coherent request as speculative memory reads are issued. The memory response pipe reads the speculative bits when memory response messages return to the coherence engine to determine how to process the message.

### 5.1.2 Command Crossbars

The LCE Command and Memory Command Crossbars arbitrate access to the outbound LCE and Memory Command network interfaces, respectively, for the various hybrid CCE modules that issue commands into the coherence and memory systems. Each crossbar provides minimal input buffering and round-robin arbitration among input sources for fair and efficient interconnect utilization.

The LCE Command crossbar arbitrates messages sent from the coherent request pipeline, the memory response pipeline, and the control unit. The control unit only issues commands when the CCE performs initialization and mode switches from an uncached request only mode to its normal fully-coherent mode. The coherent request and memory response pipelines frequently issue commands throughout the course of normal operation.

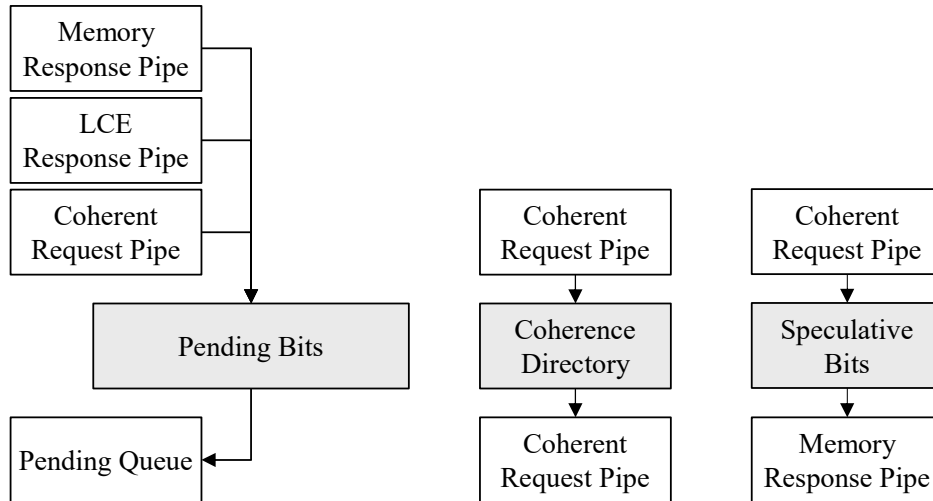


Figure 5.2: Hybrid CCE Coherence State and Pipe Interaction

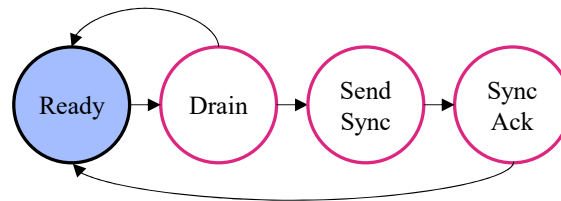


Figure 5.3: Hybrid CCE Control State Machine

The Memory Command crossbar arbitrates access to the outbound memory command interface from the uncacheable request, coherent request, and LCE response pipelines. During normal operation, the majority of memory commands are issued by the coherent request pipe as it issues speculative or non-speculative memory block reads to the LLC or main memory, with commands also coming from the LCE response pipe to perform writebacks of dirty cache blocks. The uncacheable request pipe is primarily used during startup or to interact with I/O devices through uncached accesses.

### 5.1.3 Control

The Control unit is primarily responsible for managing the mode switch from the initial uncached-only request processing mode to the CCE's fully coherent normal mode. At system boot, the hybrid CCE begins execution in an uncached-only mode that processes all requests as if they were targeting uncacheable and uncoherent memory space. All requests are forward to the uncacheable request pipeline by the request arbiter. The uncacheable request pipe then forwards the request to the memory system (LLC or main memory) without performing any coherence checks or operations. This mode is intended to facilitate system boot operations, such as preloading memory, bootroms, and other configuration registers within the multicore and system.

At some time after boot, the system or the multicore itself is expected to perform a software-managed mode switch to enable the cache coherence system. This occurs by writing a register in BlackParrot's configuration bus device, which is then observed by the control unit. Upon seeing the mode switch register write, the control state machine, depicted in [Figure 5.3](#), halts the processing

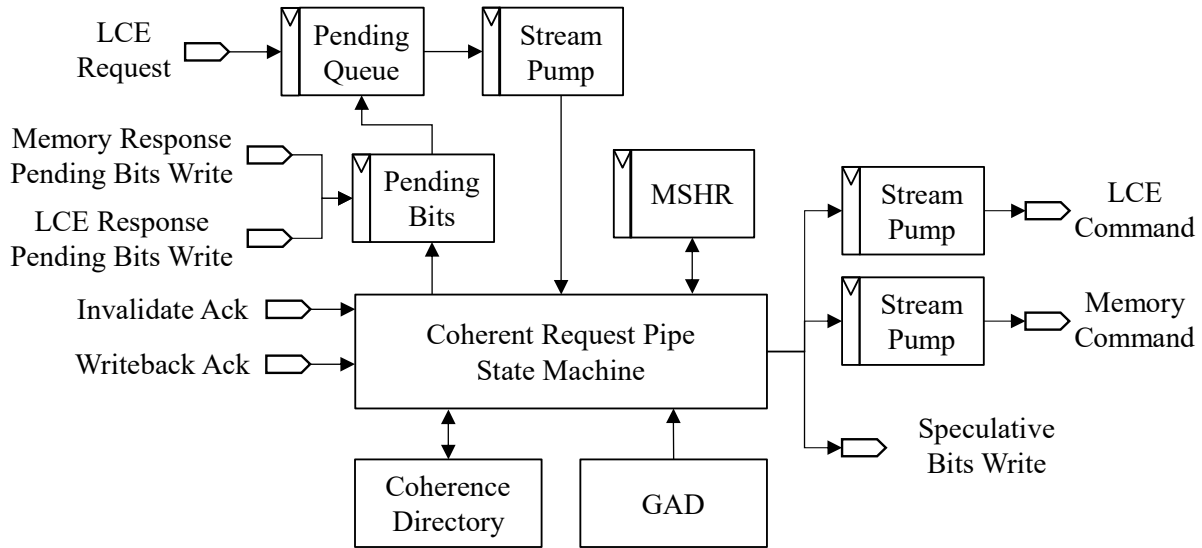


Figure 5.4: Hybrid CCE Coherent Request Pipe Block Diagram

of all new requests and drains all outstanding requests from the CCE’s various pipes by asserting a `drain_then_stall` signal. Once all requests have been drained, it issues a sync command to each LCE in the system before waiting for all sync acknowledgments to return, indicating that all LCEs in the system have entered coherent mode. Once the mode switch is complete, the control unit deasserts the `drain_then_stall` signal, allowing all of the hybrid CCE’s pipes to resume operation in coherent mode.

#### 5.1.4 Request Arbitration

The Request Arbiter module splits the inbound LCE request messages into two logical streams for processing during normal coherent operation. Uncacheable, uncoherent requests are sent to the uncacheable request pipe while all requests targeting cacheable and coherent memory are sent to the coherent request pipe. The CCE itself is not responsible for enforcing ordering between the coherent and uncoherent streams. Ordering must be enforced by the system or software running on the individual cores using mechanisms such as fencing.

Arbitration adds one cycle of latency, but can sustain one request per cycle assuming downstream resources are available. The added cycle of latency comes from a request FIFO buffer used to decouple the inbound request consumption from the arbitration logic. The size of the request buffer is parameterizable and has a default size of two elements.

It is possible for one stream to stall the other stream if the downstream module, either the uncacheable or coherent request pipe, is unable to accept a new request message. While the request arbiter does not include message buffers for each downstream module, the downstream modules both provide request message buffers to reduce the likelihood of cross-stream stall events.

#### 5.1.5 Coherent Request Pipe

The Coherent Request Pipe implements the directory request processing portion of the BedRock MOESIF cache coherence protocol using logic that is very similar to that of the FSM CCE described in [Chapter 4](#). As shown in [Figure 5.4](#), the coherent request pipe comprises a central state machine

that implements the protocol's request processing logic and interacts with the coherence state and message send and receive interfaces. As in the FSM and ucode CCE designs, coherence state is tracked using the Pending Bits and Coherence Directory. The GAD (Generate Auxiliary Directory Information) module accelerates processing of coherence directory reads, and the MSHR (Miss Status Handling Register) tracks state data for the current request being processed by the pipe.

A key difference between the logic of the coherent request pipe and the FSM CCE's state machine is that the coherent request pipe does not directly include the logic to process LCE and Memory Response messages. Instead, single-bit signals from the respective message processing pipes are routed as inputs to the coherent request pipe to indicate when important protocol messages, such as cache block writebacks and invalidation acknowledgments, have been received and processed.

A second important difference between the coherent request pipe and the FSM CCE's microarchitecture is the presence of the Pending Queue. This module buffers coherence requests that are stalled due to the associated pending bit being set, indicating that a coherence request targeting the same way group is still active. Stalled requests are pushed to the pending queue, which is a simple first-in first-out (FIFO) ordered buffer, allowing the next request in the CCE's request stream to be examined for readiness. This allows newer, younger, and independent coherence transactions to bypass older, stalled transactions, thereby increasing the realized inter-transaction concurrency and the hybrid coherence engine's effective transaction processing throughput. Throughout execution, if both the pending queue and the incoming LCE request stream have valid requests, the pending queue is prioritized, allowing older requests to make forward progress as soon as the prior request in the same way group has resolved. This preserves the ordering of related requests that is determined by the interconnection network and minimizes the complexity of managing request starvation.

Figure 5.5 shows the state machine implemented by the coherent request pipe. In the hybrid CCE, the request state machine is logically divided into two halves separated by the coherence directory update. All processing that occurs prior to the coherence directory update is effectively idempotent. These actions can only revoke access permissions for the target cache block at caches other than the requester or invalidate a block in the requesting cache to make room for the target cache block. Since the cache coherence system operates invisibly to software, the effect of revoking access permissions can only affect performance. If a cache block is invalidated from a cache but program execution requires it to be re-accessed, the cache coherence system will issue a new coherence transaction to acquire permissions for the block. Software remains oblivious to whether the block is currently cached or must be re-fetched, however re-acquiring the block will incur a latency cost that may increase execution latency of the program overall.

After the coherence directory is written to update the coherence state of the requesting LCE the request is considered to be *committed* within the scope of the coherence protocol. The directory write commits the block's coherence state change and alters permissions for the requesting LCE. This change may allow irreversible changes to the memory data within the target cache block or may allow an irrevocable access to the memory data within the cache block. Thus, the coherence protocol processing logic must guarantee that committing the transaction is allowed by the protocol and any other relevant system constraints to maintain program execution correctness. The organization of the request processing state machine into pre- and post-commit halves is a key difference between the hybrid and fixed-function CCE designs.

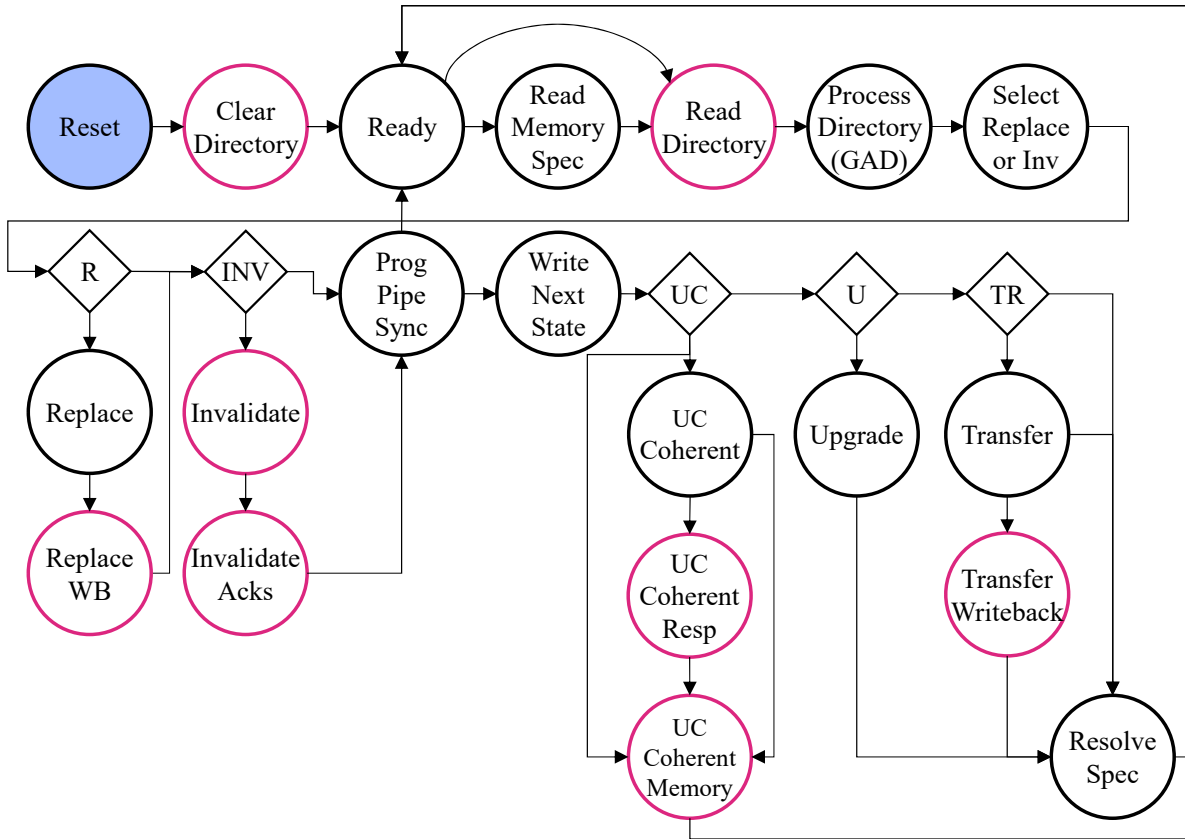


Figure 5.5: Hybrid CCE Coherent Request Pipe State Machine

### Coherent Request Pipe State Machine Occupancy

Table 5.1 describes the coherent request pipe’s no-contention occupancy, in cycles, for states in the coherent request pipe’s state machine. As with the fixed-function and programmable engine occupancy tables, the numbers provided assume a best case processing latency with no contention for resources and no waiting for inbound messages or outbound network availability. As in the other designs, reading the coherence directory requires one cycle of setup plus  $C/2$  cycles to read the tag sets from the directory SRAM’s rows, where  $C$  is the number of cores in the multicore.

In general, most states require only one cycle to execute, assuming the required resource or message is available. This includes states that process responses to commands such as writebacks, since the actual response message is processed by the LCE Response pipe’s state machine that uses single-bit signals to the request pipe to indicate that specific responses have returned and been processed. Invalidation command and response processing requires one cycle per command and response in the general case, to issue the  $S$  commands and process the  $S$  responses, where  $S$  is the number of caches holding the block in the Shared ( $S$ ) state. Other states, such as Write Next State, Resolve Speculation, and states that issue single LCE or memory commands all require one cycle to execute, as is the case in the fixed-function coherence engine design.

Table 5.2 provides the no-contention, best-case processing occupancy for various cacheable and coherent LCE requests given an initial coherence state for the target cache block. These occupancies are computed by stepping through the state machine in Figure 5.5 and summing the latency of each state visited. All requests assume that a cache block replacement is not required. The addition of

State	Occupancy (cycles)	Description
Read Directory	$(C/2) + 1$	One cycle setup, plus one cycle per two cores
Replacement WB Response	1	One cycle per ack from LCE Response Pipe
Invalidation Commands	$S$	One cycle per Sharer
Invalidation Response	$S$	One cycle per ack from LCE Response Pipe
Transfer WB Response	1	One cycle per ack from LCE Response Pipe
Uncached INV/WB Response	1	One cycle per ack from LCE Response Pipe
Uncached Coherent Memory Command	1 to $N$	One cycle per data beat for store, or one cycle for load
All other states	1	

Table 5.1: BP-BedRock Hybrid CCE Request FSM State Machine Occupancy

a replacement adds two cycles to issue the replacement and then process the response signal from the LCE Response pipe.

Examining the coherent request pipe’s state machine diagram, every request has an initial cost of  $5 + (C/2)$  cycles to move from the Ready state through the Select Replacement or Invalidation state. An additional cycle is required for all requests to resolve the speculative memory read that is issued before the directory is read, which is incurred for all transactions. Requests that require invalidating the target block in other caches require  $(2 * S)$  cycles to issue the invalidation commands and then process the invalidation acknowledgment messages. Processing the invalidation acks may overlap with issuing invalidation commands, depending on the network and LCE processing latencies in the system. Additionally, every request requires one cycle to update the coherence directory and one cycle to sync with the programmable pipe. Therefore, the total base latency cost for processing every request is  $8 + (C/2)$  cycles, which is equivalent to the base cost of the fixed-function state machine.

### 5.1.6 Uncacheable Request Pipe

The Uncacheable Request Pipe implements basic request processing logic to handle requests targeting uncacheable, uncoherent memory and for forwarding all requests during uncached-only mode at system startup. Due to the use of the BP-BedRock Stream message protocol and message formats on both the coherence and memory networks, the translation of messages from the request network to the memory command network is straightforward. All of the complex message handling logic is implemented by the stream pumps attached to the LCE request and memory command network interfaces, while the uncacheable request pipe is responsible for coordinating the network handshaking, setting the memory command message type, and populating message payload fields so the memory response pipe can process the returning memory response message correctly.

Request	LCE State	Directory State	Occupancy (cycles)	Notes
Read	I	I	$8 + (C/2)$	Block from Memory
		S	$8 + (C/2)$	Block from Memory
		E	$10 + (C/2)$	Transfer and Writeback
		M, O, F	$9 + (C/2)$	Transfer
Write	I	I	$8 + (C/2)$	Block from Memory
		S	$8 + (C/2) + (2 * S)$	Block from Memory
		E, M	$9 + (C/2)$	Transfer
		O, F	$9 + (C/2) + (2 * S)$	Invalidate and Transfer
Write	S	S	$9 + (C/2) + (2 * (S - 1))$	Invalidate and Upgrade
		O, F	$9 + (C/2) + (2 * (S - 1))$	Invalidate and Upgrade
Write	O, F	O, F	$9 + (C/2) + (2 * S)$	Invalidate and Upgrade

Table 5.2: BP-BedRock Hybrid CCE Request Occupancy

### 5.1.7 Memory Response Pipe

The memory response pipe implements the same response processing logic as the fixed-function coherence engine. The organization of the memory response pipe is depicted in [Figure 5.6](#) while [Figure 5.7](#) depicts a logical abstraction of the memory response logic as a three state FSM. As with the fixed-function coherence engine, this state machine is implemented without any explicit encoding of the three discrete states shown in the figure. The following text briefly summarizes the functionality of the memory response pipe, which is outlined in full in [Subsection 4.4.5](#).

Logically, as every returning memory response message is processed by the memory response pipe it is either forwarded to the appropriate LCE or squashed and sunk in the pipe. Responses with addresses in the cacheable memory address space also decrement the pending bit counter of the associated way group when consumed. Speculative responses read the speculative bits to determine if the request processing logic has finished and resolved the speculation, with processing stalling until speculation has been resolved in the event that the memory read response returns prior to the coherence request processing logic resolving speculation. Speculative responses can either be forwarded without modification, forwarded after modifying the coherence state supplied in the data command to the LCE, or squashed if the read is not required by the protocol. Non-speculative memory responses are either forwarded directly to the LCE specified in the message header or sunk by the memory response pipe, depending on the type of response message.

### Memory Response FSM Occupancy

[Table 5.3](#) provides the no-contention memory response logic processing occupancies for the supported memory response message types. Write and Uncached Write responses each require a single cycle to process, which includes writing the pending bit and sending a command message, if required. Uncached Read and Read responses each require  $N$  cycles to process. The number of cycles required to send the BedRock command message is determined by the the data width of the

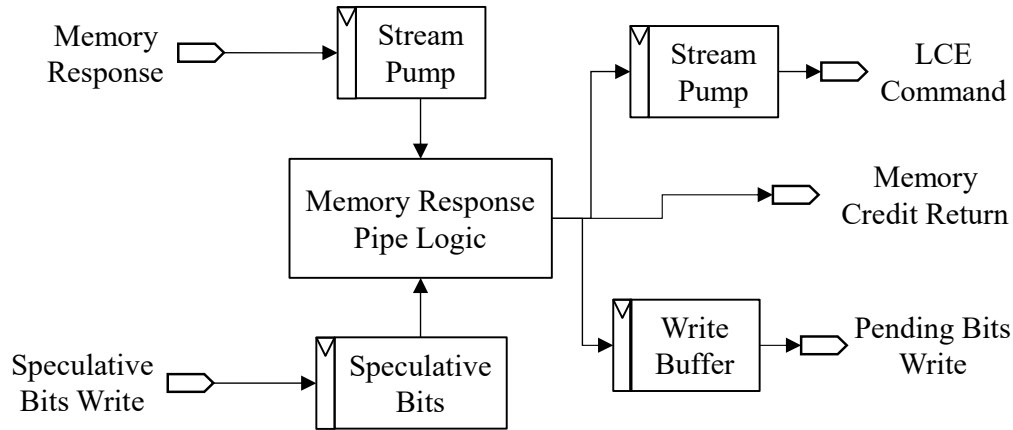


Figure 5.6: BP-Bedrock Hybrid CCE Memory Response Pipe Block Diagram

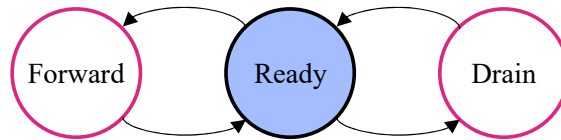


Figure 5.7: BP-Bedrock Hybrid CCE Memory Response Pipe Abstract State Machine

BedRock network channels and the cache block size in the coherence system.

### 5.1.8 LCE Response Pipe

The LCE response pipe processes response messages from the LCEs, including command acknowledgments and cache block writebacks. Figure 5.8 depicts the organization of the LCE response pipe. LCE response messages arrive from the coherence network interface into a message stream pump, which presents the messages for processing to the state machine. The response state machine then issues memory commands, updates the pending bits, or signals message arrival to the coherent request pipe, depending on the specific type of response message being processed. The LCE response pipe operates completely independently from the coherent request or uncached request pipes. However, output signals from the LCE response pipe are consumed by other pipes in the hybrid coherence engine, which requires the other pipes to be able to process these signals at any cycle, independent of any other processing occurring in those pipes.

At system startup, synchronization acknowledgment messages are sunk by the response pipe, with each message raising the sync ack signal to the control pipe. Invalidation acknowledgments are also sunk by the response pipe, with each ack causing the invalidation ack signal to be raised for one cycle to inform the coherent request pipe that an invalidation ack has returned. Writeback responses are forwarded to the last-level cache or memory controller by issuing memory command messages, while null writebacks are sunk by the response pipe. In both cases, the writeback acknowledgment signal is raised to notify the coherent request pipe that the writeback has returned and been processed. Writebacks that are forwarded as memory commands also increment the pending bit of the associated way group to maintain ordering across related coherence transactions. As coherence transactions complete, coherence acknowledgment messages return from the LCEs. Each coherence ack decrements the pending bit of the way group associated with the transaction and raises the coherence ack signal in case it is needed by one of the other pipes in the design.

Message	Occupancy (cycles)	Description
Read	$N$	Cache block read data; forward to LCE
Write	1	Cache block writeback complete; sink message
Uncached Read	$N$	Uncached load data; forward to LCE
Uncached Write	1	Uncached store committed to memory; send Uncached Store Done to LCE

Table 5.3: BP-BedRock Hybrid CCE Memory Response State Machine Occupancy

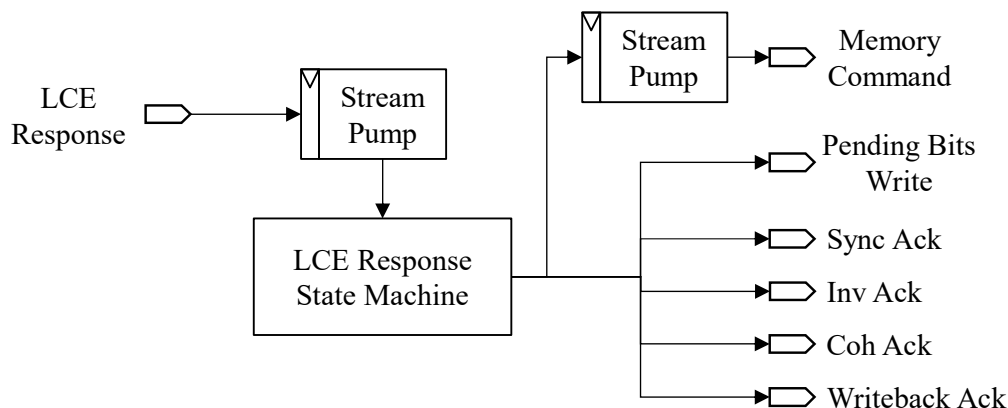


Figure 5.8: Hybrid CCE LCE Response Pipe Block Diagram

Figure 5.9 shows the state machine implemented in the LCE response pipe. Due to the use of stream pumps, the state machine is very simple. Every arriving message is processed over one or more cycles in the Ready state. Response messages that require writing the pending bits transition to the Write Pending state after the message has been consumed and the appropriate single-bit signal has been raised. The pending bit write takes a single cycle, assuming there is no contention for the port from the memory response pipe.

### LCE Response Pipe FSM Occupancy

Table 5.4 lists the message processing occupancy, in cycles, for the LCE response state machine. All messages require at least one cycle to process. Synchronization ack, invalidation ack, and null (clean) writeback messages require exactly one cycle to sink the message and raise the corresponding signal to notify other pipes that the message has returned. Coherence acknowledgments require two cycles to first sink the message and raise the coherence ack signal and then write the pending bit associated with the coherence transaction. Full cache block writeback messages require  $N$  cycles to forward the writeback as a memory command, where  $N$  is the number of beats per message as determined by the implementation's network channel width, plus one cycle to write the pending bit associated with the cache block. For writeback messages, the writeback ack signal is raised when the last beat of the memory command is sent.

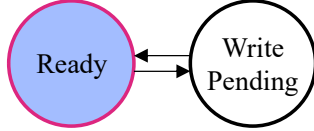


Figure 5.9: Hybrid CCE LCE Response Pipe State Machine

Message	Occupancy (cycles)	Description
Sync Ack	1	Sink message, raise synchronization ack signal
Invalidate Ack	1	Sink message, raise invalidation ack signal
Coherence Ack	2	Sink message, raise coherence ack signal, write pending bits
Writeback	$1 + N$	Forward as memory command, raise writeback ack signal, write pending bits
Null Writeback	1	Sink message, raise writeback ack signal

Table 5.4: BP-BedRock Hybrid CCE LCE Response State Machine Occupancy

## 5.2 Programmable Pipe Architecture

Figure 5.10 shows the organization of the hybrid CCE’s programmable pipe. This pipe is a trimmed-down version of the full microcode-programmable coherence engine architecture that retains the general-purpose microcode-programmable execution logic but removes most of the coherence protocol-specific logic, which is handled by the fixed-function hardware in the hybrid coherence engine. As with the microcode-programmable coherence engine, the programmable pipe is organized as a two-stage fetch-execute pipeline with 64-bit general purpose registers and datapath.

### 5.2.1 Fetch - Instruction RAM and Predecode

The fetch stage comprises the instruction storage RAM and fetch logic plus an instruction predecoder. The Instruction RAM module contains the microcode instruction memory, the fetch program counter (PC), and next PC logic. After system reset, an external configuration bus loads the programmable pipe’s microcode into the instruction memory and starts the pipe’s execution. Once execution begins, a new instruction is fetched every cycle unless the execute stage raises the stall signal. If a stall occurs, the previously fetched instruction is held valid on the output of the instruction memory.

The instruction RAM module outputs the fetched instruction and the fetch PC, which are fed to the Instruction Predecode module. The predecoder determines if the instruction is a branch instruction, whether the instructions predict taken bit is set, and the branch target encoded in the instruction. It then outputs a predicted fetch PC that is either the current PC plus one or the branch target. The instruction RAM uses the predicted fetch PC to fetch the next instruction, unless the execute stage reports a branch misprediction. Branch mispredictions unconditionally redirect the fetch PC to the resolved PC provided by the Branch module in the execute stage.

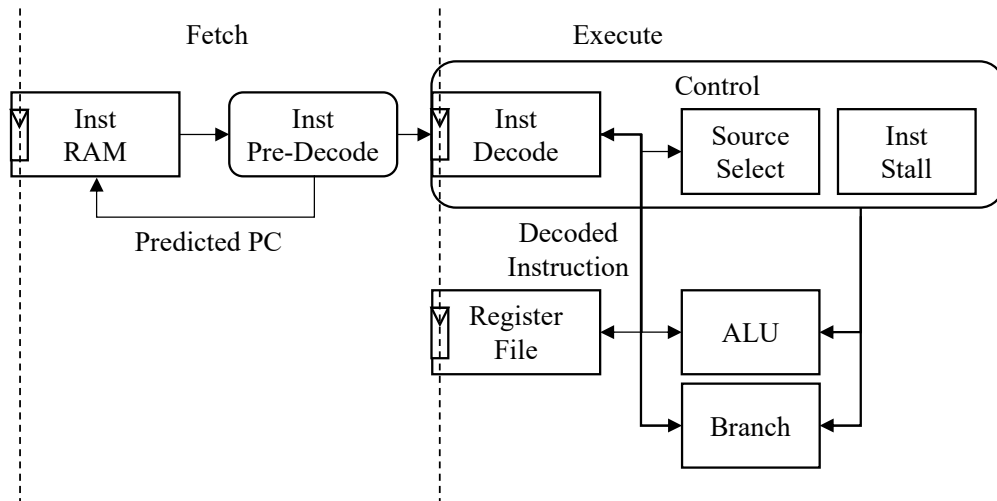


Figure 5.10: Hybrid CCE Programmable Pipe Block Diagram

### 5.2.2 Execution Control

The Instruction Decode, Source Select, and Instruction Stall modules make up the execute stage's control logic. Collectively, these modules create the necessary control signals for the programmable pipe's functional units and detect execution hazards that require the pipe to stall and replay instructions.

#### Instruction Decode

The Instruction Decode unit expands the narrow microcode instruction into a wider decoded instruction that contains functional unit control signals. The decode module also contains the current instruction and PC registers. Instruction Stalls cause the current instruction to be replayed in the next cycle, and branch mispredictions cause a single cycle bubble in execution while the execute stage waits for a new instruction to be fetched. The output of the decoder is the decoded instruction and the current execute stage PC.

#### Source Select

The source select module routes operands to the programmable pipe's functional units based on the current instruction. A source operand may come from the general purpose registers or special registers associated with the coherent request pipe to programmable pipe interface, depending on the specific instruction being executed.

#### Instruction Stall

The Instruction Stall unit controls whether the current instruction executes and commits or must be replayed in the following cycle. Stalls occur due to functional unit hazards. The unit takes the decoded instruction as input, examines its control signals, and stalls execution if any of the possible stall conditions are met. The stall signal is routed to the fetch stage to retain the previously fetched instruction, and to the instruction decoder to replay the current instruction in the next cycle. Stalls occur when the programmable pipe must wait for a new coherence transaction from the coherent request pipe.

### 5.2.3 Register File

The Register File stores the architectural state of the programmable pipe in eight 64-bit general purpose registers (GPRs). These registers can be read and written by the microcode instructions and can be used to store temporary variables and values during execution of the microcode program.

### 5.2.4 Functional Units

The programmable pipe includes two functional units that implement instruction execution. The Branch unit manages control flow while the ALU unit implements standard RISC-style general purpose arithmetic instructions.

#### Branch

The Branch unit resolves branches and validates the fetch stage's speculative fetch. The branch unit takes the current instruction's two operands, branch operation, valid bit, predict taken bit, PC, and branch target as inputs. It then computes the result of the branch operation and determines if a misprediction occurred by comparing the branch outcome to the predict taken bit. Mispredictions result in a single cycle bubble in the execute stage and redirect the fetch stage to the proper fetch PC. The next fetch PC will either be the current execute stage PC plus one or the branch target, depending on the outcome of the branch comparison.

#### ALU

The Arithmetic Logic Unit (ALU) is a simple, 64-bit wide ALU supporting addition, subtraction, logical shifts, and bitwise operations. The supported bitwise operations are AND, OR, XOR, NAND, NOR, and negation. The ALU also supports logical negation of a single operand. The hardware ALU is purposefully simplistic to reduce complexity. Additional common operations are supported at the software level by the assembler. Software supported operations include increment, decrement, add immediate, subtract immediate, and shift immediate.

### 5.2.5 Instruction Set Architecture (ISA)

The programmable pipe effectively executes a restricted subset of the microcode-programmable coherence engine's Base ISA, listed in [Table 4.11](#), [Table 4.12](#), and [Table 4.13](#). All of the basic ALU, Branch, and Data Movement instructions operating on the general purpose registers are supported, as are limited operations on some special registers associated with the coherent request pipe to programmable pipe interface, which carries an LCE request message header. Some of the instructions from the Coherence ISA's Queue subset, listed in [Table 4.16](#), are also implemented to handle processing of the LCE request message header provided by the coherent request pipe.

### 5.2.6 Programmable Pipe Interface

The programmable pipe interfaces with the coherent request pipe using a simple status message interface. In the initial implementation of the hybrid coherence engine, the status message is a one-bit wire that is driven by bit zero of GPR zero (r0). A value of zero on this signal tells the coherent request pipe to squash the current coherence request being processed, while a value of one tells the coherent request pipe to proceed processing the request and commit the transaction in the coherence protocol. The microcode program executing in the programmable pipe must set bit zero of GPR zero appropriately for every new coherence request being processed. As shown in

Figure 5.5, the coherent request pipe state machine stalls in the Programmable Pipe Sync state until the programmable pipe sends the status message for the transaction.

The information that is communicated from the programmable pipe to the coherent request pipe and the capabilities of the programmable pipe is an important design decision with many possibilities and tradeoffs. The interface can be synchronous or asynchronous and stalling (blocking) or non-stalling (non-blocking). As implemented, the interface is synchronous and stalling, requiring the programmable pipe to provide a squash or proceed status message to the coherent request pipe for every coherence request while the coherent request pipe stalls waiting for the status message.

The decision to implement a synchronous status message interface results in two major practical considerations for the coherence engine’s functionality. First, the programmable pipe’s microcode must make a binary decision about every transaction, determining whether the transaction is allowable or not. Thus, while the mechanics of processing the coherence transaction are handled by the fixed-function protocol processing logic, the programmable pipe retains full control over the system’s functional behavior and can squash any transaction. Second, the programmable logic has a strict processing latency that must be met to avoid incurring additional transaction processing overheads. As shown in Figure 5.5, the fixed-function protocol processing logic spends only  $5+(C/2)$  cycles to perform the initial pre-commit processing of each request, assuming no replacement or invalidations. Thus, the programmable pipe has only a handful of cycles to perform its processing to avoid stalling the state machine. In practice, this may limit the complexity of programmable processing that can be performed by the programmable pipe within the initial hybrid coherence engine design.

If the programmable pipe is intended to support functionality that does not control whether each transaction should proceed or be squashed, an asynchronous non-stalling interface can be used. In this situation, it may not even be necessary for the programmable pipe to return any type of status or other message back to the coherent request pipe. Rather, the programmable pipe would simply perform its processing for each coherence request independent of the coherent request pipe, including possibly accessing memory or sending messages to other system components. If the programmable pipe’s program is unable to execute with a throughput that matches the coherence protocol processing, the coherent request pipe can be made to stall until the programmable pipe, or a buffer that feeds it requests, has space available. Alternatively, processing of some coherence requests can be skipped by the programmable pipe while the coherent request pipe continues to process all requests for protocol correctness. However, having the programmable pipe process only a subset of coherence requests means that it cannot be used to implement logic that requires visibility of every coherence request.

## 5.3 Performance Comparison

The hybrid coherence engine implements identical protocol processing logic as the fixed-function coherence engine (FSM CCE), however the organization of the two designs differs significantly. Therefore, it is important to compare the request processing occupancies and protocol processing performance of the two designs to understand the implications of these design decisions.

### 5.3.1 Request Processing Occupancy

Table 5.5 presents a comparison of the coherence request processing occupancies for the hybrid and fixed-function coherence engines. As seen in the table, the two coherence engines have nearly

Request	LCE State	Directory State	FSM CCE Occupancy (cycles)	Hybrid CCE Occupancy (cycles)
Read	I	I, S	$8 + (C/2)$	$8 + (C/2)$
		E (clean)	$10 + (C/2)$	$10 + (C/2)$
		E (dirty)	$9 + (C/2) + N$	$10 + (C/2)$
		M, O, F	$9 + (C/2)$	$9 + (C/2)$
Write	I	I	$8 + (C/2)$	$8 + (C/2)$
		S	$8 + (C/2) + (2 * S)$	$8 + (C/2) + (2 * S)$
		E, M	$9 + (C/2)$	$9 + (C/2)$
		O, F	$9 + (C/2) + (2 * S)$	$9 + (C/2) + (2 * S)$
Write	S	S, O, F	$9 + (C/2) + (2 * (S - 1))$	$9 + (C/2) + (2 * (S - 1))$
Write	O, F	O, F	$9 + (C/2) + (2 * S)$	$9 + (C/2) + (2 * S)$

Table 5.5: BP-BedRock CCE Request Occupancy Comparison - MOESIF

Program	Description
Sanity	Coherence protocol sanity check program with deliberate false sharing.
Atomic Add	Atomic (amoad.d) increment of shared global variable by all cores.
LR/SC Add	LR/SC-based increment of shared global variable by all cores.
Random Walk	Epoch-based synchronization with no data sharing.
Work Sharing Sort	Cooperative sorting of a large collection of arrays with synchronization for array selection.

Table 5.6: BP-BedRock Microbenchmark Programs

identical theoretical request processing occupancies. Both designs have baseline request occupancy costs of  $8 + (C/2)$  cycles for every request and require  $(2 * S)$  cycles to perform invalidations of cache block sharers. The two designs differ only in the case where a writeback of the target coherence block is required, which occurs when a read request is made to a block cached in the Exclusive (E) state in another cache and that cache has performed a write that silently upgraded the block to the Modified (M) state. This results in the owning cache sending a dirty writeback response to the coherence engine as the block transitions to the Owned (O) state, which is dirty and shared with a single owner. The fixed-function coherence engine incurs a one cycle cost to issue the command message and then  $N$  cycles to process a dirty writeback response while the hybrid coherence engine incurs a cost of two cycles to issue the command message and then observe the writeback has been processed by the LCE response pipe.

This analysis, however, is potentially misleading and illuminates the challenges of inferring protocol processing throughput and application performance from processing occupancies. While the coherent request pipe of the hybrid coherence engine appears to have a lower processing occupancy in this particular situation, if the state machine stalls waiting for the writeback ack signal from the LCE response pipe then it will in practice experience an overhead of one plus  $N$  cycles to issue the writeback and see the writeback response, just as the fixed-function engine experiences. This happens because the LCE response pipe will take at least  $N$  cycles to process the  $N$  beats of the writeback and forward them to the memory command network.

### 5.3.2 Micro-benchmark Performance

The coherence engine request processing occupancy comparison presented above illuminates the challenges of comparing coherence system implementations at the component level. To better understand the holistic performance of the BP-BedRock hybrid coherence engine, a set of experiments are run using microbenchmarks that stress different aspects of the coherence system. Five microbenchmark programs are tested in RTL simulation of the BP-BedRock multicore processor design with core counts ranging from one to sixteen, in powers of two. At each core count, designs with all three BP-BedRock coherence engines are tested. The five microbenchmarks are listed in [Table 5.6](#).

The Sanity program was designed as a simple smoke test of the BP-BedRock coherence system. It stripes accesses to shared global memory by all cores at a data word granularity, for example core 0 access word 0, core 1 accesses word 1, core 2 accesses word 2, and so on. This creates deliberate false sharing of cache blocks, which stresses cache block sharing in the coherence system. Every core accumulates a sum of the data words it accesses into a local variable, meaning that there are no writes occurring to the shared global memory array. This program primarily stresses the throughput of the coherence directory as it continually processes and services read requests from the caches.

The Atomic Add and LR/SC Add programs both use all cores to increment a single shared global variable a large number of times. This program stresses cache to cache transfers since every increment requires write permissions, thereby causing the cache block containing the shared global variable to be continually passed around among the cores' data caches.

The Random Walk program performs epoch-based synchronization among cores. Program execution is segmented into a large number of identical epochs during which each core executes a trivial local computation. At the end of each epoch's local computation, the cores perform a global synchronization with each other, waiting for for all cores to finish the current epoch before proceeding to the next epoch. This program stresses infrequent bursts of demand for a shared block.

The Work Sharing Sort microbenchmark uses all of the cores to collaboratively sort a large collection of small to moderate sized arrays. Each core executes an acquire-then-sort loop that first performs synchronization on a shared global variable to acquire a pointer to one of the unsorted arrays. The core then sorts the array, reading and writing the array from the shared global memory. After the array is sorted, the core repeats the loop, attempting to acquire another unsorted array for sorting. All cores execute until there are no more arrays to sort. This program stresses random synchronization overlapped with constant read and write accesses to the shared global memory. While there is no sharing of array data among the cores, each core is constantly issuing requests to the coherence directory, which puts pressure on the processing throughput of the coherence system.

[Figure 5.11](#) shows the results of these microbenchmark simulation experiments with results normalized to the fixed-function coherence engine design. For each microbenchmark, total simulation time is collected and then normalized to the FSM CCE design. These results show that the microcode-programmable coherence engine-based multicore designs exhibit consistently lower program-level performance than the FSM-based design. The hybrid coherence engine-based multicore designs exhibit consistently greater program-level performance than the FSM-based design. However, there are not clear trends across the set of microbenchmarks regarding the scalability of the coherence engines. Atomic Add and Sanity show generally degrading performance for the microcode-programmable coherence engine-based designs while LR/SC Add, Random Walk, and

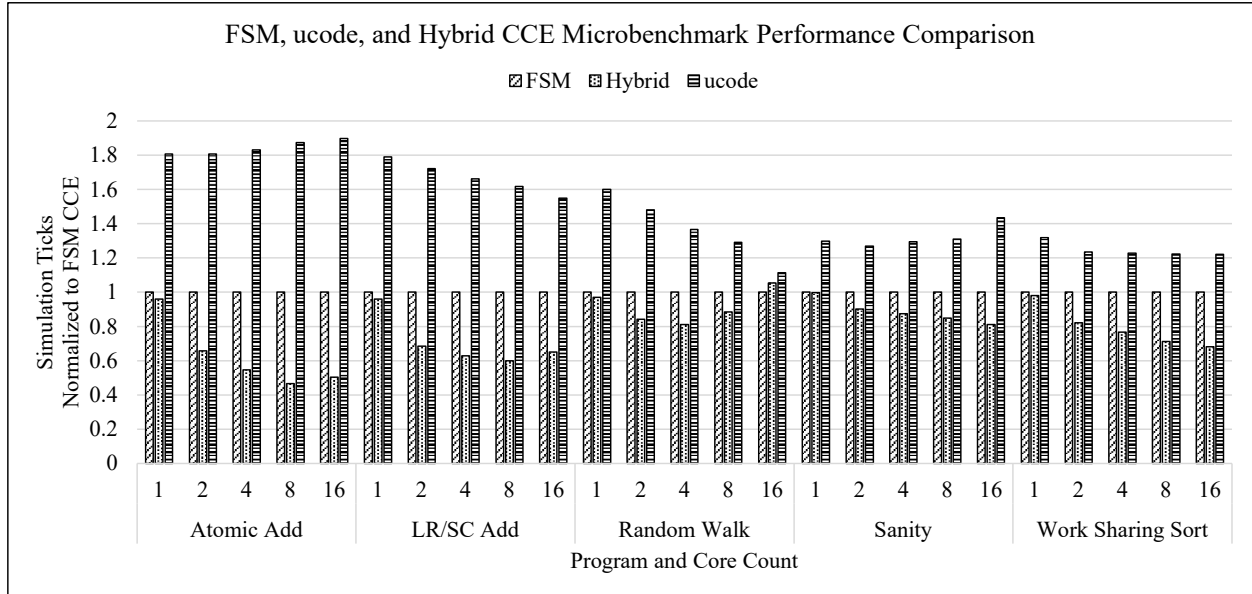


Figure 5.11: Hybrid CCE Performance Comparison

Work Sharing Sort demonstrate favorable performance scaling as the multicore core count increases. For the hybrid coherence engine, the Random Walk microbenchmark initially shows improving performance as core count increases, but then regresses when a core count of 16 is reached. The other four programs generally show favorable scaling relative to the fixed-function coherence engine design.

The results generally show that using the microcode-programmable coherence engine in the multicore results in lower application-level performance while using the hybrid engine generally results in improved performance. For the microcode-programmable coherence engine-based multicores, these results generally follow from the request processing occupancy analysis in Section 4.6. The request processing occupancy analysis shows that the microcode-programmable engine has nearly 100% request processing latency overheads, which can have a significant impact on total application performance for applications that stress the cache coherence system with frequent cache block sharing and cache to cache transfers. In contrast, the hybrid coherence engine implements nearly identical logic as the fixed-function coherence engine and has effectively identical theoretical request processing occupancy latencies. However, the microbenchmark experiments show that the hybrid coherence engine-based multicore designs have a significant performance advantage over the FSM-based designs. The hybrid coherence engine's implementation differs in subtle but important ways from the FSM coherence engine, which likely accounts for the differences in application-level performance. For example, the hybrid engine includes more buffering for inbound requests due to the use of independent coherent and uncacheable pipes and the additional request buffering provided by the request arbiter. This allows more requests to be queued up at a given coherence engine. Additionally, the hybrid engine implements a pending request queue that holds requests blocked by the pending bits while allowing newer requests targeting other way groups to proceed ahead of the blocked request. This mechanism preserves the ordering of requests targeting the same cache block but enables greater request processing throughput relative to the FSM-based coherence engine that will stall ready requests behind requests blocked by the pending bits. Collectively, these implementation details reinforce the importance of the coherence engine architecture and organization

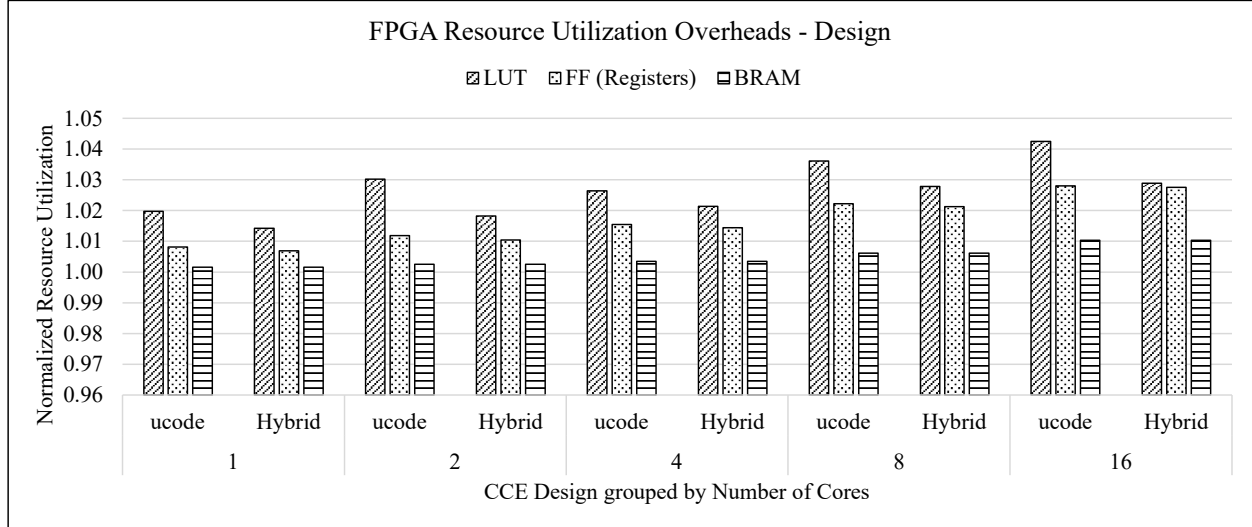


Figure 5.12: FPGA Resource Utilization Overheads - Full Design

in determining realized protocol processing and application-level performance.

## 5.4 Resource Comparison

Alongside protocol processing and application-level performance, area and resource utilization are important metrics for any processor design. As discussed in Section 4.7, the fixed-function and microcode-programmable coherence engine designs were compared in both ASIC and FPGA implementations, revealing that programmability has a small, but non-trivial resource cost. After implementing the hybrid coherence engine design, FPGA-based implementations of multicore designs leveraging all three coherence engine designs were compared again. Overall, this updated comparison reveals similar trends and overheads as the initial area and resource utilization comparisons for the FSM and ucode designs.

Figure 5.12 shows the resource utilization overheads of the ucode CCE and hybrid CCE designs at core counts ranging from 1 to 16, in powers of two. Resource utilization is recorded at the FPGA design level, which includes all logic required in the FPGA design. The complete FPGA design comprises the BP-BedRock multicore processor with one of the three coherence engine designs, PCI Express (PCIe) interface logic, AXI network interconnect blocks, FPGA host logic to control the multicore, and HBM memory controller logic. The three FPGA resources compared are the number of Lookup Tables (Total LUT), the number of flip-flop elements or registers (FF), and the number of hardened memories or block RAM elements (BRAM). The hybrid coherence engine resource utilization is normalized to a design including the hybrid coherence engine with the programmable pipe logic removed while the microcode-programmable design resource utilization is normalized to a design using the fixed-function coherence engine. The figure shows that the cost of programmability in both the microcode-programmable and hybrid coherence engines is relatively small at the overall design level. Both designs have single-digit percentage overheads for all three resource classes, which is consistent with earlier results evaluating the microcode-programmable coherence engine.

Figure 5.13 shows the resource utilization overheads at the BP-BedRock multicore design level when using either the microcode-programmable or hybrid coherence engine designs. As above,

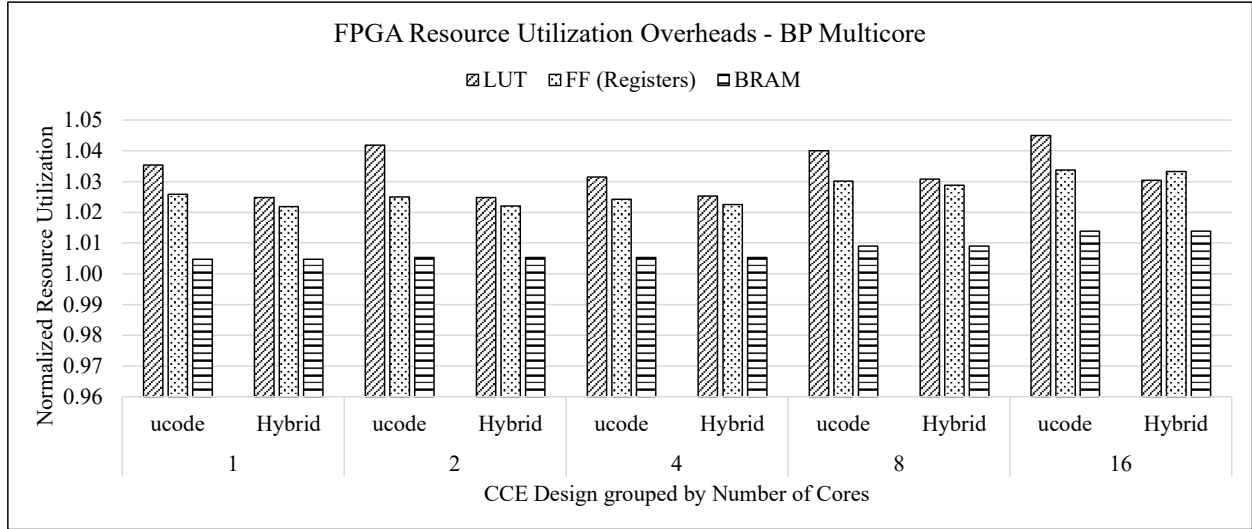


Figure 5.13: FPGA Resource Utilization Overheads - BlackParrot Multicore

the ucode CCE resource utilization is normalized to the FSM CCE resource utilization while the hybrid CCE resource utilization is normalized to a hybrid CCE design without any programmable logic (excludes the programmable pipe logic). At the multicore level of the design hierarchy, which excludes all of the peripheral system logic such as memory controllers, on-chip interconnects, and the FPGA-based processor host logic, the resource utilization overheads remain small. Overheads are still in the single-digit percentage range and are marginally lower than the overheads at the FPGA design level. This makes sense intuitively, as the peripheral logic, while providing important functionality, is still relatively minimal compared to the BP-BedRock multicore.

One important note about the FPGA resource utilization results is that FPGA implementation tools use non-deterministic algorithms. These algorithms result in different optimizations and resource utilization decisions being made depending on the total design complexity. For example, in some designs, the same logical storage element may be implemented using either LUT, flip-flop, or hardened block RAM (BRAM) resources. Therefore, the results presented do not necessarily show definitive trends of growing or shrinking overheads as the multicore processor’s core count grows. In particular, [Figure 5.13](#) shows how LUT and FF resource utilization may grow or shrink across various core counts at the BP-BedRock multicore level.

Overall, these resource utilization results confirm the earlier findings of [Section 4.7](#). The area and resource overheads required to introduce programmability into the cache coherence system are on the order of single-digit percentages when viewed at the multicore design level. Despite the significant importance of the coherence directory within the multicore in ensuring the correctness of the shared-memory system, the logic required to implement the coherence protocol is small compared to the logic and storage resources required to implement the processor pipeline and its data and instruction caches.

Data tables containing the full resource utilization numbers are provided in [Appendix E](#) for reference. Additionally, [Appendix F](#) provides screen captures of the FPGA-based implementation layouts.

## 5.5 Conclusion

The hybrid coherence engine presented in this chapter expands upon the investigations of [Chapter 4](#) to realize a coherence engine that maintains the performance of a fixed-function coherence engine design while introducing programmability to accommodate domain-specific functionality. The hybrid coherence engine design evolves the fixed-function protocol processing logic of the FSM-based coherence engine to provide additional inter-transaction concurrency. It leverages the innovations of the initial BP-BedRock coherence engines in directory organization and transaction management to preserve the low directory storage overheads and scalability of a tiled multicore implementation, while decomposing the protocol processing logic into a set of independently operating pipelines. The hybrid coherence engine architecture presents one possible method of integrating programmable logic with the coherence processing pipelines using a synchronous status message interface and discusses the tradeoffs involved when architecting the interface and interaction among the protocol processing logic and the domain-specific programmable logic. An analysis of the hybrid coherence engine in comparison to the fixed-function and microcode-programmable engines presented earlier shows that the hybrid engine's architectural enhancements result in improved protocol processing and application-level performance while retaining the low, single-digit percentage resource overheads for adding programmability to the coherence engine. These results further motivate investigating the integration of useful programmability into the cache coherence engines of shared-memory multicore processors.

# Chapter 6

## Related Work

A significant amount of research has been published on the topic of cache coherence protocols, coherence systems, and multicore RISC-V processors. Cache coherence has existed since the first multiprocessor computers included caches, and hardware-based cache coherence remains the solution of choice for nearly all modern shared-memory multicore processors. Software-based and hybrid coherence systems have been explored to a lesser extent but have received more attention recently due to the emerging popularity of GPU, manycore, and heterogeneous architectures and systems that place additional demands on the coherence and memory systems, while programmable coherence engines have been explored by a handful of prior research projects. The growing open-source hardware movement and the emergence of the RISC-V architecture has further driven contemporary research in efficient multicore processor design.

In the rest of this chapter, [Section 6.1](#) first discusses prior work on cache coherence protocols. [Section 6.2](#) describes related research spanning hardware, software, and hybrid coherence systems. [Section 6.3](#) describes past efforts involving the use of programmability within the cache coherence system and its coherence engines, the memory hierarchy, or the network. [Section 6.4](#) concludes the chapter discussing contemporary open-source RISC-V multicore processor designs and systems. Some prior works appear in more than one section as they are related to BedRock and BP-BedRock in multiple ways.

### 6.1 Cache Coherence Protocol Design

A large body of work has studied the problem of cache coherence protocol design. The topic has been of critical importance since the first multiprocessor computers with private caches attached to the processor cores were introduced. This dissertation describes the BedRock directory-based cache coherence protocol, however the focus of this dissertation is not an in-depth investigation into optimal cache coherence protocol design. BedRock draws heavily from prior research on cache coherence protocols, which makes this area highly relevant.

#### 6.1.1 The Cache Coherence Problem

An excellent contemporary survey of cache coherence is provided by Nagarajan et al. [96]. The terminology used in this dissertation is largely drawn from their overview and the reader is referred to this reference for a thorough description of the memory consistency problem, the cache coherence

problem, and their canonical solutions. Early works that described the cache coherence problem include those of Tang [119] and Censier and Feautrier [24]. Both of these papers describe a cache coherence protocol with three states, which are canonically referred to today as the MSI states. Censier and Feautrier provide an informal yet effective definition of the coherence problem, and perhaps more importantly, describe the coherence system as a set of two processes running asynchronously and in collaboration to implement the protocol. Viewing the set of coherence controllers as a collection of asynchronous processes is a common and powerful abstraction when dealing with coherence systems and remains in wide use in the literature today. This abstraction is applied to describe BedRock through its state transition and coherence protocol tables, which specify how both the cache controllers and coherence directories respond to various messages and requests.

### 6.1.2 Protocol States

The canonical set of stable coherence states used in most protocols are called the *MOESIF* states, standing for Modified (M), Owned (O), Exclusive (E), Shared (S), Invalid (I), and Forward (F). As mentioned above, both Tang [119] and Censier and Feautrier [24] effectively described three-state protocols with the MSI states. Papamarcos introduced the four-state MESI protocol, which is at times called the "Illinois Protocol" due to its author's association with the University of Illinois [104]. A year later, Katz described the Berkeley Ownership Protocol, which is equivalent to a four-state MOSI protocol [70]. The five-state MOESI protocol was proposed by Sweazey and Smith [117]. Lastly, Intel introduced the Forward state and the five-state MESIF protocol used in Intel QPI [36]. The MOESIF states can also be defined a set of four basic properties: validity, dirtiness, exclusivity, and ownership [104], [117]. In relation to these works, BedRock defines a family of coherence protocols using subsets of the MOESIF coherence states, where each state is described by the three properties of validity, dirtiness, and non-exclusivity.

### 6.1.3 Snooping versus Directory Protocols

Most protocols in use today can be classified as either *snooping* or *directory* protocols. Snooping protocols rely on all caches participating in coherence being able to observe all coherence transactions [49], [70], [104], [123]. In other words, transactions are broadcast across the communication network or shared bus to all caches in the system. Each cache takes an action in response to every transaction to maintain the overall correctness of the system. Snooping protocols have limited scalability as they typically require a shared communication bus, which quickly becomes expensive to implement as the system scales up in size. Directory protocols were introduced to overcome the scalability and bandwidth limitations of snooping protocols [3], [24], [34], [35], [42], [44], [56], [68], [77], [81], [85], [88], [111], [120], [139]. They utilize unicast, point-to-point messaging and leverage indirection through a coherence directory to maintain protocol correctness. These protocols tend to be more complex than their snooping counterparts, but their scalability and bandwidth improvements make them the preferred approach for most modern medium- to large-scale multicore processors. Directory protocols also naturally extend to inter-chip, inter-socket, and inter-node coherence systems. There are also schemes that mix snooping and directory designs [89], [108].

BedRock defines a directory protocol that is well suited for implementation on the tile-based Black-Parrot multicore architecture with small to moderate core counts. BedRock's directory design and protocol are influenced by and share similarities with the OpenSparc T1 [102] and Piranha [16]. BedRock utilizes a complete duplicate-tag directory, assumes that store misses allocate into a write-back L1 cache, and assumes the interconnection network is unordered. Additionally, the L2 cache does not participate in coherence and acts as a memory-side buffer.

## 6.2 Hardware, Software, and Hybrid Coherence

Cache coherence systems can often be defined as either hardware, software, or hybrid schemes. The emergence of heterogeneous systems and bespoke accelerators, brought about by the stalling of Moore’s Law [94], [95] and the end of Dennard Scaling [38], has resulted in the introduction of coherence systems tailored to heterogeneous systems. The driving factors in choosing a coherence system approach are the desired performance and memory system architecture of the system components. Adve et al. [1], Grahn et al. [52], and Komuravelli et al. [72] provide useful comparisons of hardware and software approaches to cache coherence. The appearance of this type of paper in each of the past three decades reveals the prevailing importance of cache coherence as researchers constantly reevaluate the best solution to this complex problem as the computing landscape changes.

### 6.2.1 Hardware-Managed Coherence

Hardware coherence schemes are by far the most common approach and are used in virtually all modern shared-memory multicore processor systems. These systems are highly specialized for the implemented coherence protocol and provide excellent performance with acceptable power and area overheads. Martin et al. effectively argue why hardware-based cache coherence has been and will continue to be the dominant coherence paradigm [86]. However, as computing systems become more heterogeneous and a broader range of applications are developed, the dominance of hardware-based coherence may not be as certain as they argue. Information about the cache coherence systems of most modern commercial multicore processors remains a tightly held secret by industry, however, from the limited published information, they all use hardware-managed coherence. Conway et al. detailed the coherence system of the AMD Opteron processor, providing rare insight into the workings of a commercial coherence system [34], [35]. An exhaustive listing of hardware schemes, protocols, and optimizations is beyond the scope of this dissertation.

### 6.2.2 Software-Managed Coherence and Scratchpads

At the other extreme, some systems manage memory and implement cache coherence, if required, completely in software. An early approach implementing fine-grain access control for shared memory was Blizzard-S [112]. This was preceded by the VMP Multiprocessor [30], which implemented coherence entirely in software, invoking software cache miss handlers when the network bus detected a coherence action was required. Similarly, Grahn et al. [51] investigate implementing the coherence directory logic entirely in software executed on a single processor without multi-threading, overlapped with hardware-based data transfers. SMTp [28], [29] extends this idea by using a hardware thread of an SMT-enabled processor to execute coherence protocol processing logic on cache misses.

The Intel Single-chip Cloud Computer (SCC) project is perhaps the most well known contemporary example of software-managed coherence [53], [55], [64], [67], [80]. Like SCC, most systems without hardware coherence rely on some form of explicit message passing for data sharing among processor cores. Another interesting example is the COMIC runtime system for the Cell BE processor, which was used in the Sony PlayStation 3 gaming console [79]. COMIC provides coherent shared memory across the two processing element complexes of the Cell BE. Software-managed coherence has also been explored for GPU devices, which have very different memory access and usage patterns than traditional CPUs [103]. Implementing coherent shared memory in software incurs large overheads or requires significant intervention from either the compiler or programmer to guarantee correctness.

Reasoning about memory correctness, both for coherence and the consistency model built atop it, remains extremely difficult and out of reach for the average programmer. Combined with the long history of hardware-based solutions in commercial products providing seamless backwards compatibility, software-managed coherence remains uncommon. BedRock proposes introducing programmability into the coherence system to enable system- or application-specific functionality as opposed to using programmability to enable arbitrary coherence protocols.

A second architecture trend that has regained popularity recently are manycore designs with scratchpad memories [37], [137]. These memories are managed purely in software and require explicit management of data movement. However, when data movement can be successfully coordinated, these architectures are highly performant and efficient. Recent work has explored techniques to introduce hardware, software, and hybrid coherence schemes for manycore architectures [6], [33], [45], [71], [125], [126]. In contrast to these efforts, BedRock’s coherence protocol targets small- to medium-scale shared-memory multicore processors, which rely on hardware-managed caches rather than software-managed scratchpad memories.

### 6.2.3 Hybrid Coherence Schemes

Hybrid coherence schemes employ dedicated coherence hardware and coherence-specific software mechanisms that either inform or control aspects of the coherence system. Compiler analysis is commonly employed and includes techniques that dictate when invalidations are required [93], [142], when coherence can be omitted for data that remains private to a single cache [39], or provide specialized hardware to accelerate a software protocol [11]. The MIT Alewife system can track between zero and five sharer caches in its limited pointer directory, falling back to software when the pointers are exhausted [2], [4], [25], [26], [32]. Another common approach relies on programmer annotations or restricted memory models [31], [62], [63], [132]. In comparison to existing hybrid hardware-software schemes, BedRock utilizes software to control the coherence directory. Application and runtime code can remain completely unaware of the microcode program controlling the directory. The programmability of the directory can be exposed to software, whether firmware, operating system, or runtime/application, to implement system- or application-specific features, however it can also be completely hidden from any level.

## 6.3 Programmability in the Coherence System

The core topic of this dissertation is the feasibility and design of a programmable cache coherence engine for modern shared-memory multicore processors. Programmability within the cache coherence system has been explored in the past, with the majority of prior work occurring during the emergence of distributed shared-memory multiprocessor computers. A primary motivation for revisiting this topic is that the computing landscape has changed significantly, in terms of both applications and technology, since the topic was last examined in depth. Compared to the programmable protocol engine research of thirty years ago that was primarily focused on supporting multiple communication models, the design described in this dissertation focuses on supporting system- or application-specific customization through the programmable coherence engine. Some of the benefits and drawbacks of programmable controllers are evaluated in [91], [92]. Their key findings are reconfirmed by the work in this dissertation, namely that reducing protocol processing occupancy in the coherence controllers and specializing the controllers for coherence are key to achieving performance competitiveness with hardware-only implementations.

### 6.3.1 Software-Based Protocol Handlers

As noted in [Section 6.2](#), cache coherence protocols have been implemented using both hardware and software mechanisms. The Blizzard-S machine [112] relies on instructions inserted into programs before shared-memory access to provide fine-grain access control. The VMP Multicore processor [30] relied on simple hardware state machines to invoke software protocol handlers when coherence actions were required as detected by communication on the shared bus. Similarly, Grahn et al. [51] and SMTp [28], [29] implement coherence protocol handlers in software that execute on the main processor core, whether single- or multi-threaded. Later systems, like MIT Alewife [2], [4], [32] with LimitLESS directories [25], [26], relied on software protocol handlers to manage exceptional conditions in the protocol, for example when the available encoding for limited sharers becomes oversubscribed. Despite the use of software protocol handlers, these projects did not focus on how the programmability and flexibility of software handlers could be used to support a wide variety of coherence protocols or to enable system-specific functionality. In contrast, the research described in this dissertation investigates the feasibility of including programmability in the coherence system for the explicit purpose of enabling non-protocol functionality.

### 6.3.2 Shared-Memory Multiprocessors

During the emergence of shared-memory multiprocessors, a number of projects investigated the use of programmability in the coherence, memory, and interconnect systems of multiprocessor designs. These included the Sun S3.mp [43], [98], [99], Wisconsin Typhoon [109], Sequent STiNG [83], Stanford FLASH [61], [78], and Piranha [16] machines. These machines primarily focused on solving one of two problems: providing inter-node coherence or enabling multiple inter-node communication paradigms within a single system.

#### Sun S3.mp

The Sun Microsystems Sun Scalable Shared-memory MultiProcessor (S3.mp) [43], [98]–[100] is a cache-coherent non-uniform memory access (CC-NUMA) multiprocessor with distributed shared memory. It is constructed by interconnecting commodity workstations using distributed directories and point-to-point communication between workstation nodes. Each S3.mp node includes multiple processor cores that are kept coherent using snooping-based coherence mechanisms, a portion of the multiprocessor’s main memory, a memory controller, and an interconnect controller. Unique characteristics of the S3.mp machine are that it has no preferred or fixed network topology, an internode cache of programmable size that is carved out of the main memory storage, and it relies on microprogrammed and multithreaded coherence protocol engines.

The memory controller on each node includes a remote memory handler (RMH) and remote access server (RAS) that handle requests to and from other nodes in the system, respectively, and collectively implement the cache coherency protocol among nodes in the multiprocessor. Both the RMH and RAS are implemented using identical microcode-programmable protocol engines. Each engine includes input and output state machines and buffers that accelerate message send and receive operations, as well as managing the creation of request threads based on the arriving messages. The microcode engine, called a microcode sequencer, executes a program that operates on one request thread at a time, and threads can be context switched with no latency penalty since all state for all threads is stored in separate hardware registers. Like BP-BedRock, the microcode engines execute an instruction set customized for cache coherence protocol operations. S3.mp’s protocol engines include message send instructions that offload the arbitration and data transfer of outbound pro-

tol messages from the microcode engine to the message send hardware. Unlike BP-BedRock, the coherence directory is stored in main memory rather than dedicated hardware directory storage.

### Wisconsin Typhoon

Wisconsin Typhoon is a hardware platform that implements the Tempest interface for low-level communication and memory system mechanisms [109]. Tempest allows programmers and compilers to directly control hardware-provided communication mechanisms such that both message passing and shared-memory can exist on the same system and be used in the same program. Typhoon is a proposed hardware system architecture that implements message passing and shared-memory communication using a fully-programmable, user-level processor in the network interface within each processor of the multiprocessor system.

Typhoon, like S3.mp, comprises workstation-like nodes connected with a point-to-point interconnection network. Each node includes processors, a memory controller, main memory, and a custom network interface processor (NP). The network processor is an off-the-shelf commodity SPARC integer processor with its own instruction and data caches and translation lookaside buffer (TLB). The NP connects the processor node and its portion of main memory to the interconnect network and the other nodes in the system. This processor is tightly-coupled to the network interface, enabling efficient handling of inbound network messages. The code running on the NP is managed using a dispatch loop that invokes a protocol or message handler based on the arriving message and handlers run to completion once invoked, similar to how BP-BedRock’s microcode examines arriving request messages and runs to completion based on the message type and current directory state. It achieves low-overhead message send and receive using memory-mapped register accesses from code executing on the NP, however, unlike BP-BedRock it lacks specialized or integrated message send and receive functional units. Typhoon also does not include any coherence-specific hardware, for example a coherence directory.

### Stanford FLASH and the MAGIC Node Controller

BP-BedRock is most similar to the MAGIC node controller of the Stanford FLASH multiprocessor [57]–[61], [77], [78]. MAGIC is a protocol-processing specialized MIPS processor and includes ISA extensions similar to those found in BP-BedRock. Both BP-BedRock and MAGIC are effectively small, specialized integer-only RISC ISA engines. Unlike MAGIC, which is designed as a generic protocol processor, BP-BedRock’s programmable engine is designed to efficiently implement the BedRock coherence protocol while enabling unique system- and application-specific functionality via programmable routines executing alongside protocol processing. BP-BedRock is not designed to support arbitrary coherence protocols or shared-memory solutions. BP-BedRock includes dedicated directory storage and a microcode instruction memory instead of general purpose instruction and data caches. Both designs use specialized RISC instruction sets with similar extensions for bit manipulations and message send and receive operations, however, BP-BedRock also includes specialized instructions for reading and processing the coherence directory and to perform efficient flag-based control flow. Neither BP-BedRock or MAGIC supports virtual memory or interrupts. [Table 6.1](#) provides a qualitative comparison of BP-BedRock and MAGIC.

[Table 6.2a](#) and [Table 6.2b](#) provide quantitative comparisons between BP-BedRock and a MIPS-based protocol processor like MAGIC. [Table 6.2a](#) compares the latency of selected directory operations such as reading and processing a duplicate-tag directory, issuing invalidations, and control flow operations. BP-BedRock’s specialized functional blocks enable highly efficient coherence direc-

Property	MAGIC	BP-BedRock
Base ISA	MIPS	Custom RISC
ISA Extensions	Bitfield Op	Directory Rd/Wr
	Set/Test Bit	Flag Op
	Tx/Rx Message	Tx/Rx Message
GPRs	32 x 64-bit	8 x 64-bit
Data Cache	32 KiB off-chip	none
Instruction Cache	16 KiB on-chip	1.5 KiB
Data Buffers	2 KiB 6-port SRAM	none
Directory Memory	none	3.625 KiB
Protocol Agnostic	yes	no
Message Passing	yes	no
Coherence Type	Distributed Directory	Distributed Directory
Coherence Domain	Inter-node	Multicore
Coherence Model	All memory blocks	Only cached blocks
HW Address Translation	no	no
Interrupts	no	no
Open Source	no	yes

Table 6.1: Architectural Comparison of BP-BedRock and MAGIC

tory reads, while a MIPS-based protocol processor such as MAGIC requires a significant number of instructions to execute the same operation. Likewise, BP-BedRock’s specialization allows it to issue one invalidation command per cycle and consume one response per cycle, whereas a MIPS-based processor would require executing these routines as tight loops with approximately 10 instructions per send or receive operation. Table 6.2b shows the processing occupancy in cycles at the coherence directory for common requests. The table assumes the requesting cache does not have a valid copy of the block, which is currently in the coherence state listed in parentheses at the directory. BP-BedRock’s specialized logic for reading and processing the directory, issuing invalidations, and executing control flow decisions based on the coherence-specific MSHR control flags give BP-BedRock a significant advantage over the MIPS-based execution of MAGIC.

The Stanford FLASH machine was also used to investigate the inclusion of non-coherence logic within coherence protocols. FlashPoint [87] incorporates performance monitoring functionality into a cache coherence protocol by leveraging the existing programmable protocol handlers provided in the MAGIC node controller. Similar to BP-BedRock, FlashPoint argues that programmability in the cache coherence or memory system can be used to implement system-specific functionality. The authors find that memory performance monitoring can be introduced with less than 10% slowdown over an unmonitored execution. BP-BedRock’s hybrid coherence engine design illustrates how the interface between the coherence processing logic and the programmable engine impacts whether system-specific functionality, such as memory performance monitoring, may impact protocol processing or application performance.

### Sequent STiNG

STiNG [83] is a cache-coherent non-uniform memory access (CC-NUMA) multiprocessor from Sequent Computer Systems, Inc. A complete STiNG system comprises multiple processor nodes,

Operation	BP-BedRock	MIPS (MAGIC)
Directory Read	$2 + C/2$	$20 * C$
Invalidation	$2 + (2 * S)$	$15 * S$
Branch	1	1
Flag Branch	1	-

(a) Selected operation latency in cycles. C is the number of cores and S is the number of sharer caches.

Request (Directory State)	BP-BedRock	MIPS (MAGIC)
Read (I)	16	184
Read (S)	30	184
Read (M)	36	219
Write (I)	27	184
Write (S)	$28 + (2 * S)$	$184 + (15 * S)$
Write (M)	31	198

(b) Request Occupancy in cycles, assuming 8-cores and an invalid block at the requester. The coherence state in parentheses indicates the state of the block at the directory. S is the number of sharer caches.

Table 6.2: Processing Latency and Occupancy Comparison of BP-BedRock and MAGIC

each of which contains four processor cores. The nodes are interconnected with a scalable coherent interconnect based on the Scalable Coherence Interface (SCI). Coherence within a single node is provided by a snooping-based MESI coherence protocol, while coherence between nodes is implemented using a directory-based protocol. The inter-node coherence controller is implemented using a programmable protocol engine within the SCI Cache Link Interface Controller (SCLIC) ASIC. STiNG’s use of a programmable protocol engine was motivated in part by the MAGIC node controller in the Stanford FLASH multiprocessor, as well as the desire to implement protocol bug-fixes or more efficient protocols post-implementation.

The programmable protocol engine is a three-stage pipelined processor with 64-bit wide instructions. The instruction set includes custom bit field operations. The engine supports twelve independent tasks that are time-multiplexed for execution on the pipeline. At high-level, the microarchitecture of the SCLIC programmable protocol processor is quite similar to both MAGIC and BP-BedRock’s microcode-programmable engine. Like BP-BedRock, each node includes dedicated storage for coherence directory data. To reduce tag access overheads, the SCLIC includes a small cache that holds directory tag information for transactions in progress. In contrast, BP-BedRock reads the directory once per transaction and then processes the output into an encoded format that can be easily operated on for control flow operations during protocol processing. The researchers also come to similar conclusions as prior work and BP-BedRock, namely that increased protocol processing occupancy results in reduced application performance. Additionally, they identify techniques to reduce occupancy, such as optimized microcode, co-designing coherence protocols with the microcode to reduce program size, and specialized hardware logic to accelerate common instruction sequences. BP-BedRock applies similar techniques through its specialized hardware blocks for coherence protocol processing that are accessed via the coherence ISA.

## Piranha

Piranha [16] is primarily a single-chip multiprocessor architecture, however it includes on-chip features that enable building scalable multi-chip multiprocessor systems. Each single-chip multiprocessor includes eight processor cores, memory controllers, and specialized Home and Remote Engines to accelerate inter-chip shared-memory and cache coherence operations. A multiprocessor Piranha system also includes I/O nodes, which participate in the global coherence protocol and

contain home and remote engines, too. The home engine manages requests for memory that resides on the node, and the remote engine handles requests for memory on other nodes in the system. The organization of Piranha’s home and remote protocol engines is derived directly from S3.mp. They are microcode-programmable engines that comprise input and output buffers and state machines as well as a microcode-programmed execution unit. The protocol engines execute a custom instruction set including message send and receive, data movement, and test and set operations. Threads of execution are multiplexed on the protocol engine using an interleaved execution paradigm that switches between active threads every cycle.

Piranha’s inter-node coherence protocol is an invalidation-based directory protocol, similar to BedRock. Like BedRock, Piranha’s protocol avoids the use of negative acknowledgment messages and supports unordered networks. However, like canonical protocols, invalidation messages are sent to the requesting node rather than to the managing directory. The microcode-programmable engine design is similar to BP-BedRock in that it executes a custom instruction set tailored for protocol operations. The instruction set also includes instructions that can behave as multi-way conditional branches that accelerate control flow decisions, similar to how BP-BedRock’s flag-based branches enable efficient control flow during request processing. As with S3.mp, Piranha does not include dedicated coherence directory storage and instead relies on storing the directory information in unused ECC bits of the main memory. Overall, Piranha’s protocol engines, like S3.mp’s are more specialized and less general-purpose than BP-BedRock’s or MAGIC’s node controller.

### 6.3.3 Programmability in the Core, Memory, or Network

Beyond research into programmable engines within shared-memory multiprocessors as described above, other recent projects have investigated programmability throughout the processor core, memory hierarchy, and interconnect.

#### Programmability in the Core

Programmability has been explored within traditional processor cores, for example to support application-specific functionality or execution profiling. Zilles et al. [143] proposed the inclusion of a microcode-programmable co-processor for execution profiling alongside an out-of-order CPU core pipeline microarchitecture. Instructions of interest are tagged in the core pipeline and then pushed to a sample buffer at retirement before being processed by routines executing on the profiling co-processor. DySER (dynamically specialized execution resources) [50] integrates a specialized circuit-switched heterogeneous array of compute elements as a functional unit in the CPU’s core pipeline, enabling application-specific functionality to be configured and invoked using special instructions. The programmable compute array can be reconfigured dynamically during runtime to accelerate specific execution patterns that are repeated within an application. Similarly, PSM (post-silicon microarchitecture) [73] and PFM (post-fabrication microarchitecture) [74] propose the integration of reconfigurable fabrics, like FPGA or CGRA, with a CPU’s core pipeline. The reconfigurable fabric can be programmed to realize new instruction or accelerator functionality after design or fabrication, enabling the device to be specialized for applications or domains as needed. The custom logic is interfaced directly with the core pipeline and appears much like existing hardened functional units from the programmer’s point-of-view. Despite focusing on different subsystems than BP-BedRock, these works share common insights and motivation with BP-BedRock. The inclusion of user-defined, application-specific functionality is an important feature for future computing systems, whether in the core itself or in the memory or interconnect systems.

## Programmability in the Memory Hierarchy

A common theme in contemporary research focuses on accelerating data movement and bringing compute closer to memory. A significant body of work focuses on prefetching data from memory, and a subset of work investigates the use of programmability within the prefetch engines. A few approaches include event-triggered programmable prefetching [5], DROPLET (data-aware decoupled prefetcher) [17], RnR (Record-and-Replay) [138], and Prodigy [118]. A common theme across this research is using programmability to improve prefetching for irregular and graph applications for which existing hardware-only prefetchers are ill-suited. These works also propose various hardware-software interfaces that expose the programmable prefetch engines to software, including user-level applications, allowing programmers to direct the prefetch algorithms or behavior.

Another interesting direction of research is exemplified by *täkō* [113], which leverages programmability to accelerate data movement. *täkō* is a polymorphic cache hierarchy enabling programmers to define software callbacks that are triggered on cache misses, evictions, or writebacks to manage data movement between the cache and other levels of the memory hierarchy. The callbacks are executed on a programmable spatial dataflow engine located near a cache, for example at the private L2 cache of each core. These callbacks can be used to manipulate data as it is moved throughout the memory hierarchy, such as compressing or decompressing data items or reshaping data structures to optimize for memory access locality.

Like BP-BedRock, these works share the goal of exposing programmability to the system- or application-programmer to enable custom functionality. An interesting avenue of research for BP-BedRock is investigating whether programmability in the coherence engine could be used to perform prefetching or data movement and manipulation, either directly or by issuing commands to other specialized engines like those proposed in the related works.

## Programmability in the Network

Research into programmable packet processing engines for networks and interconnects has continued beyond the emergence of shared-memory multiprocessors. Two examples of this research are PSM (programmable state machine) [127] and FPE (FSM-based Processing Engine) [114]. These works make similar observations as BP-BedRock related to the tradeoffs between fixed-function or programmable hardware. PSM employs a four-stage pipelined RISC processor executing an instruction set customized for packet processing and including special registers that expose packet information directly to the programmable engine. This processor can interact with other state machines or specialized packet processing hardware using register-based control interfaces. These design decisions are also found in BP-BedRock, as ISA specialization and hardware acceleration of critical path operations is necessary for both generic network packet processing and coherence protocol processing. FPE is a programmable packet processor designed for integration in a network co-processor. As in BP-BedRock, it implements a 2-stage fetch-execute pipeline and specialization of the packet processor results in significant performance improvement compared to a general-purpose RISC processor implementing the same functionality. FPE also enables multi-way branch evaluation, recognizing the importance of minimizing control flow overheads similar to BP-BedRock’s use of flag-based branching.

Programmable packet processors share many similarities with BP-BedRock in terms of both purpose and design. In one view, a directory-based coherence protocol is simply a specialized communication protocol. Coherence protocols are typically carried as payloads of the underlying interconnect packets and generally do not consider routing or control flow processing. However, every coherence

message requires packet processing to detect the type of protocol message and take appropriate actions as dictated by the protocol rules. Therefore, while the type of processing may differ between a generic network packet processor and BP-BedRock’s coherence message processing, the underlying architectural and microarchitectural designs are often quite similar.

## 6.4 Open-Source Multicore RISC-V Processors

The emergence and rapid growth of the open-source hardware movement and the RISC-V instruction set architecture are driving a new age of computer architecture. BlackParrot and BP-BedRock are an important part of this movement, and are closely related to many ongoing efforts within it. This section outlines how BP-BedRock relates to many contemporary open-source processor and system efforts, with a focus on those implementing the RISC-V architecture. All of these projects make important contributions within the open-source hardware and RISC-V processor communities. However, BP-BedRock stands apart for its investigation into both cache coherence for open-source multicore processors and programmability within the cache coherence system.

### 6.4.1 RISC-V, Rocket Chip, BOOM, and Chipyard

The RISC-V Instruction Set Architecture (ISA) [9], [128], [129] emerged from the University of California, Berkeley in 2010 and has since become a driving innovation within the open-source processor and hardware movement. The RISC-V ISA defines a processor architecture, including allowable memory consistency models, however, it does not prescribe how to implement the architecture or consistency model.

The creators of RISC-V also developed multiple open-source processor implementations and surrounding infrastructure to support researchers adopting the new architecture. Rocket Chip [10] is an open-source System-on-Chip (SoC) generator that provides implementations of both in-order and out-of-order processor cores called Rocket and BOOM [21]–[23], [141], respectively, as well as generators for the uncore and on-chip networks required to construct an SoC. Chipyard [8] expands on the work of Rocket Chip and provides a framework enabling designers to construct and evaluate complete hardware systems and SoCs. Chipyard relies on RTL generators, including Rocket Chip, to provide implementations for a system’s hardware components. Rocket Chip and Chipyard implement on-chip networks using the TileLink network architecture [115]. TileLink comprises a set of links to communicate between two agents, where each link is a collection of one-way channels carrying messages of the same priority. The TileLink Cached (TL-C) protocol supports coherent caches. Chipyard also includes the Constellation [140] network-on-chip (NoC) generator, which provides virtual-channel wormhole-routed NoC implementations. The generated network is a protocol-independent transport layer capable of carrying arbitrary system- or application-level protocols, including cache coherence protocols. No ordering is maintained between packets carried on a single flow in a Constellation network, which may break ordering assumptions in coherence protocols, requiring endpoint buffering to recover ordering.

BP-BedRock builds on the contributions of RISC-V while taking a different approach than Rocket Chip and Chipyard, differing from these works in a few important ways. First, BP-BedRock is implemented entirely in SystemVerilog, making it easy to understand, integrate, and debug in system designs using standard open-source or commercial EDA tools. In contrast, Rocket Chip and Chipyard rely on Chisel [12], an open-source hardware construction language that designers can specify entire SoC configurations that are compiled into synthesizable Verilog RTL. While Chisel raises the

level of abstraction for hardware designers, it is not yet widely adopted by hardware designers and the generated Verilog RTL is not as easily understood as human-written SystemVerilog RTL.

Second, BP-BedRock focuses on building a single-chip shared-memory cache coherent multicore while Rocket Chip and Chipyard focus on generating cores and complete SoCs. BP-BedRock provides a parameterized multicore architecture and explores the cache coherence system in depth, including the introduction of programmability. In comparison, Rocket Chip and Chipyard generate cores and SoCs, using TileLink to provide shared memory with cache coherence across tiles. However, they do not investigate cache coherence or programmability in the coherence system in depth. The default network generator connects tiles using a crossbar network, which becomes very costly as system size increases, however the integration of Constellation provides an interesting avenue for exploring SoCs with unique network topologies. BP-BedRock relies on BlackParrot’s tile-based architecture and implements a 2-D mesh network across tiles with wormhole-routed networks.

Third, BedRock provides a complete coherence protocol while TileLink Cached (TL-C) provides a specification of only the network channels and messages to support an implementation-defined coherence protocol. TL-C specifies an interconnect protocol defining the available memory access operations and channel messages, but it requires an implementation-defined coherence policy defining how cache blocks and permissions are transferred among agents in the system. TL-C employs five-channel links that can be used to implement five-phase messaging and, therefore, five-phase coherence protocols. It also does not prescribe the use of a coherence directory to maintain coherence among agents. An Inclusive Cache [66] generator for Rocket Chip provides an inclusive last-level cache that provides coherence using invalidation-based coherence with a complete coherence directory integrated with the cache tag storage. In contrast, BedRock is a fully-defined four-phase, four-network invalidation-based directory protocol, and BP-BedRock provides a complete implementation of the BedRock policy within a tiled shared-memory architecture. BP-BedRock provides a four-phase protocol and the network implementation to carry protocol messages between the cache controllers and coherence directory.

#### 6.4.2 Ariane/CVA6 and PULP

CVA6 (formerly known as Ariane) [136] is a 64-bit RISC-V application-class processor implementing the RV64GC ISA variant using a single-issue in-order commit pipeline. It was originally developed as part of the PULP (Parallel Ultra Low Power) Platform [144] at ETH Zürich. CVA6 itself does not define any cache coherence mechanisms, rather it focuses on the design and implementation of the processor core and its private caches. BlackParrot and CVA6 are very similar in implementation and philosophy. Both cores are open-source, implemented in SystemVerilog, have private virtually-indexed physically-tagged (VIPT) L1 instruction and data caches, and have AXI interfaces to memory. However, CVA6 does not natively support cache coherence or multicore implementations, whereas BP-BedRock is explicitly focused on the design and implementation of a cache-coherent BlackParrot shared-memory multicore processor.

The PULP (Parallel Ultra Low Power) Platform [144] is an open hardware platform started by ETH Zürich, originally focused on low-power, energy-efficient architecture research. Over time, the scope of the project has grown to include high-performance platform design and research. Whereas BP-BedRock focuses on the implementation of a single-chip shared-memory cache-coherent multicore, most of the PULP Platform projects focus on heterogeneous platform and domain-specific accelerator research. Both the HERO [75], [76] and Occamy [105] projects, for example, include a single CVA6 core that acts as a host processor for the chip’s accelerator fabric. The Manticore [137]

manycore conceptual architecture, which preceded the Occamy project, proposed using a quad-core CVA6 multicore on each chiplet as a host core, however this was never realized.

CVA6 has also been included in a number of other projects, ESP [20], [84], OpenPiton [13], [15], BYOC [13], [14], and Chipyard [8], demonstrating its success as a high-quality, user-friendly RISC-V implementation. Many of these projects are described in this section.

## A Consistency-Directed Cache-Coherent CVA6 Multicore

Recently, CVA6 was used to construct a multicore processor that relies on a consistency-directed coherence algorithm [90]. In contrast to the consistency-agnostic coherence protocol employed by BP-BedRock, consistency-directed protocols rely on explicit self-invalidation and writeback of cache blocks and memory data at programmer-defined synchronization points. The promoted benefit of these protocols is reduced coherence protocol complexity, since the burden of orchestrating data synchronization and coherence is shifted from the hardware-implemented protocol to the software executing in the system. However, there is often a performance tradeoff associated with this approach because it generally requires all cache lines to be invalidated and any dirty lines to be written back to the shared LLC or memory whenever a synchronization point is reached. In many applications, synchronization is frequently required.

In comparison to BP-BedRock’s sequentially consistent model, the consistency-directed CVA6 multicore aims to implement the RISC-V Weak Memory Ordering (RVWMO) memory consistency model. This model allows more load and store reorderings than are permitted in BP-BedRock, and notably, the SWMR invariant need not be maintained. Like BP-BedRock, the CVA6 multicore maintains coherence among the private L1 caches, however the implemented design was only explored up to four cores whereas BP-BedRock can scale to at least 16 or 32 cores. Each CVA6 core is connected to a shared AXI crossbar, and all cores access a unified shared memory that is also connected to the crossbar. A dual-core platform was synthesized on an FPGA to test booting a Linux operating system and running programs from the Splash-3 [110] benchmark suite. This design was compared to a similarly configured OpenPiton-based design using CVA6 cores, which maintains coherence using a directory-based protocol that shares similarities with BP-BedRock. Their experiments show an application-level performance overhead between 0% and 66% for the Splash-3 programs relative to the OpenPiton-based design, demonstrating the high performance overheads of consistency-directed coherence when synchronization events are common. Relative to a CVA6-based design without coherence state tracking, consistency-directed coherence has an area cost between 1.6% and 3.2% of total core area, although it is likely possible to reduce this further with better memory macro optimization. These results validate BP-BedRock’s decision to employ a consistency-agnostic coherence protocol.

## Culsans

Culsans [122] is another recent project investigating the design of a CVA6-based multicore processor. Culsans defines a tightly-coupled shared-memory multicore with a snooping-based cache coherence protocol. The cache coherence system implements a MOESI protocol using Arm’s AMBA ACE [7] specification. A Cache Coherency Unit (CCU) designed for small core counts, between two and four cores in the multicore, snoops the AXI crossbar connecting the processor cores with the last-level cache and main memory. Coherence is maintained among the private caches of the two to four cores in the system, and the LLC does not participate in the coherence protocol. The design is implemented in industry-standard SystemVerilog RTL and is entirely open-source.

Culsans provides an interesting point of comparison for BP-BedRock since it investigates the overheads of directory-based coherence in low core count multicores. Culsans claims significant speedups relative to a dual-core CVA6/OpenPiton-based multicore, with up to 33% performance uplift for programs from the Splash-3 benchmark suite, and a 16% performance uplift on average. The performance uplift comes from the tight coupling of snooping-based coherence, which reduces indirection and latency in the coherence protocol compared to the directory-based OpenPiton implementation. The CCU has an area overhead of less than 2% of total design area. Similar to BP-BedRock, Culsans is open-source, implemented in SystemVerilog RTL, and focuses on the design and implementation of a tightly-coupled single-chip shared-memory multicore architecture. However, Culsans' snooping-based coherence is limited to a maximum of four cores, while BP-BedRock easily scales to 16 to 32 cores. Culsans' performance uplift over an OpenPiton-based design is not surprising, as integrating CVA6 into OpenPiton requires an additional layer of cache hierarchy and the OpenPiton tiles are not tightly-coupled. BP-BedRock occupies a middle point between these two designs, using directory-based coherence to scale to larger core counts than Culsans and with cores that are more tightly coupled than the manycore tiles in OpenPiton.

### 6.4.3 ESP

ESP [20] is an open-source heterogeneous SoC research platform, enabling full-stack heterogeneous SoC research using agile design methodologies. ESP relies on a tile-based architecture to compose SoCs with various processor core, accelerator, memory, and peripheral or auxiliary device tiles. Tiles are connected by a multiplane NoC [135], and the NoC can be auto-generated to construct a system with processors, accelerators, and a distributed memory hierarchy. Tiles are encapsulated into shells and sockets that manage the tile's NoC interfaces and implement platform services. ESP aims to realize system-level design using SystemC rather than RTL, thereby raising the level of design abstraction for low-level hardware design to higher-level system design. It relies on high-level synthesis (HLS) techniques to explore implementations of the IP blocks and system components. The use of system-level design techniques and SystemC provides fast full-system simulation of virtual platforms, enabling software design and bring-up.

ESP has been extended to support cache-coherent multicore SoC designs using CVA6-based processor tiles [84]. The baseline ESP design is extended to enable coherence between the private write-back L2 caches on processor and accelerator tiles and the distributed shared LLC on memory tiles. The AXI Coherency Extensions (ACE) were used to implement invalidations between the private L2 cache and the CVA6 processor's L1 caches. The coherence protocol is a directory-based MESI protocol extended to support accelerators sending requests directly to the LLC either with or without coherence enabled. It assumes and requires point-to-point ordering of messages on the NoC and uses a three network protocol with request, forward, and response message classes. The platform has been further extended to explore cache coherence and memory hierarchies for heterogeneous systems and accelerators [47], [48]. Three common types of coherence for accelerators are defined, including non-coherent, LLC-coherent, and fully-coherent, and the baseline coherence protocol is extended with accelerator-specific actions.

BP-BedRock and ESP differ largely in their project scope and focus. Both projects employ agile design methodologies, are open-source, and create cache coherent multicore systems. The cache coherence systems of both ESP and BP-BedRock employ directory-based protocols. While BP-BedRock maintains coherence among the private L1 caches of each processor core, ESP provides coherence among a distributed LLC in the memory tiles and private L2 caches in the core and accelerator tiles. ESP explores implementing cache coherence among heterogeneous components,

but does not explore any aspects of programmability within the coherence system. The ESP approach is more similar to OpenPiton than BP-BedRock, and a key focus of the project is providing infrastructure to integrate cores or accelerators into large, tiled, heterogeneous manycore SoCs. ESP also relies on SystemC implementations and HLS methodologies to raise the level of design abstraction, whereas BP-BedRock is implemented entirely in SystemVerilog RTL. Although HLS and system-level design methodologies are attractive, they remain less supported than RTL-based design flows in open-source and commercial EDA tools.

#### 6.4.4 OpenPiton and BYOC

OpenPiton [13], [15], [54] is an open-source manycore research platform from Princeton University. The project’s original motivation was providing a framework for building large, scalable manycore prototypes in academia. The OpenPiton architecture is a tiled manycore, relying on a 2D-mesh NoC and supporting a distributed directory-based coherence protocol. At a high-level, the manycore comprises chips and chipsets. A chipset includes I/O, DRAM, and NoC routers, and each chip may be a grid of tiles. Each tile includes a processor core, private cache, slice of the distributed L2 cache, and connections to the manycore NoC. The original design employed modified OpenSparc T1 cores [102], but other cores including CVA6 and BlackParrot have since been integrated with OpenPiton.

Each tile in OpenPiton includes a private L1.5 cache and a slice of the distributed L2 cache, with the L1.5 cache originally serving to convert from the OpenSparc T1 L1 cache’s writethrough interface to a writeback interface. Cache coherence is maintained among the L1.5 and L2 caches in the system using an invalidation-based directory protocol with the MESI coherence states. The memory subsystem implements a TSO memory consistency model, as is found in the OpenSparc T1. The coherence directory is integrated into the L2 cache, and the L2 cache is inclusive of the private L1.5 and L1 caches found on each processor tile. The coherence protocol is implemented on top of three physical NoCs that provide point-to-point ordering guarantees. The NoC and coherence protocol are co-designed, with the NoC using 64-bit physical channels and protocol messages defined as sequences of 64-bit NoC flits. The protocol utilizes 4-step message communication, supports silent eviction of clean (Exclusive or Shared) cache blocks, and does not provide acknowledgments to dirty writebacks.

BYOC (Bring Your Own Core) [13], [14] extends the OpenPiton architecture to enable the construction of heterogeneous-ISA manycores. Supported ISAs include SPARCv9, RISC-V, and x86. Like OpenPiton, BYOC is fully open source and implemented in SystemVerilog RTL. The core building blocks of BYOC are the same as OpenPiton, however BYOC precisely defines an interface between arbitrary-ISA processor cores and the memory system through a Transaction-Response Interface (TRI). Any core or accelerator that conforms with the TRI receives a private cache and inclusion in the system-wide cache coherence protocol. The BYOC memory system provides the NoC, routers, last-level cache, and a BYOC Private Cache (BPC) implementing the TRI. The coherence protocol and system implemented by BYOC is largely identical to those found in OpenPiton with coherence maintained among the BPC and LLC caches. The LLC and BPC in BYOC correspond to the L2 and L1.5 caches found in OpenPiton, respectively.

OpenPiton and BYOC share many similarities with ESP, and differ from BP-BedRock in many of the same ways. While the focus of BP-BedRock is on the design and implementation of a single-chip multicore processor, OpenPiton and BYOC focus on the design of highly-scalable manycore systems. However, BP-BedRock and OpenPiton/BYOC share similarities in regard to their coherence

protocols. Both designs implement directory-based coherence and have distributed directories. In OpenPiton/BYOC, the directory is integrated into the L2/LLC, while in BP-BedRock the directory is a standalone block that maintains coherence among the L1 caches. The BP-BedRock directory is a duplicate-tag directory whereas the OpenPiton directory integrates 64-bits of directory storage per L2 cache entry. BP-BedRock and OpenPiton/BYOC rely on similar coherence network priority schemes to avoid protocol deadlock, but BP-BedRock supports unordered networks while OpenPiton/BYOC use point-to-point ordered networks. Another difference with the protocols and implementations is that OpenPiton/BYOC does not allow direct cache to cache transfers, while BP-BedRock supports this operation using the dedicated Fill network. Additionally, OpenPiton/BYOC allow for cache-initiated eviction and writeback of cache blocks, whereas BP-BedRock's coherence directory explicitly manages all coherence state transitions. OpenPiton/BYOC do not explore the use of programmability within the coherence system.

#### 6.4.5 RISC-V Manycore Processors

Manticore [137], CIFER [27], [82], DECADES [46], HammerBlade [69], and Occamy [105] are a few examples of RISC-V-based manycore processors and systems developed over the past few years. Like BP-BedRock, these projects contribute to the growing open-source hardware movement by providing high-quality processor, accelerator, and systems designs. In contrast to the cache-coherent BP-BedRock multicore, manycore processors typically comprise a large collection of loosely-coupled processing elements. Although there may be a large shared memory or shared caches, coherence among cores is generally maintained using software mechanisms rather than hardware-based cache coherence. In the open-source hardware movement, both cache-coherent multicores and loosely-coupled manycores are needed, with the former often employed as a host processor for the latter, which is one potential use for a BP-BedRock multicore.

## Chapter 7

# Conclusion

This dissertation revisits the topic of programmability within the cache coherence system of shared-memory multicore processors against the backdrop of the modern computing landscape. In the two decades since single-chip multicore processors first emerged and the nearly three decades since programmability in the cache coherence system of multiprocessors was last investigated, the computing landscape has changed dramatically. Computing systems have become more diverse and applied across an ever-expanding set of domains. The breakdown of long-relied upon transistor and technology scaling laws and the rise of novel computing applications, especially in the areas of machine learning and artificial intelligence, have driven computer architects toward both domain-specific and highly adaptable computer architectures. At the same time, the emergence and rapid growth of the open-source hardware movement and open-source RISC-V instruction set architecture have further democratized computer processor and system design. Collectively, the confluence of trends in applications, technology scaling, and open-source hardware and software have fundamentally changed the computing landscape.

Taking a bottom-up, architecture-first approach, the feasibility of introducing programmability into the cache coherence system at the coherence directory controller is explored. This investigation first presents the BedRock cache coherence protocol, an easy to implement race-free protocol suitable for small- to medium-scale modern shared-memory multicore processors. BedRock is a family of directory-based invalidate coherence protocols using subsets of the common MOESIIF coherence states. A complete specification of the BedRock protocol is presented in tabular form long with a description of the necessary system components, coherence states, coherence networks, and coherence messages required by the protocol. Comparing BedRock to a canonical directory-based coherence protocol reveals that the design tradeoffs of cache coherence protocols are not always straightforward and that implementations often dictate the realizable concurrency and performance of a given protocol.

Following the description and analysis of BedRock, a complete open-source implementation of the protocol within the BlackParrot 64-bit RISC-V shared-memory multicore processor, called BP-BedRock, is described. BP-BedRock includes both fixed-function and microcode-programmable coherence directory implementations and demonstrates the feasibility of introducing programmability at the coherence directory. Utilizing a complete duplicate tag directory organization, BP-BedRock maintains a constant 6.25% coherence directory storage overhead relative to the capacity of the coherent L1 caches, regardless of the number of processor tiles in the tiled BlackParrot multicore architecture. The microcode-programmable coherence engine realizes programmability

at low overheads due to its use of highly-specialized coherence processing modules and instruction set extensions that offload the core of the coherence protocol processing from general purpose code. Consequently, the microcode-programmable coherence engine implementation has only single-digit percentage area and resource costs at the multicore design level while incurring only a 1% average (2.3% worst-case) performance overhead for the Splash-3 benchmarks. Applying programmability to implement the cache coherence protocol has an area or resource overhead of 4-7% at the multicore tile level.

Drawing on learnings from BP-BedRock’s initial implementation, a hybrid coherence engine design is presented that blends the protocol processing performance of a hardware-based fixed-function coherence engine with the programmability and adaptability of a microcode-programmable coherence engine. The hybrid coherence engine design evolves the fixed-function protocol processing logic of the FSM-based coherence engine to provide additional inter-transaction concurrency, while integrating a programmable processing pipeline to handle application- or system-specific processing of coherence requests. The hybrid coherence engine architecture presents one possible method of integrating programmable logic with the coherence processing pipeline and illustrates the breadth of possibility in the design space. This investigation further motivates research into the integration of useful programmability into the cache coherence engines of shared-memory multicore processors.

## 7.1 Future Work

The research presented in this dissertation reveals and motivates numerous promising avenues of future research. Possible research spans from continued development of both BedRock and the BP-BedRock implementation, to cache coherence protocols and their adaptability to new system architectures or application domains, to open-source hardware and processor development.

### 7.1.1 Cache Coherence Protocols and Systems

Cache coherence protocols remain a niche area of research, despite being the backbone of nearly all contemporary shared-memory multicore processor systems. As evidenced by the lack of publications from industry, the inner workings of cache coherence systems, which are often tightly coupled with the architecture and implementation of on-chip networks, remain closely guarded secrets. However, the performance and efficiency of cache coherence systems directly impacts the achievable performance of all modern shared-memory multicore processors. Therefore, it is imperative that research continues into a wide variety of cache coherence protocols and implementations.

At the coherence protocol level, most contemporary research focuses on developing protocols for large, high-performance multicore processor architectures. However, as computing systems are applied in more and more domains, the use of small- to medium-scale processors is increasing. Thus, investigations into protocols optimized for small- to medium-scale processors is a promising direction for future research.

The investigations described in this dissertation also show that protocol design decisions are not always straightforward or obvious. There are complex relationships between the coherence protocol, its implementation, and the system’s processing elements. Thus, building real cache coherent multicore systems is critical to understanding the realizable benefits and drawbacks of any given coherence protocol and system. These questions become increasingly relevant as systems become more heterogeneous and incorporate an ever growing variety of specialized processing elements and accelerators that can access the same memory as a host processor. Contemporary accelerator

offload models largely rely on bulk-synchronous offload or direct memory access (DMA) models where there is little active sharing of data between the host and accelerator or among accelerators. Enabling fine-grained cache coherent access to shared memory in an efficient manner is an open research challenge.

### 7.1.2 Open-Source Cache-Coherent RISC-V Multicore Processors

The rapid growth of the open-source hardware ecosystem and the RISC-V instruction set architecture has democratized computer processor and system design. However, there exist few high-quality open-source cache-coherent multicore processor implementations. BP-BedRock contributes one design to this space, allowing researchers to explore new and novel coherence system designs. Due to BP-BedRock’s use of latency-insensitive interfaces between the caches and cache controllers and between the coherence directories and last-level caches and main memory, it is possible to completely swap out the coherence system in a BP-BedRock implementation. Future research can leverage the infrastructure and design methodologies from BP-BedRock to explore alternative coherence protocols and their implementations.

The availability of high-quality open-source RISC-V multicore processors can also drive research into heterogeneous system architecture. Researchers are constantly proposing new accelerator architectures for domain-specific applications, but evaluating these accelerators remains challenging. Simulation is fast but often overlooks important implementation details that may have non-trivial impacts on the accelerator’s architecture, performance, power, or area. Hardware implementation provides real world evaluation, but requires significant infrastructure development. BP-BedRock and BlackParrot enable researchers to build real systems with tightly- or loosely-coupled accelerators. One promising avenue of future research is leveraging the BP-BedRock infrastructure to explore cache coherence within heterogeneous systems including one or more domain-specific accelerators.

### 7.1.3 Use Cases for Programmability in the Cache Coherence System

This dissertation takes a bottom-up, architecture-first approach to investigating the feasibility of introducing programmability into the cache coherence system of shared-memory multicore processors. Equally important is investigating the use cases for this programmability. An important avenue for future research is taking a top-down, application-first approach to discover the types of systems and applications that may benefit most from programmability in the coherence system. This research is likely to span both system and application software.

At the system level, programmability could be exploited to provide security, virtualization, or debugging capabilities. One obvious application of programmability at the coherence directory is to provide address space isolation verification. In some systems, whether virtualized or not, it may be desirable to isolate certain processing elements from the rest of the system by restricting their access to specific regions of physical memory. Programmability in the coherence system can be used to implement memory access checks beyond the capabilities of existing mechanisms like the virtual memory and address translation systems. In other cases, it may be desirable to simply monitor and report on physical memory accesses made by specific processor cores or accelerators. Tracing memory accesses or implementing watchpoints are common techniques for application debugging, which may be implementable within a programmable coherence system. In all cases, the exact needs and demands placed on a coherence system with programmability for any of these applications are open research questions.

User software and applications may have other use cases for programmability within the coherence system. For example, a user application may wish to monitor accesses to memory it has allocated from its heap or memory pages that have been shared with other processes or among threads of a multi-threaded application. A critical unanswered question in this area is how to support and execute untrusted application functionality or code on the programmable portion of the coherence system. By definition, cache coherence systems are among the most trusted components of a multicore processor design as they have access to the entire physical address space. Since hardware-based caching operates invisibly to the user and system software, they have been developed assuming the entire coherence system is privileged and trusted. Developing a safe and secure mechanism for executing untrusted routines within the coherence domain is an important open challenge to delivering programmability that can be leveraged by user-space software.

## Appendix A

# BedRock Cache Controller (LCE) Coherence Protocol Tables

State	Cache Action			Coherence Message						
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB
I	ReqRd	ReqWr		CohAck/X						
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X	DATA, DirtyW-B/X

Table A.1: BedRock Cache Controller Protocol Table - MI

State	Cache Action			Coherence Message							
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB	
I	ReqRd	ReqWr		CohAck/X							
S	Hit	ReqWr	InvAck/I		CohAck/M						
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X	DATA, DirtyW-B/X	

Table A.2: BedRock Cache Controller Protocol Table - MSI

State	Cache Action		Coherence Message							
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB
I	ReqRd	ReqWr		CohAck/X						
S	Hit	ReqWr	InvAck/I		CohAck/M					
E	Hit	Hit/M				NullWB/E		NullWB/X	DATA/X	DATA, NullWB/X
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X	DATA, DirtyW-B/X

Table A.3: BedRock Cache Controller Protocol Table - MESI

State	Cache Action		Coherence Message												
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB					
I	ReqRd	ReqWr		CohAck/X											
S	Hit	ReqWr	InvAck/I		CohAck/M										
E	Hit	Hit/M				NullWB/E		NullWB/X	DATA/X					DATA, NullWB/X	
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X					DATA, DirtyW- B/X	
F	Hit	ReqWr								DATA/F				DATA/X	

Table A.4: BedRock Cache Controller Protocol Table - MESIF

State	Cache Action		Coherence Message											
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB				
I	ReqRd	ReqWr		CohAck/X										
S	Hit	ReqWr	InvAck/I		CohAck/M									
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X					DATA, DirtyW-B/X
O	Hit	ReqWr			CohAck/M	DirtyWB/O	DATA/O	DirtyWB/X	DATA/X					

Table A.5: BedRock Cache Controller Protocol Table - MOSI

State	Cache Action		Coherence Message												
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB					
I	ReqRd	ReqWr		CohAck/X											
S	Hit	ReqWr	InvAck/I		CohAck/M										
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X						DATA, DirtyW-B/X
O	Hit	ReqWr			CohAck/M	DirtyWB/O	DATA/O	DirtyWB/X	DATA/X						
F	Hit	ReqWr			CohAck/M		DATA/F		DATA/X						

Table A.6: BedRock Cache Controller Protocol Table - MOSIF

State	Cache Action		Coherence Message												
	Load	Store	Inv	DATA	STW	WB	TR	ST-WB	ST-TR	ST-TR-WB					
I	ReqRd	ReqWr		CohAck/X											
S	Hit	ReqWr	InvAck/I		CohAck/M										
E	Hit	Hit/M				NullWB/E		NullWB/X	DATA/X					DATA, NullWB/X	
M	Hit	Hit				DirtyWB/M		DirtyWB/X	DATA/X					DATA, DirtyW- B/X	
O	Hit	ReqWr						DirtyWB/O	DATA/O			DirtyWB/X	DATA/X		

Table A.7: BedRock Cache Controller Protocol Table - MOESI

## Appendix B

# BedRock Coherence Directory (CCE) Coherence Protocol Tables

Directory State	Coherence Request					Directory Action
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	
I	DATA to Req/M	DATA to Req/M	DATA to Req/M			
M	ST <sup>L</sup> -TR <sup>M</sup> to Owner/M	ST <sup>L</sup> -TR <sup>M</sup> to Owner/M	ST <sup>L</sup> -TR <sup>M</sup> to Owner/M			ST <sup>L</sup> -WB to Req/I

Table B.1: BedRock Coherence Directory Protocol Table - MI

Directory State	Coherence Request					Directory Action
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	
I	DATA to Req/S	DATA to Req/S	DATA to Req/M			
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M		Replacement
M	ST <sup>S</sup> -TR <sup>S</sup> -WB to Owner/S	ST <sup>S</sup> -TR <sup>S</sup> -WB to Owner/S	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I

Table B.2: BedRock Coherence Directory Protocol Table - MSI

Directory State	Coherence Request						Directory Action
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	Replacement	
I	DATA to Req/E	DATA to Req/S	DATA to Req/M				
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M			
E	ST <sup>S</sup> -TR <sup>S</sup> -WB to Owner/S	ST <sup>S</sup> -TR <sup>S</sup> -WB to Owner/S	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I	
M	ST <sup>S</sup> -TR <sup>S</sup> -WB to Owner/S	ST <sup>S</sup> -TR <sup>S</sup> -WB to Owner/S	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I	

Table B.3: BedRock Coherence Directory Protocol Table - MESI

Directory State	Coherence Request					Directory Action
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	
I	DATA to Req/E	DATA to Req/S	DATA to Req/M			Replacement
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M		
E	ST <sup>F</sup> -TR <sup>S</sup> -WB to Owner/F	ST <sup>F</sup> -TR <sup>S</sup> -WB to Owner/F	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I
M	ST <sup>F</sup> -TR <sup>S</sup> -WB to Owner/F	ST <sup>F</sup> -TR <sup>S</sup> -WB to Owner/F	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I
F	TR <sup>S</sup> to Owner/F	TR <sup>S</sup> to Owner/F	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M	

Table B.4: BedRock Coherence Directory Protocol Table - MESIF

Directory State	Coherence Request					Directory Action
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	
I	DATA to Req/S	DATA to Req/S	DATA to Req/M			Replacement
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M		
M	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I
O	TR <sup>S</sup> to Owner/O	TR <sup>S</sup> to Owner/O	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M	ST <sup>I</sup> -WB to Req/I

Table B.5: BedRock Coherence Directory Protocol Table - MOSI

Directory State	Coherence Request					Directory Action	
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	Replacement	
I	DATA to Req/F	DATA to Req/S	DATA to Req/M				
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M			
M	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I	
O	TR <sup>S</sup> to Owner/O	TR <sup>S</sup> to Owner/O	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M	ST <sup>I</sup> -WB to Req/I	
F	TR <sup>S</sup> to Owner/F	TR <sup>S</sup> to Owner/F	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M		

Table B.6: BedRock Coherence Directory Protocol Table - MOSIF

Note: it may be beneficial to make F the next state of a ReqRd to a block in S.

Directory State	Coherence Request					Directory Action
	ReqRd	ReqRd (Non-Excl)	ReqWr from Invalid	ReqWr from Sharer	ReqWr from Owner	
I	DATA to Req/E	DATA to Req/S	DATA to Req/M			Replacement
S	DATA to Req/S	DATA to Req/S	Inv all S, DATA to Req/M	Inv other S, STW <sup>M</sup> to Req/M		
E	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I
M	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>O</sup> -TR <sup>S</sup> to Owner/O	ST <sup>I</sup> -TR <sup>M</sup> to Owner/M			ST <sup>I</sup> -WB to Req/I
O	TR <sup>S</sup> to Owner/O	TR <sup>S</sup> to Owner/O	Inv all S, ST <sup>I</sup> -TR <sup>M</sup> to Owner/M	Inv other S and Owner, STW <sup>M</sup> to Req/M	Inv all S, STW <sup>M</sup> to Req/M	ST <sup>I</sup> -WB to Req/I

Table B.7: BedRock Coherence Directory Protocol Table - MOESI

## Appendix C

# BedRock Cache Controller (LCE) Coherence State Transition Tables

Event	Current State	Next State
Load	I	M
Store	I	M
Other Load	M	I
Other Store	M	I

Table C.1: BedRock Cache Controller Next State Table - MI

Event	Current State	Next State
Load	I	S
Store	I, S	M
Other Load	M	S
Other Store	S, M	I

Table C.2: BedRock Cache Controller Next State Table - MSI

Event	Current State	Next State
Load	I	S, E
Store	I, S	M
Store (Silent Upgrade)	E	M
Other Load	E, M	S
Other Store	S, E, M	I

Table C.3: BedRock Cache Controller Next State Table - MESI

Event	Current State	Next State
Load	I	S, E
Store	I, S, F	M
Store (Silent Upgrade)	E	M
Other Load	E, M	F
Other Store	S, E, M, F	I

Table C.4: BedRock Cache Controller Next State Table - MESIF

Event	Current State	Next State
Load	I	S
Store	I, S, O	M
Other Load	M	O
Other Store	S, O, M	I

Table C.5: BedRock Cache Controller Next State Table - MOSI

Event	Current State	Next State
Load	I	S, F
Store	I, S, O, F	M
Other Load	M	O
Other Store	S, O, M, F	I

Table C.6: BedRock Cache Controller Next State Table - MOSIF

Event	Current State	Next State
Load	I	S, E
Store	I, S, O	M
Store (Silent Upgrade)	E	M
Other Load	E	S
	M	O
Other Store	S, E, M, O	I

Table C.7: BedRock Cache Controller Next State Table - MOESI

## Appendix D

# BedRock Coherence Directory (CCE) Coherence State Transition Tables

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load (Any)	ReqRd, ReqRd-NE	I, M	M	M
Store	ReqWr	I, M	M	M

Table D.1: BedRock Coherence Directory Next State Table - MI

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load (Any)	ReqRd, ReqRd-NE	I, S, M	S	S
Store	ReqWr	I, S, M	M	M

Table D.2: BedRock Coherence Directory Next State Table - MSI

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load	ReqRd	I	E	E
		S, E, M	S	S
Load (Non-Excl)	ReqRd-NE	I, S, E, M	S	S
Store	ReqWr	I, S, E, M	M	M

Table D.3: BedRock Coherence Directory Next State Table - MESI

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load	ReqRd	I	E	E
		S, M	S	S
		E, F	F	S
Load (Non-Excl)	ReqRd-NE	I, S, M	S	S
		E, F	F	S
Store	ReqWr	I, S, E, M, F	M	M

Table D.4: BedRock Coherence Directory Next State Table - MESIF

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load (Any)	ReqRd, ReqRd-NE	I, S	S	S
		M, O	O	S
Store	ReqWr	I, S, O, M	M	M

Table D.5: BedRock Coherence Directory Next State Table - MOSI

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load (Any)	ReqRd, ReqRd-NE	I	F	F
		S	S	S
		M, O	O	S
		F	F	S
Store	ReqWr	I, S, O, M, F	M	M

Table D.6: BedRock Coherence Directory Next State Table - MOSIF

Event	Request Message	Current State (Dir)	Next State (Dir)	Next State (Requestor)
Load	ReqRd	I	E	E
		S, E	S	S
		M, O	O	S
Load (Non-Excl)	ReqRd-NE	I, S, E	S	S
		M, O	O	S
Store	ReqWr	I, S, O, E, M	M	M

Table D.7: BedRock Coherence Directory Next State Table - MOESI

## Appendix E

# BP-BedRock FPGA Resource Utilization Tables

The tables in this appendix list the resource utilization of FPGA-implemented BP-BedRock designs. Each table shows resource utilization for designs with 1, 2, 4, 8, and 16 cores with the FSM, ucode, and Hybrid CCE designs. The Hybrid-FSM design rows use the Hybrid CCE implementation with the programmable pipe logic removed. The columns in each table indicate the core count, CCE design, and FPGA resources. The FPGA resources include the number of Lookup Tables (Total LUT) used, the number of LUTs used for logic (Logic LUTs) or memory (Memory LUTs), the number of flip-flop elements or registers (FF), the number of hardened memories (BRAM), and the number of digital signal processing blocks (DSP).

[Table E.1](#) and [Table E.2](#) list the total number of FPGA resources per type as counts and percentages, respectively, for the complete FPGA-based BlackParrot multicore design, including all necessary support logic to connect the multicore to memory and the host computer. This additional logic includes HBM memory controllers, PCI Express (PCIe) interface logic, AXI interconnect blocks, and FPGA host logic that provides a register-based control interface to software running on the host computer.

[Table E.3](#) and [Table E.4](#) list the FPGA resource utilization per type as counts and percentages, respectively, for only the BlackParrot multicore component of the complete FPGA design. These tables exclude resources used by the support logic described above.

Cores	CCE	Total LUT	Logic LUTs	Memory LUTs	FF (Regs)	BRAM	DSP
1	FSM	110043	93336	16707	87291	306	11
	ucode	112218	95511	16707	88001	306.5	11
	Hybrid-FSM	111060	93369	17691	87393	306	11
	Hybrid	112644	94953	17691	87995	306.5	11
2	FSM	173483	148579	24904	113723	389.5	22
	ucode	178723	153819	24904	115071	390.5	22
	Hybrid-FSM	175629	148709	26920	113928	389.5	22
	Hybrid	178825	151905	26920	115119	390.5	22
4	FSM	296004	257710	38294	165589	578.5	44
	ucode	303814	265520	38294	168157	580.5	44
	Hybrid-FSM	300376	257954	42422	166007	578.5	44
	Hybrid	306786	264364	42422	168398	580.5	44
8	FSM	489766	428548	61218	226461	644.5	88
	ucode	507454	446172	61282	231493	648.5	88
	Hybrid-FSM	498240	428702	69538	227271	644.5	88
	Hybrid	512092	442554	69538	232096	648.5	88
16	FSM	869480	764590	104890	348964	776.5	176
	ucode	906422	801404	105018	358740	784.5	176
	Hybrid-FSM	886897	765279	121618	350758	776.5	176
	Hybrid	912497	790871	121626	360433	784.5	176
Total Available		1303680	1303680	600960	2607360	2016	9024

Table E.1: FPGA Design Utilization

Cores	CCE	Total LUT	Logic LUTs	Memory LUTs	FF (Regs)	BRAM	DSP
1	FSM	8.44%	7.16%	2.78%	3.35%	15.18%	0.12%
	ucode	8.61%	7.33%	2.78%	3.38%	15.20%	0.12%
	Hybrid-FSM	8.52%	7.16%	2.94%	3.35%	15.18%	0.12%
	Hybrid	8.64%	7.28%	2.94%	3.37%	15.20%	0.12%
2	FSM	13.31%	11.40%	4.14%	4.36%	19.32%	0.24%
	ucode	13.71%	11.80%	4.14%	4.41%	19.37%	0.24%
	Hybrid-FSM	13.47%	11.41%	4.48%	4.37%	19.32%	0.24%
	Hybrid	13.72%	11.65%	4.48%	4.42%	19.37%	0.24%
4	FSM	22.71%	19.77%	6.37%	6.35%	28.70%	0.49%
	ucode	23.30%	20.37%	6.37%	6.45%	28.79%	0.49%
	Hybrid-FSM	23.04%	19.79%	7.06%	6.37%	28.70%	0.49%
	Hybrid	23.53%	20.28%	7.06%	6.46%	28.79%	0.49%
8	FSM	37.57%	32.87%	10.19%	8.69%	31.97%	0.98%
	ucode	38.92%	34.22%	10.20%	8.88%	32.17%	0.98%
	Hybrid-FSM	38.22%	32.88%	11.57%	8.72%	31.97%	0.98%
	Hybrid	39.28%	33.95%	11.57%	8.90%	32.17%	0.98%
16	FSM	66.69%	58.65%	17.45%	13.38%	38.52%	1.95%
	ucode	69.53%	61.47%	17.48%	13.76%	38.91%	1.95%
	Hybrid-FSM	68.03%	58.70%	20.24%	13.45%	38.52%	1.95%
	Hybrid	69.99%	60.66%	20.24%	13.82%	38.91%	1.95%

Table E.2: FPGA Design Utilization (Percentage)

Cores	CCE	Total LUT	Logic LUTs	Memory LUTs	FF (Regs)	BRAM	DSP
1	FSM	62152	54715	7405	27419	106	11
	ucode	64347	56910	7405	28129	106	11
	Hybrid-FSM	63202	54781	8389	27521	106	11
	Hybrid	64767	56346	8389	28123	106	11
2	FSM	125609	109975	15570	53851	189	22
	ucode	130865	115231	15570	55199	190	22
	Hybrid-FSM	127768	110118	17586	54056	189	22
	Hybrid	130937	113287	17586	55247	190	22
4	FSM	248139	219115	28896	105717	378	44
	ucode	255938	226914	28896	108285	380	44
	Hybrid-FSM	252496	219344	33024	106135	378	44
	Hybrid	258895	225743	33024	108526	380	44
8	FSM	441878	389930	51692	166589	444	88
	ucode	459570	407558	51756	171621	448	88
	Hybrid-FSM	450336	390068	60012	167399	444	88
	Hybrid	464203	403935	60012	172224	448	88
16	FSM	821603	725983	95108	289092	576	176
	ucode	858618	762870	95236	298868	584	176
	Hybrid-FSM	839059	726703	111844	290886	576	176
	Hybrid	864602	752246	111844	300561	584	176
Total Available		1303680	1303680	600960	2607360	2016	9024

Table E.3: FPGA BP Multicore Utilization

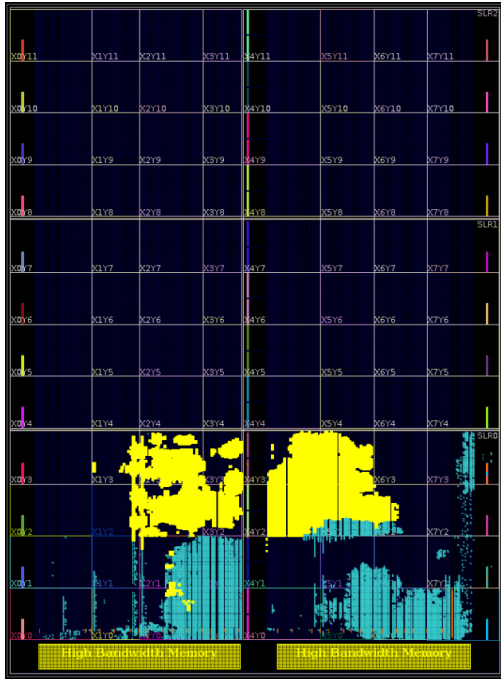
Cores	CCE	Total LUT	Logic LUTs	Memory LUTs	FF (Regs)	BRAM	DSP
1	FSM	4.77%	4.20%	1.23%	1.05%	5.23%	0.12%
	ucode	4.94%	4.37%	1.23%	1.08%	5.26%	0.12%
	Hybrid-FSM	4.85%	4.20%	1.40%	1.06%	5.23%	0.12%
	Hybrid	4.97%	4.32%	1.40%	1.08%	5.26%	0.12%
2	FSM	9.63%	8.44%	2.59%	2.07%	9.38%	0.24%
	ucode	10.04%	8.84%	2.59%	2.12%	9.42%	0.24%
	Hybrid-FSM	9.80%	8.45%	2.93%	2.07%	9.38%	0.24%
	Hybrid	10.04%	8.69%	2.93%	2.12%	9.42%	0.24%
4	FSM	19.03%	16.81%	4.81%	4.05%	18.75%	0.49%
	ucode	19.63%	17.41%	4.81%	4.15%	18.85%	0.49%
	Hybrid-FSM	19.37%	16.82%	5.50%	4.07%	18.75%	0.49%
	Hybrid	19.86%	17.32%	5.50%	4.16%	18.85%	0.49%
8	FSM	33.89%	29.91%	8.60%	6.39%	22.02%	0.98%
	ucode	35.25%	31.26%	8.61%	6.58%	22.22%	0.98%
	Hybrid-FSM	34.54%	29.92%	9.99%	6.42%	22.02%	0.98%
	Hybrid	35.61%	30.98%	9.99%	6.61%	22.22%	0.98%
16	FSM	63.02%	55.69%	15.83%	11.09%	28.57%	1.95%
	ucode	65.86%	58.52%	15.85%	11.46%	28.97%	1.95%
	Hybrid-FSM	64.36%	55.74%	18.61%	11.16%	28.57%	1.95%
	Hybrid	66.32%	57.70%	18.61%	11.53%	28.97%	1.95%

Table E.4: FPGA BP Multicore Utilization (Percentage)

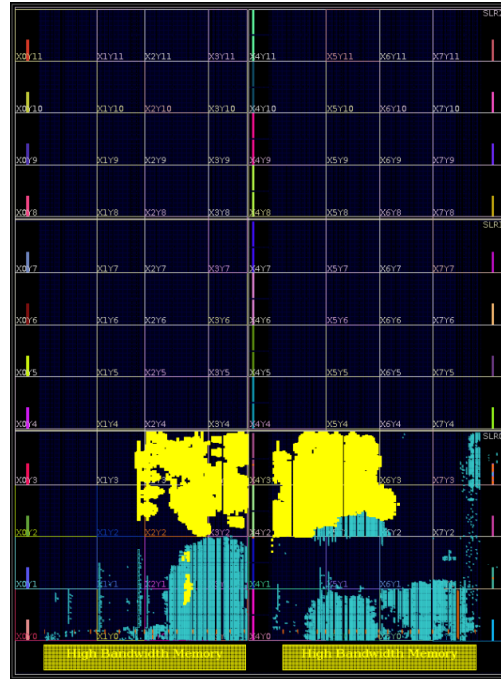
## Appendix F

# BP-BedRock FPGA Implementation Layouts

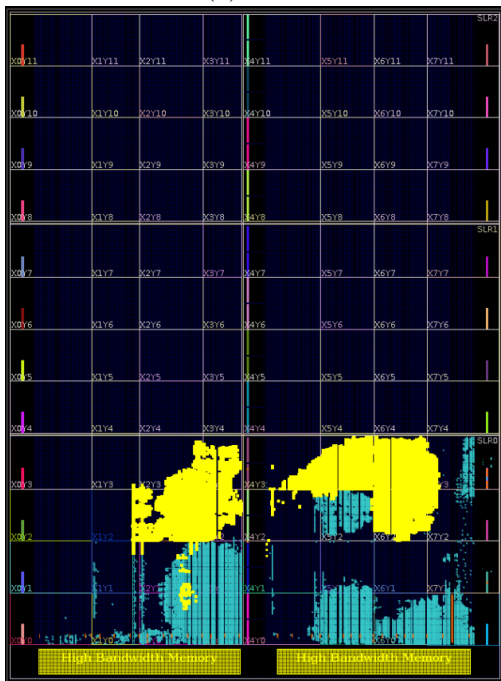
The figures in this appendix depict FPGA layouts of the four BP-BedRock designs across various core counts. The highlighted colors indicate resources consumed by individual BP-BedRock core tiles for each design. Colors do not correlate to specific core IDs within the multicore, i.e., the core tile highlighted in pink for one design may not represent the same core tile that is highlighted pink in another design, even when the core count is the same for both designs. The FSM design is a BP-BedRock multicore employing the fixed-function hardware coherence engine. The ucode designs uses the microcode-programmable coherence engine. The Hybrid FSM design uses the hybrid coherence engine design with the programmable pipe removed from the design, while the Hybrid design employs the complete hybrid coherence engine including the programmable pipe.



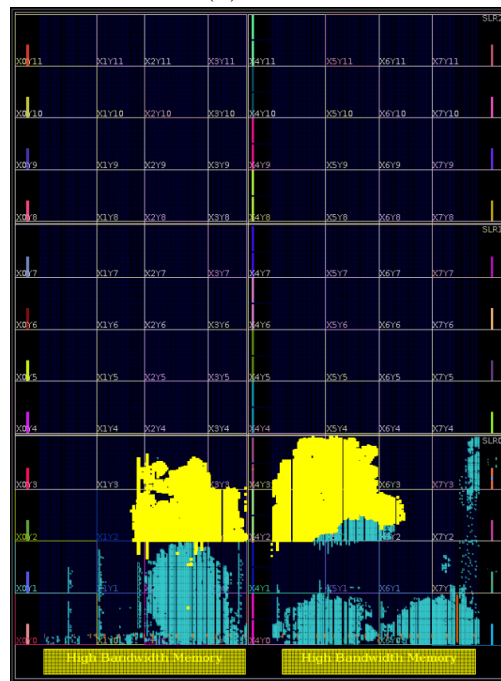
(a) FSM



(b) ucode

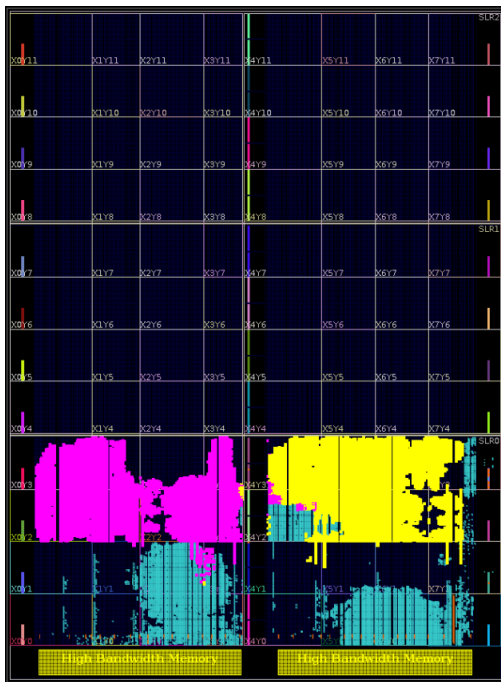


(c) Hybrid FSM

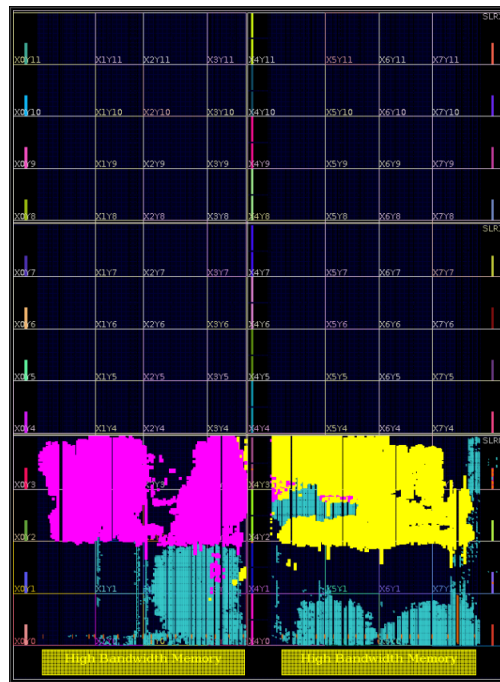


(d) Hybrid

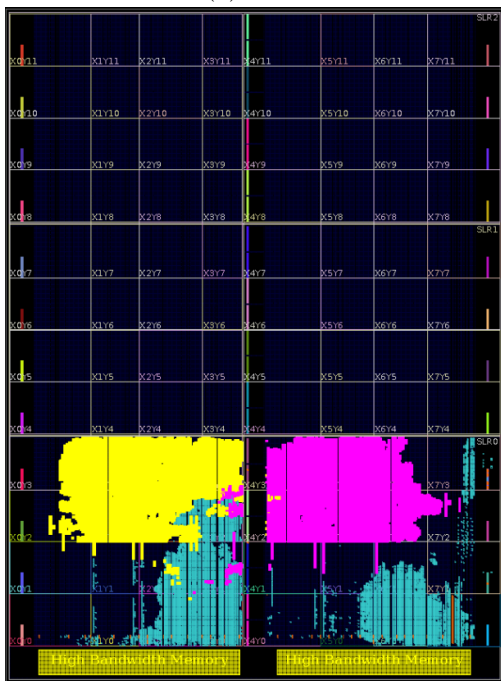
Figure F.1: BP-BedRock FPGA Layout - 1 core



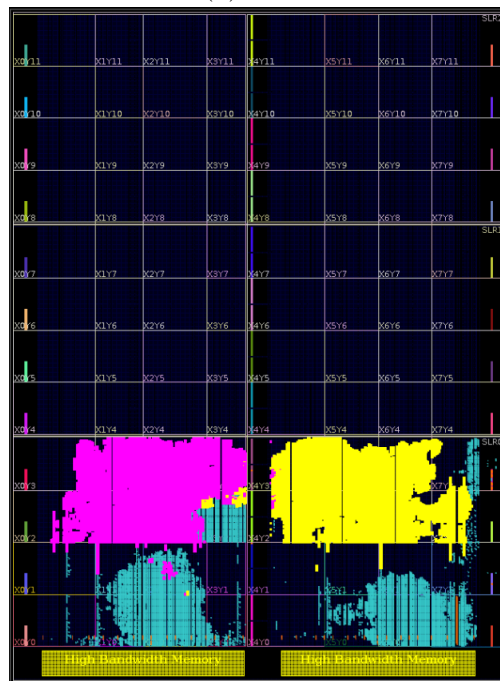
(a) FSM



(b) ucode

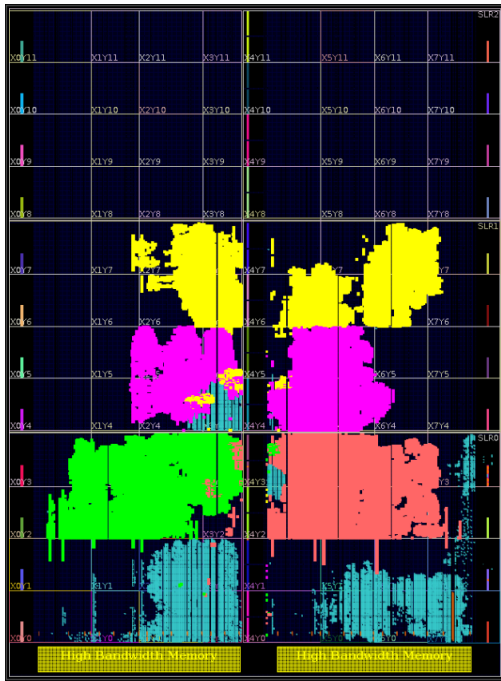


(c) Hybrid FSM

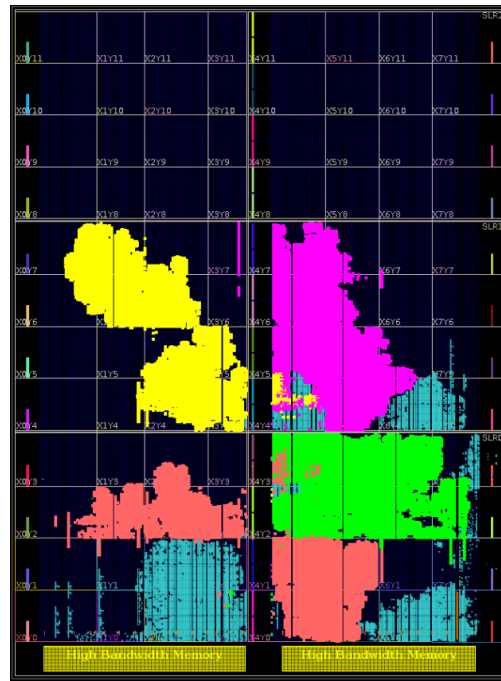


(d) Hybrid

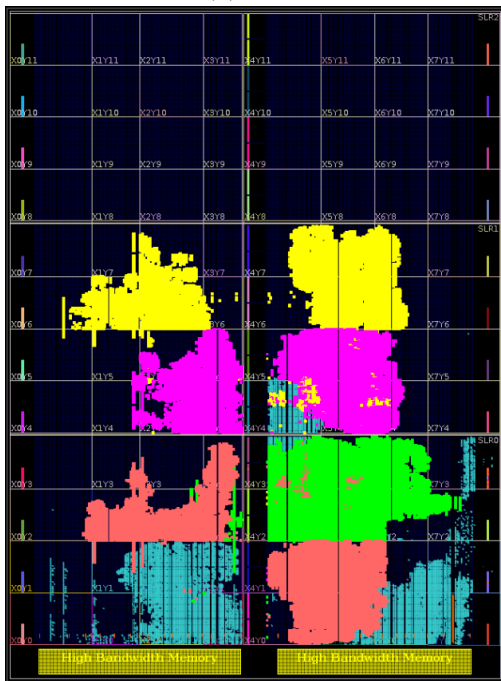
Figure F.2: BP-BedRock FPGA Layout - 2 core



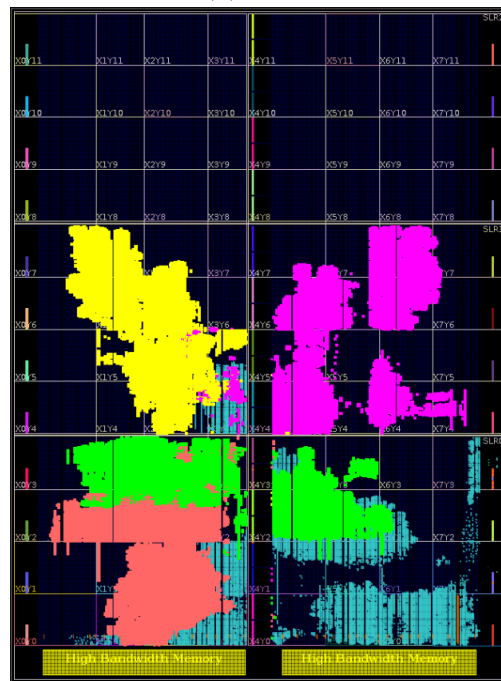
(a) FSM



(b) ucode

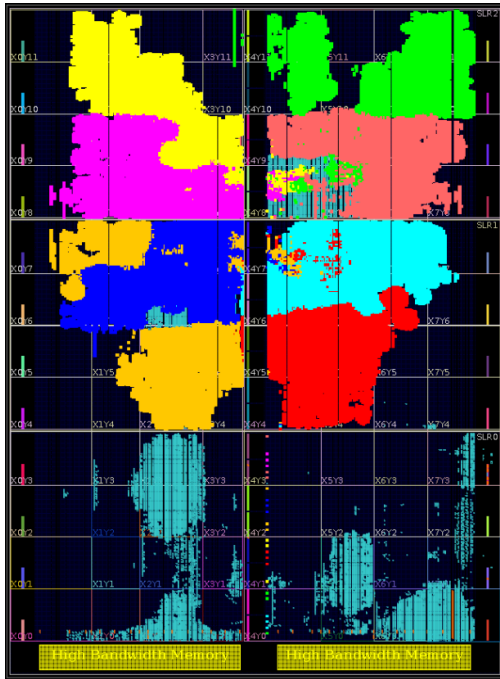


(c) Hybrid FSM

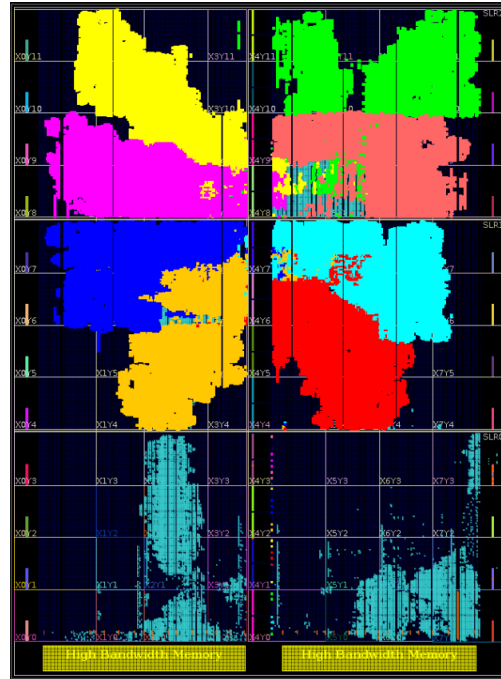


(d) Hybrid

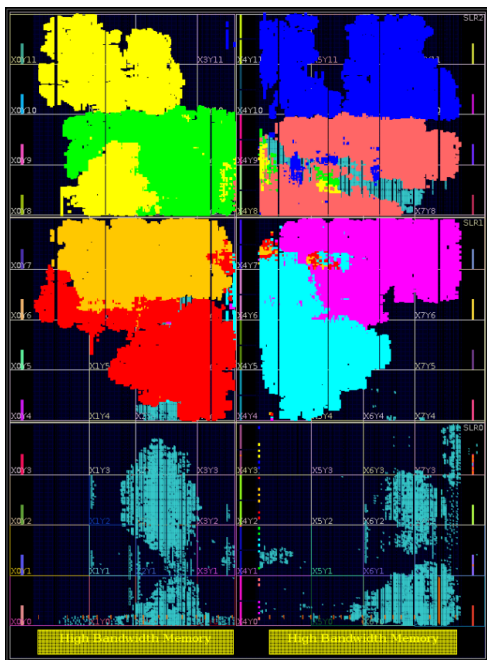
Figure F.3: BP-BedRock FPGA Layout - 4 core



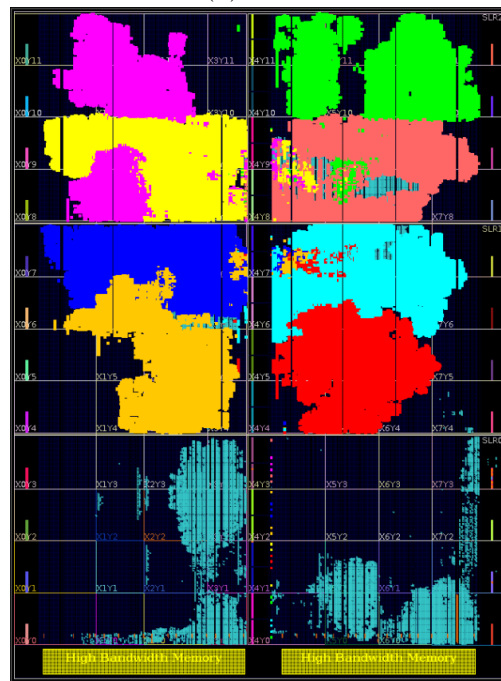
(a) FSM



(b) ucode

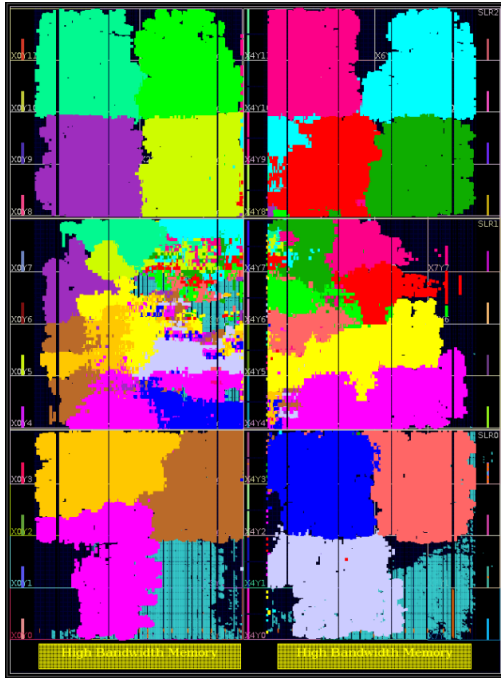


(c) Hybrid FSM

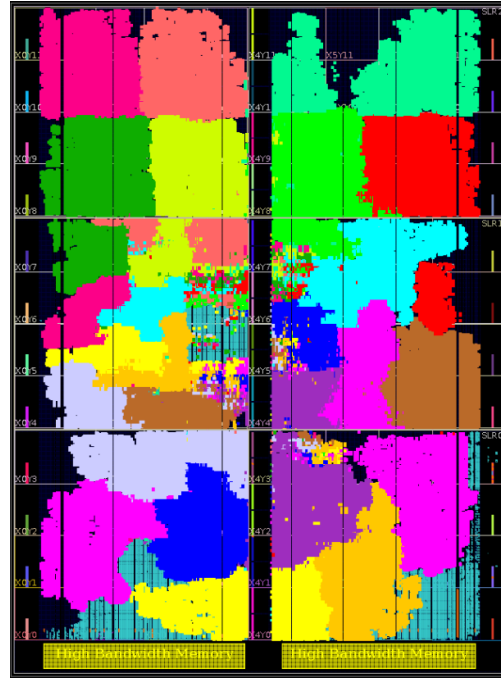


(d) Hybrid

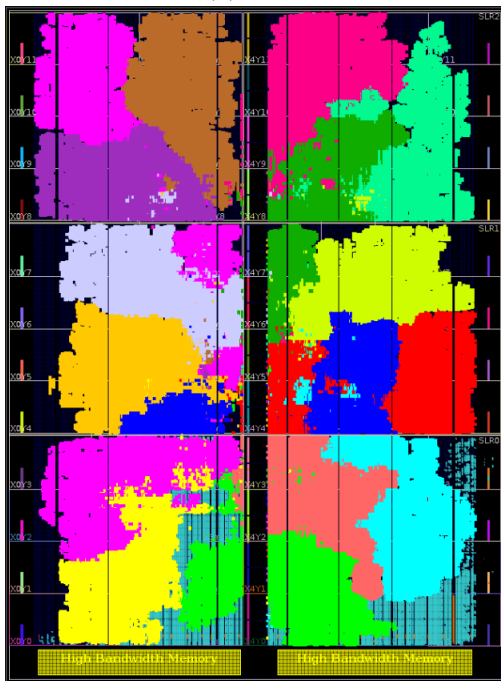
Figure F.4: BP-BedRock FPGA Layout - 8 core



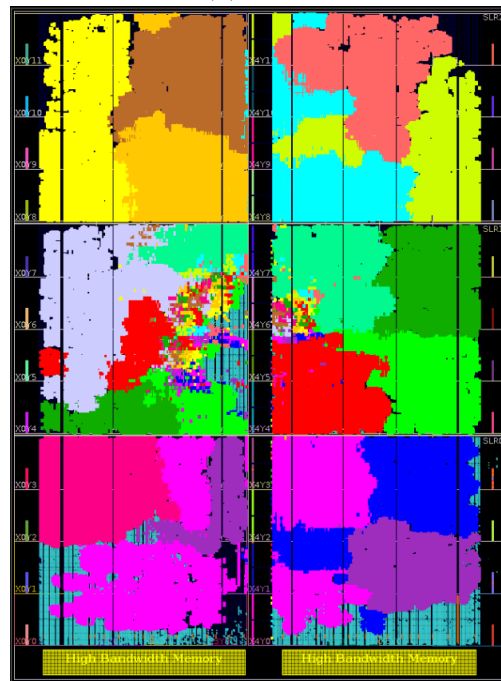
(a) FSM



(b) ucode



(c) Hybrid FSM



(d) Hybrid

Figure F.5: BP-BedRock FPGA Layout - 16 core

# References

- [1] S. V. Adve, V. S. Adve, M. D. Hill, and M. K. Vernon, “Comparison of hardware and software cache coherence schemes,” in *Proceedings of the 18th annual international symposium on Computer architecture - ISCA '91*, Toronto, Ontario, Canada: ACM Press, 1991, pp. 298–308, ISBN: 978-0-89791-394-2. DOI: [10.1145/115952.115982](https://doi.org/10.1145/115952.115982).
- [2] A. Agarwal, R. Bianchini, D. Chaiken, F. Chong, K. Johnson, D. Kranz, J. Kubiawicz, Beng-Hong Lim, K. Mackenzie, and D. Yeung, “The MIT alewife machine,” *Proceedings of the IEEE*, vol. 87, no. 3, pp. 430–444, Mar. 1999, ISSN: 00189219. DOI: [10.1109/5.747864](https://doi.org/10.1109/5.747864).
- [3] A. Agarwal, R. Simoni, J. Hennessy, and M. Horowitz, “An evaluation of directory schemes for cache coherence,” in *[1988] The 15th Annual International Symposium on Computer Architecture. Conference Proceedings*, Honolulu, HI, USA: IEEE Comput. Soc. Press, 1988, pp. 280–289, ISBN: 978-0-8186-0861-2. DOI: [10.1109/ISCA.1988.5238](https://doi.org/10.1109/ISCA.1988.5238).
- [4] A. Agarwal, R. Bianchini, D. Chaiken, K. L. Johnson, D. Kranz, J. Kubiawicz, B.-H. Lim, K. Mackenzie, and D. Yeung, “The MIT alewife machine: Architecture and performance,” in *Proceedings of the 22nd annual international symposium on Computer architecture - ISCA '95*, S. Margherita Ligure, Italy: ACM Press, 1995, pp. 2–13, ISBN: 978-0-89791-698-1. DOI: [10.1145/223982.223985](https://doi.org/10.1145/223982.223985).
- [5] S. Ainsworth and T. M. Jones, “An event-triggered programmable prefetcher for irregular workloads,” in *Proceedings of the Twenty-Third International Conference on Architectural Support for Programming Languages and Operating Systems*, Williamsburg VA USA: ACM, Mar. 19, 2018, pp. 578–592, ISBN: 978-1-4503-4911-6. DOI: [10.1145/3173162.3173189](https://doi.org/10.1145/3173162.3173189).
- [6] L. Alvarez, L. Vilanova, M. Moreto, M. Casas, M. González, X. Martorell, N. Navarro, E. Ayguadé, and M. Valero, “Coherence protocol for transparent management of scratchpad memories in shared memory manycore architectures,” in *Proceedings of the 42nd Annual International Symposium on Computer Architecture*, Portland Oregon: ACM, Jun. 13, 2015, pp. 720–732, ISBN: 978-1-4503-3402-0. DOI: [10.1145/2749469.2750411](https://doi.org/10.1145/2749469.2750411).
- [7] *AMBA AXI and ACE protocol specification*, version ARM IHI 0022H.c, ARM Limited, 2021.
- [8] A. Amid, D. Biancolin, A. Gonzalez, D. Grubb, S. Karandikar, H. Liew, A. Magyar, H. Mao, A. Ou, N. Pemberton, P. Rigge, C. Schmidt, J. Wright, J. Zhao, Y. S. Shao, K. Asanovic, and B. Nikolic, “Chipyard: Integrated design, simulation, and implementation framework for custom SoCs,” *IEEE Micro*, vol. 40, no. 4, pp. 10–21, Jul. 1, 2020, ISSN: 0272-1732, 1937-4143. DOI: [10.1109/MM.2020.2996616](https://doi.org/10.1109/MM.2020.2996616).
- [9] K. Asanovic and D. A. Patterson, “Instruction sets should be free: The case for risc-v,” University of California at Berkeley, Tech. Rep., 2014.
- [10] Asanovic et al, “The rocket chip generator,” *UC Berkeley EECS Tech Report UCB/EECS-2016-17*, 2016.

- [11] T. J. Ashby, P. Diaz, and M. Cintra, “Software-based cache coherence with hardware-assisted selective self-invalidations using bloom filters,” *IEEE Transactions on Computers*, vol. 60, no. 4, pp. 472–483, Apr. 2011, ISSN: 0018-9340. DOI: [10.1109/TC.2010.155](https://doi.org/10.1109/TC.2010.155).
- [12] J. Bachrach, H. Vo, B. C. Richards, Y. Lee, A. Waterman, R. Avizienis, J. Wawrzynek, and K. Asanovic, “Chisel: Constructing hardware in a scala embedded language,” in *The 49th Annual Design Automation Conference 2012, DAC '12, San Francisco, CA, USA, June 3-7, 2012*, P. Groeneveld, D. Sciuto, and S. Hassoun, Eds., ACM, 2012, pp. 1216–1225. DOI: [10.1145/2228360.2228584](https://doi.org/10.1145/2228360.2228584).
- [13] J. Balkind, “Open source platforms for enabling full-stack hardware-software research,” Ph.D. dissertation, Princeton University, USA, 2022.
- [14] J. Balkind, K. Lim, M. Schaffner, F. Gao, G. Chirkov, A. Li, A. Lavrov, T. M. Nguyen, Y. Fu, F. Zaruba, K. Gulati, L. Benini, and D. Wentzlaff, “BYOC: A ”bring your own core” framework for heterogeneous-ISA research,” in *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems*, Lausanne Switzerland: ACM, Mar. 9, 2020, pp. 699–714, ISBN: 978-1-4503-7102-5. DOI: [10.1145/3373376.3378479](https://doi.org/10.1145/3373376.3378479).
- [15] J. Balkind, M. McKeown, Y. Fu, T. Nguyen, Y. Zhou, A. Lavrov, M. Shahrad, A. Fuchs, S. Payne, X. Liang, M. Matl, and D. Wentzlaff, “OpenPiton: An open source manycore research framework,” in *Proceedings of the Twenty-First International Conference on Architectural Support for Programming Languages and Operating Systems*, Atlanta Georgia USA: ACM, Mar. 25, 2016, pp. 217–232, ISBN: 978-1-4503-4091-5. DOI: [10.1145/2872362.2872414](https://doi.org/10.1145/2872362.2872414).
- [16] L. A. Barroso, K. Gharachorloo, R. McNamara, A. Nowatzyk, S. Qadeer, B. Sano, S. Smith, R. Stets, and B. Verghese, “Piranha: A scalable architecture based on single-chip multiprocessing,” in *Proceedings of the 27th annual international symposium on Computer architecture - ISCA '00*, Vancouver, British Columbia, Canada: ACM Press, 2000, pp. 282–293, ISBN: 978-1-58113-232-8. DOI: [10.1145/339647.339696](https://doi.org/10.1145/339647.339696).
- [17] A. Basak, S. Li, X. Hu, S. M. Oh, X. Xie, L. Zhao, X. Jiang, and Y. Xie, “Analysis and optimization of the memory hierarchy for graph processing workloads,” in *25th IEEE International Symposium on High Performance Computer Architecture, HPCA 2019, Washington, DC, USA, February 16-20, 2019*, IEEE, 2019, pp. 373–386. DOI: [10.1109/HPCA.2019.00051](https://doi.org/10.1109/HPCA.2019.00051).
- [18] Buildroot. “Buildroot.” (), [Online]. Available: <https://buildroot.org/>.
- [19] BusyBox. “Busybox.” (), [Online]. Available: <https://busybox.net/>.
- [20] L. P. Carloni, “Invited - the case for embedded scalable platforms,” in *Proceedings of the 53rd Annual Design Automation Conference*, ser. DAC '16, Austin, Texas: Association for Computing Machinery, 2016, ISBN: 9781450342360. DOI: [10.1145/2897937.2905018](https://doi.org/10.1145/2897937.2905018).
- [21] C. Celio, “A highly productive implementation of an out-of-order processor generator,” Ph.D. dissertation, University of California, Berkeley, USA, 2017.
- [22] C. Celio, P.-F. Chiu, B. Nikolic, D. A. Patterson, and K. Asanović, “Boom v2: An open-source out-of-order risc-v core,” University of California, Berkeley, Tech. Rep. UCB/EECS-2017-157, Sep. 2017.
- [23] Celio et al, “The berkeley out-of-order machine (boom): An industry-competitive, synthesizable, parameterized risc-v processor,” *UC Berkeley EECS Tech. Rep. UCB/EECS-2015-167*, 2015.
- [24] Censier and Feautrier, “A new solution to coherence problems in multicache systems,” *IEEE Transactions on Computers*, vol. C-27, no. 12, pp. 1112–1118, Dec. 1978, ISSN: 0018-9340. DOI: [10.1109/TC.1978.1675013](https://doi.org/10.1109/TC.1978.1675013).

- [25] D. Chaiken and A. Agarwal, “Software-extended coherent shared memory: Performance and cost,” *ACM SIGARCH Computer Architecture News*, vol. 22, no. 2, pp. 314–324, Apr. 1994, ISSN: 0163-5964. DOI: [10.1145/192007.192060](https://doi.org/10.1145/192007.192060).
- [26] D. Chaiken, J. Kubiawicz, and A. Agarwal, “LimitLESS directories: A scalable cache coherence scheme,” *ACM SIGOPS Operating Systems Review*, vol. 25, pp. 224–234, Special Issue Apr. 2, 1991, ISSN: 0163-5980. DOI: [10.1145/106974.106995](https://doi.org/10.1145/106974.106995).
- [27] T. Chang, A. Li, F. Gao, T. Ta, G. Tziantzioulis, Y. Ou, M. Wang, J. Tu, K. Xu, P. J. Jackson, A. Ning, G. Chirkov, M. Orenes-Vera, S. Agwa, X. Yan, E. Tang, J. Balkind, C. Batten, and D. Wentzlauff, “CIFER: A 12nm, 16mm<sup>2</sup>, 22-core soc with a 1541 lut6/mm<sup>2</sup> 1.92 mops/lut, fully synthesizable, cachecoherent, embedded FPGA,” in *IEEE Custom Integrated Circuits Conference, CICC 2023, San Antonio, TX, USA, April 23-26, 2023*, IEEE, 2023, pp. 1–2. DOI: [10.1109/CICC57935.2023.10121294](https://doi.org/10.1109/CICC57935.2023.10121294).
- [28] M. Chaudhuri and M. Heinrich, “SMTp: An architecture for next-generation scalable multi-threading,” *ACM SIGARCH Computer Architecture News*, vol. 32, no. 2, p. 124, Mar. 2, 2004, ISSN: 0163-5964. DOI: [10.1145/1028176.1006712](https://doi.org/10.1145/1028176.1006712).
- [29] M. Chaudhuri and M. Heinrich, “Integrated memory controllers with parallel coherence streams,” *IEEE Transactions on Parallel and Distributed Systems*, vol. 18, no. 8, pp. 1159–1173, Aug. 2007, ISSN: 1045-9219. DOI: [10.1109/TPDS.2007.1044](https://doi.org/10.1109/TPDS.2007.1044).
- [30] D. R. Cheriton, G. Slavenburg, and P. D. Boyle, “Software-controlled caches in the VMP multiprocessor,” in *Proceedings of the 13th Annual Symposium on Computer Architecture, Tokyo, Japan, June 1986*, H. Aiso, Ed., IEEE Computer Society, 1986, pp. 366–374. DOI: [10.1145/17356.17399](https://doi.org/10.1145/17356.17399).
- [31] B. Choi, R. Komuravelli, H. Sung, R. Smolinski, N. Honarmand, S. V. Adve, V. S. Adve, N. P. Carter, and C.-T. Chou, “DeNovo: Rethinking the memory hierarchy for disciplined parallelism,” in *2011 International Conference on Parallel Architectures and Compilation Techniques*, Galveston, TX, USA: IEEE, Oct. 2011, pp. 155–166. DOI: [10.1109/PACT.2011.21](https://doi.org/10.1109/PACT.2011.21).
- [32] F. Chong, Beng-Hong Lim, R. Bianchini, J. Kubiawicz, and A. Agarwal, “Application performance on the MIT alewife machine,” *Computer*, vol. 29, no. 12, pp. 57–64, Dec. 1996, ISSN: 00189162. DOI: [10.1109/2.546610](https://doi.org/10.1109/2.546610).
- [33] A. Cilardo, M. Gagliardi, and V. Scotti, “Lightweight hardware support for selective coherence in heterogeneous manycore accelerators,” in *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy: IEEE, Mar. 2019, pp. 932–935, ISBN: 978-3-9819263-2-3. DOI: [10.23919/DATE.2019.8714723](https://doi.org/10.23919/DATE.2019.8714723).
- [34] P. Conway and B. Hughes, “The AMD opteron northbridge architecture,” *IEEE Micro*, vol. 27, no. 2, pp. 10–21, Mar. 2007, ISSN: 0272-1732. DOI: [10.1109/MM.2007.43](https://doi.org/10.1109/MM.2007.43).
- [35] P. Conway, N. Kalyanasundharam, G. Donley, K. Lepak, and B. Hughes, “Cache hierarchy and memory subsystem of the AMD opteron processor,” *IEEE Micro*, vol. 30, no. 2, pp. 16–29, Mar. 2010, ISSN: 0272-1732. DOI: [10.1109/MM.2010.31](https://doi.org/10.1109/MM.2010.31).
- [36] I. Corporation, *An introduction to the Intel quickpath interconnect, january 2009*, 2009.
- [37] S. Davidson, S. Xie, C. Torng, K. Al-Hawai, A. Rovinski, T. Ajayi, L. Vega, C. Zhao, R. Zhao, S. Dai, A. Amarnath, B. Veluri, P. Gao, A. Rao, G. Liu, R. K. Gupta, Z. Zhang, R. Dreslinski, C. Batten, and M. B. Taylor, “The celerity open-source 511-core RISC-v tiered accelerator fabric: Fast architectures and design methodologies for fast chips,” *IEEE Micro*, vol. 38, no. 2, pp. 30–41, Mar. 2018, ISSN: 0272-1732, 1937-4143. DOI: [10.1109/MM.2018.022071133](https://doi.org/10.1109/MM.2018.022071133).
- [38] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” *IEEE Journal of Solid-State Circuits*, vol. SC-9, no. 5, pp. 256–268, Oct. 1974.

- [39] E. Derebasoglu, I. Kadayif, and O. Ozturk, “Coherency traffic reduction in manycore systems,” in *2022 25th Euromicro Conference on Digital System Design (DSD)*, Maspalomas, Spain: IEEE, Aug. 2022, pp. 262–267, ISBN: 978-1-66547-404-7. DOI: [10.1109/DSD57027.2022.00043](https://doi.org/10.1109/DSD57027.2022.00043).
- [40] D. Dill, A. Drexler, A. Hu, and C. Yang, “Protocol verification as a hardware design aid,” in *Proceedings 1992 IEEE International Conference on Computer Design: VLSI in Computers & Processors*, IEEE Comput. Soc. Press, 2004. DOI: [10.1109/iccd.1992.276232](https://doi.org/10.1109/iccd.1992.276232).
- [41] *Ds890 ultrascale architecture and product data sheet: Overview, v4.1.1*, Xilinx, 2022.
- [42] M. Ferdman, P. Lotfi-Kamran, K. Balet, and B. Falsafi, “Cuckoo directory: A scalable directory for many-core systems,” in *2011 IEEE 17th International Symposium on High Performance Computer Architecture*, San Antonio, TX, USA: IEEE, Feb. 2011, pp. 169–180, ISBN: 978-1-4244-9432-3. DOI: [10.1109/HPCA.2011.5749726](https://doi.org/10.1109/HPCA.2011.5749726).
- [43] Fong Pong, M. Browne, A. Nowatzky, and M. Dubois, “Design verification of the s3.mp cache-coherent shared-memory system,” *IEEE Transactions on Computers*, vol. 47, no. 1, pp. 135–140, Jan. 1998, ISSN: 00189340. DOI: [10.1109/12.656100](https://doi.org/10.1109/12.656100).
- [44] A. Franques, A. Kokolis, S. Abadal, V. Fernando, S. Misailovic, and J. Torrellas, “WiDir: A wireless-enabled directory cache coherence protocol,” in *2021 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Seoul, Korea (South): IEEE, Feb. 2021, pp. 304–317, ISBN: 978-1-66542-235-2. DOI: [10.1109/HPCA51647.2021.00034](https://doi.org/10.1109/HPCA51647.2021.00034).
- [45] Y. Fu, T. M. Nguyen, and D. Wentzloff, “Coherence domain restriction on large scale systems,” in *Proceedings of the 48th International Symposium on Microarchitecture*, Waikiki Hawaii: ACM, Dec. 5, 2015, pp. 686–698, ISBN: 978-1-4503-4034-2. DOI: [10.1145/2830772.2830832](https://doi.org/10.1145/2830772.2830832).
- [46] F. Gao, T. Chang, A. Li, M. Orenes-Vera, D. Giri, P. J. Jackson, A. Ning, G. Tziantzioulis, J. Zuckerman, J. Tu, K. Xu, G. Chirkov, G. Tombesi, J. Balkind, M. Martonosi, L. P. Carloni, and D. Wentzloff, “DECADES: A 67mm<sup>2</sup>, 1.46tops, 55 giga cache-coherent 64-bit RISC-V instructions per second, heterogeneous manycore soc with 109 tiles including accelerators, intelligent storage, and efpga in 12nm finfet,” in *IEEE Custom Integrated Circuits Conference, CICC 2023, San Antonio, TX, USA, April 23-26, 2023*, IEEE, 2023, pp. 1–2. DOI: [10.1109/CICC57935.2023.10121257](https://doi.org/10.1109/CICC57935.2023.10121257).
- [47] D. Giri, P. Mantovani, and L. P. Carloni, “Accelerators and coherence: An soc perspective,” *IEEE Micro*, vol. 38, no. 6, pp. 36–45, 2018. DOI: [10.1109/MM.2018.2877288](https://doi.org/10.1109/MM.2018.2877288).
- [48] D. Giri, P. Mantovani, and L. P. Carloni, “Runtime reconfigurable memory hierarchy in embedded scalable platforms,” in *Proceedings of the 24th Asia and South Pacific Design Automation Conference, ASPDAC 2019, Tokyo, Japan, January 21-24, 2019*, T. Shibuya, Ed., ACM, 2019, pp. 719–726. DOI: [10.1145/3287624.3288755](https://doi.org/10.1145/3287624.3288755).
- [49] J. R. Goodman, “Using cache memory to reduce processor-memory traffic,” in *Proceedings of the 10th annual international symposium on Computer architecture - ISCA '83*, Stockholm, Sweden: ACM Press, 1983, pp. 124–131, ISBN: 978-0-89791-101-6. DOI: [10.1145/800046.801647](https://doi.org/10.1145/800046.801647).
- [50] V. Govindaraju, C. Ho, and K. Sankaralingam, “Dynamically specialized datapaths for energy efficient computing,” in *17th International Conference on High-Performance Computer Architecture (HPCA-17 2011), February 12-16 2011, San Antonio, Texas, USA*, IEEE Computer Society, 2011, pp. 503–514. DOI: [10.1109/HPCA.2011.5749755](https://doi.org/10.1109/HPCA.2011.5749755).
- [51] H. Grahn and P. Stenström, “Efficient strategies for software-only protocols in shared-memory multiprocessors,” in *Proceedings of the 22nd Annual International Symposium on Computer Architecture, ISCA '95, Santa Margherita Ligure, Italy, June 22-24, 1995*, D. A. Patterson, Ed., ACM, 1995, pp. 38–47. DOI: [10.1145/223982.225958](https://doi.org/10.1145/223982.225958).

- [52] H. Grahn and P. Stenström, “A comparative evaluation of hardware-only and software-only directory protocols in shared-memory multiprocessors,” *Journal of Systems Architecture*, vol. 50, no. 9, pp. 537–561, Sep. 2004, ISSN: 13837621. DOI: [10.1016/j.sysarc.2003.08.014](https://doi.org/10.1016/j.sysarc.2003.08.014).
- [53] M. Gries, U. Hoffmann, M. Konow, and M. Riepen, “SCC: A flexible architecture for many-core platform research,” *Computing in Science & Engineering*, vol. 13, no. 6, pp. 79–83, Nov. 2011, ISSN: 1521-9615. DOI: [10.1109/MCSE.2011.109](https://doi.org/10.1109/MCSE.2011.109).
- [54] W. P. R. Group, *Openpiton microarchitecture specification*, Princeton University, 2016.
- [55] P. Gschwandtner, T. Fahringer, and R. Prodan, “Performance analysis and benchmarking of the intel SCC,” in *2011 IEEE International Conference on Cluster Computing*, Austin, TX, USA: IEEE, Sep. 2011, pp. 139–149, ISBN: 978-1-4577-1355-2. DOI: [10.1109/CLUSTER.2011.24](https://doi.org/10.1109/CLUSTER.2011.24).
- [56] A. Gupta, W. Weber, and T. C. Mowry, “Reducing memory and traffic requirements for scalable directory-based cache coherence schemes,” in *Proceedings of the 1990 International Conference on Parallel Processing, Urbana-Champaign, IL, USA, August 1990. Volume 1: Architecture*, B. W. Wah, Ed., Pennsylvania State University Press, 1990, pp. 312–321.
- [57] J. Heinlein, K. Gharachorloo, S. Dresser, and A. Gupta, “Integration of message passing and shared memory in the stanford FLASH multiprocessor,” in *Proceedings of the sixth international conference on Architectural support for programming languages and operating systems - ASPLOS-VI*, San Jose, California, United States: ACM Press, 1994, pp. 38–50, ISBN: 978-0-89791-660-8. DOI: [10.1145/195473.195494](https://doi.org/10.1145/195473.195494).
- [58] M. Heinrich, D. Ofelt, M. Horowitz, and J. Hennessy, “Hardware/software co-design of the stanford FLASH multiprocessor,” *Proceedings of the IEEE*, vol. 85, no. 3, pp. 455–466, Mar. 1997, ISSN: 00189219. DOI: [10.1109/5.558720](https://doi.org/10.1109/5.558720).
- [59] M. Heinrich, V. Soundararajan, J. Hennessy, and A. Gupta, “A quantitative analysis of the performance and scalability of distributed shared memory cache coherence protocols,” *IEEE Transactions on Computers*, vol. 48, no. 2, pp. 205–217, Feb. 1999, ISSN: 00189340. DOI: [10.1109/12.752662](https://doi.org/10.1109/12.752662).
- [60] M. Heinrich, “The performance and scalability of distributed shared-memory cache coherence protocols,” Ph.D. dissertation, 1998.
- [61] M. Heinrich, M. Horowitz, A. Gupta, M. Rosenblum, J. Hennessy, J. Kuskin, D. Ofelt, J. Heinlein, J. Baxter, J. P. Singh, R. Simoni, K. Gharachorloo, and D. Nakahira, “The performance impact of flexibility in the stanford FLASH multiprocessor,” in *Proceedings of the sixth international conference on Architectural support for programming languages and operating systems - ASPLOS-VI*, San Jose, California, United States: ACM Press, 1994, pp. 274–285, ISBN: 978-0-89791-660-8. DOI: [10.1145/195473.195569](https://doi.org/10.1145/195473.195569).
- [62] M. D. Hill, J. R. Larus, S. K. Reinhardt, and D. A. Wood, “Cooperative shared memory: Software and hardware support for scalable multiprocessors,” in *ASPLOS-V Proceedings - Fifth International Conference on Architectural Support for Programming Languages and Operating Systems, Boston, Massachusetts, USA, October 12-15, 1992*, B. Flahive and R. L. Wexelblat, Eds., ACM Press, 1992, pp. 262–273. DOI: [10.1145/143365.143537](https://doi.org/10.1145/143365.143537).
- [63] M. D. Hill, J. R. Larus, S. K. Reinhardt, and D. A. Wood, “Cooperative shared memory: Software and hardware for scalable multiprocessors,” *ACM Transactions on Computer Systems*, vol. 11, no. 4, pp. 300–318, Nov. 1993, ISSN: 0734-2071, 1557-7333. DOI: [10.1145/161541.161544](https://doi.org/10.1145/161541.161544).
- [64] J. Howard, S. Dighe, Y. Hoskote, S. Vangal, D. Finan, G. Ruhl, D. Jenkins, H. Wilson, N. Borkar, G. Schrom, F. Paillet, S. Jain, T. Jacob, S. Yada, S. Marella, P. Salihundam, V. Erraguntla, M. Konow, M. Riepen, G. Droege, J. Lindemann, M. Gries, T. Apel, K.

- Henriss, T. Lund-Larsen, S. Steibl, S. Borkar, V. De, R. V. D. Wijngaart, and T. Mattson, “A 48-core IA-32 message-passing processor with DVFS in 45nm CMOS,” in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA: IEEE, Feb. 2010, pp. 108–109, ISBN: 978-1-4244-6033-5. DOI: [10.1109/ISSCC.2010.5434077](https://doi.org/10.1109/ISSCC.2010.5434077).
- [65] “Ieee standard for systemverilog–unified hardware design, specification, and verification language,” *IEEE Std 1800-2017 (Revision of IEEE Std 1800-2012)*, pp. 1–1315, 2018. DOI: [10.1109/IEEESTD.2018.8299595](https://doi.org/10.1109/IEEESTD.2018.8299595).
- [66] “Inclusive cache.” (), [Online]. Available: <https://github.com/chipsalliance/rocket-chip-inclusive-cache>.
- [67] Intel Corporation. “IntelSCC.” (), [Online]. Available: <https://www.intel.cn/content/dam/www/public/us/en/documents/technology-briefs/intel-labs-single-chip-platform-overview-paper.pdf>.
- [68] D. James, A. Laundrie, S. Gjessing, and G. Sohi, “Distributed-directory scheme: Scalable coherent interface,” *Computer*, vol. 23, no. 6, pp. 74–77, Jun. 1990, ISSN: 0018-9162. DOI: [10.1109/2.55503](https://doi.org/10.1109/2.55503).
- [69] D. C. Jung, M. Ruttenberg, P. Gao, S. Davidson, D. Petrisko, K. Li, A. K. Kamath, L. Cheng, S. Xie, P. Pan, Z. Zhao, Z. Yue, B. Veluri, S. Muralitharan, A. Sampson, A. Lumsdaine, Z. Zhang, C. Batten, M. Oskin, D. Richmond, and M. B. Taylor, “Scalable, programmable and dense: The hammerblade open-source RISC-V manycore,” in *51st ACM/IEEE Annual International Symposium on Computer Architecture, ISCA 2024, Buenos Aires, Argentina, June 29 - July 3, 2024*, IEEE, 2024, pp. 770–784. DOI: [10.1109/ISCA59077.2024.00061](https://doi.org/10.1109/ISCA59077.2024.00061).
- [70] R. H. Katz, S. J. Eggers, D. A. Wood, C. L. Perkins, and R. G. Sheldon, “Implementing a cache consistency protocol,” *ACM SIGARCH Computer Architecture News*, vol. 13, no. 3, pp. 276–283, Jun. 1985, ISSN: 0163-5964. DOI: [10.1145/327070.327237](https://doi.org/10.1145/327070.327237).
- [71] S. Kommrusch, M. Horro, L.-N. Pouchet, G. Rodriguez, and J. Tourino, “Optimizing coherence traffic in manycore processors using closed-form caching/home agent mappings,” *IEEE Access*, vol. 9, pp. 28 930–28 945, 2021, ISSN: 2169-3536. DOI: [10.1109/ACCESS.2021.3058280](https://doi.org/10.1109/ACCESS.2021.3058280).
- [72] R. Komuravelli, S. V. Adve, and C.-T. Chou, “Revisiting the complexity of hardware cache coherence and some implications,” *ACM Transactions on Architecture and Code Optimization*, vol. 11, no. 4, pp. 1–22, Jan. 9, 2015, ISSN: 1544-3566, 1544-3973. DOI: [10.1145/2663345](https://doi.org/10.1145/2663345).
- [73] C. Kumar, A. Chaudhary, S. Bhawalkar, U. Mathur, S. Jain, A. Vastrad, and E. Rotenberg, “Post-silicon microarchitecture,” *IEEE Computer Architecture Letters*, vol. 19, no. 1, pp. 26–29, Jan. 1, 2020, ISSN: 1556-6056, 1556-6064, 2473-2575. DOI: [10.1109/LCA.2020.2978841](https://doi.org/10.1109/LCA.2020.2978841).
- [74] C. Kumar, A. Seshadri, A. Chaudhary, S. Bhawalkar, R. Singh, and E. Rotenberg, “Post-fabrication microarchitecture,” in *MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture*, Virtual Event Greece: ACM, Oct. 18, 2021, pp. 1270–1281, ISBN: 978-1-4503-8557-2. DOI: [10.1145/3466752.3480119](https://doi.org/10.1145/3466752.3480119).
- [75] A. Kurth, B. Forsberg, and L. Benini, “Herov2: Full-stack open-source research platform for heterogeneous computing,” *IEEE Trans. Parallel Distributed Syst.*, vol. 33, no. 10, pp. 4368–4382, 2022. DOI: [10.1109/TPDS.2022.3189390](https://doi.org/10.1109/TPDS.2022.3189390).
- [76] A. Kurth, P. Vogel, A. Capotondi, A. Marongiu, and L. Benini, “HERO: heterogeneous embedded research platform for exploring RISC-V manycore accelerators on FPGA,” *CoRR*, vol. abs/1712.06497, 2017. arXiv: [1712.06497](https://arxiv.org/abs/1712.06497).
- [77] J. Kuskin, D. Ofelt, M. Heinrich, J. Heinlein, R. Simoni, K. Gharachorloo, J. Chapin, D. Nakahira, J. Baxter, M. Horowitz, A. Gupta, M. Rosenblum, and J. Hennessy, “The stanford FLASH multiprocessor,” in *Proceedings of 21 International Symposium on Computer*

- Architecture*, Chicago, IL, USA: IEEE Comput. Soc. Press, 1994, pp. 302–313, ISBN: 978-0-8186-5510-4. DOI: [10.1109/ISCA.1994.288140](https://doi.org/10.1109/ISCA.1994.288140).
- [78] J. Kuskin, “THE FLASH MULTIPROCESSOR: DESIGNING a FLEXIBLE AND SCALABLE SYSTEM,” Ph.D. dissertation, 1997.
- [79] J. Lee, S. Seo, C. Kim, J. Kim, P. Chun, Z. Sura, J. Kim, and S. Han, “COMIC: A coherent shared memory interface for cell be,” in *Proceedings of the 17th international conference on Parallel architectures and compilation techniques*, Toronto Ontario Canada: ACM, Oct. 25, 2008, pp. 303–314, ISBN: 978-1-60558-282-5. DOI: [10.1145/1454115.1454157](https://doi.org/10.1145/1454115.1454157).
- [80] J. Lee, J. Kim, J. Kim, S. Seo, and J. Lee, “An OpenCL framework for homogeneous manycores with no hardware cache coherence,” in *2011 International Conference on Parallel Architectures and Compilation Techniques*, Galveston, TX, USA: IEEE, Oct. 2011, pp. 56–67. DOI: [10.1109/PACT.2011.12](https://doi.org/10.1109/PACT.2011.12).
- [81] D. Lenoski, J. Laudon, K. Gharachorloo, W.-D. Weber, A. Gupta, J. Hennessy, M. Horowitz, and M. Lam, “The stanford dash multiprocessor,” *Computer*, vol. 25, no. 3, pp. 63–79, Mar. 1992, ISSN: 0018-9162. DOI: [10.1109/2.121510](https://doi.org/10.1109/2.121510).
- [82] A. Li, T.-J. Chang, F. Gao, T. Ta, G. Tziantzioulis, Y. Ou, M. Wang, J. Tu, K. Xu, P. Jackson, A. Ning, G. Chirkov, M. Orenes-Vera, S. Agwa, X. Yan, E. Tang, J. Balkind, C. Batten, and D. Wentzlauff, “Cifer: A cache-coherent 12-nm 16-mm<sup>2</sup> soc with four 64-bit risc-v application cores, 18 32-bit risc-v compute cores, and a 1541 lut6/mm<sup>2</sup> synthesizable efpga,” *IEEE Solid-State Circuits Letters*, vol. 6, pp. 229–232, 2023. DOI: [10.1109/LSSC.2023.3303111](https://doi.org/10.1109/LSSC.2023.3303111).
- [83] T. Lovett and R. M. Clapp, “Sting: A CC-NUMA computer system for the commercial marketplace,” in *Proceedings of the 23rd Annual International Symposium on Computer Architecture, Philadelphia, PA, USA, May 22-24, 1996*, J. Baer, Ed., ACM, 1996, pp. 308–317. DOI: [10.1145/232973.233006](https://doi.org/10.1145/232973.233006).
- [84] P. Mantovani, D. Giri, G. D. Guglielmo, L. Piccolboni, J. Zuckerman, E. G. Cota, M. Petracca, C. Pilato, and L. P. Carloni, “Agile soc development with open ESP : Invited paper,” in *IEEE/ACM International Conference On Computer Aided Design, ICCAD 2020, San Diego, CA, USA, November 2-5, 2020*, IEEE, 2020, 96:1–96:9. DOI: [10.1145/3400302.3415753](https://doi.org/10.1145/3400302.3415753).
- [85] M. Martin, M. Hill, and D. Wood, “Token coherence: Decoupling performance and correctness,” in *30th Annual International Symposium on Computer Architecture, 2003. Proceedings.*, San Diego, CA, USA: IEEE Comput. Soc, 2003, pp. 182–193, ISBN: 978-0-7695-1945-6. DOI: [10.1109/ISCA.2003.1206999](https://doi.org/10.1109/ISCA.2003.1206999).
- [86] M. M. K. Martin, M. D. Hill, and D. J. Sorin, “Why on-chip cache coherence is here to stay,” *Communications of the ACM*, vol. 55, no. 7, pp. 78–89, Jul. 2012, ISSN: 0001-0782, 1557-7317. DOI: [10.1145/2209249.2209269](https://doi.org/10.1145/2209249.2209269).
- [87] M. Martonosi, D. Ofelt, and M. Heinrich, “Integrating performance monitoring and communication in parallel computers,” in *Proceedings of the 1996 ACM SIGMETRICS international conference on Measurement and modeling of computer systems - SIGMETRICS '96*, Philadelphia, Pennsylvania, United States: ACM Press, 1996, pp. 138–147, ISBN: 978-0-89791-793-3. DOI: [10.1145/233013.233035](https://doi.org/10.1145/233013.233035).
- [88] L. G. Menezes, V. Puente, and J. A. Gregorio, “Rainbow: A composable coherence protocol for `jspan style="font-variant:small-caps;"` multi-chip servers,” *Concurrency and Computation: Practice and Experience*, vol. 32, no. 24, Dec. 25, 2020, ISSN: 1532-0626, 1532-0634. DOI: [10.1002/cpe.5947](https://doi.org/10.1002/cpe.5947).
- [89] L. G. Menezes, V. Puente, and J.-A. Gregorio, “Flask coherence: A morphable hybrid coherence protocol to balance energy, performance and scalability,” in *2015 IEEE 21st Interna-*

- tional Symposium on High Performance Computer Architecture (HPCA)*, Burlingame, CA, USA: IEEE, Feb. 2015, pp. 198–209, ISBN: 978-1-4799-8930-0. DOI: [10.1109/HPCA.2015.7056033](https://doi.org/10.1109/HPCA.2015.7056033).
- [90] M. Miceli, “A coherence-capable write-back l1 data cache for ariane,” Politecnico di Torino, 2023.
- [91] M. Michael, A. Nanda, and Beng-Hong Lim, “Coherence controller architectures for scalable shared-memory multiprocessors,” *IEEE Transactions on Computers*, vol. 48, no. 2, pp. 245–255, Feb. 1999, ISSN: 00189340. DOI: [10.1109/12.752666](https://doi.org/10.1109/12.752666).
- [92] M. M. Michael, A. K. Nanda, B.-H. Lim, and M. L. Scott, “Coherence controller architectures for SMP-based CC-NUMA multiprocessors,” *ACM SIGARCH Computer Architecture News*, vol. 25, no. 2, pp. 219–228, May 1997, ISSN: 0163-5964. DOI: [10.1145/384286.264203](https://doi.org/10.1145/384286.264203).
- [93] S. L. Min and J. Baer, “A timestamp-based cache coherence scheme,” in *Proceedings of the International Conference on Parallel Processing, ICPP '89, The Pennsylvania State University, University Park, PA, USA, August 1989. Volume 1: Architecture*, Pennsylvania State University Press, 1989, pp. 23–32.
- [94] G. E. Moore, “Cramming more components onto integrated circuits,” *Electronics*, vol. 38, no. 8, pp. 114–117, 1965.
- [95] G. E. Moore, “Cramming more components onto integrated circuits,” *Proc. IEEE*, vol. 86, no. 1, pp. 82–85, 1998. DOI: [10.1109/JPROC.1998.658762](https://doi.org/10.1109/JPROC.1998.658762).
- [96] V. Nagarajan, D. J. Sorin, M. D. Hill, and D. A. Wood, *A Primer on Memory Consistency and Cache Coherence* (Synthesis Lectures on Computer Architecture). Springer International Publishing, 2020. DOI: [10.1007/978-3-031-01764-3](https://doi.org/10.1007/978-3-031-01764-3).
- [97] J. von Neumann, “First draft of a report on the EDVAC,” *IEEE Ann. Hist. Comput.*, vol. 15, no. 4, pp. 27–75, 1993. DOI: [10.1109/85.238389](https://doi.org/10.1109/85.238389).
- [98] A. Nowatzky, G. Aybay, M. Browne, E. Kelly, D. Lee, and M. Parkin, “The s3.mp scalable shared memory multiprocessor,” in *Proceedings of the Twenty-Seventh Hawaii International Conference on System Sciences HICSS-94*, Wailea, HI, USA: IEEE Comput. Soc. Press, 1994, pp. 144–153, ISBN: 978-0-8186-5090-1. DOI: [10.1109/HICSS.1994.323149](https://doi.org/10.1109/HICSS.1994.323149).
- [99] A. Nowatzky, M. Monger, M. Parkin, E. Kelly, M. Browne, G. Aybay, and D. Lee, “The s3.mp architecture: A local area multiprocessor,” in *Proceedings of the fifth annual ACM symposium on Parallel algorithms and architectures - SPAA '93*, Velen, Germany: ACM Press, 1993, pp. 140–141, ISBN: 978-0-89791-599-1. DOI: [10.1145/165231.165249](https://doi.org/10.1145/165231.165249).
- [100] A. Nowatzky, G. Aybay, M. C. Browne, E. J. Kelly, M. Parkin, B. Radke, and S. Vishin, “Exploiting parallelism in cache coherency protocol engines,” in *Euro-Par '95 Parallel Processing, First International Euro-Par Conference, Stockholm, Sweden, August 29-31, 1995, Proceedings*, S. Haridi, K. A. M. Ali, and P. Magnusson, Eds., ser. Lecture Notes in Computer Science, vol. 966, Springer, 1995, pp. 269–286. DOI: [10.1007/BFB0020471](https://doi.org/10.1007/BFB0020471).
- [101] OpenSBI. “Opensbi.” (), [Online]. Available: <https://github.com/riscv-software-src/opensbi>.
- [102] *OpenSPARC t1 micro architecture specification*, 2008.
- [103] S. Pai, R. Govindarajan, and M. J. Thazhuthaveetil, “Fast and efficient automatic memory management for GPUs using compiler-assisted runtime coherence scheme,” in *Proceedings of the 21st international conference on Parallel architectures and compilation techniques*, Minneapolis Minnesota USA: ACM, Sep. 19, 2012, pp. 33–42, ISBN: 978-1-4503-1182-3. DOI: [10.1145/2370816.2370824](https://doi.org/10.1145/2370816.2370824).
- [104] M. S. Papamarcos and J. H. Patel, “A low-overhead coherence solution for multiprocessors with private cache memories,” in *Proceedings of the 11th annual international symposium*

- on *Computer architecture - ISCA '84*, Not Known: ACM Press, 1984, pp. 348–354, ISBN: 978-0-8186-0538-3. DOI: [10.1145/800015.808204](https://doi.org/10.1145/800015.808204).
- [105] G. Paulin, P. Scheffler, T. Benz, M. A. Cavalcante, T. Fischer, M. Eggimann, Y. Zhang, N. Wistoff, L. Bertaccini, L. Colagrande, G. Ottavi, F. K. Gürkaynak, D. Rossi, and L. Benini, “Occamy: A 432-core 28.1 dp-gflop/s/w 83% FPU utilization dual-chiplet, dual-hbm2e risc-v-based accelerator for stencil and sparse linear algebra computations with 8-to-64-bit floating-point support in 12nm finfet,” in *IEEE Symposium on VLSI Technology and Circuits 2024, Honolulu, HI, USA, June 16-20, 2024*, IEEE, 2024, pp. 1–2. DOI: [10.1109/VLSITECHNOLOGYANDCIR46783.2024.10631529](https://doi.org/10.1109/VLSITECHNOLOGYANDCIR46783.2024.10631529).
- [106] G. D. Penna, B. Intrigila, I. Melatti, E. Tronci, and M. V. Zilli, “Exploiting transition locality in automatic verification of finite-state concurrent systems,” *International Journal on Software Tools for Technology Transfer*, vol. 6, no. 4, pp. 320–341, Jul. 2004. DOI: [10.1007/s10009-004-0149-6](https://doi.org/10.1007/s10009-004-0149-6).
- [107] D. Petrisko, F. Gilani, M. Wyse, D. C. Jung, S. Davidson, P. Gao, C. Zhao, Z. Azad, S. Canakci, B. Veluri, T. Guarino, A. Joshi, M. Oskin, and M. B. Taylor, “Blackparrot: An agile open-source RISC-V multicore for accelerator socs,” *IEEE Micro*, vol. 40, no. 4, pp. 93–102, 2020. DOI: [10.1109/MM.2020.2996145](https://doi.org/10.1109/MM.2020.2996145).
- [108] S. H. Pugsley, J. B. Spjut, D. W. Nellans, and R. Balasubramonian, “SWEL: Hardware cache coherence protocols to map shared data onto shared caches,” in *Proceedings of the 19th international conference on Parallel architectures and compilation techniques*, Vienna Austria: ACM, Sep. 11, 2010, pp. 465–476, ISBN: 978-1-4503-0178-7. DOI: [10.1145/1854273.1854331](https://doi.org/10.1145/1854273.1854331).
- [109] S. Reinhardt, J. Larus, and D. Wood, “Tempest and typhoon: User-level shared memory,” in *Proceedings of 21 International Symposium on Computer Architecture*, Chicago, IL, USA: IEEE Comput. Soc. Press, 1994, pp. 325–336, ISBN: 978-0-8186-5510-4. DOI: [10.1109/ISCA.1994.288138](https://doi.org/10.1109/ISCA.1994.288138).
- [110] C. Sakalis, C. Leonardsson, S. Kaxiras, and A. Ros, “Splash-3: A properly synchronized benchmark suite for contemporary research,” in *2016 IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS 2016, Uppsala, Sweden, April 17-19, 2016*, IEEE Computer Society, 2016, pp. 101–111. DOI: [10.1109/ISPASS.2016.7482078](https://doi.org/10.1109/ISPASS.2016.7482078).
- [111] D. Sanchez and C. Kozyrakis, “SCD: A scalable coherence directory with flexible sharer set encoding,” in *IEEE International Symposium on High-Performance Comp Architecture*, New Orleans, LA, USA: IEEE, Feb. 2012, pp. 1–12. DOI: [10.1109/HPCA.2012.6168950](https://doi.org/10.1109/HPCA.2012.6168950).
- [112] I. Schoinas, B. Falsafi, A. R. Lebeck, S. K. Reinhardt, J. R. Larus, and D. A. Wood, “Fine-grain access control for distributed shared memory,” in *Proceedings of the sixth international conference on Architectural support for programming languages and operating systems - ASPLOS-VI*, San Jose, California, United States: ACM Press, 1994, pp. 297–306, ISBN: 978-0-89791-660-8. DOI: [10.1145/195473.195575](https://doi.org/10.1145/195473.195575).
- [113] B. C. Schwedock, P. Yoovidhya, J. Seibert, and N. Beckmann, “Tākō: A polymorphic cache hierarchy for general-purpose optimization of data movement,” in *Proceedings of the 49th Annual International Symposium on Computer Architecture*, New York New York: ACM, Jun. 18, 2022, pp. 42–58, ISBN: 978-1-4503-8610-4. DOI: [10.1145/3470496.3527379](https://doi.org/10.1145/3470496.3527379).
- [114] K. Septinus, P. Pirsch, H. Blume, and U. Mayer, “A fully programmable FSM-based processing engine for gigabytes/s header parsing,” in *2010 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation*, Samos, Greece: IEEE, Jul. 2010, pp. 45–54, ISBN: 978-1-4244-7936-8. DOI: [10.1109/ICSAMOS.2010.5642093](https://doi.org/10.1109/ICSAMOS.2010.5642093).
- [115] SiFive, *SiFive TileLink Specification, Version 1.8.1*, 2020.

- [116] D. Sorin, M. Plakal, A. Condon, M. Hill, M. Martin, and D. Wood, “Specifying and verifying a broadcast and a multicast snooping cache coherence protocol,” *IEEE Transactions on Parallel and Distributed Systems*, vol. 13, no. 6, pp. 556–578, Jun. 2002, ISSN: 1045-9219. DOI: [10.1109/TPDS.2002.1011412](https://doi.org/10.1109/TPDS.2002.1011412).
- [117] P. Sweazey and A. J. Smith, “A class of compatible cache consistency protocols and their support by the IEEE futurebus,” *ACM SIGARCH Computer Architecture News*, vol. 14, no. 2, pp. 414–423, May 1986, ISSN: 0163-5964. DOI: [10.1145/17356.17404](https://doi.org/10.1145/17356.17404).
- [118] N. Talati, K. May, A. Behroozi, Y. Yang, K. Kaszyk, C. Vasiladiotis, T. Verma, L. Li, B. Nguyen, J. Sun, J. M. Morton, A. Ahmadi, T. M. Austin, M. F. P. O’Boyle, S. A. Mahlke, T. N. Mudge, and R. G. Dreslinski, “Prodigy: Improving the memory latency of data-indirect irregular workloads using hardware-software co-design,” in *IEEE International Symposium on High-Performance Computer Architecture, HPCA 2021, Seoul, South Korea, February 27 - March 3, 2021*, IEEE, 2021, pp. 654–667. DOI: [10.1109/HPCA51647.2021.00061](https://doi.org/10.1109/HPCA51647.2021.00061).
- [119] C. K. Tang, “Cache system design in the tightly coupled multiprocessor system,” in *Proceedings of the June 7-10, 1976, national computer conference and exposition on - AFIPS ’76*, New York, New York: ACM Press, 1976, p. 749. DOI: [10.1145/1499799.1499901](https://doi.org/10.1145/1499799.1499901).
- [120] Tao Li and L. John, “ADir/sub p/NB: A cost-effective way to implement full map directory-based cache coherence protocols,” *IEEE Transactions on Computers*, vol. 50, no. 9, pp. 921–934, Sep. 2001, ISSN: 00189340. DOI: [10.1109/12.954507](https://doi.org/10.1109/12.954507).
- [121] M. B. Taylor, “Basejump STL: systemverilog needs a standard template library for hardware design,” in *Proceedings of the 55th Annual Design Automation Conference, DAC 2018, San Francisco, CA, USA, June 24-29, 2018*, ACM, 2018, 73:1–73:6. DOI: [10.1145/3195970.3199848](https://doi.org/10.1145/3195970.3199848).
- [122] R. Tedeschi, L. Valente, G. Ottavi, E. Zelioli, N. Wistoff, M. Giacometti, A. B. Sajjad, L. Benini, and D. Rossi, *Culsans: An efficient snoop-based coherency unit for the cva6 open source risc-v application processor*, 2024. arXiv: [2407.19895](https://arxiv.org/abs/2407.19895) [eess.SY].
- [123] C. P. Thacker and L. C. Stewart, “Firefly: A multiprocessor workstation,” in *Proceedings of the second international conference on Architectural support for programming languages and operating systems*, Palo Alto California USA: ACM, Oct. 1987, pp. 164–172. DOI: [10.1145/36206.36199](https://doi.org/10.1145/36206.36199).
- [124] L. Torvalds. “Linux.” (), [Online]. Available: <https://github.com/torvalds/linux>.
- [125] A. Vianes, F. Petrot, and F. Rousseau, “A case for second-level software cache coherency on many-core accelerators,” in *2022 IEEE International Workshop on Rapid System Prototyping (RSP)*, Shanghai, China: IEEE, Oct. 13, 2022, pp. 29–35. DOI: [10.1109/RSP57251.2022.10038999](https://doi.org/10.1109/RSP57251.2022.10038999).
- [126] M. Wang, T. Ta, L. Cheng, and C. Batten, “Efficiently supporting dynamic task parallelism on heterogeneous cache-coherent systems,” in *2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA)*, Valencia, Spain: IEEE, May 2020, pp. 173–186, ISBN: 978-1-72814-661-4. DOI: [10.1109/ISCA45697.2020.00025](https://doi.org/10.1109/ISCA45697.2020.00025).
- [127] Wangyang Lai and Chin-Tau Lea, “A programmable state machine architecture for packet processing,” *IEEE Micro*, vol. 23, no. 4, pp. 32–42, Jul. 2003. DOI: [10.1109/MM.2003.1225965](https://doi.org/10.1109/MM.2003.1225965).
- [128] A. Waterman, “Design of the RISC-V instruction set architecture,” Ph.D. dissertation, University of California, Berkeley, USA, 2016.
- [129] A. Waterman, Y. Lee, R. Avizienis, D. A. Patterson, and K. Asanović, “The RISC-V instruction set manual, volume i: User-level ISA, version 2.0,” University of California, Berkeley, Tech. Rep. UCB/EECS-2016-118, May 2016.

- [130] W.-D. Weber, “Scalable directories for cache-coherent shared-memory multiprocessors,” Ph.D. dissertation, Stanford University, 1993.
- [131] S. C. Woo, M. Ohara, E. Torrie, J. P. Singh, and A. Gupta, “The SPLASH-2 programs: Characterization and methodological considerations,” in *Proceedings of the 22nd Annual International Symposium on Computer Architecture, ISCA '95, Santa Margherita Ligure, Italy, June 22-24, 1995*, D. A. Patterson, Ed., ACM, 1995, pp. 24–36. DOI: [10.1145/223982.223990](https://doi.org/10.1145/223982.223990).
- [132] D. A. Wood, S. K. Reinhardt, S. Chandra, B. Falsafi, M. D. Hill, J. R. Larus, A. R. Lebeck, J. C. Lewis, S. S. Mukherjee, and S. Palacharla, “Mechanisms for cooperative shared memory,” in *Proceedings of the 20th annual international symposium on Computer architecture - ISCA '93*, San Diego, California, United States: ACM Press, 1993, pp. 156–167, ISBN: 978-0-8186-3810-7. DOI: [10.1145/165123.165151](https://doi.org/10.1145/165123.165151).
- [133] M. Wyse. “The bedrock cache coherence protocol and system v1.1.” (2022), [Online]. Available: [https://github.com/black-parrot/black-parrot/blob/master/docs/bedrock\\_protocol\\_specification.pdf](https://github.com/black-parrot/black-parrot/blob/master/docs/bedrock_protocol_specification.pdf).
- [134] M. Wyse, D. Petrisko, F. Gilani, Y.-M. Chueh, P. Gao, D. C. Jung, S. Muralitharan, S. V. Ranga, M. Oskin, and M. Taylor, *The blackparrot bedrock cache coherence system*, 2022. arXiv: [2211.06390](https://arxiv.org/abs/2211.06390) [cs.AR].
- [135] Y. Yoon, N. Concer, M. Petracca, and L. P. Carloni, “Virtual channels and multiple physical networks: Two alternatives to improve noc performance,” *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 32, no. 12, pp. 1906–1919, 2013. DOI: [10.1109/TCAD.2013.2276399](https://doi.org/10.1109/TCAD.2013.2276399).
- [136] F. Zaruba and L. Benini, “The cost of application-class processing: Energy and performance analysis of a linux-ready 1.7-GHz 64-bit RISC-v core in 22-nm FDSOI technology,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 11, pp. 2629–2640, Nov. 2019, ISSN: 1063-8210, 1557-9999. DOI: [10.1109/TVLSI.2019.2926114](https://doi.org/10.1109/TVLSI.2019.2926114).
- [137] F. Zaruba, F. Schuiki, and L. Benini, “Manticore: A 4096-core RISC-v chiplet architecture for ultraefficient floating-point computing,” *IEEE Micro*, vol. 41, no. 2, pp. 36–42, Mar. 1, 2021, ISSN: 0272-1732, 1937-4143. DOI: [10.1109/MM.2020.3045564](https://doi.org/10.1109/MM.2020.3045564).
- [138] C. Zhang, Y. Zeng, J. Shalf, and X. Guo, “RnR: A software-assisted record-and-replay hardware prefetcher,” in *2020 53rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)*, Athens, Greece: IEEE, Oct. 2020, pp. 609–621, ISBN: 978-1-72817-383-2. DOI: [10.1109/MICRO50266.2020.00057](https://doi.org/10.1109/MICRO50266.2020.00057).
- [139] M. Zhang, A. R. Lebeck, and D. J. Sorin, “Fractal coherence: Scalably verifiable cache coherence,” in *2010 43rd Annual IEEE/ACM International Symposium on Microarchitecture*, Atlanta, GA, USA: IEEE, Dec. 2010, pp. 471–482, ISBN: 978-1-4244-9071-4. DOI: [10.1109/MICRO.2010.11](https://doi.org/10.1109/MICRO.2010.11).
- [140] J. Zhao, A. Agrawal, B. Nikolic, and K. Asanović, “Constellation: An open-source soc-capable noc generator,” in *2022 15th IEEE/ACM International Workshop on Network on Chip Architectures (NoCArc)*, IEEE, 2022, pp. 1–7.
- [141] J. Zhao, B. Korpan, A. Gonzalez, and K. Asanovic, *Sonicboom: The 3rd generation berkeley out-of-order machine*, May 2020.
- [142] Zhiyuan Li, “Software assistance for directory-based caches,” in *Proceedings of 8th International Parallel Processing Symposium*, Cancun, Mexico: IEEE Comput. Soc. Press, 1994, pp. 151–157, ISBN: 978-0-8186-5602-6. DOI: [10.1109/IPPS.1994.288307](https://doi.org/10.1109/IPPS.1994.288307).
- [143] C. Zilles and G. Sohi, “A programmable co-processor for profiling,” in *Proceedings HPCA Seventh International Symposium on High-Performance Computer Architecture*, Monterrey,

Mexico: IEEE Comput. Soc, 2001, pp. 241–252, ISBN: 978-0-7695-1019-4. DOI: [10.1109/HPCA.2001.903267](https://doi.org/10.1109/HPCA.2001.903267).

- [144] E. Zürich. “PULP Platform.” (2013), [Online]. Available: <https://pulp-platform.org/index.html>.