LOW NOISE DESIGN TECHNIQUES FOR RADIO FREQUENCY INTEGRATED CIRCUITS

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Abstract

Low Noise Design Techniques for Radio Frequency Integrated Circuits

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Wireless communication has experienced explosive growth world-wide in the last decade and its huge market potential is driving relentless efforts in the information industry to improve the performance of wireless communication systems. Academia has also witnessed a flourish of research activities in communications, digital signal processing and radio frequency integrated circuit design.

A major objective of wireless communication is the need to operate in hostile environments while achieving accurate transmission and reception of information, in which one of the great challenges is achieving sufficient fidelity in the presence of "unwanted signals" such as noise and interference nearby. For example, the ubiquitous thermal noise in electronic circuits degrades the signal-to-noise ratio

(SNR) of received signals. In this dissertation this critical issue is addressed in the development of low-noise design techniques for radio frequency integrated circuits. Although the discussion is focused primarily on *Complementary Metal Oxide Semiconductor* (CMOS) technology, some of the techniques described in the thesis are also applicable to bipolar junction transistor (BJT) technologies.

Low-noise amplifier (LNA) is a critical amplification stage in the on-chip portion of a receiver chain, which requires low noise and high gain. In this dissertation, a novel g_m-boosted common-gate LNA (CGLNA) architecture is proposed herein that exhibits lower noise figure with lower power consumption than the conventional CGLNA. It preserves the advantage of insensitivity to parasitics at input and is well suitable for high-frequency applications.

The spectral purity of the local oscillator (LO) signal is of great importance since it directly affects the SNR of the down-converted signal. The LO signal is usually generated using a phase-locked loop (PLL) wherein the required voltage-controlled oscillator (VCO) is often the main source of phase noise. In this work, a novel differential Colpitts VCO and a quadrature VCO are proposed that result in lower phase noise and more robust start-up characteristics than previous approaches.

In contrast to the belief that RF circuit design is a mature subject, this dissertation demonstrates that significant performance benefits are obtained with continued design innovations. With the aggressive scaling of CMOS technology, efforts in CMOS RF IC design will continue for many years into the future.

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As an outstanding teacher, Professor Allstot deserves for his passion in teaching, his humor in class and his ability to provide simple explanation on profoundness, which accounts for the popularity of his series analog IC courses at UW.

I am grateful to my reading committee member, Professor Mani Soma, Professor Richard Shi and Dr. Monte Mar for taking time to serve on my general and final exam committee. In particular, I would like to thank Dr. Monte Mar for taking the time to read my dissertation and for his high standard and helpful suggestions which improve the dissertation.

I appreciate the helpful discussions and friendship offered by my colleagues in SOC group at UW. I would like to thank Mr. Sudip Shekhar, a bright people to work with, for always being a source of help and for his stimulating discussion on research, his hard work on transformer modeling and all of his great help in measurement activity during final time. The measurement could not have been finished without him.

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Finally, I would like to thank my parents and sister for their deeply love and high expectations which have been and will be sources of support and encouragement during my whole life. They taught me to be honest, nice and hardworking, which I will remember forever.

DEDICATION

TO MY PARENTS

Chapter 1 : Introduction

1.1 Motivation

Wireless communication has experienced a global boom in the last decade because it enables easier communication among individuals. For example, the cellular telephone will become even more popular because of its convenience and added features. Wireless communication also provides more convenient access to information; e.g., wireless LAN allows one to access the Internet without having to connect to the network physically. Nowadays it is very common to see one exploring the Internet at a coffee bar. The huge market value of wireless communication systems has driven non-stop efforts in the information industry to improve the performance of wireless communication systems. Academia has also witnessed a flourish of wireless communications research in the fields of communication, digital signal processing and integrated circuit design.

In wireless communications, the information must be transmitted and received with acceptable fidelity. Unfortunately, wireless communication systems usually operate in a hostile environment, which makes transmission and reception more difficult. One of the great challenges in wireless communications is that the system should tolerate a hostile environment, as for example in the presence of "unwanted signals". More specifically, interferers from the environment that contains many unrelated RF signals and noise associated with the device itself can degrade transceiver performance drastically if care is not taken in design of such systems.

Selectivity and sensitivity are two important characteristics of wireless communication systems. Both reflect the ability of a system to transmit and receive information in the presence of interferers and noise. Selectivity denotes the ability of a receiver to detect a weak desired signal accompanied by large interferers that may cause distortion and degrade the fidelity of received signal. Sensitivity is related to noise in the receiver, which is another important source of an "unwanted signal". For the system to reliably detect the received signal, it is usual that the signal be at least as strong as the noise level. Hence, noise sets the lower bound of the received signal, which is usually called the sensitivity of the receiver [1].

Recently, much research effort has been focused on CMOS implementations of low-cost high-performance wireless communication systems, mainly owing to the aggressive scaling of CMOS, which provides the capability of integrating large-scale complex digital signal processing circuitry with lower cost compared to Bipolar, SiGe and GaAs integrated circuit technologies.

In this dissertation low-noise design techniques for radio frequency integrated circuits implemented in CMOS technology are explored. Some of the techniques can also be applied to bipolar technology, although the discussion in later chapters is focused primarily on CMOS implementations.

1.2 Overview

This dissertation is organized as follows. In Chapter 2, a brief introduction to several popular receiver architectures is given. Specifically, the superheterodyne receiver, direct conversion receiver and image rejection architectures are discussed. Tradeoffs in choosing architectures are also highlighted. In Chapter 3, design considerations of CMOS low-noise amplifiers are discussed, including optimization

of the noise figure of the common-source LNA, and a comparison of CMOS LNA topologies. Next, a new topology called the g_m-boosted CGLNA is introduced. It is shown that the g_m-boosted CGLNA exhibits lower noise figure and consumes less power than the conventional CGLNA. Next, several possible implementations of it are described.

Chapter 4 begins with a brief introduction to basic oscillation principles followed by a detailed discussion of phase noise of an oscillator. Comparisons between cross-coupled and Colpitts LC oscillators based on performance parameters such as phase noise, start-up characteristics and tuning range are given. The comparisons portend the possibility of improving the phase noise of a conventional Colpitts oscillator and lead to the introduction of a novel differential Colpitts VCO. Finally, a quadrature VCO (QVCO) based on the new differential Colpitts configuration is described.

Experimental data is given in Chapter 5 including detailed implementation, testing setup and measured results. Chapter 6 concludes the thesis.

Chapter 2 : Receiver Architectures

The goal of radio reception is to detect and extract selectively the desired RF signal in the presence of noise and interference. Amazingly, in a hostile wireless communication environment, the interference may be as much as twelve orders of magnitude larger than the desired signal! Because there are currently many devices operating with multiple standards at the same time and in the same space, it is often possible that an interferer lies very close in frequency to the desired signal in the spectral band of interest. The strong interferers within the crowded spectrum exacerbate the task of detecting the desired signal and rejecting the unwanted interference signals.

In Chapter 1, we defined the selectivity and sensitivity of a receiver, and in this chapter we discuss those concepts in a stricter sense. Following that, the currently most popular receiver architecture is described and comparisons among the receiver architectures are highlighted based on system-level tradeoffs. Some of the most important issues in homodyne receivers such as DC offset voltages, flicker noise and image rejection are also briefly discussed.

2.1 Radio Reception

In receiving the RF signal from the antenna and the external band select filter, the receiver should fulfill the following important functions.

- Provide sufficient amplification for the desired RF signal. Since the received signal from the antenna and band select filter is at a very low power level and

the output of the RF front end is usually digitized by the base band or intermediate frequency analog-to-digital converter (ADC), the overall required gain of the front end should typically be 60-100dB!

- Perform demodulation to extract the digital information. The information modulated with the carrier needs to be recovered or demodulated which involves first down converting the signal from the RF carrier frequency to a lower intermediate frequency (IF) or directly to a base band frequency. Demodulation is usually performed at the base band frequencies because complex modulation and demodulation methods are often used to achieve high signal-to-noise ratios (SNR) with correspondingly low bit-error-rates (BER).

- Suppress all unwanted signals to the degree necessary.

As discussed previously, during RF reception unwanted signals such as noise and interference may corrupt the weak desired signal, which imposes a great challenge for radio reception.

Noise is one kind of "unwanted signal" accompanying the desired signal. It is random in nature and usually has an average value of zero in typical electronic devices. Consequently, noise is often characterized using its variance or equivalently its noise power.

Noise is ubiquitous in electronic components. Among the many noise sources, the thermal noise from a resistor is extremely important because resistors are commonly used; in fact, thermal noise is so common that other forms of noise are often expressed in the form of equivalent "thermal resistance". This endeavor has resulted in a clear physical representation of noise performance as is discussed later.

The study of noise in electronics began early in the 20th century. In 1928, Johnson and Nyquist found that the noise associated with a resistance is white in terms of its spectral content [2]. They also observed that the available power of thermal noise from a resistor is only determined by the bandwidth of interest for a given temperature as given by

$$P_{n,available} = kT\Delta f \tag{2-1}$$

where k is the Boltzmann's constant and T is the absolute temperature.

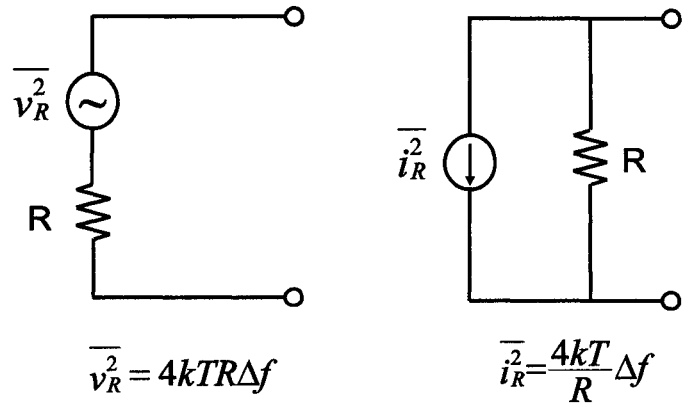


Figure 2-1 Noise model for the thermal noise of a resistor

However, it seems more convenient to express the noise in terms of an equivalent voltage or current for the purposes of circuit calculations. Since the maximum power delivered to a load resistor is achieved with the conjugate matching condition, the available power is

$$P_{n,available} = \left(\frac{v}{2R}\right)^2 R = \frac{v^2}{4R} \tag{2-2}$$

Substituting (2-1) into (2-2), we obtain the equivalent mean squared noise voltage as

$$\overline{v_R^2}=4kTR\Delta f\ .$$

Similarly, the Norton equivalent mean squared noise current is

$$\overline{i_R^2}=\frac{4kT\Delta f}{R}\ .$$

The equivalent Thévenin and Norton noise models for a resistor are shown in Figure 2-1.

In addition to thermal noise, there are other important noise sources such as channel thermal noise, induced gate current noise and flicker noise in MOSFETs, shot noise in BJTs, etc. These are discussed in detail in Chapter 3.

In an RF receiver, the presence of noise degrades the signal-to-noise ratio, which is related to the BER. The relationship between BER and SNR is determined by the specific modulation technique used in the receiver. In general, BER is related to SNR through the Q function (cumulative density function associated with a Gaussian probability density function) defined as

$$Q(x)=\frac{1}{\sqrt{2\pi}}\int_{\infty}^{x}\exp(-\frac{u^2}{2})du$$

For example, for binary phase-shift key (BPSK) modulation, BER depends on SNR as

$$BER=Q\left(\sqrt{\frac{E_d}{2N_0}}\right)$$

where E_d is the energy of signal and $N_0/2$ is the power spectral density of additive white noise [3].

In a receiver, the antenna usually has an equivalent source resistance of 50Ω, which adds thermal noise to the received signal and thus limits the SNR. When the received signal passes through the receiver chain, SNR decreases due to the noise added by subsequent stages (comprising either passive or active devices) in the receiver. At the output of the receiver, a certain minimum SNR is required to maintain BER below a preset value, for example, BER = 10^{-3}. Consequently, this sets a lower bound on the signal power that can be reliably detected with the antenna—the sensitivity of the receiver defined as the minimum signal level that the system can reliably detect.

Clearly, it is hoped that a receiver adds as little noise power as possible so that SNR degradation is minimized. In general, either noise factor (F) or noise figure (NF) is used to characterize the noise performance of a system. Noise factor represents how much the input signal-to-noise ratio is degraded at the output by the added noise from the given network. Noise figure is just noise factor expressed in dB.

$$F \equiv \frac{(S/N)_{in}}{(S/N)_{out}}$$

$$= \frac{\textit{Total output noise power}}{\textit{Output noise power due to input source impedance}}$$

$$= 1 + \frac{\textit{Output noise power added by the network}}{\textit{Output noise power due to input source impedance}}$$

$$NF = 10\log_{10}(F)\,[\text{dB}]$$

For a given required minimum signal-to-noise ratio at the output, sensitivity is expressed as

$$P_{in\_sig} = NF + (SNR)_{out} - 174 dBm/Hz + 10\log_{10}(BW)$$

where $(SNR)_{out}$ is the signal-to-noise ratio at output, and BW is the channel bandwidth.

It is seen from the above expression that sensitivity is limited by the noise performance of the receiver for a given SNR at its output. It constitutes the lower end of the dynamic range in an RF system. Therefore, minimizing noise power added by the receiver is essential for increasing its dynamic range.

In summary, the noise performance of receiver, e.g., NF, determines the sensitivity of the receiver.

In addition to amplifying the desired signal, the receiver should also reject interference sufficiently so that it does not overwhelm the desired signal and saturate various gain stages. The ability to selectively detect a desired signal is called the selectivity of receiver.

Selectively is quantified by many factors. One of the most important factors is the non-linearity created in an amplifier, a mixer, etc. For a weakly nonlinear circuit, Taylor expansion can be applied so that the output v_o is related to input v_i as

$$v_o = c_0 + c_1 \cdot v_i + c_2 \cdot v_i^2 + c_3 \cdot v_i^3 + \ldots \qquad (2\text{-}3)$$

where coefficient c_0 represents the DC term, c_1 corresponds to the linear gain, and coefficients c_2 and c_3 represent the second- and third-order distortion components, respectively.

Suppose two tones with equal amplitude A at frequencies ω_1 and ω_2 are input to an amplifier. Due to the nonlinearity described in (2-3), intermodulation distortion

(IM) terms at $p\omega_1 \pm q\omega_2$ appear at the output. Among these IM products, the second- and third-order terms are especially troublesome. For example, the third-order IM products at frequencies $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ may fall in the frequency band of interest and corrupt the desired signal if not sufficiently suppressed. In RF applications, the input-referred intermodulation products (IIP) are often cited as measures of linearity. For example, the input-referred third-order intercept point (IIP3) is defined at the intersection of the extrapolated fundamental and third-order IM products on a logarithmic scale as depicted in Figure 2-2. The input-referred second-order intermodulation product (IIP2) is determined in a similar way. IIP2 (IIP3) is more important in a direct conversion (heterodyne) receiver as discussed later.

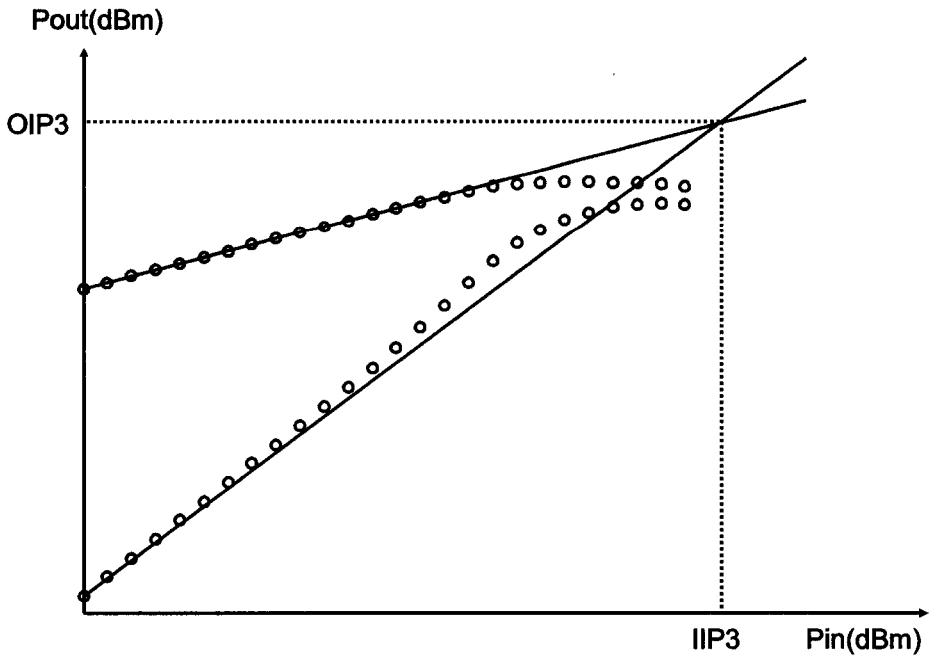


Figure 2-2 Definition of IIP3

2.2 Receiver Architectures

Next, we briefly discuss various receiver architectures.

2.2.1 Superheterodyne (Heterodyne) Receiver

The superheterodyne is probably the most popular receiver architecture since being invented by Armstrong in 1918. Even now the superheterodyne receiver is viewed as the most reliable method for achieving radio reception [4]. The superheterodyne architecture is shown in Figure 2-3.

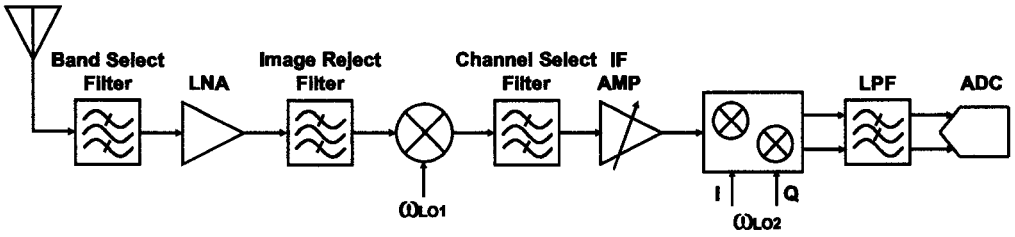


Figure 2-3 Superheterodyne double-IF receiver architecture

In a superheterodyne receiver, an RF band select filter removes out-of-band interferers after which the signal is amplified by a low-noise amplifier. Placing such an amplification stage as close to the antenna as possible helps suppressing noise contributions from the following stages. The image reject filter attenuates interference at the so-called "image" frequencies before the signal at the LNA output is down-converted in frequency by a mixer. The mixer performs the down-conversion and the channel select filter removes interferers in the adjacent channels. The amplifier at IF, usually with variable gain, relaxes the distortion and dynamic range requirement of the subsequent blocks. The signal at IF is further down-converted to base band by a quadrature down-converter and a base band filter

(usually a low pass filter) performs further attenuation of the interference. The base band signal is subsequently digitized by an ADC and processed in the digital domain.

The most attractive feature of a superheterodyne receiver is that the required high gain is distributed along the receiver chain to achieve a good tradeoff between NF and IIP3. Figure 2-3 shows a "dual IF" structure in which the down-conversion is achieved in two steps. By progressively decreasing the IF frequency in this manner, the requirements for the quality factor of the off-chip filters are relaxed [5]. In a single IF structure, the down-conversion is performed in one step. However, the narrow channel bandwidth requires a very high quality factor for the image reject and channel select filters and therefore increases the cost.

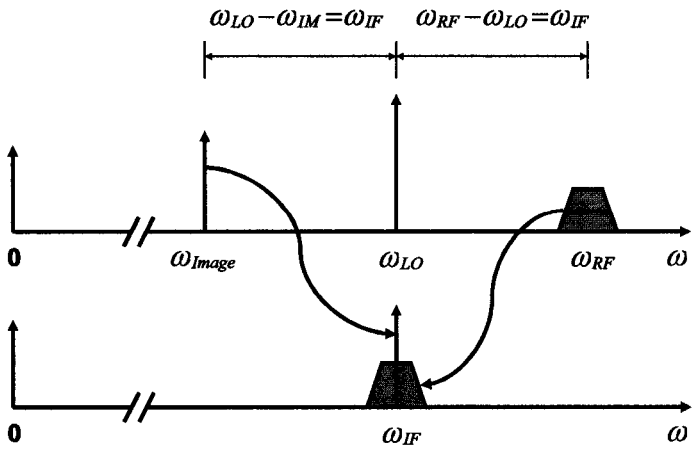


Figure 2-4 Image problem in superheterodyne receiver

The image problem is another serious issue as illustrated in Figure 2-4. The origin of the image problem is actually that while down converting the desired RF signal

to the intermediate frequency (IF), the mixer also down converts the energy at the image frequency to the same IF frequency if the image frequency satisfies

$$\omega_{RF} - \omega_{LO} = \omega_{LO} - \omega_{IM} = \omega_{IF}$$

Unfortunately, the interference power at the image frequency can be much larger than the desired signal in magnitude, which requires that the receiver have a large image rejection ratio (IRR). Typically IRR is as high as 60dB, a difficult value to achieve in practice considering typical process, voltage, and temperature variations in IC technologies.

The intermediate frequency is a critical parameter in heterodyne receiver design, which involves a fundamental tradeoff between image rejection and channel selection. More specifically, a higher IF eases image rejection because the image frequency is further away from the desired frequency. However, a lower IF leads to a larger rejection of the interference of adjacent channels.

In a heterodyne receiver, the required image rejection and channel selection with highly selective transfer functions necessitate the use of passive and discrete implementations, which are incompatible with an integrated solution that targets low cost [6][7]. The off-chip filters also require the LNA to drive the 50Ω input impedance of the image rejection filter, leading to greater power consumption.

2.2.2 Image Reject Architecture

To alleviate the problem of image rejection, an image-reject architecture such as a Hartley receiver can be used as shown in Figure 2-5.

The operation of the Hartley structure can be analyzed mathematically or graphically. Herein, a graphical explanation is given for easier visualization as

shown in Figure 2-6. In the frequency domain, a 90° phase shift is equivalent to multiplying the spectrum by $G(\omega) = -j \cdot \mathrm{sgn}(\omega)$. In other words, the 90° phase shift multiplies the positive frequency part by $-j$ and the negative frequency part by $+j$.

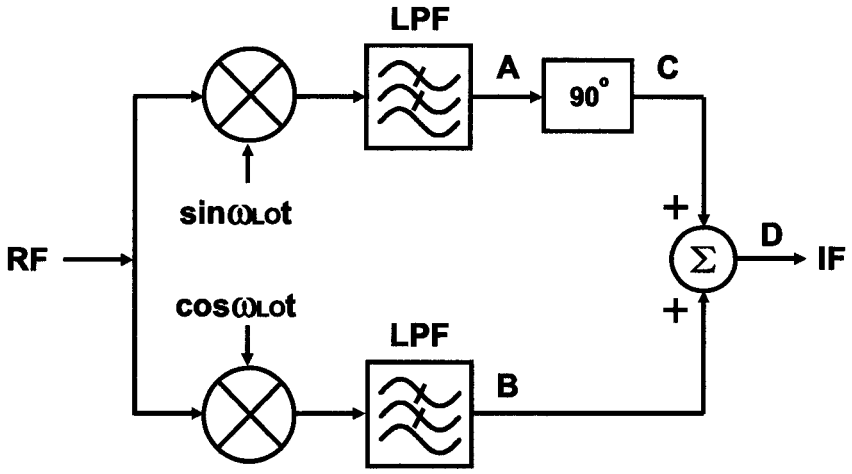
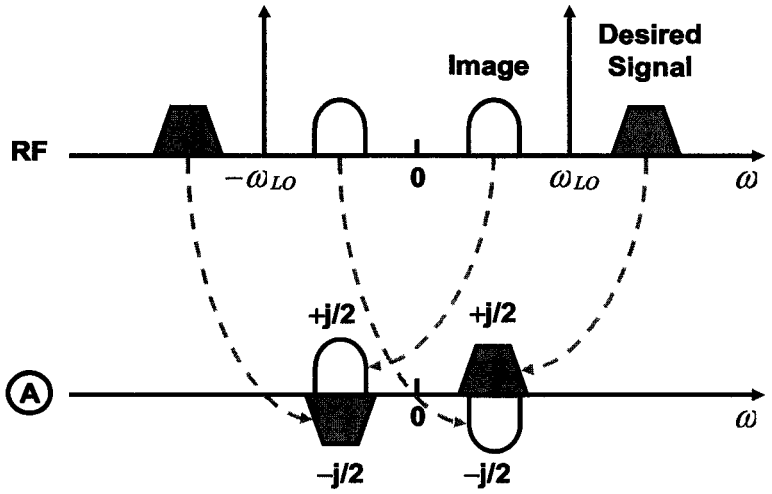
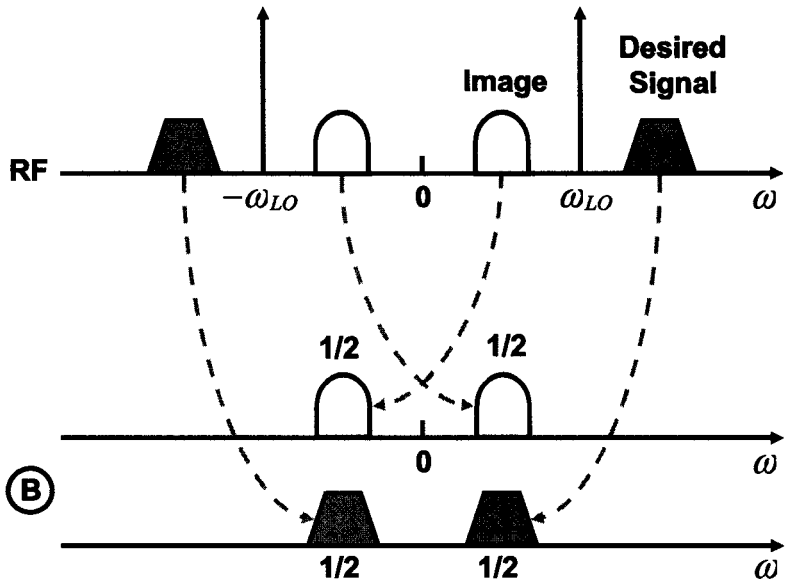


Figure 2-5 Hartley structure

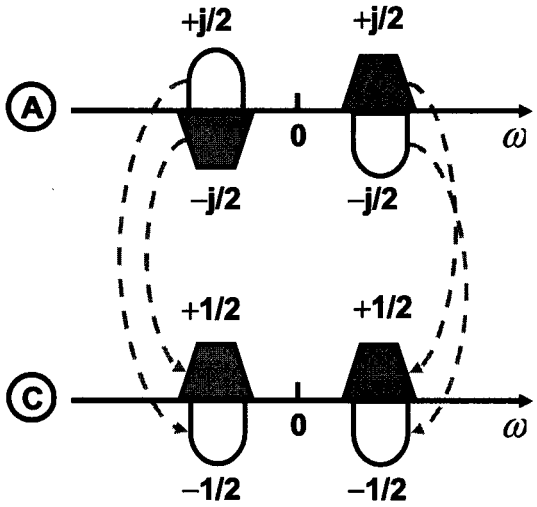


(a)

Figure 2-6 Cancellation of an image signal in a Hartley receiver

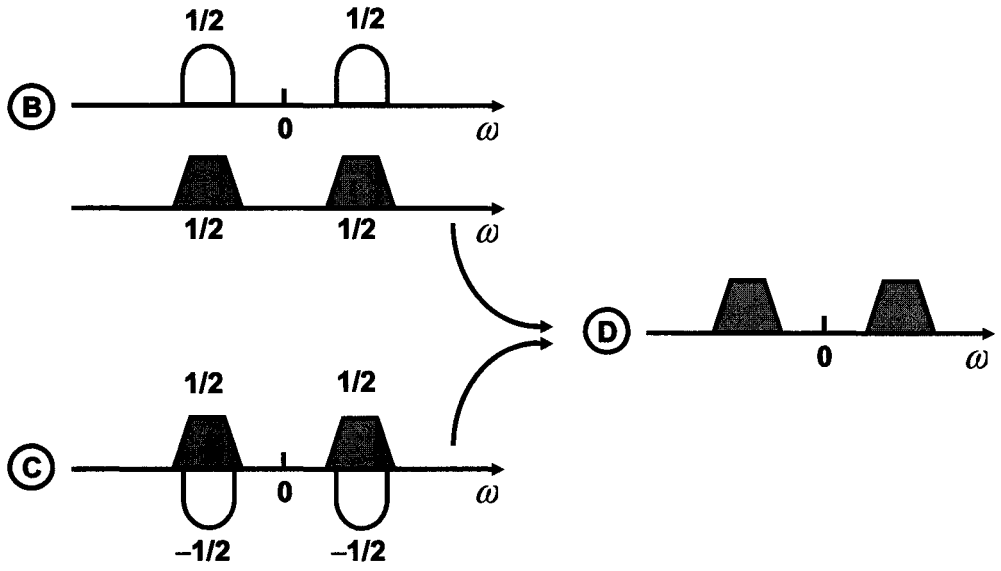


(b)



(c)

Figure 2-6 Cancellation of an image signal in a Hartley receiver (continued)



(d)

Figure 2-6 Cancellation of an image signal in a Hartley receiver (continued)

Intuitively, the cancellation relies on perfect matching between the in-phase (I) and quadrature (Q) paths, and a simple calculation reveals that this is true. It turns out that IRR depends on the relative amplitude error and phase error between the I and Q paths according to

$$IRR = \frac{1-2(1+\varepsilon)\cos\theta+(1+\varepsilon)^2}{1+2(1+\varepsilon)\cos\theta+(1+\varepsilon)^2}.$$

For small ε and θ, the above expression can be simplified to

$$IRR = \frac{\varepsilon^2+\theta^2}{4}.$$

Therefore, IRR depends on the matching between I- and Q-channels. In practice, it is quite difficult to maintain mismatch less than 0.1%, which leads to an IRR of -60dB.

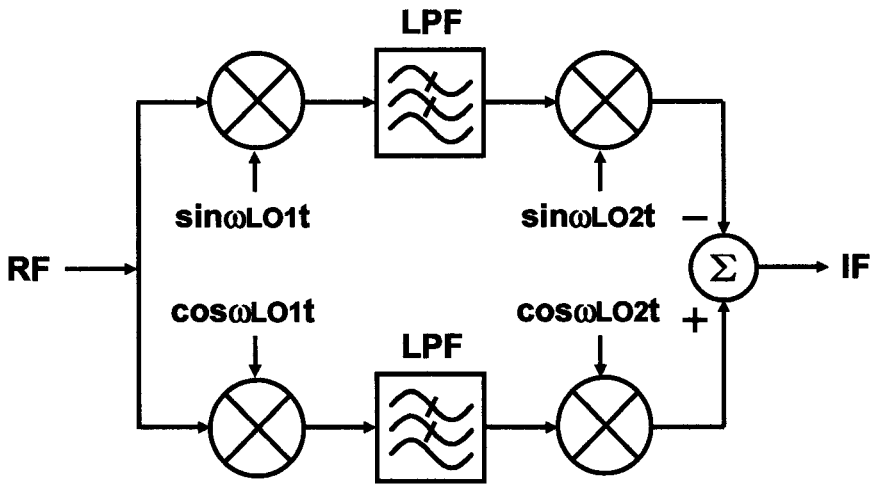


Figure 2-7 Weaver receiver

The 90° phase shift required in a Hartley receiver is difficult to implement. Alternatively, the Weaver structure (Figure 2-7) provides another similar approach to cancel the image signal in that the signal and image are processed differently to allow the cancellation. It can also be analyzed graphically similar to that shown in Figure 2-6, but it is not presented here for the sake of brevity.

2.2.3 Direct Conversion Receiver

A direct conversion receiver (DCR) is also called a zero-IF (ZIF) or homodyne receiver (Figure 2-8). It down-converts RF signal frequencies directly to base band frequencies [8]. Since the IF is at zero frequency or DC, the problem of the image is naturally eliminated as well as the requirement for an off-chip image reject filter, resulting in a more compact structure with lower cost. Since the LNA directly

drives the mixer, there is no need to drive the 50-Ω impedance of an off-chip image-reject filter, which reduces power consumption.

Due to its compactness, a direct conversion receiver is more amenable to monolithic integration. However, despite its simplicity, the DCR does have some performance issues relating to DC offset, flicker noise, even-order distortion and local-oscillator (LO) leakage, that impede its widespread adoption [9].

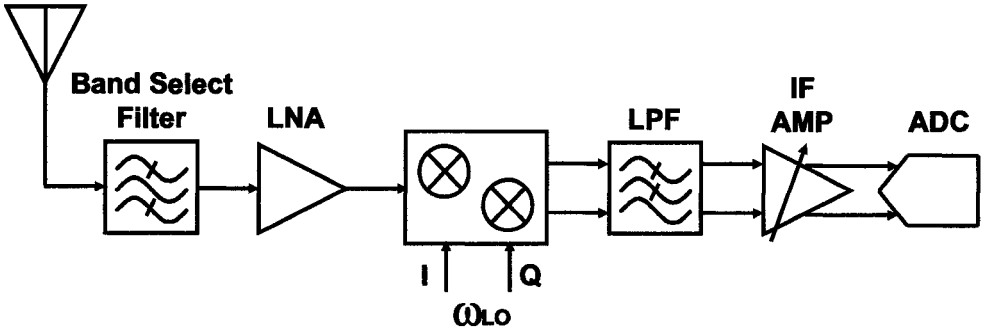


Figure 2-8 Direct conversion receiver

1. DC Offset

Since in DCR the IF frequency is at base band, any DC offset can easily overwhelm the desired signal and saturate the following stages. One of the most important origins of DC offset voltage is the so-called "LO self-mixing" [10]. For example, if the isolation between the various signal ports of a mixer is not perfect, a certain amount of the LO signal is coupled to the input of the LNA or mixer (through capacitive coupling or substrate coupling). The LO leakage is then amplified and mixed with LO signal itself, resulting in a DC offset voltage at the output of the mixer. The DC offset is further amplified by the IF amplifier and may saturate the following ADC stages.

2. Flicker Noise

Flicker noise is low frequency noise that can affect the mixer noise performance significantly, and base band circuits also suffer from it. To minimize it, it is possible to increase the sizes of the MOSFET transistors (both W and L) used in the base band circuits. However, increasing the area of the transistor dramatically lowers its bandwidth, which is an unacceptable penalty to pay for RF circuits such as mixers. If the output of mixer resides at a very low frequency that is within the corner frequency of the flicker noise, the overall SNR can drop significantly. This is more severe for a narrow bandwidth standard such as GSM where the channel bandwidth is only $200KHz$. Flicker noise imposes difficulties in implementing a direct conversion receiver for GSM applications.

3. Even-order Distortion

A DCR also suffers from even-order distortion, especially second-order distortion. First, if two interferers exist at the input of the LNA, a low frequency distortion product appears at its output due to the second-order distortion. If an ideal mixer follows the LNA, this low frequency distortion is translated to a higher frequency and does not affect the down-converted signal at all. However, in reality, imbalances in the mixer and any deviation from a 50% LO duty cycle cause a finite amount of feed through from the RF to IF ports. Thus, the low frequency second-order distortion from the LNA can appear at the mixer output and degrade the signal-to-distortion ratio (SDR).

The second-order harmonic distortion product at the LNA output can also be down-converted to the base band if it is mixed with the second-order harmonic of the LO signal. Similarly, higher order harmonics can be down-converted to base band through the same mechanism. Since the magnitudes of higher order harmonics are inversely proportional to frequency, in practice only second-order components are

significant. Although differential circuits can be employed to suppress even-order distortion terms, mismatches limit the cancellation to about 40dB in practice.

2.2.4 Wideband IF Receiver

A wideband IF architecture [11] can be viewed as extension of the Weaver structure as shown in Figure 2-9.

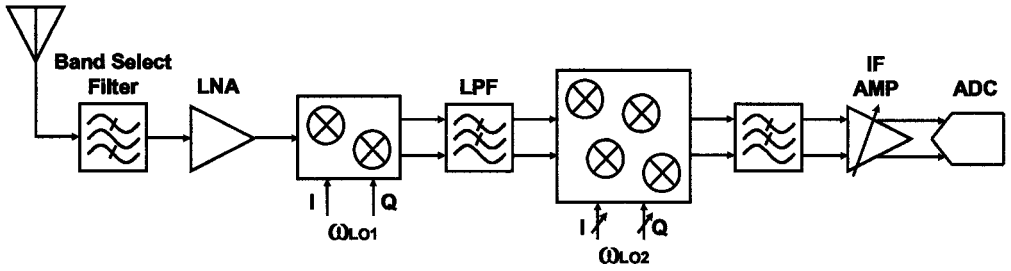


Figure 2-9 Wideband IF receiver

In the wideband IF architecture, the first down-conversion is controlled by a fixed LO signal that translates all channels from RF to IF. The up-converted frequency components are then filtered away using a low pass filter. Then, the second down-conversion stage directly moves the signal from IF to base band by means of a tunable frequency synthesizer. The base band low pass filter performs channel selection and removes signals at alternate channels. As can be seen, the second down-conversion stage is very similar to a direct conversion structure. However, since it operates at a low frequency compared to the RF frequency, the low frequency IF synthesizer consumes much less power and does not require an on-chip high-Q inductor. In addition, the RF LO signal has a fixed frequency, which allows a higher reference frequency to be used and thus provides a wider loop bandwidth for the phase-locked loop. The higher loop bandwidth suppresses phase

noise from the VCO, which can therefore be implemented using a low-Q on-chip inductor.

In addition to the feasibility of achieving low phase noise with on-chip low-Q inductors, the wideband IF architecture also eliminates the LO self-mixing problem since the LO frequency is different from the RF carrier frequency, just like in the superheterodyne receiver.

2.3 Summary

In this chapter, some basic concepts in RF design such as sensitivity, selectivity and noise figure are reviewed. Several popular receiver architectures such as the superheterodyne, direct conversion and image reject receivers are briefly discussed. The various system-level tradeoffs are highlighted as well, including important issues such as DC offset, flicker noise in homodyne receivers, image rejection, etc.

Chapter 3 : Design of Low Noise Amplifier

The ever-increasing interest in wireless communication systems is emphasizing higher levels of integration, more complex functionalities and lower cost. Recently, CMOS has emerged as a viable candidate for RF and microwave integrated circuits (MIC) thanks to the continued scaling of its minimum feature size. Its ability to integrate complex digital signal processing functions makes CMOS a more attractive candidate for system-on-chip (SOC) implementations.

System-on-chip solutions necessitate the implementation of different analog building blocks on the same die together with the large-scale digital integrated circuits that are required for complex digital signal processing functions. Unfortunately, parasitic coupling effects present in silicon technology (especially through the common silicon substrate) allow the switching of digital circuitry to corrupt the weak analog RF signal. As a result, the analog signal is more susceptible to the "noisy" environment produced by the switching digital circuitry in SOC solutions. Consequently, low-noise design is one the most challenging requirements in such systems.

As mentioned in Chapter 2, noise factor (F) or noise figure (NF) is often used to characterize the noise performance of an RF system. It represents the ratio of total output noise power to the output noise power due to input source impedance only. An ideal noiseless circuit adds no noise and hence F=1 or NF=0dB. In general, noise factor is a function of source impedance; different source impedances result in different noise factor values. Fortunately, the building blocks in most RF systems

are designed to have 50Ω input and output impedances, which eliminates the ambiguity of the noise factor definition in RF systems.

As implied by the definition of noise figure, one should minimize the ratio of noise added by the network to the noise contributed by the source impedance so as to minimize the signal-to-noise ratio degradation. This in turn improves the sensitivity of the receiver, as discussed in Chapter 2.

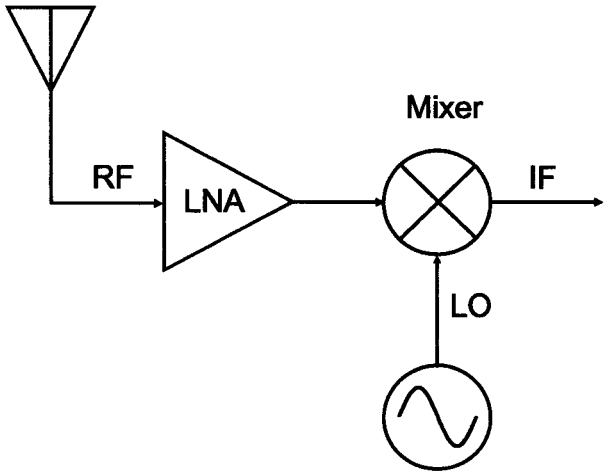


Figure 3-1 Simplified receiver architecture

A simple receiver architecture is shown in Figure 3-1. In an RF receiver, the input radio frequency signal from the antenna first passes through a low-noise amplifier that amplifies it and suppresses noise contributions from subsequent stages such as the mixer. This can be appreciated by considering the *Friis* equation,

$$F_{total} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1}A_{p2}} + \cdots$$

where F_{total} is the noise factor of cascade receiver chain, F_{i} is the noise factor of the ith stage, and A_{pi} is the available power gain of the ith stage.

The *Friis* equation manifests the fact that noise from the block following the LNA (typically a mixer) is suppressed by the gain of LNA when referred to the input. Considering that the mixer usually exhibits a high noise figure, it is desirable to place the LNA as close to the antenna as possible so that the weak input RF signal is first amplified with low noise before any further processing. Therefore, low noise and high gain are the most important figures of merit of an LNA.

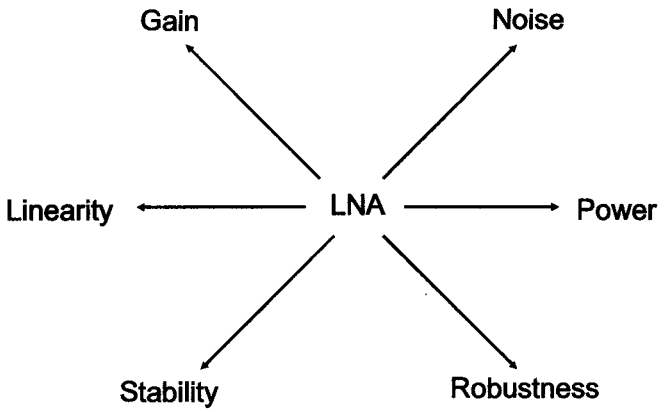


Figure 3-2 LNA design considerations

In addition to the gain and noise requirements, the LNA should be as linear as possible. As mentioned in Chapter 2, nonlinearity results in inter-modulation distortion term that degrades the selectivity of the receiver. This requires that the LNA introduce as little nonlinearity as possible. In an RF system, the figure-of-merit of linearity is often expressed as IIP3 or IIP2. As discussed later, there is a fundamental tradeoff between linearity and noise in the design of an LNA.

The design of an LNA also involves considerations of stability, reverse isolation, robustness, and power consumption. All of these tradeoffs complicate the design of an LNA as illustrated in Figure 3-2.

Before considering the design of an LNA, it is instructive to review the fundamental two-port network noise theory, which provides the necessary method for characterization and analysis of a general two-port network.

3.1 Two-Port Network Noise Theory

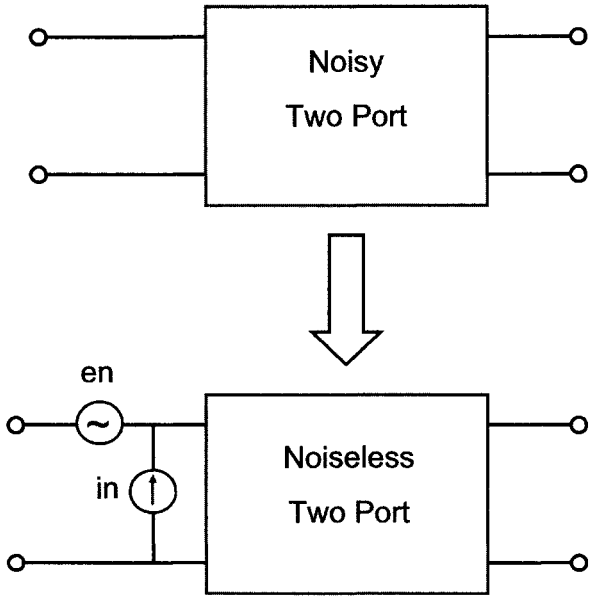


Figure 3-3 Two port network noise model

For a given two-port network, noise sources inside the network, either from passive or active components, add additional noise to the circuit. For the sake of computation convenience, the concept of ***equivalence*** can be applied to ease the calculation of noise. In this approach, an ***equivalent noise model***, which consists of a noiseless network and two input noise sources, namely, an input noise voltage source e_n and an input noise current source i_n (Fig. 3-3), models the original noisy network. Note that representing the noise inside the network by equivalent noise

voltage and current sources at the input is not the only possible way to characterize a noisy network. For example, noise inside the network can also be lumped into a noise current/voltage source at both the input and output ports. However, the representation shown in Figure 3-3 is most widely used.

The equivalent input noise voltage source e_n describes the noise behavior of the network when the input port is shorted to ground, while the equivalent input noise current source i_n describes the noise behavior of network when input port is open. Each alone is insufficient to completely characterize the noisy network. The network can only be fully characterized when both e_n and i_n are considered. In general, e_n and i_n are partly correlated[1]. The correlation between e_n and i_n is expressed using the correlation matrix C_A

$$C_A = \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} = \begin{bmatrix} \dfrac{\langle e_n^2 \rangle}{4kT\Delta f} & \dfrac{\langle e_n i_n^* \rangle}{4kT\Delta f} \\ \dfrac{\langle e_n^* i_n \rangle}{4kT\Delta f} & \dfrac{\langle i_n^2 \rangle}{4kT\Delta f} \end{bmatrix}.$$

The noise correlation matrix C_A embodies information about the noise performance of the network [12]. Alternatively, correlation is expressed using the correlation admittance Y_C where

$$Y_C = \frac{\langle e_n^* i_n \rangle}{\langle e_n^2 \rangle} = \frac{C_{A21}}{C_{A11}} = G_C + jB_C$$

Noise current i_n can be partitioned into two parts: i_u is uncorrelated with e_n and i_c is correlated with e_n:

[1] Actually there is no way to guarantee that e_n and i_n are uncorrelated.

$$i_n = i_u + Y_c \cdot e_n$$

As mentioned in Chapter 2, it is common to express noise as equivalent thermal noise from a resistance or conductance. Hence, we can define

$$R_n = C_{A11} = \frac{\overline{e_n^2}}{4kT\Delta f}$$

$$G_u = \frac{\overline{i_u^2}}{4kT\Delta f}$$

$$G_s = \frac{\overline{i_s^2}}{4kT\Delta f}$$

Therefore, the noise factor can be expressed in terms of the equivalent noise sources as:

$$F = F_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right] \tag{3-1}$$

$$F_{\min} = 1 + 2R_n\left[G_{opt} + G_c\right] = 1 + 2R_n\left[\sqrt{G_c^2 + \frac{G_u}{R_n}} + G_c\right] = 1 + 2\left(\mathrm{Re}\{C_{A12}\} + C_{A11}G_{opt}\right)$$

$$Y_s = G_s + jB_s$$

$$Y_{opt} = G_{opt} + jB_{opt} = \sqrt{\frac{C_{A22}}{C_{A11}} - \left(\frac{\mathrm{Im}\{C_{A12}\}}{C_{A11}}\right)^2} + j\frac{\mathrm{Im}\{C_{A12}\}}{C_{A11}} = \sqrt{G_c^2 + \frac{G_u}{R_n}} + j(-B_c)$$

$$C_A = \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} = \begin{bmatrix} R_n & \frac{F_{\min} - 1}{2} - R_n Y_{opt} \\ \frac{F_{\min} - 1}{2} - R_n Y_{opt}^* & R_n \left| Y_{opt} \right|^2 \end{bmatrix}$$

where $F_{\min}$ is the minimum noise figure, Y_s is input source admittance (usually $20mS$), G_s and B_s are real and imaginary parts of Y_s, respectively, R_n is the

equivalent noise resistance, Y_{opt} is the optimum input admittance which results in the minimum noise figure F_{min}, and G_{opt} and B_{opt} are the real and imaginary parts of Y_{opt}, respectively. (F_{min}, R_n, G_{opt}, B_{opt}) are also known as the four noise parameters that describe the noisy two-port network.

As can be seen from (3-1), F_{min} gives the minimum achievable noise factor when the input admittance Y_s is varied. Y_{opt} expresses the noise matching condition at which the minimum noise factor F_{min} can be obtained. R_n represents the sensitivity of the noise factor degradation when Y_s differs from Y_{opt}. To minimize the noise factor, R_n should be decreased to increase the suppression of the deviation of Y_s from Y_{opt}. In addition, a good match between Y_s and Y_{opt} is desirable so that F can approach F_{min} as closely as possible. The relationships between the different noise parameters above are listed in Figure 3-4.

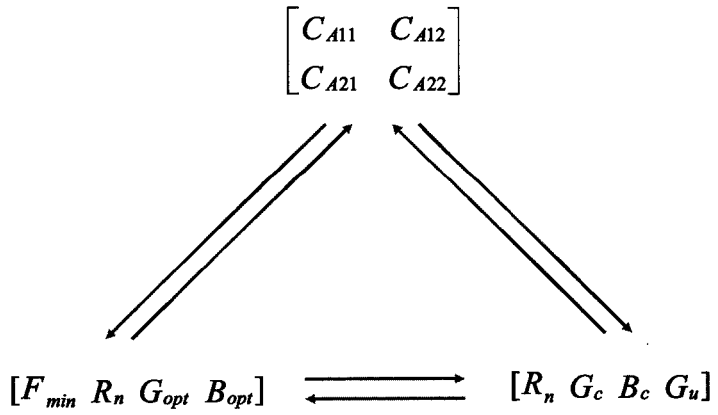


Figure 3-4 Conversion between different noise parameters

Knowing the noise correlation matrix C_A, the noise characteristic of the network is readily determined. Next, one example of a MOSFET is discussed to illustrate the general two-port network noise model. To focus on the intrinsic noise behavior of

the MOSFET, we surmise that its main noise sources are the thermal channel noise i_d and the induced gate noise i_g, which is often a good assumption.

The channel thermal noise i_d shows a white power spectral density as described by

$$\overline{i_d^2} = 4kT\Delta f\gamma g_{d0} \tag{3-2}$$

where g_{d0} is the zero-bias drain conductance, γ is a bias-dependent empirical factor, k is Boltzmann's constant and Δf is the bandwidth of interest.

A typical value of γ for a long-channel MOSFET operating in the saturation region is 2/3. However, for short channel devices, γ can be substantially higher than 2/3.

In addition to channel thermal noise i_d, a companion noise current i_g at the gate of the MOSFET, which is known as induced gate noise, has been observed in both theory and experiment:

$$\overline{i_g^2} = 4kT\Delta f\delta g_g \tag{3-3}$$

$$g_g = \frac{(\omega C_{gs})^2}{5g_{d0}} \tag{3-4}$$

where δ is another bias-dependent empirical parameter. Unlike the white noise spectrum of the channel thermal noise, induced gate noise has a *blue* spectrum proportional to frequency. Interestingly enough, induced gate noise i_g and channel thermal noise i_d are partly correlated due to that fact that they originate from the same mechanism

$$\overline{i_g i_d^*} = c\sqrt{\overline{i_g^2 i_d^2}}$$

It is found that the correlation coefficient c is almost a pure imaginary number; for a long-channel device $c=j0.395$.

The following calculation helps to highlight the relative magnitudes of gate and channel noise. From (3-2)-(3-4), we have

$$\kappa = \frac{\overline{i_g^2}}{\overline{i_d^2}} = \frac{\delta g_g}{\gamma g_{d0}} = \frac{\delta}{\gamma}\frac{\omega_0^2 C_{gs}^2}{5 g_{d0}^2} = \frac{\delta}{\gamma}\frac{\alpha^2}{5}\left(\frac{\omega_0}{\omega_T}\right)^2$$

where $\alpha = g_m / g_{d0}$. If γ=2, δ=4, α=0.85, ω_T/ω_0=5, then κ=1.16%. Hence, gate noise is much smaller in magnitude than channel thermal noise in a MOSFET. However, this does not necessarily mean that gate noise is negligible, as is discussed in Section 3.3.

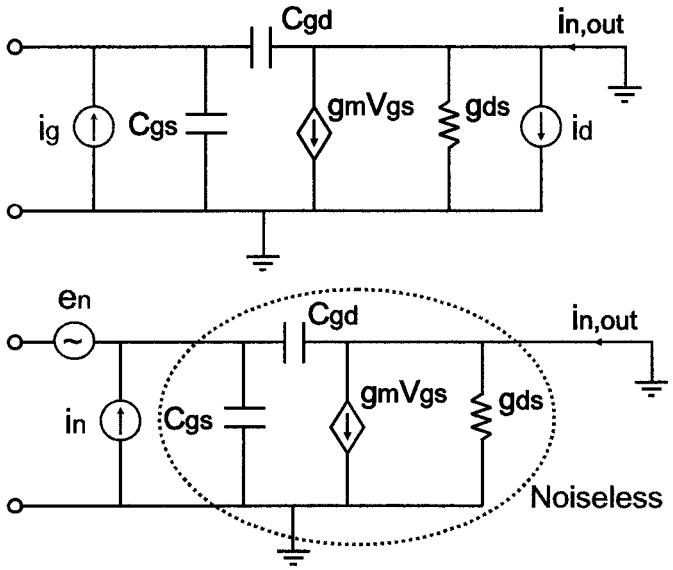


Figure 3-5 Equivalent noise model of a MOSFET

Knowing the main noise sources in a MOSFET, we are now ready to derive its two-port noise parameters. A small-signal noise model of a MOSFET is shown in

Figure 3-5. The calculation of the input noise voltage e_n and the input noise current i_n involves two steps:

1) Short the input to ground and calculate the equivalent input noise voltage source e_n;

2) Open the input and calculate the equivalent input noise current source i_n.

Based on the noise model in Figure 3-5, it can be shown that the equivalent input noise voltage e_n and noise current i_n of the MOSFET are

$$\begin{cases} e_n = i_d \dfrac{1}{g_m - j\omega C_{gd}} \\ i_n = i_g + i_d \dfrac{j\omega(C_{gs}+C_{gd})}{g_m - j\omega C_{gd}} \end{cases} \tag{3-5}$$

It can be seen from (3-5) that i_g contributes to i_n, but not to e_n. On the other hand, i_d contributes to both to e_n and i_n. Thus, e_n and i_n are partly correlated since they share the common components related to i_d. The correlation simply means $\overline{e_n i_n} \neq 0$.

Equation (3-5) enables us to calculate the noise correlation matrix C_A as follows

$$C_{A11} = R_n = \frac{\langle e_n^2 \rangle}{4kT\Delta f} = \frac{\gamma g_{d0}}{g_m^2 + \omega^2 C_{gd}^2}$$

$$C_{A21} = C_{A12}^* = \frac{\langle e_n^* i_n \rangle}{4kT\Delta f}$$

$$= c\sqrt{\frac{\delta\gamma}{5}} \frac{\omega C_{gs}}{g_m + j\omega C_{gd}} + j\omega(C_{gs}+C_{gd}) \frac{\gamma g_{d0}}{g_m^2 + \omega^2 C_{gd}^2}$$

$$C_{A22}=\frac{\langle i_n^2\rangle}{4kT\Delta f}$$
$$=\delta\frac{(\omega C_{gs})^2}{5g_{d0}}+\gamma g_{d0}\frac{\omega^2(C_{gs}+C_{gd})^2}{g_m^2+\omega^2C_{gd}^2}+2\mathrm{Re}\left\{-c\sqrt{\frac{\delta\gamma}{5}}\omega C_{gs}\frac{j\omega(C_{gs}+C_{gd})}{g_m+j\omega C_{gd}}\right\}$$

If C_{gd} is neglected (which is often a reasonable assumption) and we assume that c is purely imaginary (or $c=j|c|$), we have

$$C_{A11}=\frac{\gamma g_{d0}}{g_m^2}$$

$$C_{A21}=C_{A12}^*=j\omega C_{gs}\left(|c|\sqrt{\frac{\delta\gamma}{5}}\frac{1}{g_m}+\frac{\gamma g_{d0}}{g_m^2}\right)$$

$$C_{A22}=(\omega C_{gs})^2\left(\frac{\delta}{5g_{d0}}+\frac{\gamma g_{d0}}{g_m^2}+2|c|\frac{1}{g_m}\sqrt{\frac{\delta\gamma}{5}}\right)$$

The above serves as a good example to illustrate the two-port network noise model derivation. In deriving the noise factor, it is often more convenient to directly calculate it according to its definition.

3.2 Topology Candidates for CMOS LNA

Providing a resistive input impedance of 50Ω is one critical requirement of an LNA. The 50Ω termination is required primarily by the preceding band-select filter, whose characteristics such as insertion loss, pass band ripple, and stop band attenuation, are only guaranteed for a given range of terminating impedance (e.g., between 25Ω and 100Ω). Impedance deviations out of the range can result in substantial performance degradations.

The LNA should also be designed so that it adds minimum noise in the RF signal path while synthesizing the input impedance of 50Ω. This precludes obvious approaches such as shunting a 50Ω resistor at the input to create the termination impedance. In low-noise amplification, two topologies are widely adopted: the common-source amplifier with inductive degeneration [13][14] and the common-gate amplifier [15].

3.2.1 Common-source Low-noise Amplifier (CSLNA)

The resistive input impedance can be achieved by adding an inductance in series with the source of the MOSFET to degenerate the common-source amplifier as shown in Figure 3-6.

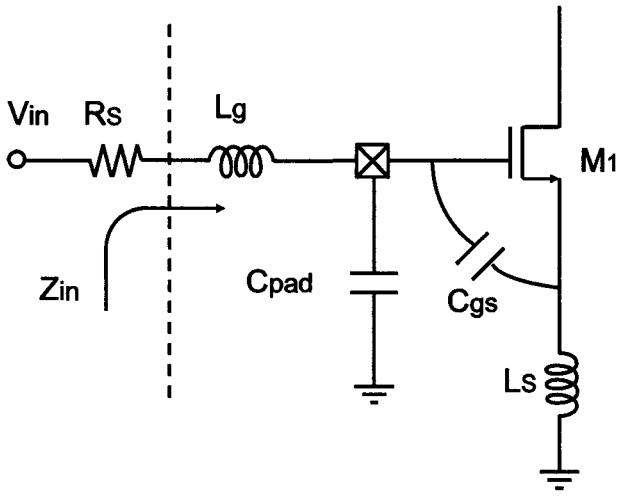


Figure 3-6 Common-source low-noise amplifier (CSLNA)

It is instructive to calculate the input impedance looking into gate of MOSFET when its source is degenerated by inductor L_S. The input impedance of CSLNA is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right) L_s \quad .$$

Note that there is a resistive component in the input impedance. To get a resistive input impedance of 50Ω at the operating frequency, one can choose the value of L_g and L_s such that C_{gs} is resonated out at the operating frequency with $(g_m/C_{gs})L_s$ set equal to 50Ω.

$$j\omega_0(L_g+L_s)+\frac{1}{j\omega_0 C_{gs}}=0$$

$$\left(\frac{g_m}{C_{gs}}\right)L_s \approx \omega_T L_s = 50$$

One of the most attractive advantages of this topology is that the resistive component of the input impedance is noiseless because it is synthesized using an inductor, unlike other techniques where a noisy resistor is added in the signal path to provide the 50Ω termination resistance [16]. This explains the low-noise performance and popularity of the inductively degenerated common-source LNA.

It is interesting to calculate the effective small-signal transconductance of the input transistor. Notice that the input matching circuit is a pure series RLC resonant circuit. At resonance, the voltage across C_{GS} is enhanced by Q times, where Q is the quality factor of input matching RLC circuit. In other words, the Q enhancement mechanism provides a free gain of Q for both the input signal and the noise from the source resistance R_S. The added gain from the input matching circuit helps to suppress channel thermal noise, which accounts for the superior noise performance of the common-source LNA with inductive degeneration. Furthermore, the effective transconductance is also enhanced by a factor of Q as

$$G_m = g_m Q = \frac{g_m}{\omega_0 C_{gs}(R_s+\omega_T L_s)} = \frac{\omega_T}{\omega_0 R_s\left(1+\frac{\omega_T L_s}{R_s}\right)}$$

If the input is matched to R_s, we have

$$G_m = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_0}\right) \tag{3-6}$$

Usually in an RF system R_s is equal to 50Ω. It is worth noting that the effective transconductance G_m is only related to the ratio of ω_T to ω_0 and is independent on MOSFET small-signal transconductance g_m.

However, CSLNA suffers from the parasitic gate-to-drain capacitance C_{gd} and pad capacitance C_p as shown in Figure 3-6. The gate-to-drain capacitance C_{gd} provides a feedthrough path from input to output and thus decreases the reverse isolation. In addition, its interaction with the inductive load at the output introduces a negative resistance at the input, which causes stability concerns. Furthermore, the Miller effect of C_{gd} and C_p associated with the bond pad provides a shunt current branch at the input, which further complicates the input matching. One can add a cascode stage to mitigate the Miller effect of C_{gd} and improve the reverse isolation. However, this results in additional noise from the cascode transistor, which degrades the noise figure if the cascode transistor is not optimally designed.

3.2.2 Common-gate Low-noise Amplifier (CGLNA)

Figure 3-7 shows a common-gate LNA where the gate terminal is shorted to an AC ground and the input signal is injected at the source terminal. The resistance looking into the source terminal is $1/g_m$, which provides the possibility of 50Ω input matching. Inductor L_s tunes out the capacitance at source terminal (including pad capacitance C_p, gate-to-source capacitance C_{gs} and source-to-bulk capacitance C_{sb}) at the resonant frequency to provide the required resistive impedance.

Unlike CSLNA, there is no Miller effect associated with C_{gd} in CGLNA, which results in better reverse isolation. In addition, parasitic source-to-bulk capacitance C_{sb} of the MOSFET, bond pad capacitance C_p and gate-to-source capacitance C_{gs} are naturally absorbed in the input *RLC* tank. In other words, CGLNA is less prone to the effects of the input parasitic capacitance than CSLNA.

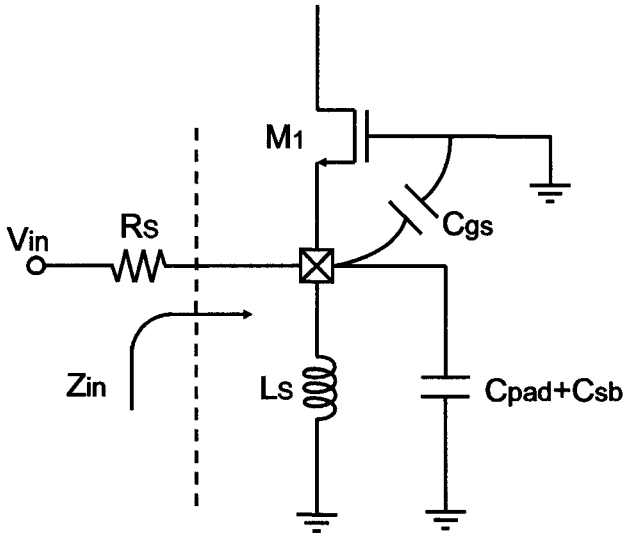


Figure 3-7 Common-gate low-noise amplifier (CGLNA)

The effective small-signal transconductance of the input transistor of CGLNA is

$$G_m = \frac{1}{2R_s} \tag{3-7}$$

However, the common-gate LNA suffers from the presence of a noisy channel conductance in the signal path, which is detrimental to noise performance. It can be shown that under a perfect input matching condition, the common-gate LNA has the following noise factor

$$F = 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega}{\omega_T}\right)^2$$

In the above expression, the second term is from the contribution of induced gate noise, which is negligible compared to the contribution of channel noise. Neglecting gate noise for the CGLNA is a reasonable approximation. Therefore, the noise factor of CGLNA can be approximated by

$$F = 1 + \frac{\gamma}{\alpha}$$

However, this approximation should be cautiously applied since in certain situations such as that in the CSLNA, gate noise is amplified and becomes comparable to channel noise.

For a long-channel device, the noise figure of CGLNA is about 2.2dB. However, with the scaling of technology, γ can be higher than 2/3, and the corresponding noise figure is significantly higher. For example, if γ=2, F=4.8dB, which is higher than that for a long-channel device. This high noise figure would seem to prohibit the use of the CGLNA topology for very low-noise applications. In addition, from (3-6) and (3-7), we can see that CGLNA is inferior to CSLNA from a gain perspective.

Compared to CGLNA, CSLNA has been more popular due to its low-noise capability. However, one should be cautious with this conclusion because the presence of induced gate noise complicates the optimization of the noise figure. If not considered, one may end up with substantial deviation from the optimum noise figure [17].

3.3 Noise Optimization of CSLNA

Next, noise optimization of the CSLNA topology is considered.

3.3.1 Noise Optimization

Of course one can start from the two-port noise model to derive the noise factor of the CSLNA, just as is done for a general two-port network. Here we will derive the noise figure according to its definition, that is, the ratio of total output noise power to the output noise power due to input source impedance only. To obtain the expression for noise figure, it is instructive to calculate the transfer functions of the different noise sources in the MOSFET [18]. The small-signal circuit used in the computation is shown in Figure 3-8.

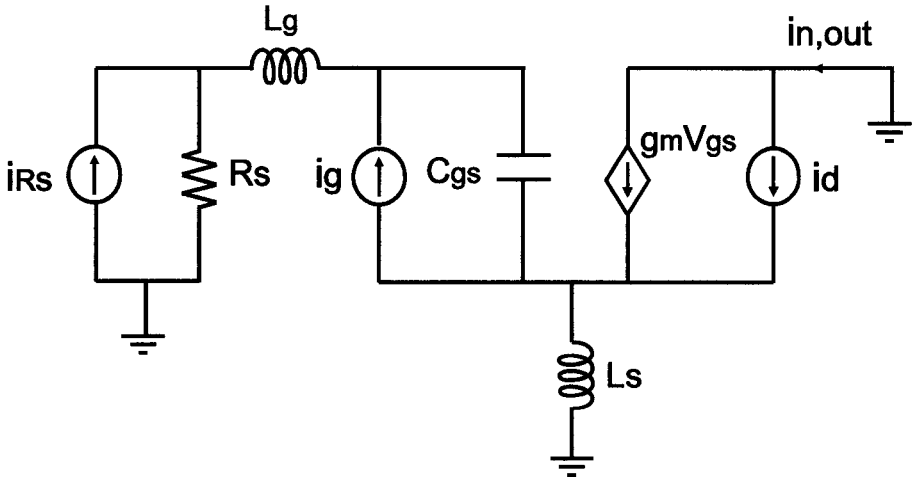


Figure 3-8 Small-signal model for noise calculations of CSLNA

$$i_{o,Rs} = \frac{R_s}{R_s+\omega_T L_s}\frac{g_m}{sC_{gs}} i_{Rs} = \frac{R_s}{R_s+\omega_T L_s}\frac{\omega_T}{j\omega} i_{Rs}$$

$$i_{o,d} = \frac{R_s}{R_s+\omega_T L_s} i_d$$

$$i_{o,g} = \frac{R_s}{R_s+\omega_T L_s}\frac{g_m}{sC_{gs}}\left(1-\frac{1}{sC_{gs}R_s}\right) i_g = \frac{R_s}{R_s+\omega_T L_s}\frac{g_m}{j\omega C_{gs}}\left(1-\frac{1}{j\omega C_{gs}R_s}\right) i_g \qquad (3\text{-}8)$$

$$= \frac{R_s}{R_s+\omega_T L_s}\frac{\omega_T}{j\omega}(1+jQ) i_g$$

where

$$\overline{i_{Rs}^2} = \frac{4kT\Delta f}{R_s}$$

$$\overline{i_d^2} = 4kT\gamma\, g_{d0}\Delta f$$

$$\overline{i_g^2} = 4kT\delta\, g_g \Delta f$$

$$\omega_T = \frac{g_m}{C_{gs}}$$

$$Q = \frac{1}{\omega C_{gs} R_s}$$

As suggested by (3-8), there exists a gain boosting mechanism in the input matching circuit. That is, the series input RLC resonant circuit boosts the noise current i_{RS} from source impedance R_s by a factor of G_mR_s=0.5ω_T/ω (in magnitude). This welcome boosting mechanism helps to lower the noise figure, which makes this topology very popular in modern LNA design.

Unfortunately, the accompanying effect associated with the gain boosting mechanism is that the gate noise is also amplified by the factor $[0.5\omega_T/\omega]^2(1+Q^2)$. On the other hand, channel noise i_d is attenuated by a factor of 0.25 at the resonant condition. Although gate noise is much smaller than channel noise in magnitude, the higher gain for gate noise makes it an important noise source in the CSLNA topology, which highlights the fact that neglecting gate noise in CSLNA is problematic.

The total noise current at the MOSFET drain terminal is

$$\overline{i_{n,out}^2} = \overline{i_{o,Rs}^2} + \overline{i_{o,d}^2} + \overline{i_{o,g}^2} + \overline{i_{o,g} i_{o,d}^*} + \overline{i_{o,g}^* i_{o,d}}$$

According to the definition, noise factor is therefore

$$F=\frac{\overline{i_{n,out}^2}}{\overline{i_{Rs}^2}}=1+\frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega}{\omega_T}\right)\left[1+\frac{\delta\alpha^2}{5\gamma}(1+Q^2)+2|c|\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right] \tag{3-9}$$

If we set δ=0, or equivalently, neglect the gate noise term, we have

$$F=\frac{\overline{i_{n,out}^2}}{\overline{i_{Rs}^2}}=1+\frac{\gamma}{\alpha}\frac{1}{Q}\left(\frac{\omega}{\omega_T}\right)=1+\frac{\gamma}{\alpha}\frac{1}{g_m R_s Q^2}$$

It is commonly believed that in order to lower the noise figure, Q should be increased as suggested by (3-9). However, this is only true if the gate noise is neglected. Insight can be achieved by carefully observing the noise figure expression. As can be seen from (3-9), the second term includes three parts: channel noise, gate noise and the correlation part. As mentioned before, the gate noise of a MOSFET is enhanced by the quality factor Q of the input resonant circuit. Decreasing Q helps to lower the contribution from gate noise. On the other hand, increasing Q tends to reduce the contribution from channel noise. Therefore there exists an optimum Q, which minimizes the noise figure. For fixed ω_T, it is found to be

$$Q_{opt}=\sqrt{1+2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}+\frac{5\gamma}{\delta\alpha^2}} \tag{3-10}$$

The typical value that (3-10) predicts is about 2~3. One may also optimize the NF while keeping the power consumption as small as possible. In this case, one would determine a Q value of about 4~5. Although higher Q is beneficial for suppressing channel noise and lowering the required current consumption, there are several reasons that make a lower Q design approach preferable.

A high-Q input-matching network makes the design sensitive to variations of the inductance and capacitance components, which may result in a large deviation of the input impedance from the nominal value of 50Ω. This problem is even worse considering the difficulty of accurate characterization of on-chip inductor. Therefore, a low-Q input-matching network is preferred to avoid tuning and decrease the fabrication cost [19].

Knowing ω_T and Q, the optimum size and bias of the device can be determined. Figure 3-9 shows the contours of noise figure by varying V_{gs} and W. It is not surprising that the optimum transistor width stays almost constant with respect to different V_{gs} values since (3-10) predicts that the optimum Q_{opt} depends only on such constants as c, δ and γ if α is close to 1.

In Figure 3-9, to eliminate any possible error in investigating the relation between noise figure, V_{gs} and W of the MOSFET, an *HSPICE* netlist is generated to simulate the small-signal parameters. In other words, simulation instead of analytical assumption is adopted.

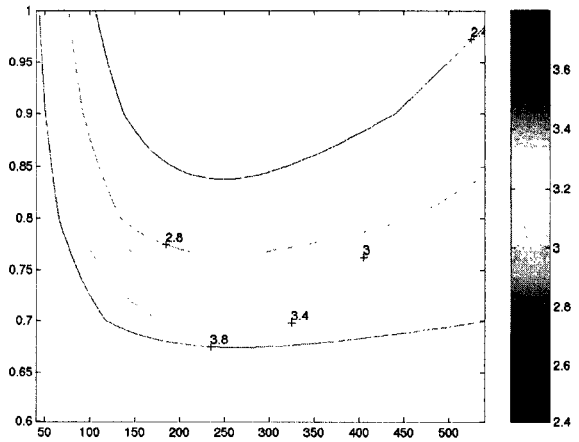


Figure 3-9 Noise figure vs. V_{gs}-V_t and W

3.3.2 Second-Order Effects

3.3.2.1 Gate Resistance

The material used for the gate of the MOSFET has finite conductivity. Gate resistance directly adds additional noise to LNA. A simple expression for gate resistance is shown as follows

$$R_{G,poly} = \frac{R_{Gsh}}{N_f L_f} \frac{W_f}{\alpha}$$

where $R_{G,sh}$ is the gate sheet resistance, W_f is the channel width per finger, L_f is the channel length, N_f is the number of fingers, α is a fitting parameter, typically 3 or 12 depending on whether the gate fingers are connected on one side or on both sides [20][21].

As implied by the above equation, multi-finger layout can be used to efficiently lower gate resistance to make the associated noise contribution negligible.

3.3.2.2 Pad Capacitance

Since any noise associated with L_g directly adds noise to the LNA, it is beneficial to use off-chip or bond-wire inductors for L_g. However, the pad capacitance introduces an extra shunt path to ground. This has adverse effects on both noise and gain if a resistive component is present in the path, which is often the case in *Silicon* technology.

To eliminate the resistive component of the bonding pad, a shielding metal under the top metal can be used as shown in Figure 3-10, along with the equivalent circuit model [22].

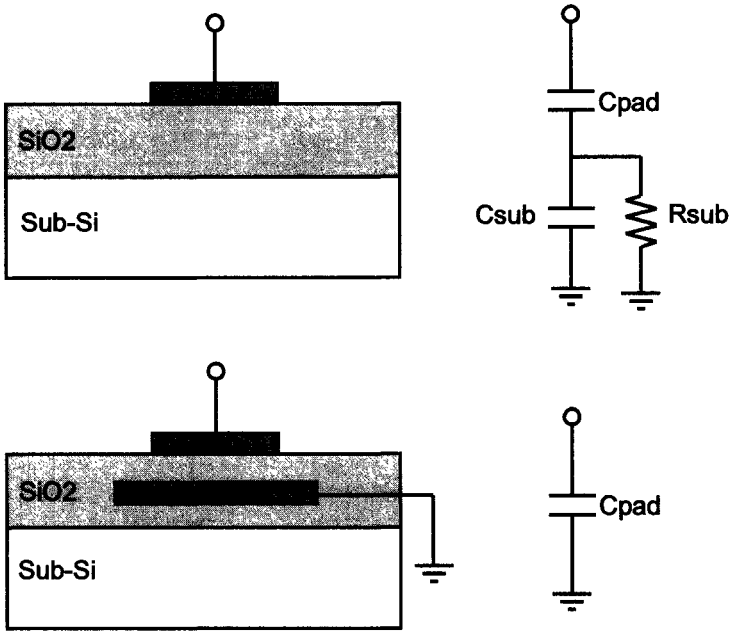


Figure 3-10 Shielded pad for input

3.3.2.3 Cascode Transistor

In implementing CSLNA, a cascode structure is usually adopted (Figure 3-11). First, the cascode stage effectively reduces the Miller effect of C_{gd1}. In addition, it provides good isolation between the input and output ports of the LNA. Good isolation makes the input and output matching independent of each other and also increases the stability of amplifier.

Optimization of a low-noise amplifier usually involves only the input transistor M_1. Noise contributions from cascode transistor M_2 are assumed to be negligible. However, simulation shows that neglecting the noise of M_2 is problematic; if not optimized, the noise contribution from M_2 can be as much as 60% of M_1.

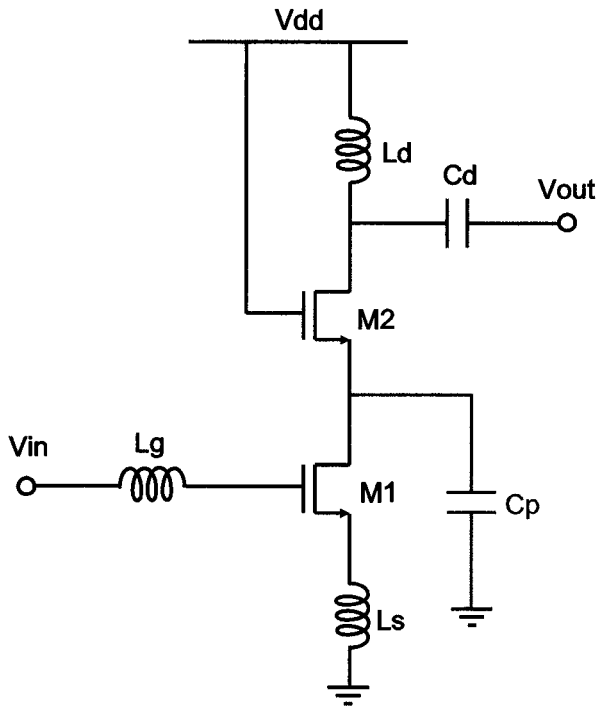


Figure 3-11 Common-source low-noise amplifier with cascode stage

The noise contribution of M_2 can be understood when the parasitic capacitance C_p at the source node of M_2 is considered. The parasitic capacitance C_p associated with the source of the cascode transistor provides another current path to ground which attenuates the signal current and increases the noise figure.

To prevent the cascode transistor from contributing noise at the output, one should consider minimizing C_p. This can be achieved by utilizing the so-called *dual gate* layout technique (Figure 3-12) [23]. In this technique, the parasitic capacitance at M_1's drain and M_2's source is substantially reduced as shown in Figure 3-12. Since the souce of M_1 and drain of M_2 are shared and there are no contacts within the cascode node, the distance from the gate of M_1 to M_2 can be minimized. This substantially reduces the area of cascode node.

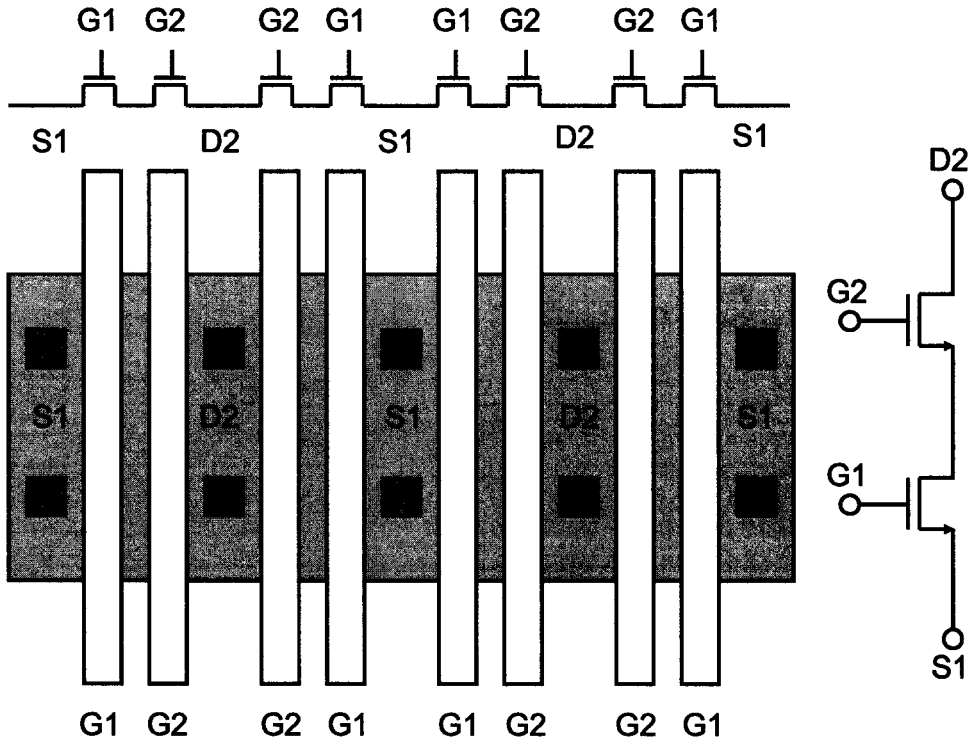
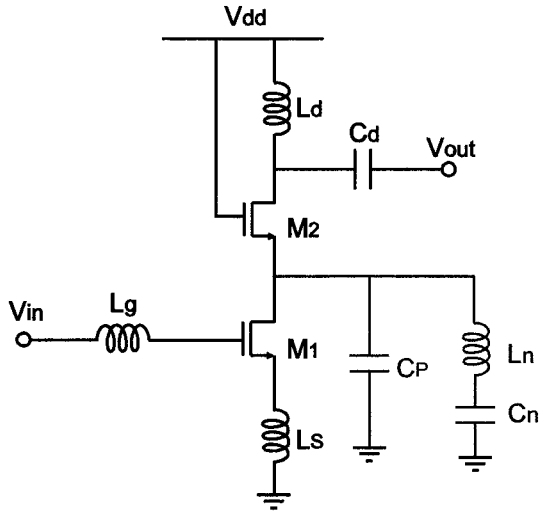
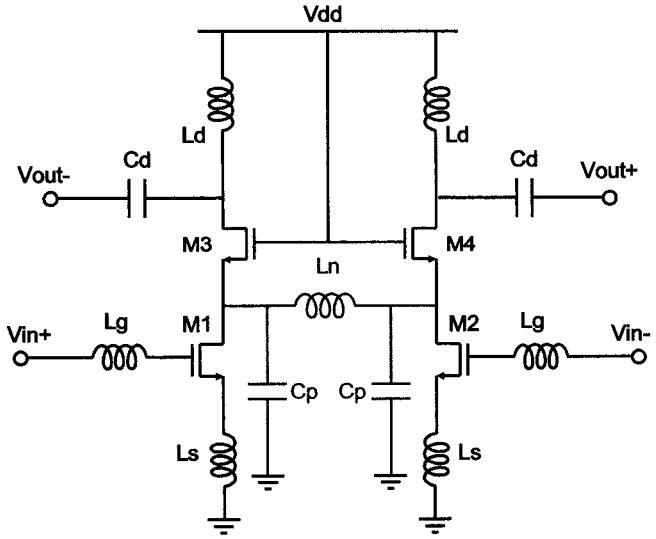


Figure 3-12 Dual gate layout technique

Another consideration in reducing the effect of C_p is to add another inductor at the source of M_2 to resonate with C_p, as depicted in Figure 3-13. In Figure 3-13-a, L_n is the tuning inductor and C_n is the blocking capacitor to isolate the DC bias voltage. Figure 3-13-b shows the differential version. Note that the choice of a differential topology eliminates the requirement of a huge blocking capacitor C_n. However, on-chip inductors usually suffer from low quality factors, and the parasitic resistance of L_n adds additional noise to the output. An accurate model of the inductor is necessary for careful simulation in order to determine whether it is beneficial or not to add L_n.



(a) Single ended version



(b) Differential version

Figure 3-13 Tuning out C_p by inductors

3.4 Comparisons of CSLNA and CGLNA

As discussed in Section 3.3, CSLNA is now more popular due to its higher gain and lower noise figure than CGLNA. To get deeper insight, performance characteristics of the basic CSLNA and CGLNA topologies are next analyzed and compared.

3.4.1 Gain

$$G_{m,CSLNA} = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_0}\right) \leftrightarrow G_{m,CGLNA} = \frac{1}{2R_s}$$

The value of ω_T/ω_0 typically lies in the range of 5~10 depending on the operating frequency and process details. Therefore, CSLNA provides higher gain than its conventional common-gate counterpart.

3.4.2 Noise

By substituting (3-10) into (3-9), we get the minimum noise factor as

$$\begin{aligned} F_{\min,CSLNA} &= 1+\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)\frac{2\delta\alpha^2}{5\gamma}Q_{opt} \\ &= 1+\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right)\left(\frac{2\delta\alpha^2}{5\gamma}\sqrt{1+2|c|\sqrt{\frac{5\gamma}{\delta\alpha^2}}+\frac{5\gamma}{\delta\alpha^2}}\right) \end{aligned}$$

If γ=2, δ=4, α=0.85, then we have

$$F_{\min,CSLNA} = 1+1.41\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right) \leftrightarrow F_{CGLNA} = 1+\frac{\gamma}{\alpha}$$

The above result is of great importance since it reveals that to the first order, the noise factor of the common-gate amplifier is constant with respect to ω/ω_T, whereas the noise factor of the common-source amplifier is a linear function of ω/ω_T (Figure 3-14).

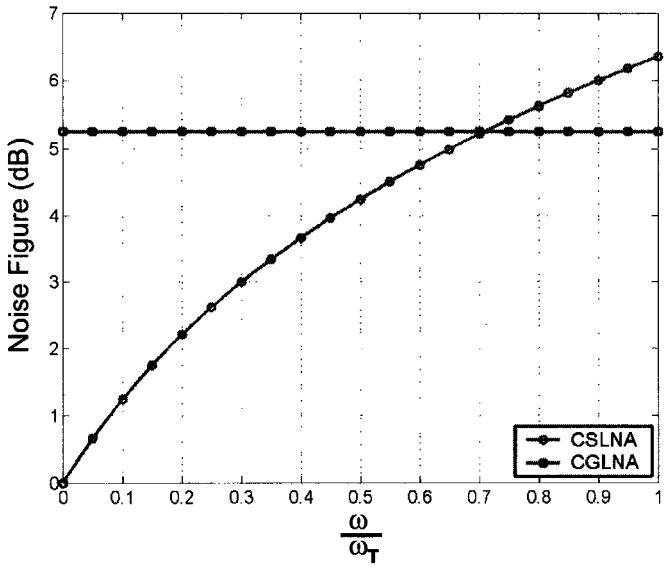


Figure 3-14 Noise figure of CSLNA and CGLNA vs. frequency

Usually for LNA design, ω_0/ω_T is relatively small. As a result, as far as low-noise is concerned, CSLNA is a better choice than the conventional CGLNA.

3.4.3 Input Matching

A fundamental difference between the input matching networks is that CSLNA is a series resonant circuit while CGLNA is a parallel one; the associated quality factors are

$$Q_{CS-LNA} = \frac{1}{2\omega_0 C_{gs} R_s} > 1 \leftrightarrow Q_{CG-LNA} = \frac{\omega_0 C_{gs} R_s}{2} < 1$$

It is known that the sensitivity of Z_{in} to parasitic components is proportional to the quality factor of the input matching network. Hence, CGLNA with its lower Q parallel resonant network is more robust against typical production process, voltage, and temperature variations. Moreover, parasitic capacitance at the CGLNA input is naturally absorbed into the LC tank.

3.4.4 Reverse Isolation and Stability

Reverse isolation ($-S_{12}$) represents amplification in the reverse direction. For an amplifier, it is hoped that this reverse transmission is minimized. In a direct conversion receiver the large signal LO can be coupled to the output of LNA. With finite reverse isolation it can be transmitted back to input of LNA. Being reflected back from antenna, this leakage from the LO is mixed with the LO signal itself, generating a DC offset voltage. Known as LO self-mixing, this is a serious problem in DCR.

Reverse isolation is also related to stability, as can be seen from Stern stability factor

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{21}||S_{12}|} \quad and \quad |\Delta| = |S_{11}S_{22}-S_{12}S_{21}|$$

The amplifier is stable if $K>1$ and $|\Delta|<1$. So, lower S_{12} or better reverse isolation means better stability [24].

In a conventional CSLNA, C_{gd} provides a feed-forward path between input and output that degrades reverse isolation and stability. In contrast, since the Miller

effect on C_{gd} does not exist in CGLNA, it exhibits better reverse isolation. Also, cascoding is not necessary in a conventional CGLNA so there is no added noise from cascode transistors.

3.4.5 Power Consumption

CSLNA has one major drawback that it is sensitive to the variations of inductance and capacitance in the input matching circuit. To make it less prone to this problem, one can design a low-Q input matching-network by using constant-Gm optimization approach. However, this results in higher power consumption. Simulations show that CSLNA usually consumes more DC current than CGLNA does. From the point view of power consumption, CGLNA is more efficient than CSLNA.

Table 3-1 Comparison between CSLNA and CGLNA

	CSLNA	CGLNA
Noise Factor	+	–
Effective Gm	+	–
Power Consumption	–	+
Input Matching	–	+
Parasitic Sensitivity	–	+
Reverse Isolation	–	+

As a summary, Table 3-1 lists the comparisons between CGLNA and CSLNA. Based on the above discussion, CGLNA has advantages such as lower power consumption, easier input matching, less sensitivity to parasitics and better reverse isolation when compared to CSLNA.

3.5 Proposed Gm-boosted CGLNA

Since noise figure is the most important characteristic of an LNA, it is interesting to revisit the noise calculation of the common-gate amplifier to discern the possibility of improving its noise performance.

Similar to the case of CSLNA, let's first look at the transfer functions of different noise currents in the circuit (Figure 3-15).

$$i_{o,Rs} = \frac{g_m}{g_m + 1/R_s} i_{Rs} = \frac{g_m R_s}{1 + g_m R_s} i_{Rs}$$

$$i_{o,d} = \left(1 - \frac{g_m R_s}{1 + g_m R_s}\right) i_d = \frac{1}{1 + g_m R_s} i_d$$

$$F = \frac{\overline{i_{Rs}^2} + \overline{i_d^2}}{\overline{i_{Rs}^2}} = 1 + \frac{4kT\gamma g_{d0}\Delta f}{4kT/R_S \Delta f}\left(\frac{1}{g_m R_S}\right)^2 = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_S} \qquad (3\text{-}11)$$

Input matching requires that $1/g_m = R_s$, which results in

$$F = 1 + \frac{\gamma}{\alpha} \qquad (3\text{-}12)$$

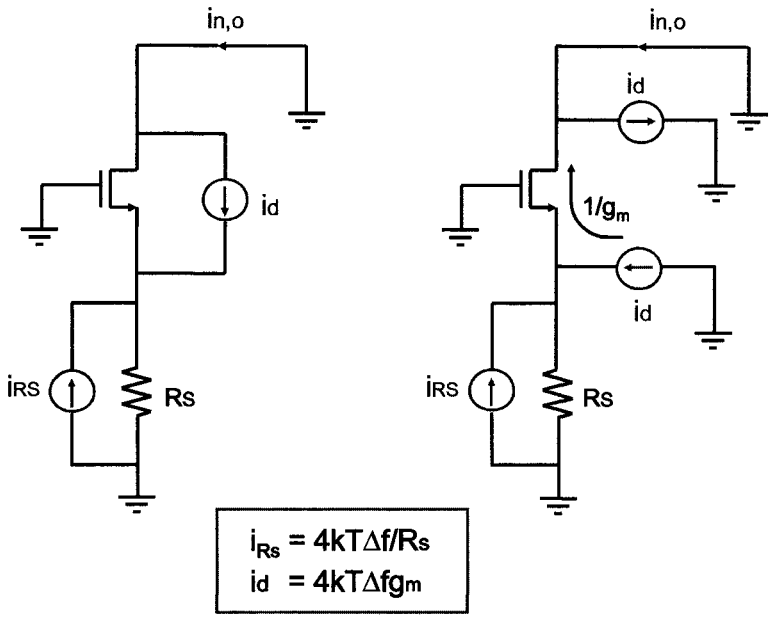


Figure 3-15 Calculation of noise figure for common-gate amplifier

As (3-11) implies, increasing g_m reduces the noise factor. In RF systems, however, input matching requires that $g_m = 1/R_S$, which results in $F = 1+\gamma/\alpha$. From another point of view, it is the input-matching requirement that prevents a designer from increasing g_m to lower the noise factor, and this in turn sets a lower bound on the noise factor. Note that in CGLNA, impedance matching may be traded against noise figure. More specifically, if some input mismatch can be tolerated, g_m can be increased to decrease the noise figure while the input reflection is maintained below some reasonable value. For example, if $\gamma = 2$ and $1/g_m = 30\Omega$, $S_{11} = -12$dB, which is often acceptable. In this case, NF = 3.4dB, which is about 1.4dB lower than the value of 4.8dB when the input is matched to 50Ω.

3.5.1 General Scheme of Gm-boosted CGLNA

The above discussion illuminates the tight link between noise figure and input matching in CGLNA. To maintain a good input matching, one cannot decrease noise figure due to the limit on device g_m. This is the fundamental tradeoff between noise figure and input matching in a conventional common-gate amplifier.

It is even more interesting to investigate Figure 3-15 to get some insight. Notice that there are two "g_m"s in calculating the noise figure. One "g_m" is the effective transconductance looking into source terminal. It is more convenient to denote it as G_m. The other "g_m" is the intrinsic transconductance of device itself, which is related to channel noise i_d.

In general, G_m is not necessarily equal to g_m. However, in the conventional CGLNA shown in Figure 3-7, since gate terminal is shorted to ground, $G_m = g_m$. The question is: what happens if we modify the circuit such that $G_m \neq g_m$?

To make $G_m \neq g_m$, coupling between gate and source terminals can be introduced. Figure 3-16 depicts the topology of the g_m-boosted CGLNA. In this structure, rather than connecting the gate terminal to a dc bias voltage, an inverting amplification is introduced between the source and gate nodes of the MOSFET. Consequently, the effective transconductance looking into the source terminal is boosted from $G_m = g_m$ to $G_m = (1+A)g_m$, where A is the gain from source to gate. More important, the resulting noise factor is calculated to be

$$F = 1 + \frac{4kT\gamma g_{d0}\Delta f}{4kT/R_S\Delta f}\left(\frac{1}{(1+A)g_m R_S}\right)^2 = 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A)^2 g_m R_S}$$

Input matching requires that $\frac{1}{(1+A)g_m} = R_S$, which in turn results in

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{1+A} \tag{3-13}$$

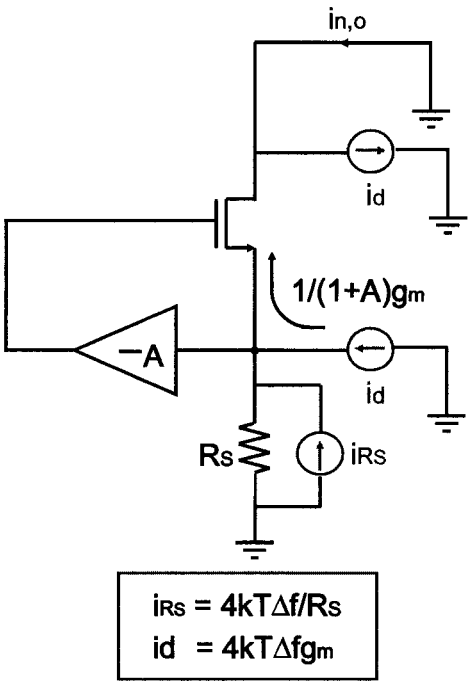


Figure 3-16 Introduction of coupling between source and gate

It can be clearly seen from (3-12) and (3-13) that the noise factor of the structure shown in Figure 3-16 is reduced by the factor (1+*A*). For example, if A=1, γ =2, δ=4, α=0.85, then

$$NF_{CG-LNA} = 5.25dB \leftrightarrow NF_{CG-LNA,GM-BOOSTED} = 3.38dB$$

It can be seen that 1.9dB of improvement in the noise figure is achieved by the g_m-boosted CGLNA relative to its conventional counterpart.

Figure 3-17 shows the noise performance of CSLNA, CGLNA and g_m-boosted CGLNA. The g_m-boosted CGLNA (with A = 1) achieves lower noise figure than

CSLNA for $\omega_0/\omega_T > 0.35$. In addition, if $1/g_m = 30\Omega$, $S_{11} = -12$dB, usually an acceptable value, g_m-boosted CGLNA outperforms CSLNA for $\omega_0/\omega_T > 0.2$. It also consumes less power than the conventional CGLNA. That is, since $(1+A)g_{m,new} = 1/R_S$, $g_{m,new}$ is reduced to $1/(1+A)g_m$ and the power consumption is reduced by the same factor. So the above discussion reveals that the g_m-boosted CGLNA is attractive for high frequency applications.

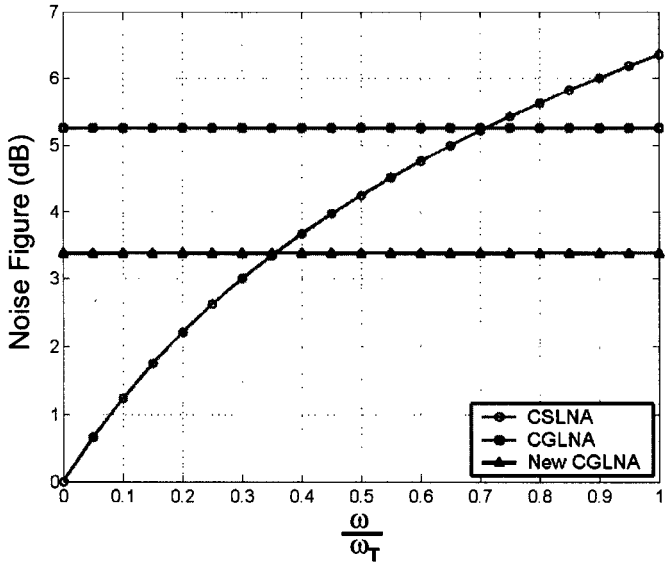


Figure 3-17 Noise figure of CSLNA, CGLNA and gm-boosted CGLNA

Figure 3-18 shows the general scheme of the proposed g_m-boosted CGLNA. In this scheme, an inverse gain between source and gate is required. The implementation of the gain between source and gate is mainly determined by noise considerations. Obviously there are two choices: either active or passive. Since active devices inevitably introduce more noise, it seems more attractive to resort to a passive implementation.

3.5.2 Possible Implementations

Next, the capacitor cross-coupled CGLNA is reviewed as one possible implementation of a g_m-boosted CGLNA [25]. As shown in Figure 3-19-a, the inverting gain is naturally available (with A = 1) in differential configuration, wherein L_s resonates with the input node capacitance at the operating frequency. L_d and C_d form an L-match circuit at the output.

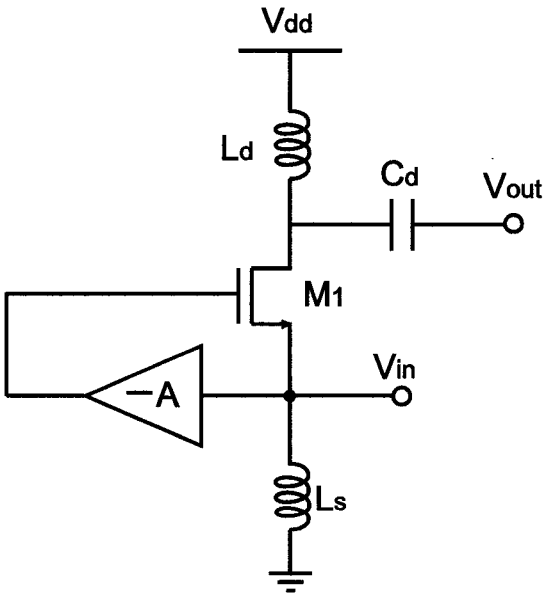
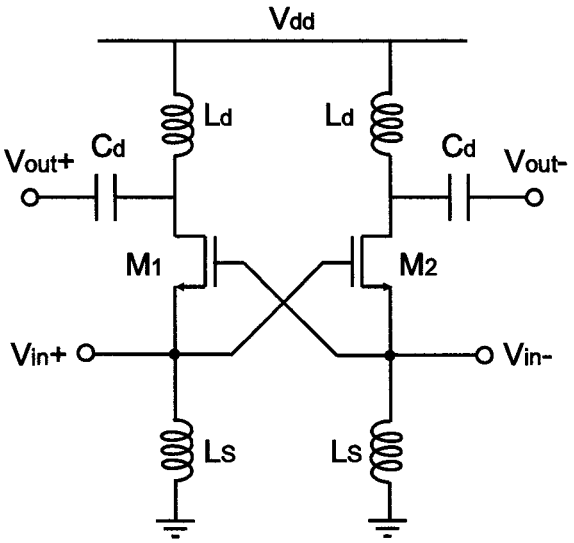
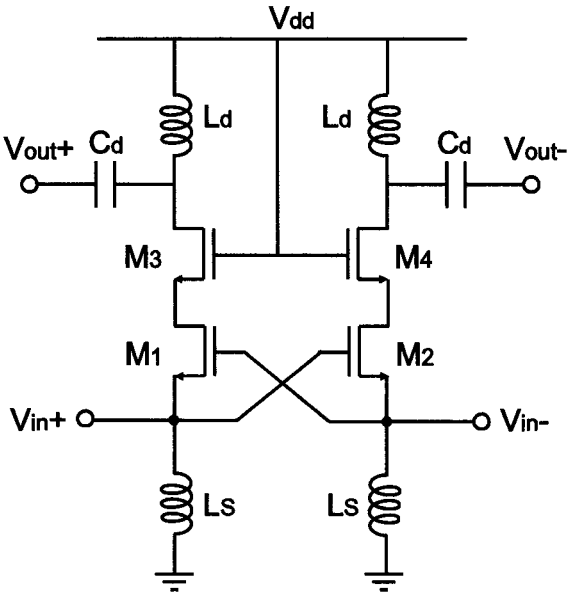


Figure 3-18 General scheme of g_m-boosted CGLNA

For the sake of simplicity, bias is not shown in Figure 3-19-a. Since now the gate terminal is not shorted to *AC* ground, the circuit shown in Figure 3-19-a has the drawback that the reverse isolation deteriorates due to C_{gd}. Unlike the case in the conventional common-gate amplifier, C_{gd} in Figure 3-19-a suffers from the Miller effect. To overcome this problem, a cascode transistor can be added as shown in Figure 3-19-b (*DC* bias is not explicitly shown). The cascode transistors also help to increase reverse isolation and stability.



(a) Without cascode



(b) With cascode

Figure 3-19 Capacitive Cross-Coupled CGLNA

The drawback of adding a cascode is the additional noise contributions. To minimize the noise from the cascode, a dual gate layout technique can be applied. Another solution is to add an inductor at the cascode node. As stated before, careful simulation should be performed to determine whether adding L_n is beneficial.

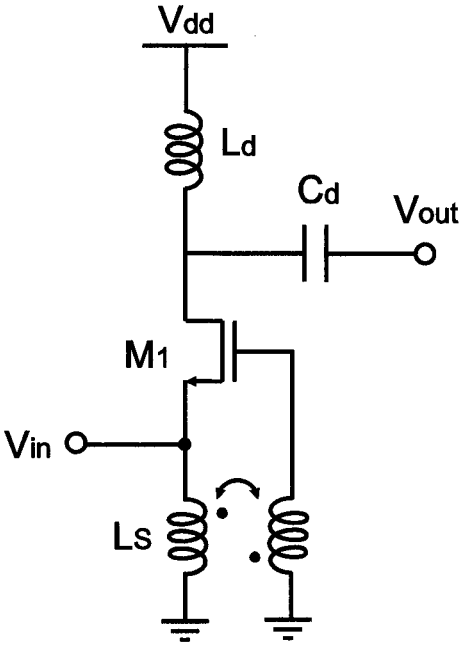


Figure 3-20 Gm-boosted CGLNA with transformer

The inverse gain between source and gate can also be implemented through the use of on-chip transformer (Figure 3-20). The coupling between two inductors ensures the opposite phase between the gate and source nodes, and therefore the desired inverse gain. Before analyzing it, let's first look at the transformer and its circuit model.

A transformer is basically a pair of inductors coupled to each other (Figure 3-21-a) [26]. The two coupled inductors are usually called the primary inductor L_P and secondary inductor L_S. A monolithic transformer is often implemented as two

square spiral inductors laid out in a interleaving fashion to achieve the desired magnetic coupling [27]. The magnetic coupling coefficient k, which indicates the strength of coupling, is related to the mutual inductance M between the primary and secondary inductors

$$k = \frac{M}{\sqrt{L_P L_S}} \tag{3-14}$$

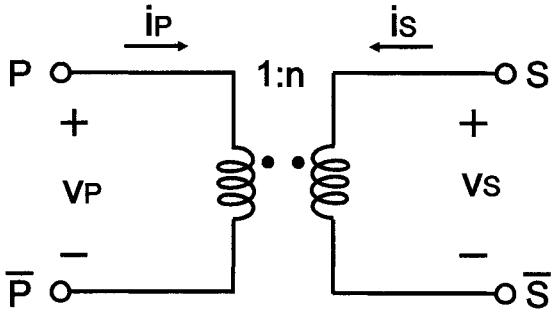
In an ideal transformer, the voltage and current at the primary and secondary winding (as labeled in Figure 3-21-a) are related to the turns ratio as

$$n = \frac{v_S}{v_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}} \tag{3-15}$$

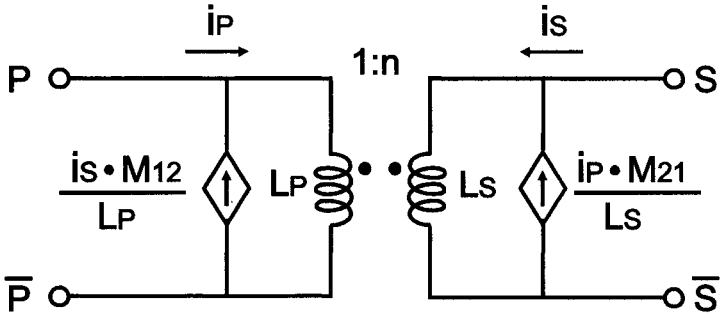
The magnetic flux in the primary inductor introduces a voltage drop across S and $\overline{S}$ at the secondary winding, and vice versa. This behavior can be characterized by the following expression

$$\begin{cases} v_P = L_P \dfrac{di_P}{dt} + M_{12} \dfrac{di_S}{dt} = L_P \dfrac{d}{dt}\left(i_P + i_S \dfrac{M_{12}}{L_P}\right) \\ v_S = L_S \dfrac{di_S}{dt} + M_{12} \dfrac{di_P}{dt} = L_S \dfrac{d}{dt}\left(i_S + i_P \dfrac{M_{12}}{L_S}\right) \end{cases} \tag{3-16}$$

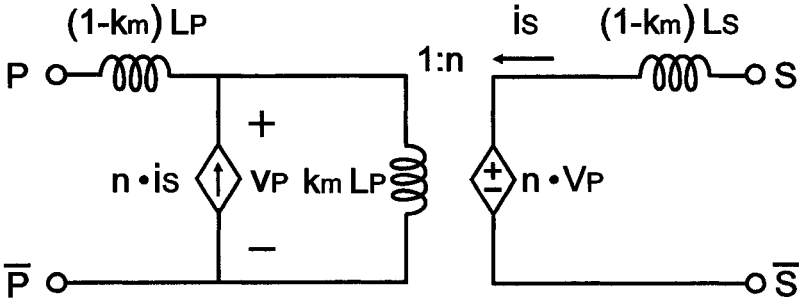
Based on the above expression, the circuit model of a transformer (shown in Figure 3-21-b) can be synthesized [28]. Alternative circuit models (in Figure 3-21-c and Figure 3-21-d) can also be obtained by including (3-14) and (3-16).



(a)

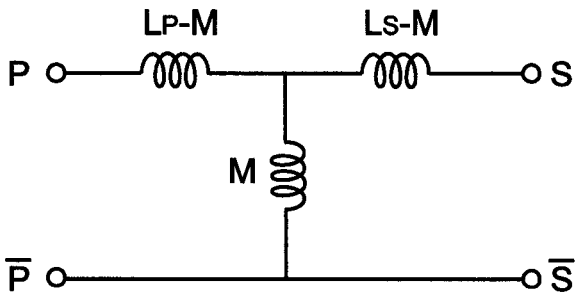


(b)



(c)

Figure 3-21 Transformer and its circuit model



(d)

Figure 3-21 Transformer and its circuit model (continued)

During the following analysis, we will use the transformer model in Figure 3-21-b. The corresponding small-signal model is drawn in Figure 3-22. Applying KCL at node S, we get

$$i_x + g_m v_{gs} - i_S = nk \cdot i_S + \frac{v_x}{sL_P}$$

$$i_S = \frac{v_g}{sL_S} + \frac{k}{n} i_P$$

$$v_{gs} = -\frac{i_S}{sC_{gs}}$$

$$i_P = i_x + g_m v_{gs}$$

$$v_g = v_x + v_{gs}$$

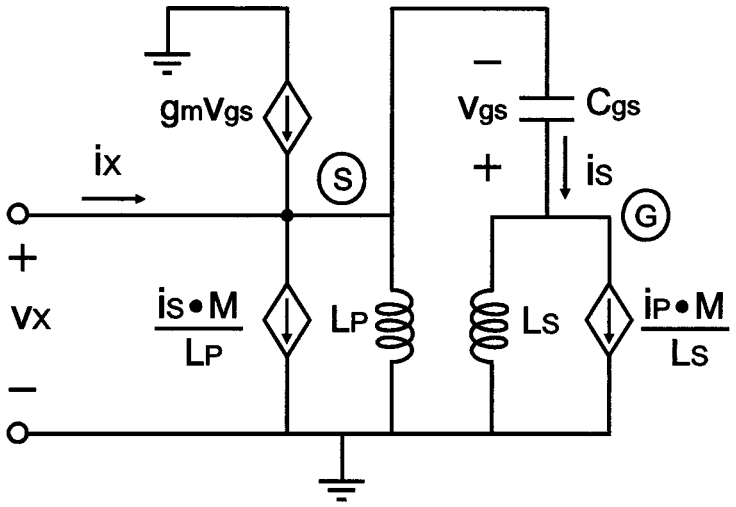


Figure 3-22 Small signal model for gm-boosted CGLNA with transformer

Solving the above equations, we finally get

$$\frac{i_x}{v_x}=\frac{1}{sL_P}\cdot\frac{1+\frac{k}{n}g_m sL_S+(1+\frac{k}{n})s^2L_SC_{gs}}{1+(1-k^2)\,s^2L_SC_{gs}}+\frac{1}{sL_S}\cdot\frac{g_m sL_S+(1+nk)s^2L_SC_{gs}}{1+(1-k^2)\,s^2L_SC_{gs}} \qquad (3\text{-}17)$$

For modern IC technology, a reasonably good coupling coefficient can be achieved; For example, typically k varies from 0.6 to 0.9, which allows the approximation that $\left|(1-k^2)\;s^2L_SC_{gs}\right|<<1$. Therefore, (3-17) can be simplified as

$$\begin{aligned}\frac{i_x}{v_x}&\approx\frac{1}{sL_P}\cdot\frac{1+\frac{k}{n}g_m sL_S+(1+\frac{k}{n})s^2L_SC_{gs}}{1}+\frac{1}{sL_S}\cdot\frac{g_m sL_S+(1+nk)s^2L_SC_{gs}}{1}\\&=\frac{1}{sL_P}+\frac{k}{n}g_m\cdot\frac{L_S}{L_P}+(1+\frac{k}{n})sC_{gs}\cdot\frac{L_S}{L_P}+g_m+(1+nk)sC_{gs}\end{aligned}$$

Notice that with $\frac{L_S}{L_P}=n^2$, the above expression can be further simplified as

$$\frac{i_x}{v_x} \approx \frac{1}{sL_P} + (1+nk)\,g_m + (1+2nk+n^2)\,sC_{gs} \tag{3-18}$$

Equation (3-18) implies a clear physical meaning; that is, the input impedance can be viewed as a parallel RLC circuit (Figure 3-23) where

$$L=L_P$$

$$C_{GS}'=(1+2nk+n^2)\,C_{GS}$$

$$G_m=(1+nk)g_m$$

Considering the ideal case with k=1, n=1, we have

$$G_m=2g_m$$

$$L=L_P$$

$$C_{GS}'=4C_{GS}$$

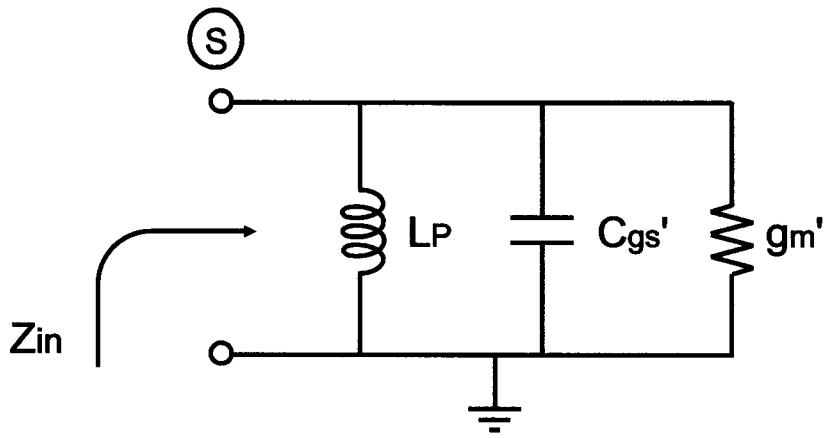


Figure 3-23 Equivalent circuit model fro input impedance of gm-boosted CGLNA with transformer

3.6 Summary

Being the first amplification stage in a receiver, the LNA is one of the critical building blocks. It should be able to amplify the RF signal and suppress the noise from the subsequent mixer stage. CSLNA is currently more popular than CGLNA, mainly due to its capability of low-noise and high gain. However, owing to the high quality factor of the input matching circuit, CSLNA is also more sensitive to any variations and parasitic capacitance, which are difficult to predict and control. On the other hand, compared to CSLNA, CGLNA has easier input matching and is more robust in input matching, reverse isolation and stability. Unfortunately, the input matching sets a lower bound for the noise figure in a conventional CGLNA. In this chapter, a novel gm-boosted CGLNA is proposed to break the tight link between input matching and noise figure to some extent. The Gm-boosted CGLNA effectively boosts the transconductance and lowers the noise figure while preserving the advantages of CGLNA, such as robust input matching, high linearity, good reverse isolation, etc. In addition, it reduces the DC power consumption, which is very important for portable applications. The proposed gm-boosted CGLNA is more suitable for high frequency applications since to the first order, its noise figure is constant when frequency varies. Finally, some possible implementations such as capacitive-cross coupled and transformer-based CGLNA topologies are also described.

Chapter 4 : Design of Voltage Controlled Oscillator

In Chapter 3, low-noise design techniques for the very first amplification stage in a receiver chain, the LNA, were discussed. After the radio frequency signal is amplified it usually needs to be down-converted to a lower intermediate frequency; the circuit block that performs this function is a mixer. As implied by its name, it performs frequency conversion by simply mixing the RF signal with an ideally pure local oscillation (LO) signal. One of the challenging tasks in integrated RF receiver design is to provide, or synthesize, the high quality LO signal on chip, as required by the stringent communication standards. There are many ways to synthesize the LO signal, with the most popular being the use of a phase-locked loop (PLLL) [29][30][31].

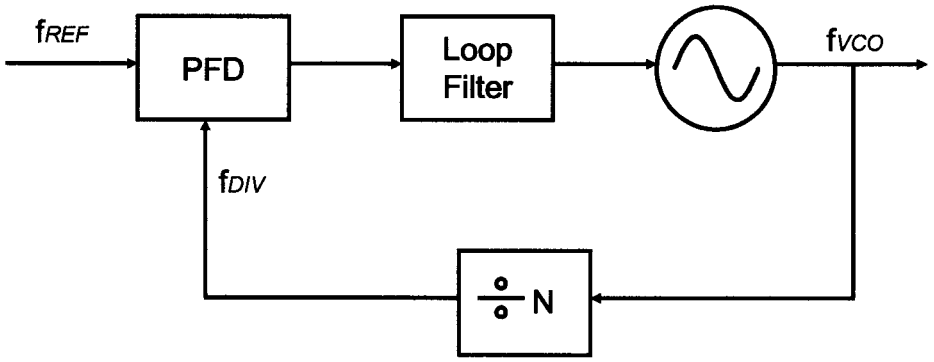


Figure 4-1 Simplified structure of phase-locked loop

Shown in Figure 4-1 is a typical block diagram of a PLL. A phase-frequency detector (PFD) detects the phase and/or frequency difference between the applied

reference frequency and the divided VCO output frequency and generates a DC voltage proportional to the difference. Therefore, PFD is conveniently modeled as a gain block. The low pass loop filter following the PFD introduces poles to attenuate high frequency components and extract the DC information from PFD output signal. It usually includes zeros to guarantee a sufficient unity-gain phase margin ensuring that the feedback loop is stable. A voltage-controlled oscillator generates an oscillating waveform at the desired frequency according to control signal V_{ctrl} applied to its input. In the phase domain, the VCO is modeled as an integrator.

A PLL is essentially a feedback system with high loop gain, which guarantees that in steady state or locked condition the phase difference between the reference and divided VCO output waveforms is constant. Since frequency is the time derivative of phase, the reference frequency and divided VCO output frequency must satisfy

$$f_{VCO} = N \cdot f_{REF}$$

To obtain the desired frequency of the VCO as applied to the RF receiver, N is designed to be variable. It is modeled simply as a gain block with a gain of $1/N$ in the phase/frequency domain.

The purity of the synthesized output is extremely important characteristic in determining the reliability of RF reception. For example, the sidebands adjacent to the desired oscillation frequency in a practical oscillator may corrupt the desired signal by a process known as "reciprocal mixing".

The purity of the oscillation signal is often characterized using phase noise in the frequency domain, or jitter in the time domain. In this thesis, we use phase noise as the measure of signal purity, which is more common in RF applications.

In a PLL, all the constituent circuit blocks such as the VCO, frequency divider, loop filter, charge pump and PFD contribute phase noise at the output. For a well-designed PLL, however, it is often the case that the VCO is the dominant source of phase noise [32][33]. Therefore, in the following discussion, we focus on VCO design with phase noise as a primary concern. Due to its superior phase noise performance, the basic *LC* oscillator topology is widely used in RF receiver design. Consequently, we focus our discussion on *LC* oscillators. Before we discuss the phase noise of the LC oscillator, it is instructive to look at the principles of oscillation first.

4.1 Principle of Oscillation

An ideal oscillator generates a periodic output (in strict sense). In an LC oscillator, the output usually takes the form of sinusoid, which may be expressed as $V_0(t)=A\cos(\omega_0 t+\phi_0)$, where A is the amplitude, ω_0 is the oscillation frequency, and ϕ_0 is the phase reference.

In a practical LC oscillator the output is given by

$$V_o(t) = A(t)\cos[\omega_0 t+\phi(t)] \tag{4-1-a}$$

The instantaneous frequency f(t) is simply the time derivative of the total phase

$$f(t) = \frac{d}{dt}[\omega_0 t+\phi(t)] = \omega_0 + \frac{d}{dt}[\phi(t)] \tag{4-1-b}$$

In general, both the amplitude A(t) and phase ϕ (t) of a practical oscillator are functions of time, which reveals the fact that in nature, the oscillator is a ***time variant*** system. The fluctuations of the phase and amplitude in time domain lead to the existence of sidebands around the resonant frequency ω_0 in the spectrum of a

practical oscillator. The time variant phase causes frequency deviation, as is implied by equation (4-1-b). This phenomenon is referred as phase noise in the spectrum of oscillator output.

An oscillator can be viewed as a feedback system or equivalently from a one-port point of view. Next, we consider the principle of oscillation from both views.

4.1.1 Feedback Model

Although not all, most oscillators can be regarded as a feedback system as depicted in Figure 4-2 where the transfer function from $X(s)$ to $Y(s)$ is

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1-H(s)}$$

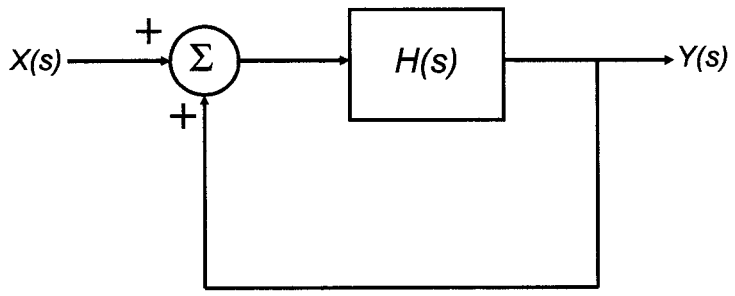


Figure 4-2 Oscillator viewed as feedback system

Oscillation occurs for the condition $H(s_0)=1$. Even without an input stimulus, i.e., $X(s)=0$, the oscillation is self-sustained. To maintain a constant amplitude, s_0 should be purely imaginary; that is,

$$H(j\omega_0) = 1$$

The above condition implies the two necessary yet not sufficient conditions that must be met at ω_0 to sustain steady-state oscillation:

$$\begin{aligned} |H(j\omega_0)| &= 1 \\ \angle H(j\omega_0) &= 0^\circ \end{aligned} \tag{4-2}$$

Known as Barkhausen's criteria, (4-2) reveals the requirements for both amplitude and phase shift of the loop gain transfer function of the system.

An *LC* resonant tank is an integral component of an *LC* oscillator circuit. It functions as a frequency selective network to eliminate higher-order harmonics and to therefore stabilize the oscillation frequency (Figure 4-3).

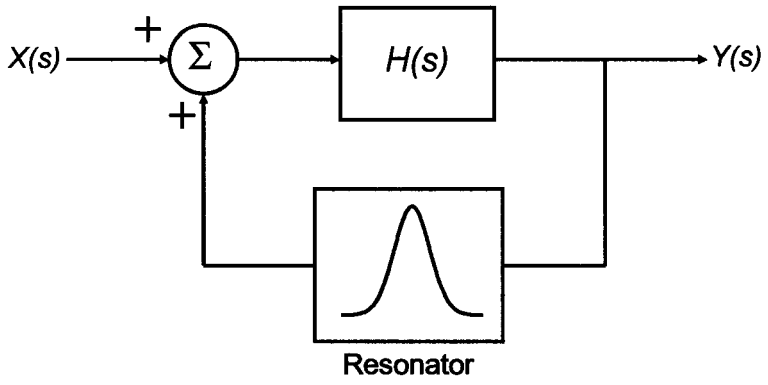
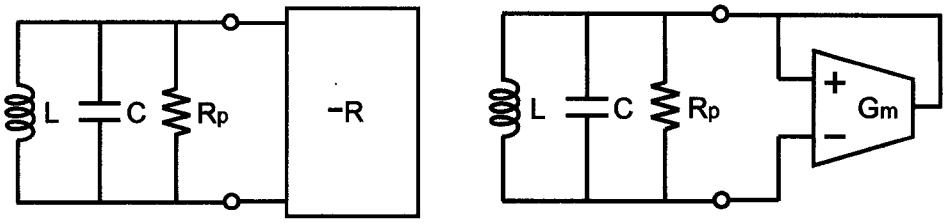


Figure 4-3 Feedback model of oscillator with resonant circuit

4.1.2 One-Port Oscillator Model

The resonant circuit in Figure 4-3 is usually implemented as an *LC* tank. If the *LC* tank is lossless, the oscillation frequency and amplitude are maintained at stable values because the poles of the transfer function lie on the imaginary axis. However, the loss resistance associated with the inductor *L* and capacitor *C* causes

the poles to move into left half plane so that the oscillation decays away over time if there is no mechanism to periodically compensate for the energy losses.



(a) (b)

Figure 4-4 One-port view of oscillators (a) RLC tank with negative resistance (b) Possible implementation

In a typical IC implementation of an on-chip inductor and capacitor, the resonator has a relatively high quality factor, Q, which validates a narrow band frequency approximation. That is, over a narrow range of frequencies the *LC* tank can be modeled as a parallel combination of inductance, capacitance and resistance as shown in Figure 4-4-a. The *LC* tank with high Q produces a sinusoidal output signal with a dominant fundamental frequency component. This situation is quite different from that of a ring oscillator wherein the output has numerous significant harmonic components.

To overcome the energy loss from R_P, active components forming a small-signal negative resistance is required to replenish the energy loss during every cycle of oscillation. This one-port view of oscillation provides a useful alternative view of the basic principle of oscillation.

In *Si*-based IC technologies, the negative resistance/conductance is conveniently realized as a small-signal transconductance through the use of MOSFETs or BJTs (Figure 4-4-b).

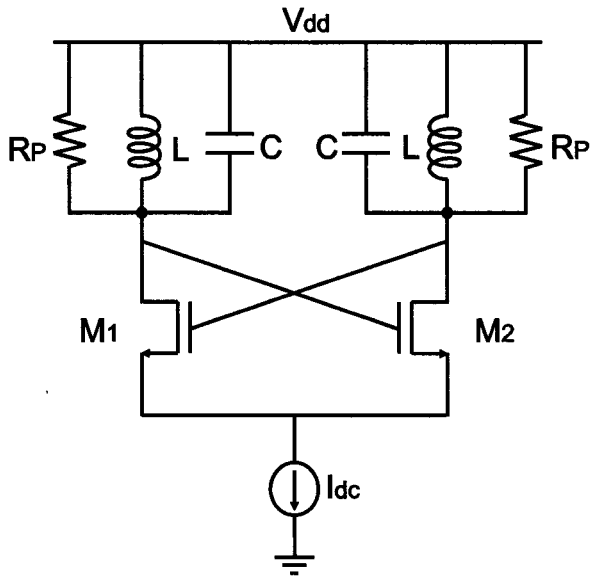


Figure 4-5 Cross coupled oscillator

The cross-coupled *LC* oscillator that is widely used in modern RF IC design serves as a good example to illustrate the one-port view of oscillation. As shown in Figure 4-5, it comprises the *LC* tank and the negative conductance circuit formed by cross-coupled transistors M_1 and M_2. From small-signal point of view, the cross-coupled transistor pair provides the negative resistance required to compensate for the losses in the *LC* tank circuit. It can be shown that the small-signal impedance looking into drains of M_1 and M_2 is $-2/g_m$ assuming the parasitic capacitance is neglected. Although MOSFETs are used herein to explain the negative-G_m principle, BJTs are, of course, another viable circuit topology for implementing a negative conductance.

To enable oscillation, the negative small-signal conductance added by the cross-coupled transistor pair should overcome the loss in R_P; hence,

$$g_m > 1/R_P$$

$$\text{or } g_m R_P > 1 \tag{4-3}$$

The above inequality is commonly referred to as the start-up condition. It imposes a lower bound on the power dissipation of the overall oscillator circuit. In practice, because process variations can be as large as 20%, a suitable safety margin (e.g., 3X in (4-3)) is ensure reliable start-up over all possible operating conditions.

A negative conductance can also be synthesized using only a single active device, which is highly desirable for noise consideration. The Colpitts configuration is one such one-transistor oscillator (Figure 4-6), in which the negative conductance is formed using transistor M_1 and capacitive divider C_1 and C_2 in a positive feedback arrangement. It can be shown that the small-signal impedance looking into the drain of M_1 is

$$\frac{V_X}{I_X} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2}$$

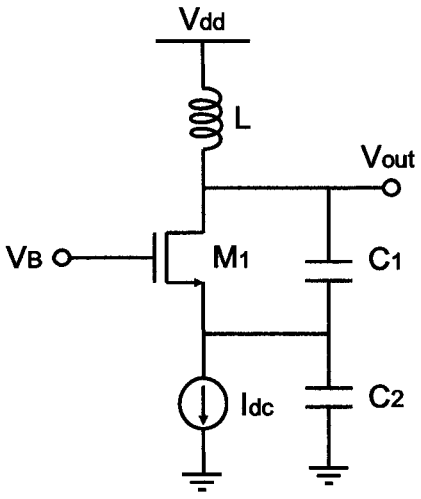


Figure 4-6 Colpitts oscillator

Therefore, the interaction between M_1 and the capacitive divider C_1 and C_2 results in a small signal negative resistance of $-g_m/\omega^2 C_1 C_2$. The capacitive component loading the tank circuit is given by the series combination $C_1C_2/(C_1+C_2)$. Performing a series to parallel transform, the negative conductance loading the tank is found to be

$$G_M = -\frac{g_m C_1 C_2}{(C_1+C_2)^2}$$

Therefore, the start-up condition for the Colpitts oscillator is

$$\frac{g_m C_1 C_2}{(C_1+C_2)^2} > \frac{1}{R_P}$$

$$\text{or } g_m R_P > \frac{(C_1+C_2)^2}{C_1 C_2} \geq 4 \qquad (4\text{-}4)$$

Comparing (4-3) and (4-4), we conclude that the Colpitts oscillator has an inherently more difficult start-up condition than the conventional cross-coupled LC oscillator. For example, under the typical condition that $C_2 = 4C_1$, (4-4) becomes

$$g_m R_P > 6.25$$

Therefore, a higher small-signal transconductance and greater power consumption are required for the Colpitts oscillator to achieve reliable start up. With lower power supply voltages, start-up is a more severe issue for Colpitts oscillator.

We have briefly reviewed the principles of oscillation from both the feedback and one-port points of view. Both approaches are related and provide insights on oscillatory behavior. For example, the negative resistance/conductance is usually synthesized through the use of a positive feedback configuration. The cross-coupled

and Colpitts oscillator configurations both accommodate the feedback and one-port models. On the other hand, their detailed operation and phase noise performance are quite different as discussed below.

Phase fluctuations of the LO signal are problematic at the inputs to the mixer in a RF receiver or transmitter chain [34]. Fundamentally, phase noise causes a random variation in the zero crossing instants of the LO signal. The effect is equivalent to sampling at twice the LO frequency the random thermal and flicker noise sources using commutating switches. The up-conversion of flicker noise from the switching operation to IF frequencies at the mixer output is especially troublesome for a narrow channel width; if the flicker noise corner frequency is comparable to the channel bandwidth it may degrade the achievable SNR. Next, the origin of phase noise and a model to characterize it are described.

4.2 Phase Noise in Oscillator

There has been extensive study on the mechanism of phase noise in oscillators only with which can circuit designer optimize oscillator circuits [35][36]. As depicted in Figure 4-7, the phase noise of an oscillator is defined as

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}\ (\omega_0+\Delta\omega\ , 1Hz)}{P_S}\right]$$

where P_{sideband} $(\omega_0+\Delta\omega, 1Hz)$ represents the single side-band power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz, and P_S is the power of the carrier [37].

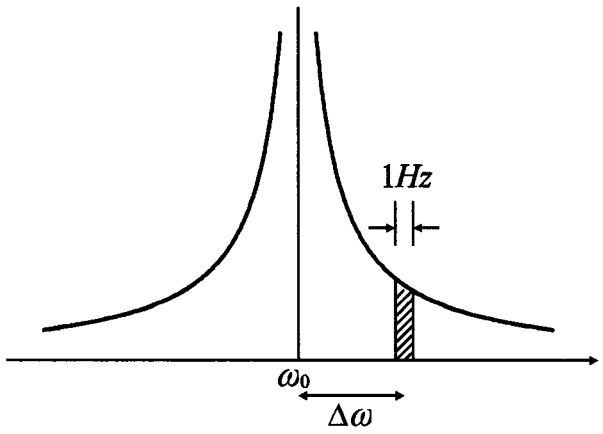


Figure 4-7 Phase noise definition

Figure 4-8 shows a typical phase noise plot with three characteristic regions; namely, the $1/f^3$ region, the $1/f^2$ region and the frequency-independent noise floor. It seems plausible to attribute the $1/f^3$ region to 1/f noise introduced by various active devices. In the $1/f^2$ region Figure 4-8 shows that phase noise is proportional to the square of the offset frequency. This is explained using the following linear analysis.

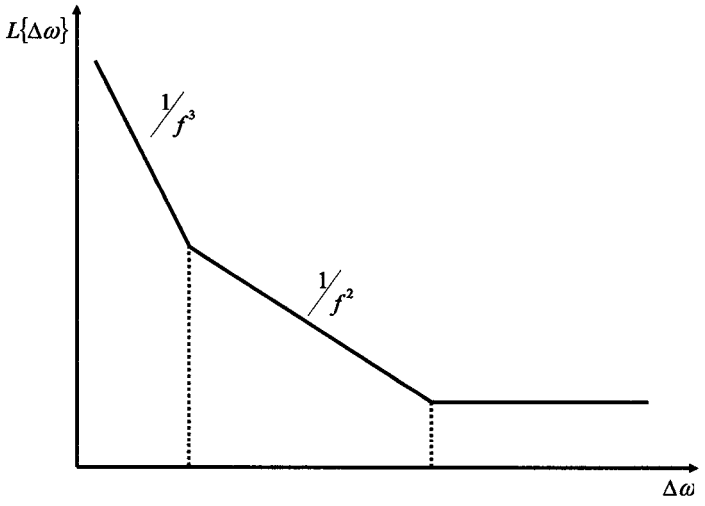


Figure 4-8 A typical phase noise plot

If there are no losses, the *LC* tank circuit conserves the energy stored in the system so that the output oscillates forever without any decay in amplitude. The poles associated with the LC tank lie exactly on the imaginary axis in the *s*-plane. However, any parasitic resistance R_P dissipates power so active devices are required to compensate the energy loss. The random thermal noise from both R_P and the active devices affects both the amplitude and phase of the oscillatory waveform. Because the tank is a parallel RLC resonant circuit, it is convenient to use an equivalent noise current source to model the noise from R_P, as depicted in Figure 4-9 where

$$\overline{i_n^2}/\Delta f = 4kTG = 4kT/R_P .$$

The noise current that is injected into the *LC* tank circuit and converted to noise voltage causes a phase shift error that accumulates over time. The transfer function is simply the impedance of the *RLC* tank evaluated an offset frequency of $\Delta\omega$. In practice, it is usually true that $\Delta\omega << \omega_0$. The impedance is calculated to be

$$\begin{aligned} Z(\Delta\omega) &\approx \frac{1}{G_L}\cdot\frac{1}{1+j2Q_L\frac{\Delta\omega}{\omega_0}} \\ &\approx \frac{1}{G_L}\cdot\left(1-j2Q_L\frac{\Delta\omega}{\omega_0}\right) \end{aligned}$$

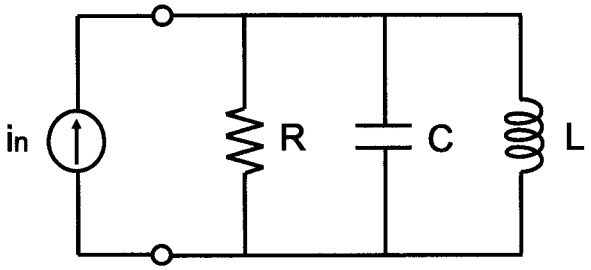


Figure 4-9 RLC tank with injected noise current source

In steady-state operation, the real part of the impedance is cancelled by the negative conductance produced by the active circuitry. Therefore, the resulting transfer function is just the imaginary part of the impedance

$$H(\Delta\omega) = -j\frac{1}{G_L}\cdot\frac{\omega_0}{2Q_L\Delta\omega}$$

To account for the effects of all noisy current sources in the oscillator circuit, the power spectral density associated with the output voltage of the *LC* tank is commonly multiplied by an empirical parameter *F*, and becomes

$$\begin{aligned}\overline{v_n^2}/\Delta f &= \left|H(\Delta\omega)^2\right|\cdot\overline{i_n^2}/\Delta f \\ &= \left(\frac{1}{G_L}\right)^2\cdot\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\cdot 4FkTG_L\end{aligned}$$

According to the *Equipartition Theorem*, the random fluctuation of the output voltage leads to both amplitude and phase noise contributions that are equally distributed between amplitude and phase fluctuations, which accounts for the factor ½ in the equations below. Neglecting amplitude fluctuations gives a phase noise of

$$\begin{aligned}L(\Delta\omega) &= 10\log\left(\frac{\overline{v_n^2}/\Delta f}{\overline{v_{sig}^2}}\right) \\ &= 10\log\left(\frac{\frac{1}{2}\left|H(\Delta\omega)^2\right|\cdot\overline{i_n^2}/\Delta f}{\frac{1}{2}\overline{v_{sig}^2}}\right) \\ &= 10\log\left[\frac{2FkT}{P_S}\cdot\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\end{aligned} \tag{4-5}$$

where P_S is the average power dissipated in the equivalent resistive part of the tank.

To encompass the three regions of the phase noise plot of Figure 4-8, (4-5) is revised as

$$L\{\Delta\omega\} = 10\log\left\{\frac{2FkT}{P_S}\cdot\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right\}$$

where $\Delta\omega^3_{1/f}$ is the corner frequency between the $1/f^3$ and $1/f^2$ regions shown in Figure 4-8.

The above equation is known as Leeson's phase noise model. Although semi-empirical in nature, it is widely referenced because it relates phase noise to practical design parameters such as oscillation amplitude, quality factor of the LC tank, oscillation frequency and offset frequency. It provides significant intuition; e.g., doubling the quality factor Q of the *LC* tank improves the phase noise by 6dB.

Unfortunately, Leeson's model does not provide any insights into the empirical noise factor F that is usually known only *a posteriori*. The question remains: what determines the value of the noise factor F and how is it related to the circuit parameters for different oscillator topologies?

The question posed above is addressed using a non-empirical phase noise model. Clearly, the model should deal in an analytic way with the inherent time-variant nature of phase noise. Recently, Hajimiri and Lee proposed a linear time-variant (LTV) phase noise model [38][39][40] based on the following assumptions:

- The random phase shifts are added linearly.
- The phase shift introduced by the noise current is time variant.

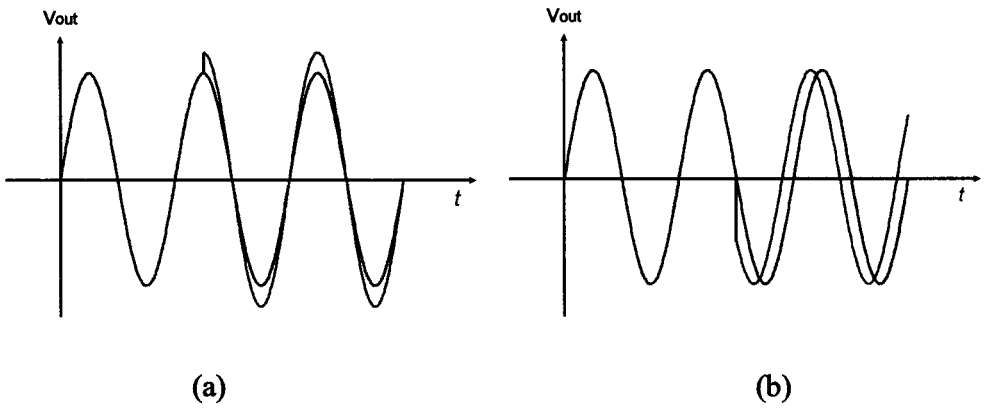


Figure 4-10 Phase shift vs. time instant of injected noise current

The first assumption is easily understood since random noise from either passive or active devices is usually in such a small magnitude that its effect can be regarded as a perturbation that is accurately treated using the superposition principle.

The second assumption is appreciated in view of the following important observation. The phase shift introduced in the output waveform by the noise current injected into the *LC* tank depends on the specific time instant when it is injected (Figure 4-10). In Figure 4-10-a, for example, the noise current injected at the peak of the voltage waveform causes an amplitude fluctuation but no phase shift at all in the zero crossing point. In contrast, in Figure 4-10-b, noise current injected exactly at the zero crossing point results in zero amplitude error but a maximum phase shift error that cannot be corrected.

From Figure 4-10, we conclude that the magnitude of the excess phase shift error not only depends on the power spectral density of the noise current, but also on the time instant when the noise current is injected into the tank circuit. In other words, the impulse response $h_\phi(t,\tau)$ is time-variant, where τ is the time at which the noise current impulse is injected. The time dependency is conveniently described

using the so-called impulse sensitivity function (ISF) $\Gamma(\tau)$; it represents the amount of phase shift that results from the injection of an impulse of noise current at time τ. Because $\Gamma(\tau)$ is periodic it can be written as $\Gamma(\omega_0\tau)$. The impulse response $h_\phi(t,\tau)$ is related to the ISF as

$$h_\phi(t,\tau) = \Gamma(\omega_0\tau) \cdot u(t-\tau)$$

Based on the assumption that the phase shift errors add linearly, the total phase shift error can be expressed as

$$\phi(t) = \int_{-\infty}^{+\infty} h_\phi(t,\tau) i(\tau) d\tau = \int_{-\infty}^{t} \Gamma(\omega_0\tau) i(\tau) d\tau$$

After obtaining the phase shift $\phi(t)$ and relating it to (4-1-a), it can be shown that the phase noise due to a noisy current with power spectral density $\overline{i_n^2}/\Delta f$ is

$$L\{\Delta\omega\} = \frac{\overline{i_n^2}/\Delta f}{2q_{max}^2} \cdot \frac{\Gamma_{eff,rms}^2}{\Delta\omega^2}$$

where $\Delta\omega$ is the offset frequency from the carrier frequency, $\Gamma_{eff,max}$ is the rms value of the effective impulse sensitivity function associated with that particular noise source and q_{max} is the maximum charge swing across the LC tank.

4.3 Comparisons of Cross-Coupled and Colpitts LC Oscillators

The cross-coupled *LC* oscillator configuration is currently popular because of its good phase noise performance, easy start-up and relatively wide tuning range [41][42][43]. As discussed before, most *LC* oscillators can be viewed as an

amplifier with an *LC* resonant load configured in a positive feedback fashion, as illustrated by the cross-coupled *LC* oscillator example redrawn in Figure 4-11. It clearly shows that the cross-coupled *LC* oscillator actually comprises a two-stage common-source amplifier with an *LC* resonant load where the overall output is connected to the input. At resonance, the *LC* tank exhibits real impedance, and therefore the phase shift around the loop is 360°, which suggests that the feedback is positive in nature. At low frequencies, the LC tank shows low impedance that effectively suppresses the possibility of latch-up, rather than oscillation. The nominal 180° phase shift provided by a single common-source amplifier stage necessitates the use of two stages to synthesize a positive feedback oscillator. In addition, the cross-coupled oscillator configuration naturally provides the differential outputs required in many practical realizations.

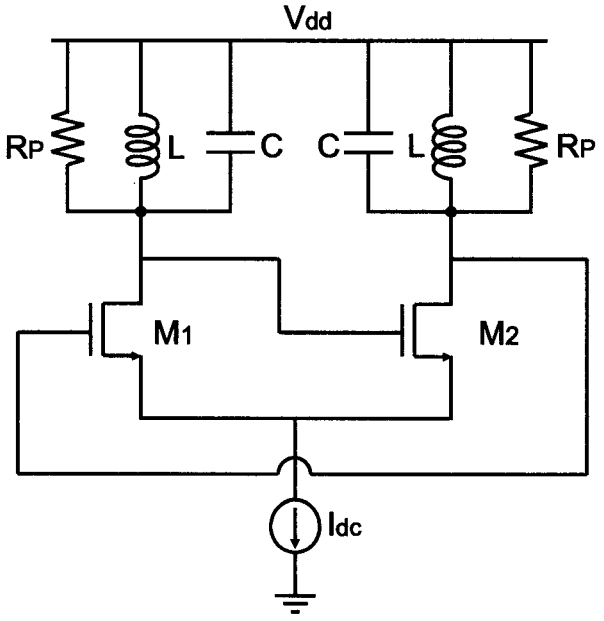


Figure 4-11 Cross-coupled oscillator redrawn as common-source amplifier in positive feedback

The amplitude of cross coupled oscillator can be approximated by

$$A = \frac{4}{\pi} I_B \cdot R_P \tag{4-6}$$

where it has been assumed that square wave current is injected into the LC tank during steady oscillation.

Similar to the cross-coupled oscillator, the Colpitts oscillator can also be synthesized using a common-gate amplifier. The basic idea is to form a positive feedback loop using the common-gate amplifier with the LC tank as its load. Based on the fact that the common-gate amplifier is inherently non-inverting, we surmise that only one stage is needed to achieve the positive feedback configuration.

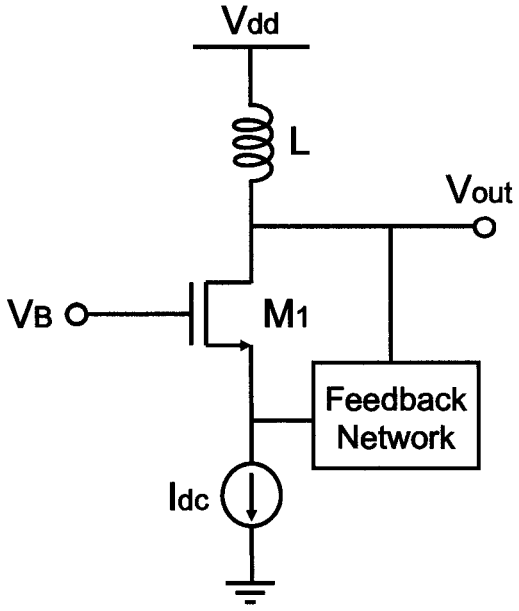


Figure 4-12 Common-gate amplifier based oscillator

To complete the positive feedback loop, the output (MOSFET drain terminal) should be connected to input (MOSFET source terminal) through a feedback network that can be either passive or active (Figure 4-12). The feedback network is needed to prevent the low impedance of the source node from directly loading the LC tank at the output and degrading its quality factor Q. Therefore, the capability of impedance transformation is necessary for the feedback network to achieve the desired isolation between the drain and source nodes of the active device. Notice that the effective transconductance in steady-state operation is different from the small-signal transconductance; in general, the large-signal transconductance is less than its small-signal counterpart.

As mentioned above, the positive feedback network can be either an active or passive implementation. An ideal active candidate for the feedback network is the basic source-follower circuit that is also often used for impedance transformation purposes. By merging a source-follower circuit into the basic feedback topology shown in Figure 4-12, we obtain the oscillator shown in Figure 4-13. It is instructive to calculate the small-signal impedance at the drain node of M_1. Applying KCL at source node of M_1, we obtain

$$v_S = \frac{g_{m2}}{g_{m1}+g_{m2}} v_X \tag{4-7}$$

$$i_X = -g_{m2} V_S$$

$$\frac{i_X}{v_X} = -\frac{g_{m1} g_{m2}}{g_{m1}+g_{m2}}$$

If $g_{m1} = g_{m2} = g_m$, we have

$$\frac{i_X}{v_X} = -\frac{g_m}{2}$$

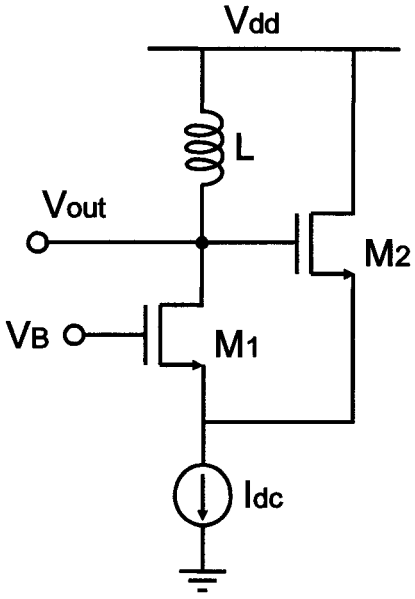


Figure 4-13 Common-gate amplifier based oscillator with source follower as feedback network

Of course, a passive impedance down-conversion feedback network is also possible. For example, a tapped-capacitor network can be used as in Figure 4-12 which results in the well known Colpitts LC oscillator configuration. Although the Colpitts LC oscillator has many variants, we specifically refer to the oscillator in Figure 4-6 as Colpitts oscillator in the following discussion.

Similar to (4-7), v_S is an attenuated version of v_X in a Colpitts oscillator,

$$v_S = \frac{C_1}{C_1+C_2} v_X$$

In summary, in Figure 4-6 and Figure 4-13, the drain node voltage swing is replicated with attenuation and applied to the source terminal of the MOSFET to form the required positive feedback loop. The primary differences are in the details of the implementation of the feedback network. Of course, implementations other than those described above are also possible. In a Hartley oscillator, for example, the feedback network is often implemented using a tapped-inductor impedance transformer and it can also be realized using a monolithic transformer with the desired turns ratio.

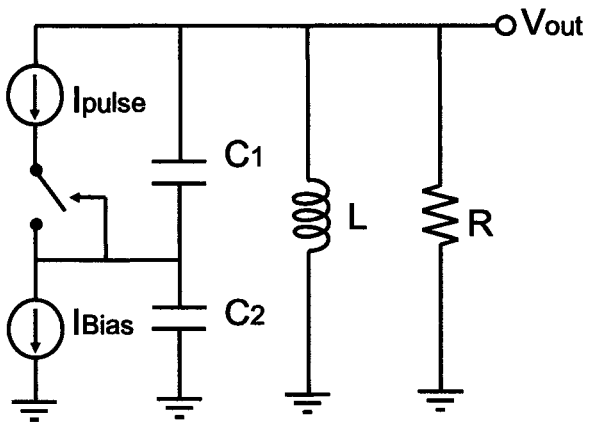


Figure 4-14 Simplified model for Colpitts oscillator

It is also instructive to compare the cross-coupled LC oscillator to the Colpitts oscillator in terms of phase noise performance.

Figure 4-14 depicts a simplified model of the Colpitts oscillator wherein M_1 acts as a switch. When V_{out} and V_S are low, M_1 is ON and node V_S is charged to a higher voltage level. When V_{out} and V_S are high, M_1 is OFF and V_S is discharged by the tail current source I_{Bias}. The switch is ON for a fractional period that is usually less than half a cycle. From another viewpoint, the switch works in a *class-C* mode as illustrated in Figure 4-15. The restriction imposed by the tail current source is that

the average of drain current I_{pulse} must equal I_{Bias}. Clearly, if the voltage swings of V_{out} and V_S are increased, a higher peak value of I_{pulse} results that leads to shorter duration τ during which the switch is ON. Therefore, the average value of V_S is closer to V_B-V_{TH}. Note that the operation described above is independent of the details of M_1. In fact, M_1 can be replaced by a BJT without affecting the basic operation since the transistor simply behaves as a switch.

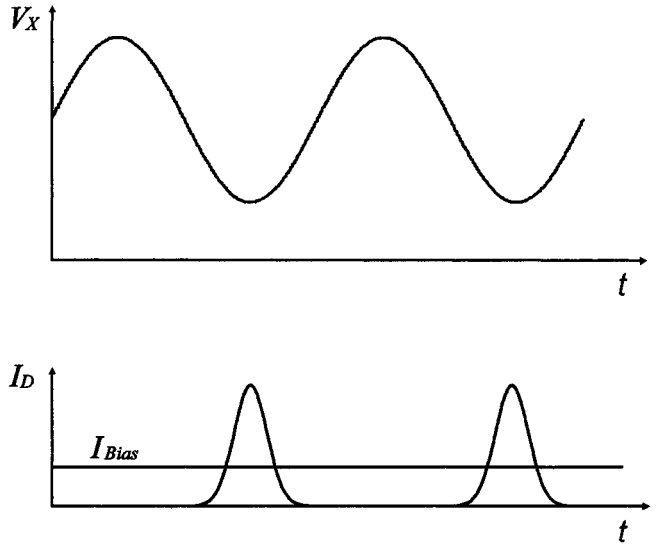


Figure 4-15 Voltage and current waveform of Colpitts oscillator

Consider the limiting case of Figure 4-15 where the current in M_1 is modeled as a square pulse with duration of τ. Since the average of I_{pulse} is I_{Bias}, τ is found to be

$$\tau = T \cdot \frac{I_{Bias}}{I_{pulse}}$$

Hence, if the available current from transistor is increased, τ is restricted to a shorter duration; carrying this further, the current pulse eventually approaches a Dirac function with area $T \cdot I_{Bias}$ and the fundamental component is

$$a_1 = \frac{2}{T}\int_0^T I_{Bias} T \cdot \delta(t) \cos \omega_0 t dt$$
$$= 2I_{Bias}$$

Hence the amplitude of oscillation exhibited by the Colpitts *LC* oscillator is approximately

$$A = 2I_{Bias} \cdot R_P \tag{4-8}$$

Therefore, Colpitts oscillator has larger amplitude compared to that of cross coupled oscillator, as implied by (4-6) and (4-8).

4.4 Proposed Differential Colpitts VCOs

As discussed in Section 3.3 with reference to the Colpitts *LC* oscillator, the drain current that carries channel thermal noise and flicker noise is injected into the *LC* tank circuit near the time of its peak voltage. As described earlier, at that point the sensitivity of the phase noise of the oscillator to the injected noise current is minimal. This highly desirable behavior accounts for the superior phase noise performance of the Colpitts configuration.

Although it has been very popular in discrete deign, the Colpitts *LC* oscillator has not seen widespread use in integrated circuit design for several reasons. First, it is more difficult to ensure a reliable start-up condition as seen from (4-3) and (4-4); reliable start-up in the presence of PVT variations mandates the use of a safety margin in design. The required margin is larger with the Colpitts configuration, which consumes additional DC power.

Second, being a basic one-transistor oscillator, the Colpitts *LC* oscillator provides only a single-ended output. To suppress even-order harmonic distortion and

common-mode interference, differential topologies are preferable in modern IC design. The lack of differential outputs impedes use of the conventional Colpitts oscillator.

In summary, although the Colpitts oscillator behaves ideally in terms of phase noise performance, the conventional form suffers from the need for more current consumption to ensure start up and the lack of differential outputs [44].

Our efforts to improve the performance of the Colpitts oscillator begin with synthesis of a differential Colpitts oscillator. It is shown shortly that easier start up is a direct byproduct of such a circuit topology.

Several important observations are made before we delve into the synthesis.

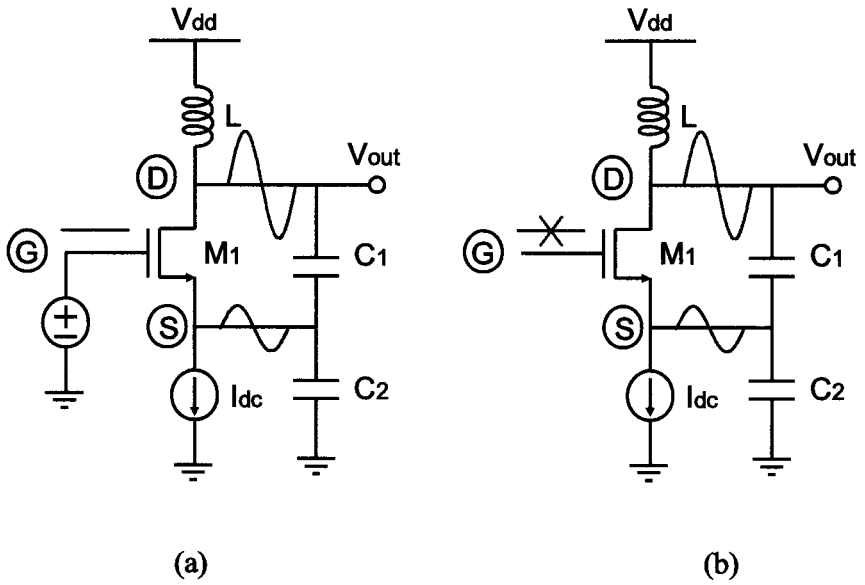
- From an amplifier point of view, a Colpitts *LC* oscillator is essentially based on a common-gate amplifier. During start up, M_1 operates as small-signal common-gate amplifier in a positive feedback configuration. The positive feedback ensures that the amplitude of oscillation increases towards a steady-state condition.

- In steady-state oscillation, however, M_1 functions as a switch. The switch is ON when the tank voltage peaks for the duration of less than half a cycle. The resulting class-*C* mode of operation ensures that the drain current is injected into tank only when the sensitivity of the phase to noise current is minimal.

- Just as in the case of a mixer, fast switching is desired to minimize the time when the tank voltage passes through the zero crossing point, during which the sensitivity of the phase to noise current is maximum.

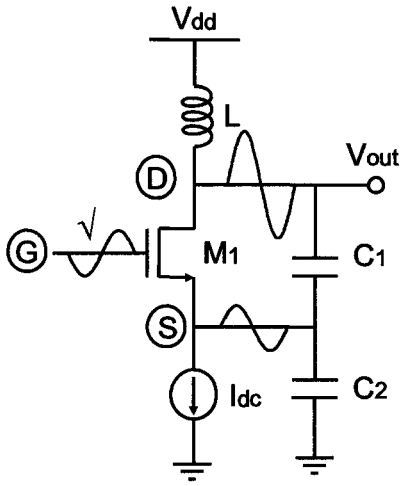
Recall from Chapter 3 that simply connecting the gate terminal of the conventional common-gate amplifier to a DC bias voltage is inefficient. Rather, coupling a portion of the oscillation signal from the source node to gate terminal enhances the effective transconductance and lowers the noise figure. Interestingly, this advantage not only holds for small-signal operation, but it applies to switching in the large signal model despite the fact that operation of the oscillator is *time variant* and that of the amplifier is *time invariant.*

A closer look at the operation of the Colpitts oscillator provides additional insight (Figure 4-16-a). The oscillator output voltage at the drain of M_1 has greater amplitude than the source voltage swing due to the passive voltage divider C_1 and C_2. The source voltage working with the fixed gate node voltage determines the switching of M_1 at every cycle. The first step towards achieving faster switching is to float the gate node as shown in Figure 4-16-b. Next, we address the question of what waveform to apply to the floating gate node and from where to obtain it.



(a) (b)

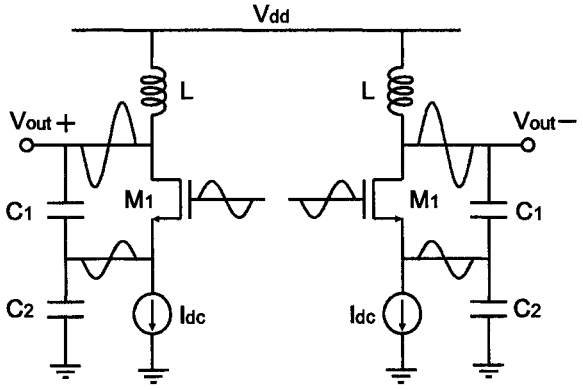
Figure 4-16 Evolution of the differential Colpitts oscillator



(c)

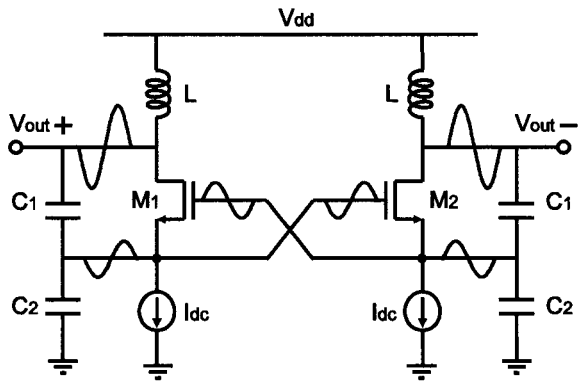
Figure 4-16 Evolution of the differential Colpitts oscillator (continued)

From our previous discussion on LNA circuits, it is natural to postulate that the gate node should be driven by a voltage swing inverted to that of the source so as to commutate M_1 more sharply. This advancement is shown in Figure 4-16-c.



(d)

Figure 4-16 Evolution of the differential Colpitts oscillator (continued)



(e)

Figure 4-16 Evolution of the differential Colpitts oscillator (continued)

In a conventional single-ended Colpitts oscillator, there is no such inversion available to be applied to the gate node. This is simply because the basic common-gate amplifier is non-inverting. However, the required inverse signal is readily available in a differential circuit with costs of doubling of DC power consumption and circuitry. Bearing in mind that differential topologies are desired in IC implementations to suppress even-order distortion and common-mode interference, it is desirable to consider the differential extension of the circuit in Figure 4-16-c, as shown in Figure 4-16-d.

We now revisit the question of how and where to connect the gate nodes. Obviously, they can be coupled to the source nodes of the opposite sides just as was done in g_m-boosted CGLNA. This leads to the conceptual, but not yet totally practical, Colpitts oscillator circuit shown in Figure 4-16-e.

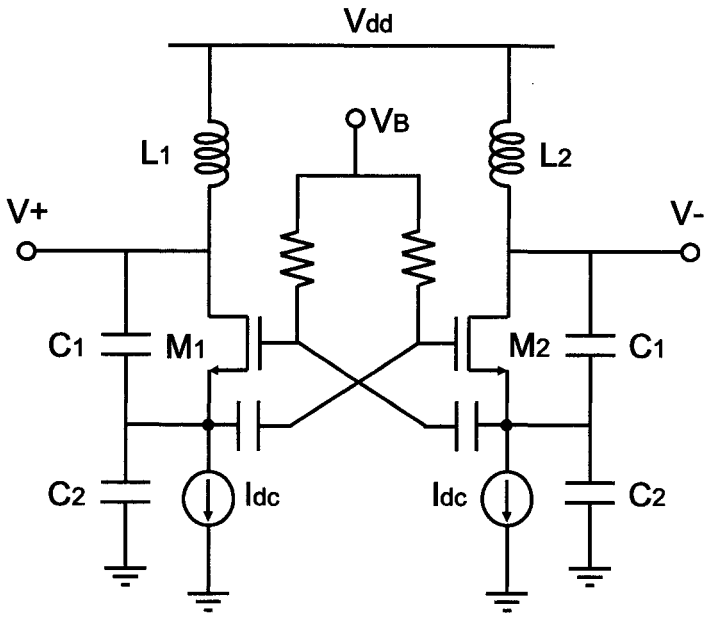


Figure 4-17 Differential Colpitts oscillator #1

Note that the circuit in Figure 4-16-e still has a problem of establishing the proper DC bias conditions. The final step is to add the transistor biasing circuitry. As shown in Figure 4-17, the cross coupling function can be maintained and the DC bias is introduced using blocking capacitors and resistors as shown.

We have synthesized a new differential Colpitts oscillator, and now we compare its performance to the conventional Colpitts oscillator.

- The differential configuration provides differential outputs.

- The approximately unity coupling between the gate and source terminals of M_1 effectively doubles the small-signal transconductance of the MOSFETs. Therefore, start up is easier than in the conventional Colpitts oscillator.

- Since the gate and source terminals are driven by signals of opposite phase, the transistors commutate the currents more sharply and behave more like ideal switches. The resulting faster switching is desired since it leads to improved phase noise performance. Interestingly enough, sharp switching is also welcome in mixer to suppress the noise from switching transistors [45][46].

A small-signal analysis shows that the start-up condition for the new differential Colpitts oscillator is given by

$$g_m R_P > \frac{(C_1+C_2)^2}{2C_1C_2}$$

Because the effective small-signal transconductance is doubled, the start-up condition is also relaxed by a factor of two.

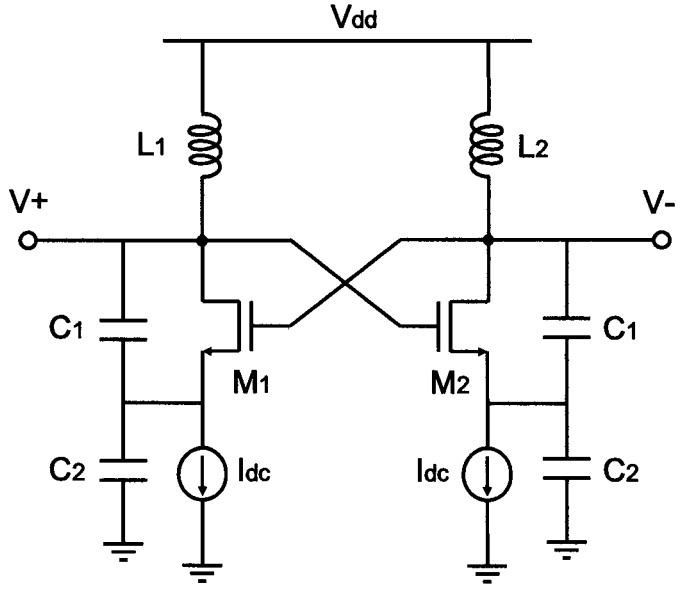


Figure 4-18 Differential Colpitts oscillator #2

Now returning to Figure 4-16-d, rather than connecting the floating gate node to the source of the transistor at the other side, we can alternatively connect it to the opposite drain terminal. Noticing that the opposite drain node has the same required phase relationship to allow differential operation and faster switching. The resulting new differential Colpitts oscillator is shown in Figure 4-18.

Compared to the oscillator in Figure 4-17, the oscillator in Figure 4-18 does not require coupling capacitors and bias resistors because it is effectively self-biased. Applying the same technique to the oscillator in Figure 4-13, we get the oscillator of Figure 4-19.

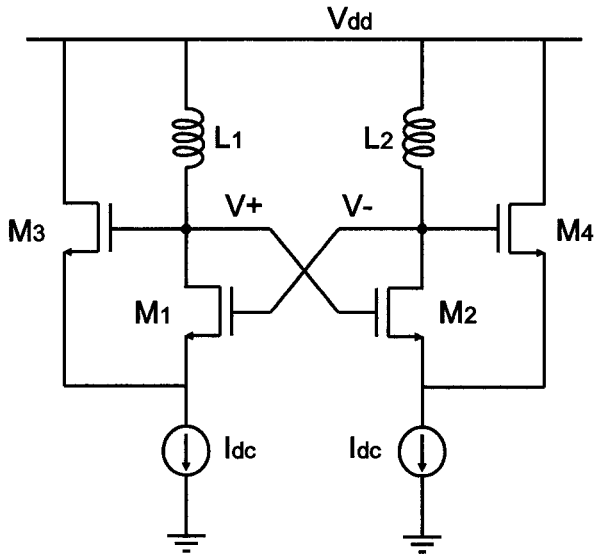


Figure 4-19 Differential Colpitts oscillator #3

In a conventional Colpitts oscillator, the tail current source is always ON. To reduce power consumption, a switching current source can be employed. The key point is that because in a Colpitts oscillator the MOSFET is on for less than half of a cycle, two switches can be used to steer ONE current source to the two MOSFETs while sustaining oscillation (Figure 4-20).

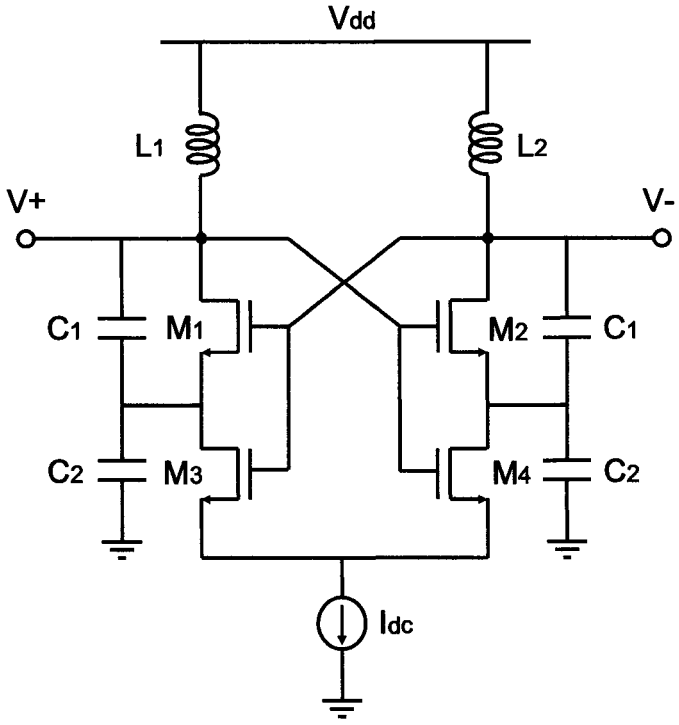


Figure 4-20 Differential Colpitts oscillator #4

4.5 Proposed Quadrature Colpitts VCO

Quadrature down-conversion is often required in direct conversion, image reject and wideband IF receiver architectures. There are several choices for this purpose. For example, quadrature operation can be achieved using frequency division from a VCO operating at twice the desired LO frequency. The drawbacks of this approach are that the VCO operates at a higher than needed frequency and the additional frequency division circuitry also consumes additional power.

The quadrature LO signals can also be synthesized by applying differential signals from a VCO to an RC polyphase filter. Unfortunately, undesirable attenuation from

the passive RC filter necessitates the use of buffers and therefore higher power consumption.

The third way to generate quadrature signals is through the use of a quadrature VCO, which is essentially a pair of oscillators coupled to each other so that it outputs quadrature signals directly [47][48][49][50]. Operation of the QVCO is explained using the linear model shown in Figure 4-21.

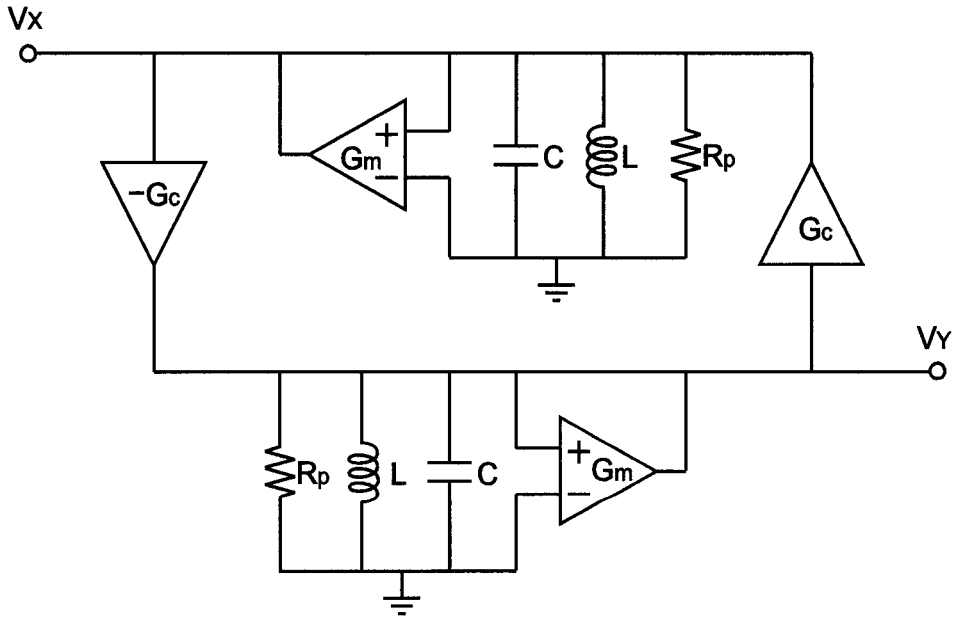


Figure 4-21 Linear model of QVCO

There are many ways to achieve quadrature coupling of two independent VCOs to obtain quadrature oscillation; e.g., parallel or series. The key point is that the unidirectional coupling between the two VCOs should always be in an inverse sense.

Next, we synthesize a novel QVCO based on the proposed differential Colpitts VCO with its superior phase noise performance. Again refer to the circuit shown in Figure 4-20. In this oscillator, M_3 and M_4 act as a switching current source that steers the bias current to either M_1 or M_2 to save power. To enable the steering function, the gate of M_3 is connected to the gate of M_1. Keeping in mind that we need proper coupling between the two independent VCOs, it is natural to surmise that we may use M_3 as the coupling connection in the QVCO; for example, its gate can be connected to the appropriate output of the other VCO. A similar connection is applied to M_4. After completing the connections, we arrive at the QVCO topology shown in Figure 4-22.

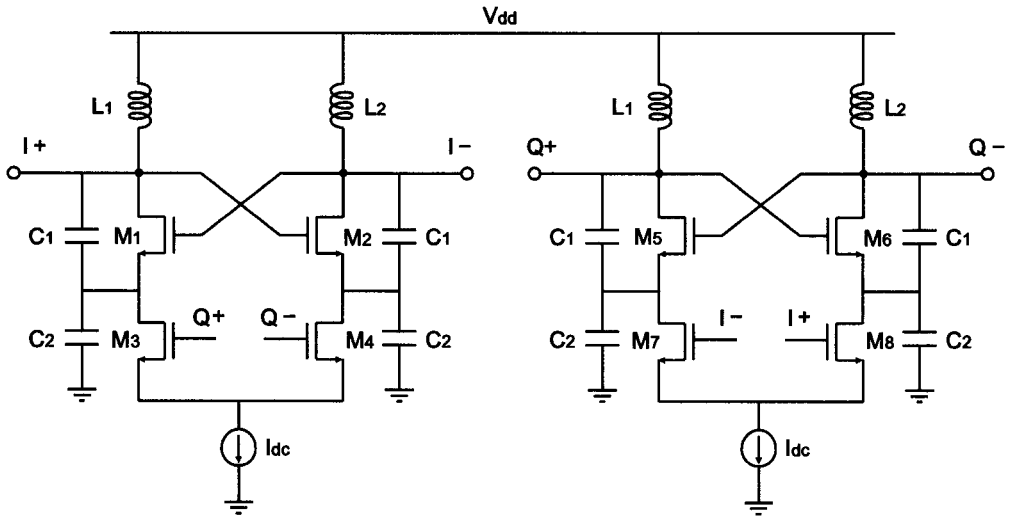


Figure 4-22 QVCO based on differential Colpitts topology

4.6 Summary

In this chapter, the basic principles of oscillation are first reviewed including the feedback model and one-port view of an oscillator. Next, the phase noise of the *LC*

oscillator is briefly discussed. Comparisons of cross-coupled and Colpitts VCOs, especially in terms of phase noise performance reveal methods of improving the phase noise performance in comparison to the conventional Colpitts VCO. A novel differential Colpitts VCO is introduced that provides differential outputs with superior phase noise performance. A quadrature VCO based on the new differential Colpitts VCO is also introduced.

Chapter 5 : Experimental Results

So far our discussion on low-noise design techniques has been focused on concepts and principles. In this Chapter, detailed circuit implementations are described.

Simulated using Cadence *SpectreRF* and fabricated in the IBM 0.18μm CMOS 7RF process available through MOSIS, the circuits were tested using a Cascade Microtechnology probe station with high frequency probing capability. On-wafer probing is adopted mainly for quick turnaround time.

The measurement results are reported along with detailed circuit schematics, testing setups and measured performance.

5.1 A Gm-Boosted CGLNA Using On-Chip Transformer

Figure 5-1 shows a schematic of the gm-boosted CGLNA. The source and gate terminals of MOSFET M_1 are coupled through an on-chip transformer that consists of primary inductor L_P and secondary inductor L_S. In this implementation, the turns ratio is designed to be n = 1:1, which corresponds to a feedback gain of A = 1. As discussed before, $A > 1$ is also possible by using a greater turns ratio. For example, if the turns ratio is designed to be n = 1:2, A=2 is achieved, which results in a lower noise figure. Herein, a turns ratio of n = 1:1 is used to verify the design principle due to its ease of implementation and modeling.

At the time of tape-out, there was no transformer model available from the foundry in the Cadence library. Consequently, the transformer circuit model was extracted

with the aid of *ASITIC*. The modeling accuracy is relaxed owing to the relatively wideband input matching characteristics of the common-gate amplifier as discussed in Chapter 3. To achieve lower noise figure, the coupling coefficient k (k<1) should be maximized. Simulation in *ASITIC* shows that smaller spacing between metal traces results in a higher coupling coefficient k. Therefore, minimum spacing is used to maximize k. The transformer is also designed so that it resonates with the capacitance associated with source of M_1, which includes the C_{SB} parasitic of M_1 and the parasitic capacitance of transformer itself. The gate of M_1 is biased from V_B, which also serves as an *AC* ground for the secondary inductor L_S. Transistor M_2 is added in the signal path to achieve higher reverse isolation, which also makes the input and output matching relatively independent. At the output, a tapped-capacitor matching network transforms the impedance at the drain of M_2 to 50Ω.

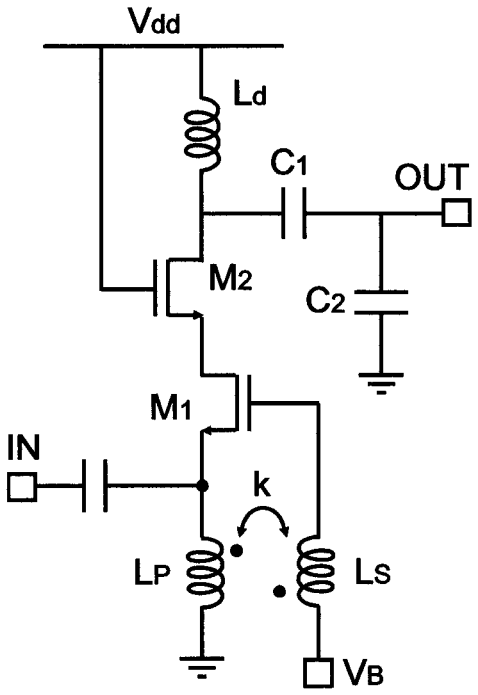


Figure 5-1 Gm-boosted CGLNA with on-chip transformer

A chip microphotograph of the gm-boosted CGLNA with on-chip transformer is shown in Figure 5-2. The circuit consumes an area of 910μm × 670μm including the probe pads.

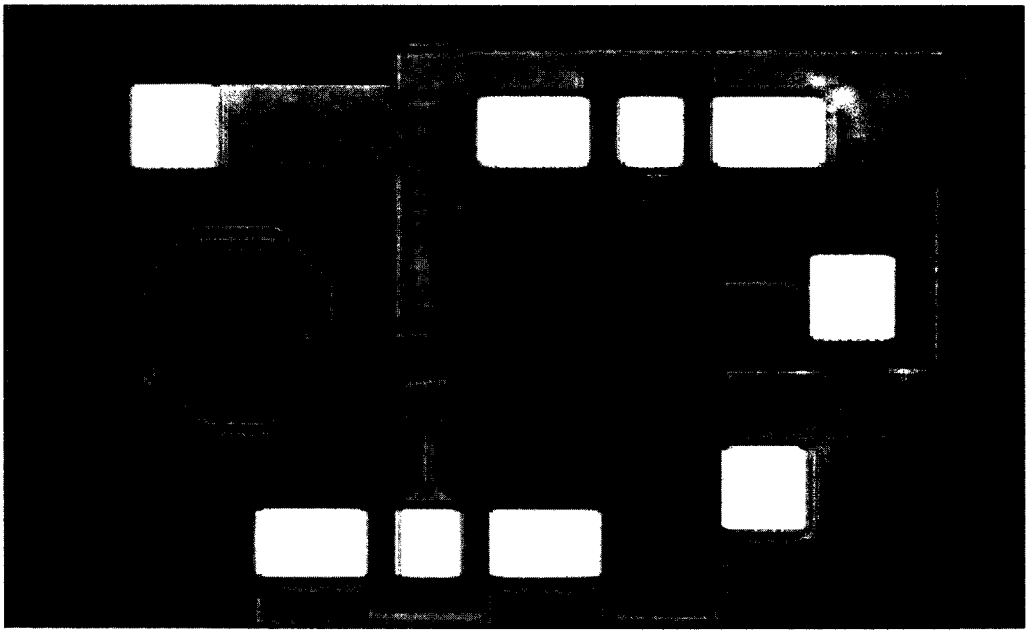


Figure 5-2 Chip microphotograph of gm-boosted CGLNA with transformer

The LNA has been tested using on-wafer probing with an *Agilent* E8364A PNA used for s-parameter measurements as depicted in Figure 5-3. Before measuring the s-parameters of the LNA, a short-open-load-through (SOLT) calibration was performed to remove errors caused by reflections and losses in the cables and adapters.

The measured s-parameters are plotted in Figure 5-4. As can be seen, S_{11} is less than -10dB from 4GHz to 7GHz, which validates the broadband input matching provided by the common-gate configuration. S_{21} is 9.4dB with its peak at 5.8GHz, S_{22} is -14.8dB, and S_{12} is -30.3dB.

As mentioned earlier, the transformer is modeled using *ASITIC*. Since no detailed process information about the substrate was known at the time of the design, which is critical for electromagnetic simulation [51][52], the transformer circuit model is extracted based on information from the inductor models that were already known. However, the first-order estimation led to inaccuracies in the transformer circuit model, as expected. Thanks to the wideband input matching of the common-gate configuration, however, S_{11} remains less than -10dB over the frequency range from 4GHz to 7GHz, which demonstrates that the common-gate amplifier can tolerate process, voltage, and temperature variations as well as modeling errors. Compared to a common-source amplifier, CGLNA is more robust for input matching.

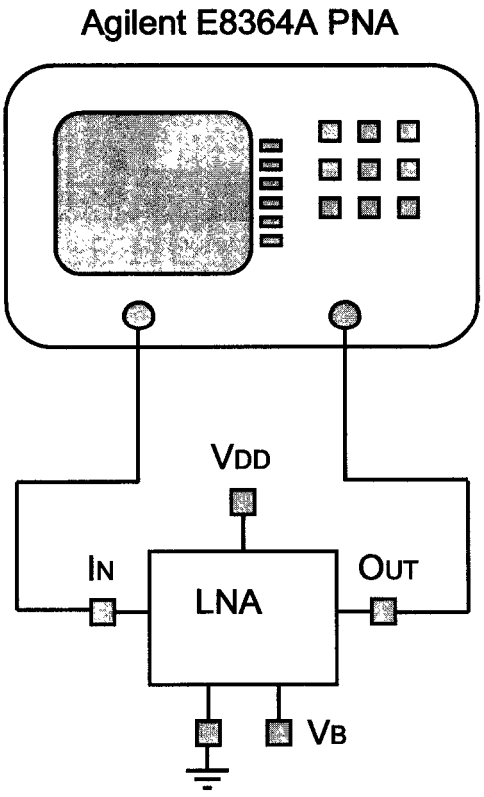


Figure 5-3 Test setup to measure the S-parameters of the Gm-boosted CGLNA with transformer

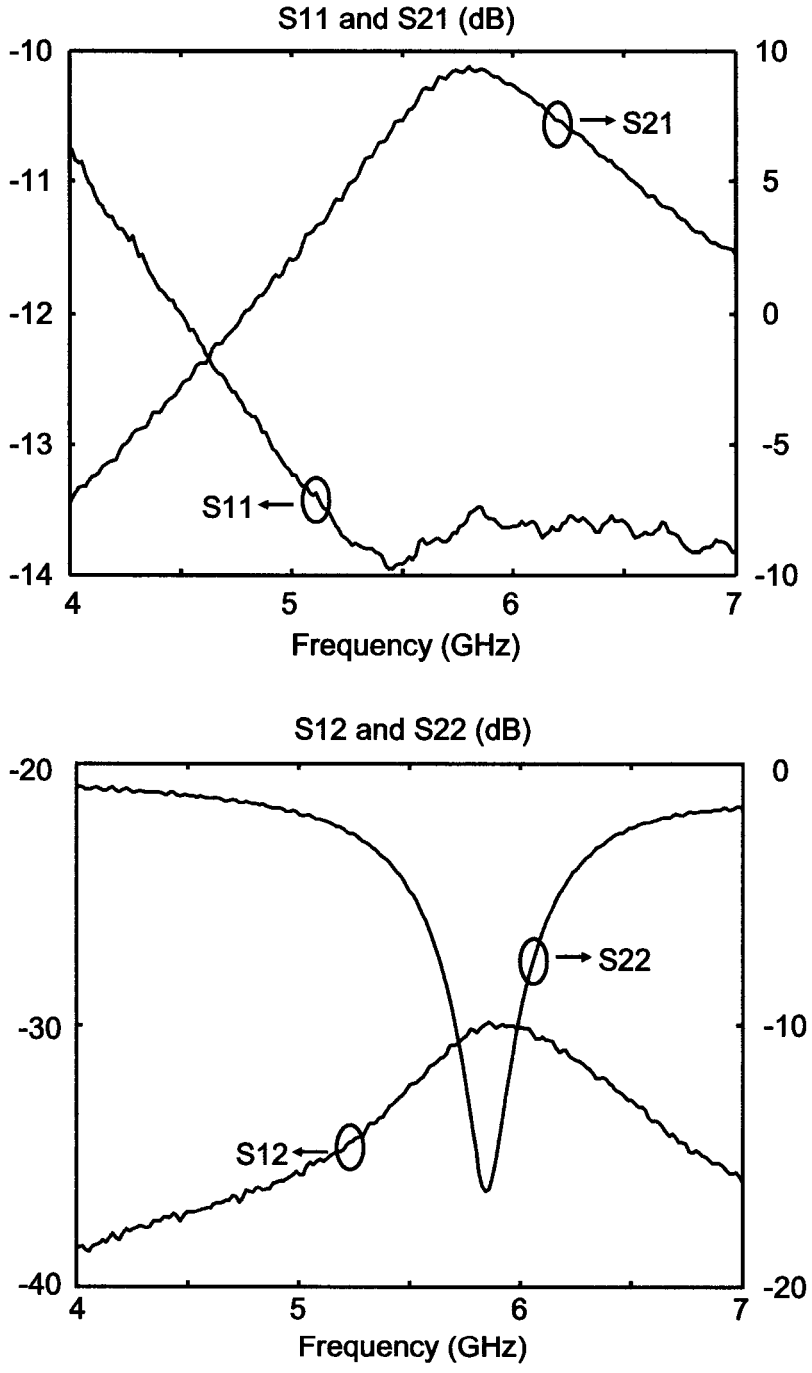


Figure 5-4 Measured S-parameters of the Gm-boosted CGLNA with on-chip transformer

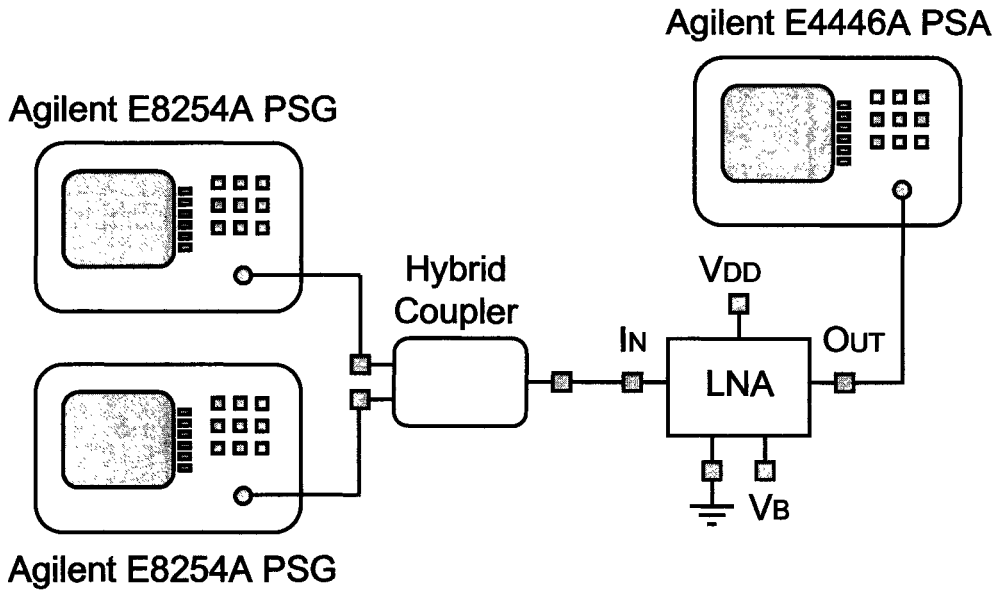


Figure 5-5 Testing setup for measuring IIP3 of the Gm-boosted CGLNA with transformer

The input-referred third-order intercept point (*IIP3*) is measured using the two-tone test as illustrated in Figure 5-5. Two *Agilent* E8254A Programmable Signal Generators generate the required two tones at f_1=5.8GHz and f_2=5.805GHz, which are combined with a hybrid coupler and injected into the input of LNA. The output of LNA is fed into an *Agilent* E4446A spectrum analyzer to perform spectral analysis after the losses associated with the cabling is calibrated out. Figure 5-6 shows the measured spectrum resulting from the two-tone test with P_{in} = −20dBm. The loss from the hybrid coupler, cables, and probing is measured to be 10.3dB. The output power at the fundamental frequency is -20.5dBm. Therefore, the power gain of the LNA is

$$\begin{aligned} A_P &= -20.5dBm - (-20dBm) + 10.3dB \\ &= 9.8dB \end{aligned}$$

The IM3 frequency components appear at $2f_1-f_2$= 5.795GHz and $2f_2-f_1$= 5.81GHz and are evident in the measured spectrum (Figure 5-6).

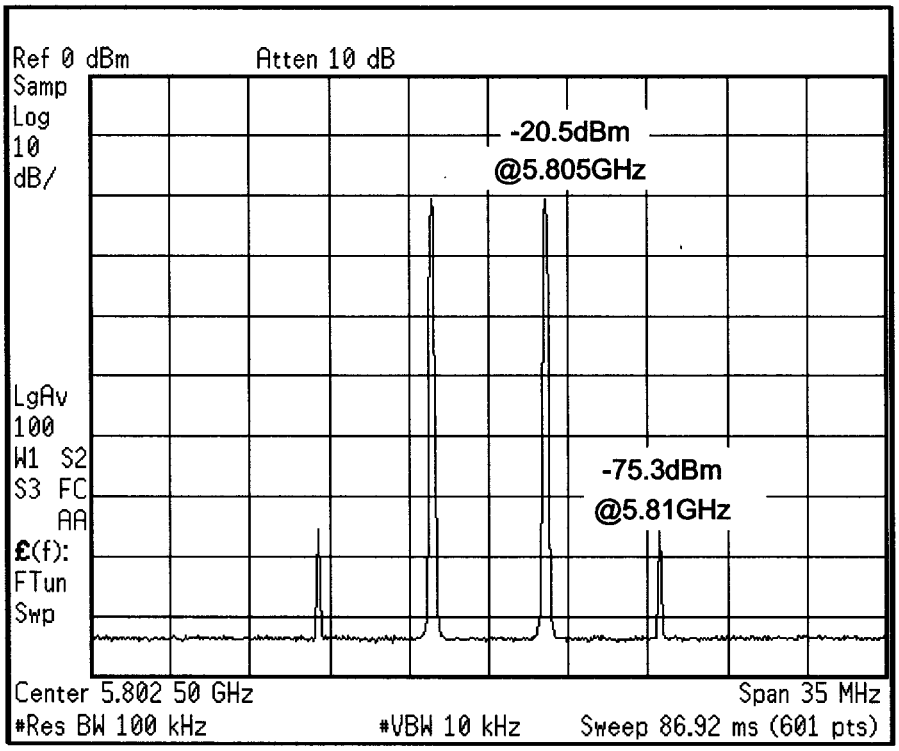


Figure 5-6 Measured spectrum of a two-tone test for the Gm-boosted CGLNA with transformer (f_1=5.8GHz, f_2=5.805GHz, Pin=-20dBm)

The input power P_{in} is swept from -24dBm to 0dBm with steps of 1dBm. Figure 5-7 shows the output power vs. input power for both the fundamental frequency and the third-order intermodulation components; an input-referred third-order intercept point (*IIP3*) of 7.6dBm and an *OIP3* of 17.4dBm are indicated.

The noise figure is measured using an *Agilent* N8975A noise figure analyzer (NFA) and N4002A smart noise source (SNS), as depicted in Figure 5-8. The measured noise figure is plotted in Figure 5-9.

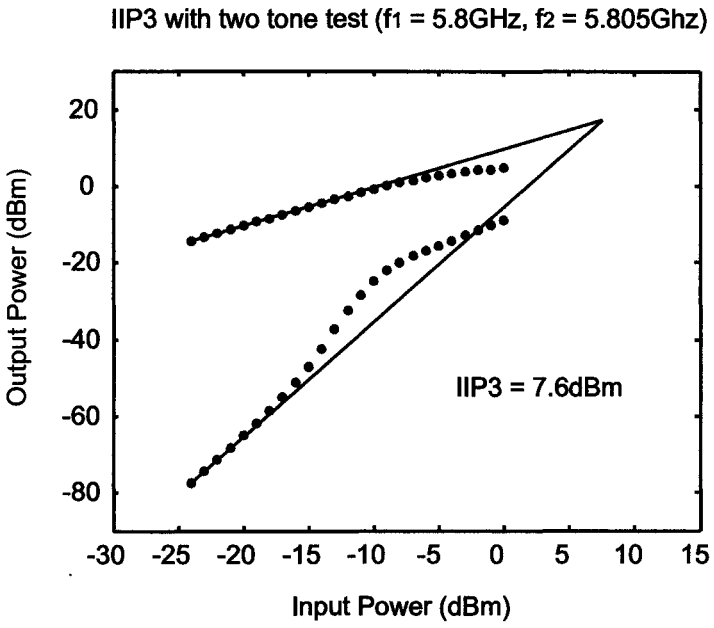


Figure 5-7 Measured IIP3 of the Gm-boosted CGLNA with transformer

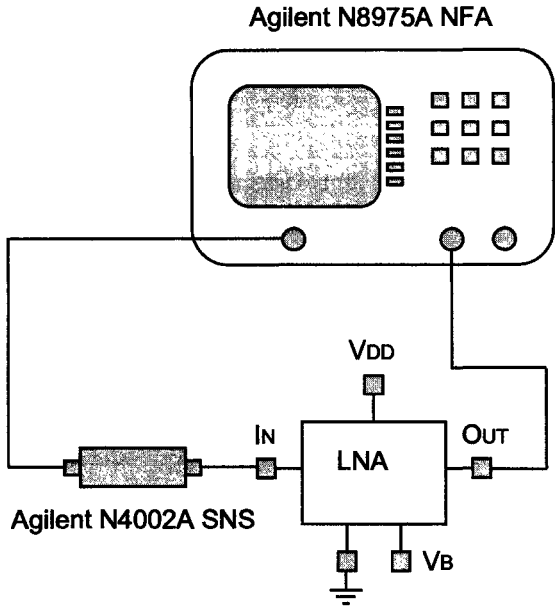


Figure 5-8 Testing setup for measuring noise figure of the Gm-boosted CGLNA with transformer

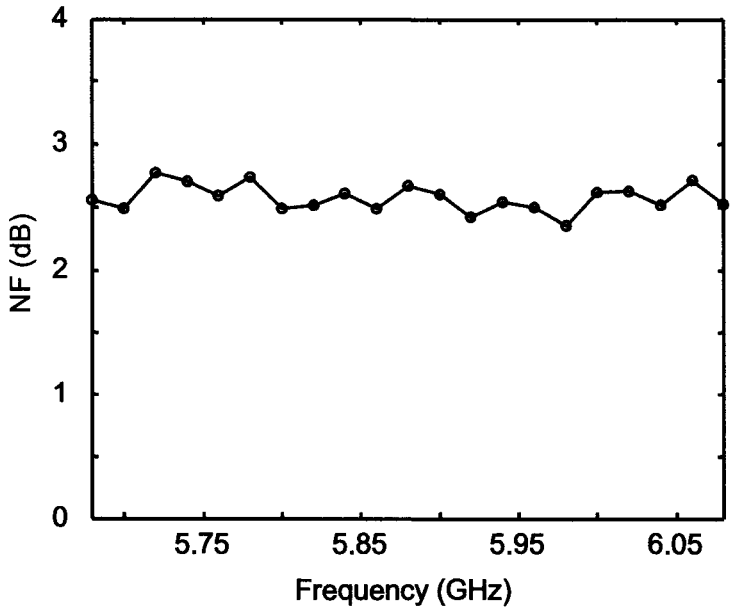


Figure 5-9 Measured noise figure of the Gm-boosted CGLNA with transformer

Table 5-1 Measured LNA Performance Summary

Technology	0.18μm CMOS	
Power Supply	1.8V	
DC Current	1.9mA	
Operating Frequency	5.8GHz	
S-parameters	S11	-13.5dB
	S21	+9.4dB
	S12	-30.3dB
	S22	-14.8dB
Noise Figure	2.5dB	
IIP3	7.6dBm	
Die Area	910μm × 670μm	

Table 5-1 summarizes the measured performance of gm-boosted CGLNA with transformer.

5.2 A Differential Colpitts VCO

Figure 5-10 depicts a differential Colpitts voltage-controlled oscillator with simplified bias circuitry. To deliver sufficient power into the 50Ω input of the spectrum analyzer, an output buffer consisting of differential pair M_3 and M_4 is added. In this design, the sources of M_1 and M_2 drive the buffer rather than the drains of M_1 and M_2 because isolating the buffer from the LC tank prevents it from directly loading the *LC* tank. The tuning range is also maintained with the addition of the buffer stage. Simulations show that even with a relatively low power supply voltage of $1.8V$, the voltage swings at nodes *A* and *B* are sufficient to fully switch M_3 and M_4, and therefore completely steer the tail current to the 50Ω output load.

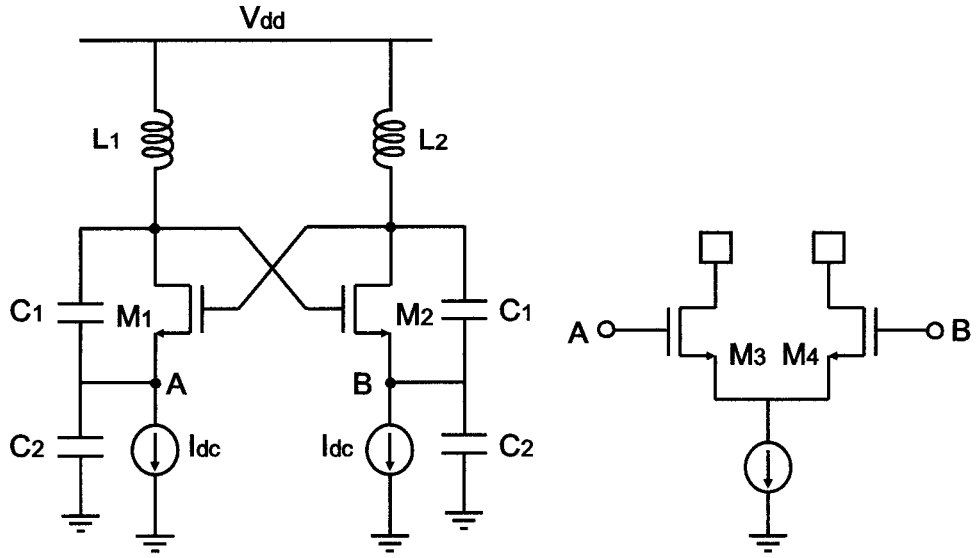


Figure 5-10 A differential Colpitts VCO

The differential Colpitts VCO has also been laid out and fabricated using the IBM 0.18μm 7RF CMOS process available through MOSIS. Exceptional care was paid in the layout to maintain symmetry to avoid undesired flicker noise up-conversion [53][54]. The sizing of the transistors is also critical in achieving good phase noise performance. More specifically, the length of the tail current transistor is chosen as non-minimum to suppress channel-length modulation effects; flicker noise from the tail current source is also reduced due to the larger gate area. The sizing of the switching transistors involves a compromise between tuning range and phase noise, which required several design and optimization iterations to arrive at an optimal tradeoff.

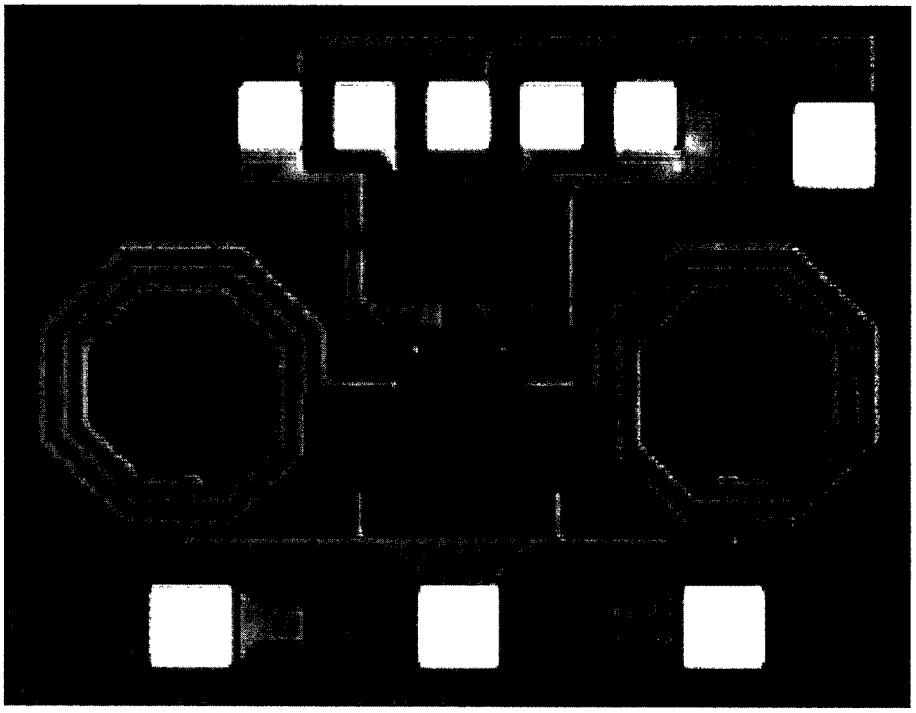


Figure 5-11 Chip microphotograph of the differential Colpitts VCO

A chip microphotograph of the Colpitts VCO is shown in Figure 5-11; it consumes an area of 970μm × 710μm including the probe pads. Phase noise of the differential

Colpitts VCO is measured using an *Agilent* E4446A spectrum analyzer with a phase noise personality. Since an open-drain differential pair is used as an output buffer, two bias tees are required to bias the buffer stage properly. As depicted in Figure 5-12, one of the outputs is fed into the spectrum analyzer and the other is loaded with an accurate 50Ω termination.

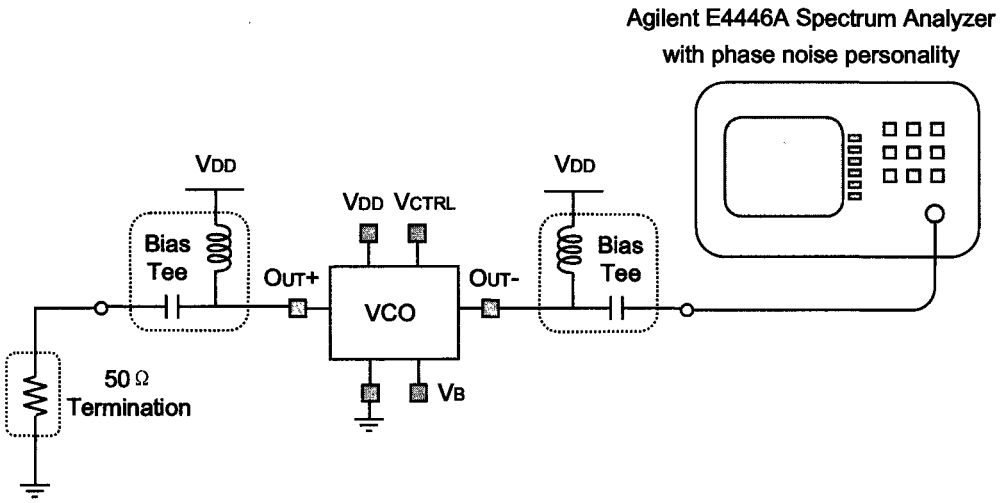


Figure 5-12 Testing setup for the differential Colpitts VCO

Figure 5-13 shows the measured output spectrum of the Colpitts VCO under a bias current of 3.6mA. The output power is -11.8dBm and is lower than expected from simulations. This is caused by losses associated with the cabling and a 3dB loss associated with the test setup.

To measure the tuning curve, the control voltage applied to the varactor is varied from 1.2V to 2.7V with steps of 0.1V. The measured tuning curve is shown in Figure 5-14, along with the simulated tuning curve. It can be seen that the measured tuning curve is linear in the vicinity of 2.0V and is in good agreement with simulation results.

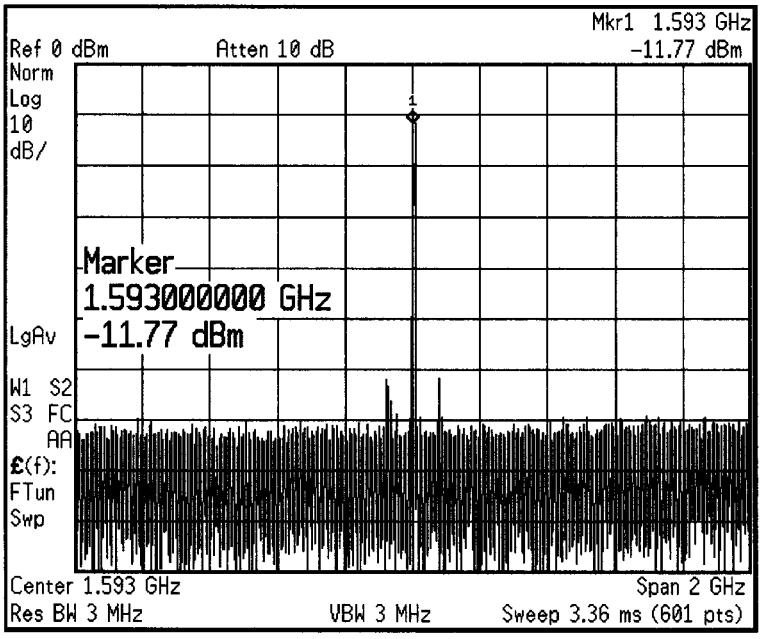


Figure 5-13 Output Spectrum of the differential Colpitts VCO with a bias current of 3.6mA and a 2.0V power supply

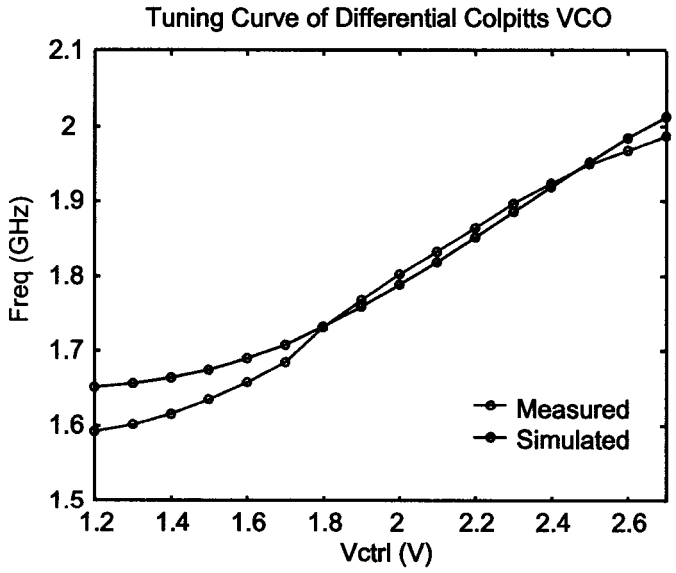


Figure 5-14 Tuning curve of differential Colpitts VCO

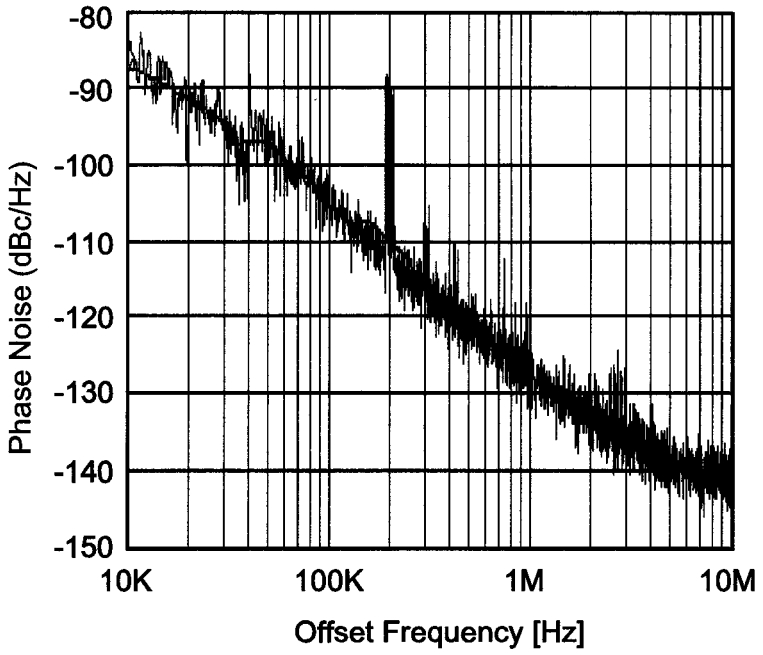


Figure 5-15 Measured phase noise of differential Colpitts VCO

Table 5-2 Measured VCO Performance Summary

Technology	0.18μm CMOS		
Power Supply	2.0V		
DC Current	3.6mA		
Frequency	1.59GHz ~ 1.98GHz		
Tuning Range	22%		
Phase Noise	Offset frequency	Phase noise	FOM
	@10KHz	-87.7dBc/Hz	183.2dB
	@100KHz	-105.8dBc/Hz	181.3dB
	@600KHz	-122.9dBc/Hz	182.8dB
	@1MHz	-128.0dBc/Hz	183.5dB
Die Area	970μm × 710μm		

The measured phase noise is shown in Figure 5-15. With a total output power of about -12dBm and a noise floor of -154dBm, the phase noise measurement floor is limited to -144dBc/Hz. Calibration is performed to subtract out the noise floor of spectrum analyzer. However, the measurement at higher offset frequencies is still not perfectly accurate as the measurement noise floor is approached. It is believed that phase noise at greater than 3MHz offset frequencies is unreliable in the measurement. Being well above the noise floor, however, measurements at less than 1MHz offset frequencies are accurate. The VCO achieves a measured phase noise performance of -128.0dBc/Hz at 1MHz offset frequency. Table 5-2 summarizes the performance of the VCO.

5.3 A Quadrature Colpitts VCO

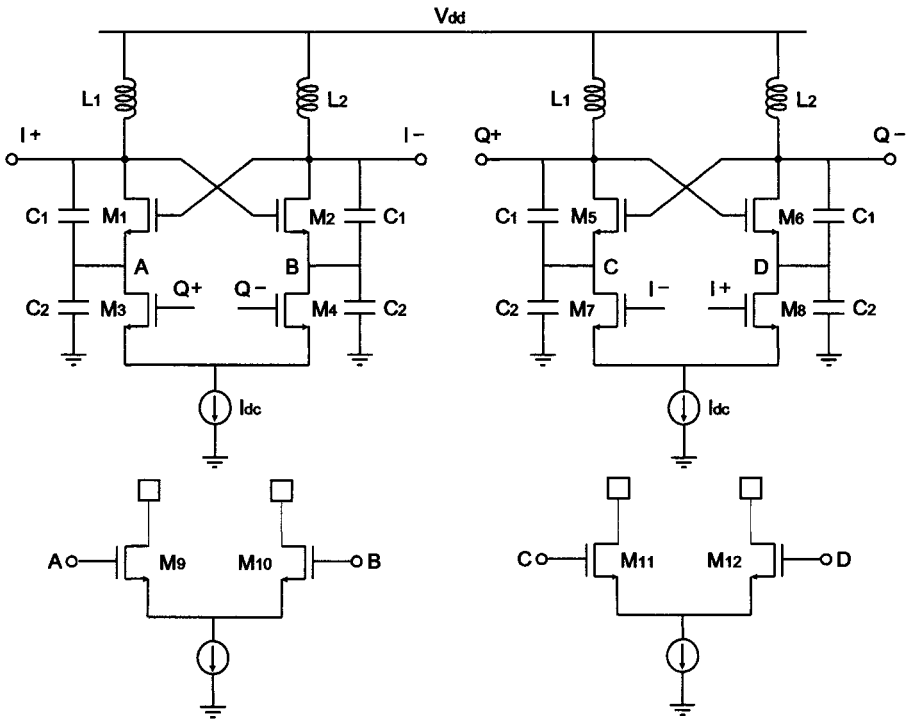


Figure 5-16 Colpitts Quadrature VCO

A circuit diagram of the implemented quadrature Colpitts VCO is shown in Figure 5-16. Open-drain buffer stages similar to those used in the differential Colpitts VCO are also used in the implementation.

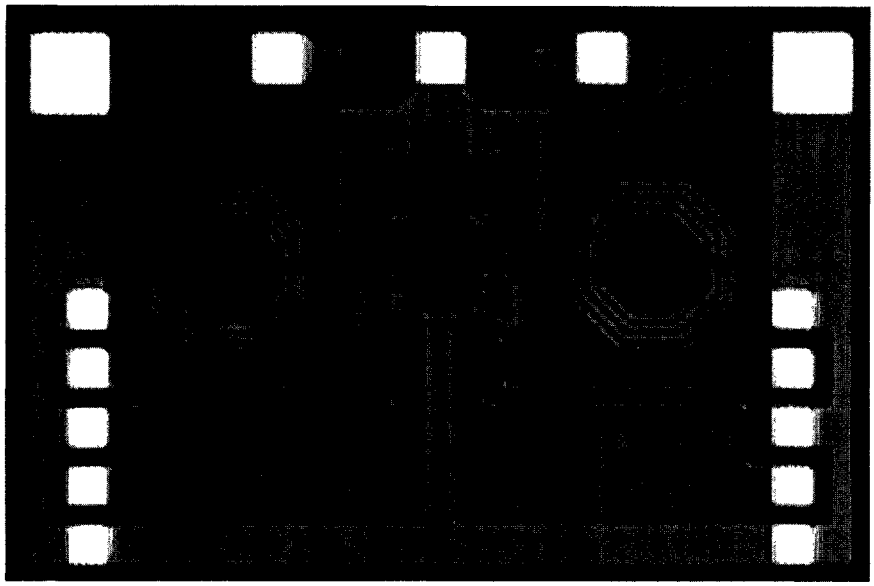


Figure 5-17 Chip microphotograph of Colpitts quadrature VCO

Chip microphotograph of the quadrature Colpitts VCO is shown in Figure 5-17; it consumes an area of 1450μm × 940μm including the probe pads.

Figure 5-18 shows the measured output spectrum of the QVCO with a bias current of 4.3mA and a power supply of 2.0V. The QVCO oscillates at 1.83GHz with an output power of -18.2dBm when a DC voltage of 1.2V is applied at the control voltage of the varactor. The measured tuning curve is plotted in Figure 5-19 showing a tuning range of 20%. It can be seen that oscillation frequency is higher than simulated. This is mainly due to the inaccuracies of transformer modeling with the inductance apparently overestimated. The tuning curve of the QVCO is quite linear, however, which suggests its suitability for frequency synthesis applications.

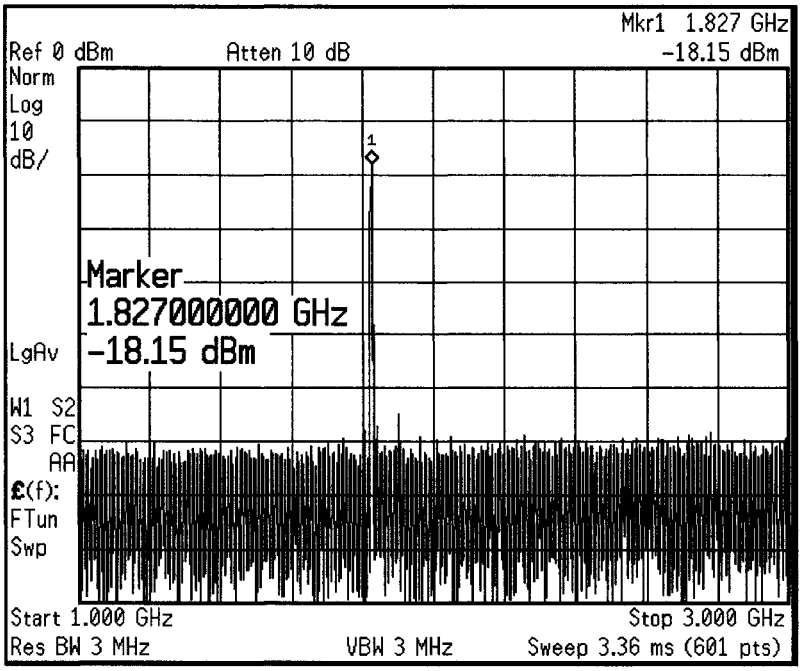


Figure 5-18 Output Spectrum of Colpitts quadrature VCO with a bias current of 4.3mA and a 2.0V power supply voltage

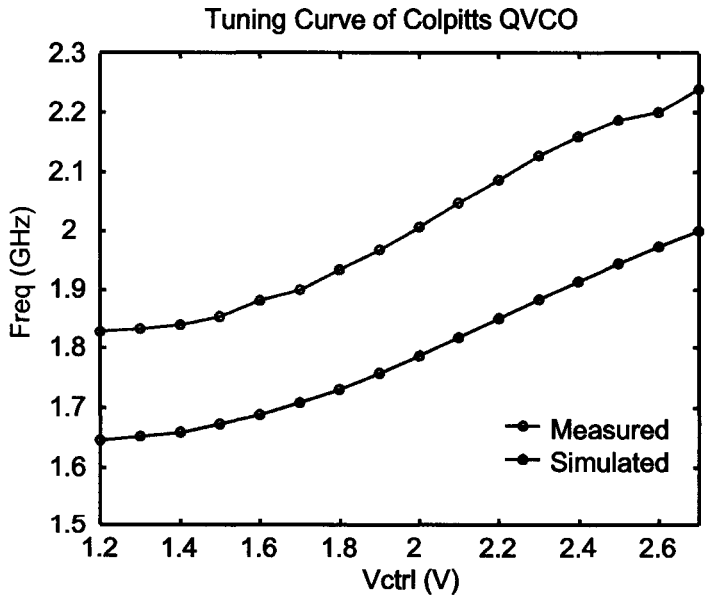


Figure 5-19 Tuning curve of the Colpitts quadrature VCO

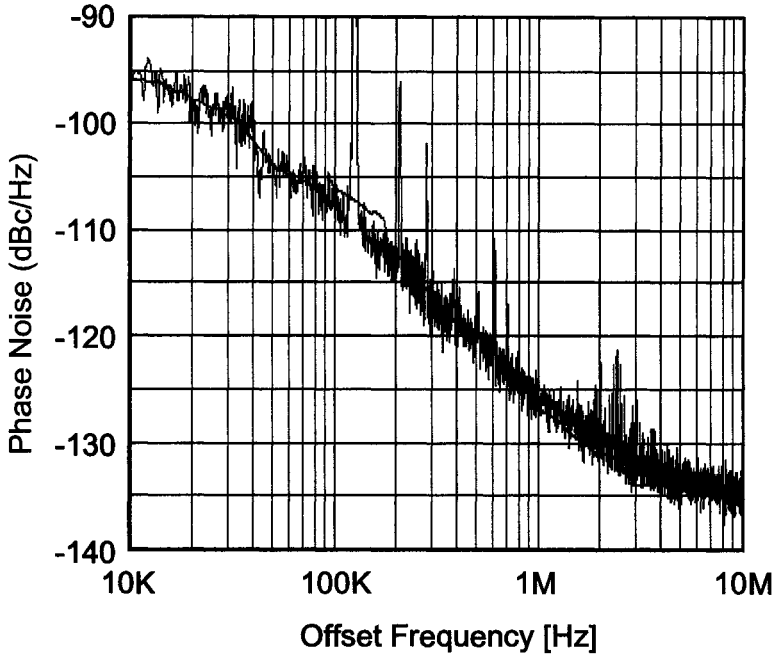


Figure 5-20 Measured phase noise of the Colpitts quadrature VCO

Table 5-3 Measured QVCO Performance Summary

Technology	0.18μm CMOS		
Power Supply	2.0V		
DC Current	4.3mA		
Frequency	1.83GHz ~ 2.24GHz		
Tuning Range	20%		
Phase Noise	Offset frequency	Phase noise	FOM
	@10KHz	-95.9dBc/Hz	191.8dB
	@100KHz	-106.3dBc/Hz	182.2dB
	@600KHz	-121.4dBc/Hz	181.7dB
	@1MHz	-127.0dBc/Hz	182.9dB
Die Area	1450μm × 940μm		

The measured phase noise is plotted in Figure 5-20 at the conditions of 4.3mA DC bias current and 2.0V power supply voltage. The measured phase noise at 1MHz offset frequency is -127.0dBc/Hz. Table 5-3 summarizes the measured performance of the quadrature Colpitts VCO.

5.4 Summary

In this Chapter, implementations of the gm-boosted CGLNA using an on-chip transformer, a Colpitts differential VCO, and a quadrature VCO are described. Measured performance is presented for each.

Relatively broadband input matching is achieved even with inaccuracy in transformer modeling in the CGLNA, confirming the theoretical analysis in Chapter 3. The measured S_{21} value of 9.4dB at 5.8GHz is close to the expected result from simulations. The LNA achieves an IIP3 of 7.6dBm and a noise figure of 2.5dB.

Both the VCO and QVCO are tested using an *Agilent* E4446A spectrum analyzer with phase noise personality. The measured tuning curve of the VCO is close to simulation values whereas that of QVCO is shifted due to some inaccuracy in the transformer modeling. The VCO achieves a tuning range of 22% and phase noise of -128.0dBc/Hz @1MHz while the QVCO has tuning range of 20% and phase noise of -127.0dBc/Hz @1MHz.

Chapter 6 : Conclusions

Loosely speaking, noise is an "unwanted signal" that accompanies the desired signal that needs to be detected. In nature it is random and ubiquitous in electronics. It often sets the lower end of the dynamic range of a receiver, that is, its sensitivity. Low-noise circuit design is one of the most challenging tasks in RF IC design. This dissertation addresses low-noise design techniques for low-noise amplifiers and voltage-controlled oscillators, which are critical building blocks in integrated receivers from the perspective of noise.

The main contributions of this work include introducing a novel gm-boosted CGLNA, which exhibits lower noise figure and consumes less power consumption than a conventional CGLNA. The key point is that instead of connecting the gate terminal to an AC ground, coupling between the source and gate terminals is introduced to enhance the effective transconductance, which lowers the noise figure. Due to the low quality factor of the input matching circuit, the gm-boosted CGLNA has more robust input matching compared to the CSLNA. It is also shown that the proposed gm-boosted CGLNA is more suitable for emerging high frequency applications.

A novel differential Colpitts VCO is also introduced. Its differential operation not only provides differential outputs that are advantageous in modern IC implementations in suppressing even-order distortion products, it also enables faster commutation, which results in better suppression of noise. The easier start-up saves DC power consumption required to guarantee oscillation. Finally, a quadrature VCO based on the differential Colpitts configuration is described.

Interesting enough, although the LNA and VCO are two different circuits, they share some similarities, and the gm-boosted mechanism is applied to both in this thesis. The former leads to a gm-boosted CGLNA and the latter results in a differential Colpitts VCO. Of course, the differences between the LNA and VCO implementations are obvious; in the LNA it is the enhancement of the small-signal effective transconductance that improves performance while in the VCO, faster commutation of the switches in a large-signal mode of operation lowers the phase noise.

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