Development of Fabrication Process for Twisted Rhombohedral Trilayer-Bilayer Graphene Transport Devices

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Abstract

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This work presents the development and refinement of a fabrication methodology for twisted rhombohedral trilayer-bilayer graphene (tRTBG) transport devices. The tRTBG system is predicted to host flat electronic bands with high Chern numbers at twist angles of 1.1°~1.4°, promoting highly correlated, potentially fractionalized topological phases. This methodology covers parameters for exfoliation, identification, isolation, and stacking of graphene and hexagonal Boron Nitride flakes into van der Waals heterostructures via AFM and polymer-based dry transfer techniques, as well as modified PC/PDMS transfer slide properties. The resulting heterostructures are patterned into devices using electron-beam lithography, reactive ion etching, and Cr/Au metal evaporation. We find that increased O_2 plasma cleaning and baking times of SiO_2 wafers prior to and during exfoliation promotes the generation of large, pristine flakes with regions of both bilayer and trilayer graphene. Four devices were successfully fabricated using this methodology, and initial 4K transport measurements confirm functional operation and reveal features consistent with the predicted tRTBG band structure, including a displacement field-dependent band gap at $\nu = 0$ and a resistive bump within the range $0 < \nu < 1$, suggestive of emergent states at millikelvin temperatures. This methodology provides a reproducible route for the fabrication of tRTBG devices and establishes the foundation for future work aimed at more thorough characterization of the underlying physics of this system.

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Acknowledgements

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Last but not least I would like to thank Remi, who is always a reliable source of chaos when I feel like things are getting dull.

1. Introduction

Graphene, the two-dimensional analogue of graphite consisting of a single layer of carbon atoms arranged in a hexagonal lattice, first made the jump from a theoretical model to an experimental reality following its isolation by Novoselov and Geim in 2004[1]. Graphene's band structure, comprised of Dirac cones centered at the K & K' points of the hexagonal Brillouin zone, is responsible for its many notable electronic properties[1,2]. Without chemical or electrostatic modifications, graphene behaves as a zero-gap semiconductor due to the lack of available states at the Fermi level. Electrostatic doping occurs through the application of a voltage to a gate, which can be described as a parallel plate capacitor when separated from the graphene by a thin layer of hexagonal Boron nitride (or another dielectric material). Changing the voltage on the gate (one of the parallel plates) without changing the capacitance increases the charge and therefore charge density on a constant area sample. Placing the graphene between two gates effectively adds two of these capacitors together, leading to a charge carrier density described by

$$n = \frac{V_{tg}C_{tg} + V_{bg}C_{bg}}{e}$$

where V_{tg} (V_{bg}) is the applied voltage on the top gate (bottom gate) and C_{tg} (C_{bg}) are the capacitances between the top gate (bottom gate) and the graphene. In addition to changing the charge carrier density, gate voltages are also used to apply electric displacement fields which influence the Fermi level through modifications of the overall band structure[1,3–5]. The charge carriers in graphene were experimentally shown[6–8] to behave as massless Dirac Fermions due to the band dispersion obtained by solving the low-energy Hamiltonian of graphene:

$$H = -t \sum_{i,j} \left(a_i^\dagger b_j + b_j^\dagger a_i \right)$$

where i and j are nearest neighbor sublattice pairs, $a_i^\dagger$ ($b_j^\dagger$) and a_i (b_j) are creation and annihilation operators for sublattice a (sublattice b), and t is the nearest-neighbor hopping energy. Fourier-transforming the creation and annihilation operators, defining $\psi(\vec{k}) = \left(a(\vec{k}), b(\vec{k}) \right)^T$, and plugging them back into the low-energy Hamiltonian results in the form

$$H = -t \sum_{\vec{k}} \psi^\dagger(\vec{k}) h(\vec{k}) \psi(\vec{k})$$

where $h(\vec{k})$ is the Bloch Hamiltonian. Expanding at low energy near the K' point of the Brillouin zone results in the linear dispersion:

$$h\left(\overrightarrow{K'} + \vec{q}\right) = \hbar v_F \vec{q} \cdot \vec{\sigma}$$

where σ is the Pauli matrix vector. This result holds for both the K and K' points, and is similar to the Dirac equation for massless particles, with v_F taking the role of the speed of light[6,9].

Beyond the intrinsic electronic properties of graphene, it has also proved to be a remarkably versatile platform to both study and create novel quantum phenomena. Advances in isolation and fabrication methodologies for 2D material-based devices, namely the now well-known dry transfer technique, have made this possible by increasing the yield and quality of graphene domains and devices made from them (and other 2D crystals such as $MoTe_2$) [1,10–16]. The ability to fabricate high quality devices from such a wide variety of 2D materials provides a direct means to study how electron correlations, symmetry breaking, and topology generate

novel phases of matter, particularly in systems where flat electronic bands enhance the effect of interactions[17–21].

1.1: Electronic Structures and Modifications

The wide range of parameters that affect graphene's electronic properties, including but not limited to layer number, stacking order, and twist angle between layers, adds to its usefulness as a tool to study novel physics[22–24]. Increasing the number of graphene layers causes the addition of extra bands, which hybridize to form far more complex structures than are seen in monolayer graphene. For example, bilayer graphene has bands which are parabolic rather than linear and an additional set of dispersive bands above and below the parabolic conduction and valence bands, and trilayer graphene has yet another set of bands added on top of the bilayer structure[2,25]. Further increasing the layer number continues to increase the number of bands present, causing increasingly metallic behavior until the bulk limit is reached at ~10 layers[26,27]. These stacks of graphene layers are most commonly arranged in the thermodynamically stable ABA, or Bernal, stacking order. However, they are occasionally found to be in the metastable ABC (rhombohedral) stacking order when there are at least 3 layers present. Figure 1 summarizes these structural and electronic properties, as well as those discussed in subsequent paragraphs.

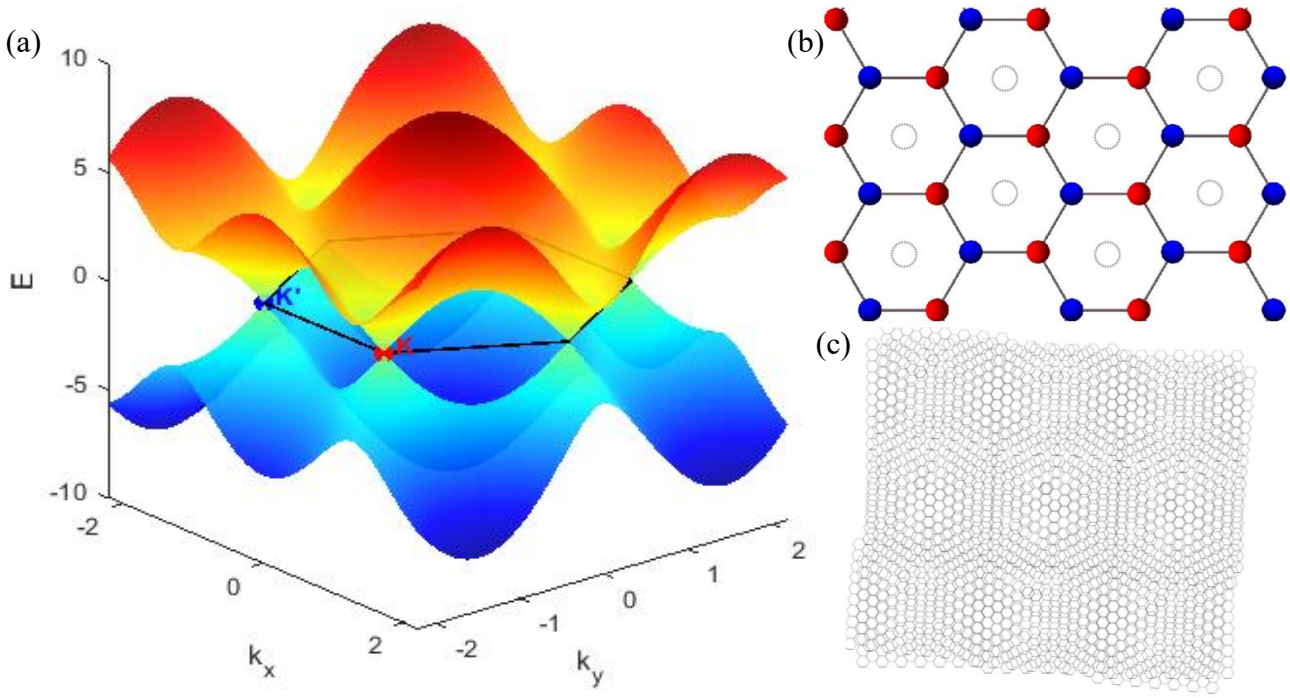

Figure 1: (a) Band structure in the first Brillouin zone of graphene calculated from tight-binding models. The hexagonal Brillouin zone and inequivalent K and K' valleys are marked. (b) Honeycomb structure of graphene showing A, B, and C stacking sites in blue, red, and white respectively. (c) Moiré pattern created by overlaying two graphene lattices with a relative twist angle.

The rhombohedral stacking order of bulk graphite has been known for many decades[28–30]; however, it took until the explosion of graphene research in the 2010s for rhombohedral-stacked few-layer graphene (FLG) transport properties to be studied in depth[31–33]. Rhombohedral FLG is particularly interesting due to the presence of flat electronic bands which are easily accessible via electrostatic doping[32,34,35], and whose dispersion ε_p is (to a lowest order approximation) given by the relation $\varepsilon_k = k^N$ where N is the number of layers[32,36–38]. Furthermore, in contrast to Bernal FLG's electrostatically tunable band overlap the application of an electric field to rhombohedral FLG opens a gap near the Fermi level while retaining the bands' characteristic flat dispersion (Figure 2)[39–42]. The robustness of the flat bands across many different layer numbers and values of electric field is extremely valuable, as it provides the ability to study a wide range of correlated and topological states across a variety of sample morphologies[20,35,40,43–45].

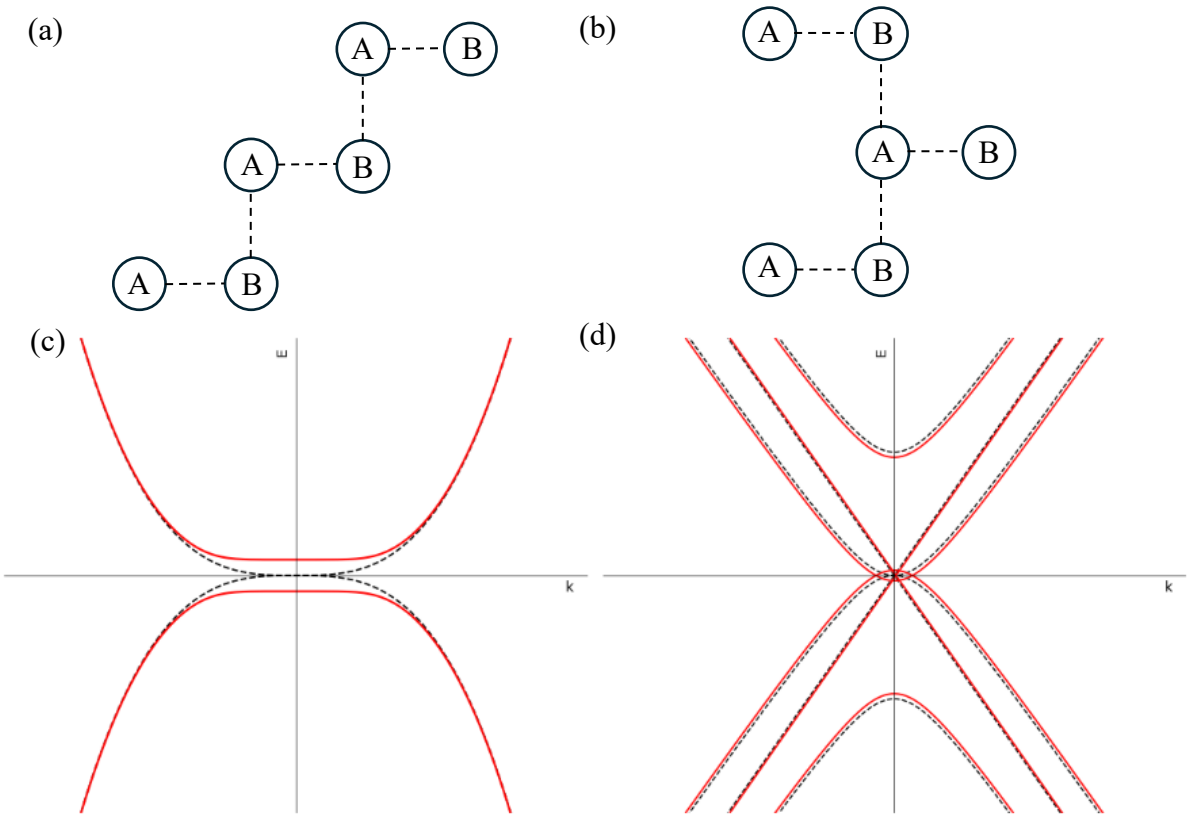

Figure 2: (a), (b) Side view diagram of the rhombohedral and Bernal stacking order, respectively, with A and B sublattice atoms denoted. (c), (d) Band structure of rhombohedral (c) and Bernal (d) trilayer graphene both with (red) and without (black) an applied perpendicular electric field.

Similarly, the long-range interference, or Moiré, patterns that are seen when layers have a relative twist angle between them were first observed many years ago on the surface of bulk graphite[46], but were not seen as much besides a novelty until they were created in few-layer graphene systems[23,47–49]. The Moiré superlattice hosts highly tunable electronic bands, including those with flat dispersion which promotes highly correlated electronic states such as unconventional superconductivity and Chern insulators[17,50–52]. A notable Moiré system as well as the progenitor of this subfield of 2D material-based research is the so-called "magic angle" twisted bilayer graphene (MATBG) system, consisting of two monolayer graphene sheets with a twist angle of 1.1° between them[47]. The discovery of electrostatically tunable flat bands and correlated electron states in MATBG gave rise to an entire field of study focused on the

properties of twisted two-dimensional materials including graphene, hBN, transition metal dichalcogenides (TMDs), and combinations thereof[52–57].

1.2: Probing Electronic States via Transport Measurements

Measurement of electronic transport properties, i.e. how electrons flow through a material, can offer insight into fascinating and oftentimes wholly exotic phases of matter. Transport measurements study the behavior of the two-dimensional electron gas (2DEG) as a function of applied electric and magnetic fields, device carrier density, and temperature in order to characterize quantum phenomena, electron correlation effects, and topological properties of materials. Similarly to bulk materials' electronic properties, temperatures near absolute zero, high magnetic fields, or both are most often required to observe the most interesting transport properties. For example, many 2D and bulk materials transition to superconductors at low enough temperature due to the phonon-mediated attractive potential exceeding the strength of Coulomb repulsion, a condition which can only be met at low T when thermal excitations are suppressed. Superconductivity happens to be primarily temperature and material property-dependent, however another phenomenon which incorporates a magnetic field as well as temperature is the quantum Hall effect. In sufficiently high field strengths and sufficiently low temperatures, longitudinal resistivity of a sample ρ_{xx} is exponentially suppressed while transverse resistivity ρ_{xy} approaches quantized values of $\frac{h}{e^2}\frac{1}{\nu}$ [58].

The quantum Hall effect comes in both integer and fractional varieties, so named due to the values which ν takes in the relation $\rho_{xy} = \frac{h}{e^2}\frac{1}{\nu}$, either being an integer or a fraction. In graphene, the integer quantum Hall effect (IQHE) arises from the transformation of the continuous Dirac cone band dispersion to discrete Landau levels in the presence of a magnetic

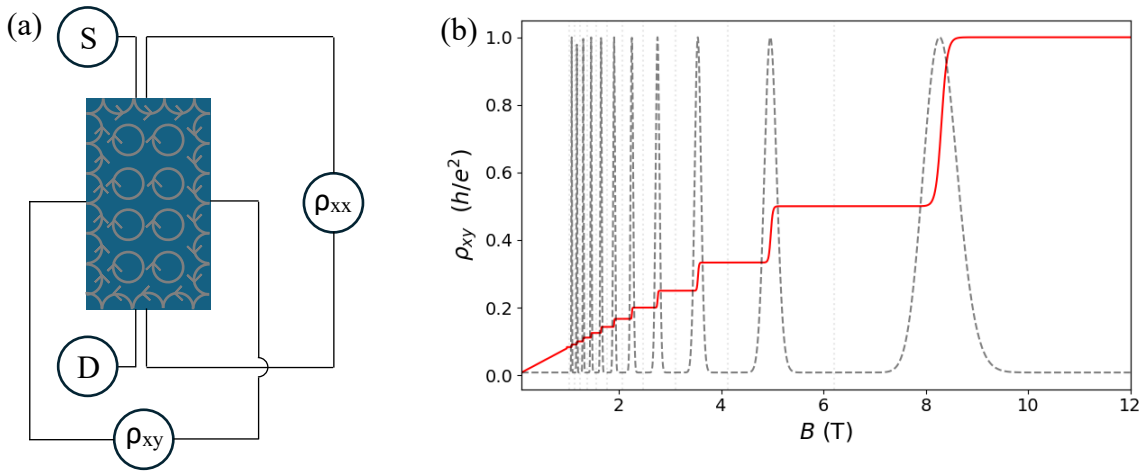

Figure 3: (a) Simplified diagram of the measurement scheme to determine R_{xx} and R_{xy}, also showing the semiclassical electron cyclotron motion and the creation of a chiral edge mode. Current is sourced at one end of a bar-shaped sample (Hall Bar) and drained at the other, and contacts are made to measure voltages in the longitudinal and transverse directions. (b) Plot of a hypothetical ρ_{xy} (red) as a function of applied magnetic field, showing the formation of plateaus consistent with Landau level creation. ρ_{xx} has been added as a grey dotted line at approximate values between plateaus.

field, with ν indicating the index of the highest filled Landau level. As the strength of the magnetic field is increased, the spacing between Landau levels also increases and therefore the width of the resistivity plateau increases before finally reaching a maximum when $\nu = 1$ (Figure 3). Additionally, longitudinal resistivity ρ_{xx} is only finite outside of the Landau levels due to there being no back scattering within the conductive chiral edge mode(s) formed through this process. With no back scattering, there is no voltage change to contribute to resistivity according to Ohm's law V=IR. The voltage instead equilibrates at the contacts which are creating the overall potential difference (the source and drain), and therefore when a measurement is performed in a direction such that those contacts are crossed over a finite resistivity is seen. This concept is illustrated by the Landauer-Buttiker formalism[59,60]:

$$I_{12} = \frac{e^2}{h} T_{12}(V_1 - V_2)$$

where I_{12} is the current across hypothetical contacts 1 and 2 per edge mode, T_{12} is the transmission probability from 1 to 2 ($T_{12} = 1$ in ballistic transport), and V_1 and V_2 are the

voltages of contacts 1 and 2 respectively (equal to the source and drain voltages). The index of the current Landau level ν also indicates the number of edge modes and therefore may replace the transmission probability in the above expression when $T_{12} = 1$. Finally, by assuming that the drain voltage $V_{drain} = V_2 = 0$ and converting to resistance using Ohm's law, the quantized result is given:

$$R_{12} = \frac{h}{e^2}\frac{1}{\nu}$$

On the other hand, the fractional quantum Hall effect (FQHE) is caused by a more complicated electron interaction mechanism. In this mechanism, electrons partially filling Landau levels may be described as coupling to even numbers of magnetic flux vortices (each of which contains magnetic flux $\Phi_0 = \frac{h}{2e}$) to become "composite Fermions" and behave as though they carry only a fraction of the usual electronic charge e[58,61–63]. This effect is seen in Landau levels due to the strength of electron-electron interactions as a result of the bands' perfectly flat dispersion.

There are two other closely related phenomena which may be observed through transport measurements: Chern insulators and the quantum anomalous Hall effect (QAHE). Both states exhibit broken time-reversal symmetry, insulating bulk, and conductive chiral edge channels not as a result of an applied magnetic field as with the QHE (and FQHE), but instead as a result of intrinsic material properties. An important note is that the Chern insulator and the QAHE are in fact not fundamentally different phases; the QAHE is simply the manifestation of a Chern insulator at zero magnetic field. The application of a magnetic field may in fact lead to the formation of Landau levels even in Chern insulators, however this does not negate the fact that

the system is a Chern insulator[18,62,64–66]. The Landau levels formed in this process (or in the QHE) are essentially electronic bands with Chern number C = 1. Additionally, the fractional Chern insulator (FCI) state shows similar behavior to the FQHE in terms of the allowed values of conductance quantization not being restricted to integers. However, the specifics of fractionalization differ between the two. In the FCI, the band which is fractionally filled is crystallographic in origin, whereas in the FQHE the band which is fractionally filled is a Landau level formed by the applied magnetic field. In both cases the fractional filling of a band with a nonzero Chern number leads to fractional quantized conductance.

The Chern number is a core part of the topological origin of many electronic states and arises from a property of the system known as the Berry curvature. The Berry curvature is related to the quantum geometry of the system and may be thought of as an intrinsic magnetic field acting on the charge carriers. Integrating the Berry curvature over the entire first Brillouin zone gives a quantized result designated by $C \in Z$, the so-called Chern number[7,67,68]. Extending this result, Thouless, Kohmoto, Nightingale, and den Nijs showed that the Hall conductivity σ_{xy} of a band is quantized in multiples of $\frac{e^2}{h}$ as given by:

$$\sigma_{xy} = \frac{e^2}{\hbar} \oint_{BZ} \frac{d^2k}{(2\pi)^2} * \Omega_n(k) = \frac{Ce^2}{h}$$

where $\Omega_n(k)$ is the Berry curvature of the band and C is the Chern number[69]. The Chern number of a band has another physical significance in that it is equal to the number of chiral edge modes (Figure 3a). These edge modes arise from the topological properties of the electronic bands in the bulk, an interaction known as the bulk-boundary correspondence, and are dissipationless due to their chiral nature disallowing back-scattering of electrons[65,70,71].

The ability to engineer flat bands in FLG through both stacking order selection and Moiré construction naturally leads to the idea of combining the two. This work is focused on just such a construction, namely a Bernal bilayer stacked atop a rhombohedral trilayer with a small relative twist angle between them, referred to henceforth as Twisted Rhombohedral Trilayer Bilayer Graphene (tRTBG). The tRTBG system is predicted to host a variety of exciting correlated states including Chern insulators with $C > 1$[72,73], many of which have only been observed in select few material systems. We hope that the tRTBG system will offer another avenue by which the underlying physics of these systems can be studied.

1.3: tRTBG & Related Rhombohedral Moiré Systems

Previously studied rhombohedral Moiré systems support the hypothesis that tRTBG will also have interesting and relevant physical properties. For example, twisted double rhombohedral trilayer graphene exhibits bands with $C > 1$ at small twist angles for integer values of band filling factor ν as well as nonzero Chern number bands at larger twist angles and fractional values of ν[74]. Additionally, the twisted monolayer-rhombohedral pentalayer system hosts high Chern number flat bands across a range of twist angles and filling factors[45]. In both cases, the most interesting phenomena occur when the electrons are polarized to the rhombohedral graphene layer furthest away from the Moiré interface, in contrast to the case of twisted M+N Bernal graphene systems which have Moiré interfaces that behave as twisted 1+2 systems[54].

Initial theoretical[73] and experimental[72] work on the tRTBG system indicate the presence of high Chern number flat bands polarized via displacement field to the Moiré distant face of the rhombohedral trilayer at twist angles of 1.1°~1.4°. By partially filling these bands, we hope to uncover further exotic states such as fractional Chern insulators, which have recently been seen

in untwisted rhombohedral graphene aligned to hBN[20,75,76] following their first experimental observation in twisted $MoTe_2$[77–80]. MATBG has also been shown to host states designated as FCIs due to the lattice influence on their physics, however these states required magnetic field strengths of ≥5 T in order to be stable[81,82]. Given the elusiveness of experimental platforms to study low-field FCIs, the possibility of observing these states in tRTBG devices makes the development of a reliable fabrication pipeline for them even more important.

2. Methodology

2.1: Micromechanical Exfoliation & Device Fabrication

Bulk graphite is comprised of many layers of graphene which are held together via weak van Der Waals (vDW) forces, and as a result they are easily separated from each other to form FLG. The method pioneered by Novoselov and Geim in their initial study of graphene[1], known as the "scotch tape method", is still the most common way to perform this separation. Bulk graphite flakes were placed on the sticky side of Scotch tape, which was then repeatedly folded over upon itself and rapidly peeled apart thereby cleaving the graphite into progressively thinner flakes. This method has the advantage of both simplicity as well as creating extremely high uniformity graphite surfaces on the cleaved faces. Once a sufficient area of the tape had been covered by graphite, it was placed in contact with degenerately doped 285 nm SiO_2 which had been cleaned in a 50W O_2 plasma, and gentle pressure with lab tweezers ensured good contact between graphite and substrate. Prior to the removal of the tape from the SiO_2 the assemblies were placed on a hot plate at 100°C to increase the yield of graphene domains. Care was taken during the initial selection of graphite flakes to ensure that they were all of the same thickness as

well as being as flat and smooth as possible. Exfoliation of hBN is similar where a gentle upward pulling is used to peel the tape away over the course of several minutes immediately after applying the tape to the SiO_2 instead of performing the O_2 and hot plate steps. hBN is more brittle than graphite, so the slow removal of the tape was performed so as not to break apart the flakes with the application of a large force.

Both O_2 plasma cleaning and hot plate bake times were modulated to find the best combination of parameters for the generation of flakes with large bilayer and trilayer regions (Figure 4). In order to find the optimal times for each, O_2 plasma cleaning time was varied from 1-5 minutes and bake time was varied from 45 seconds to 3 minutes. Once baking was completed, the tape was rapidly peeled off from the substrate and the surfaces were examined via optical microscopy to identify flakes with regions of both bilayer and trilayer graphene. Both regions must come from the same flake when making twisted graphene devices, as that is the only way to guarantee that both regions start out in the same crystallographic orientation. Each layer of graphene reduces the amount of transmitted light by 2.3%, so a custom Python script was used to analyze the percent transmittance compared to background in order to determine the number of layers in a given region. Near-field IR imaging of trilayer graphene regions was also attempted, however the small size of the stacking order domains as well as the low IR signal

intensity obtained from trilayer graphene made this an impractical route to identify rhombohedral domains.

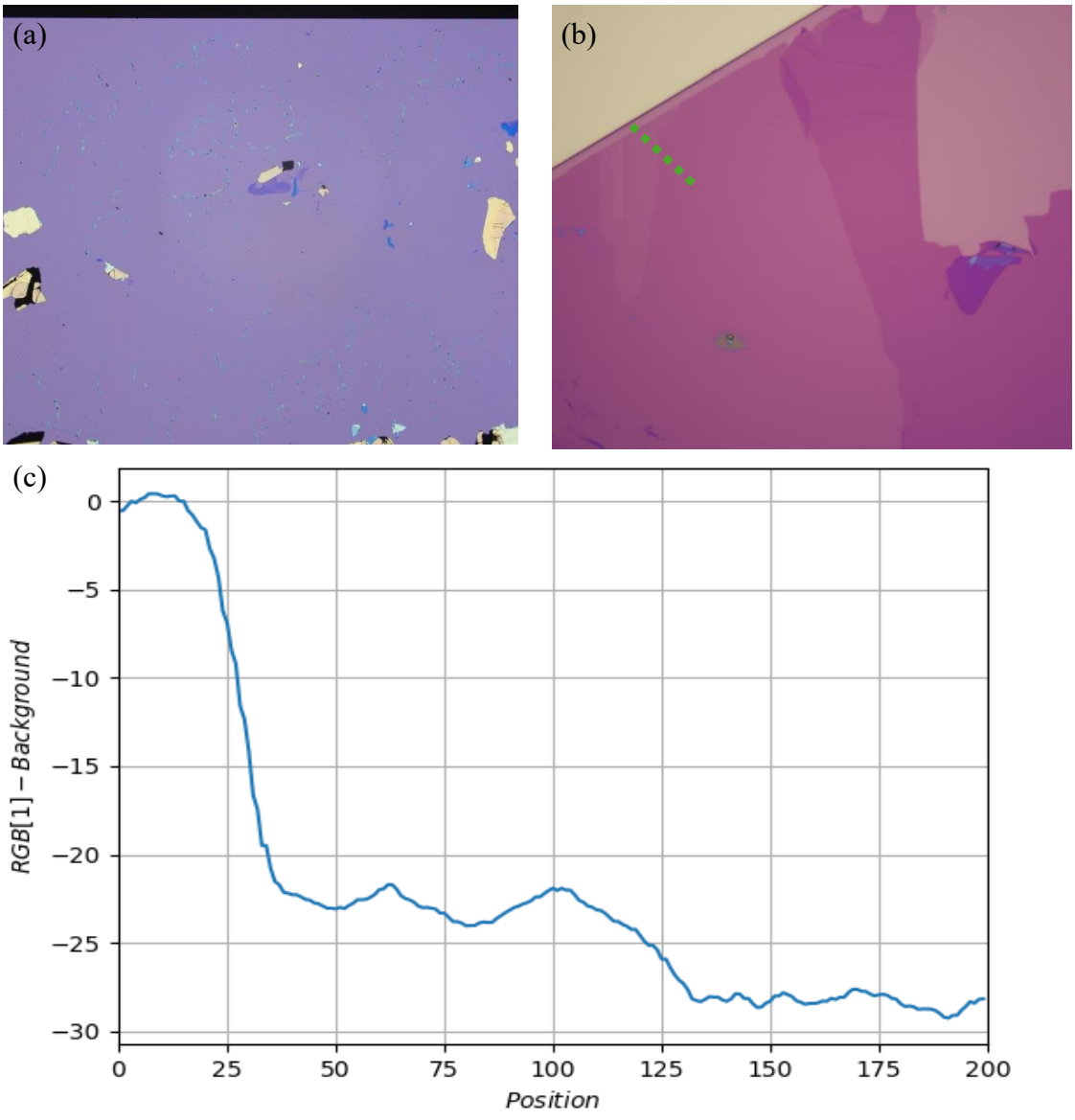

Figure 4: (a) 2x optical micrograph of an exfoliation on SiO_2. (b) 100x optical micrograph of a flake having regions of monolayer, bilayer, trilayer, and tetralayer graphene. (c) Optical contrast graph taken along the green linecut in (b), showing an initial large reduction in transmittance when moving from bare SiO_2 to bilayer graphene, then a smaller transmission reduction when moving from the bilayer to trilayer regions.

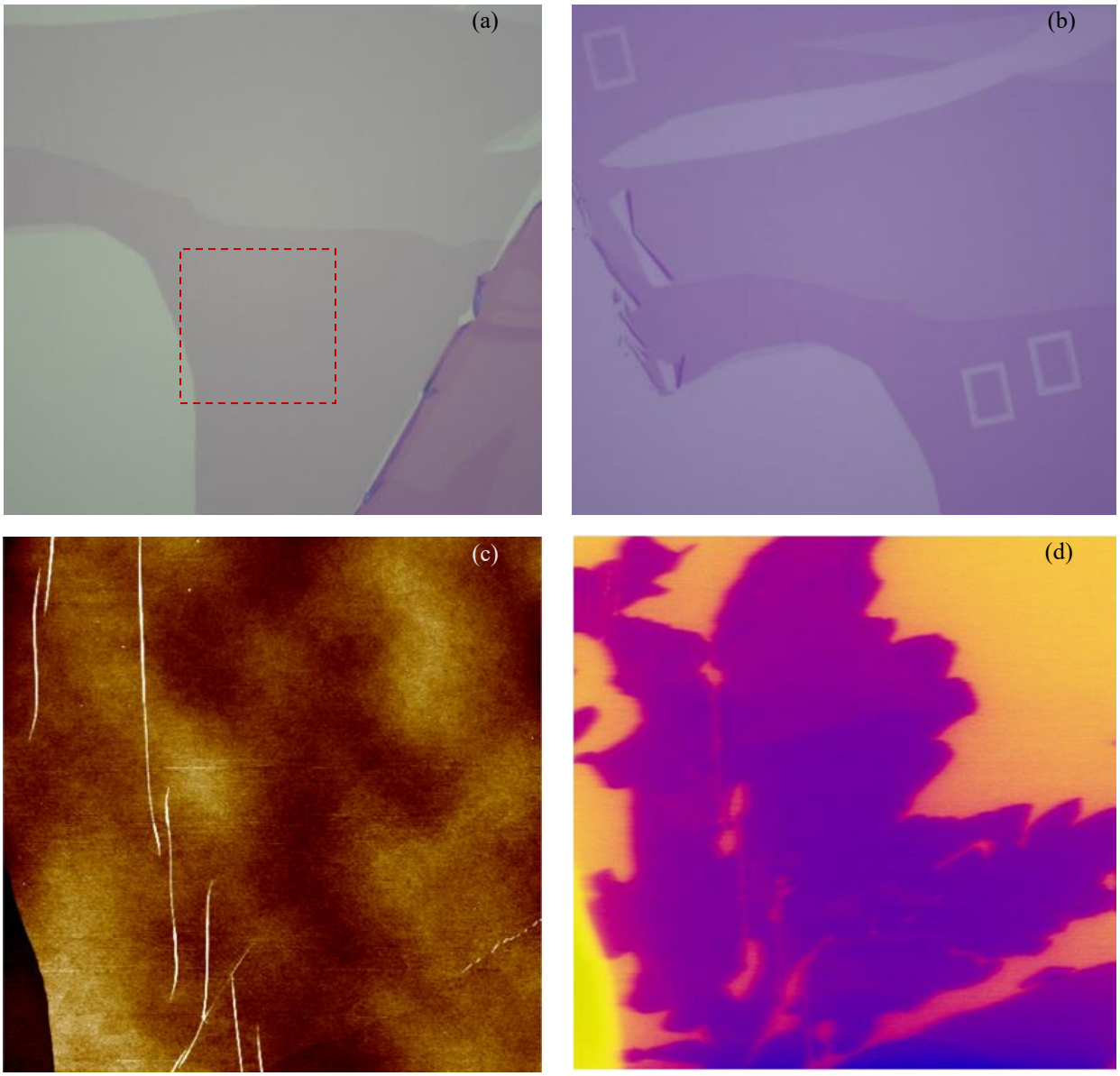

Figure 5: (a), (b), Optical micrographs of a graphene flake having both trilayer and bilayer regions before and after local anodic oxidation respectively. (c) Height scan of the area within the red box in (a) obtained via tapping mode AFM. (d) AM-KPFM data of the region scanned in (c). Yellow regions (except the lower left corner, which is bare SiO_2) are rhombohedral domains and purple regions are Bernal; however, this was unknown at the time leading to making cuts in both areas (b) and distinguishing via Raman spectroscopy. The window size for (c) & (d) was 25 μm, and the vertical scale of (c) was 6.5 nm.

After flakes with the proper layer numbers were identified, Amplitude Modulated Kelvin Probe Force Microscopy (AM-KPFM) was performed using an atomic force microscope (AFM) in order to identify rhombohedral stacking domains in the trilayer regions (Figure 5)[83]. KPFM measures local work function of the surface and often requires the sample to be grounded; however, Bernal and rhombohedral graphene have enough contrast between their work functions

that ungrounded flakes may be scanned and domains of different stacking orders identified using this method. The entire trilayer region must be rhombohedral as any present Bernal domains would encourage relaxation of the flake to become entirely the more stable Bernal stacking order. Therefore, the size of regions used was, on average, roughly 6μm by 8μm. Resist-free local anodic oxidation (LAO) nanolithography was used to isolate rhombohedral trilayer and corresponding bilayer domains[15,84], and Raman spectroscopy was performed on the isolated trilayer regions to confirm rhombohedral stacking order following isolation[85]. The two regions were cut at a relative angle of 1.2°, the target twist angle of the tRTBG devices, and having fringes around the edges such that they would lock together when stacked which would hold the twist angle in place during subsequent fabrication steps.

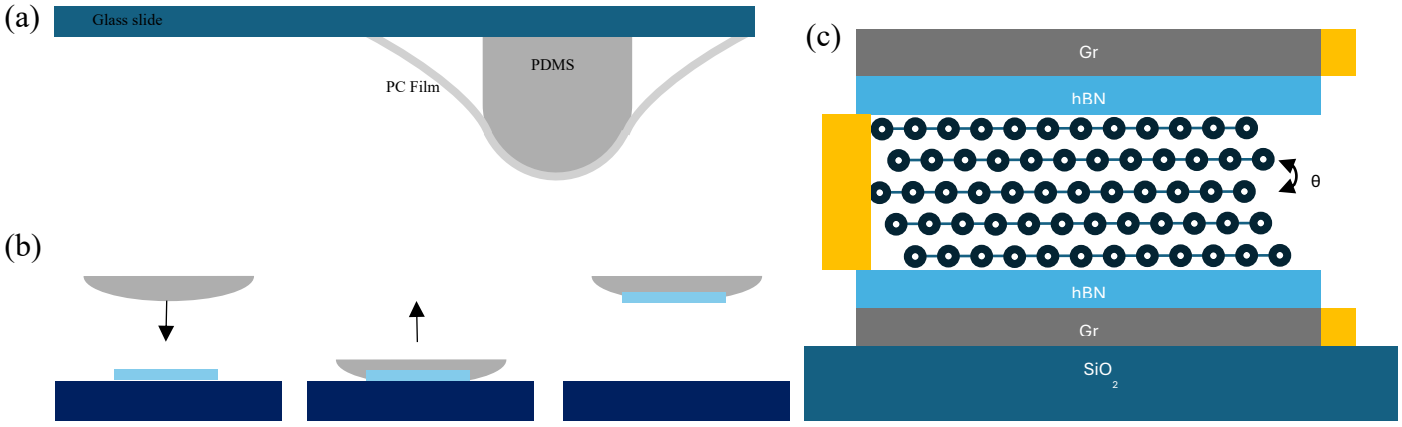

Figure 6: (a) Diagram of a transfer slide. Note that the PDMS dome shown here is more similar in shape to that used in a PCL stamp, and the dome used in a PC transfer slide is far shallower. (b) Process of the PC film of a transfer slide contacting and picking up a flake exfoliated on SiO_2. (c) Side-view schematic of a device, showing tRTBG encapsulated between hBN with graphite top and bottom gates as well as gold contacts to the graphene and both gates.

In order to construct a stack of 2D materials, a "transfer slide" was assembled which allowed for the picking up and deposition of layers of graphene, graphite, and hBN. To create this transfer slide, a diagram of which is shown in Figure 6, a batch of polymethyldisiloxane (PDMS) was first prepared by combining the resin and curing agent in a 10:1 ratio and allowing the mixture to cure for 24 hours in a 100 mm petri dish. Once solidified, a hole punch was used

to cut and remove a cylinder of PDMS which then had a small droplet of additional uncured PDMS deposited on top, forming a shallow dome once the droplet cured. The purpose of the domed PDMS was twofold; it created a consistent, well controllable touch point between the PC and SiO_2, and it may reduce internal stresses in the graphene layers induced during the pickup process[15]. In tandem, a solution of 13.3% wt/vol of polycarbonate (PC) in cyclopentanone was prepared[15,86], which required stirring at 450 rpm at 150-160°C for approximately eight hours to fully dissolve the solid PC. Initial experiments were performed using PC films made by casting a 10/90 wt% PC/chloroform solution between two microscope slides, which would lead to a thin PC film on the inner surface following rapid lateral removal of the top slide. Additionally, the first batch of PC in cyclopentanone was made using ~13.5% wt/wt rather than wt/vol, however this was again changed during later experiments. The wt/vol cyclopentanone solution was used for all device fabrication reported on here.

After preparing the PC solution in cyclopentanone, it was spun onto 1 cm^2 SiO_2 wafers (oxide thickness 90 nm) at 1400 rpm for 1 minute. The most consistent results were obtained by using PC films which had been allowed to cure for >24 hours in a nitrogen storage box, and in fact the films remained stable and usable for many weeks after. The transfer slide was finally constructed by picking up the PC film with scotch tape and laying it over top of the PDMS dome affixed to a glass microscope slide. The PC had a small hole punctured near the edge away from the PDMS dome for venting prior to heating the entire slide on a hot plate at 160°C for 3 minutes, which aided in removing trapped air bubbles and adhering the PC film to the PDMS[15].

Debris near the stack that accumulated from picking up extra flakes during stacking was reduced by cleaning the region near each flake of interest before picking it up with a PC stamp. Cleaning was done with a stamp made by laying a thin film of Polycaprolactone (PCL) over a

dome of PDMS in a similar manner to the construction of a PC slide, albeit with a far more sloped dome. The PDMS dome was made in the same way as described previously for the PC slide but using a much larger droplet of uncured PDMS when creating the dome. The PCL film was also made in a similar manner to the PC film, being spin coated onto 90 nm SiO_2 at 2000 rpm for 1 minute then baked at 70°C for 1 minute. Once constructed, the same transfer stage used to stack was used to bring the PCL into contact with the region of a flake that required cleaning. The stage was heated to 60°C for ~1 minute, then cooled to 36°C before being raised away from the surface of the flake. PCL melts at 55-60°C, so this process would effectively trap any debris or undesirable flakes within the film, leaving an empty region near the flake which is to be used in stacking.

Following confirmation of rhombohedral stacking in the isolated domains, construction of a transfer slide, and cleaning of debris near the flakes, they were stacked into vDW heterostructures using a modified version of the dry-transfer technique developed by Zomer et al.[10]. Using a transfer station equipped with high-precision micromanipulators, vacuum chuck, and heated stage, the surface of the PC was slowly brought into contact with the SiO_2 near the flake of interest after preheating the stage to 120°C. The slide was lowered until the contact area covered the flake, then slowly raised to pick up the flake as diagrammed in Figure 6. The pickup process was then repeated for the subsequent layers of the heterostructure, using lower temperature on the order of 60°C in cases where the entire flake was covered by those already on the PC as the vDW forces between layers would be sufficient to pick them up. The stage was rotated by 1.2° after picking up the first FLG layer in order to create the twist angle between the two layers, and the second half was picked up as slowly as possible to reduce twist angle disorder within the device. Finally, after all layers had been picked up the stack was put into

contact with a clean SiO_2 wafer which had been prepatterned with alignment markers for electron beam lithography (EBL) and the stage heated to 155°C. After lowering the slide enough that the contact region extended 100-200 μm beyond the stack, the transfer slide was slowly raised so that the PC detached from the PDMS. The stage temperature could then be incrementally increased to ~190°C which would fully melt the PC and smoothly separate the stack from the transfer slide[12]. The completed stack was then soaked in chloroform overnight to remove any leftover polymer.

Rather than stacking all layers at the same time and therefore increasing the risk of twist angle relaxation between graphene layers, the bottom halves of the stacks consisting of the bottom hBN layer and back gate were prefabricated using the stacking method described above. Additionally, these partial stacks were made using two layers of hBN on top of the back gate, with the topmost one being large enough to completely cover the layers beneath. This structure was made so that the top hBN layer on the back stack could be slid off the layers beneath using a specially made PDMS/PC transfer slide with an extremely narrow PDMS pillar supporting the PC film. When the two layers are put into contact, any trapped debris coalesces into bubbles, which are removed along with the upper BN layer leaving a clean surface without any debris or leftover polymer in a more efficient manner than cleaning with contact mode AFM (Figure 7)[87]. The upper portion of the heterostructure, i.e. the top gate, top hBN, and graphene layers, was then stacked separately and melted down on top of the prefabricated bottom half following careful alignment to the back gate.

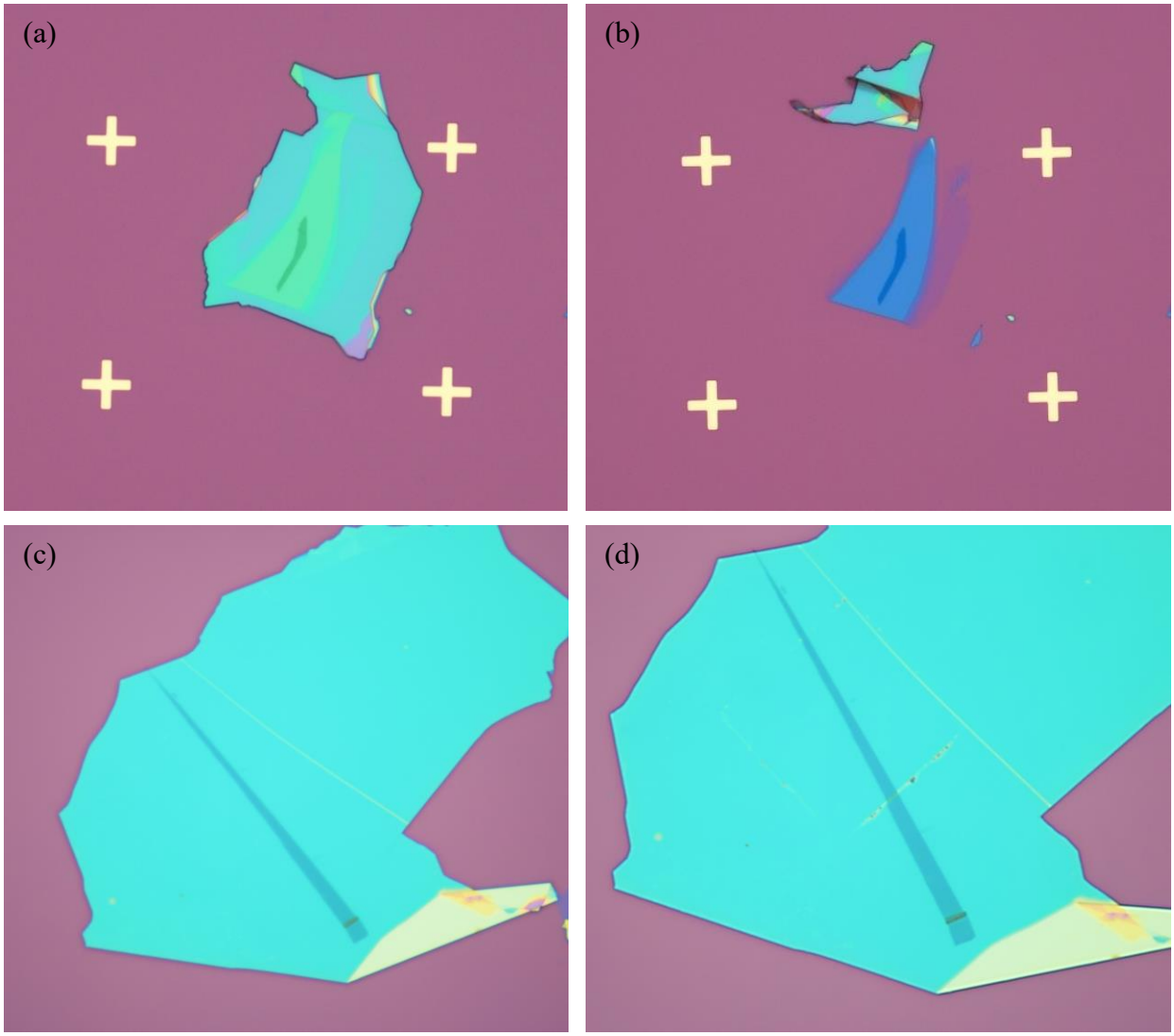

Figure 7: (a), (b) Back stack with the double hBN structure above the bottom gate before and after sliding the upper hBN flake, respectively. The entire surface of the hBN was equally clean following the removal of the second hBN flake. (c), (d) Back stack with only one hBN flake and bottom gate before and after contact mode AFM cleaning, respectively. The border of the cleaned region is seen in (d) as faint lines, with the region outside that area remaining dirty.

Once the stack was completed, it was fabricated into a transport device having a shape known as a Hall bar. EBL was performed using poly(methyl methacrylate) (PMMA) as a positive resist to define the device layout, which becomes more soluble in a 3:7 H_2O:Isopropanol solution once exposed to the electron beam. The PMMA resist consisted of two layers, both of which were spin coated onto the chip and baked for 5 minutes at 180°C preceding each EBL step. The lower layer was more sensitive to the electron beam, creating an undercut once the layer was developed which assisted in removing the undesired chromium/gold that was deposited in the

final step. Fabrication included several EBL steps, all performed at 100 kV of acceleration voltage. First, a large section of the top gate was exposed to air so it could be removed via O_2 plasma, preventing it from shorting to the graphene when metallic contacts were deposited. Removal typically required a plasma etching time of 3-5 minutes at 50W, performed in 1 minute increments to ensure the top hBN was not also etched away. Next, the geometry of the Hall bar was defined and the exposed areas were etched for 10 minutes with a CHF_3-based reactive ion etch (RIE). Finally, the metallic contacts were patterned and deposited by first evaporating ~7 nm of chromium for adherence, then 70-100 nm of gold on the stack. The unexposed PMMA masked all areas except the contacts and left the deposited metal in only the contact regions when washed away with acetone for 60 minutes. Excess gold was dislodged by repeatedly aspirating and expelling small volumes of the acetone bath from a disposable pipette positioned just above the surface of the SiO_2 chip. Table 1 summarizes the resist parameters used for each step.

Table 1: Type of PMMA and the spin coater rpm used to apply it for each EBL exposure step. The 495 PMMA type is more sensitive to the electron beam, which led to an undercut once developed.

Step	1st Layer PMMA Type	1st Layer Spin Speed (rpm)	2nd Layer PMMA Type	2nd Layer Spin Speed (rpm)
Top Gate Etch	A6 495	2000	A6 950	2000
Channel Etch	A4 495	2500	A4 950	4000
Evaporation	A4 495	2000	A4 950	2000

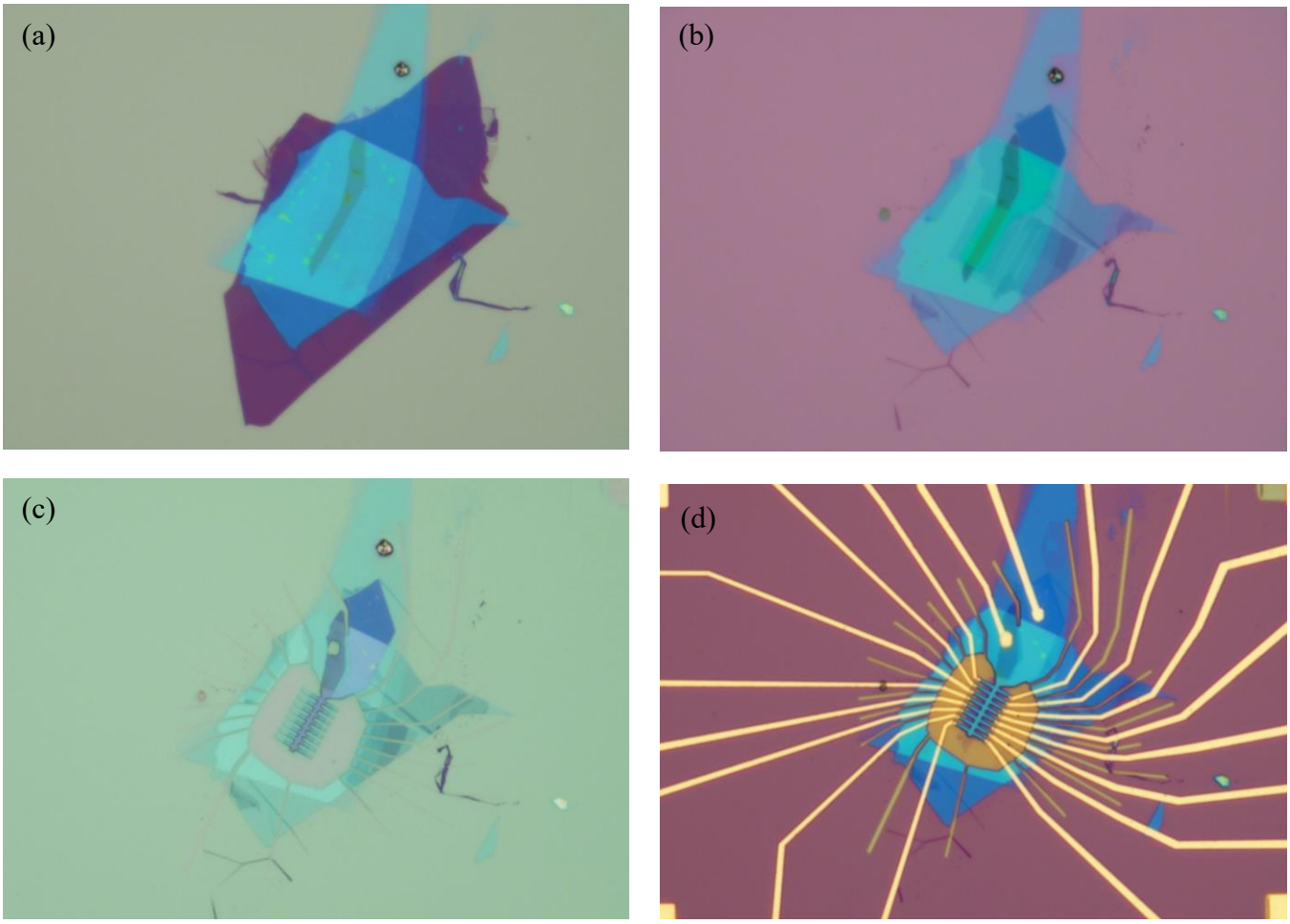

Figure 8: Images of a device at each step between melting down onto the prepatterned SiO_2 and deposition of metallic contacts. Variation in background color is due to differences in PMMA thickness at different stages of fabrication. (a) Completed stack melted down prior to the top gate etch. Large dark purple region is the top gate, blue regions are the hBN dielectrics, and the narrow dark grey region is the back gate. The graphene layers are faintly visible as slightly darker regions near the long arm of the back gate. (b) Stack following the top gate etch, as seen by the lack of dark purple graphite. A portion of the top gate was left intact, which can be seen by the variations in hBN color (darker blue when over one hBN layer, greener when over both). (c) Stack following the channel etch step, where the geometry of the Hall bar is defined. Note the additional etched separations to ensure any remaining portions of the top gate do not short to the graphene. (d) Completed device following gold deposition and liftoff.

Figure 8 shows the results of each step for one device, starting from complete stack and ending at a patterned device made from it. Devices were initially not made using the prepatterned SiO_2 substrates and therefore required alignment markers to be written and developed prior to each pattern exposure. The use of the prepatterned chips was extremely beneficial in this regard, as the number of EBL steps was effectively halved.

2.2: Device Measurement

Graphene devices are characterized by measuring their resistance as a function of both temperature and applied electromagnetic fields. Measurements may be made in either a two-point or four-point configuration. Four-point measurements decouple the sourcing and draining of current through the device from the measurement of resistance, which eliminates in-line contact resistance that could interfere with accurate interpretation of data. In this configuration, a current was sourced from a metallic contact on one end of the device and drained through a contact as far as possible towards the other side, and two other secondary contacts between them were used to measure voltage drop and extrapolate resistance from Ohm's law. The secondary contacts may be on the same or opposite sides of the device in order to measure longitudinal and transverse resistance, respectively, as shown in Figure 3(a).

To test the device's functionality, a room-temperature probe station measured the resistance between each contact and ground in a pseudo-two-point configuration. 10 nA was sourced through one contact with all others grounded, with a voltmeter in parallel used to extrapolate resistance. The contact was confirmed to be working if a value between 0.01 mV and 1 mV was observed, corresponding to resistance between 1 kΩ and 100 kΩ. This process also verified that the graphite gates were not shorted to the graphene or to ground by testing the resistance of the gate contacts with no applied current. If a large voltage was observed, then the gate was isolated. Once the device was tested, excess areas of the SiO_2 substrate were removed and the device was attached to a dual in-line package (DIP) socket with silver paste. The assembly was baked on a hot plate at 100°C for 15 minutes to remove the solvents in the silver paste and leave a solid connection between the device substrate and the DIP socket. A wedge

bonder was used to connect wires between the patterned device contacts and the DIP socket pins. Additionally, another pin was connected to the silicon wafer itself in order to apply a "silicon gate" voltage that assisted in reducing contact resistance. The device could then be placed in a cryostat for measurement, which had a DIP socket mount that ran connections between the pins and a breakout box.

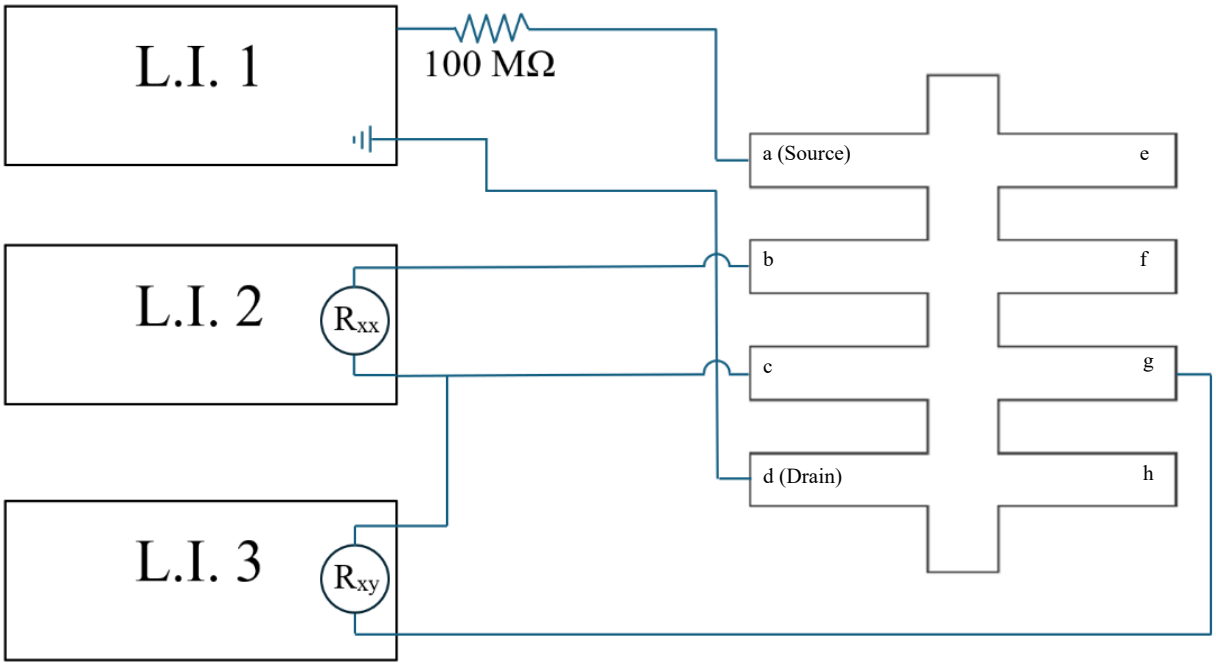

Figure 9: Circuit diagram of applied current from lock-in amplifier 1 (L.I. 1) as well as R_{xx} and R_{xy} measurements from lock-in amplifiers 2 (L.I. 2) and 3 (L.I. 3) respectively. Note that contact "c" is shared between R_{xx} and R_{xy}, a situation which was required in cases where there were not enough functional device contacts to have R_{xx} and R_{xy} both be measured separately. Voltages applied to graphite gates using source meters are not shown here, as they are electrically isolated from the Hall bar itself.

The experimental setup used to measure the devices was as follows: A 1 V, 17.7 Hz AC signal from a lock-in amplifier was applied through a 100 MΩ resistor to one of the device contacts, designated the "source", and another device contact designated the "drain" was connected to ground on that same lock-in. The 10 nA of current was used in this setup so that the fragile graphene layers were not damaged either through shorting via dielectric breakdown or the creation of uncontrollable thermal environments within the device. Other lock-in amplifiers slaved to the source/drain frequency were used to measure voltage drop between longitudinally

and transversely oriented contacts as described previously. Source meters were connected to the top and bottom gate contacts so that a voltage could be applied to them, leading to electrostatic doping or the application of an electric displacement field. A diagram of the lock in amplifier connections to a Hall bar is shown in Figure 9.

Initial measurements of the devices were to determine the gate voltage limits. Past a certain voltage the hBN layers will experience dielectric breakdown, potentially damaging the device. A Janis helium cryostat without magnetic field capabilities was used to determine these gate limits by slowly increasing the voltage applied and measuring current. Prior to dielectric breakdown the relationship between voltage and current is linear; however, at the onset of breakdown the current exponentially increases, at which point the voltage sweep direction is manually reversed or cancelled. Testing the gates with this method has the additional functionality of confirming their isolation from ground and other device contacts once the device is brought to liquid helium temperatures.

Once gate limits were determined, or simply once the first tests were performed if the limits were not reached as in the case of device 8, initial resistance maps were taken. Four-point measurements as described above were used to measure R_{xx} and R_{xy} while sweeping each gate from their lower to their upper limits and plotted on a color scale in Python. Data in the form of V_{tg} vs. V_{bg} was converted to plots of resistance as functions of charge carrier density n and electric displacement field strength D according to the relations

$$n = \frac{V_{tg}C_{tg} + V_{bg}C_{bg}}{e}$$

and

$$|D| = \left|\frac{V_{tg}C_{tg} - V_{bg}C_{bg}}{2\varepsilon_0}\right|$$

where ε_0 is the vacuum permittivity, V_{tg} and V_{bg} are the voltages of the top and bottom gates respectively, and C_{tg} and C_{bg} are the respective capacitances between the top and bottom gate and the graphene. C_{tg} and C_{bg} for these maps were estimated using the approximate thickness of the top and bottom hBN layers, respectively, according to the formula

$$C = \frac{k\varepsilon_0}{t}$$

where k is 3.5, the average dielectric constant for hBN, ε_0 is the vacuum permittivity in Farads per nanometer, and t is the thickness of the relevant BN layer. This formula gives the capacitance in units of $\frac{F}{nm^2}$, and subsequently n and D in $\frac{10^{12}}{nm^2}$ and $\frac{V}{nm}$ respectively, assuming that 10^{12} charge carriers per nanometer is full filling of the bands. Before plotting, n is converted to filling factor ν by normalizing n at full filling to 1 and scaling by 4 for graphene's fourfold valley and spin degeneracy. More precise values for the capacitances could be determined later using Landau fans once the devices were measured in a cryostat with magnetic field capabilities, and data plotted accordingly.

3. Results & Discussion

3.1: Flake Isolation, Stacking, & Device Fabrication Parameters

For exfoliated flakes to be usable they needed to meet two requirements: the flake must have both bilayer and trilayer regions, and the trilayer domain must have a large enough rhombohedral domain that it can be isolated and used in a device. Occasionally, the bilayer

region of a flake would be narrower than the isolated rhombohedral trilayer region, in which case the regions needed to be closely aligned or large enough that the relative angle of 1.2° could be maintained over the entire center channel of the Hall bar. These requirements were rather stringent, and the number of flakes which met them when using the initial exfoliation parameters was low enough that the amount of time spent exfoliating and searching for usable flakes was unreasonably high. Therefore, parameters were modulated as described in the methodology to promote the generation of suitable flakes. The number of flakes having bilayer and trilayer regions as a function of O_2 plasma cleaning time and hot plate baking time is shown in Figure 10.

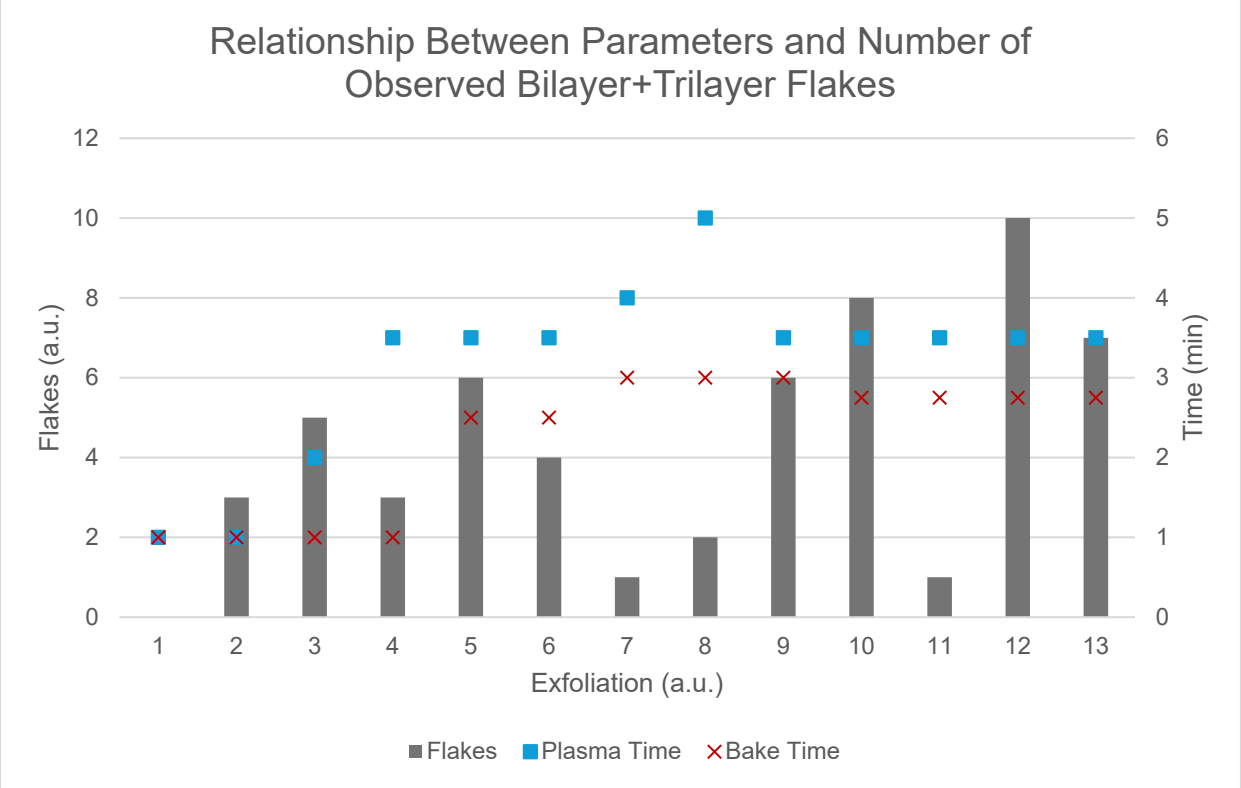

Figure 10: (grey, primary axis) Number of observed flakes having both bilayer and trilayer graphene regions within each exfoliation. (blue, secondary axis) Time that the SiO_2 wafers were cleaned in 50 W O_2 plasma prior to placing the scotch tape with exfoliated graphite onto the surface. (red, secondary axis) Time that the wafers/graphite-laden scotch tape were baked at 100°C before rapid removal of the tape. 13 exfoliations are shown here, however 19 total exfoliations were performed, with the excluded exfoliations all having been performed prior to those shown in the graph at the starting parameters of 1 minute each of O_2 cleaning and baking. None of the excluded exfoliations contained 2+3 flakes.

3 minutes 30 seconds of O_2 plasma cleaning and 2 minutes 45 seconds of baking at 100° was found to result in the most flakes having both bilayer and trilayer regions. These parameters left a more sparse distribution of FLG overall when compared to 1 minute for both plasma cleaning and hot plate baking, however the regions which were present were qualitatively more likely to be large, continuous, and high quality (Figure 11). Confirming whether these exact parameters were best or if the improved yield was due to a general increase to the 3-4 minute/2-3 minute range is left to future work. None of the above discussion includes information on parameters which promote the formation of rhombohedral domains in the trilayer graphene regions. This exclusion is primarily because there was no change in parameters which had an immediately noticeable effect on the amount of rhombohedral vs. Bernal stacked graphene. This would be an interesting direction of future study, in addition to the advancement of initial work on expanding rhombohedral domains via application of local electric fields and mechanical pushing of domain walls with a blunted AFM tip[88–90]. Development of the domain expansion

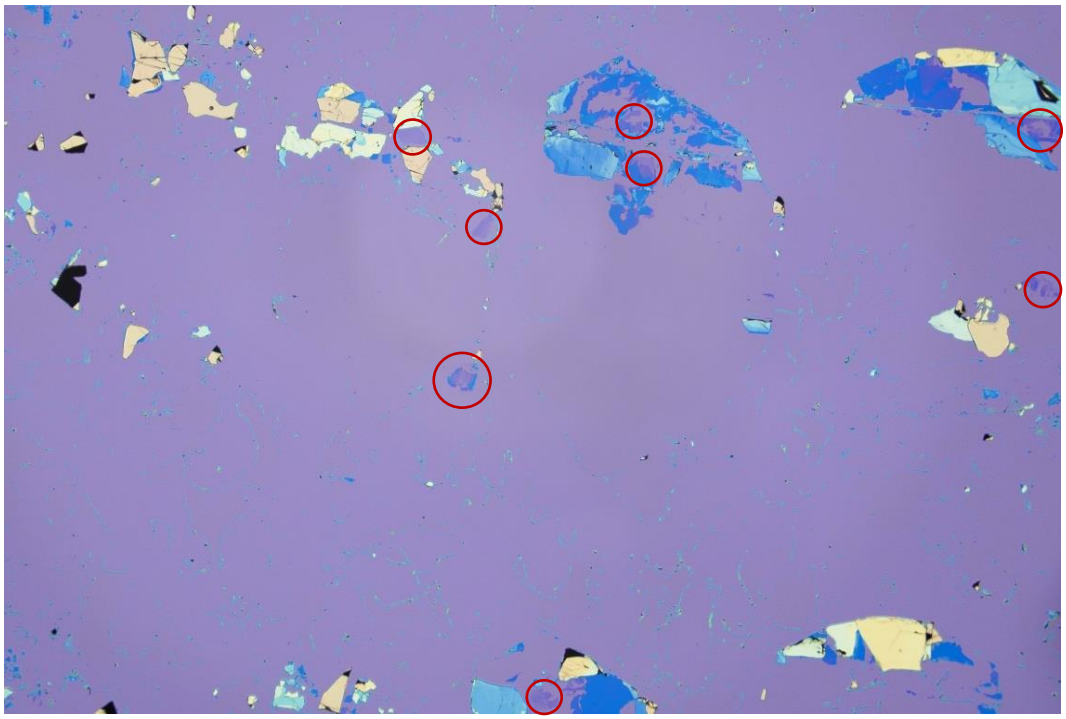

Figure 11: 2x optical image of an exfoliated flake using the optimal parameters. Red circles denote large, continuous FLG regions (varying from 1~10 layers).

technique would be particularly valuable to the present work, as device design was often constrained by the low size of continuous rhombohedral domains in trilayer graphene.

As previously discussed, continuous rhombohedral domains within the trilayer regions were small when compared to the size of FLG regions which are typically fabricated into devices. In addition to challenges during stacking, discussed later, the small size of the domains impeded the AFM-based LAO process used to isolate the domains from the rest of the flakes. The small fringes, or fingers, around the edges of the isolated domains were introduced with the goal of reducing the emergence of twist angle disorder between graphene sheets once stacked. However, the small size of the trilayer rhombohedral domains used in our devices caused the width of the fringes, and the spacing between them, to be below the resolution of the LAO process. Therefore, the width of the borders around the isolated regions were instead simply expanded to the length of the fingers, further reducing the size of the usable regions (Figure 12). This error was not caught until the fabrication of the fourth tRTBG device, at which point the fringes were removed from the cutting pattern and a simple rectangle was used instead, leaving a larger portion of the rhombohedral domain intact.

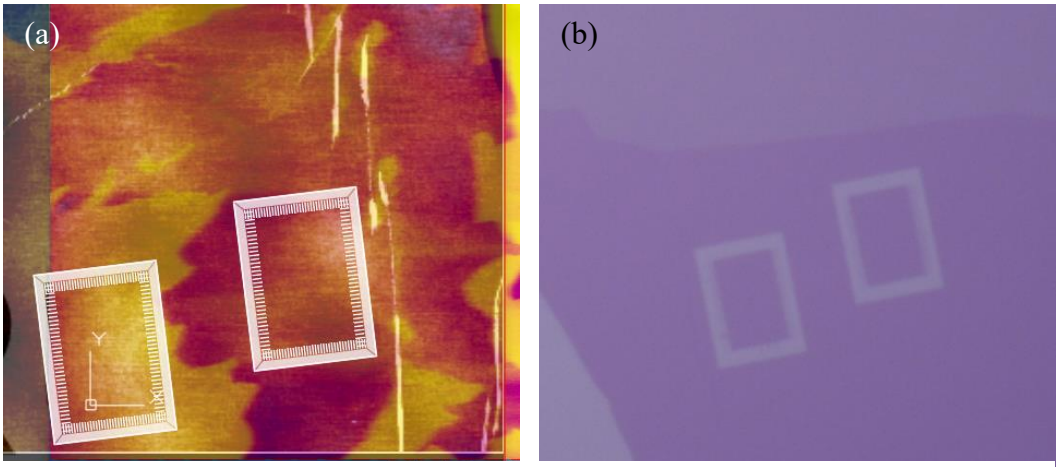

Figure 12: (a) LAO cutting pattern (white rectangles), AM-KPFM of the relevant region, and AFM height map of the same region all overlaid during the process of setting up the LAO process. (b) Optical micrograph of the cut regions defined in (a). Note the wider borders than in (a) and the lack of fringes. Some shadowing/debris is indeed present in the regions where the fringes should be, but there is otherwise no definition to them.

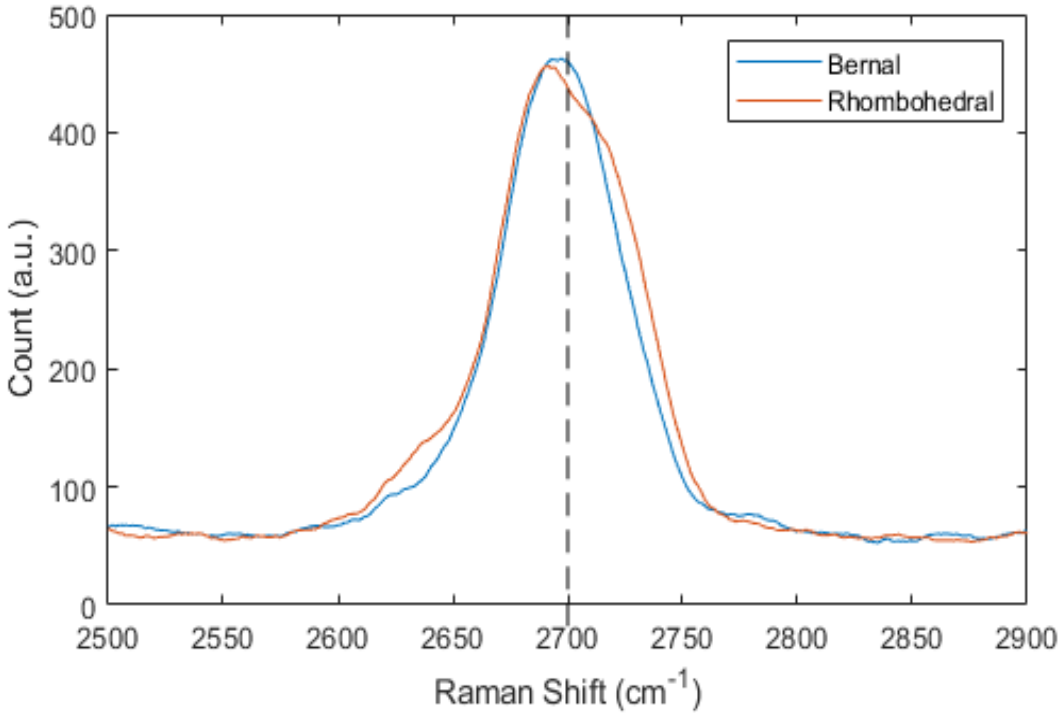

Figure 13: Raman spectra of the 2D mode of rhombohedral (red) and Bernal (blue) domains of graphene flake Gr128b, exfoliated after 3.5 minutes of O_2 plasma and 2 minutes 45 seconds of baking. The rhombohedral peak is centered more closely about 2700 cm^{-1} (grey dashed line) than the Bernal peak and displays a characteristic shoulder shape.

Initial identification of rhombohedral domains was performed with the AM-KPFM technique described in section 2.1. However, determination of rhombohedral stacking order following LAO isolation of the region was done via Raman spectroscopy measurement of the isolated flake. Figure 13 shows a representative Raman spectrum of an isolated rhombohedral domain and Bernal stacked region from the same flake. Characterization via this method addressed two issues at once; if performed after the LAO process it confirmed that the isolated flake did not relax into the Bernal stacking configuration due to applied stresses or electronic environments created by the LAO process. Additionally, it provided more concrete evidence for the presence of rhombohedral stacking order than AM-KPFM alone, which may be misleading or misunderstood without further context from other characterization methods (see the slightly lighter purple shadow in the AM-KPFM image in Figure 5d). Generally, Raman spectra of

rhombohedral graphene and graphite is shifted towards higher wavenumbers (~2700 cm^{-1}) than the Bernal stacking order and shows a characteristic "shoulder", or slanted top to the spectral peak rather than a uniform Gaussian-like distribution[85].

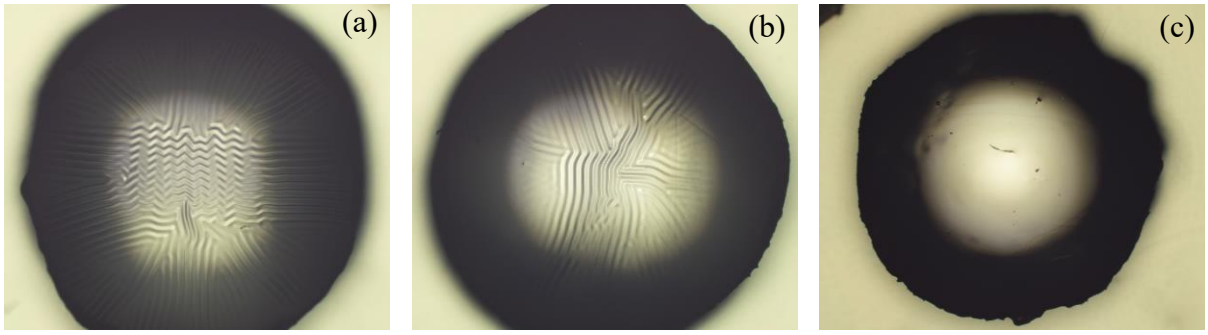

Figure 14: (a) Surface of a transfer slide made using the wt/wt PC in cyclopentanone solution after being cooled rapidly on a metal heatsink after the 3 minute bake at 160°C. (b) same as (a) except the slide was cooled on the hot plate, which was turned off at the 3 minute mark and left to cool to room temperature gradually. The slide was removed once the thermometer on the hot plate read 40°C, but the wrinkles formed prior to that temperature being reached. (c) Surface of a PC slide made using the wt/vol PC in cyclopentanone solution showing no wrinkles even after the baking step. This particular slide was made using a PDMS dome which was smaller in diameter than those in (a) and (b), however others were made using the same diameter PDMS and showed similar behavior to the slide in (c).

PC slide construction was not initially a concern, however issues that arose during stacking and meltdown led to its inclusion in the set of process refinements developed in this work. Slides made from PC films spin coated onto 90 nm SiO_2 and extremely shallow PDMS domes were found to be optimal for fabricating tRTBG stacks. Figure 14 shows the surfaces of PC transfer slides made using various techniques. The slides made using the wt/wt PC/cyclopentanone solution appeared to contain a large amount of residual stress, as evidenced by the wrinkling structure present regardless of cooling rate. This stress may have been introduced during the transfer slide fabrication process or it may have been introduced by spin coating and drying. However, the exact characteristics of the wt/vol solution which made it immune from such spin and drying induced stresses are unknown, if those are indeed the culprit of the wrinkles.

Stacking methodology was originally based on the process developed by Díez-Merída et al.[12], however our meltdown process required a higher temperature of ~155°C to induce separation between the PC and PDMS. This may be due to the specific formulation of PC in cyclopentanone or the geometry of the PDMS domes used in our experiments. Regardless, by using the higher temperature we observed similar results to previous work and made no other significant changes to the methodology. During meltdown, the PDMS needed to be prevented from coming back into contact with the PC due to thermal expansion by slightly raising the transfer slide while increasing the temperature. When the microscope slide-cast, PC in chloroform solution was used and the PC film was not detached from the PDMS in this way (which required the use of the domed PDMS), the separation of the two would instead happen gradually and only with the application of a very large upwards force once the stage temperature reached ~200°C. At this point the PC was above its T_M and adhered very strongly to the PDMS.

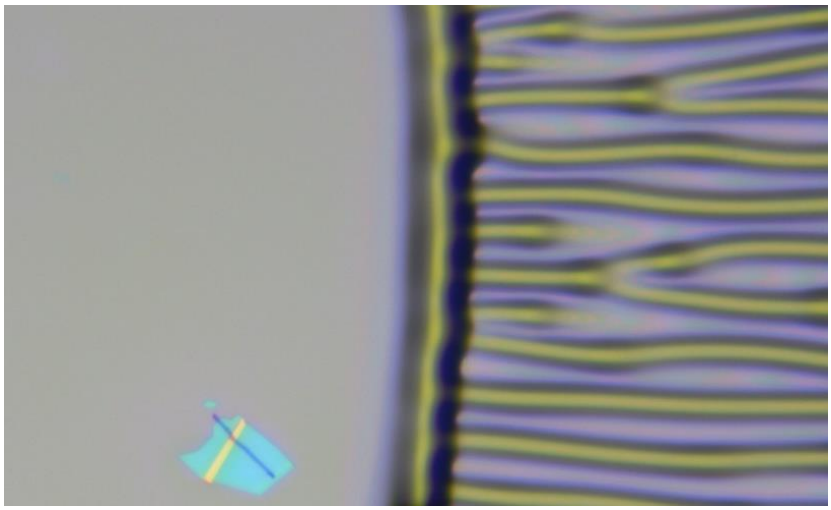

Figure 15: Image taken during the meltdown of a back gate and bottom hBN (lower left). The left side of the image shows the area where the PC and PDMS are still in contact with each other, the right side shows the strain-induced lamellar PC structure, with a large boundary between them. This boundary region is where the highest upwards strain is being applied.

Once separated, the PC would exhibit a pronounced lamellar structure caused by large out of plane strain occurring at the contact boundary (Figure 15) oftentimes leading to the destruction

of the stack due to the shifting of relative layer position. Thus, a meltdown process which removed the possibility of such a large strain being applied to the stack was necessary.

Remaining fabrication steps (EBL, RIE, gold evaporation & liftoff) did not show any unexpected behavior. Images of the four devices fabricated for this work are shown in Figure 16.

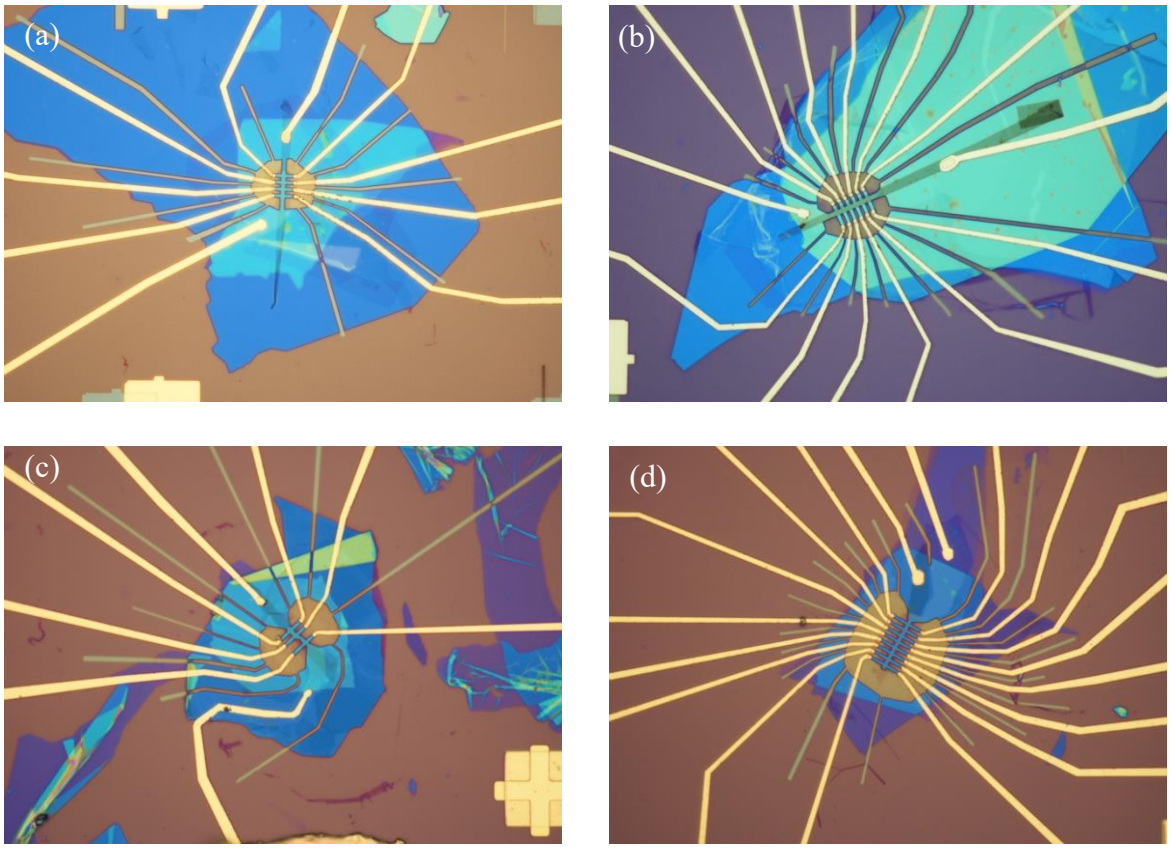

Figure 16: 100x optical micrographs of the four devices completed using the fabrication parameters developed here. (a), (b), (c), and (d), are designated device 8, device 9, device 10, and device 11 respectively.

3.2: Measurements

Resistance maps reported in this work were all taken in a Janis helium cryostat, which has a base temperature of 4K and no magnetic field capabilities. This instrument is primarily used in other experiments for initial, quick probes into device characteristics as well as to confirm that the device works as expected at liquid helium temperatures, but in the case of this

work was used as the measurements were not the primary focus. Figure 17 shows the device gate limit tests which were performed on devices 8 & 9. Device 8 showed expected gate behavior with no signs of dielectric breakdown up to the values we tested. The gates could likely be pushed even beyond these values, but for initial characterization these were determined to be good enough. Although the back gate on device 9 was very high quality, the top gate showed extremely limited range, with dielectric breakdown occurring at voltages of just ±0.5V. Resistance maps were taken of both devices as a function of both top gate and back gate voltage across their entire ranges following this characterization.

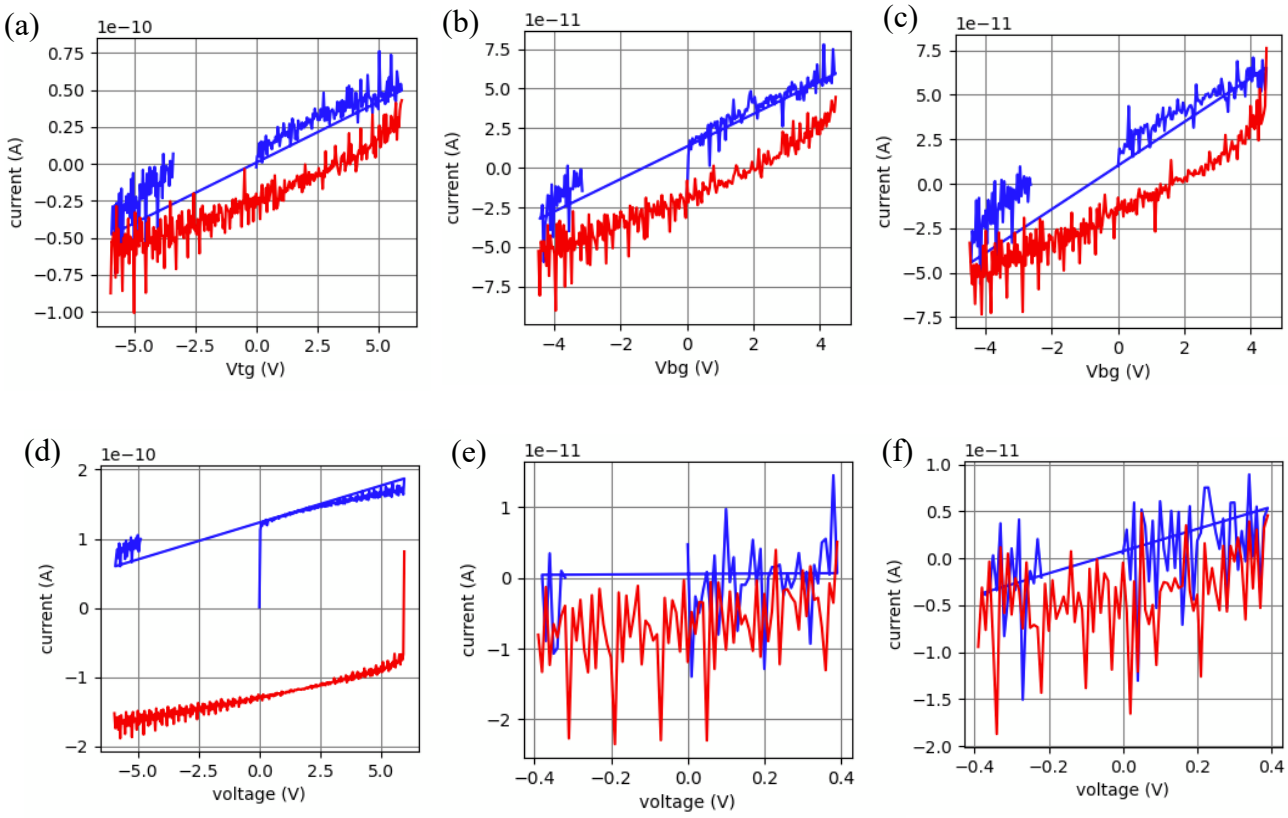

Figure 17: Voltage vs. current graphs used to characterize the gate limits of devices 8 (a-c) & 9 (d-f). (a) Device 8 top gate sweep from -6 V to +6 V, holding the back gate at 0 V. (b), (c) back gate sweep from -4.5 V to +4.5 V at top gate values of +6 V and -6V respectively. (d) Device 9 back gate sweep from -6 V to +6 V, top gate held at 0 V. (e), (f) top gate sweep from -0.4 V to +0.4 V while holding the back gate at +6 V and -6 V respectively. The top gate showed signs of dielectric breakdown past these values.

Figure 18 shows a color plot of resistance as a function of filling factor ν and electric displacement field D, calculated from gate voltages as described in Methods, for device 8.

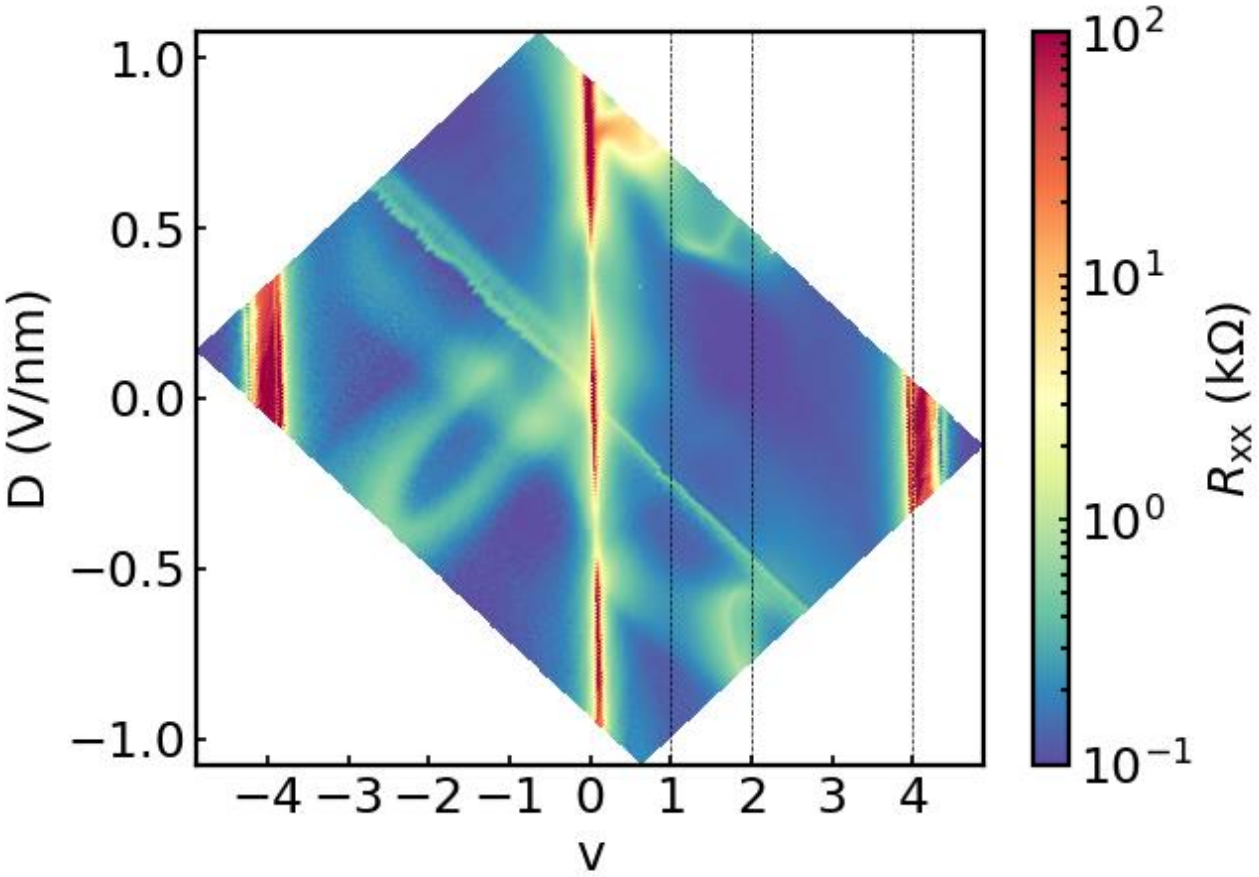

Figure 18: Color map of longitudinal resistance R_{xx} as a function of band filling factor ν and electric displacement field D for device 8. Positive D in this device is defined as the field pointing towards the rhombohedral trilayer, polarizing the electrons to the graphene layer most distant from the Moiré interface. The resistive line which tracks V_{tg} = 0 V is attributed to a trapped state at a metal/graphite contact interface. Vertical dotted lines at ν = 1, 2, and 4 were added as visual aids.

Several interesting features can already be observed on just this map. Firstly, as evidenced by the two "pinch points" in the resistive stripe at charge neutrality (ν = 0) there is an intrinsic band gap which closes near D = ±0.3 V/nm and reopens at D = ±0.5 V/nm. Additionally, there is a resistive bump at positive D and ν = 0 ~ 1. Notably, this value of D corresponds to electrons polarized to the Bernal bilayer, in contrast to theoretical predictions. Within this bump, R_{xx} has a slight dip which is to a qualitative analysis near ν ≈ 2/3. The closing and reopening of a gap seen in this device is in qualitative agreement with previous work on other rhombohedral Moiré systems

described in section 1.3, and other similar features between those devices and this one seem to indicate that this device has a twist angle $\Theta > 1.4°$, although this is simply a first approximation and must be confirmed by further measurements. The most interesting feature of this device is the resistive bump near D = 0.75 V/nm and ν between 0 and 1. Fractional states may be observed in this regime at lower temperatures, and future experiments will explore this region in more detail to confirm whether this is the case.

Although the gate range is extremely limited, a resistance map was also taken of device 9 across the full range of accessible parameters (Figure 19). Unfortunately, the range does not appear to encompass even the charge neutrality point of the device, and no further characterization will be done on this device. The true cause of the limited top gate range is unknown; however, the most likely explanation is a crack which formed in the hBN layer separating that gate from the graphene during stacking. This crack would cause the dielectric environment to be uneven throughout the region covered by the gate, or even have a small portion which does not have any dielectric at all between the gate and graphene.

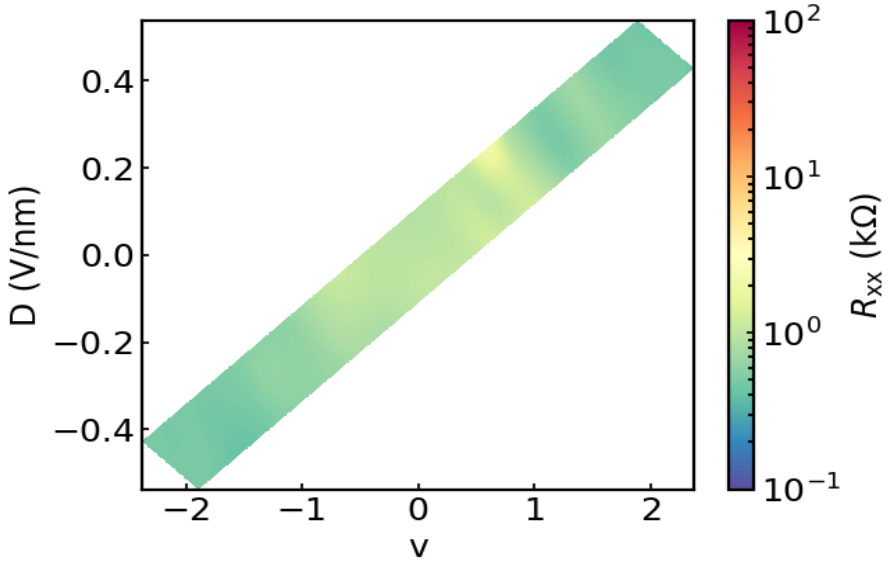

Figure 19: Resistivity map of device 9, having a small enough top gate range that no interesting features are accessible via displacement field or electron filling.

3.3: Anomalies

During the sliding of the second hBN layer on the prefabricated bottom halves of stacks, an interesting behavior was observed where the bottom hBN appeared to be cleaved horizontally (i.e. made thinner) after sliding the upper layer away. Figure 20 shows optical micrographs of the hBN flakes used in the fabrication of partial stacks for devices 10 and 11, both as exfoliated and following the hBN sliding process.

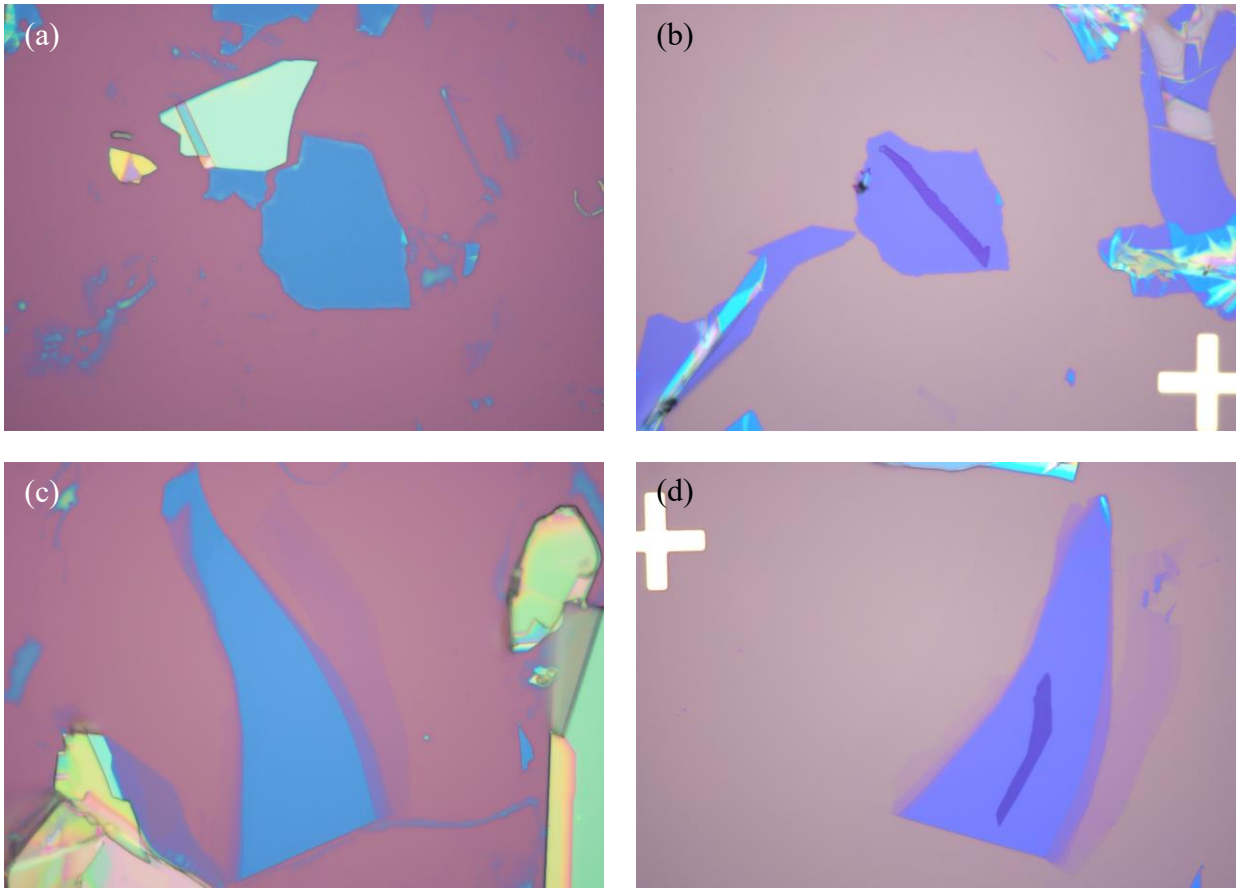

Figure 20: (a), (c) 100x optical micrographs of the as exfoliated hBN flakes used in the construction of partial stacks which were used to fabricate devices 10 and 11, respectively. (b), (d) 100x optical micrographs of the partial stacks following the hBN sliding process. Slightly different SiO_2 substrates led to altered background colors, however despite this fact the hBN flakes are clearly reduced thickness when compared to (a) and (c).

Initially, accidental alignment between the crystal lattices of the hBN layers prior to sliding away the upper layer was suggested as a mechanism by which the two layers became strongly adhered to one another. However, this effect was observed in two separate structures

which were fabricated weeks apart from one another. Given that alignment of hBN typically requires careful, intentional fabrication to achieve, the inadvertent creation of aligned stacks was deemed improbable. Further experiments should be performed to determine if this cleaving is consistently reproducible, as well as to characterize how thinly the flake is cleaved. Most likely, this is a somewhat stochastic process and the final thickness of the hBN layer is not controllable. However, if the cleaving can be performed intentionally and the thickness of the final flake is consistent, this process would offer an extremely useful avenue by which dielectric layers of transport devices can be tuned for particular use cases. Another interesting question is whether this process can be repeated by placing another layer of hBN on top of the already cleaved flake and performing the sliding process again, and if so to what extent the lower hBN can be thinned before it too is destroyed.

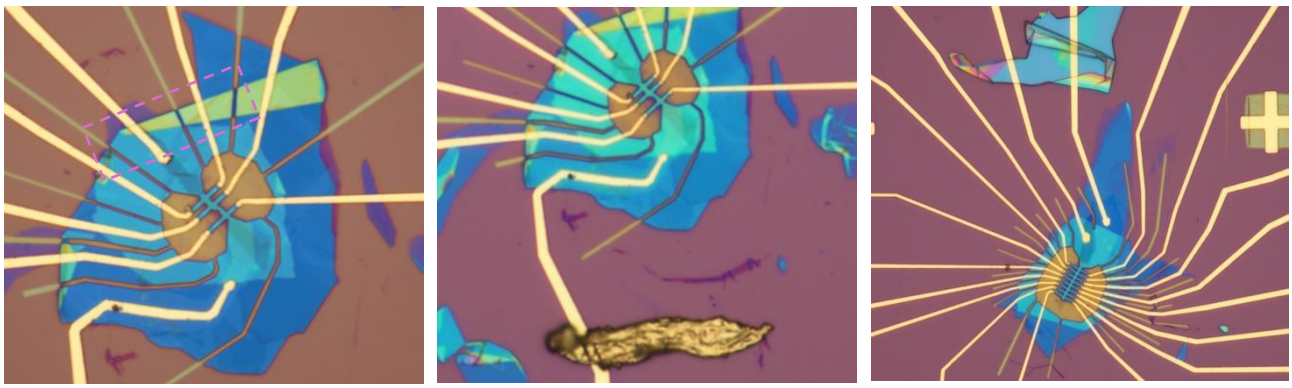

Figure 21: Optical micrographs of devices 10 and 11. (a) 100x image of device 10, inset box shows where hBN remains connected after etching offering a potential short to the back gate contact if graphene/graphite remains present underneath. (b) 50x image of device 10. The large gold colored debris in the lower middle section has broken the contact between the top gate and the rest of the gold channel (not pictured). (c) 50x image of device 11, with the tall hBN debris seen in the upper middle portion. The gold channels appear to be continuous at the angle the image was taken but are likely broken in the plane of the page (i.e. there is a jump in height somewhere along the debris not connected by gold).

Finally, during the initial testing of devices 10 and 11 they were both found to have complications with their gates (Figure 21). In the case of device 10, the back gate was shorted to the graphene channel, and the top gate was not connected to the gold contact pad used to interface with it. The former issue was attributed to either an incomplete etch of the separating

channels or inadvertent connection to the graphene via gold contact to the gate. The latter issue was caused by debris introduced in the final PMMA spin coating step (Figure 21a), which was in fact observed prior to gold evaporation but was dismissed due to confidence that it would not threaten functionality of the contact. Unfortunately, this was not the case, and a secondary etch and evaporation was needed to fix these issues. In the case of device 11, neither the top gate nor the back gate was connected to their contact pads. The most obvious culprit was a rather tall piece of debris left on the SiO_2 from the hBN sliding of the partial stack which the gold channels were patterned over (Figure 21c). To repair the device, one of the channel contacts was first etched away to ensure isolation from the graphene layers, then the back gate contact was connected to it via a second gold evaporation. The top gate contact did not require the sacrifice of a channel contact in this way, as there was enough room to create a channel going around the debris.

4. Conclusion

This work developed the following methodology for the fabrication of tRTBG devices. First, ~1 cm^2 285 nm SiO_2 chips are cleaned in a 50 W O_2 plasma for 3 minutes and 30 seconds. Micromechanically exfoliated graphene is quickly placed into contact with the surface of the SiO_2 and baked at 100°C for 2 minutes and 45 seconds. The tape is rapidly peeled off the surface, at which point they can be examined via optical microscopy for the presence of flakes having bilayer and trilayer regions. AM-KPFM is used to identify rhombohedral domains within trilayer regions, and LAO isolates them from the rest of the flake. Raman spectroscopy is used to verify the isolated flakes have remained rhombohedral throughout the process. A 13.3% wt/vol PC in cyclopentanone solution is spin coated onto 285 nm SiO_2 at 1400 rpm for 60 seconds then laid over top of an extremely shallow PDMS dome to create a transfer slide. Flakes are picked up at 120°C unless fully covered by layers already on the PC, and the stacks are melted down at 190°C after detachment of the PC from the PDMS at ~155°C. Partial stacks consisting of a back gate and bottom hBN layer on prepatterned SiO_2 substrates and cleaned using the BN sliding technique are used to assist in reducing strain and twist angle relaxation. Electron beam lithography using a bilayer of PMMA as a positive resist in combination with O_2 plasma etching, RIE, and evaporation of 7/70 nm chromium/gold is used to define device and contact geometry.

This exfoliation method showed strong promotion of bilayer/trilayer flakes, and the stacking method led to consistently functional devices. Future work on methods to better control twist angle would be useful, as the interlocking fringes occasionally used in other experiments was unable to be applied to this work. Additionally, development of methods to artificially create or expand rhombohedral domains in trilayer graphene would prove highly beneficial, as the size

of domains was a primary constraint on device fabrication. Investigation of the behavior of hBN during the application of the sliding technique could lead to interesting methods to control the thickness of hBN dielectric layers, offering a greater degree of control over device geometry and allow for the effect of interlayer spacing to be more systematically studied.

Measurements performed at millikelvin temperatures and in a magnetic field are the next primary focus for the tRTBG system. Further measurements of device 8 will shed light on the nature of the resistive bump at positive displacement field, and measurements of devices 10 and 11 following completion of their repairs will offer a larger sample size of tRTBG devices opening the door to investigation of twist angle dependence on observed physical phenomena. Based on ours and others' exciting initial work on tRTBG, we are optimistic that it is a promising new platform to study highly correlated electronic states, and are confident that this work will serve as a useful foundation for further experimentation.

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