

# A Terabit Optical Link in Silicon

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**Abstract**

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As data centers grow, there is a need to be able to densely pack low power, high bandwidth, kilometer-reach interconnects into the same available rack space as existing technologies. Silicon is particularly well suited for this task due to its ability to accommodate high-speed single-mode optical systems-on-chip. An outstanding question is whether silicon photonics can easily scale to these larger systems and, more importantly, if these types of systems can yield reliably. This dissertation first investigates the design, fabrication, and test of a bi-wavelength polarization splitting grating coupler and two high-speed Mach-Zehnder modulators for integration into the OpSIS process development kit library (PDK). Finally, this dissertation discusses the integration of these components from the OpSIS PDK to demonstrate a  $48 \times 50$  Gb/s parallel single mode transceiver.

A novel bi-wavelength polarization splitting grating coupler is designed and tested. It is experimentally shown that it is possible to couple C-band and O-band wavelengths and perform polarization splitting simultaneously in a single device. For C-band light, we

measure a maximum transmission of 7.6 dB, polarization isolation of 24 dB, and -1.5 dB transmission window of 35 nm. For O-band light, we measure a maximum transmission of 8.2 dB, polarization isolation of 8.4 dB, and -1.5 dB transmission window of 18 nm.

Two differentially driven Mach-Zehnder modulators are designed and characterized for digital and analog applications. The first is demonstrated to operate at 50 Gb/s with a differential 1.5 V<sub>pp</sub> RF driving signal with 0 V DC bias, suggesting an RF power efficiency of 450 fJ/bit. The second device is placed into an analog optical link and spur-free dynamic range measurements are performed. A SFDR<sub>IMD</sub> of 97 dB·Hz<sup>2/3</sup> and SFDR<sub>SHD</sub> of 82 dB·Hz<sup>1/2</sup> are measured by differentially driving the modulator.

Lastly, the parallel single mode transceiver we report here represents nearly an order of magnitude greater aggregate data rate and four to five times the channel count compared against other silicon transmitters. Our receiver also compares favorably against previous arrays of Ge-on-Si photodetectors and is monolithically integrated on the same wafer as the transmitter. We present bit-error-rate versus received optical power curves as well as DC performance for all 48 channels of the transmitter and open eyes at 50 Gb/s for the receiver.

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Finally, I would like to thank my family for their support and encouragement. I don't think I could have done this without them, and the dedication on the next page can't properly express how grateful I am to have them.

## **Dedication**

To my family:

My parents, David and Sharon, who must have done something right;

My grandma, Pat, who will read every word of this and to whom I will delight in explaining every word;

My fiancée, Emma, who put up with my late nights finishing this thing.

## Chapter 1. Introduction

### Motivations for Silicon-Based Optical Devices

Starting from the 1970s, fiber optic systems have been field tested and deployed in order to meet the world's needs to communicate. Early first generation systems operated at wavelengths near 850 nm using AlGaAs lasers or GaAs LEDs on multi-mode fiber. Losses (approximately 2 dB/km) and modal dispersion limited the performance of these systems. With graded-index fiber, the dispersion-limited bandwidth-distance product was 2 Gb/s·km, with systems operating at up to 45 Mb/s over 10 km [BL90]. With the development of InGaAsP lasers operating at 1.3  $\mu\text{m}$  and single-mode fibers, much greater transmission distances were possible. These second-generation systems were no longer dispersion-limited, but were instead loss limited with attenuations near 0.4 dB/km. In this wave, systems operating at 1.7 Gb/s over 50 km spans were commercially available [BdMI95]. The third generation systems moved to 1.55  $\mu\text{m}$  single-mode lasers in the mid-1980s, where the losses were now around 0.2 dB/km and the dispersion limit was up to 5000 Gb/s·km. Finally, the fourth generation systems saw the widespread integration of wavelength division multiplexed (WDM) transmission systems. Advancements in WDM and amplifier technologies allowed the rapid doubling of fiber capacities by virtue of squeezing more wavelengths through a single fiber. Figure 1.1 plots the growth of fiber optic communications through its first two and a half decades of deployment [K00]. Further advancements in error correcting codes, amplification, advanced modulation formats, polarization multiplexing, and digital signal processing have pushed forward fifth-generation systems and beyond.

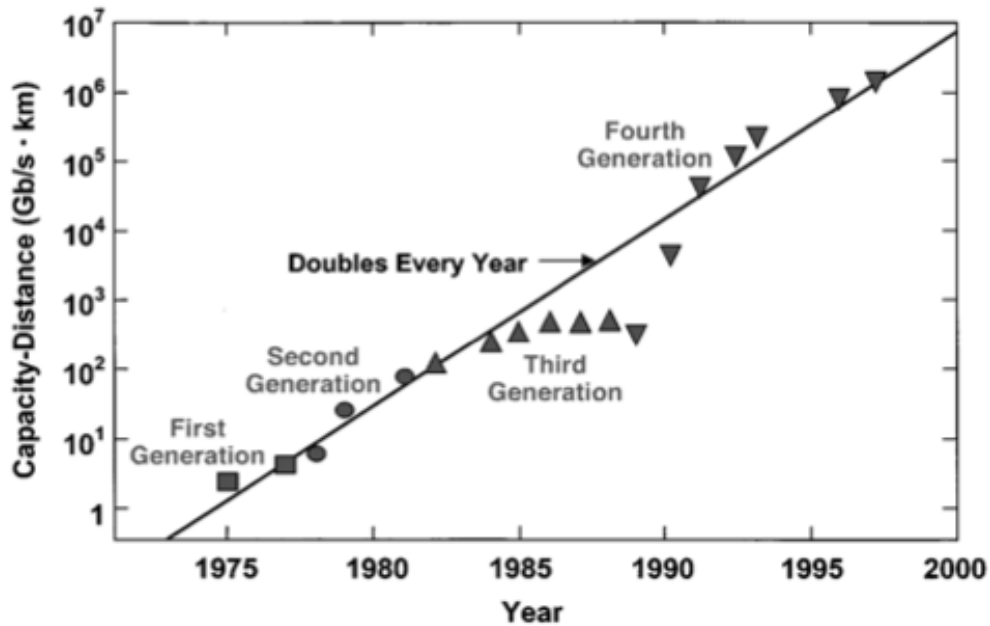


Figure 1.1: Bandwidth-distance product growth of fiber optic communication systems over time. Figure from [K00].

In recent years, this constant demand for more capacity has been driven by the expansion of internet-connected devices and consumer streaming media. This growth, approximated by the growth of Ethernet bandwidth for finance, scientific computing, cable, peering, and IP traffic, is visualized in Figure 1.2 [IEEE10]. As the total available bandwidth increases, the length scales at which it is economically feasible to replace electronic data communication with optics decreases. Recently, there has been significant research into integrating optics into the data center [VLZ+11], high performance computing [HAC+13], inter-chip [UHN+12], and intra-chip interconnects [CRZ+11]. These levels of optical integration simply cannot use the same material systems that dominated the long-haul fiber optic communication infrastructure, where modulators might be fabricated in lithium niobate, detectors on III-V wafers, optical multiplexers with doped glass, switches with MEMS, and everything connected via lenses or optical fibers.

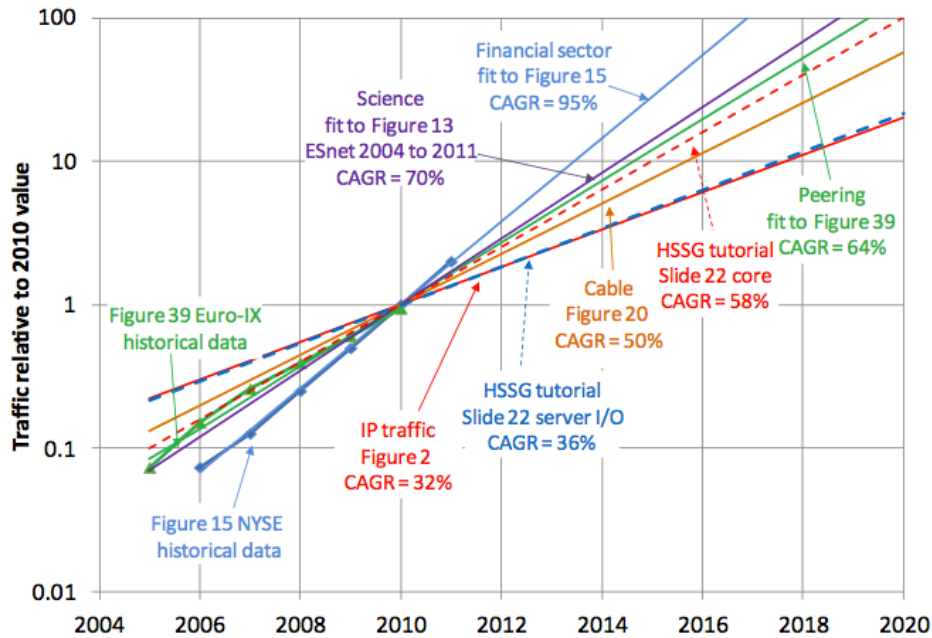


Figure 1.2: Aggregated Ethernet growth rates. From the 2012 IEEE 802.3 Working Group Ethernet Bandwidth Assessment [IEEE10].

By taking advantage of the high refractive index contrast between silicon and silicon dioxide, and using silicon-on-insulator (SOI) wafers similar to those used for CMOS transistors, it is possible to construct micrometer-scale integrated optical circuits. This study of silicon-based optics, or silicon photonics, has benefitted from the billions of dollars invested in CMOS fabrication [HB10]. The already established processing infrastructure allows for extremely high levels of integration: devices that modulate, detect, route and filter light can all be co-located on the same wafer and built using the same tools in tandem. Moreover, building optical devices with the same silicon processing tools and wafers that the semiconductor industry uses to fabricate CMOS transistors gives access to an immense infrastructure for yield improvement, metrology and process control [BPG+12].

Typically, the major obstacle to leveraging CMOS infrastructure is the cost of accessing it: developing a silicon photonics process is at least a multi-million dollar endeavor. Silicon photonics has thus far been an expensive industry for startup activity, where the only players were those with immediate access to foundries that were willing

to change their process to accommodate optical devices; however, this is beginning to change. Commercial efforts by companies Luxtera and Kotura have produced products in silicon, for example. Additionally, a number of organizations around the world, including the A\*STAR Institute of Microelectronics (IME) [IME], CEA-Leti, Imec, and others [EPIX], have now developed silicon photonic processes with varying levels of capability. Access to these processes are available through multi-project wafer (MPW) shuttle run services, similar to what MOSIS offers for the integrated circuits community.

In addition to the MPW services providing optics-only options, there are several processes that can be used to fabricate transistors next to the optical components, such as IBM's 90-nm CMOS-photonics platform and Luxtera's and PETRA's processes, though these are not yet publicly accessible. Much of the development is focused on low-capacitance bonding between the standard foundry silicon for electronics and the silicon photonic wafers, since this obviates the need to make technical compromises, as well as the cost disadvantages associated with monolithic integration [ZLL+12].

In the absence of monolithically integrated transistors and optics, there are varying levels of alternative integration schemes available: separate optical and CMOS chips in a 2.5- or 3-dimensional integration scheme [HLL+09], or optical and electrical chips placed together on a printed circuit board [UHN+12]. Bonding processes are extremely mature and commercially available, and they provide an elegant solution to electronic-photonic integration, although co-integration of electronics will not be necessary for all applications. It is likely that many silicon photonic optical components will be in some type of standard form factor or as stand-alone packaged optical devices. Regardless of the final scheme chosen, it is clear that silicon photonics has the potential to drastically increase the possible complexity and economical viability of large-scale optical systems.

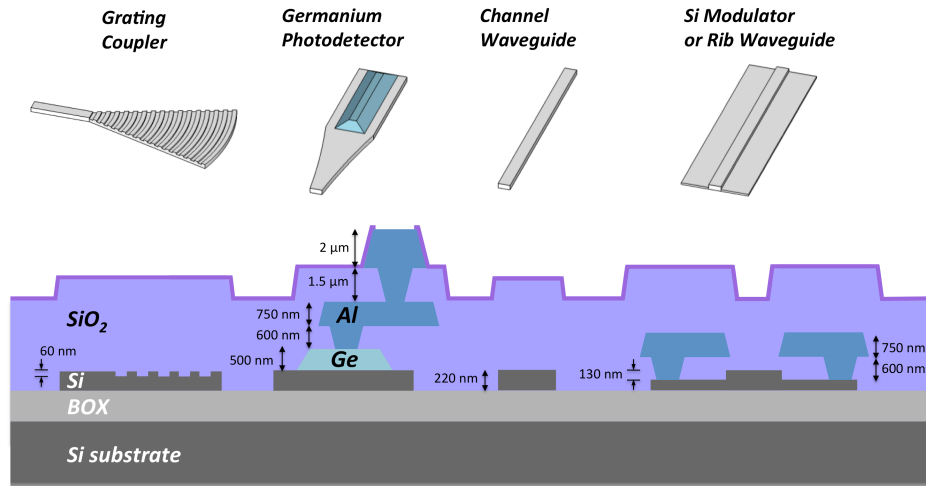


Figure 1.3. A few basic building blocks of systems in silicon photonics.

### Building Blocks of Silicon Photonics

The financial motivation for silicon photonics becomes more compelling when one considers the systems possibilities enabled by silicon photonics. Typical optical circuits consist of a few fundamental building blocks built on a silicon-on-insulator wafer: passive components such as waveguides, couplers and filters, and active devices such as modulators and photodetectors. Based on these building blocks, large systems can be pieced together without significant reengineering at the device level.

Due to the high refractive index contrast between silicon and silicon dioxide, it is possible to design tightly confining submicron waveguides. These devices typically consist of rectangular waveguides defined by a full etch to the bottom oxide layer, or by what are called strip-loaded or rib waveguides that are defined by a timed partial etch. The key to making low loss waveguides is in the ability to control sidewall roughness, which can introduce scattering processes and reflections [LLL+00]. Losses for single-mode waveguides are typically near 2 dB/cm [EPIX11]. For long path lengths along the chip, large multi-modal waveguides may be used. Typical losses for this type of waveguide are near 0.026 dB/cm [LYT+12], which is tolerable when an entire chip may be less than 1 cm<sup>2</sup>. Other passive devices such as grating couplers [NFH+11], waveguide

crossings [BDT+07], distributed Bragg reflectors [WSY+12], echelle gratings [HGO+09], and arrayed waveguide gratings [FD11] have also been demonstrated with low losses.

Electrooptic modulation is typically achieved by using the plasma dispersion effect, in which the refractive index of the waveguide is dependent on the density of free-carriers. The most common modulator designs are Mach-Zehnder interferometers and ring resonator based devices. By modulating the reverse bias of a PN-junction, speeds as high as 50 Gbps have been achieved with 450 fJ/bit power consumption in a Mach-Zehnder modulator [SDY+13]. On the other hand, a forward biased p-i-n junction is able to induce a much larger phase shift per voltage input, but at the cost of a slower response. Ring modulators, on the other hand, modulate light by shifting the resonance of an optical cavity. Ring modulators benefit from a much smaller footprint and power consumption than do MZM devices, but at the cost of increased temperature sensitivity and narrower wavelength operating window. A power consumption of 7 fJ/bit at 25 Gbps has been reported in literature [LZY+11].

Also of utmost importance is the detection of light at high speeds. The bandgap of silicon is too large to absorb at telecommunications wavelengths, and thus other materials are grown on or bonded to SOI wafers. The most common materials are epitaxially grown germanium on silicon or SiGe. It is also possible to bond III-V materials. Waveguides are usually butt or evanescently coupled into the photodetector. Due to the relatively tightly confined mode, the photodiode can achieve high responsivity with a small cross section in order to result in large bandwidths. A germanium photodiode has been demonstrated at 120 GHz with 0.8 A/W responsivity at 1550 nm [VPM+12]. Avalanche photodiodes in silicon are also possible; IBM has presented a device with 10 dB gain and a 30 GHz bandwidth [AXV10].

The final component of any optical system is the light source. Current techniques use an off-chip laser coupled in via grating or edge couplers. Several different methods for hybrid integration have been proposed, such as bonding [PFK+05] or epitaxial growth [FPC+06] of III-V materials. However III-V materials are incompatible with most standard CMOS processes. Germanium may also act as a gain medium, but must be

heavily n-type doped and strained in order to overcome the difference between its direct and indirect band gaps [SLK+10]. However, for most applications an on-chip light source is likely not a requirement. Just as in the electronics world with off-chip clock sources, off-chip laser sources could be used, especially when considering that the light eventually needs to be coupled off the chip for most applications.

Given the recent progress in achieving such an advanced state of many devices in silicon, work developing truly complex systems is just beginning. Barriers to building these types of systems have historically included immature design tools, a packaging ecosystem that is only beginning to be able to handle silicon, and the relatively high expense of doing systems-level work. Despite these barriers, the greatest advantage of using silicon in photonics, just as in the microelectronics industry, is the integration capabilities for constructing complex systems.

Examples of these complex systems in the literature span a wide range of applications. Several pieces of work have demonstrated passively and actively steered optical beams, as well as biological sensor components. A passive-only 2-dimensional array of an optical phased array antenna with  $64 \times 64$  nano-antennas integrated onto a single chip projected the MIT logo in a far-field pattern [STY+13]. The authors also demonstrated the active tuning of an  $8 \times 8$  version of the same antenna phased array. A similar concept was also demonstrated on a phased array featuring an on-chip laser [DHB+11]. In the biosensing realm, 16 photonic crystal resonators were integrated on a single chip to detect refractive index changes in microfluidic cavities [SE08].

Data communications has been the first and largest thrust of commercialization efforts for silicon photonics. Systems as complex as an integrated 224 Gb/s coherent silicon transceiver with on-chip polarization diversity [DLS+13] and a 360 Gb/s WDM ring modulator array [DLL+14] have previously been demonstrated. Single chip WDM receivers at up to 32-channels and higher have also been reported [FLS+10]. As the barriers to building complex systems are addressed, the community should expect to see systems with complexities even greater than those listed here.

## Silicon Photonics Modeling Techniques

Shuttle run services such as OpSIS or ePIXfab are mirroring practices well known to the microelectronics industry. Services such as MOSIS have provided researchers across academia and industry the tools and processes to build complex electronic systems at little risk. Aside from the cost savings that shared shuttle runs offer the community, they also provide design rules and well-characterized devices as part of a process design kit (PDK). Rather than designing a library of parts from scratch, users can piece together a series of devices that are known to work. However, what is missing from this equation for the optics world is the electronic design automation (EDA) infrastructure for design entry and verification.

Before fabricating large integrated electronic systems, an engineer may simulate the chip layout across process corners, compare it to a schematic (layout versus schematic, or, LVS), and check for layout errors that will not yield in fabrication (design rule checking, or DRC). Unfortunately, only the design rule checking exists as a somewhat mature toolset for optical design. Even so, given the smooth curves and non-manhattan features of the optical integrated circuit, which differ greatly from standard CMOS layouts, there is significant interest from the EDA tool vendors in modified DRC decks [CFG+14].

Compact models and schematics for verifying the final layout and performance of designs are still in their infancy. There are, however, several promising tools that are beginning to address these issues, such as Mentor Graphics Pyxis and Calibre, Lumerical Interconnect, and the IPKISS component design framework. As more features are added to these tools, the complexity of systems being taped out through multi-project wafer runs will also likely increase. A central challenge for the near term will be in standardizing the model sets and characterization methodologies, but this is now being taken on by industry organizations such as Si2 [NC14].

The silicon photonic devices themselves are typically modeled with numerical solutions of Maxwell's equations in either a 2-dimensional mode solver or 2- or 3-dimensional finite-difference time-domain solver. The former case is found by first starting with Faraday's law and Ampere's law:

$$\begin{aligned}\nabla \times \mathbf{E} &= -\frac{\partial \mathbf{B}}{\partial t} \\ \nabla \times \mathbf{H} &= \frac{\partial \mathbf{D}}{\partial t} + \mathbf{J}\end{aligned}\tag{1}$$

For a time-harmonic field and no current density, the above can be simplified to the set of equations:

$$\begin{aligned}\nabla \times \mathbf{E} &= i\omega\mu\mathbf{H} \\ \nabla \times \mathbf{H} &= -i\omega\epsilon\mathbf{E}\end{aligned}\tag{2}$$

which can be further rearranged into the eigenvalue problem:

$$\nabla \times \frac{1}{\epsilon} \nabla \times \mathbf{H} = \omega^2 \mathbf{H}\tag{3}$$

Thus, given some geometry, boundary conditions, and discretization ( $\Delta x, \Delta y, \Delta z$ ), a numerical eigenvalue solve routine may be employed (e.g. the Lanczos method). The solved-for eigenvalues will be the modal constants and eigenvectors the modal profile. A typical output of such a mode solve is shown in Figure 1.4 and Figure 1.5.

Likewise, a 3-D finite-difference time-domain simulator solves the curl equations by setting an appropriately small time step  $\Delta t$ . Using the Yee grid with spatial indices  $i, j, k$ , the  $x$ -component of the electric field at time step  $n\Delta t$  is found as:

$$\begin{aligned}
& \frac{E_x|_{i+1/2,j,k}^{n+1} - E_x|_{i+1/2,j,k}^n}{\Delta t} \\
&= \frac{1}{\epsilon_{i+1/2,j,k}} \left( \frac{H_z|_{i+1/2,j+1/2,k}^{n+1/2} - H_z|_{i+1/2,j-1/2,k}^{n+1/2}}{\Delta y} \right. \\
&\quad \left. - \frac{H_y|_{i+1/2,j,k+1/2}^{n+1/2} - H_y|_{i+1/2,j,k-1/2}^{n+1/2}}{\Delta z} \right)
\end{aligned} \tag{4}$$

The remaining components of the electric and magnetic field six-vector may be found similarly.

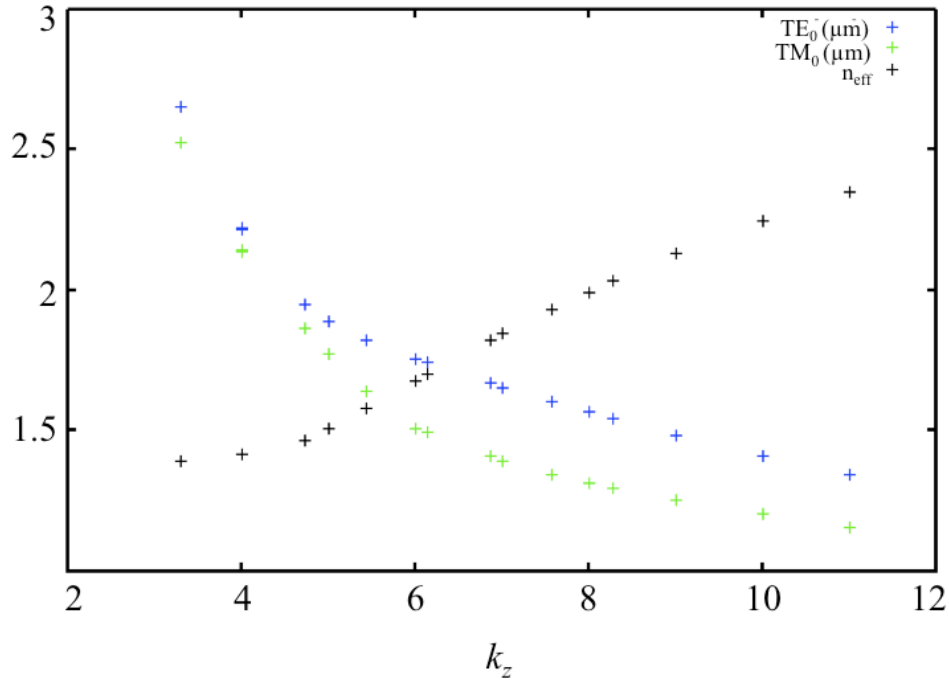


Figure 1.4: Results of a typical mode solve for an SOI silicon waveguide with geometry 400 nm x 200 nm.

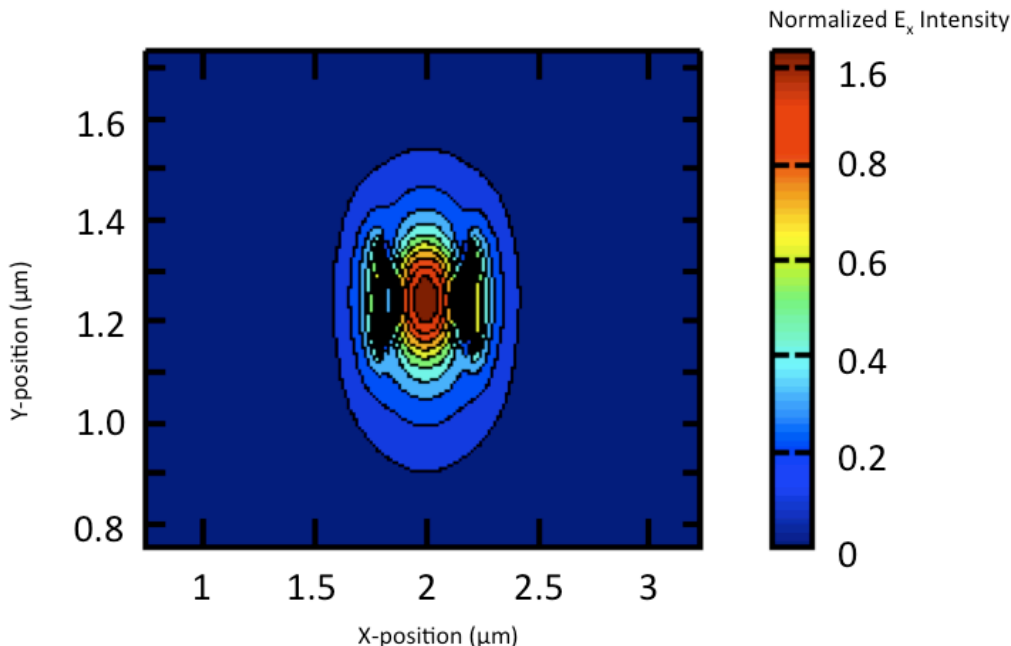


Figure 1.5: Illustrative mode profile of the fundamental  $TE_0$  mode of a 400 nm x 200 nm silicon waveguide on an SOI wafer without cladding.

## Organization of this Work

This technical content of this thesis is derived from works published in peer-reviewed journals. The most relevant publications are referenced at the end of this chapter. Generally, this work is organized into two categories: (1) photonic library development, and (2) system design. As is implied, the effort developing individual optical devices is leveraged to construct a larger system based on the smaller optical building blocks.

At the device level, my work focused on novel grating-based optical coupling devices and in very high-speed modulators. Both of these devices are key components of any silicon photonic optical system. Chapter 2 discusses my work on a polarization-splitting bi-wavelength grating coupler. This is the first experimental demonstration of a grating coupler that is capable of coupling both polarizations of light in two wavelength bands simultaneously.<sup>1</sup> This functionality was enabled by a novel device geometry. Chapter 3 discusses a high-speed Mach-Zehnder modulator for 1.3  $\mu\text{m}$  light. This device was based on a 25 Gb/s Mach-Zehnder “first generation” modulator.<sup>2</sup> The improved modulator described in Chapter 3 was the first demonstration of an O-band Mach-Zehnder modulator operating at 50 Gb/s.<sup>3,4</sup> Chapter 4 presents further measurements of the “first-

generation” device for the purposes of RF analog optical applications. The results reported in this chapter are the first reported spur-free dynamic range measurements of an optical link using a silicon Mach-Zehnder modulator.<sup>5</sup> The silicon device exhibited a high linearity, which had been an outstanding question with depletion-mode optical modulators. These devices were integrated into a silicon photonic platform as part of the OpSIS multi-project wafer shuttle run service.<sup>6</sup>

Chapter 5 discusses a terabit optical link built on a silicon-photonic platform and utilizing components of the OpSIS PDK photonic component library. A 48-channel modulator and photodetector array are integrated on the same wafer and shown to operate at 50 Gb/s. Bit-error-rate measurements on the modulator array and eye diagrams on the receiver array show excellent uniformity.<sup>7</sup> The system demonstrates that large optical systems can be built in a silicon platform and reliably yield.

### **Papers Related to this Work**

Here is listed a list of the most relevant papers to this work. A full publication list may be found in the Vita at the end of this thesis.

1. **M. Streshinsky**, R. Shi, A. Novack, R. Tern Poh Cher, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, “A compact bi-wavelength polarization splitting grating coupler fabricated in a 220 nm SOI platform,” *Optics Express*, vol. 21, no. 25, pp. 31019-31028, 2013.
2. T. Baehr-Jones, R. Ding, Y. Liu, A. Ayazi, T. Pinguet, N. C. Harris, **M. Streshinsky**, P. Lee, Y. Zhang, A. Eu-Jin Lim, T.-Y. Liow, S. Hwee-Gee Teo, Guo-Qiang Lo, and M. Hochberg, "Ultralow drive voltage silicon traveling-wave modulator." *Optics Express*, vol. 20, no. 11, pp. 12014-12020, 2012.
3. **M. Streshinsky**, R. Ding, Y. Liu, A. Novack, Y. Yang, Y. Ma, X. Tu, E. K. S. Chee, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, “Low power 50 Gb/s silicon traveling wave Mach-Zehnder modulator near 1300 nm,” *Optics Express*, vol. 21, no. 25, pp. 30350-30357, 2013.

4. **M. Streshinsky**, R. Ding, A. Novack, Y. Liu, X. Tu, A. E.-J. Lim, E. K. S. Chen, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "50 Gb/s Silicon Traveling Wave Mach-Zehnder Modulator near 1300 nm," *Opt. Fiber Comm. Conference* (San Francisco, CA, 2014), paper Th2A.5.
5. **M. Streshinsky**, A. Ayazi, Z. Xue, A. Eu-Jin Lim, G. Qiang Lo, T. Baehr-Jones, M. Hochberg, "Highly Linear Silicon Traveling Wave Mach-Zehnder Carrier Depletion Modulator Based on Differential Drive," *Optics Express*, vol. 21, no. 3, pp. 3818-3825, 2013
6. **M. Streshinsky**, A. Novack, Y. Liu, R. Ding, M. Gould, T. Baehr-Jones, Q. Li, Y. Yang, Y. Ma, Y. Zhang, K. Padmaraju, K. Bergmen, A. E.-J. Lim, G.-Q. Lo, and M. Hochberg "A 30 GHz Silicon Photonic Platform: Multi-Project Wafer Shuttles for Next-Generation Optical Systems," in *IEEE Photonics Society Summer Topical Meeting Series* (Waikoloa, HI, 2013), pp. 225-226.
7. **M. Streshinsky**, A. Novack, R. Ding, Y. Liu, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Silicon nanophotonic parallel single mode 48×50 Gb/s transmitter and receiver," *IEEE J. Lightw. Technol.*, vol. 32, no. 22, pp. 3768-3775, 2014.

## Chapter 2. Grating Couplers with Integrated Wavelength and Polarization Filtering

In this chapter, I discuss my work on a novel grating coupler device to simultaneously couple two distant wavelength bands and all polarizations of input light. This device directly addresses the two most challenging problems with using grating couplers in systems: narrow bandwidths and polarization sensitivity. The device could have uses in coarse wavelength-division multiplexed optical systems, such as fiber-to-the-home. I performed the design, simulation, layout, and majority of the testing of the device. Ruizhi Shi assisted with simulations after the device was tested to confirm the operating principle. Ari Novack assisted in the device testing. This work has been published in *Optics Express*:

**M. Streshinsky**, R. Shi, A. Novack, R. Tern Poh Cher, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, “A compact bi-wavelength polarization splitting grating coupler fabricated in a 220 nm SOI platform,” *Optics Express*, vol. 21, no. 25, pp. 31019-31028, 2013.

### 2.1. Grating Couplers for Integrated Optical I/O

One of the fundamental challenges for integrated optics is the design and fabrication of a device to efficiently couple light from a fiber optic mode into an on-chip waveguide mode. In silicon, there are two preferred methods: butt-coupling a fiber into an edge coupler in the plane of the chip, or orienting the fiber vertically with respect to the top surface of the chip into a grating coupler. In both of these cases, some method is required for the mode conversion from an up-to 15  $\mu\text{m}$  fiber mode to a single  $\mu\text{m}$ -scale waveguide mode.

For edge couplers, there are several methods to achieve this mode conversion. For example, it is possible to use an adiabatic taper from narrow single-mode waveguides to very wide multi-mode waveguides that have a horizontal modal diameter close to the fiber optic mode. However, in this method the vertical mode diameter actually decreases with increasing waveguide width, and so efficient fiber coupling is impossible. Instead, an adiabatic taper to very a very small waveguide, near to 0.1  $\mu\text{m}$  wide, reduces the horizontal and vertical optical confinement and

enables mode matching [STW<sup>+</sup>02, APL03]. The optical chip is then either diced very accurately or a deep trench etch near the edge coupler is performed to enable the nearby placement of a fiber.

More complicated fiber edge-coupling schemes have also been reported in the literature. By using a grayscale mask, tapers that expand in 2-dimensions are possible with materials that are still compatible with CMOS processing [SDM<sup>+</sup>03]. Starting with a thicker silicon substrate and performing an etch to define the photonic device layer enables coupling from the fiber to tall silicon waveguides, and then to the vertically thin waveguides [DHT06]. However, even well-controlled silicon etches will introduce significant variability into the optical device performance.

In contrast to edge couplers, grating couplers typically exhibit higher insertion losses with narrower optical bandwidths. However, despite the decreased performance there are several motivations for the use of grating couplers for on-chip integrated photonics. Grating couplers ease optical routing constraints by enabling I/O to be placed at relatively arbitrary points on the surface of the chip. They also enable a much larger total coupling density since there is significantly more surface area on the top of the chip than along the edge of the chip. This advantage can be realized, for example, when moving towards spatial division multiplexed optical fiber [KPW<sup>+</sup>14]. Vertical coupling also enables devices and systems to be tested at the wafer-scale, rather than the device scale. Thus, high efficiency grating couplers are of immense use to the photonics designer.

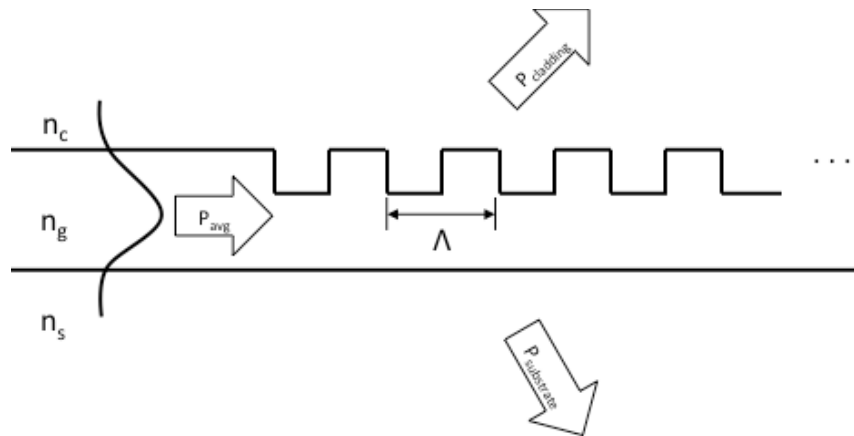


Figure 2.1. Illustrative cross-section of a grating coupler.

As previously mentioned, a grating coupler is a device that works for specific wavelengths and polarizations. In addition, the grating is also sensitive to input angle. Light that is in the correct passband, polarization, and angle will be diffracted into the waveguide mode, while light outside these parameters will pass through the grating. Simple gratings can be easily analyzed using the Bragg condition. Consider Figure 2.1, a 2-dimensional periodic series of gratings. Light in the waveguide mode enters the grating, and a certain amount is diffracted up and down. In this scenario, the relationship between the two propagating modes in the waveguide and cladding satisfy the Bragg condition:

$$k_0 \sin(\theta) = \frac{2\pi n_{eff}}{\lambda_0} - m \frac{2\pi}{\Lambda} \quad (2.1)$$

where  $k_0$  is the freespace wavenumber,  $\theta$  is the angle of vertically scattered light,  $n_{eff}$  is the effective index of the waveguide mode,  $m$  is an integer, and  $\Lambda$  is the period of the gratings. Thus, a method to diffract light vertically can be designed and optimized based on the simple geometry of the grating structure. Standard single-polarization grating couplers have been demonstrated in an SOI platform to couple a single polarization state into a waveguide mode with losses as low as 1.2 dB using an apodized grating coupler [CLF<sup>+</sup>10].

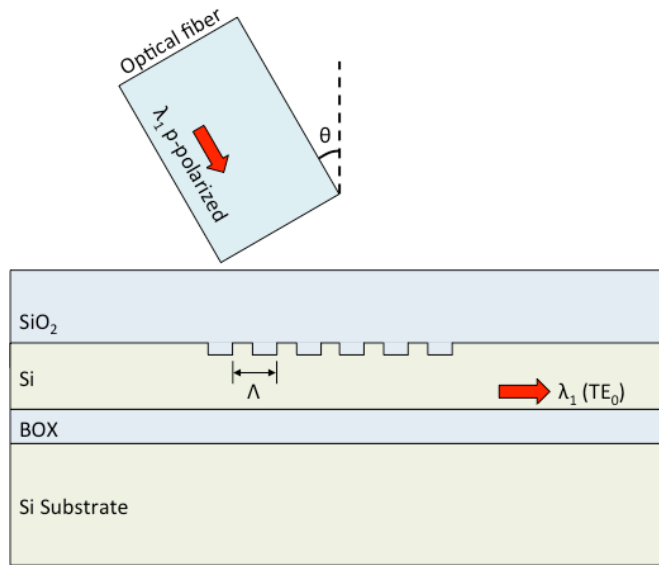


Figure 2.2. Illustration of a 1-dimensional single-polarization single-wavelength grating coupler.

Further, the above analysis typically assumes a 1-dimensional grating coupler. That is, the position of the gratings along the z-axis is described completely by the z-location along the grating and the pitch. Such a device is realizable in practice by using a wide grating coupler and adiabatically tapering to the desired waveguide size after the grating coupler. In order to conserve space by obviating the need for long adiabatic tapers, the gratings can be arranged into a focusing shape. One simple assumption to make is that the wavefronts above the grating in the substrate are circular. If the wavefronts impinge upon the grating at an angle,  $\theta$ , then the resulting profile is that of a series of elliptical wavefronts. In this way, familiar equations that describe ellipses can be used, and the gratings along the z- and x-axes are then defined by:

$$z(x)^2 = \frac{\gamma^2 + 1}{(1 + \gamma^2)^2} z_0^2 + \frac{1}{\gamma^2 - 1} x^2$$

where  $z_0$  is the position of the grating at position  $x = 0$ . The eccentricity of the ellipses,  $\gamma$ , is calculated as  $\gamma = (n_c/n_{eff}) \cdot \sin(\theta)$ .

Coupling is not perfectly efficient due to a number of factors. First, unless care is taken to use an apodized grating, the vertically diffracted mode will be far from a Gaussian shape and thus incur mismatch loss to the fiber mode. Secondly, some power will be transferred to the substrate. The substrate coupling can be mitigated by designing the dielectric stack below the waveguides to reflect or by the inclusion of backside mirrors. Secondly, some power will also be diffracted downward into the substrate. Thirdly, back reflection can be a source of loss, but is mitigated by using a non-vertical fiber placement to eliminate the first-order back reflections. Also apparent from the Bragg condition above is the sensitivity of the coupling to both wavelength and polarization. Typically, grating-based devices are designed to operate for a single polarization and near a single wavelength. As will be discussed in the following sections, these two disadvantages can be addressed through additional design effort.

## 2.2. The Need for a Bi-Wavelength PSGC

Silicon, as a platform for integrated optics, has a large need for grating-based optical coupling, the advantages of which have been briefly mentioned in the preceding section. For experimental work, the polarization-dependence of the standard grating coupler is ideal for the on-chip polarization dependent behavior of most silicon devices. In standard 220 nm top-silicon thickness platforms, standard passive and active optical devices rarely perform equally well for

both polarizations. Additionally, even just waveguides that are symmetric in the horizontal and vertical directions (i.e.  $220 \text{ nm} \times 220 \text{ nm}$ ) are rarely used outside of edge coupler devices due to the very low confinement near telecom wavelengths. Instead, if the other polarization is desired, a polarization beam splitter and rotator are often used to convert orthogonal polarizations from the  $\text{TM}_0$  or higher modes into the  $\text{TE}_0$  mode while the optical signal is on the chip [GNS<sup>+</sup>14].

However, outside of the laboratory, it is critical to enable polarization-insensitive optical interfaces for robust communication. Polarization-maintaining fiber and polarization tracking systems are significantly more costly or limited in application than a simple optical link based on single-mode fiber. There have been several promising demonstrations of grating devices to couple from orthogonal polarization states [CCF<sup>+</sup>10, RVS<sup>+</sup>11]. Either 1-D or 2-D grating coupler designs are implemented in order to couple orthogonal polarizations into on-chip waveguides.

1-D polarization splitting grating structures operate by coupling incident light into a forward-propagating waveguide TE mode and reverse-propagating TM mode. In this scenario, the phase matching condition is satisfied at a single fiber angle, but with  $\theta_{\text{TM}} = -\theta_{\text{TE}}$ . Roelkens et al. have demonstrated a 1-D PSGC with transmission efficiency as high as 3 dB near 1310 nm and polarization-dependent losses less than 1 dB on a 220-nm SOI wafer with a polysilicon overlay [RVS<sup>+</sup>11]. A 1-D grating coupler with transmission efficiency near 1550 nm of 42% [WTZ<sup>+</sup>09] has also been demonstrated in 260 nm SOI. With the use of a backside metal mirror, Zaoui et al. have demonstrated a 1-D PSGC with 2.4 dB coupling efficiency in a 250 nm SOI platform [ZKV<sup>+</sup>13].

In contrast to 1-D PSGC structures, 2-D PSGCs couple light from orthogonal polarization states into the same waveguide mode. Taillert et al. first demonstrated such a device in 220 nm SOI with 20% coupling efficiency and less than 18 dB polarization cross talk near 1550 [TCB<sup>+</sup>03]. In 300 nm SOI, Meklis et al. demonstrated a 3.2 dB 2-D PSGC [MGM<sup>+</sup>11]. Unlike 1-D devices, 2-D designs are compatible with focusing techniques in order to reduce the overall device footprint, such as in the case of [MGM<sup>+</sup>11] and [vLBP<sup>+</sup>09].

There have also been alternative fabrication methodologies to produce polarization-splitting grating couplers. Feng *et al.* describe a two-layer SOI structure in which each layer is demonstrated to either couple TE or TM incident light with 50% efficiency [FZ07]. Xiao *et al.*

demonstrated a double-corrugated PSGC structure, in which gratings are added to both the top and bottom layers of the top-silicon layer [XLZ<sup>+</sup>12]. They achieved 55% efficiency near 1550.

Here, I will present a 2-D polarization splitting grating coupler. The single polarization device described earlier is modified to act as a polarization splitting device by superimposing two identical grating couplers rotated away from each other by 90°. Rather than continuous gratings, scattering elements are placed at the intersection points of the gratings of the two single-polarization grating couplers. The fiber is tilted along the axis of the bisector angle of the two output waveguides and the optical mode is tilted by 45°. Since the two overlaid grating couplers are oriented 90° from one another, they each couple orthogonal input polarization states from one another. Due to symmetry, the device will couple into the same waveguide mode for each input fiber polarization. Thus, the output of each waveguide will be a function of the input polarization state. Figure 2.3 shows a schematic illustration of the PSGC device.

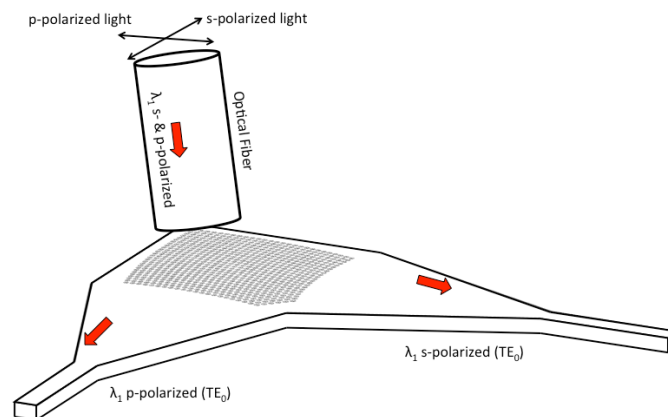


Figure 2.3. Illustration of a polarization-splitting grating coupler. Light is coupled into either waveguide depending on the input polarization state.

### 2.3. Bi-Wavelength Polarization Splitting Design

Silicon enables very high levels of integration in a CMOS-like fabrication flow that can scale to very large volume production. This platform capability enables silicon optical devices to hold promise for use in systems that may have been too costly or complex to package in other material systems. One such system may be future high-data rate WDM passive optical network (PON) solutions for fiber-to-the-home (FTTH). In several implementations of a WDM PON, such as IEEE 802.3av GPON, light near 1310 nm is chosen for the upstream band and light near 1550 nm may be used for downstream communication. In order to reduce costs in such a

system, it is desirable to use a single fiber and avoid expensive external modulators. Thus, silicon-based optical systems offer an attractive solution by potentially increasing integration density and reducing packaging complexity through integration of many components onto the same chip. One essential silicon component for such a system is the grating or edge coupler.

In similar vein to the extension of a single polarization grating coupler to a polarization splitting design, the same 1-D and 2-D topologies can be adopted for a bi-wavelength grating coupler. A 1-D device with efficiency as high as 2.5 dB has been demonstrated in the 1310 nm and 1490 nm bands [RVS<sup>+</sup>11]. A 2-D single-polarization grating coupler for the 1310 and 1490 nm bands with -7 and -8 dB loss, respectively, was also demonstrated [VRvT<sup>+</sup>09]. Finally, Xu et al. presented a 2-D bi-wavelength grating coupler for the 1490 and 1550 nm wavelengths with -6 and -6.5 dB insertion loss, respectively [CCF<sup>+</sup>10, XCL<sup>+</sup>11].

In addition to single grating coupler structures to duplex light, it is also possible to use a PSGC followed by a filter such as an arrayed waveguide grating to implement polarization-insensitive duplexing of light [BTD<sup>+</sup>07a, BTD<sup>+</sup>07b, PVD<sup>+</sup>12]. However, for systems such as FTTH where the upstream/downstream wavelengths are sufficiently spaced (for example, 1310 nm and 1550 nm), the limited bandwidth of a single-wavelength grating coupler will prevent the use of this type of solution. Roelkens et al. also presented a theoretical bi-wavelength polarization splitting grating coupler (PSGC) by overlaying two 1-D structures into a 2-D arrangement [RvTB07]. Doerr et al. presented one solution using the  $\Gamma$ -M and  $\Gamma$ -X axes of a photonic crystal structure, allowing for polarization insensitivity near 1270 nm while still allowing a single polarization of 1577 nm light to couple on chip [DCR<sup>+</sup>09]. Instead, here I will present a grating coupler device that is polarization insensitive and operates in both the 1550 and 1310 nm transmission windows.

The bi-wavelength PSGC consists of a symmetric lattice of scattering elements. An optical fiber is placed along the symmetry axis and tilted along this axis to reduce back reflection. The design process for this grating coupler can be broken down into two steps: The design of a single-polarization bi-wavelength grating coupler to define the grating pitch and duty cycle, and the overlap of two single-polarization devices in order to achieve a polarization splitting action.

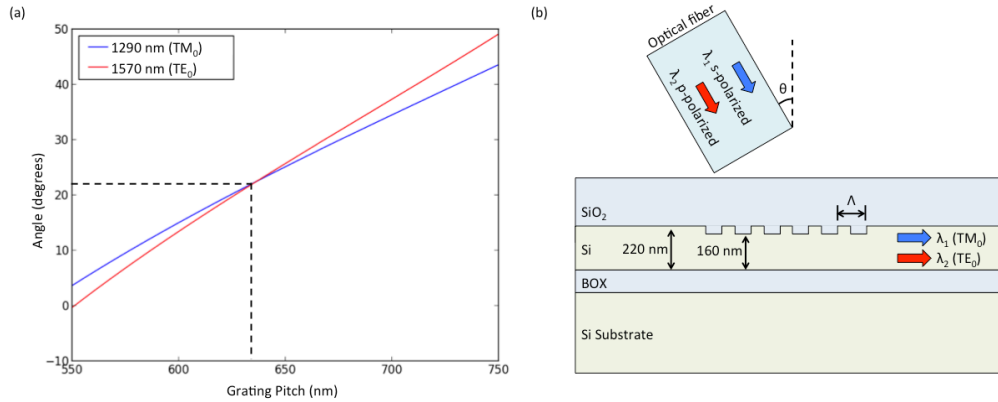


Figure 2.4: Design of a 1-D bi-wavelength grating coupler. (a) Phase matching condition for the TM<sub>0</sub> mode at 1290 nm and TE<sub>0</sub> mode at 1570 nm. The optimum grating pitch and fiber angle is 636 nm and 22.5°, respectively. (b) Schematic illustration of a 1-D device (not to scale).

In order to achieve bi-wavelength performance the angle of the fiber and the pitch of the gratings are adjusted to satisfy the above phase matching condition for 1550 and 1310 nm light. For 220 nm thick silicon, the effective indices of the 1550 TE<sub>0</sub> and 1310 TM<sub>0</sub> slab modes are very near one another: 2.85 and 2.41, respectively. This enables the phase matching condition to be met within achievable grating pitches and fiber angles. Solving Eq. 1 for these conditions at 1550 nm and 1310 nm yields an optimum grating pitch of 550 nm and fiber angle of 1.4°. These conditions are not ideal for two reasons. First, since a 550 nm grating pitch will yield features that are very close to the design rules of the process, this pitch may have problems yielding well-defined features. Secondly, the steep fiber angle may result in additional back-reflection. Instead, we have elected to design the device to couple light centered at 1570 nm and 1290 nm. Shown in Figure 2.4(a) is the phase matching condition for these wavelengths, where the optimum grating pitch and fiber angle is 636 nm and 22.5°, respectively. Note that since the fiber illuminates the device through a layer of oxide cladding, I have applied Snell's law to calculate the fiber angle.

Once the grating pitch and fiber angle has been selected for the single polarization device, the steps outlined previously may be used to build a focusing design, and enable polarization-splitting action. One thing to note in the polarization-splitting design, the overlap of two gratings can no longer be considered as simply a series of gratings. Instead, it is an array of scattering elements that are arranged in two dimensions. It is found that the shape of the scattering

elements has a large effect on polarization dependent losses. Thus, I have elected to use a rounded diamond-like pattern similar to that used in [MGM<sup>+</sup>11], which was found to perform better than purely circular scattering elements.

It is also important to note that since the fiber is no longer aligned to the output waveguide, there must be slight adjustments in the phase matching condition and the focusing design [MGM<sup>+</sup>11]. First, the parameter  $\phi$  in Eq. 1 is now  $\pi/4$  to account for the fiber orientation. This shifts the theoretical optimum fiber angle for this design to  $33^\circ$ . Secondly, the eccentricity of the focusing design now also has an additional factor of  $\sin(\pi/4)$ .

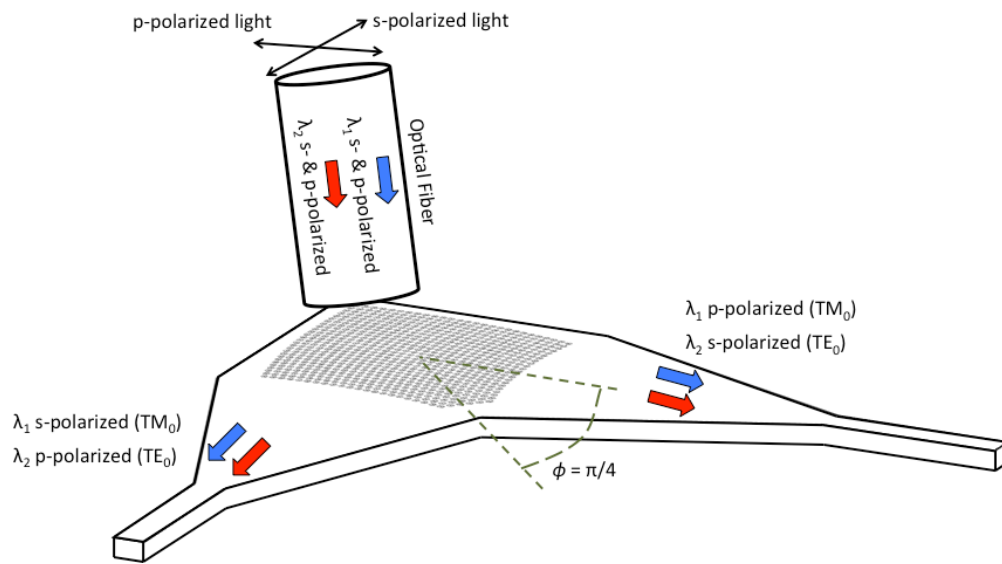


Figure 2.5. Schematic illustration of the bi-wavelength polarization splitting grating coupler (not to scale). Two sources in different wavelength bands and random polarizations are input into the fiber. Light in the first wavelength band is split according to polarization and coupled into the waveguide  $TM_0$  mode. Similarly, light in the second wavelength band is split according to polarization and coupled into the waveguide  $TE_0$  mode.

Figure 2.7 presents 3-D finite difference time domain (FDTD) simulations for the device performed in Lumerical FDTD. In the FDTD simulation, the grating coupler is illuminated by an optical fiber oriented along the symmetry axis of the device. Perfectly matched layer absorbing boundary conditions were used. Two simulations were performed—one where the electric field of the source is parallel to the output waveguide ( $TM_0$ -coupled), and the other where the electric field is perpendicular ( $TE_0$ -coupled). Coupling efficiency is measured from the fiber output to the waveguide  $TE_0$  and  $TM_0$  modes.

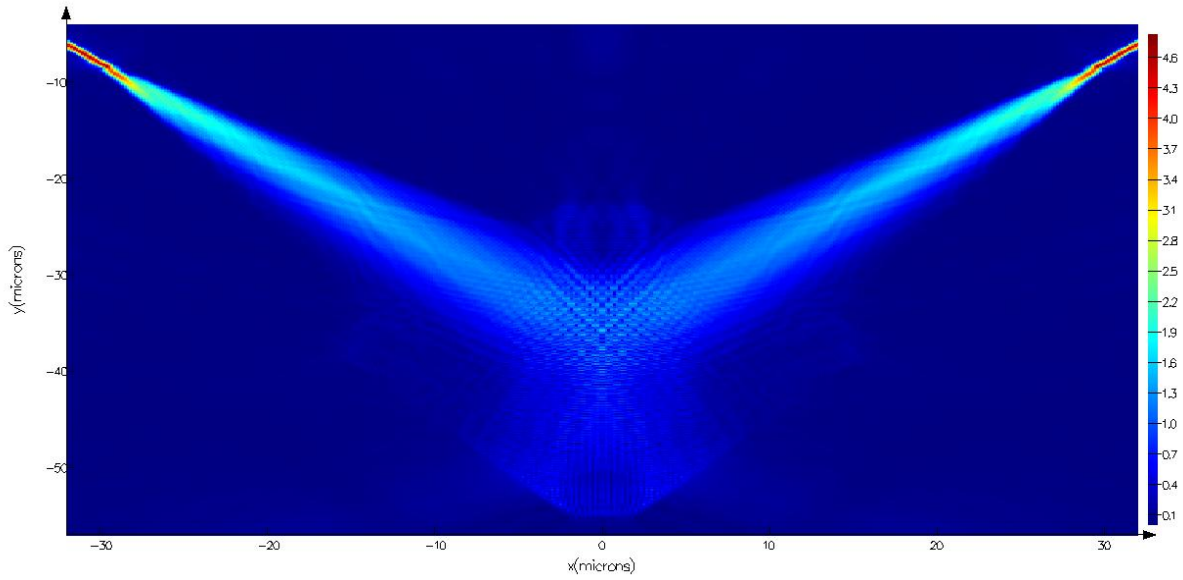


Figure 2.6. A cross-section of a 3-D FDTD simulation showing the electric field profile in the PSGC. Light enters vertically (into the page) in the center of the device and exits in the outer two waveguides (top left and top right).

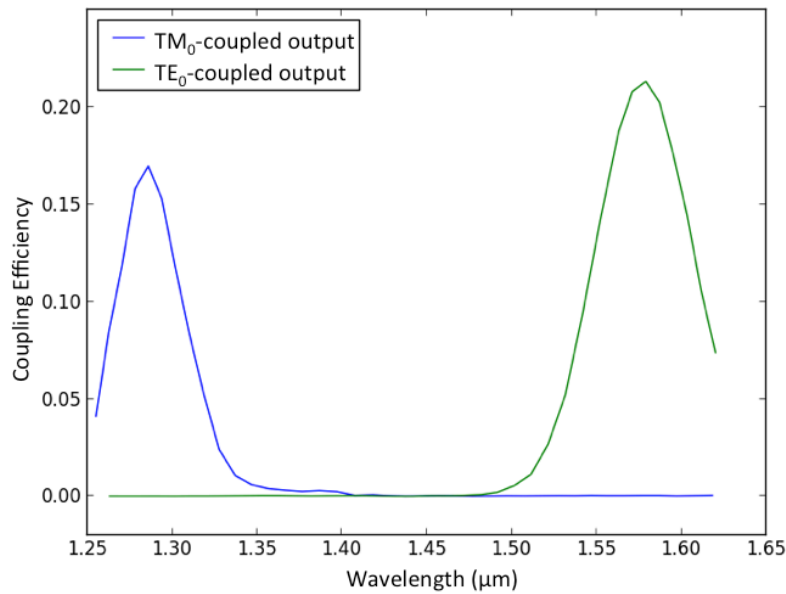


Figure 2.7. 3D FDTD simulation of the coupling efficiency of the PSGC. Light in the wavelength band near 1.3 μm couples into the waveguide TM<sub>0</sub> mode, while light in the 1.55 μm band couples into the waveguide TE<sub>0</sub> mode.

Fabrication of these devices was performed at the Institute of Microelectronics (IME), A\*STAR, Singapore [LAF<sup>+</sup>10] in a multi-project wafer run through the OpSIS foundry service [ops]. The starting material was a 200 mm SOI wafer with 220 nm top silicon and 2  $\mu\text{m}$  buried oxide thicknesses. First, a 60 nm etch was performed to define the grating trenches. Subsequent etch steps removed the unwanted silicon in order to define the output ridge waveguides and output taper. Lastly, 2.1  $\mu\text{m}$  of oxide was deposited on top of the wafer. In all cases, 248 nm lithography was used. Figure 2.8 shows an optical micrograph of the fabricated device as well as a rendering of a section of the device layout.

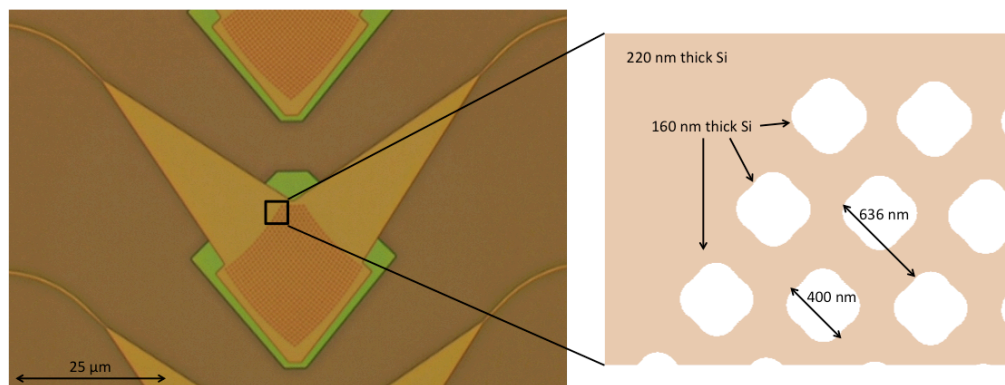


Figure 2.8. Optical micrograph image of the fabricated device. Inset is a rendering of a section of the device layout. The scattering elements consist of rounded diamond-like 60 nm deep trenches in the 220 nm top silicon layer.

In order to efficiently test the device, an array of polarization maintaining (PM) fibers with a pitch of 127  $\mu\text{m}$  was used. The fast and slow axes of the PM fiber were oriented at a 45° angle in order to test the efficiency of a single polarization channel at a time. The fiber array arrangement is shown in Figure 2.9(a-c). The test setup and circuit arrangement shown in Figure 2.10(a, b) is designed to correspond to this fiber array. In this circuit, light is input into the center device and output from identical devices on the left and right. The wavelength and input polarization is varied and the corresponding output on the outer two grating couplers is measured.

In order to first align the fiber array to the device, the fiber array position is swept across the surface of the device and then moved to the position of maximum power transmission. At this point, no further positions of either the device or the fiber array are changed in order to measure polarization-dependent loss as well as wavelength-dependent loss. To test PDL, an Agilent

8169A polarization controller is placed before the input fiber in the fiber array and an internal half-wave plate is used to vary the input polarization state into the center PSGC. The output is measured from the two output PSGCs at each input polarization.

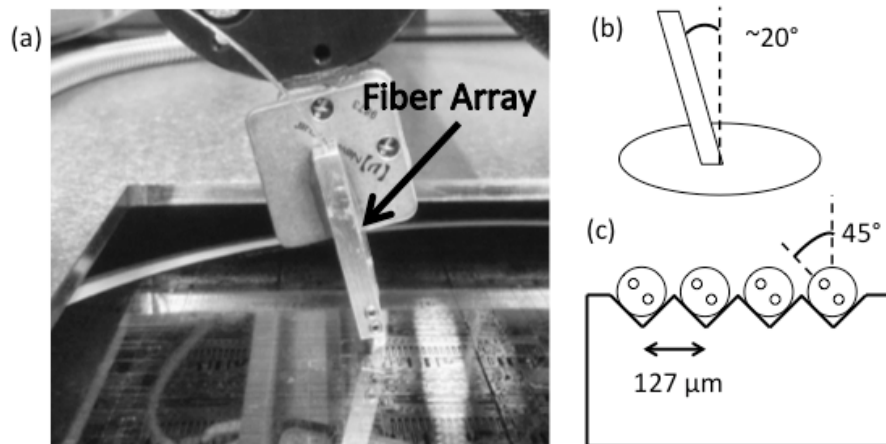


Figure 2.9: Fiber array testing apparatus. (a) An array of polarization-maintaining fiber from PLC Connections is mounted above the wafer. (b) The grating coupler is designed for a fiber angle of 23°. (c) The fibers are mounted such that the fast and slow axes are rotated 45° from vertical.

## 2.4. Experimental Results

The performance of the device is shown in Figure 2.12. Maximum transmission is measured to be -7.1 dB at 1576 nm and -8.2 dB at 1296 nm. The -1.5 dB transmission windows are 18 nm and 35 nm for light near 1310 and 1550, respectively. Within the -1.5 dB window, the difference in transmission between s-polarized light and p-polarized light is less than 1 dB for both wavelength bands.

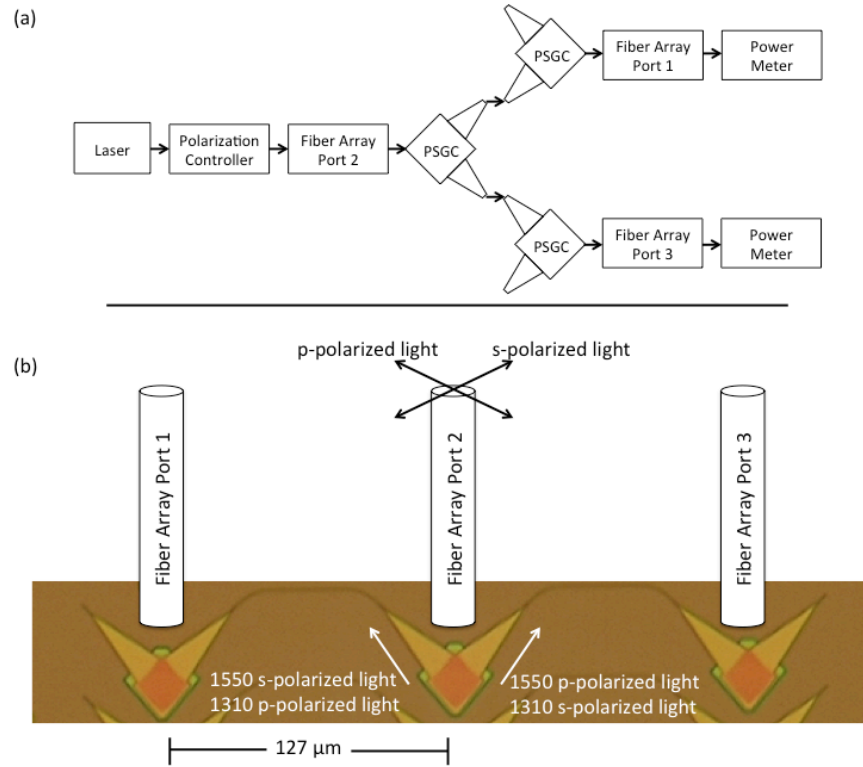


Figure 2.10: (a) Schematic block diagram of test setup. (b) Optical micrograph of test cell to extract device performance with a schematic illustration of the test setup overlaid. Light is launched into the center grating coupler and the output is measured from the left and right couplers.

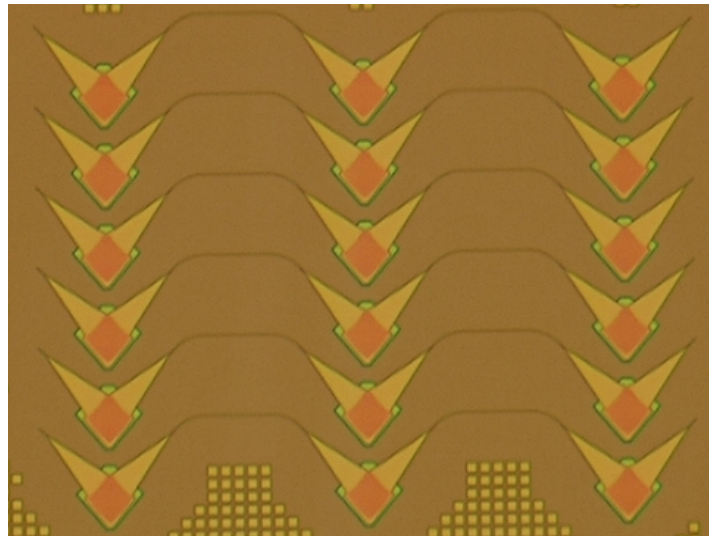


Figure 2.11. Optical micrograph image of a collection of PSGC test cells.

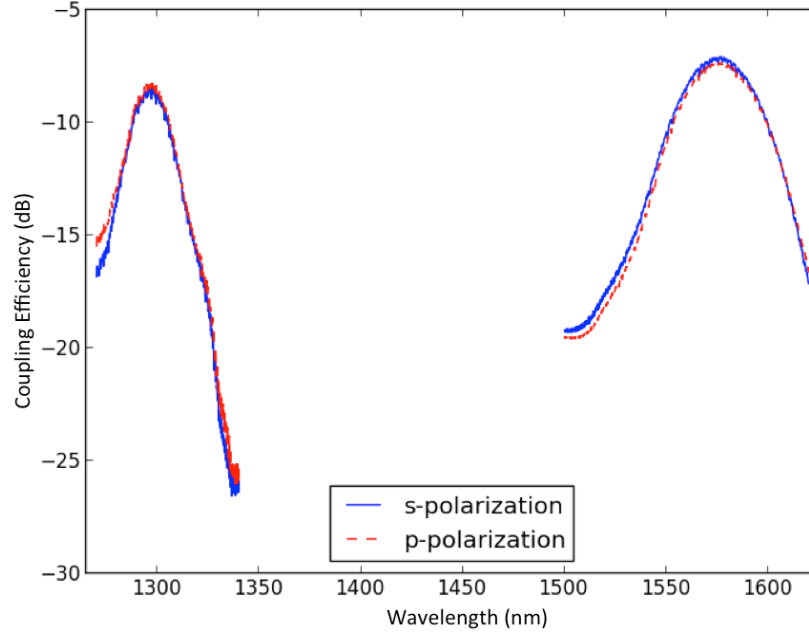


Figure 2.12: Measured transmission spectrum of the device. Maximum transmission of -8.2 and -7.1 dB is observed for the wavelength bands near 1300 nm and 1550 nm, respectively.

Polarization dependent loss (PDL) measurements at 1550 nm are shown in Figure 2.13. A similar test was performed at 1310 nm. PDL at 1550 nm is 1.06 dB, while PDL at 1310 nm is measured to be 5.6 dB. It is also possible to extract a lower bound for polarization isolation from PDL measurements. In the worst case, PDL is due entirely to interference between the desired polarization and undesired coupling from the opposite polarization. In this situation, the swing in total power will be the difference between the cases where the desired and undesired fields inside the output waveguide add constructively and destructively. Therefore, based on the PDL measurements, the minimum polarization isolation is found from the relationship:

$$PDL = 2 \cdot 20 \log_{10} \left( 1 + 10^{\frac{P_{isolation}}{20}} \right) \quad (3)$$

With 1.06 dB PDL at 1550 nm, this corresponds to a polarization isolation of 24 dB. Similarly, polarization isolation at 1310 nm is calculated to be 8.4 dB. Since there may be other sources of PDL, this calculation understates the polarization isolation for linearly polarized light.

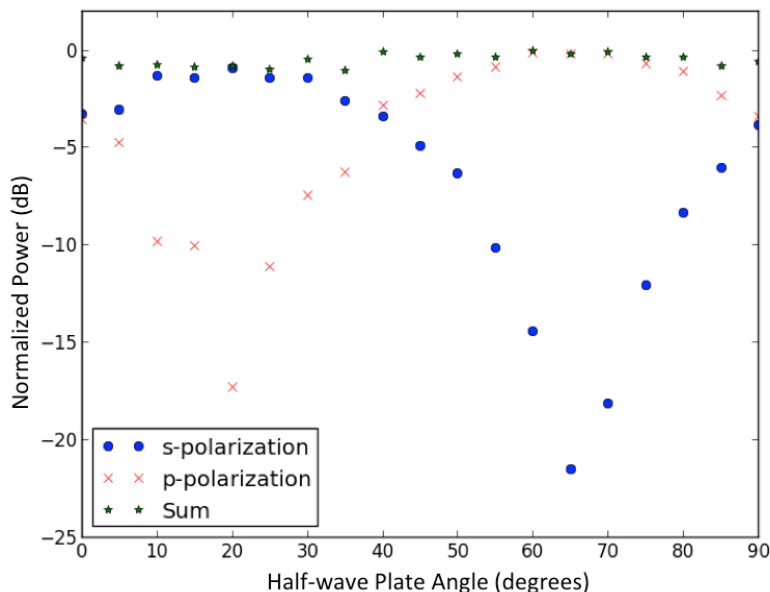


Figure 2.13: Polarization dependent loss near 1550 nm is less than 1.06 dB.

## 2.5. Conclusions

There are several design parameters that may be changed in order to improve polarization isolation. The large tilt angle of approximately  $20^\circ$  is likely the root cause of PDL in this device [vLBP<sup>+</sup>09]. By choosing wavelengths nearer to 1310 nm and 1550 nm, the optimum fiber angle would be closer to vertical. Introducing a  $\pi$  phase shifter in one of the output waveguides has also been shown to improve PDL [HVR10]. Furthermore, as noted in [MGM<sup>+</sup>11], the shape of the scattering element also has a large impact on polarization dependence. Meklis et al. found that purely circular scatterers performed much worse than the rounded diamond-like pattern that is used in both of these works. It is likely that further experiments with the device geometry are necessary in order to find a shape that effectively isolates in both wavelength bands.

There are also several design parameters that may improve coupling efficiency. FDTD simulations (see Figure 2.14) of the device predict that 59% of the power is lost due to coupling into the substrate at 1570 nm. This is significantly higher than the typical 35-45% substrate coupling in standard grating couplers [VVL<sup>+</sup>10]. Thus, to improve coupling efficiency, substrate coupling should be addressed first. Two solutions that have been demonstrated in literature to decrease this substrate coupling are a polysilicon overlay [WTZ<sup>+</sup>09] and a backside metal mirror

[ZKV<sup>+</sup>13]. Additionally, a thicker top-silicon thickness substrate may be used to improve directionality of the gratings [CLF<sup>+</sup>10]. Finally, changing the lithographic exposure from 248 nm to 193 nm would enable much sharper features. In particular, smaller features would enable the coupling of light that is closer to 1550 nm and 1310 nm, rather than near 1570 nm and 1290 nm. While current losses are high compared to single wavelength PSGCs or bi-wavelength single polarization grating couplers, it is expected that with further optimization this type of device may prove useful for telecommunication systems such as FTTH PON networks.

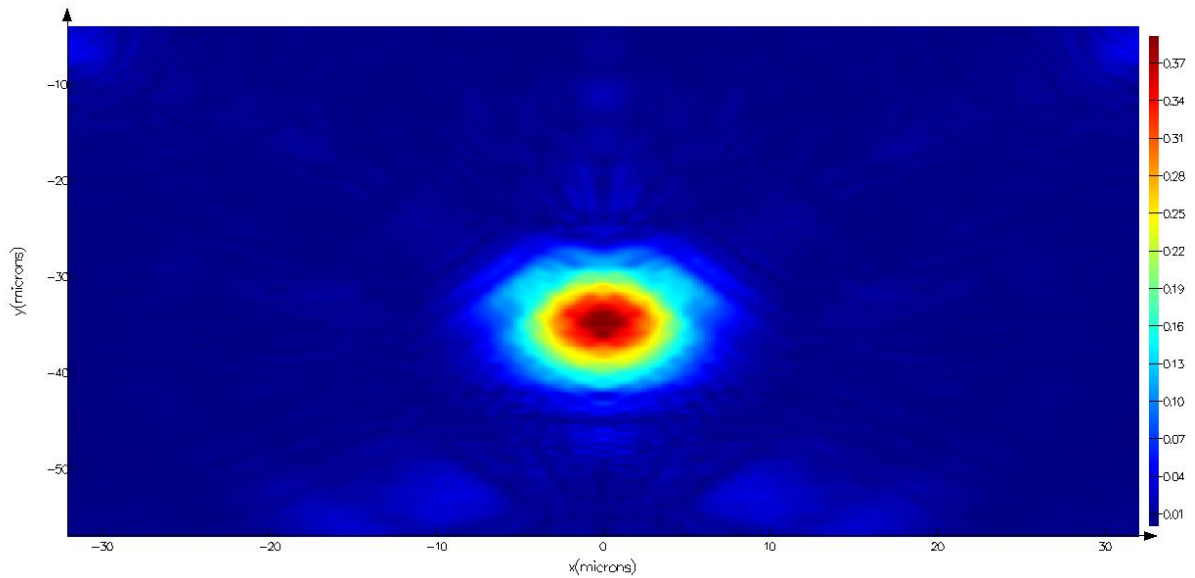


Figure 2.14. E-field cross-section of a 3-D FDTD simulation showing the light transmitted through the PSGC and into the substrate.

## Chapter 3. High-Speed Silicon Traveling Wave Mach-Zehnder Modulators

This chapter discusses a silicon Mach-Zehnder modulator for 1.3  $\mu\text{m}$  light operating at 50 Gb/s. Mach-Zehnder modulators form the basis for most modern telecommunications, and demonstrating high-speed and low-voltage modulators in silicon is a critical step to bringing silicon photonics into real-world applications. The device presented in this chapter is an improved version of a previously published device operating at 25 Gb/s. I performed DC and RF testing on the original device and this improved device. I also assisted with RF analysis on the original device; extracting RF index, impedance, losses and transmission line inductance and capacitance. I also assisted with the design and performance predictions for the second-generation device. Yang Liu designed the implant recipes and also performed performance predictions. Ran Ding designed the transmission lines in HFSS. This work was previously published in *Optics Express*:

M. Streshinsky, R. Ding, Y. Liu, A. Novack, Y. Yang, Y. Ma, X. Tu, E. K. S. Chee, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Low power 50 Gb/s silicon traveling wave Mach-Zehnder modulator near 1300 nm," *Optics Express*, vol. 21, no. 25, pp. 30350-30357, 2013.

### 3.1. Achieving Phase Shift in Silicon

While passive optical devices built in silicon enable novel functionality, the chief advantage of a silicon photonics platform is the capability of highly integrated active optical devices operating at high speeds. Unfortunately, the optical properties of pure silicon show very small nonlinearities relative to other materials, most notable of which is lithium niobate. In the well-regarded paper by Soref and Bennett in 1987, they quantify the electro-optic properties of ion-implanted silicon (carrier refraction). They predicted effective carrier-depletion based phase modulators on the order of millimeters using commonly available implantation doses [SB87]. Since then, many demonstrations have

followed demonstrating the carrier-depletion based silicon modulators predicted by Soref and Bennett at GHz speeds [LFL+04].

Simplistically, the fundamental effect in a carrier depletion modulator is that silicon with varying carrier concentrations will have varying band structure, resulting in different levels of interband and intraband (free-carrier) absorption. As is well known, a change of absorption must be accompanied by a change in refractive index, as governed by the Kramers-Kronig dispersion relationship. Thus, by varying the carrier concentration within a silicon waveguide, it is possible to modulate the optical path length of the device.

To first order, the change in refractive index due to free-carrier absorption can be predicted by the Drude model [HLB81]. The Drude model begins from a simplistic equation of motion for a charged particle under a time varying electric field (e.g. varying at an optical frequency):

$$m \frac{dv}{dt} + \frac{m}{\tau} v = eE \quad (1)$$

where  $\tau$  is the mean free time between ionic collisions. Under a sinusoidal input  $E = E_0 e^{-i\omega t}$ , there is the solution  $v = v_0 e^{-i\omega t}$ , and the above equation becomes:

$$\left(-im\omega + \frac{m}{\tau}\right) v_0 = eE_0 \quad (2)$$

To derive conductivity, relate a current density,  $J$ , with the drift velocity  $v_0$  so that we have  $J = nev_0$ , where  $n$  is the carrier density. Substituting this into Eq. 2, and solving for conductivity, we then have:

$$\sigma = \frac{ne^2\tau}{m(1 - i\omega\tau)} \quad (3)$$

And the complex permittivity is:

$$\varepsilon(\omega) = \varepsilon_0 + \frac{4\pi i}{\omega} \sigma = \varepsilon_0 + \frac{4\pi i}{\omega} \frac{ne^2\tau}{m(1-i\omega\tau)} \quad (4)$$

Writing the contributions from holes and electrons separately yields the following:

$$\varepsilon = \varepsilon_0 + \frac{4\pi e^2 i}{\omega} \left( \frac{n_h e^2 \tau_h}{m_h (1 - i\omega\tau_h)} + \frac{n_e e^2 \tau_e}{m_e (1 - i\omega\tau_e)} \right) \quad (5)$$

For optical frequencies, typically  $\omega\tau \gg 1$ , thus, the above can be approximated as:

$$\begin{aligned} \varepsilon(\omega) &= \varepsilon_0 + \frac{4\pi i ne^2\tau(1+i\omega\tau)}{\omega m(1+(\omega\tau)^2)} \\ \Rightarrow \varepsilon(\omega) &\approx \varepsilon_0 + \frac{4\pi i ne^2\tau(1+i\omega\tau)}{\omega m\omega^2\tau^2} = \varepsilon_0 - \frac{4\pi ne^2}{m\omega^2} + i \frac{4\pi ne^2}{m\omega^3\tau} \end{aligned} \quad (6)$$

Since we are interested in the index of refraction and absorption coefficient, it is convenient to relate the permittivity to the complex index of refraction:

$$\begin{aligned} \varepsilon_1(\omega) &= n^2(\omega) - k^2(\omega) \\ \varepsilon_2(\omega) &= 2n(\omega)k(\omega) \end{aligned} \quad (7)$$

For a semiconductor material where  $n \gg k$ :

$$\begin{aligned} n^2(\omega) - k^2(\omega) &\approx \varepsilon_0 \\ \Rightarrow 2n(\omega)k(\omega) &\approx 2\sqrt{\varepsilon_0}k(\omega) = \frac{4\pi ne^2}{m\omega^3\tau} \end{aligned} \quad (8)$$

And the absorption coefficient is then:

$$k(\lambda) = \frac{2\pi n e^2}{m\sqrt{\epsilon_0}c \left(\frac{2\pi c}{\lambda_0}\right)^3 \tau}; \quad \alpha(\lambda) = \frac{2\pi k}{\lambda_0} \quad (9)$$

Thus, the change in intra-band free carrier absorption, or, the plasma dispersion effect, is approximately proportional to the square of wavelength and linear with changes in carrier concentration:

$$\begin{aligned} \Delta n &= -\left(\frac{e^2 \lambda_0^2}{8\pi^2 c^2 \epsilon_0 n}\right) \left(\frac{n_e}{m_e} + \frac{n_h}{m_h}\right) \\ \Delta \alpha &= \left(\frac{e^3 \lambda_0^2}{4\pi^2 c^3 \epsilon_0 n}\right) \left(\frac{n_e}{m_e^2 \mu_e} + \frac{n_h}{m_h^2 \mu_h}\right) \end{aligned} \quad (10)$$

Here,  $e$  is the electron charge,  $\lambda_0$  is the freespace wavelength,  $n$  is the refractive index of unperturbed material,  $m_e$  is the effective mass of electrons,  $m_h$  is the effective mass of holes,  $\mu_e$  is the electron mobility, and  $\mu_h$  is the hole mobility.

As is noted by Soref and Bennett, there are three primary optical interactions occurring with crystalline-silicon under varying carrier concentrations: free-carrier absorption, Burstein-Moss bandfilling, and Coulombic interactions. All three interactions will occur simultaneously. In Burstein-Moss bandfilling, the energy between the top of the valence band and bottom of the conduction band shifts with doping level. An n-type material will experience an upward shift in Fermi level (blocking absorption/blue shift), while a p-type material will shift the Fermi level downwards towards the valence band (increasing absorption/red shift) [P71]. Coulombic interactions, in comparison, are where ionized impurities reduce the electron and hole mobilities of free carriers. The reduced mobility can result in a higher rate of absorption (red-shifting the absorption spectrum). Since the overall affect on absorption with donor implantation is a red shift, Coulombic interactions must dominate over the Burstein-Moss effect.

Due to these interactions, the absorption spectrum of silicon shifts with different implantation conditions. At the time of Soref and Bennett's paper, there was significant

work in characterizing the optical absorption under a variety of carrier concentrations found in semiconductor processing ( $\sim 10^{16}$  to  $10^{20}$ ). The well-known Kramers-Kronig relationship can be used to derive refractive index changes from absorption data. The relationship relates the real and imaginary parts of any causal complex function.

$$n(\omega) = \frac{c}{\pi} \text{P} \int_0^{\infty} \frac{\Delta\alpha(\omega') d\omega'}{\omega'^2 - \omega^2} \quad (11)$$

With this relationship, Soref and Bennett performed a simple numerical integration on the existing absorption data published in literature. Note that although the integral extends over all frequencies, as  $\omega' \gg \omega$ , the integrand quickly approaches zero. In this way, relatively accurate predictions can be made about local frequency phenomena without requiring extensive data.

In their 1987 paper, Soref and Bennett derived the following relationships for carrier refraction at 1550 nm:

$$\Delta n = \Delta n_e + \Delta n_h = -[8.8 \times 10^{-22} (\Delta N_e)^{1.04} + 8.5 \times 10^{-18} (\Delta N_h)^{0.818}] \quad (12)$$

where  $N_e$  and  $N_h$  are the carrier densities of electrons and holes in units of  $\text{cm}^{-3}$ . Comparing this relationship to the expectations from the Drude model, the Drude model predicts that a change in electrons should be 0.66 times as effective as a change in holes, whereas the equation above finds the opposite: a change in electrons are 3.3 times as effective as a change in holes. Furthermore, the empirically derived result also found a  $x^{0.8}$  exponential relationship between index and hole carrier concentration, whereas the Drude model predicts a linear relationship.

The empirical relationships between carrier concentration, refractive index, and absorption have since been refined and updated. At 1550nm, the most recently reported results list the following relationship [NSM11]:

$$\Delta n = \Delta n_e + \Delta n_h = -[5.4 \times 10^{-22} (\Delta N_e)^{1.011} + 1.5 \times 10^{-18} (\Delta N_h)^{0.838}] \quad (13)$$

It is interesting to note that since a change in hole concentration has a stronger effect on index shifts and a weaker effect on absorption relative to a change in electron concentration, it is preferred to primarily use holes to adjust the refractive index in modulator design.

The change in effective index of the optical mode in the waveguide can be calculated by integrating the change in the 2-dimensional geometry:

$$\Delta n_{eff} = \frac{\iint_S \Delta n(x, y) |E(x, y)|^2 dx dy}{\iint_S |E(x, y)|^2 dx dy} \quad (14)$$

where  $\Delta n(x, y)$  is the change in effective index and  $E(x, y)$  is the electric-field intensity as a function of spatial location in the waveguide mode (for z-propagating radiation). This integral is effectively a weighted average of the change in index by the relative optical power in the waveguide.

There are primarily three methods of varying the carrier concentration in a waveguide in order to enact modulation: carrier injection in a P-I-N diode, carrier accumulation in a Metal-Oxide-Silicon capacitor (or other type of capacitor), and carrier depletion in a PN diode.

In the first of these methods to achieve phase shift, a P-I-N diode is overlaid with a silicon waveguide, where the intrinsic region is located in the core of the waveguide, as shown below in Figure 3.1. Under a forward bias voltage, electrons and holes are injected through the intrinsic region. When the voltage is returned to zero, the free electrons and holes recombine. Thus, the bandwidth of this type of device is typically limited by the carrier recombination lifetime, which is on the order of tens of nanoseconds.

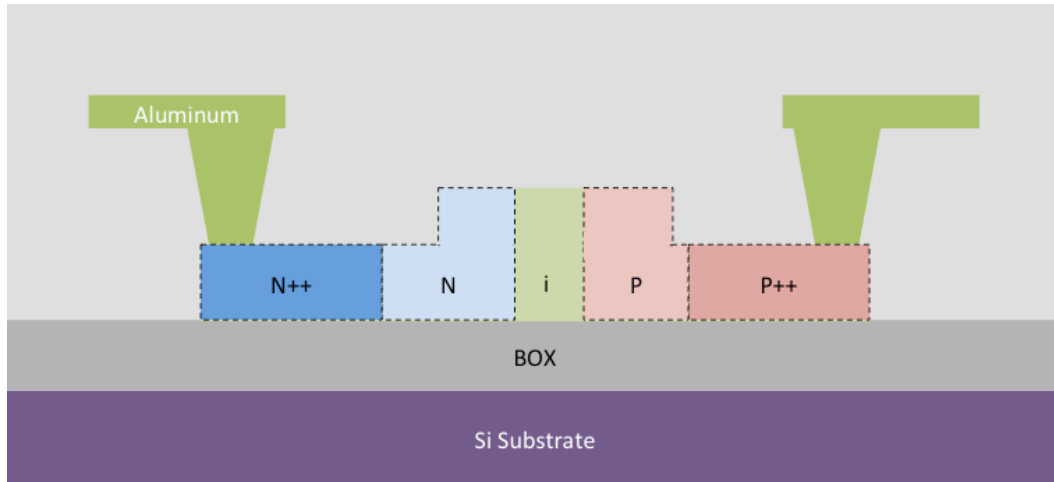


Figure 3.1. Example cross-section geometry of a carrier-injection based P-I-N diode.

The second type of modulation scheme uses carrier accumulation in the waveguide to modulate the refractive index. A CMOS-style thin gate oxide is grown directly above the core of the waveguide and a polysilicon gate is deposited above. This type of device has one major advantage over carrier depletion based approaches using a PN junction: the electro-optic effect is approximately linear. Additionally, the device is not limited by the recombination lifetime as in the carrier injection modulator. An example cross-section of such a device is shown in Figure 3.2.

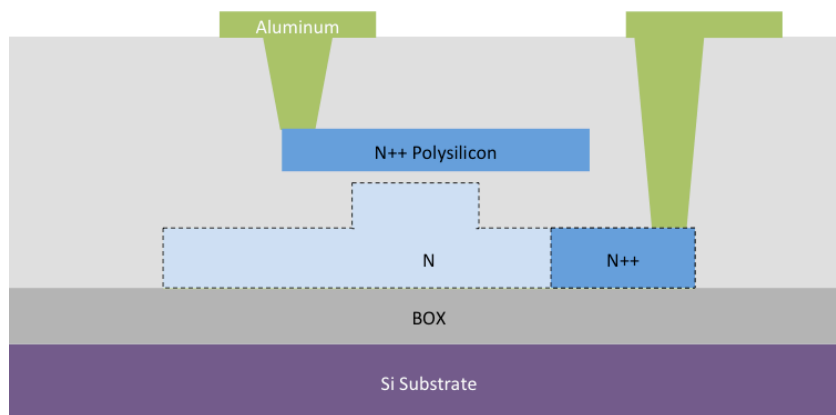


Figure 3.2: Example illustration of a carrier-accumulation type of modulator.

Lastly, a carrier-depletion based modulator uses a reverse-biased PN junction. By varying the reverse bias voltage on the junction the depletion width changes, which corresponds to a change in carrier concentration inside the waveguide. An example illustration is shown in Figure 3.3. The bandwidth of this type of device is typically limited by the RC time constant when driving from a  $50\ \Omega$  source impedance. Typical device capacitances are on the order of 0.1 to 1 pF, thus the RC-limited time constant may range from 3 to 30 GHz. The next section will discuss the traveling wave method to extend the bandwidth of this type of device.

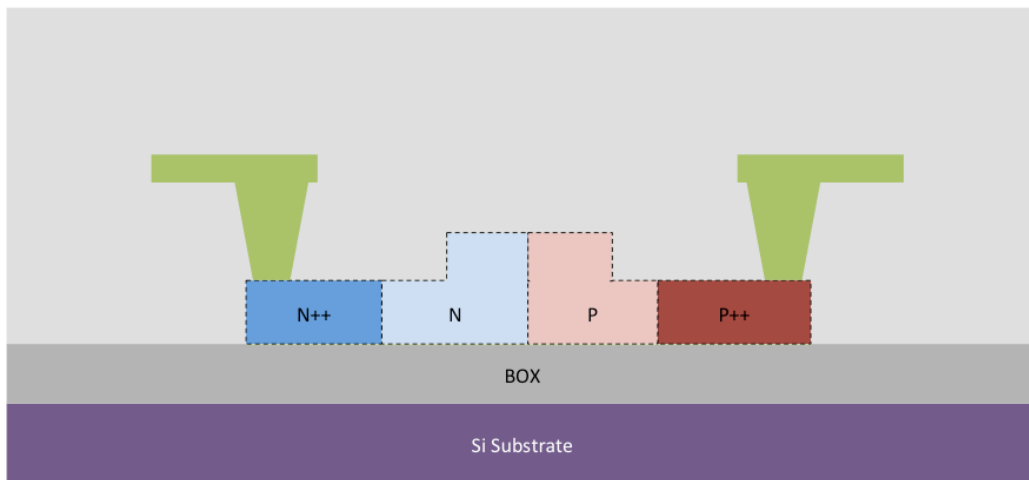


Figure 3.3: Example illustration of a carrier-depletion type modulator.

### 3.2. The Silicon Traveling Wave Mach-Zehnder Modulator

A common topography for modulators in silicon is the Mach-Zehnder interferometer. A simple schematic of this type of device is shown in Figure 3.4. This type of architecture is attractive for use as a planar integrated intensity modulator. The change in optical path length,  $\Delta L$ , can be realized with a carrier-depletion waveguide phase shifter. If the remaining paths are closely balanced, then the modulator is relatively temperature insensitive, as temperature changes affects both arms of the interferometer equally. Furthermore, the bandwidth of the modulator is only limited by the phase shift mechanism. As derived previously, the carrier depletion phase shifter has a wide optical bandwidth. For these reasons, the Mach-Zehnder carrier depletion modulator has seen great use in digital data communications [RMG+10]. Bulk CMOS processing in silicon

further allows for highly complex and integrated systems [BPL+12, SDY+13]. Significant progress has been made for silicon Mach Zehnder modulators operating near 1550 nm, with devices that have been demonstrated to be suitable at data rates exceeding 50 Gb/s [TLS+13, XXL+13], drive voltages less than 1.0 V<sub>pp</sub> [BDY+12, DJZ+12], and linear analog applications [SAX+13, VMB+10].

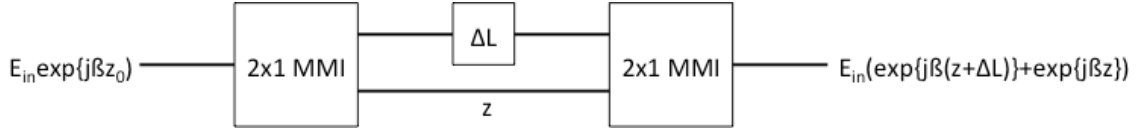


Figure 3.4: Illustration of a Mach-Zehnder interferometer. The output optical intensity varies with wavelength and path length difference  $\Delta L$ .

The optical phase response and small-signal bandwidth of a PN-junction based phase shifter is presented in the previous section. As was mentioned previously, the RC bandwidth due to the series resistance of the source impedance and junction capacitance limits very high-speed applications. Adopting a traveling-wave approach may circumvent this problem. In the design of a traveling wave Mach-Zehnder (TWMZ) modulator, the propagation speed of the RF signal along a transmission line is matched to that of the optical signal within the waveguide. By velocity matching the electrical and optical signal paths, the effective interaction length at high speeds is extended. In this way, the design space is greatly expanded for a high-speed Mach-Zehnder modulator, while still maintaining relatively low insertion loss and  $V_\pi$ .

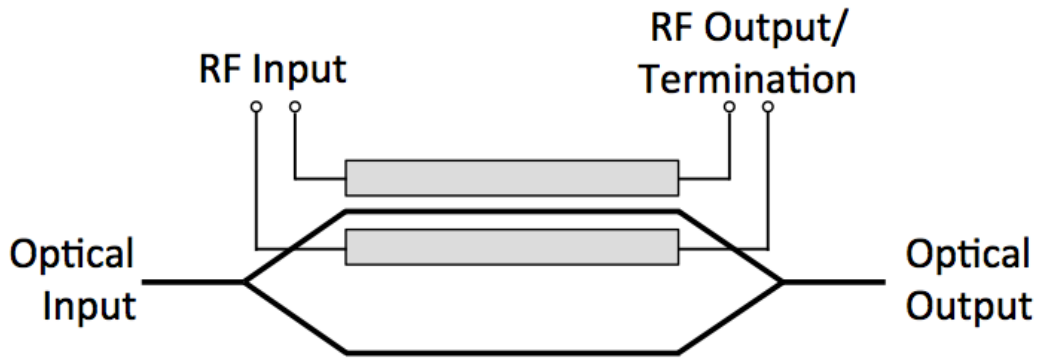


Figure 3.5: Illustration of a TWMZ. The RF and optical modes co-propagate to increase the effective opto-electronic interaction length at high speeds.

Typically, the most important performance metrics of the silicon traveling wave Mach-Zehnder modulator are bandwidth, insertion loss,  $V_{\pi}$ , and footprint. Other metrics that must also be considered in terms of system performance are RF reflections due to electrical impedance mismatch and transfer function linearity. The primary controls the designer has over these values are in the choice of silicon implants, device length, and transmission line geometry. In general, there are a few fundamental tradeoffs in these design choices: heavier doping in the junction leads to higher waveguide losses, lower  $V_{\pi}L$ , and higher bandwidth; longer device lengths leads to higher insertion losses, lower  $V_{\pi}$ , and lower bandwidth; and a lower device electrical impedance improves bandwidth at the cost of electrical reflections at the input. Transfer function linearity will be discussed in the following chapter. These tradeoffs are summarized in Table 3.1.

Given this interplay of parameters, it is necessary to establish design goals. However, it also may be impossible to satisfy all four specifications (Bandwidth,  $V_{\pi}$ , Insertion Loss, Footprint) at the same time, especially if one is working in a fixed process with already established dopant implant recipes. It is often easier and more convenient to aggressively target just one or two metrics. For example, in digital applications  $V_{\pi}$  and bandwidth are often the most important metrics, where device insertion loss or footprint may relax to meet these requirements. The following sections present an analysis of how to design a TWMZ and the nature of these tradeoffs.

### 3.3. TWMZ Transmission Line Design

Given a PN-junction phase shifter with defined phase shifter efficiency, series resistance per unit length, and capacitance per unit length, one may design a transmission line to interface to this junction. In order to simplify the design process, I start with the telegraph line circuit model of a transmission line, and introduce the junction series resistance and capacitance into the circuit, as shown in Figure 3.6.  $L_{TL}$  (In units of H/m) is the transmission line self-inductance,  $R_{TL}$  ( $\Omega/m$ ) is the transmission line series resistance,  $C_{TL}$  (F/m) is the transmission line capacitance, and  $R_{PN}$  ( $\Omega.m$ ) and  $C_{PN}$  (F/m) are the PN junction series resistance and capacitance. Note that all of these values are per unit length.

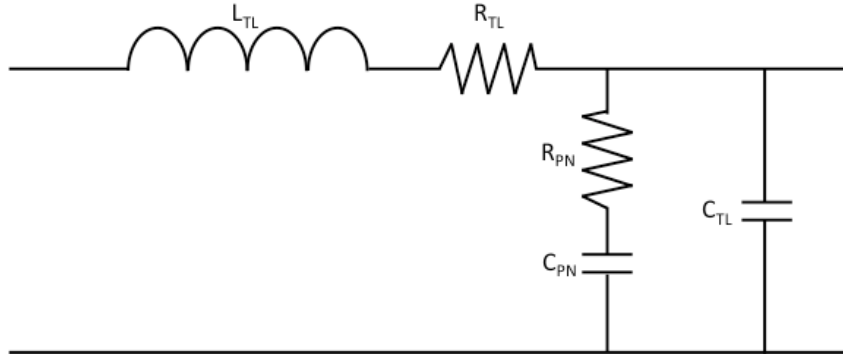


Figure 3.6 Equivalent circuit of a transmission line loaded with a PN junction.

Using the above circuit model, the high-speed device impedance and RF index can be calculated as:

$$Z_{device} = \sqrt{\frac{L_{TL}}{C_{TL} + C_{PN}}} \quad (15)$$

$$n_{TL} = c_0 \sqrt{L_{TL}(C_{TL} + C_{PN})}$$

It is important to note that  $R_{PN}$  and  $C_{PN}$  are dependent on the reverse bias operation point of the modulator. While the built-in potential of the PN-junction allows operation for small forward biases, some reverse DC bias is typically required for large-signal operation.

Since the *modus operandi* of a TWMZ is to phase match between the RF and optical waves, it is necessary to closely match  $n_{TL}$  to the group velocity of the waveguide  $n_g$ . However, the device bandwidth specification will ultimately determine the actual degree of phase matching that is required. Ignoring RF and optical attenuation, the small-signal response of a phase shifter in a TWMZ with a velocity mismatch is given by [L05]:

$$\Delta\phi(f, t) = \int_0^L \Delta\beta(f, t, z) dz = \Delta\phi_0(f)/L \int_0^L e^{-\alpha z} \cos\left(2\pi f \left(\frac{\tau_{VM} z}{L} - t\right)\right) dz \quad (16)$$

where  $\Delta\phi_0$  is the phase response at frequency,  $f$ ,  $\Delta\beta$  is the change in propagation constant induced by some voltage applied to the phase shifter, and  $\tau_{VM}$  is the velocity mismatch defined by:

$$\tau_{VM} = \frac{L}{c} |n_{TL} - n_g| \quad (17)$$

In the case where rf attenuation,  $\alpha$ , is zero the integral reduces to:

$$\Delta\phi(f, t) = \Delta\phi_0(f) \frac{\sin(\pi\tau_{VM})}{\pi f \tau_{VM}} \cos\left[2\pi f \left(t - \frac{\tau_{VM}}{2}\right)\right] \quad (18)$$

If the frequency is well below the RC bandwidth of the PN-junction, the 3-dB bandwidth is then approximately:

$$\begin{aligned} \Delta\phi_0(0)/2 &= \Delta\phi_0(0) \frac{\sin(\pi\tau_{VM})}{\pi f \tau_{VM}} \cos\left[2\pi f \left(t - \frac{\tau_{VM}}{2}\right)\right] \\ \Rightarrow f_{3dB} &\approx \frac{2}{\pi\tau_{VM}} \end{aligned} \quad (19)$$

Fortunately, designing  $n_{TL} > n_g$  may also circumvent the bandwidth limitation due to index mismatch. Since short lengths of intrinsic silicon waveguides have negligible losses in the context of a TWMZ, optical delay lines may be periodically inserted in order

to regroup the RF and optical signals. In this way, while the velocity mismatch is not corrected, the periodicity of these optical delay lines allows for a bandwidth extension.



Figure 3.7: Example layout of an optical delay line in the case where the RF and optical propagation speeds are unmatched.

It is also necessary stage to choose the transmission line impedance target. Since most external modulator drivers and other electronics use a  $50\Omega$  source impedance, oftentimes a  $50\Omega$  TWMZ device impedance is used to reduce reflections between these devices. However, it is not necessarily the best decision to use an exactly  $50\Omega$  device impedance. The tolerance of other electronics to RF reflections may only necessitate maintaining reflected signals to near  $-10$  dB. In this case, a transmission line with impedance as low as  $25\Omega$  could be used. As will be described in the following section, lower device impedances may improve device bandwidths. However, this is also at the cost of reduced on-chip voltage and thus a reduced effective  $V\pi$  at high speed. Using a  $25\Omega$  impedance, the on-chip voltage along the transmission line will be 67% of the applied voltage due to reflection losses:

$$\Gamma = \frac{Z_{dev} - Z_0}{Z_{dev} + Z_0} \quad (20)$$

Once the target  $L_{TL}$  and  $C_{TL}$  parameters are specified, it is necessary to design the physical geometry of the transmission line. Due to the nature of needing to contact both sides of a rib waveguide, coplanar Ground-Signal (GS) or Ground-Signal-Ground (GSG) transmission lines are usually employed.

Typically, finite-element modeling software such as HFSS is used to solve for the transmission line parameters. In rare cases, analytic approximations do exist, although to achieve high performance, an FEM field solver is necessary. The  $L_{TL}$  and  $C_{TL}$  of the transmission line may be simply extracted via two simulations: a length of transmission

line with the end open, and a length of transmission line with the ground and signal lines shorted together by an ideal conductor. By examining the  $Z$ -parameters of launching RF radiation into the device, the  $L_{TL}$  and  $C_{TL}$  may be calculated via the following equations:

$$\begin{aligned} C_{TL} &= -\frac{1}{2\pi f \operatorname{Im}\{Z_{11}\}}; \text{ (Open Simulation)} \\ L_{TL} &= \frac{\operatorname{Im}\{Z_{11}\}}{2\pi f}; \text{ (Shorted Simulation)} \end{aligned} \quad (21)$$

In order to derive these two relationships, reexamine the circuit in Figure 3.6. First, in the case where the two metal lines are left open, the transmission line inductance is very close to zero. At some low-enough frequency, the capacitive impedance will be much greater than the resistance. Similarly, for a simulation where the two metal lines are shorted, the capacitance is disregarded. A simple diagram of these two cases is shown in Figure 3.8.

$$\begin{aligned} Z_{11} &\approx \frac{1}{j\omega C_{TL}} \text{ (Open Simulation)} \\ Z_{11} &\approx j\omega L_{TL}; \text{ (Shorted Simulation)} \end{aligned} \quad (22)$$

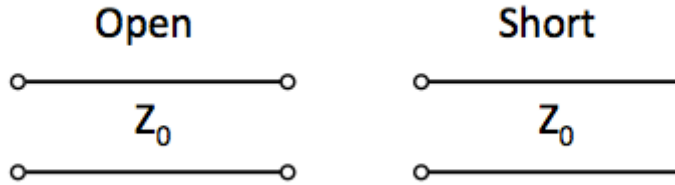


Figure 3.8: Circuit diagrams of the two simulations necessary to extract transmission line self-impedance and capacitance.

After performing this analysis, it may be discovered that the desired transmission line is not physically feasible within the constraints of the fabrication process or footprint goals. There are two possible “easy” changes to obtain the correct impedance and

propagation constants: change the wire width to change the series inductance or reduce the capacitive loading on the transmission line. In the former case, changing the width of the transmission line ( $w$  in Figure 3.9) modifies  $L_{TL}$ . (The shunt capacitance can also be modified by altering the distance between the signal and ground wires. This works only up to the point at which the shunt PN junction capacitance dominates.) In the latter scenario, rather than have a continuous length of PN-junction, the phase shifter is striated. For example: if for every 10  $\mu\text{m}$  of waveguide, 5  $\mu\text{m}$  consists of the PN-junction phase shifter and 5  $\mu\text{m}$  of intrinsic silicon waveguide, then the effective  $C_{PN}$  seen by the transmission line is half of the nominal  $C_{PN}$ . Of course, this will reduce the  $V_\pi$  of the device for the same total device length. Alternatively, it may be necessary to either redesign the PN junction or become creative in the design of the transmission line, such as by employing inductive loops or capacitors to tune the transmission line parameters.

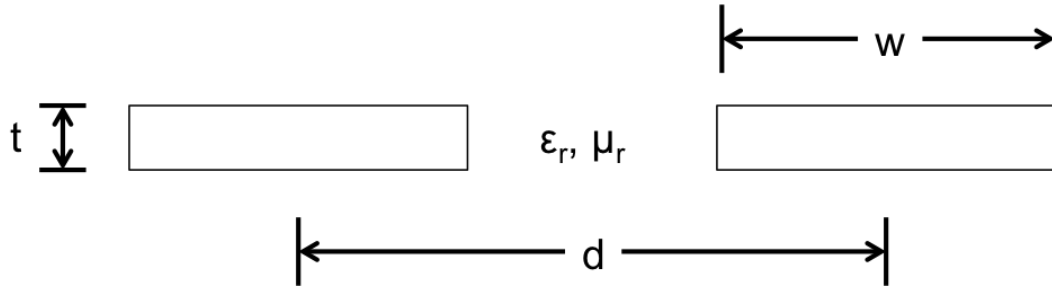


Figure 3.9: A cross section of a simple GS coplanar transmission line.

In a properly designed TWMZ modulator, the primary bandwidth limitation should be RF loss. The primary contributors to this loss are due to the metal resistance and junction series resistance:

$$\alpha = \alpha_{metal} + \alpha_{silicon} \quad (23)$$

$$\alpha = \frac{1}{2} \frac{R_{TL}(f)}{Z_{dev}} + \frac{2\pi^2 f^2 R_{PN} C_{PN}^2 Z_{dev}}{1 + (2\pi R_{PN} C_{PN} f)^2}$$

Considering again the small-signal response:

$$\Delta\phi(f, t) = \frac{\Delta\phi_0(f)}{L} \int_0^L e^{-\alpha z} \cos\left[2\pi f \left(\frac{\tau_{VM}}{L} z - t\right)\right] dz \quad (24)$$

if there is no velocity mismatch, the integral reduces to:

$$\Delta\phi(f, t) = \Delta\phi_0(f) \frac{1 - e^{-L\alpha(f)}}{\alpha(f)L} \cos(2\pi f t) \quad (25)$$

In the case where we are operating well below the inherent RC bandwidth of the junction and where series resistance dominates, the total attenuation is approximately:

$$\alpha \approx 2\pi^2 f^2 R_{PN} C_{PN}^2 Z_{dev} \left[ \frac{1}{m} \right] \quad (26)$$

Additionally, still assuming that the RF and optical modes are well-matched, the electrooptical 3-dB bandwidth of a TWMZ is related to the electrical 3-dB bandwidth of the transmission line as:

$$L_{dev} \alpha(f_{EO,3dB}) \approx 6.4 \text{ dB} \quad (27)$$

From the above approximations, several key proportionalities become apparent. These tradeoffs between the junction design, device length, and device impedance are summarized in Table 3.1.

Table 3.1: TWMZ design summary. The proportionalities are approximate.

	<b>Device Length (<math>L</math>)</b>	<b>Series Resistance (<math>R_{PN}</math>, related to <math>d_{n++}</math> and <math>d_{p++}</math>)</b>	<b>Junction Capacitance (<math>C_{PN}</math>, related to implant concentration)</b>	<b>Device Impedance (<math>Z_{dev}</math>)</b>
<b>Insertion Loss</b>	$L$	$e^{-(d_{n++}+d_{p++})}$	$\sim(N_A + N_D)$	1
<b>Bandwidth</b>	$\frac{1}{\sqrt{L}}$	$\frac{1}{\sqrt{R_{pn}}}$	$\frac{1}{C_{PN}}$	$\frac{1}{\sqrt{Z_{dev}}}$
$V_\pi$	$\frac{1}{L}$	1	$\sim \frac{1}{N_A + N_D}$	$\frac{Z_{dev} - Z_0}{Z_{dev} + Z_0}$
<b>Footprint</b>	$L$	1	1	1

### 3.4. Design of a 50 Gb/s Mach-Zehnder Modulator for 1310 nm

Using the previous concepts I have adapted the design of an 18 GHz traveling wave Mach Zehnder device to a similar device with a bandwidth improved to 30 GHz. This bandwidth is then shown to support 50 Gb/s data communication. The wavelength band near 1300 nm is attractive for telecommunication systems, such as upstream/downstream communication in passive optical networks or working beyond the dispersion limit at long transmission distances in high-speed communications [K06]. While many hybrid silicon modulators have also been demonstrated in this band [TPB12, LHM+11, JTS+13], these geometries are not currently compatible with CMOS bulk processing in silicon photonic platforms. Notably, J. Fujikata, et al present a traveling wave Mach-Zehnder modulator operating at 25 Gb/s near 1300 nm using a MOS junction [FTT+13], which is compatible with CMOS processing.

The first generation modulator was designed for 1550 nm and speeds only up to 25 Gb/s. This previous device used 2 levels of implant concentration for p-type and n-type doping. In order to minimize optical loss while still maintaining relatively low series resistance (proportional to bandwidth by  $R_{pn}^{-\frac{1}{2}}$ ), the high level implants (p++ and

n++) are placed 0.95  $\mu\text{m}$  away from the core of the waveguide as shown below. The p++ and n++ implants are necessary for low contact resistance with the Aluminum back end of line. A cross sectional diagram of the device is shown in Figure 3.10.

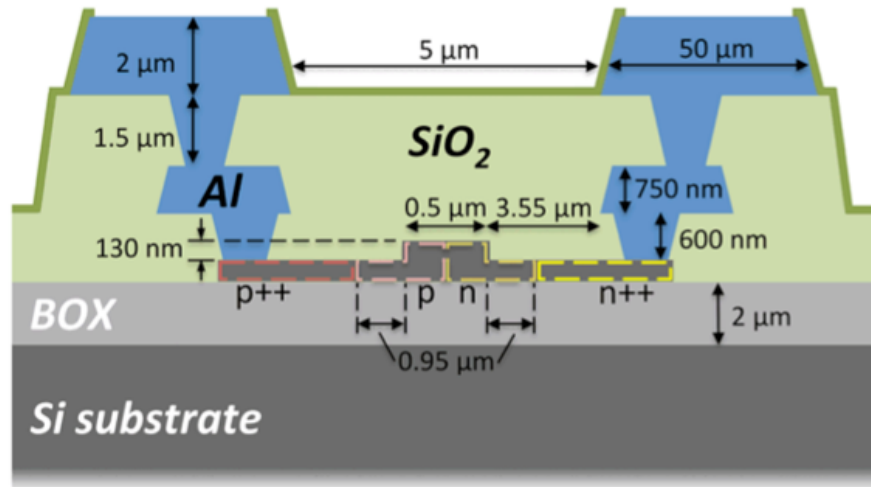


Figure 3.10: Cross section of the 18-GHz 3.0mm long traveling wave Mach-Zehnder modulator (not to scale).

The first generation device was optically probed on-wafer. An array of polarization-maintaining optical fibers is incident onto on-chip grating couplers. The grating couplers convert the vertically incident light into the waveguide TE-mode. Waveguides then route the light into the modulator, and the modulated signal is coupled back into another optical fiber by an output grating coupler. RF probes contact aluminum pads that directly connect to the on-chip transmission line. Figure 3.11 shows an illustration of a typical test structure for this type of device.

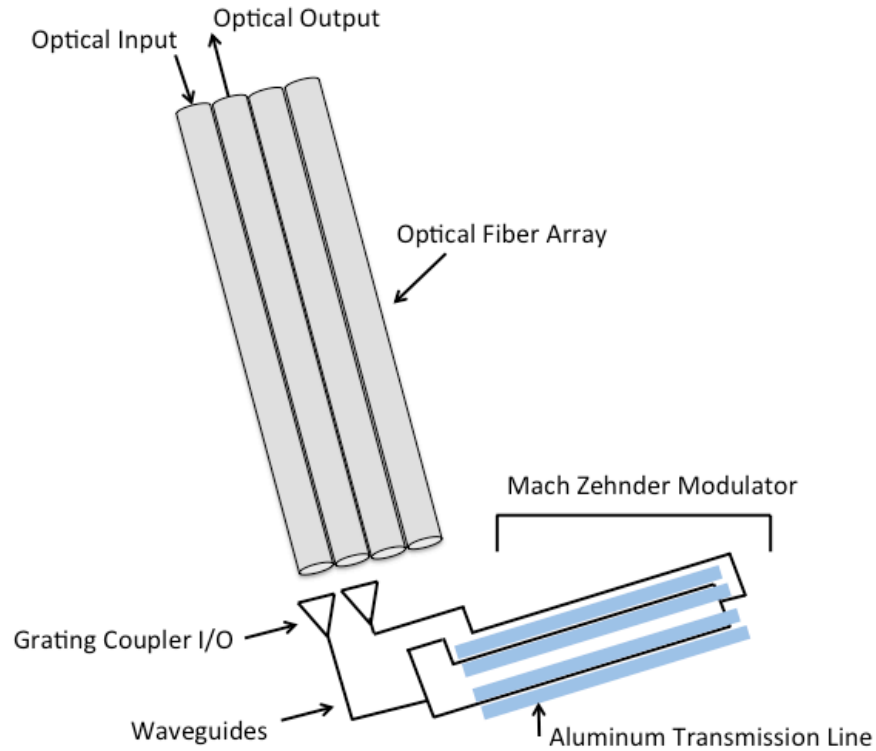


Figure 3.11: Illustration of a typical test structure for the traveling wave Mach-Zehnder modulator. Light is coupled onto and off of the chip through a fiber array incident onto a grating coupler.

The phase response of the device is measured by adjusting the transmission line DC bias offset. Since the modulator is unbalanced by  $100\ \mu\text{m}$ , the phase shift can be easily extracted by tracking the change in spectrum versus bias voltage. The phase response normalized per unit length of this device is shown in Figure 3.12. Due to the PN junction nonlinearity, the phase response decreases at larger biases. For silicon modulators, a small-signal  $V\pi L$  is usually reported to characterize the performance of the junction. Since at some device lengths it could be physically impossible to achieve a  $\pi$  phase shift before PN junction breakdown. For this device, a small-signal  $V\pi L$  of  $2.4\ \text{V}\cdot\text{cm}$  at a  $1\ \text{V}$  reverse bias is measured (Figure 3.12). The difference between top and bottom arms is likely due to a mask misalignment problem during fabrication. The n-type side of the PN junction is always connected to the signal arm of the device, such that positive voltages always reverse bias the device. Thus, a slight shift upwards or downwards of one of the

implantation masks during lithography would have different effects on the top and bottom arms.

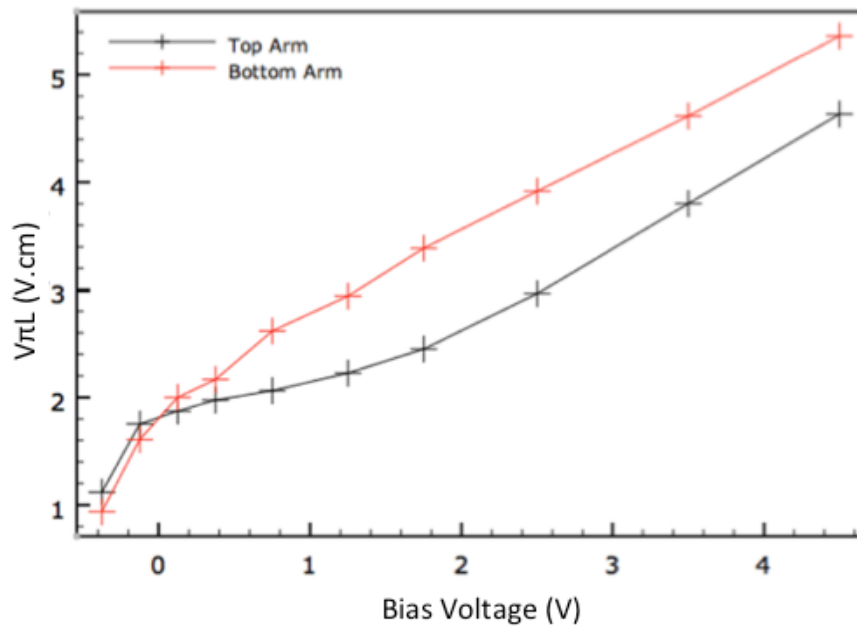


Figure 3.12: Phase shift versus bias voltage of the first-generation device: an 18 GHz traveling wave Mach Zehnder modulator

Finally, the bandwidth of the device is measured using a vector network analyzer. A block diagram of the test setup is shown in Figure 3.13. The test setup is similar to that of the DC electro-optical measurements, with the addition of high-speed probes. Electrooptic S21 measurements show a 3-dB bandwidth of 17.5 GHz for the top arm and 15.5 GHz for the bottom arm of the interferometer. The difference in bandwidth is again caused by the same mask misalignment error. The bandwidth is plotted in Figure 3.14.

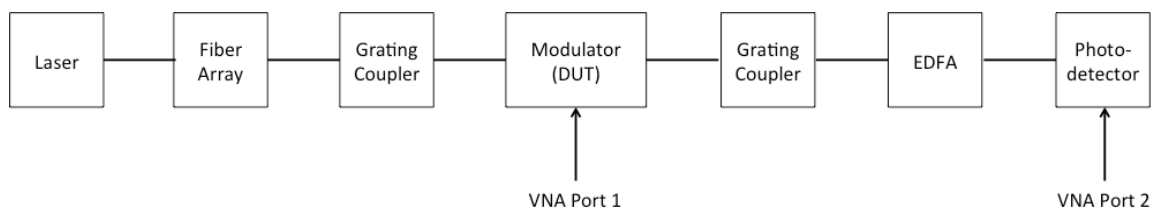


Figure 3.13: Block diagram of the test setup.

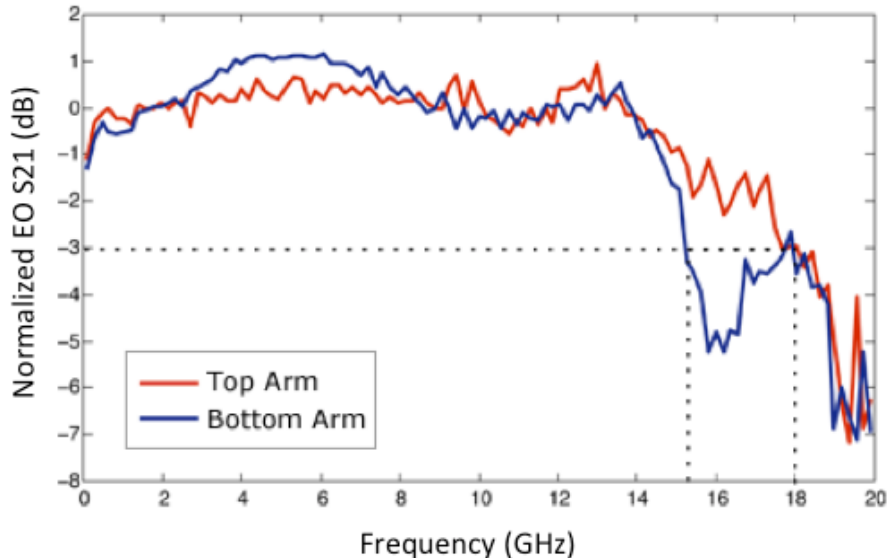


Figure 3.14: Electrooptic S21 measurement of the original un-optimized device, showing 15.5 and 18 GHz bandwidths. The transmission line is biased at -1 V.

The goal of the next iteration of modulator was to extend this bandwidth to 30 GHz without increasing the optical insertion loss or  $V_{\pi}L$  figure of merit. From the table in the previous sections, changing the device length, series resistance, junction capacitance, or device impedance can all modify bandwidth. A shorter device will definitely have a larger bandwidth, but will require larger drive voltage to achieve the same extinction ratio. A change in  $C_{PN}$  could yield a higher bandwidth device, but may also result in a lower phase efficiency, since the depletion width will increase with decreasing doping concentration. Finally, we limit our bandwidth to  $33 \Omega$  in order to maintain an acceptable reflection coefficient. While the simplest method to reduce  $R_{PN}$  is to reduce the clearance between the waveguide and high dopant concentration regions, this results in a tradeoff between insertion loss and bandwidth. Instead, by introducing intermediate dopants, it is possible to primarily sacrifice process complexity for bandwidth.

The optimized device is similar in architecture to that presented in [BDY+12]. There were, however, several key differences between the two devices. Firstly, the device was optimized for the 1310 nm wavelength band. Thus, the waveguides were scaled from 500 nm wide to 420 nm to obtain similar confinement for the  $TE_0$  mode at 1310 nm and similar mode overlap with the PN junction. Secondly, the p+ and n+ implantation layers

were added as intermediate concentration levels between the highly doped contact layers and the active layer forming the PN junction. Thirdly, each arm of the Mach-Zehnder modulator integrates thermal phase tuners to properly bias the device (test structures still use a 100  $\mu\text{m}$  arm unbalance for easy testing—truly athermal devices would require equal arm lengths and phase tuners). Lastly, the modulator uses other devices optimized for 1310 nm operation, including grating couplers and a Y-Junction MMI structure. An optical micrograph image of the device is shown in Figure 3.15.

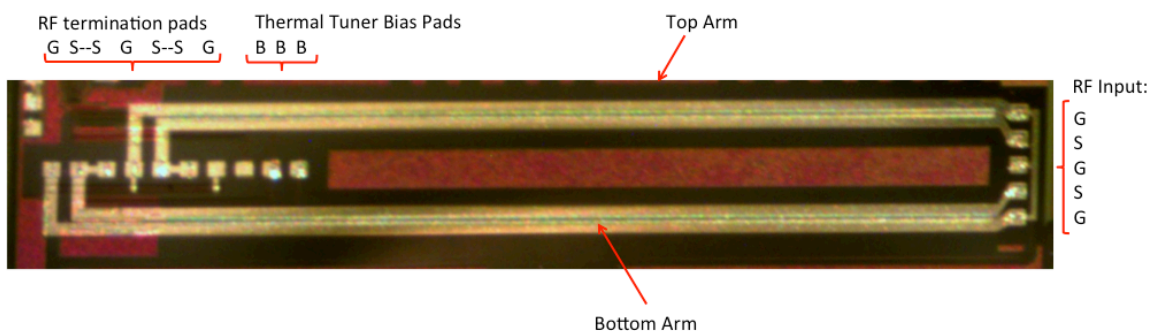


Figure 3.15: Optical micrograph of the 1310 nm traveling wave modulator.

An illustration of the cross-section of the PN junction phase shifter is shown in Figure 3.16. In [BDY+12], the P and N-type layers had  $10 \text{ k}\Omega/\square$  and  $7 \text{ k}\Omega/\square$  sheet resistance, respectively. The distance from the highly doped region to the waveguide core is  $0.95 \mu\text{m}$ , therefore this doping profile resulted in  $1.62 \Omega\text{-cm}$  series resistance due to the partially etched silicon. From simulation, the sheet resistances of the p+ and n+ intermediate dopants in partially etched silicon were expected to be  $3.8 \text{ k}\Omega/\square$  and  $1.5 \text{ k}\Omega/\square$ , respectively. With the junction as depicted in Figure 3.16, this corresponds to a series resistance in the partially etched silicon of  $0.65 \Omega\text{-cm}$ . As was derived above, the approximate proportionality between the modulator 3-dB bandwidth and series resistance  $R_{PN}$  was  $f_{EO,3dB} \propto \frac{1}{\sqrt{R}}$ . Using this scaling proportionality, the reduction in series resistance by adding intermediate dopants should improve the previous 3-dB bandwidth of 18 GHz for the 3 mm long device to approximately 29 GHz.

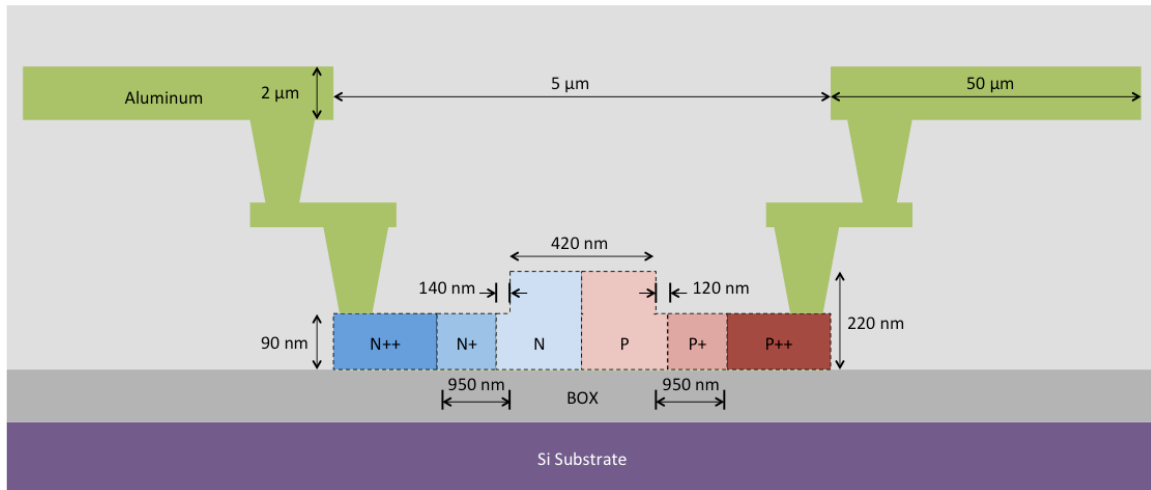


Figure 3.16: Cross sectional diagram of the PN junction phase shifter, not to scale.

The transmission line is designed to have a  $33 \Omega$  impedance when loaded with the PN junction. Each arm of the Mach-Zehnder consists of a 3 mm long lateral PN-junction phase shifter, broken down into  $10 \mu\text{m}$  long segments. To insure the current travels through the metal rather than laterally through the silicon, each  $10 \mu\text{m}$  segment of phase shifter consists of a  $9.2 \mu\text{m}$  long PN-junction followed by a  $0.8 \mu\text{m}$  length of undoped silicon. The transmission lines are driven by a set of GSGSG input pads and terminated by a set of GSSGSSG output pads. The GSSGSSG pads are to allow for a  $25 \Omega$  termination impedance, rather than  $50 \Omega$  with conventional RF cabling. The  $2.0 \mu\text{m}$  thick top aluminum layer is used for the transmission line to minimize RF losses. The via-stack from M2 to silicon was determined by design rules as well as via and contact resistance considerations.

Fabrication occurred at the Institute of Microelectronics (IME), A\*STAR, Singapore in a multi-project wafer run through the OpSIS foundry service. Each lithography step utilized 248 nm photolithography. The starting material is a 220 nm top-silicon thickness SOI wafer with a  $2 \mu\text{m}$  thick buried oxide layer and a high-resistivity  $750 \Omega\text{-cm}$  silicon substrate. The high-resistivity silicon substrate is necessary for high-speed RF performance [WBH10]. The first etch defined the grating coupler partial etched layer with a 60 nm anisotropic dry etch. This is followed by an additional lithography mask

and etch step to define the 90 nm slab layer. Finally, the silicon ridge is defined by a full silicon over-etch. The p<sup>++</sup>, p<sup>+</sup>, p, n, n<sup>+</sup>, and n<sup>++</sup> implants were performed next on the exposed silicon before oxide deposition. The peak doping densities for the p<sup>+</sup>, p, n, and n<sup>+</sup> layers were chosen to be 2e18/cm<sup>3</sup>, 7e17/cm<sup>3</sup>, 5e17/cm<sup>3</sup>, and 3e18/cm<sup>3</sup>, respectively. The implants were followed by a rapid thermal anneal at 1030 °C for 5 seconds. Finally, two layers of aluminum vias and interconnects were formed.

### 3.5. Experimental Results

Just as with the previous devices, light is coupled onto and off of the chip via grating couplers. In order to extract insertion loss, a pair of grating couplers near the device formed a loop. Recording the spectral transmission through the loop with no Mach-Zehnder modulator, and then subtracting the spectrum of the modulator, can measure device insertion loss. The total insertion loss of the device is measured to be 5.5 dB. Of this 5.5 dB, 1.6 dB excess loss is due to two Y-Junctions, 0.1 dB is due to tapers from ridge to rib waveguides, 0.16 dB is due to the thermal tuner, and the remaining 3.34 dB is due to the 3 mm long phase shifter. Within a  $2\pi$  phase shift in the thermal tuners, the loss of the n-type layer dominates, such that the variation in thermal tuner loss as a function of applied phase shift is insignificant.

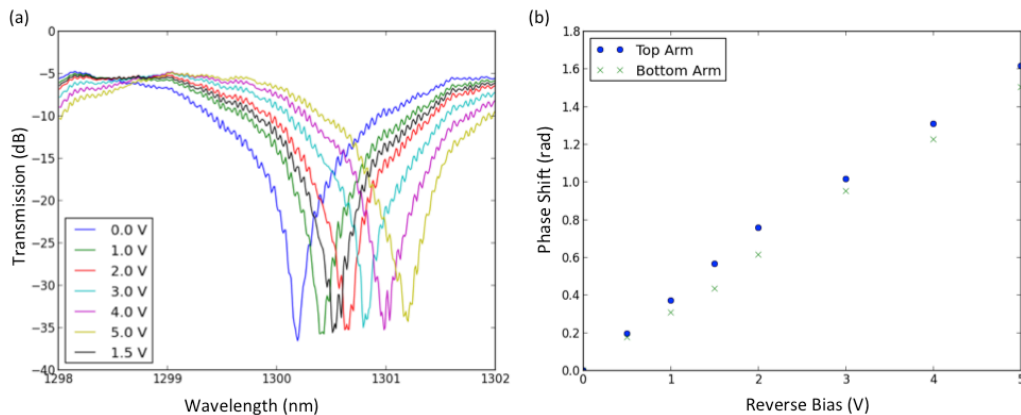


Figure 3.17: DC electrooptic measurements of the TWMZ. (a) Typical measured spectrum of the modulator at different reverse bias voltages. (b) Extracted phase shift versus bias voltage for the top and bottom arms of the modulator.

The Mach-Zehnder interferometer is intentionally unbalanced by  $100\ \mu\text{m}$  to enable easy testing by tuning the input wavelength. To test the DC performance of the phase shifters, wavelength sweeps are measured at various reverse bias voltages. Due to the unbalanced interferometer, the phase shift may be tracked by observing the shift in null points of the fringes in the spectrum. A typical spectrum at different DC bias voltages is shown in Figure 3.17(a) and the phase shift versus reverse bias is shown in Figure 3.17(b). The small-signal  $V\pi L$  between 0 V and 1 V reverse bias is 2.64 V-cm and 2.43 V-cm for the bottom and top arm, respectively. Additionally, since the device is intended to operate with no or low bias, C-V and I-V curves are presented in Figure 3.18(a, b).

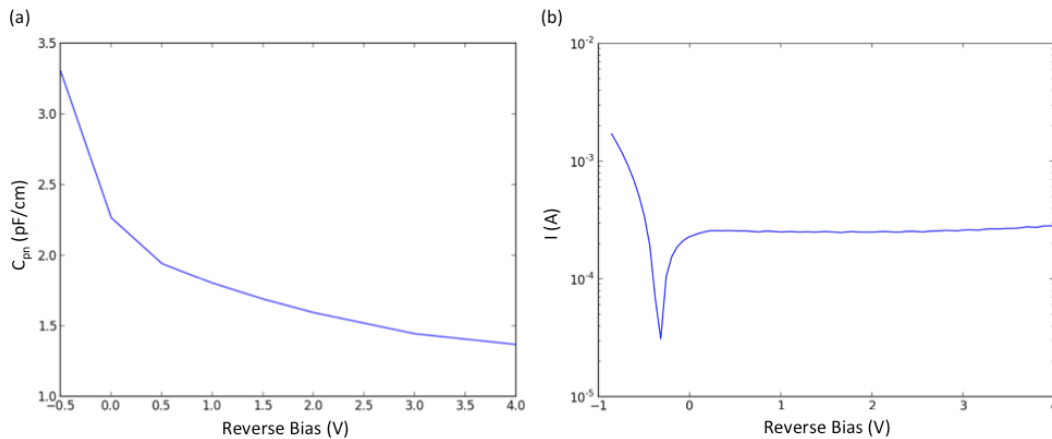


Figure 3.18: Modulator PN junction characteristics. (a) Capacitance versus bias voltage of the PN junction of the phase shifter. (b) Current-voltage relationship of the device without the  $50\ \Omega$  RF termination.

The cross section of the thermal tuner is shown in Figure 3.19. The n-type doped waveguide core acts as a heater and is measured to have a resistance of approximately  $42\ \Omega$ . The shift in null point is also used to test the efficiency of these thermal phase shifters. A constant DC bias is applied to the resistor and the power required to achieve a  $\pi$ -phase shift is measured to be 27 mW. The phase shift versus power into the resistor is shown in Figure 3.20. Additionally, at least within a phase shift of  $2\pi$ , the change in index is primarily due to thermal tuning and not due to injected carriers. The relationship

between index and carrier concentration in silicon has opposite sign from the relationship between index and temperature. Thermal index changes are proportional with the square of current and carrier refraction is approximately linearly proportional with current. From the plot of phase shift vs. power, if carrier concentration were to dominate at small currents, the total phase shift should decrease below a certain power. However, since a purely linear relationship is observed, we conclude that the phase shift is dominated by the thermal tuning at measureable phase shift and currents.

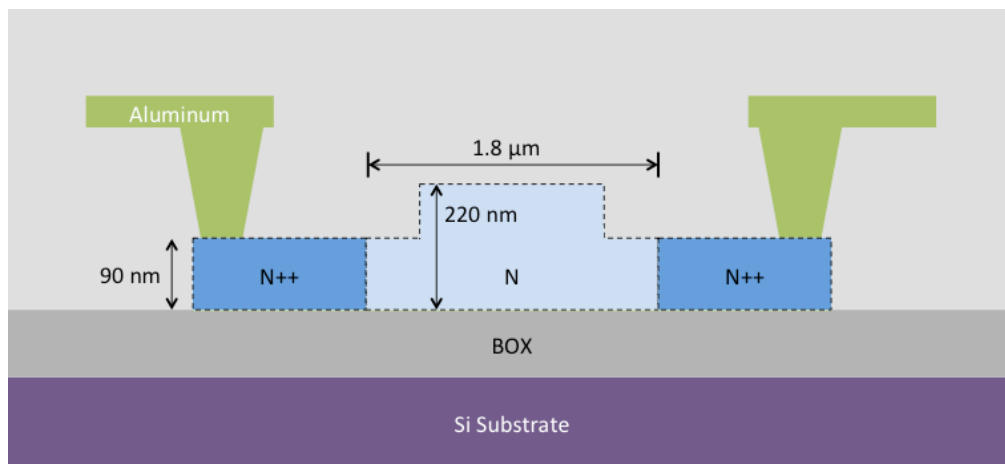


Figure 3.19: Cross-sectional diagram of the thermal phase tuner. The core of the waveguide forms the resistive heater

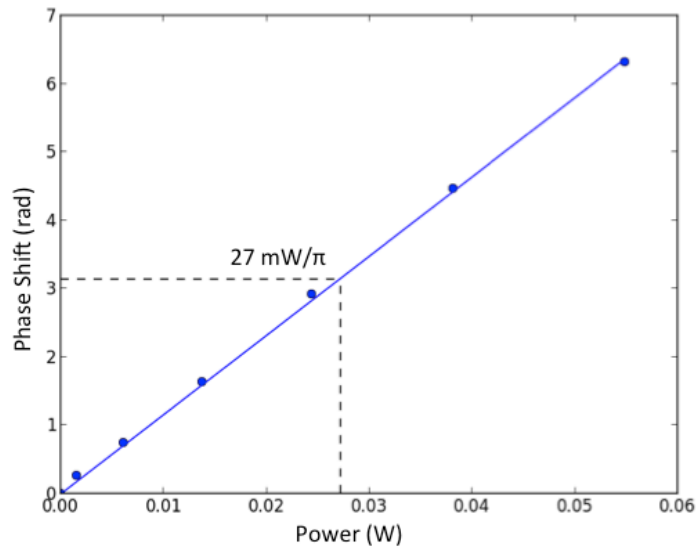


Figure 3.20: Measured phase shift versus applied power in the thermal phase tuner. 27 mW is required to tune the phase of the output light by  $\pi$  radians.

The high speed performance of the device is characterized by an electrooptic S-parameter sweep, and a typical S11 and S21 trace is shown in Figure 3.21. In order to test the bandwidth, the wavelength was biased at the optical -3 dB point in the spectrum. An Agilent N4373C Lightwave Component Analyzer and a Newport 1414 photodetector were used to test the device. Each arm was driven individually with a GSGSG probe, where the arm not under test was connected to a 50  $\Omega$  termination resistor. A GSSGSSG probe is used to terminate the device, where each signal path is connected to two 50  $\Omega$  termination resistors in parallel, resulting in an equivalent 25  $\Omega$  termination impedance. Terminating with a lower impedance suppresses modulation depth at low speeds, which then improves operation bandwidth when normalizing to the low frequency response. Although there appears to be ripples on the order of 2 dB in the S21 of the bottom arm that fall below the -3dB point, as will be shown below, this does not prevent the device from achieving 50 Gbps performance.

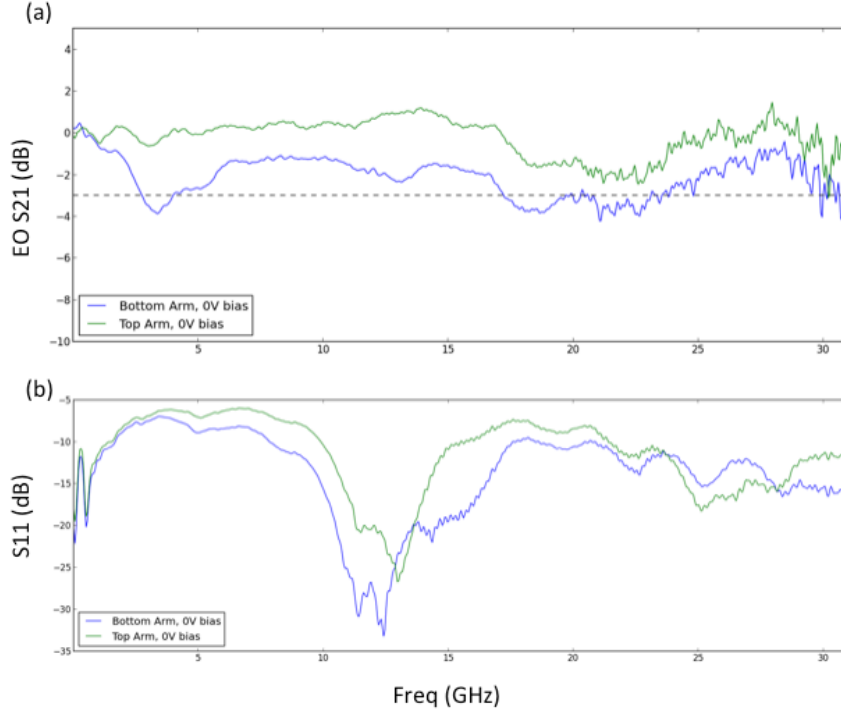


Figure 3.21: S-parameter measurements of the TWZM. (a) Electro-optic S21 measurement of the traveling wave modulator showing 30 GHz device bandwidth at 0V reverse bias. (b) Electrical S11 measurement of the device.

To demonstrate high speed digital performance, a 50 Gbps PRBS signal is driven through the device. An Anritsu MP1822A Pattern Generator is used to generate a differential  $2^{15}-1$  PRBS signal, which is then applied to the input pads using a GSGSG RF probe. Light at the -3dB point, in this case 1301.91 nm, is input into the device and then received by a Picometrix AD-10ir photodetector connected through a DC block to an Agilent Digital Communications Analyzer (DCA). Although the received electrical signal is AC coupled, the extinction ratio may still be extracted. Knowing the responsivity of the photodetector, the DC optical power into the photodetector ( $P_{avg}$ ) can be recorded through a current monitor on the AD-10ir photoreceiver. Similarly, the peak-to-peak voltage amplitude measured by the DCA can be converted to the peak-to-peak optical power,  $P_{p-p}$ . If we then assume that the PRBS signal consists of an even distribution of “1” and “0” bits, the extinction ratio is calculated as:

$$ER = 10 \log_{10} \left( \frac{P_{avg} + P_{pk-pk}/2}{P_{avg} - P_{pk-pk}/2} \right) \quad (28)$$

Also of interest is the “1” bit excess loss of the device, defined as the additional loss incurred for output representing a digital “1” bit compared to the maximum transmission. This loss is calculated based on the optical bias point,  $P_{bias}$ , as:

$$1 \text{ bit loss} = P_{bias} + 10 \log_{10} \left( \frac{P_{avg} + P_{pk-pk}/2}{P_{avg}} \right) \quad (29)$$

I demonstrate eye diagrams using three different drive voltage conditions. Driving with a signal amplitude of  $1.5 V_{pp}$  and 0 V bias yields an energy efficiency of 450 fJ/bit, extinction ratio of 3.4 dB, and “1” bit loss of 1.6 dB; driving with a signal amplitude of  $2.0 V_{pp}$  and 0 V bias yields an energy efficiency of 800 fJ/bit, extinction ratio of 4.6 dB, and “1” bit loss of 1.3 dB, shown in; and by driving with a  $3.0 V_{pp}$  signal with a 1.0 V reverse bias we achieve an energy efficiency of 3.4 pJ/bit, extinction ratio of 4.2 dB, and “1” bit loss of 1.4 dB. These three eye diagrams are shown in Figure 3.22 to Figure 3.24.

With an equivalent  $25 \Omega$  termination resistance, energy per bit is calculated by:

$$\text{Energy/bit} = \frac{N_{input}}{B} \left( \frac{(V_{pp}/2)^2}{50 \Omega} + \frac{V_{bias}^2}{25 \Omega} \right) \quad (30)$$

where  $N_{input}$  is the number of electrical inputs and  $B$  is the data rate in bits per second. Since the PRBS signal generator uses a  $50 \Omega$  output impedance, this value is used for estimating power consumption. Note that since the transmission line impedance is  $33 \Omega$ , the on-chip drive voltage is actually less than the drive voltage that is reported here due to reflections at the input of the device. The energy consumption could be improved if lower impedance modulator drivers were designed (thus requiring lower output drive voltages).

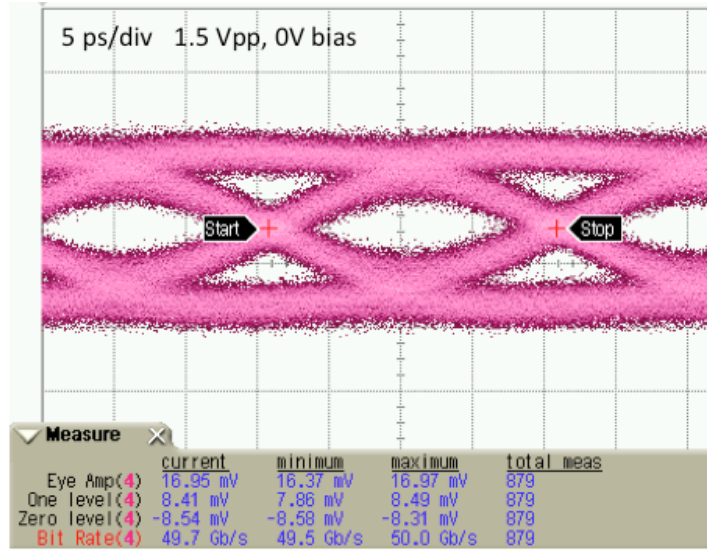


Figure 3.22: 50 Gb/s eye diagram using a differential PRBS15 signal at 1.5 V<sub>pp</sub> and 0 V reverse bias.

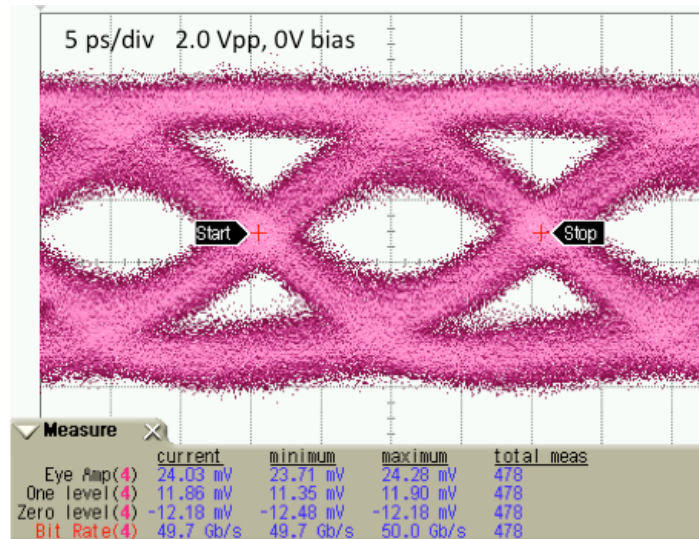


Figure 3.23: 50 Gb/s eye diagram using a differential PRBS signal at 2.0 V<sub>pp</sub> and 0 V reverse bias.

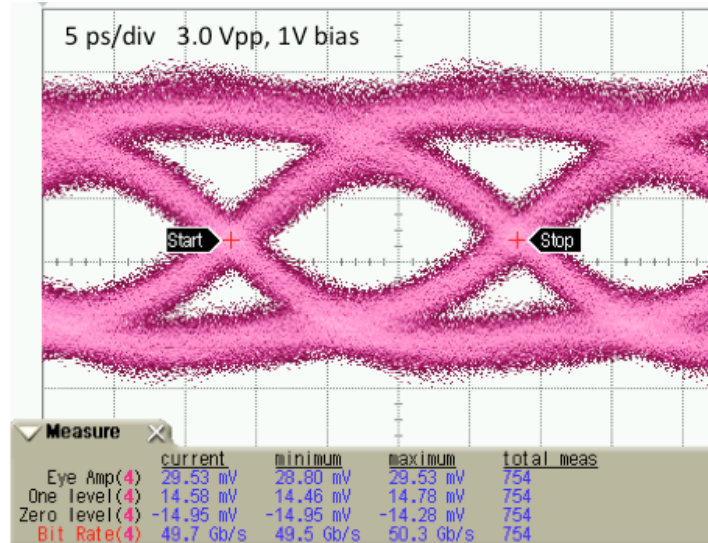


Figure 3.24: 50 Gb/s eye diagram using a differential PRBS signal at 3.0 Vpp and 1 V reverse bias.

### 3.6. Conclusions

A comparison of the performance of our modulator to other Mach-Zehnder modulators, including results at 1550 nm, is shown in

Table 3.2. DC loss of the phase shifters is presented in the right-most column of

Table 3.2. Here I only compare the performance of the phase shifters rather than total on-chip loss in order to normalize for passive performance not related to the modulator design. For example, low loss and compact Y-Junctions and MMI's have been extensively demonstrated in a variety of SOI processes, but not all of the modulator results referenced utilize such devices.

As can be seen in the table, this device demonstrates the highest energy efficiency of any silicon Mach-Zehnder modulator capable of at least 40 Gb/s. While the results reported in [DJZ+13] report a lower energy efficiency, they achieve only 0.92 dB of extinction, which would likely incur a very large penalty. Their device also has a relatively low bandwidth for the data rate (less than or equal to half the symbol rate). Finally, since the wavelength band near 1300 nm is important for many short-reach (e.g. within a data center) telecommunications systems, silicon devices that can modulate light

in this band are desirable. This is the first demonstration of a silicon modulator to operate at 50 Gb/s near 1300 nm.

Table 3.2: Comparison to other traveling-wave modulators in silicon above 40 Gb/s

Reference	PN junction type, configuration, wavelength	Driving voltage and bias <sup>a</sup>	Data rate, Energy-per-bit <sup>b</sup>	Extinction Ratio, "1" bit loss (dB)	Electro-optic BW (GHz)	$V_{\pi}L$ at bias (V-cm)	Phase shifter length (mm)	DC Phase Shifter Insertion loss (dB)
[LLR+07]	Vertical pn, single-arm, 1550 nm	6 V <sub>pp</sub> -3 V bias	40 Gb/s, 4.5 pJ/bit	ER: 1.1 dB Loss: NA	30	4	1	1.8
[XXL+13]	Lateral pn, single-arm, 1550 nm	6.5V <sub>pp</sub> -5 V bias	60 Gb/s, 3.5 pJ/bit	ER: 3.6 dB Loss: 1.6 dB	28	2.05	0.75	1.2
[GTE+11]	Wrapped pn single-arm, 1550 nm	6V <sub>pp</sub> -3 V bias	40 Gb/s, 4.5 pJ/bit	ER: 6.5 dB Loss: 10 dB	NA	11	1.35	7.7
[TGF+12]	Lateral pn, single-arm, 1550 nm	6.5V <sub>pp</sub> -4 V bias	50 Gb/s, 4.2 pJ/bit	ER: 3.1 dB Loss: 3.2 dB	NA	2.8	1	3.2
[ZMR+12]	Pipin diode, single-arm, 1550 nm	7V <sub>pp</sub> bias NA	40 Gb/s, 6.1 pJ/bit	ER: 6.6 dB Loss: 0 dB	20	3.5	4.7	4.7
[ZMR+12]	Pipin diode, single-arm, 1550 nm	7V <sub>pp</sub> bias NA	40 Gb/s, 6.1 pJ/bit	ER: 3.2 dB Loss: 2 dB	40	3.5	0.95	0.95
[TGH+12]	Lateral pn, single-arm, 1550 nm	4V <sub>pp</sub> bias NA	40 Gb/s, 2 pJ/bit	ER: 7 dB Loss: 0 dB	NA	2.7	3.5	15.75
[TGH+12]	Lateral pn, single-arm, 1550 nm	6.5V <sub>pp</sub> bias NA	40 Gb/s, 5.2 pJ/bit	ER: 3.5 dB Loss: 0 dB	NA	2.7	1	4.5
[TLS+13]	Lateral pn, single-arm, 1550 nm	7V <sub>pp</sub> -5 V bias	50 Gb/s, 4.9 pJ/bit	ER: 5.56 dB Loss: NA	25.6 <sup>c</sup>	2.67	4	4.1
[DCC12]	Lateral pn, single-drive push-pull, 1550 nm	5V <sub>pp</sub> -5 V bias	40 Gb/s, 3.1 pJ/bit	ER: 6 dB Loss: NA <sup>e</sup>	NA	2.08	4	4.8
[DCC12]	Lateral pn, single-drive push-pull, 1550 nm	5V <sub>pp</sub> -6 V bias	50 Gb/s, 2.5 pJ/bit	ER: 4.7 dB Loss: NA <sup>f</sup>	NA	2.4	2	2.4
[DJZ+13]	Lateral pn, two-arm differential drive, 1550 nm	0.36 V <sub>pp</sub> 0 V bias	40 Gb/s, 0.036 pJ/bit	ER: 0.92 dB Loss: 0 dB	20 <sup>d</sup>	0.75	2	4.5
<b>[SDL+13]</b>	<b>This work</b> <b>Lateral pn, two-arm differential drive, 1310 nm</b>	<b>1.5 V<sub>pp</sub></b> <b>0 V bias</b>	<b>50Gb/s,</b> <b>0.45 pJ/bit</b>	<b>ER: 3.4 dB</b> <b>Loss: 1.6 dB</b>	<b>30</b>	<b>2.43/</b> <b>2.64</b>	<b>3</b>	<b>3.34</b>

<sup>a</sup>Bias voltage for eye-diagram and/or bandwidth measurement.

<sup>b</sup>Possible DC power consumption at the termination resistor is excluded for [23], [25], and [26].

<sup>c</sup>Measurement plot in [4] suggests that EO response rolls off about 5 dB at this frequency. Other numbers in this column are 3 dB bandwidth.

<sup>d</sup>EOS21 bandwidth in [7] is simulated from a measured RF S21 trace of the device transmission line

<sup>e</sup>Light is biased at the optical -3 dB point, though "1" bit loss is not reported

<sup>f</sup>The authors of [28] report that the measurement was performed "with a wavelength close to the minimum transmission point."

## Chapter 4. Spur-free dynamic range measurements of a silicon optical modulator

In this chapter, I present measurements of an optical link using a silicon Mach-Zehnder modulator. These are the first measurements of spur-free dynamic range of such an optical link, and demonstrate a high linearity. Highly linear devices are necessary for analog optical links in order not to add other distortions to the signal. It has been an outstanding question whether silicon optical modulators based on carrier-depletion could have suitable linearity due to the PN-junction nonlinearity inherent in their phase shift. I performed the RF link measurements and analysis of the Mach-Zehnder modulator. Ali Ayazi assisted with these measurements, and Tom Baehr-Jones designed the original device. This work was previously published in *Optics Express*:

**M. Streshinsky**, A. Ayazi, Z. Xue, A. Eu-Jin Lim, G. Qiang Lo, T. Baehr-Jones, M. Hochberg, “Highly Linear Silicon Traveling Wave Mach-Zehnder Carrier Depletion Modulator Based on Differential Drive,” *Optics Express*, vol. 21, no. 3, pp. 3818-3825, 2013

### 4.1. Optical modulators for RF applications

Optical modulators have been actively explored and deployed over the past several decades to meet the needs of complex and high-capacity RF communication links. The low attenuation of single-mode optical fiber enables the transport of RF signals over longer distances than previously possible [FS02]. Additionally, fiber optics is significantly less bulky, has larger bandwidth, is more mechanically stable, and is much more resistant to electromagnetic interference when compared to electrical beam forming networks [PRM96]. These traits are highly desirable for space-based satellite communication applications where size and reliability are of utmost importance. Additionally, the reduction in bulk and gain in transmission distances are also advantageous in compact wireless local area networks for picocellular networks [SKG07]. In general, photonics can make its way into microwave networks in areas

where very complex functionality prohibits the use of the radio-frequency domain directly.

The main application for microwave photonics is in radio-over-fiber systems. With less than a dB/km of RF attenuation and bandwidths in the many-GHz range, the design of microwave photonic links is very flexible: RF repeaters are not typically necessary except for extremely long links, antennas can be remotely placed and routed through a centralized architecture, and links are future-proofed through the large bandwidth of the system [CN07]. A common implementation of radio-over-fiber systems integrates both wireless and fiber networks together. An example of such a system includes cellular networks, antenna distribution systems, wireless local area networks (WLAN), and broadband mobile networks. For some scenarios, such as WLAN, the RF over fiber is at 5 GHz, and the implementation can be achieved with directly-modulated lasers [QHI+05]. In contrast, picocellular networks can operate in the 30 GHz band, and wireless personal area networks in the 60 GHz band, which make RF-over-fiber implementations challenging [HP00]. As the challenges of RF design are overcome, these types of technologies enable new concepts for antenna and access architecture [MPM01, WJM97].

One important performance metric for an analog optical link is spur-free dynamic range (SFDR) [ILM+07]. SFDR is defined as the signal-to-noise ratio when the power in the largest harmonic is equal to the noise level. For example, for a proposed picocellular WLAN system, an SFDR of  $95 \text{ dB}\cdot\text{Hz}^{2/3}$  is required [SKG07]. Both directly-modulated lasers and externally modulated  $\text{LiNbO}_3$  modulators can provide sufficient bandwidth and linearity for many RF applications. Directly modulated lasers with 3rd order limited SFDR performance up to  $125 \text{ dB}\cdot\text{Hz}^{2/3}$  have been demonstrated at 1 GHz, however the performance diminishes rapidly at higher frequencies ( $100 \text{ dB}\cdot\text{Hz}^{2/3}$  at 20 GHz) [GCC+93]. In addition, these performances in uncooled directly modulated lasers are dependent on temperature, with SFDR of  $100.3 \text{ dB}\cdot\text{Hz}^{2/3}$  at  $25^\circ\text{C}$  dropping to  $90 \text{ dB}\cdot\text{Hz}^{2/3}$  at  $85^\circ\text{C}$  [QHI+05].

In contrast to directly modulated links, externally modulated links can have high SFDR at much higher frequencies, but suffer from lower SFDR at lower frequencies.

The Mach-Zehnder modulator can be biased at the quadrature point so that very high output powers are possible.  $117 \text{ dB}\cdot\text{Hz}^{2/3}$  was demonstrated for a modulator from 2 to 17 GHz. The performance of these types of links can be improved using high power detectors: A second-order limited  $119 \text{ dB}\cdot\text{Hz}^{2/3}$  and a third-order limited  $123 \text{ dB}\cdot\text{Hz}^{2/3}$  were demonstrated using a photodetector with a +32 dBm third-order intercept point [WNE98]. Likewise, optical power handling ability have typically limited the linearity of links using electroabsorption modulators when biased at quadrature [CAB+06]. However, the electroabsorption modulator can be biased so as to minimize 3<sup>rd</sup> order distortion, and thus sub-octave (intermodulation distortion-limited) EAM links have been demonstrated at 10 GHz with an SFDR of  $128 \text{ dB}\cdot\text{Hz}^{4/5}$  [LSC+03].

Lithium niobate Mach-Zehnder modulators have been the *de facto* standard for externally modulated links with many decades of engineering development. These types of modulators benefit from the linear electro-optic effect, in which the phase shift in either arm of the modulator is linearly proportional to the voltage. Most high-speed silicon modulators, however, rely on the carrier-depletion of a PN junction. Due to the nature of carrier-depletion modulation, the transfer function contains additional nonlinearities not exhibited in more conventional optical modulation platforms.

Vacondio *et al.* have studied the third-order nonlinearity of a Mach-Zehnder Modulator (MZM) and found it to be attractive for certain communications applications with low inter-modulation distortion [VMB+10], but the SFDR was not reported. Recently, Ayazi *et al.* have characterized the nonlinearities in a silicon ring modulator and found a third-order limited SFDR as high as  $84 \text{ dB}\cdot\text{Hz}^{2/3}$  [ABL+12] and Gutierrez *et al.* presented a ring-assisted MZM with SFDR of  $71.65 \text{ dB}\cdot\text{Hz}^{2/3}$  [GGH+12]. Additionally, Khilo *et al.* have presented a thorough study of the nonlinearities of a silicon MZM, as well as a biasing and detection scheme to linearize the device [KMK11]. This work aims to demonstrate the viability of silicon optical modulators in analog optical links.

## 4.2. Nonlinear Distortions in a Mach-Zehnder Modulator

Full spur-free dynamic range measurements of an analog optical link can be difficult or costly to perform. Here, I will derive an analytic link model to predict the nonlinear distortions from a DC description of the modulator transfer function. I have previously derived this relationship in [S12]. To begin, first consider a linear time invariant system with transfer function  $H(j\omega)$ . If we apply an input  $X(j\omega)$ , the system output is described as  $Y(j\omega) = H(j\omega)X(j\omega)$ . However, in the presence of nonlinearities, the standard frequency response of the system cannot describe the input-output behavior of the device. Instead, the output function may be described as a general function of the input,  $x(t)$ , denoted here as  $Y(x)$ . For analog signaling, we typically assume “small-signal” behavior. In the small-signal regime, approximation techniques such as Taylor expansions can accurately predict complex behavior. The Taylor series expansion of  $Y(x)$  about  $x = a$  is:

$$Y(x) = \sum_{n=0}^{\infty} c_n x^n = c_0 + c_1(x - a) + c_2(x - a)^2 + c_3(x - a)^3 + \dots \quad (1)$$

where  $c_n$  are the series coefficients:

$$c_n = \frac{1}{n!} \left( \frac{d^n Y}{dx^n} \right)_{x=a}$$

For sinusoidal inputs  $x(t) = \sin(2\pi f t)$ , the Taylor expansion shown in (1) about  $x = 0$ , becomes:

$$\begin{aligned} Y(x) &= \sum_{n=0}^{\infty} c_n \sin^n(2\pi f t) \\ &= c_0 + c_1 \sin(2\pi f t) + c_2 \sin^2(2\pi f t) + c_3 \sin^3(2\pi f t) + \dots \end{aligned} \quad (2)$$

From the double-angle trigonometric identity, (2) may be rewritten:

$$Y(x) = c_0 + c_1 \sin(2\pi ft) + \frac{c_2}{2} \sin(4\pi ft) + \frac{c_3}{4} \sin(6\pi ft) + \dots \quad (3)$$

Thus, it can be shown that harmonic distortion and intermodulation distortion may create output frequency components at frequencies other than those of the input. Often times for a single input frequency, the third order nonlinearity is far outside the pass band of the system. However, if two in-band sinusoids of near but distinct frequencies are present, the third order effect will create an additional term that is also in-band. For example, consider a double sideband suppressed carrier wave represented as:

$$x(t) = a_1 \cos(2\pi f_1 t) + a_2 \cos(2\pi f_2 t) \quad (4)$$

The  $n = 2$  term from (2) is expanded:

$$\begin{aligned} c_2 x^2 &= c_2 (a_1 \cos(2\pi f_1 t) + a_2 \cos(2\pi f_2 t))^2 \\ \Rightarrow &\left[ \frac{c_2 a_1^2}{2} + \frac{c_2 a_2^2}{2} \right] + \frac{c_2 a_1^2}{2} \cos(4\pi f_1 t) + \frac{c_2 a_2^2}{2} \cos(4\pi f_2 t) \\ &+ c_2 a_1 a_2 \cos(2\pi(f_1 + f_2)t) \end{aligned} \quad (5)$$

And, similarly, the  $n = 3$  term from (2) is expanded:

$$\begin{aligned} c_3 x^3 &= c_3 (a_1 \cos(2\pi f_1 t) + a_2 \cos(2\pi f_2 t))^3 \\ \Rightarrow &\left[ \frac{3c_3 a_1^3}{4} + \frac{3a_1 a_2^2}{2} \right] \cos(2\pi f_1 t) + \left[ \frac{3c_3 a_2^3}{4} + \frac{3a_2 a_1^2}{2} \right] \cos(2\pi f_2 t) \\ &+ \frac{c_3 a_1^3}{2} \cos(6\pi f_1 t) + \frac{c_3 a_2^3}{2} \cos(6\pi f_2 t) \\ &+ \frac{3c_3 a_1 a_2^2}{4} (\cos((2(2\pi f_1) + 2\pi f_2)t) \\ &+ \cos((2(2\pi f_1) - 2\pi f_2)t)) \\ &+ \frac{3c_3 a_2 a_1^2}{4} (\cos((2(2\pi f_2) + 2\pi f_1)t) \\ &+ \cos((2(2\pi f_2) - 2\pi f_1)t)) \end{aligned} \quad (6)$$

The frequency doubling effect in the  $n = 2$  term is known as harmonic distortion. For the  $n = 3$  expansion, the additional in-band sinusoidal terms at  $2f_2 - f_1$  and  $2f_1 - f_2$  are known as intermodulation distortion. Here, I am ignoring terms for  $n > 3$  under the assumption that these higher order effects are sufficiently attenuated.

Representing the carrier wave input in (4) as a sum and difference of frequency  $f_m$  on a principal frequency  $f_c$ :

$$x(t) = a_1 \cos(2\pi(f_c + f_m) t) + a_2 \cos(2\pi(f_c - f_m) t) \quad (7)$$

Thus, it is shown that intermodulation distortion results in additional output sinusoids at frequencies:

$$f = f_c \pm n f_n \quad (8)$$

while harmonic distortion results in output frequencies at:

$$f = m f_c \pm n f_n \quad (9)$$

The transfer function and its first three derivatives of a Mach-Zehnder modulator biased at quadrature are:

$$I_{out} = \frac{G I_{in}}{2} (1 + \sin(\phi)) \quad (10)$$

$$\frac{dI_{out}}{dV} = \frac{G I_{in}}{2} \cos(\phi) \phi' \quad (11)$$

$$\frac{d^2 I_{out}}{dV^2} = \frac{G I_{in}}{2} [-\sin(\phi) \phi'^2 + \cos(\phi) \phi''] \quad (12)$$

$$\frac{d^3 I_{out}}{dV^3} = \frac{G I_{in}}{2} [-\cos(\phi) \phi'^3 - 2 \sin(\phi) \phi' \phi'' - \sin(\phi) \phi' \phi'' + \cos(\phi) \phi'''] \quad (13)$$

Where  $\phi$  is the phase vs. voltage relationship of the modulator and is a nonlinear a function of voltage  $V$ ,  $I_{in}$  is the intensity of input light, and  $G$  is the optical insertion loss of the modulator.

From the previous section, it can be shown that the harmonic distortion in the optical signal is defined as:

$$SHD = \frac{1}{2!} \frac{d^2 I_{out}}{dV^2} \Big|_{V=0} \frac{1}{2} V_0^2 \cos(2\omega t) \quad (14)$$

For input  $V = V_0 \cos(\omega_1 t) + V_0 \cos(\omega_2 t)$ , the intermodulation product for the optical signal is:

$$IMD_3 = \frac{1}{3!} \frac{d^3 I_{out}}{dV^3} \Big|_{V=0} \frac{3}{4} V_0^3 \cos(2\omega_2 t - \omega_1 t) \quad (15)$$

To obtain a prediction for the SFDR measured at a spectrum analyzer after a photodetector, one may use the following conversion from optical power into electrical power in dBm:

$$P_{sig} = 10 \log \left( \frac{(P_{recv} \sigma)^2}{1000 \cdot R} \right) \quad (16)$$

where  $P_{recv}$  is the optical power at the photodetector,  $\sigma$  is the response of the photodetector in Volts/Watt, and  $R$  is the impedance of the receiving electronics.

### 4.3. Linearity Measurements of a Silicon Optical Modulator

A traveling wave silicon Mach-Zehnder modulator was fabricated in a similar process as described in Chapter 3. The mask layout and micrograph of the device are shown in

Figure 4.1. Just as before, the device is unbalanced by  $100\ \mu\text{m}$ . DC measurements are performed by optically and electrically probing the device and measuring the spectrum at various reverse bias voltages. Each arm of the Mach-Zehnder was tested individually. Phase shift was extracted by examining the shift in the optical spectrum at various bias voltages, as demonstrated in Figure 4.2. Experimental data for the phase shift as a function of voltage is shown in Figure 4.3. This device exhibits a  $V_{\pi}L$  figure of merit of  $3.33\ \text{V}\cdot\text{cm}$  and  $4.77\ \text{V}\cdot\text{cm}$  for the top and bottom arms, respectively.

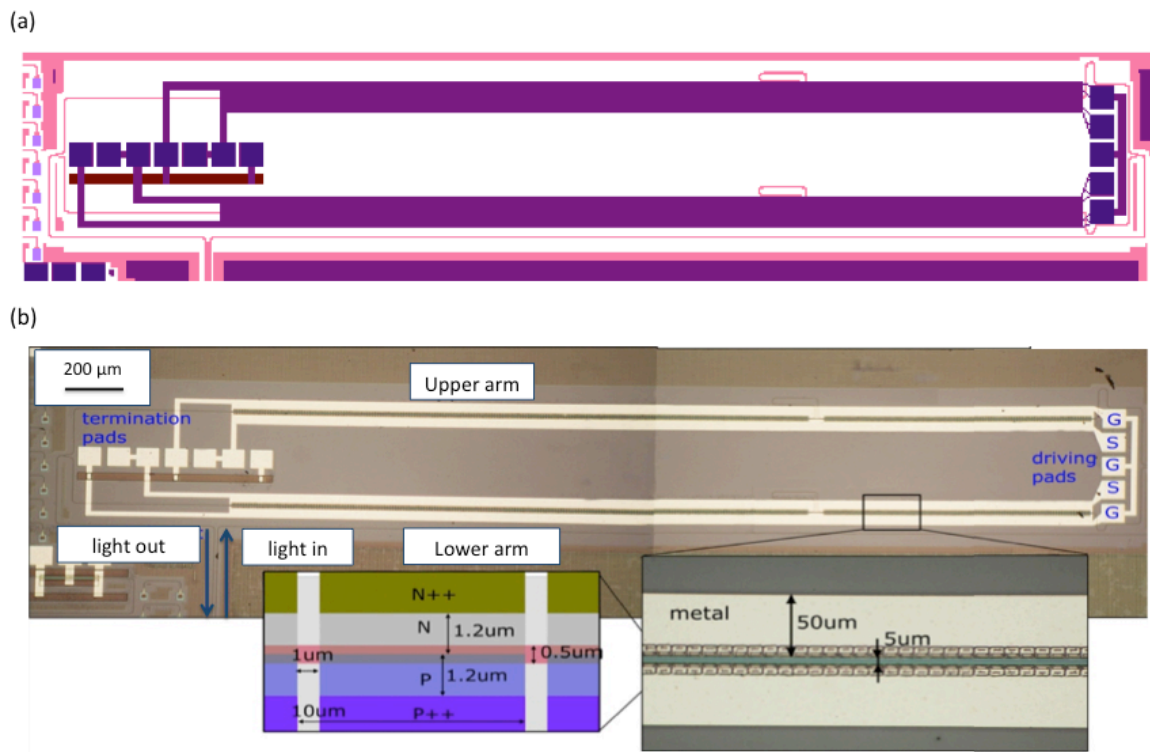


Figure 4.1: Image and layout of the analog TWMZ device. (a) Illustration of the mask layout of the device. (b) Micrograph of the fabricated device. Inset is an illustration of the PN junction geometry.

The DC phase shift vs. voltage data for each arm was fit with a third order polynomial of the form:

$$\phi = bV + cV^2 + dV^3 \quad (17)$$

where  $V$  is the reverse bias across the junction. Table 1 lists the extracted fit parameters for each arm of the MZM. The linear term,  $b$ , indicates the small signal performance and a corresponding small-signal  $V_{\pi}L$  figures of merit of  $2.3 \text{ V}\cdot\text{cm}$  and  $2.4 \text{ V}\cdot\text{cm}$  for the top and bottom arms, respectively. Note that the data for the bottom arm phase shift versus reverse bias voltage is negated in order to compare against the performance of the top arm.

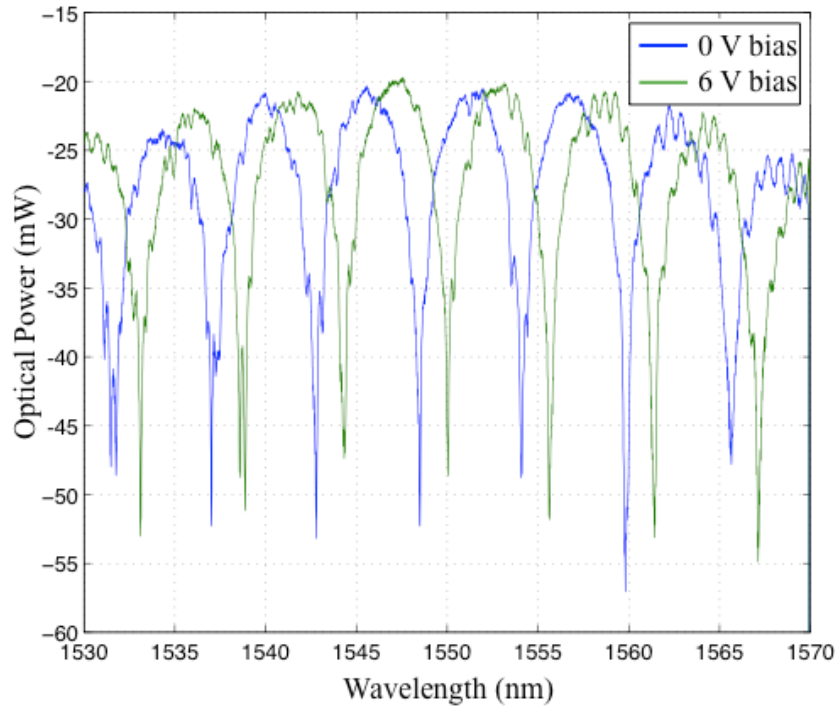


Figure 4.2: Optical transmission versus wavelength at 0 V and 6 V reverse bias conditions of the bottom arm of the device.

Based on the fit of the phase shift versus junction bias at a 0 V bias, we predict a 2<sup>nd</sup> order limited  $\text{SFDR}_{\text{SHD}}$  of  $87 \text{ dB}\cdot\text{Hz}^{1/2}$  for a differentially driven MZ and  $75 \text{ dB}\cdot\text{Hz}^{1/2}$  when driving only a single arm. The gain achieved by differential drive for second harmonic distortion is limited by the relative pn-junction performance of each arm. The difference in phase shift performance between the top and bottom arms, while not known, is assumed to be due to mask misalignment during processing. Since the top and bottom arms exhibit different nonlinearities, biasing the modulator at quadrature does not cancel

the second order term as it does for a linear electrooptic effect modulator. This model also predicts an  $SFDR_{IMD}$  of  $94 \text{ dB}\cdot\text{Hz}^{2/3}$  and  $96 \text{ dB}\cdot\text{Hz}^{2/3}$  for the single arm and differential drive cases, respectively. In this case, the third order SFDR is expected to improve by 2 dB not due to cancellation of the third order terms from the pn-junction nonlinearity, but because differential drive effectively increases the output powers of the fundamental and distortion terms by 3 dB.

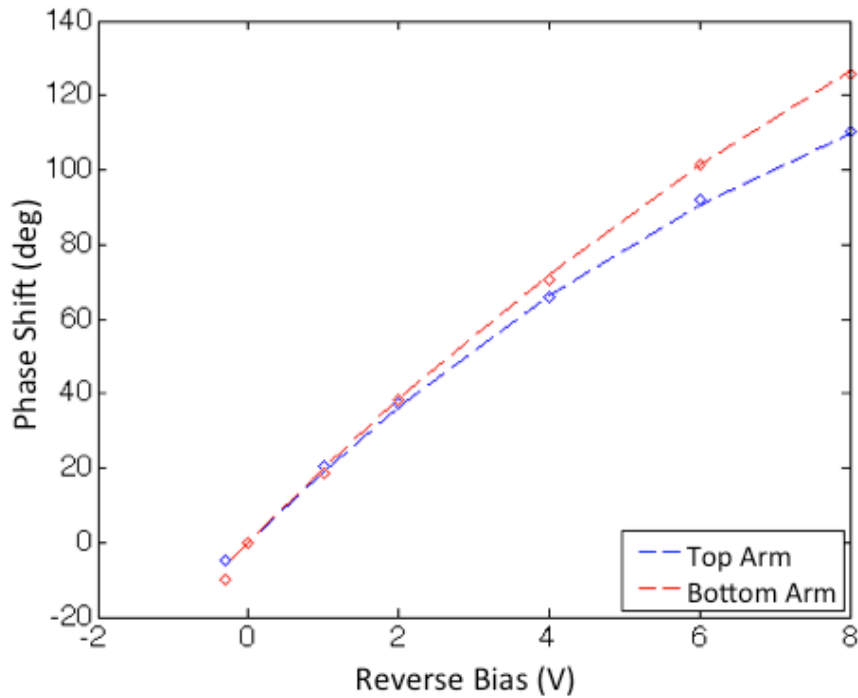


Figure 4.3: Measured phase shift versus reverse bias voltage of each arm of the MZM. The dashed lines are polynomial fits of each data series.

Table 4.1: Fitting parameters for the phase response of the 3.0 mm long traveling wave modulator as a function of reverse bias

MZM arm	b (rad/V)	c (rad/V <sup>2</sup> )	d (rad/V <sup>3</sup> )
Bottom	0.398	0.0189	$3.95 \times 10^{-4}$
Top	0.408	-0.0142	$2.83 \times 10^{-4}$

A tunable laser light source is input into an erbium-doped fiber amplifier and then through a polarization rotator. The polarized light is coupled into the modulator from an optical fiber with a grating coupler holographic lens and routing waveguides. The modulated signal is coupled back into an optical fiber with another grating coupler. Each grating coupler has a known  $4.4 \pm 0.2$  dB loss and the waveguides have  $2.2 \pm 0.8$  dB/cm loss. To achieve quadrature, the wavelength of input light is adjusted to the -3 dB point in the spectrum. The principal limiting factor of this test was the photodetector saturation power of 2 mW. The experimental setup is shown in Figure 4.4.

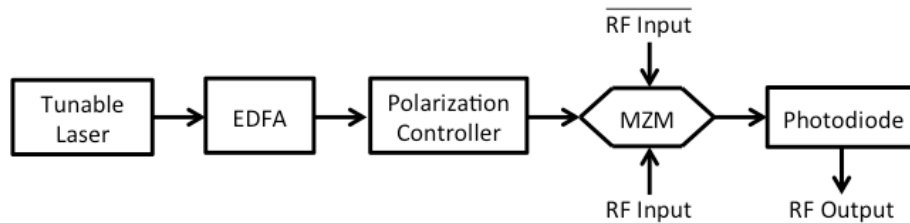


Figure 4.4: SFDR experiment block diagram. When driving the MZM in the single arm configuration, the RF input is applied only to the bottom arm.

An arbitrary waveform generator (AWG) and a vector network analyzer (VNA) are used as signal sources. The AWG is capable of producing complementary signals, while the VNA is not. To create a complementary signal, the VNA output is passed through a splitter and recombined after delaying one path with close to three inches of additional rf cabling. The frequency of modulation was adjusted to tune the phase difference and achieve complementary signals. Two signals near 1 GHz were applied to the MZM. In principle, higher bandwidth signals could be used but is limited here by the detection bandwidth of the spectrum analyzer. The detector is a New Focus 1414 photodetector, which has a conversion gain of 15 V/W and responsivity of 0.6 A/W. The bandwidth of the device was measured to be 15.5 GHz, as indicated in Figure 4.5.

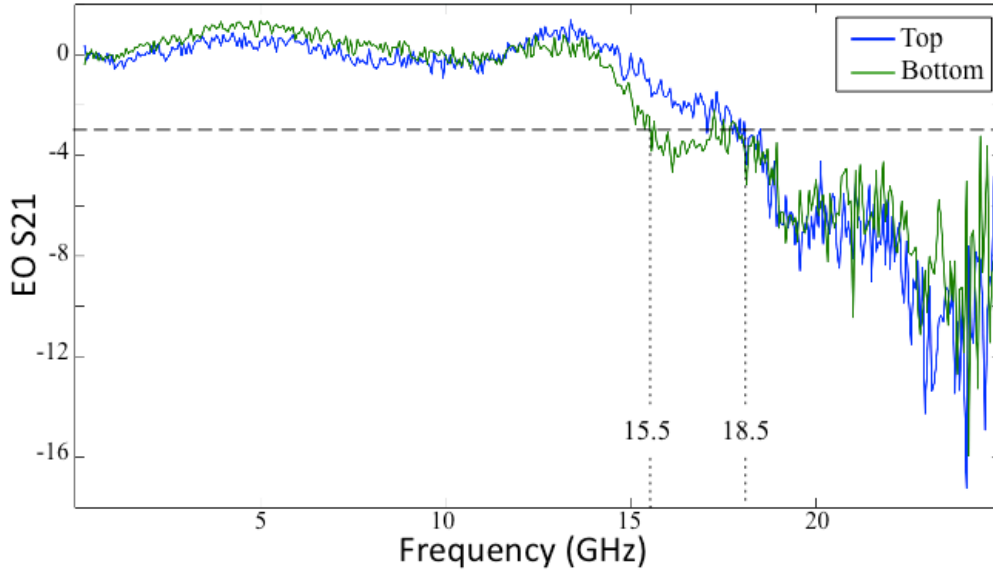


Figure 4.5: Electrooptic S21 for each arm of the MZM. Driven differentially, the device has 15.5 GHz bandwidth.

A typical RF spectra of intermodulation distortion is presented in Figure 4.6. The nonlinearity of the MZM driven by a single arm is presented in Fig. 7 and the nonlinearity of the differentially driven MZM is shown in Fig. 8. The EDFA amplified the tunable laser to about 500 mW and 1 mW of light is received at the photodetector. Excess losses due to the implants in the MZM in this process have been reported to be 10 dB/cm [6], and the total insertion loss of the device biased at quadrature is 6.7 dB. A noise floor of -165 dBm/Hz, limited by optical amplifier noise, was observed and is used to calculate SFDR. A noise figure for the test setup link of 58 dB is measured. This figure could be improved in the future by improving the slope efficiency with a longer device, however, at the cost of a reduced bandwidth.

$SFDR_{SHD}$  and  $SFDR_{IMD}$  for the single arm case at 0 V bias are found to be  $72 \text{ dB}\cdot\text{Hz}^{1/2}$  and  $92 \text{ dB}\cdot\text{Hz}^{2/3}$ , respectively. By differentially driving the modulator the SFDR is found to increase to  $82 \text{ dB}\cdot\text{Hz}^{1/2}$  and  $97 \text{ dB}\cdot\text{Hz}^{2/3}$  for  $SFDR_{SHD}$  and  $SFDR_{IMD}$ , respectively. For both single arm and differential drive operation, these values are within 5 dB of the expected performance from DC measurements of the pn junction nonlinearity. This suggests that the junction is the dominant nonlinearity for this system.

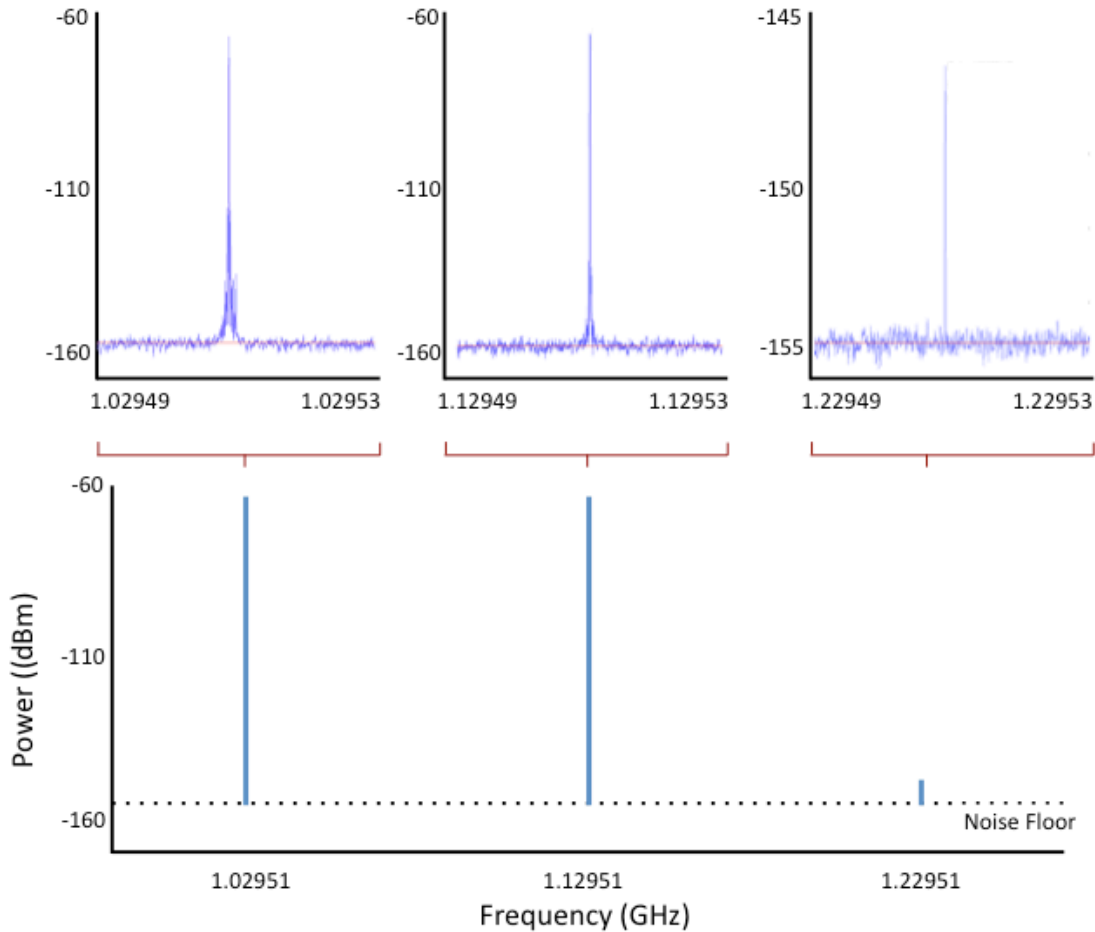


Figure 4.6: RF spectra of the fundamental tones at 1.02951 and 1.12951 GHz and the intermodulation distortion at 1.22951 GHz. These measurements are taken at a 10 Hz resolution bandwidth. The full range of 1 GHz to 1.3 GHz is not swept at this resolution bandwidth due to the slow sampling time, and a reconstructed spectrum is shown instead. The RF noise in this regime was observed to be uniformly around the noise floor of -165 dBm/Hz during test.

Additionally, since there is a known optical loss after the device, the SFDR of this optical link may be improved in the future. After the output of the MZM, there is 1.2 dB of loss in the routing waveguides, and 6.3 dB of net loss under testing conditions due to the grating coupler. One cannot generally normalize out optical losses from an SFDR calculation, since this neglects the possible power-handling limitations of the devices. But known losses that occur after the device can certainly be removed with improved engineering efforts, without affecting the power that flows through the device. This

improvement would be realized in optical links that use photodetectors with higher saturation currents. In fact, a high-speed photodetector fabricated in this platform has previously been demonstrated to exhibit linear behavior for optical powers up to 7.8 mW [24].

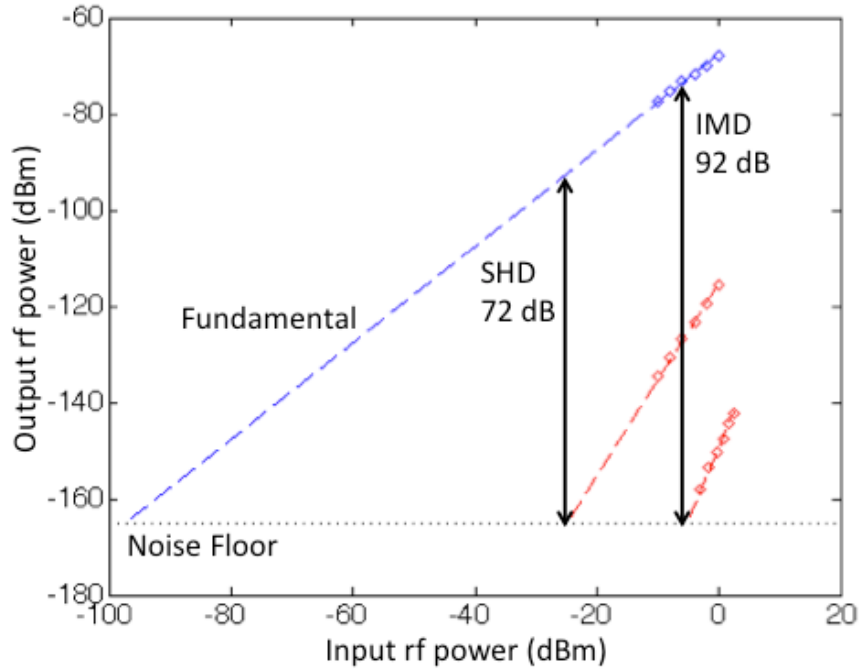


Figure 4.7: Output power vs. input power of the second harmonic distortion and intermodulation distortion for an MZM driven by a single arm. Spur-free dynamic ranges of  $72 \text{ dB}\cdot\text{Hz}^{1/2}$  and  $92 \text{ dB}\cdot\text{Hz}^{2/3}$  are measured for  $\text{SFDR}_{\text{SHD}}$  and  $\text{SFDR}_{\text{IMD}}$ , respectively.

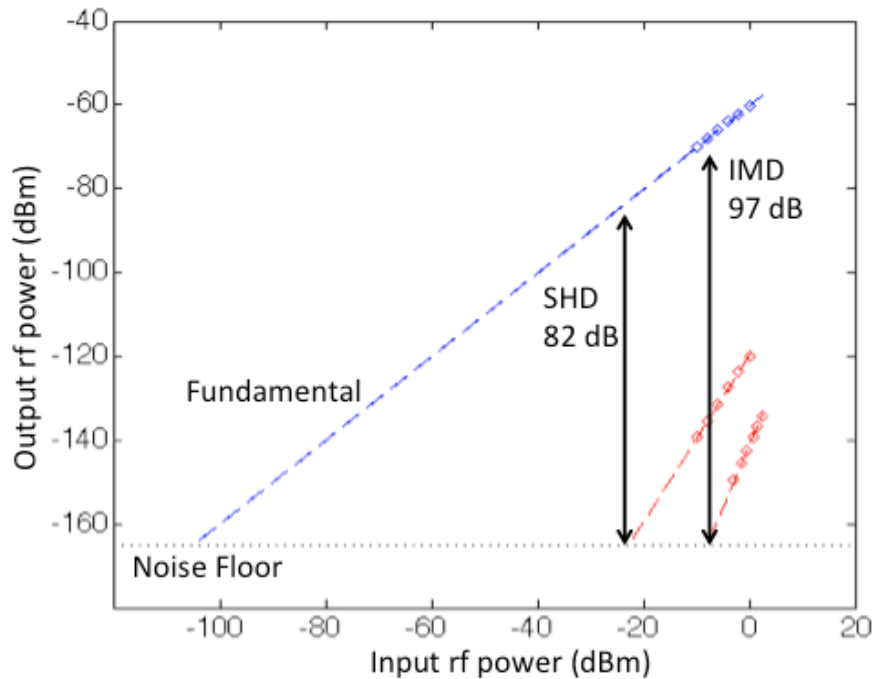


Figure 4.8: Output power vs. input power of the second harmonic distortion and intermodulation distortion for a differentially driven MZM. Spur-free dynamic ranges of  $82 \text{ dB}\cdot\text{Hz}^{1/2}$  and  $97 \text{ dB}\cdot\text{Hz}^{2/3}$  are measured for  $\text{SFDR}_{\text{SHD}}$  and  $\text{SFDR}_{\text{IMD}}$ , respectively.

In this case, note that only about 50 mW of optical power enters the input waveguide of the MZM due to losses from a polarization controller ( $<1 \text{ dB}$ ), insertion loss from the fiber array to the on-chip grating coupler (6.3 dB), routing waveguides (1 dB), and y-junction (4 dB). This optical power is well below the power saturation limit of typical silicon photonics devices with these dimensions [25]. Presumably, the SFDR could be further improved by increasing the optical power in the device, through either a more powerful input optical signal, or lower coupling losses. Also note that the propagating power in the results described in [19, 20] was on the order of 500 mW and 240 mW, respectively.

#### 4.4. Conclusions

An outstanding question has been whether the analog performance of silicon components can compete with conventional optical material systems such as Lithium Niobate. A key challenge for silicon photonics is the fact that most modulators, including the one reported here, are based on a reverse biased PN junction. PN junctions exhibit significant nonlinearities, and it has thus been unclear whether analog performance in the silicon platform could ever compete with what has been achieved with Lithium Niobate based modulators.

Characterized here is one of the key metrics for analog performance, the Spur Free Dynamic Range (SFDR). This is a measure of the degree of nonlinear cross-talk between different frequencies propagating in a single system. With the proper device configuration, this work shows that the SFDR of a silicon modulator can approach that of Lithium Niobate based systems. In particular, this modulator achieves  $104.5 \text{ dB}\cdot\text{Hz}^{2/3}$  SFDR for IMD, which is within 15 dB of the best result in Lithium Niobate,  $120.5 \text{ dB}\cdot\text{Hz}^{2/3}$ . This level of performance is also already sufficient for a number of analog applications, including WLAN for picocellular networks.

There are a number of reasons to believe that performance in integrated silicon photonic systems can be improved in the future, and likely match the performance seen in the very best optical systems for analog links. Firstly, the SFDR of the link could be improved by reducing the insertion loss of the silicon PIC to enable higher launch powers with available laser technologies. Additionally, high power photodetectors have been demonstrated in silicon, with saturation currents up to 65 mA [LST+14]. Secondly, the integration of silicon photonics enables complicated RF systems, and broadband linearization schemes too complicated for larger optical components could potentially scale effectively for silicon. As the silicon platforms mature, analog and digital links of increasing complexity will certainly become more common.

## **Chapter 5. A 2.4 Tb/s Parallel Single Mode Silicon Photonic Link**

In this chapter I present the design and test of a terabit optical link fabricated in a silicon material system. The link consists of 48 modulator and photodetector channels, each operating at 50 Gb/s. This result demonstrates that it is possible to build large optical systems operating at high data rates on a silicon platform with reliable yield and performance. I performed the design, layout, fabrication, and testing of this system. Ari Novack assisted with the fabrication and testing. Ran Ding and Yang Liu assisted with the modulator device design. This work was published in the *IEEE Journal of Lightwave Technology*:

**M. Streshinsky**, A. Novack, R. Ding, Y. Liu, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, “Silicon nanophotonic parallel single mode 48×50 Gb/s transmitter and receiver,” *IEEE J. Lightw. Technol.*, vol. 32, no. 22, pp. 3768-3775, 2014.

### **5.1. High Bandwidth Silicon Optical Links**

As consumer demand for services such as streaming media and cloud computing rise, there is a greater need for high complexity and low cost optical transceiver technologies in the data center. Within modern data centers the computing infrastructure to support this demand may extend between racks, or even between buildings, and will require integrating more communications ports into the same rack space with reaches of up to 2 km [VHZ+11, DJM+13]. This level of networking scale will necessitate cost effective many-channel links using single mode fiber at aggregate bandwidths of terabit/s and beyond [LLJ+10].

Furthermore, within the development of next-generation supercomputers, there is a growing demand for similar I/O reach and bandwidth targets as in the datacenter [B14]. The available bandwidth for on and off-chip communication decreases as the number of cores in a multi-core processor increases. Using current memory access architectures,

there is a bottleneck between the processor and DRAM [HRG+10]. With required line speeds predicted to reach 40 Gb/s by 2020 [ITRS09], there are no known electrical solutions for meeting these needs and highly integrated photonic transceivers are one solution to overcoming this bottleneck. Photonics also has the advantage of being relatively distance and data rate agnostic, which allows for the disaggregation of hardware for large computing clusters. Thus, as high performance computing facilities grow, their interconnect needs can mirror that of the data center—with the additional desire to co-locate the I/O onto the physical chips.

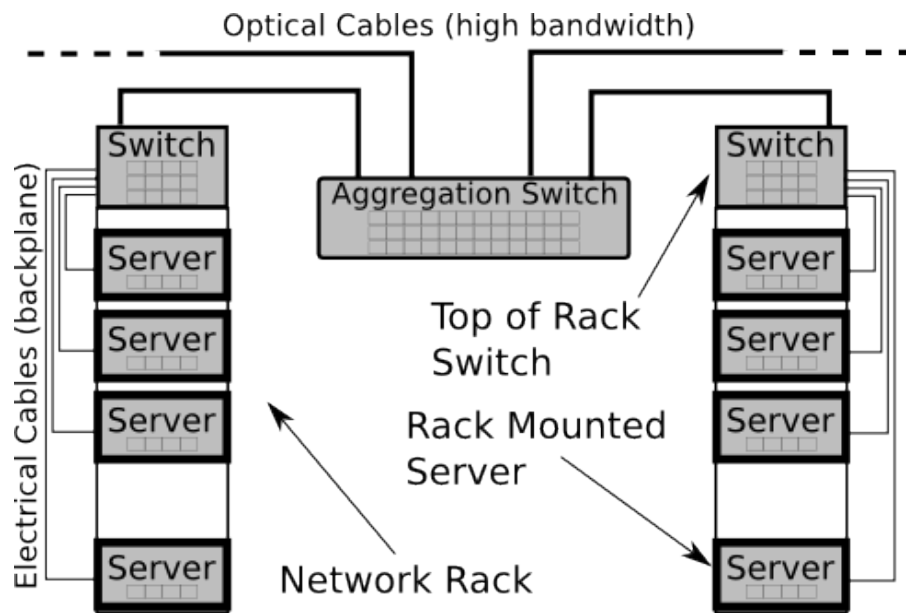


Figure 5.1: Diagram of the common “Top of Rack” datacenter architecture. Each server in a given rack is routed to a switch at the top of the rack. The top-of-rack switch then communicates with the aggregation switch.

For current-generation data center interconnects, photonics has mostly taken the form of pluggable transceivers, but there is also room for higher degrees of photonic integration. Current top of rack switches make use of active optical cables for high bandwidth links (see Figure 5.1). However, large numbers of these cables are needed and the cost is relatively high. By integrating the photonic chip directly into the switch as seen in Figure 5.2, passive optical cables can be used at the output of the switch, lowering

complexity and increasing aggregate bandwidth [F10]. Due to the high cost of packaging, the reduction in complexity provided by the mid-board solution results in significantly lower cost for the entire system [KBW+13].

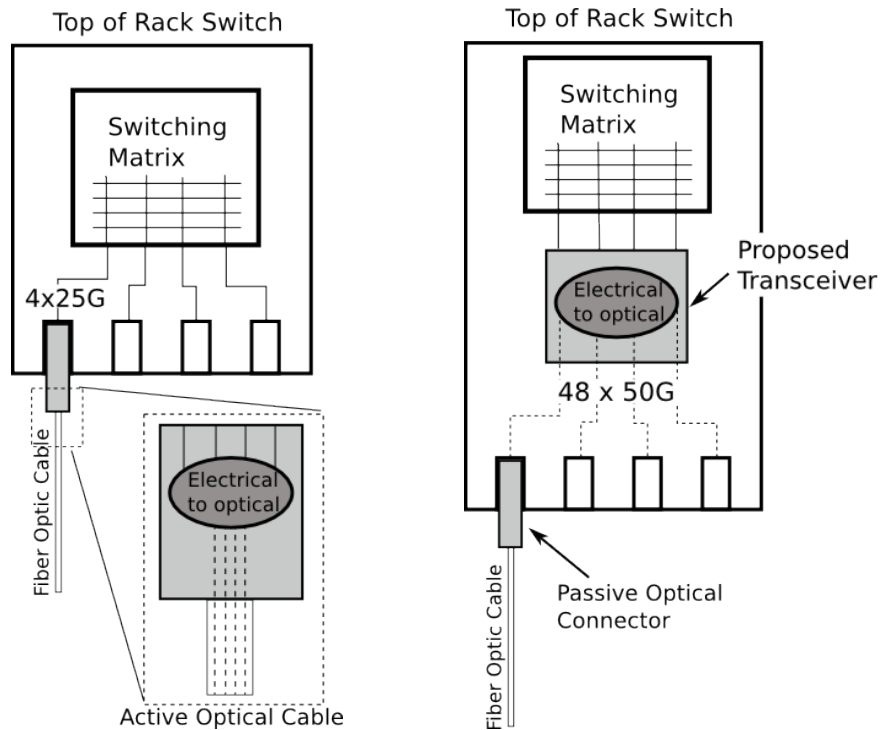


Figure 5.2: New architecture enabled by mid-board optics. On the left is the current architecture of top-of-rack switches. These have electrical outputs and use active optical cables to convert the signal to/from light. A mid-board optical chip that could do the electrical/optical conversion will enable 400G+ communications while drastically increasing port density and replacing a large number of active optical cables with a single chip.

There are several promising technologies and material systems to enable this style of mid-board highly integrated terabit/s interconnect. These include vertical cavity emitting semiconductor lasers (VCSELS), indium phosphide, and silicon photonics. Discrete optics based solutions have been the default choice in the telecom market due to a legacy of superior performance. However, for data center applications, the large form factors and cost prohibit their use. Additionally, when considering high data rate-distance

products, indium phosphide and silicon photonics stand out over VCSELS as the most promising contenders for high bandwidth systems.

Many of the common optical technologies in use today in the data center rely on a network of multimode fiber using VCSELS. VCSEL-based solutions have been adopted for many standard parallel datacom standards, including InfiniBand, SDR, DDR, QDR, Ethernet 40, and 100 GbE. Additionally, VCSEL data rates and reaches continue to improve, with recent demonstrations of a directly modulated VCSEL at 56 Gb/s [KSR+13] and OM4 fiber extending the effective modal bandwidth reach of multimode fibers to 4.7 GHz-km [B09]. However, as can be seen by these metrics, even using state of the art technology, creating VCSEL-based optical I/O that can operate at line rates greater than 25 Gb/s over one to two kilometers is not currently feasible.

Single mode indium phosphide with edge emitting lasers is promising for its ability to integrate many optical functions into a single photonic integrated circuit (PIC). Unlike silicon, the direct bandgap of InP enables on-chip lasers, which can be directly modulated. Additionally, most other standard optical functions can be built onto a single wafer. Generally, InP manufacturing technologies are not as mature as in silicon, which has benefited from tens of billions of dollars of investment from the electronics industry. However, even the larger defect density and lower process sophistication has not prevented the demonstration of very complex high-speed transceivers on InP chips, such as a 500 Gb/s aggregate data rate packaged transceiver [PSY+13]. While InP PICs are able to integrate a laser, the on-chip laser necessitates thermoelectric cooling, whereas off-chip lasers can be cooled in a more flexible form factor. Both InP and silicon photonics have overlapping application domains, where the ultimate material choice will depend on cost, performance, reliability, and power requirements.

Silicon photonics, in a similar vein to InP, is a promising platform for low-cost and high-speed optical interconnects [HB10, JF06]. Particularly, the monolithic integration of high-speed photodetectors [NGY+13, KLM+09, DKS+04], modulators [LRL+04, XMS+07, DLL+14], and low-loss passive components [MGM+11, LYT+12, NFH+11] enables the design of large-scale integrated photonic circuits. While silicon is not the best platform for every device in such a link, several silicon devices are already competitive

with best-in-class performance [KLM+09, HHD+13]. Moreover, a single silicon photonic chip can integrate hundreds to thousands of what may formerly have been discrete components. Using glass arrays of fiber or multi-core fiber interfaces, tens to hundreds of optical I/O are possible [KPW+14]. Thus, ultra-high-throughput systems can be built up on a single silicon chip.

A key unexplored question is whether it is, in fact, possible to obtain high yields across numerous channels on a silicon photonics chip, thus realizing the potential of the technology. The primary challenges in achieving this level of performance are the development of a well-characterized fabrication process and a library of stable and fabrication-tolerant devices. To address the former, there are several silicon platforms available to the public and in private industry, which include: Luxtera's 130 nm Freescale platform, Mellanox's 150 mm foundry, and MPW services through ePIXfab and OpSIS. In collaboration with the OpSIS-IME foundry service, we have access to a full suite of modulators, detectors, and passive devices capable of operating at data rates up to 50 Gb/s [XMS+07, SDL+13].

There are several architectures, modulation schemes, and fiber arrangements that may be used to construct an ultra-high-bandwidth silicon link, each with their own tradeoffs (see Figure 5.15). The vast majority of results in literature use wavelength-division-multiplexed systems. The result in [LDL+14] uses 8 ring modulators that are multiplexed on a single bus waveguide carrying each wavelength. By using thermal tuners embedded in each ring, the authors' are able to modulate 8 wavelengths each at 40 Gb/s, which represented nearly 3x improvement over other results using ring modulators. The results in [ZCS+13] use a similar technique, but at 10 Gb/s and with flip-chipped drivers and TIAs integrated. The primary achievement in this case is the dense integration of CMOS drivers with a silicon photonic chip via flip-chip integration for multi-channel 10 Gb/s data communications. The authors in [ZCS+13] also demonstrated error-free transmission on all 8 channels of their WDM transceiver.

Since resonant-based modulators in silicon have strong temperature dependences, many systems also use balanced Mach-Zehnder modulators [CDD+11, LLC08, DLC+13, ALJ+11, PAH+12, UUF+14], which are much less sensitive to temperature but require

more chip area and consume more energy. The results in [CDD+11, LLC08, DLC+13, ALJ+11, PAH+12] integrated some form of WDM on chip in combination with an array of MZMs. While WDM links can significantly improve the spectral efficiency of each fiber channel, this type of transmitter does incur additional expense in the form of lasers and wavelength filtering. In contrast, parallel single mode (PSM) links require fewer lasers but do need additional optical fibers. Urino, et al. [UUF+14] demonstrated a highly parallel link using an array of laser diodes, each split 4 ways, and directed into silicon MZMs with a line rate of 20 Gb/s. The parallel link by Urino, et al. is specifically targeted for silicon interposers, where the goal is to have several LSI chips flip chipped to the interposer. The primary differences between building optical interposers and mid-board data center interconnects is that for interposers, the target link reach is not much larger than 1 cm and the interconnect chip density is much more important. Here, a silicon transceiver with 48 x 50 Gb/s channels is proposed and demonstrated, for a total aggregate data rate of 2.4 terabits/s. The transmitter channels have been individually tested for sensitivity, insertion loss and power consumption. The photodetectors are tested for open eyes at 50 Gb/s.

## 5.2. Platform Capabilities

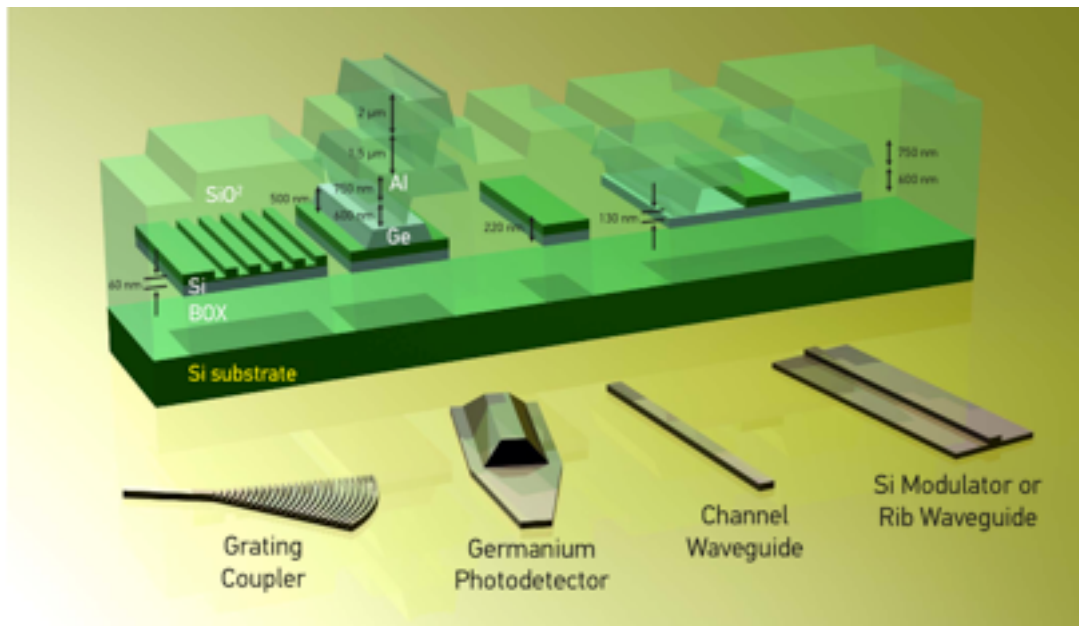


Figure 5.3: Cross-section and rendering of the key devices of the OpSIS platform (not to scale). Figure courtesy of [SDY+13].

In order to construct the parallel link, library components from the OpSIS process development kit (PDK) are used with minimal changes in order to ensure high yield and reliability. See Figure 5.3 for a cross section of the major devices. For optical I/O to and from the chip, grating couplers are used with an insertion loss of  $4.4 \pm 0.2$  dB at 1550 nm and 1.5 dB bandwidth of 50 nm [DBP+12]. Three types of waveguides are used on chip: 500 nm channel for short routing, strip-loaded 500 nm rib for the pn junction phase tuner and thermal phase shifter, and a wide 1.2  $\mu\text{m}$  channel waveguide for long routing. The wide routing waveguides, which constitute most of the on-chip optical path, result in  $0.27 \pm 0.06$  dB/cm loss [NLD+13]. A Y-junction with  $0.28 \pm 0.02$  dB excess loss is used as part of an on-chip splitter network and in the arms of the Mach-Zehnder modulator [ZYL+13].

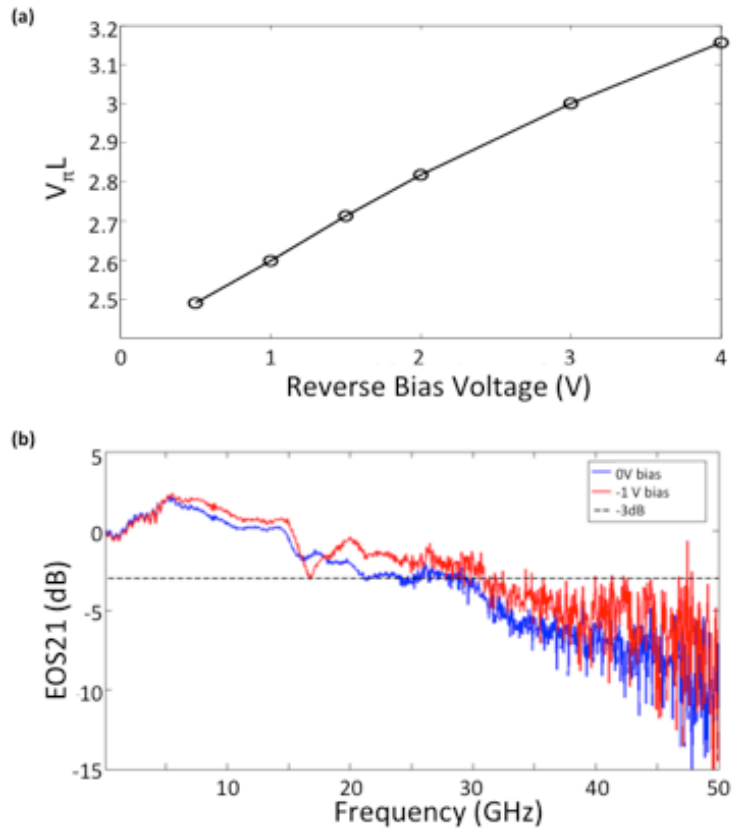


Figure 5.4: Performance of the PDK TWMZ. (a) The small signal  $V_{\pi L}$  versus bias voltage of the PDK traveling wave Mach-Zehnder modulator. The small signal  $V_{\pi L}$  is 2.6 V-cm at a -1 V reverse bias. (b) EOS21 response of the Mach-Zehnder modulator at 0 V and -1 V reverse bias.

The traveling-wave modulator used here has a 3-dB bandwidth of 30 GHz and a similar geometry for 1.3  $\mu\text{m}$  light has been shown to operate at 50 Gb/s [RLL+14, SDL+13]. A 3-mm long pn-junction phase shifter is used with periodic undoped striations such that the pn-junction encompasses 90% of the total phase shifter length. The implants add 11.1 dB/cm additional loss to the 2.0 dB/cm strip-loaded rib waveguide loss. The phase shifter has a small-signal  $V_{\pi}L$  at a -1V bias of 2.6 V-cm, and the 3-dB bandwidth of the modulator is 30 GHz at a -1 V reverse bias, as shown in Figure 5.4(a, b). The gain-peaked photodetector in the receiver chip has been previously shown to have a bandwidth of 67 GHz, responsivity of 0.75 A/W, and dark current of 0.61  $\mu\text{A}$  at a 2 V reverse bias [NGY+13]. Photodetector responsivity and bandwidth data from this wafer is shown in Figure 5.5(a, b).

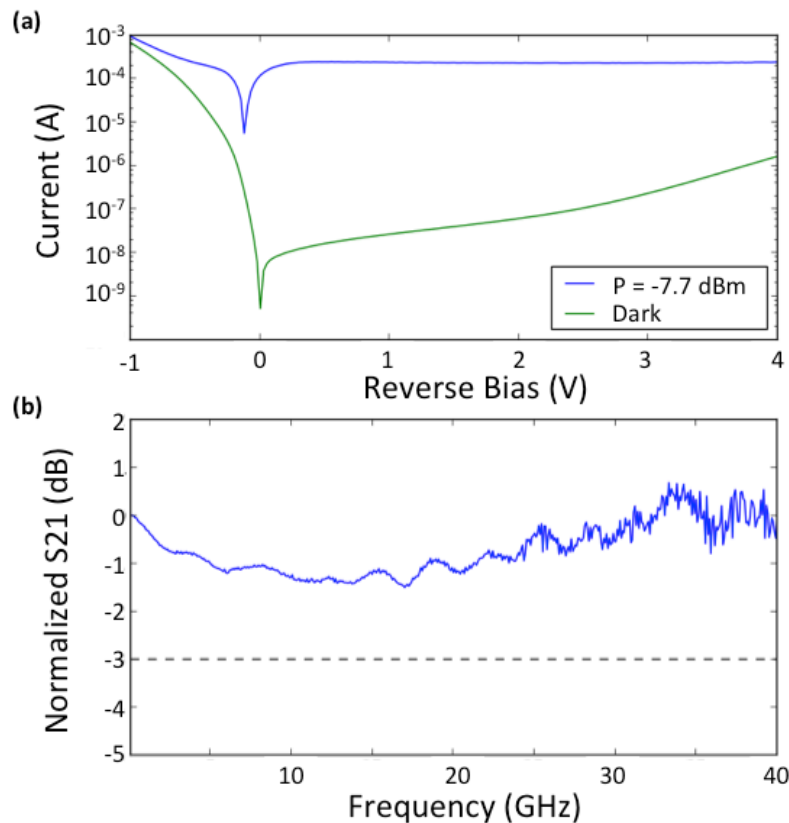


Figure 5.5: Performance of the PDK gain-peaked photodetector. (a) I-V response under illumination and dark showing 0.75 A/W responsivity and 0.61  $\mu\text{A}$  dark current at -2 V bias. (b) Frequency response showing 3-dB bandwidth in excess of 40 GHz.

### 5.3. System Design

The modulators and photodetectors are placed on separate chips on the same wafer. The modulator chip is 13.2 mm x 32 mm and the detector chip is 11.8 mm x 32 mm. The large size of these chips is to enable easier eventual packaging (the optical devices for the transceiver consume much less area than the total available chip area). Block diagrams and photographs of each channel of the transmitter and receiver chip are shown in Figure 5.6(a-d).

Light is coupled into the chips via grating couplers and, whenever possible, 1.2  $\mu\text{m}$  wide waveguides are used to minimize waveguide loss. On the modulator chip, there are 12 total laser inputs, each split 4 times to form 48 output channels. There are also 2 additional dedicated grating couplers to perform active alignment with a fiber array for eventual packaging. Thus, there are a total of 62 input grating couplers in the modulator chip. The receiver chip is similarly laid out with 48 input and 2 alignment grating couplers. All grating couplers are located in the center of the chips and are uniformly spaced in a single line at a 127  $\mu\text{m}$  pitch.

In order to reduce crosstalk, each photodetector is placed on a 900  $\mu\text{m}$  pitch and each modulator is placed on an approximately 815  $\mu\text{m}$  pitch, where the outer ground wires of the modulator transmission lines are separated by at least 300  $\mu\text{m}$ . The 70  $\mu\text{m}$  x 70  $\mu\text{m}$  RF input pads of the modulators are placed around the periphery of the chip in a GSGSG configuration, and are connected to 25  $\mu\text{m}$  long tapers that directly lead into the transmission line of each traveling wave modulator. On-chip RF termination is accomplished by using the n++ implanted silicon layer. These termination resistors are located at the end of the traveling wave modulator. DC pads for the thermal phase tuners in each arm of the Mach-Zehnder interferometer are placed along the bottom edge of the chip. Two layers of metal are used to route the DC phase tuner signals from each Mach-Zehnder to their respective pads. In total there are 98 DC bond pads evenly spaced along the bottom edge of the chip (2 thermal phase tuners for each channel and 2 common ground pads).

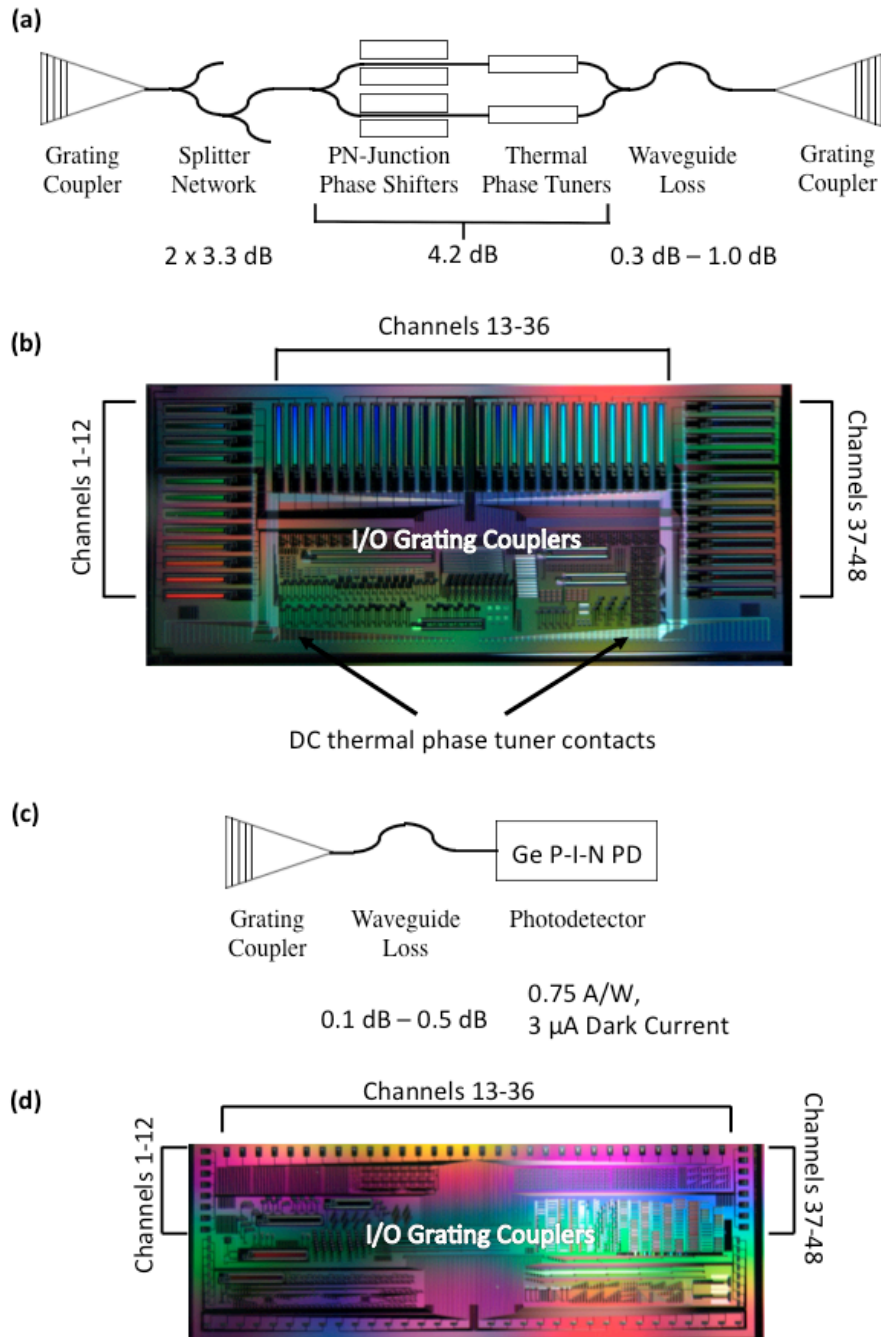


Figure 5.6: Block diagram (a, c) of each channel of the transmitter and receiver and photographs (b, d) of the transmitter and receiver chips with key features identified

The layout of the traveling wave modulator has been slightly modified from what is found in the OpSIS-IME process development kit (PDK). On the original PDK device, RF contact pads are present at either end of the transmission line. In this system, the terminating RF contact pads are replaced with on-chip termination resistors formed by

220 nm silicon implanted with n<sup>++</sup> doping. The typical n<sup>++</sup> sheet resistance is 65  $\Omega/\square$  and the termination resistor was targeted to be 33  $\Omega$  to match the transmission line impedance. Finally, resistors are embedded next to the waveguide after the pn junction phase shifter to form thermal phase tuners. These resistors are constructed from n<sup>++</sup>-doped silicon implanted in the 90 nm thick strip portion of a strip-loaded rib waveguide. Using thermal phase tuners to bias the device rather than changing the bias on the RF phase shifters is desirable for several reasons. First, it allows for much lower power operation than applying a bias on the transmission line since the device requires termination. Second, it allows the junction to operate at the same bias voltage across the chip—only the tuning power varies from device to device. Finally, since the depletion-mode phase shifters exhibit diminishing phase shifts at higher voltages, thermal phase tuners enable proper optical biasing no matter the electrical bias condition.

#### **5.4. Experimental Measurements of the Terabit Link**

##### *Testing Methodology*

The chip was tested on a wafer-scale test setup with optical and electrical probing. Optical coupling was achieved by a vertically incident array of fibers and input into on-chip grating couplers, which redirect the light from the fiber mode into the on-chip waveguide mode. The fiber array consists of a linear array of polarization maintaining fibers at a 127  $\mu\text{m}$  pitch. All testing is performed on a thermally-controlled chuck kept at 30  $^{\circ}\text{C}$ , although no significant changes in performance are expected based on small fluctuations in temperature. With only one test setup the two chips are tested separately: the transmitter is tested with a commercial receiver, and the receiver is tested with a commercial modulator.

For high speed testing of the transmitter, a tunable laser source was set to 1550 nm and input into an EDFA, the device under test, a second EDFA, a low pass filter, and finally a variable attenuator before being received by a Picometrix AD10-ir photoreceiver. The photoreceiver has a rated sensitivity at 40G of -8 dBm. Each Mach-Zehnder modulator was biased at the -3 dB point by changing the power input to the

thermal phase tuners embedded in each arm of the interferometer. For BER and eye diagram testing, an Anritsu MP1822A is used to generate and analyze the 50 Gb/s PRBS31 pattern. Eye diagrams were measured using an Agilent 86100C Digital Communications Analyzer (DCA). The reference lithium niobate modulator that was used to compare this transmitter against is a Covega LN05S MZM driven to high extinction with a Centellax OA4MVM3 modulator driver. Similarly, the receiver is tested using the same tunable laser, first EDFA, and bandpass filter. Each photodetector in the receiver is probed with a  $50\ \Omega$  terminated microprobe and input into the same Centellax amplifier used to drive the lithium niobate modulator. See Figure 5.7(a, b) for a block diagram illustration of these two respective test setups.

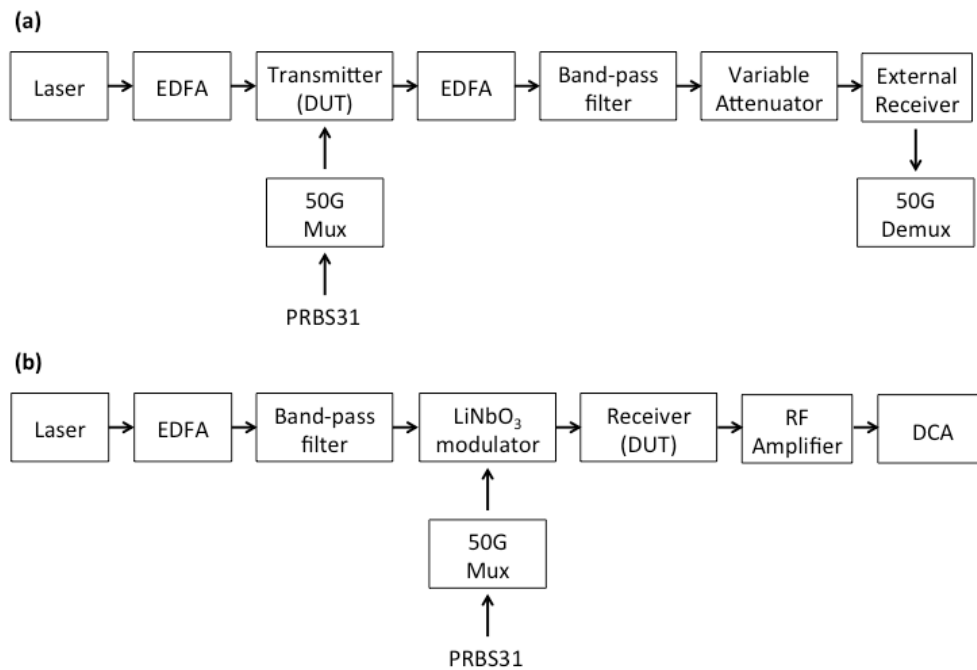


Figure 5.7: Block diagrams of the test setup for the transmitter (a) and receiver (b) chips.

### *DC performance*

All 48 channels of the transmitter were tested for insertion loss and BER versus received optical power. The on-chip insertion loss is  $-11.89 \pm 0.83$  dB, which includes routing waveguides and two Y-junctions to split each input channel into four output channels. The variation of the on-chip insertion loss is likely an overestimate of the

actual variation due to unaccounted-for differences in the grating coupler efficiencies between channels as well as measured differences in optical waveguide path lengths. The grating couplers used in this testing have been previously characterized and found to have an average insertion loss of  $4.4 \pm 0.2$  dB. Loss due to routing waveguides varies from 0.3 dB to 1.0 dB due to path length differences between channels. The optical losses across the 48 channels are summarized in Figure 5.8(a).

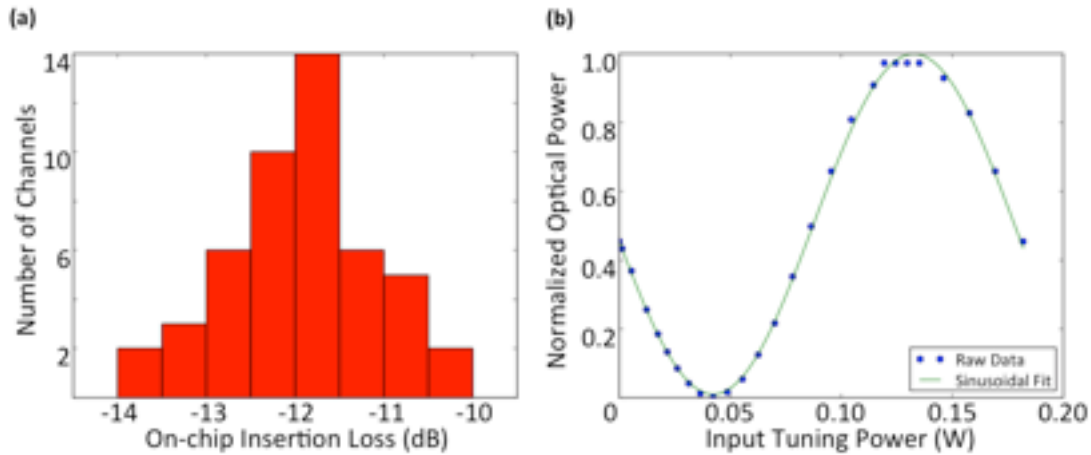


Figure 5.8: DC performance of the transmitter. (a) Average insertion loss across the 48 channels of the transmitter is  $-11.89 \text{ dB} \pm 0.83 \text{ dB}$ . (b) The thermal tuning efficiency of the phase tuners is  $90 \text{ mW}/\pi$

Thermal phase tuners using  $185 \Omega$  resistors next to the waveguides are integrated into both arms to bias the device. The average thermal tuning power to bias each arm of the device is 22.5 mW, shown in Figure 5.8(b). Linewidth nonuniformity induces random phase errors in these devices [SBP+10]. Due to a relatively short coherence length, the 0 V bias point for each channel is effectively random, and thus requires manual tuning to reach the desired bias point on each channel.

### *High-speed performance*

The measured termination resistance is found to be  $40 \Omega$ . A plot of a typical S11 is shown in Figure 5.9. RF reflections are kept near or below -10 dB up to 30 GHz and do not prevent the attainment of 50 Gb/s performance. Future iterations of this device will include termination resistors that are more accurately matched to the transmission line.

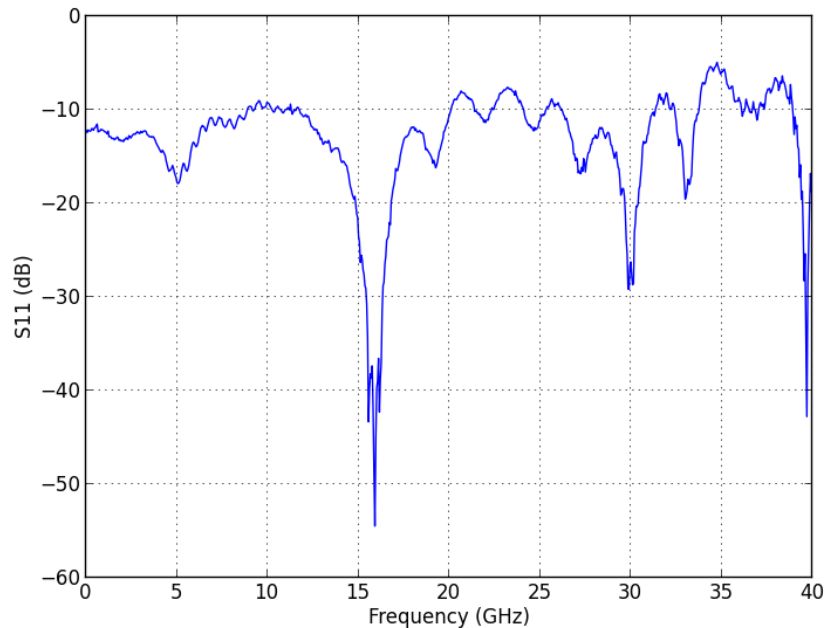


Figure 5.9: Measured S11 of the traveling wave modulator with on-chip termination resistor.

Each channel of the transmitter is tested for bit error rate vs. received optical power using an external photoreceiver and the results are shown in Figure 5.10(a). The traveling wave modulator transmission line characteristic impedance is  $33 \Omega$ , which is terminated by a  $40 \Omega$  resistor constructed from n++ implanted silicon (the termination resistor was targeted at  $33 \Omega$  but is subject to fabrication variation). Each channel of the transmitter is driven with a differential  $3.5 V_{pp}$  signal with  $1.5 V$  reverse bias. With the optical bias set to the quadrature point, a random sample of six modulators achieved  $7.0 \pm 0.96$  dB of extinction. The 20%-80% rise time across the same random sample is measured to be  $10.4 \pm 1.1$  ps, and the peak-to-peak jitter is measured to be  $8.17 \pm 1.65$  ps. Note that one channel of this set of modulators had only one neighbor, while the remaining modulators have neighboring channels on both sides. All testing is performed while modulating only a single channel.

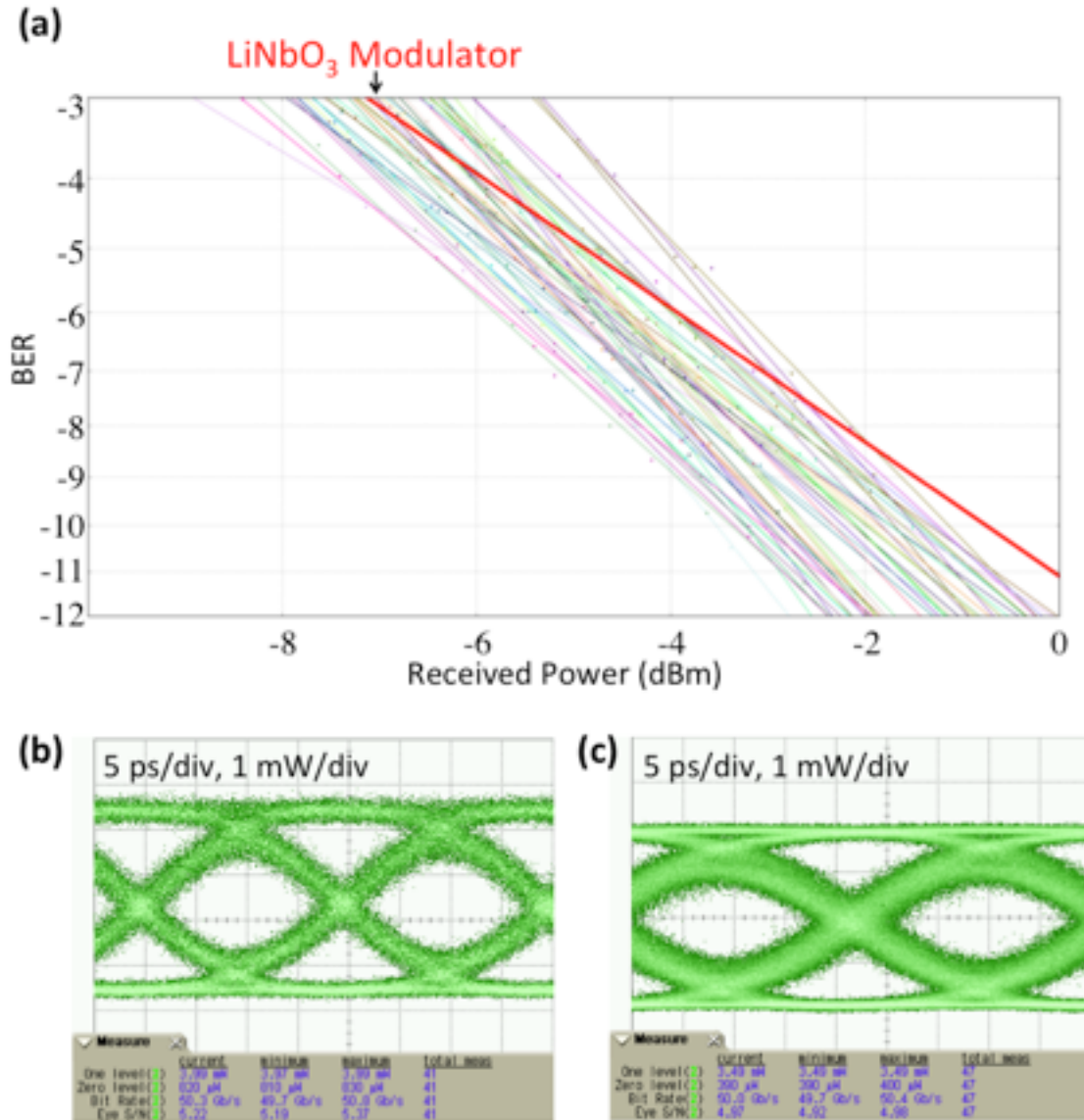


Figure 5.10: 50 Gb/s performance of the transmitter. (a) Bit error rate versus received optical power of all 48 channels of the silicon transmitter using a PRBS31 signal. A comparison trace using a commercial LiNbO<sub>3</sub> modulator in place of the transmitter is shown in red. (b) Optical eye diagrams of a typical silicon modulator channel at 50 Gb/s, (c) as well as the LiNbO<sub>3</sub> modulator at 50 Gb/s for comparison (c).

Across all 48 channels of the modulator array, the sensitivity at a BER of  $10^{-9}$  is  $-2.87 \pm 0.63$  dBm with a slope of  $-0.32 \pm 0.05$  dB<sup>1/2</sup>/dBm<sup>-1</sup>. The random sample of six modulators mentioned previously exhibited a sensitivity of  $-3.0 \pm 0.76$  dBm. A commercial lithium niobate modulator driven to high extinction with a 5.0 V<sub>pp</sub> signal is

also tested in the same link. It is found to result in a sensitivity of -1.48 dBm at the same BER. A typical eye diagram for one channel of the transmitter is shown in Figure 5.10(b), and an eye diagram of the LiNbO<sub>3</sub> modulator is shown in Figure 5.10(c). The statistics of bit-error-rate versus received optical power of the transmitter is shown in Figure 5.11(a, b). As can be seen from the histogram, the sensitivity of every channel falls within a 3 dB window and the slopes of the BER curves are relatively uniform.

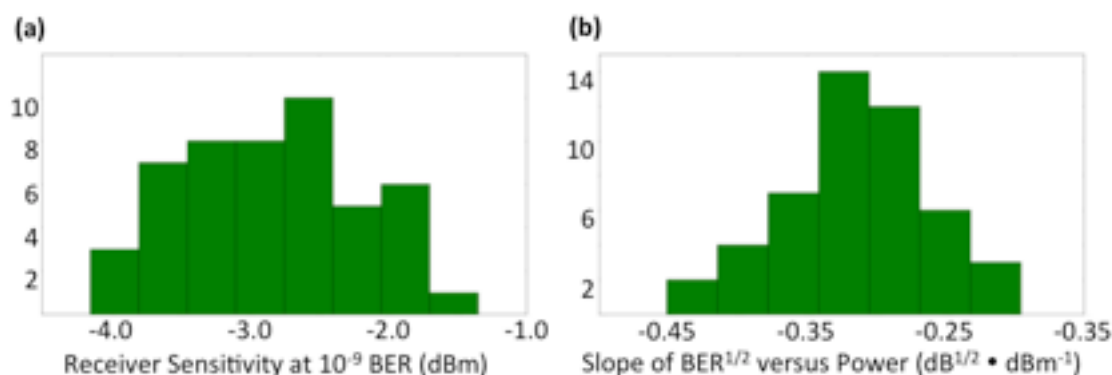


Figure 5.11: Statistics of the BER versus received optical power of the silicon transmitter. Receiver sensitivities at a BER of 10<sup>-9</sup> (a) show high uniformity across all channels, as do the slopes (b) of the BER<sup>1/2</sup> vs. power traces

The receiver is not packaged, and is thus only tested at the die level for open 50 Gb/s eye diagrams. Typical eye diagrams at 43 Gb/s and 50 Gb/s are shown in Figure 5.12(a, b). From the eye diagram at 50 Gb/s of one of the photodetector channels, the 20%-80% rise time is  $9.8 \pm 0.3$  ps and the peak-to-peak jitter is  $10.5 \pm 0.6$  ps. Given the RF performance and dark current and considering shot and thermal noise, if we assume this PD is input to an ideal TIA with 5 dB noise figure and 30 GHz bandwidth, the receiver sensitivity is theoretically predicted to be -9.5 dBm.

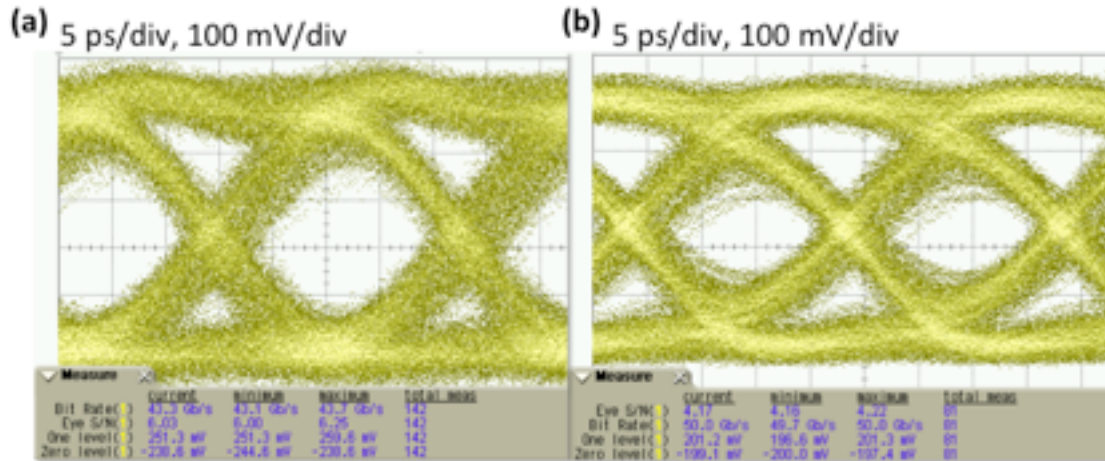


Figure 5.12: Typical receiver eye diagrams at 43 Gb/s (a) and 50 Gb/s (b).

It is possible to estimate the minimum required power for a certain bit error ratio, given assumptions about the noise sources. For a photodetector input into a TIA, it is usually only necessary to consider shot noise, thermal noise, and the TIA noise figure. Assuming these noise sources are uncorrelated Gaussian processes, it is possible to calculate the required power to ensure that less than  $10^{-9}$  bits are received in error, as illustrated in the figure below.

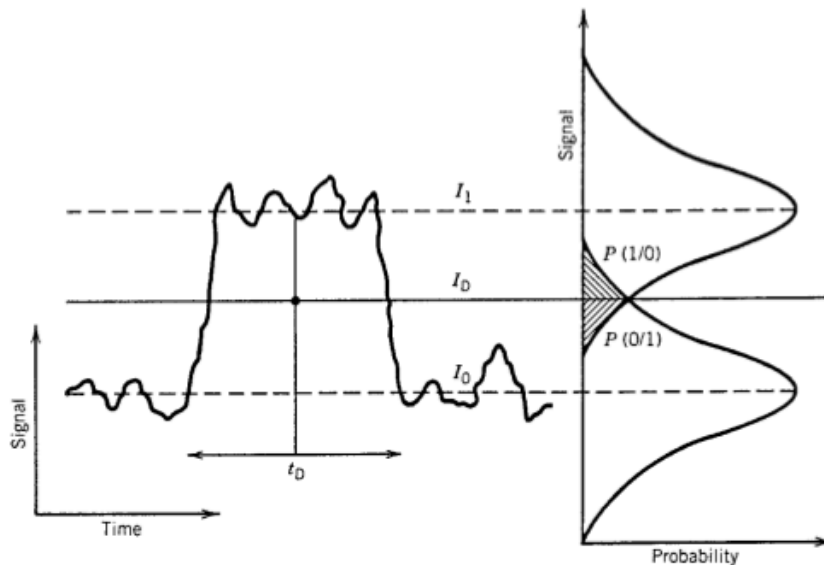


Figure 5.13: Illustration of noise in a on-off keyed signal. Given Gaussian probabilities of "1" and "0" bits, it is straightforward to estimate the likelihood that an error will occur. Figure from *Fibre-Optic Communication Systems*, 3<sup>rd</sup> edition, Chapter 4.

The Q factor of an on-off keyed signal and the associated bit error rate is defined as:

$$Q = \frac{I_1 - I_0}{\sigma_1 + \sigma_0} BER = \frac{1}{2} \operatorname{erfc} \left( \frac{Q}{\sqrt{2}} \right) \quad (1)$$

where  $I$  and  $\sigma$  are the current and noise of the subscripted bits and  $\operatorname{erfc}$  is the complementary error function. Shot noise and thermal noise can also be calculated as:

$$\begin{aligned} \sigma_{th}^2 &= \left( \frac{4k_b T T}{R_L} \right) F_n \Delta f \\ \sigma_s^2 &= 2qI\Delta f \end{aligned} \quad (2)$$

where  $k_b$  is Boltzmann's constant,  $T$  is temperature,  $R_L$  is the load impedance,  $F_n$  is the noise factor of the amplifier,  $q$  is the elementary charge of an electron,  $I$  is the photocurrent output, and  $\Delta f$  is the electrical bandwidth of the receiver.

Previous measurements have shown the photodetectors to have responsivities of  $0.74 \pm 0.13$  A/W [NLD+13]. Assuming the same responsivity distribution on this wafer, receiver sensitivity would then vary from -8.6 dBm to -10.13 dBm for the 5 dB amplifier noise figure case. The receiver sensitivity of the chip will also ultimately be affected to a large degree by the insertion loss from fiber to chip, the packaging scheme, and the design of the amplifier receiver chain. Grating couplers are used here due to their ease of testability. However, future iterations may make use of edge couplers, which have been shown to have coupling losses as low as 2 dB in this platform.

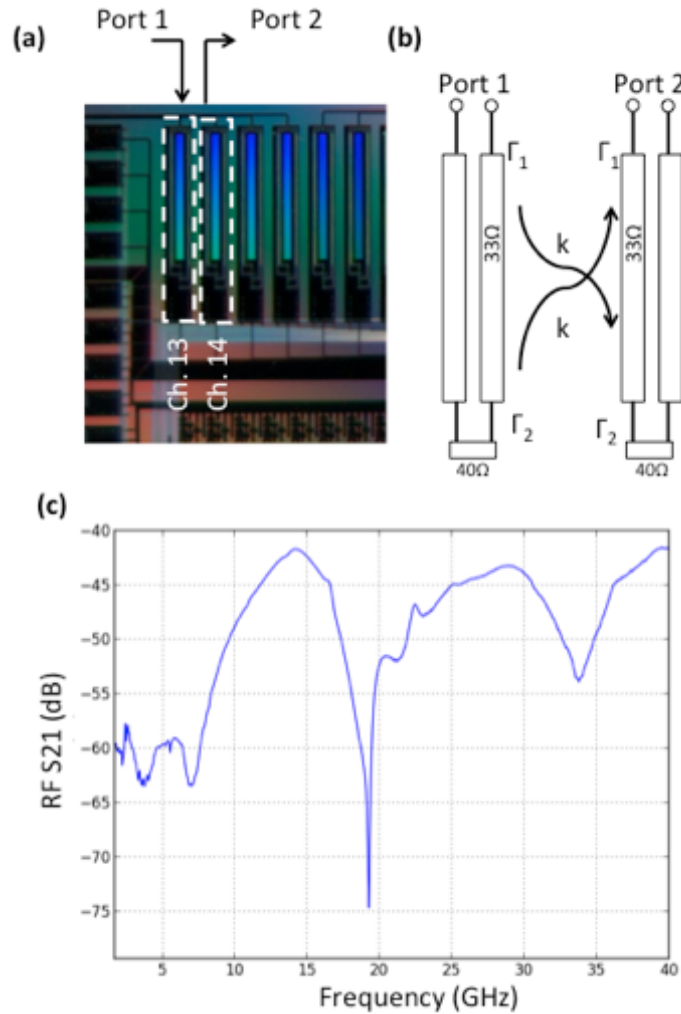


Figure 5.14: Electrical S21 of driving transmission line contact pads of adjacent arms of two neighboring modulators.

Cross talk between modulators is potentially a serious issue in tightly packed photonic systems. Thermal cross talk from the neighboring channel was found to be approximately 1.8 rad/W for the pn modulator termination resistor and 0.36 rad/W for the thermal tuners. While BER degradation due to RF crosstalk is also an important parameter to characterize, it is infeasible to directly measure due to geometrical limitations with our current test setup. It is physically impossible to optically probe the device as well as apply two bulky RF probes and the two DC probes to adjacent channels. Instead, we present the electrical S21 between the input RF contact pads of neighboring devices, with the general configuration outlined in Figure 5.14(a, b). By knowing that the impedance of the RF probes is  $50\Omega$ , that the transmission line impedance is  $33\Omega$ , and

that the termination resistor is  $40 \Omega$ , it is possible to estimate the coupling,  $k$ , between adjacent arms. From Figure 5.14(c), the largest value for the  $S_{21}$  between adjacent modulator input pads is  $-41.5 \text{ dB}$ . An upper bound can be calculated by making the conservative assumption that the entire coupling between adjacent modulators is due to the forward propagating wave, and that the measured  $S_{21}$  is due to the reflection of this forward coupled wave. Thus, the coupling,  $k$ , may be solved:

$$S_{21} = 2\Gamma_2(k - k^2)(1 - |\Gamma_1|)^2 \quad (3)$$

where  $\Gamma_1$  is the reflection coefficient between the probe and the modulator transmission line, and  $\Gamma_2$  is the reflection coefficient due to the on-chip termination. While a likely overestimate of the coupling, this suggests that the coupling between adjacent devices is at most  $-23 \text{ dB}$  at  $14.2 \text{ GHz}$ , and is lower than this at other frequencies. Observing the rule of thumb presented by [SN06], there is expected to be less than  $0.74 \text{ ps}$  of crosstalk-induced jitter in this modulator array.

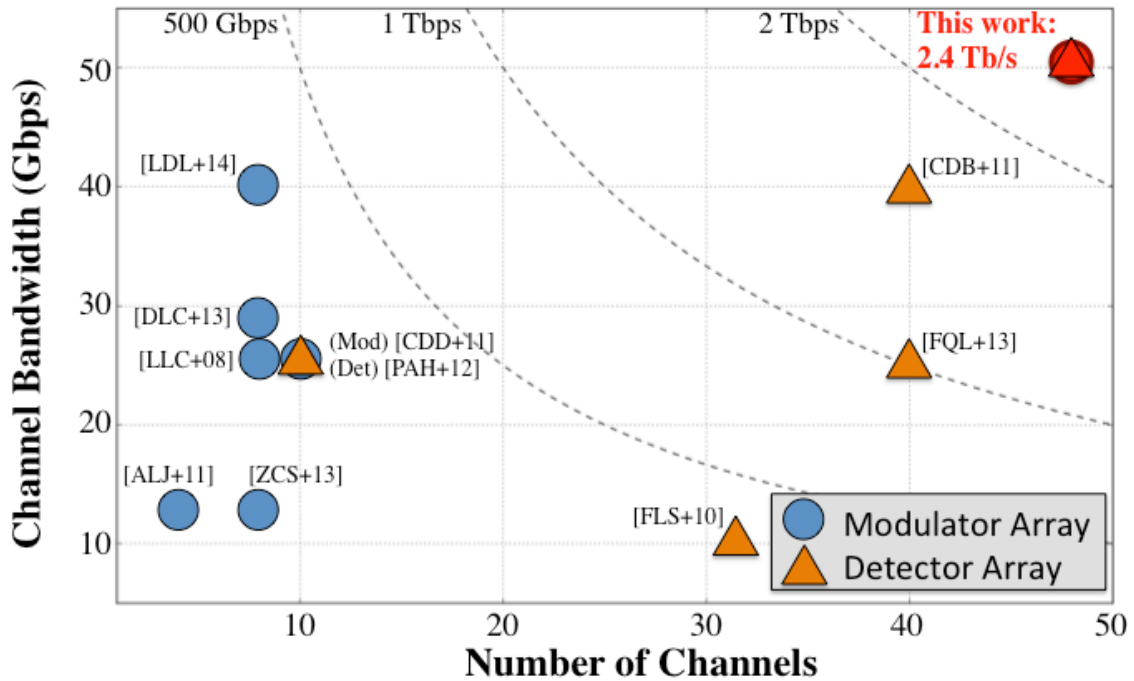


Figure 5.15: Comparison of high-bandwidth silicon systems.

### *Energy efficiency*

The power consumption of this device can be estimated by assuming an ideal NRZ input signal and measuring the average thermal tuning power. The total energy efficiency of each channel of this transmitter may then be described by the equation:

$$\text{Energy/bit} = \frac{N_{\text{input}}}{B} \left( \frac{(V_{\text{pp}}/2)^2}{40 \Omega} + \frac{V_{\text{bias}}^2}{40 \Omega} \right) + \frac{P_{\text{tuning,avg}}}{B} \quad (4)$$

where  $N_{\text{input}}$  is the number of electrical inputs (two due to differential drive),  $B$  is the data rate in bits per second, and  $P_{\text{tuning,avg}}$  is the average power consumption to bias the Mach-Zehnder interferometer. The coherence length of the waveguides is found to be shorter than the Mach-Zehnder arm length. Since there is a thermal phase tuner in both arms of the Mach Zehnder the necessary thermal bias power of each channel is randomly distributed between 0 and  $P_{\pi}/2$ . Operating at 50 Gb/s using a 3.5 V<sub>pp</sub> signal with 1.5 V reverse bias, the energy efficiency of the transmitter is 5.1 pJ/bit where 2.4 pJ is due to the driving signal, 2.2 pJ is due to heating in the transmission line termination resistor due to the bias voltage, and 0.45 pJ is due to thermal tuning.

For improved power consumption, this device could be operated at 0 V bias with a 2.0 V<sub>pp</sub> drive signal (though with reduced sensitivity performance) [RLL+14]. The efficiency of the thermal tuners could also be improved by lightly doping the core of the waveguide to act as a resistor [SDY+13, HMM+14], or by performing isolation etches around the thermal tuners [DQL+10]. Ultimately though, the system power consumption will be largely dominated by the modulator driver amplifiers and high power lasers.

## **5.5. Conclusions**

In conclusion, we have demonstrated a single-chip parallel single mode transmitter and receiver fabricated in a fully-integrated SOI platform with 2.4 terabit/s aggregate data

rate. The transceiver makes use of the OpSIS PDK device library and fabrication process steps. The transmitter is based on the Mach-Zehnder modulator and consists of 48 channels, each operating at 50 Gb/s. The receiver utilizes a gain-peaked Ge p-i-n photodetector. While in our experiments we use an EDFA, the bandpass filter before the receiver removes the majority of the amplifier noise. Thus, the link may be effectively compared against other unamplified links one might find within data center networking or high-performance computing.

In future work to package these chips, it will be important to carefully manage the electrical crosstalk between neighboring channels. Flip chip bonding would provide the lowest parasitic effects [ZCS+13]. Due to the large size of the chip, accommodating wire bonds to a PCB is also possible, though this introduces signal integrity challenges. Differential signaling through the wirebonds will help to reduce crosstalk compared to the wirebonding for a single-drive modulator. On the receiver, it would be ideal to directly wirebond from the photodetectors to a TIA. A typical high-speed TIA die may be on the order of 1.2 mm to a side, and thus for 48 channels would require at least 57.6 mm of total chip edge length, assuming only single-channel TIA dies are used. By using multi-channel TIA chips, and given the large size of the receiver chip, it should be possible to accommodate such an array of amplifiers.

While we demonstrate a parallel single mode fiber link, one could use devices already demonstrated in this platform to construct other architectures, such as polarization- or wavelength-division multiplexing based transceivers. The high-uniformity across all channels demonstrates that it is possible to scale large highly parallel silicon transmitters to many terabit/s and beyond.

## Chapter 6. Conclusion

### 6.1. Results Summary

The primary focus of this research is the contribution to a library of silicon photonic devices and the use of this library to build large-scale complex integrated optical systems. Both individual passive and active optical devices were designed, fabricated, tested, and integrated into the OpSIS process development kit. Using components of this PDK library, a single-chip terabit optical link was demonstrated.

Chapter 2 describes the design and test of the first experimental demonstration of a polarization-splitting bi-wavelength grating coupler. The design builds upon previous work on symmetrical 2-dimensional gratings for polarization splitting with a novel dual wavelength transmission band coupling scheme. In this device, both polarizations of O-band and C-band light can be coupled into on-chip waveguides. There are two output waveguides, and in each waveguide the 1310 nm light is coupled into the  $TM_0$  mode and the 1550 nm light is coupled into the  $TE_0$  mode. This effect was achieved by solving for a grating period and fiber angle at the Bragg condition with these two modes. The device insertion loss at 1576 nm is 7.6 dB and at 1296 nm is 8.2 dB. The -1.5-dB transmission bandwidth of the device is 35 nm for C-band light and is 18 nm for O-band light. Polarization isolation measurements were also performed and showed 8.4 dB isolation for 1310 nm light and 24 dB for 1550 nm light.

Chapter 3 introduces a high-speed silicon carrier-depletion Mach-Zehnder modulator. This device was based on a first-generation modulator with 18 GHz bandwidth and demonstrated 25 Gb/s data transmission. The bandwidth of the first generation device was limited by RF losses. It is shown that reducing series resistance by introducing two intermediate implantation layers can dramatically increase the device bandwidth without sacrificing insertion loss or  $V_\pi L$ . The series resistance was decreased from approximately 1.62  $\Omega$ -cm to a series resistance of 0.65  $\Omega$ -cm. Bandwidth scales approximately as  $1/\sqrt{R_{pn}}$ , which is close to the measured improvement: 18 GHz to 30

GHz. The device is shown to transmit 50 Gb/s under 3 different driving voltages. With 1.5 V<sub>pp</sub> and 0 V bias, the device effectively requires 450 fJ/bit of RF power and achieves 3.4 dB extinction with “1” bit loss of 1.4 dB.

Chapter 4 presents further measurements of a silicon traveling wave modulator for analog optical applications. The spur-free dynamic range is a measurement of the linearity of an optical link. Silicon modulators based on the carrier-depletion effect have an inherent nonlinearity due to the variation in depletion width of a reverse-biased PN junction. Using a single-ended driving condition, an SFDR<sub>SHD</sub> and SFDR<sub>IMD</sub> of 72 dB·Hz and 92 dB·Hz are measured, respectively. By differentially driving the same modulator an SFDR<sub>SHD</sub> and SFDR<sub>IMD</sub> of 82 dB·Hz and 97 dB·Hz are measured, respectively. The SFDR of this link is within 5 dB of the value predicted by considerations of only the Mach-Zehnder transfer function and carrier depletion phase non linearity. This suggests that the dominant nonlinearity of the link is due to the PN junction.

Finally, Chapter 5 discusses a single chip parallel single mode optical link consisting of 48 channels, each operating at 50 Gb/s. The system uses devices from the OpSIS process development kit, including a slightly modified version of the modulator described in Chapter 3. The principle question is whether such a large active optical system can reliably yield. The transmitter consists of an array of 12 input grating coupler and 48 output grating couplers. The light from each input grating coupler is split into 4 channels and input into separate traveling wave Mach-Zehnder modulators. All 48 channels of the link were tested for DC performance as well as high-speed 50 Gb/s eye patterns and bit-error-rate versus received optical power. Cross-chip uniformity of 3 dB is measured for both insertion loss and link sensitivity. A commercial 35 GHz lithium niobate modulator is measured in the same system, replacing the silicon modulator, to show that there is no link penalty when using the silicon transmitter. In aggregate, the transceiver can send and receive up to 2.4 Terabits/s.

## 6.2. Research Outlook

As more and more systems demonstrations appear, silicon photonics will likely continue to gather immense interest from the research and industrial communities. It is undisputed that optical data transport systems are required to move vast amounts of data over large distances. It is also undisputed that the distance over which it makes sense to use optics has been shrinking over time. As interconnect bottlenecks and economic motivations push the needs of optical I/O, the ability to move silicon photonics into high-volumes by virtue of an already existing CMOS manufacturing infrastructure will prove immensely valuable. Still, there are many avenues of research that can help enable these solutions faster, and that build upon the work presented here.

Fundamentally, all of the individual silicon devices demonstrated in literature have room for improvement—whether it is from more complex and optimized geometries or due to increasing process complexity. The grating and edge couplers to move light from on-chip to a fiber have seen steady improvement over the last decade in both their raw insertion losses, as well as functionality. The bi-wavelength polarization splitting grating coupler presented here could be improved with a polysilicon overlay or finer features enabled by a more advanced lithography process such as 193 nm immersion. Even greater process changes such as backside metal mirrors could push the performance even lower.

Similar performance increases are also likely possible for electrooptic devices such as the traveling wave Mach-Zehnder modulator presented in this work. More work into advanced junction designs could dramatically improve phase shifter performance. Additionally, novel RF driving schemes are enabled by the tight integration and CMOS-like processing of silicon photonics. Even work in transmission line design could allow for lower impedance modulators, thereby enhancing bandwidth. Furthermore, complex linearization schemes are likely much more feasible in silicon photonics than other material systems. The tight device integration and manufacturing yield control could enable novel electro-optic planar radio-frequency circuits. In addition, integrating other devices in the optical domain could extend bandwidth. Devices such as a ring-assisted Mach Zehnder modulator have already shown that low-hanging fruit is available.

Most importantly, by integrating hundreds to thousands of optical functions on a chip, novel systems and system architectures can be explored. Many optical networks were designed around an assumption set about available technology. Building optical systems in silicon permits the photonic integrated circuit to absorb system complexity. There has been very little literature showing novel architectures in silicon. Much of this work will also be boosted by a developing packaging infrastructure. With the rise in accessibility and complexity of multi-project wafer runs, more researchers will have access to these opportunities.

Whether they develop complex system or not, most research groups now have the means to at least bring a silicon photonic product to market. Even in very small volumes, the chip costs of silicon photonic devices rapidly shrink to the point where they will be in the few-dollar range. Other costs, such as packaging and lasers, will often dominate the overall price of silicon photonic solutions. There are already relatively complex products available from Kotura and Luxtera, and it is easy to see that even relatively complex photonic circuits will cost hundreds of dollars or less, including packaging costs, without having to go to extremely high volumes. We will see, in the next few years, an explosion both in the number of silicon photonic products coming to market, and a significant increase in the number of complex silicon photonic systems being developed in academia. Furthermore, novel applications will continue to emerge, creating fundamentally new commercial and research opportunities over the coming years.

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## VITA

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### Peer-Reviewed Publications

1. **M. Streshinsky**, A. Novack, R. Ding, Y. Liu, A. E.-J. Lim, P. G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "Silicon nanophotonic parallel single mode 48×50 Gb/s transmitter and receiver," *IEEE J. Lightw. Technol.*, vol. 32, no. 22, pp. 3768-3775, 2014.
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