A Multi-Time over Threshold Data Acquisition System for Silicon Photomultipliers based Positron Emission Tomography Imaging

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Abstract

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Recent developments in the area of Positron Emission Tomography (PET) detectors using Silicon Photomultipliers (SiPMs) have demonstrated the feasibility of higher resolution PET scanners due to a significant reduction in the detector form factor. However, reduced size implies a corresponding increase in the detector density, resulting in a proportional rise in the number of channels interfacing a SiPM array with the digital backend. In addition, the fast timing response of the SiPMs requires very high-resolution data acquisition systems with sampling speeds of multiple Gigasamples/sec, resulting in considerably high power and area budget.

The main focus of this work is to explore analog and mixed signal circuit design techniques to enable power and area optimized data acquisition system design. As part of this work, three different readout systems were implemented in CMOS silicon. The first readout chip was fabricated in STMicroelectronics 130 nm CMOS process. The main focus of the ASIC was to reduce the number of channels in the backend using row column channel combining scheme and employ threshold detection technique to reduce dark noise contribution across the readout channels. The second generation of the readout chip was fabricated in TSMC 65nm Low Power process with a modified front-end interface design. The third generation of the ASIC, the main focus of this thesis, presents a chip level implementation of a Time-over-Threshold based data acquisition system for PET Imaging systems, which will help to replace the high-speed digitizers with a power and area optimized design. This was fabricated in TSMC 65nm Low Power process flavor. With multiple thresholds, this chip enables multiple time stamps on the fast rising edges, thereby resulting in an improved timing resolution for the system. These time stamps can be used to develop better algorithms for image reconstruction, using various statistical estimation techniques and machine learning algorithms. Also, multiple ToT helps in improving the tradeoff between timing and energy resolution. This thesis addresses different challenges associated with implementing a high resolution ToT system. This new implementation will allow more compact scanner/detector

designs without having to sacrifice any of the data fidelity, reduce cost, and increase reliability.

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explore new hobbies, rekindled my love for reading books and made me fall in love with theaters and musicals.

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To,

Ma and Baba

And

To,

Didibhai and Subhro

Chapter 1. INTRODUCTION

Physics have revolutionized the human life over a long period of time. One of its most rewarding applications has been that of Medical Physics in the form of various Imaging Technologies. It started with the discovery of X-rays in 1895 by Wilhelm Rontgen, a German professor of physics. The radiation from the X-rays is absorbed differently depending on the type of tissues in the body, particularly its density and composition. This property is used to map the different densities within the body on a photographic film. Then came the use of pharmaceutical contrast agents between 1906 and 1912. Administered orally or using vascular injection, they were the first one to help visualize blood vessels, digestive and gastro-intestinal systems, bile ducts and gall bladder. They paved the way for angiography by the 1960's. In angiography, a radio-opaque contrast agent injected into the blood vessel is used to visualize the flow of blood vessels and organs in the body, with specific interest in arteries, veins and the chambers of the heart.

The advent of Nuclear Physics in medical imaging was made possible in the early 1950s when Geiger Muller counters were used to measure counting rates from iodine-131 in the thyroid gland from point-to-point over the neck. As years went by, nuclear physicists made considerable improvements with inventions like the gamma camera [1] and the emission tomography system. The early part of 1950's also saw the rise of Positron Emission Tomography (PET), thanks to the work of Gordon Brownell, Charles Burnham and their associates at the Massachusetts General Hospital [2]. Later, pioneering work by Michel Ter-Pogossian at the Washington University of St. Louis led to great advancements in the field of PET [3]. In the 1960's, the principals of sonar in the form of ultrasound were applied to the field of diagnostic imaging. Since then, it has become a very popular imaging technique due to the lack of any adverse bio-effects. Computed

Tomography (CT) scan introduced in the 1970's uses computer processed X-rays to produce tomographic slices of specific areas of the body, giving better insight into the pathogenesis of the body. The motivation behind Magnetic Resonance Imaging (MRI) was the discovery of the fact that the magnetic relaxation times of tissues and tumors differ, and this was shown by Raymond Damadian in 1971. The next 20 years saw vast improvements in the field of MRI due to the contributions of different scientists. Radio waves stronger than the magnetic field of the earth are used to form a strong magnetic field around the area to be imaged. This causes the alignment of protons (hydrogen atoms) in tissues containing water molecules. The excited protons emit a radio frequency signal which is picked up by a scanner and transformed into an image on the computer.

PET is based on a radioactive tracer imaging technique. A radioactive tracer compound is a chemical compound in which one or more atoms have been replaced by radioisotope, in this case by positron-emitting radionuclides. When injected into the human body, these tracer compounds can then be used to track the mechanism of various biochemical and physiological processes in vivo by virtue of their radioactive decay. The system detects the pair of gamma rays emitted as a result of this decay, and 3D images of tracer concentration within the body is then created by image reconstruction algorithms. Existence of positron-emitting isotopes of elements such as carbon, nitrogen, oxygen and fluorine makes PET detection an important tool in medical research and practice, because these compounds can be processed to create tracer compounds similar to naturally occurring substances in the body. Some of the most common radiotracer compounds used clinically are carbon-11 (^{11}C), nitrogen-13 (^{13}N), oxygen-15(^{15}O) and fluorine-18 (^{18}F). They have been used to identify and diagnose cancers, epilepsy and other movement disorders, and heart and cardiovascular problems.

A PET scanner consists of three main systems: the photodetectors, the data acquisition (DAQ) and pulse processing electronics, followed by the image reconstruction systems in the back-end. This thesis will concentrate on the data acquisition portion of the scanner, specifically the front-end readout electronics. The scope of the DAQ system depends on the application, but in general, it starts from front-end electronics which receive the signals from the detector modules and ends with the data transmission network circuits which are used to send the processed data from the photon events, to the image reconstruction PC. The front-end electronics need to properly acquire the signals from all the channels, where the number of channels can be of the order of few hundreds or thousands. Without multiplexing, the number of channels interfaced to the back-end Analog-to-Digital Converters (ADCs) would increase, and the power dissipation would scale accordingly. There are examples of existing multiplexing schemes in the optical [4][5] and electrical domains [6][7]. Most of the works in the electrical domain are based on discrete board level implementations, even though the emerging solid-state photodetector technologies are based on CMOS technologies. Therefore, the research paradigm for DAQ systems has shifted towards CMOS implementations because there is a potential for the integration of the data acquisition and pulse processing electronics on the same substrate as the detector modules [8][9]. The disadvantage with multiplexing circuit is the introduction of more noise in the signal path compared to a channel with one-to-one coupling with the detector. If this added noise is similar or larger than the noise in the original crystal scintillation signal, the energy resolution will be degraded. The input circuits of a DAQ system needs to have enough SNR both for energy resolution and multiplexing. Another way to tackle the issue of large number of channels is to reduce the amount of electronics needed in a single channel. This will help to reduce the power consumption as well. The waveform digitizers contribute a significant proportion of the power

budget in the DAQ system. The main reason for this is the higher sampling rates required in this application. The rise time of the SiPM pulses are of the order of few nano seconds. For example, time of flight PET applications use fast detectors, such as LSO or LYSO coupled to fast PMTs, which produce pulses with a rise time of about 2.2ns. For this case, a sampling rate of 1.3GSps is required to achieve time resolutions of 200-300 ps FWHM [10]. This sampling rate corresponds to about four samples on the rising edge. Even in non-time-of-flight PET applications, a sampling rate of at least 100MSps is required to achieve at least 1.7 ns FWHM time resolution. For covering the entire dynamic range of the SiPM pulses, around 8-10 bits are required for the converters. These specifications are not trivial for the realization of traditional converter architectures. According to the survey on converters given in [11], a state-of-the art ADC with the above specifications has a power consumption ranging from few mW to tens of mW. This thesis explores an alternate way of waveform digitization used for systems with SiPMs or single photon avalanche diodes (SPAD). This technique is known as Time-over-Threshold (ToT). ToT compares the pulse with a predetermined threshold and outputs the time the pulse spent over the threshold. This method takes advantage of the fact that the shape of the SiPM pulses is uniform, the major difference being the pulse height. As shown in Figure 1.1 ,compared to a traditional converter, ToT needs very few samples to encode the energy information. The channel architecture is simplified with the use of just a comparator and a time-to-digital converter (TDC) for digitization. This results in reduced power consumption as well. In a PET system, the time stamps on the rising edge are used to extrapolate to the first electron timing point. In a ToT implementation, the time stamps corresponding to the thresholds on the rising edge can be used to calculate the first electron timing point, thus preserving the timing resolution of the system.

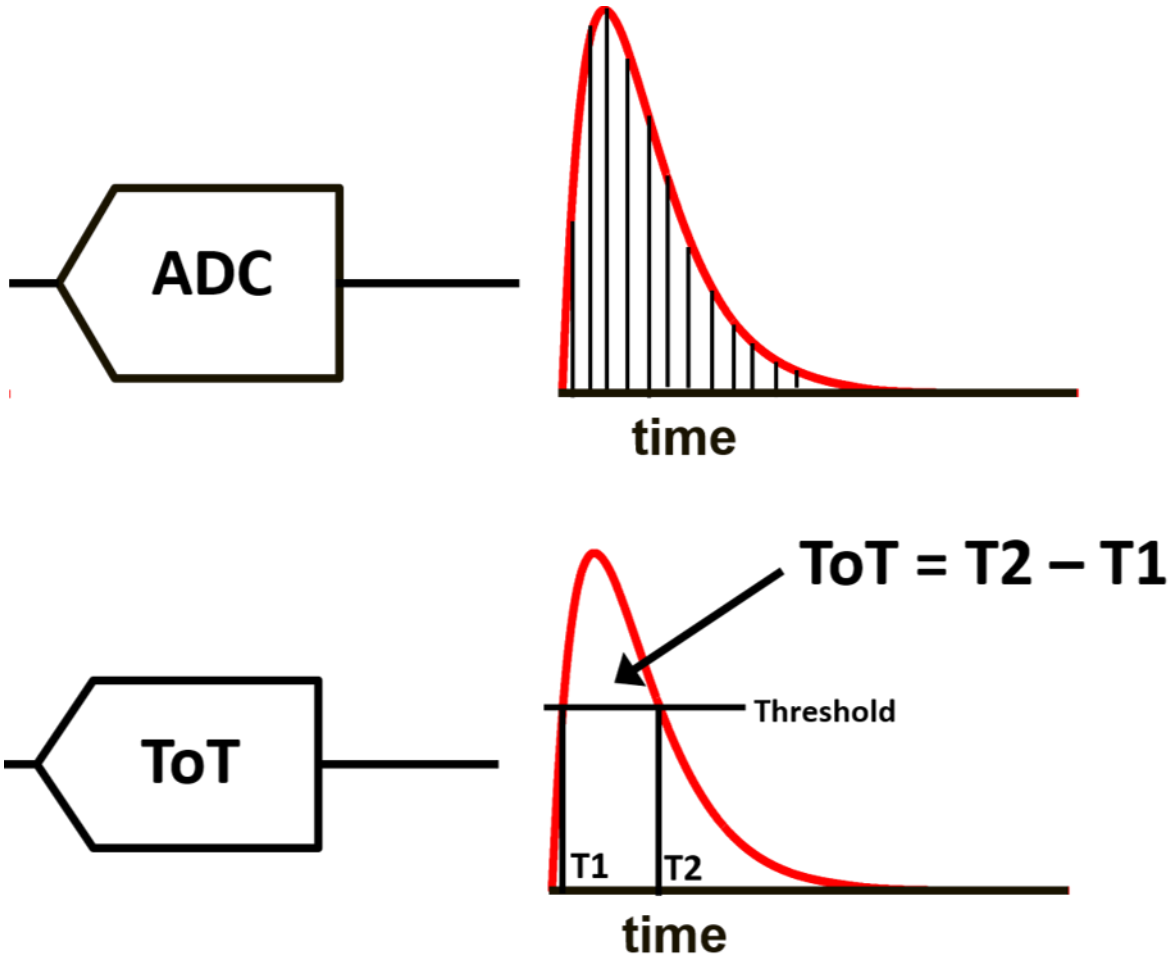

Figure 1.1. Conceptual comparison of an ADC vs ToT for a PET channel.

This thesis is organized as follows -

Chapter 2 : Positron Emission Tomography introduces the main building blocks of PET imaging systems including the tracer chemistry, the scanner hardware including the detector modules and the DAQ, the back end image reconstruction algorithms and the uses of PET.

Chapter 3 **:** System Design covers the impact of analog non-idealities associated with front-end electronics on PET imaging systems and the motivation behind the architecture used in this implementation.

Chapter 4 **:** Time-over-threshold explains the ToT technique and compares the single and multi-threshold based ToT implementations.

Chapter 5**:** Front-end Interface discusses the circuit level implementations of the front-end amplifier in the different versions of the ASIC.

Chapter 6**:** Comparator describes a novel input driven self-clocked comparator architecture implemented in this work.

Chapter 7**:** Time-to-Digital converter (TDC) explains the TDC architecture implemented in this work.

Chapter 8 **:** Measurements presents the test results of the chip in various test setups.

Chapter 9 : Conclusions and Future Work **s**ummarizes the contributions of the thesis and some possible future works.

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Chapter 2. POSITRON EMISSION TOMOGRAPHY

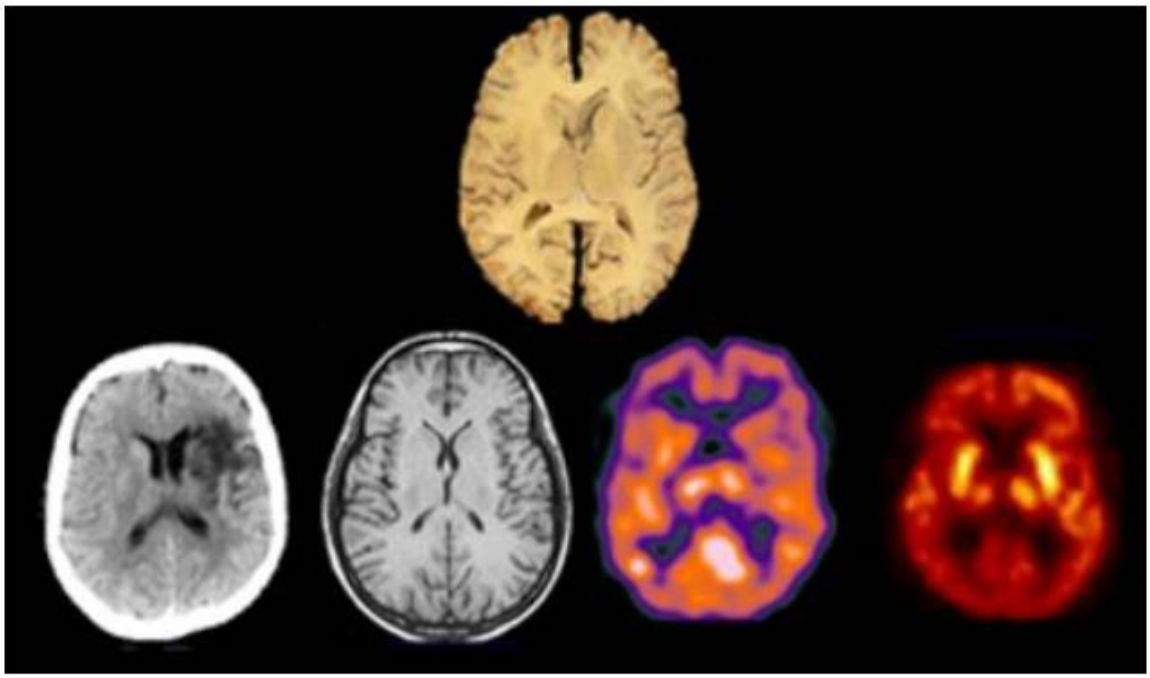

Figure 2.1. Transaxial slice of the human brain (top) acquired with different imaging modalities (bottom) from left to right: X-ray CT, MRI, SPECT and PET [12].

Medical imaging techniques can be broadly classified into two different categories – structural and bio-chemical. Ultrasound, X-rays, CT (Computed Tomography) and MRI (Magnetic Resonance Imaging) belong to the first kind, as they produce image of the body anatomy. Biochemical imaging modalities, on the other hand, map the different chemical processes inside the body, like blood flow and metabolism. Positron emission tomography (PET) and single-photon emission computed tomography (SPECT) are well-established examples of biochemical imaging modalities, which provide physicians with information about the body's chemistry not available through any other procedure. Figure 2.1 shows a transaxial slice through the human brain (top row) acquired with X-Ray CT, MRI, SPECT and PET (bottom row) giving different information about the brain function and anatomy.

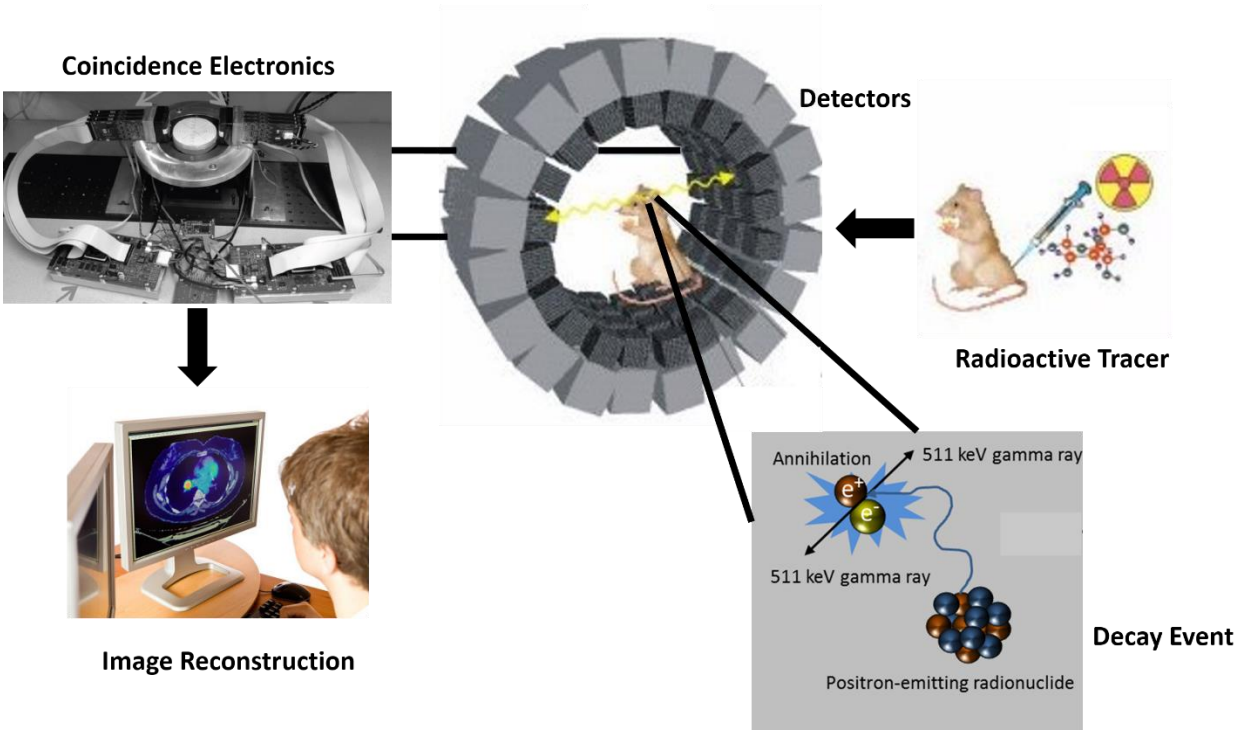

Figure 2. 2. PET Scanner Ring and the associated electronics [13].

The main components of the PET imaging system are shown in Figure 2. 2. The first step is to generate and administer the radioactive tracer, composed of a radioactive isotope and a metabolically active molecule. These tracers are injected into the body of the patient to be scanned. After enough time has elapsed for the tracer to distribute and concentrate in certain tissues, the subject is placed inside the scanner. The radioactive decay events for tracers used in PET studies give off two 511KeV antiparallel photons. The scanner hardware is designed to efficiently and accurately capture these photons. The scanner, the second component of PET, consists of a ring of sensors attached to electronics. The sensors are made up of scintillator crystals attached to a photodetector. The scintillator converts the 511KeV photon into many visible light photons, while the photodetector generates an electrical pulse in response to the burst of visible light. These pulses are processed by the front-end digital acquisition electronics to determine the parameters of each

pulse (i.e. energy, timing). Finally, the data is sent to a host computer that performs the tomography to turn the data into a 3-D image.

2.1 RADIOPHARMACEUTICAL

Before the start of the actual PET scan, the first step is to synthesize the radiopharmaceutical (or tracer). This is done by removing one or more atoms of a metabolically active molecule by the radioisotope. To conduct the scan, the tracer is injected into the body of the subject. There is a waiting period before it becomes concentrated in the tissue of interest and the scanning can actually begin. The metabolically active molecule speeds up this process by acting as a carrier for the radioactive isotope. Most of the radioisotopes have a short half-life, thereby ensuring large portion of the decays will occur during the scanning period. This helps to gather maximum information for a given dose of radiation. However, due to the short half-lives of most radioisotopes, the radiotracer has to be produced in close proximity to the PET imaging facility. At present, the most commonly used radiotracer in clinical PET scanning is fluorodeoxyglucose (also called FDG or fludeoxyglucose), an analogue of glucose that is labeled with fluorine-18. This makes up a large majority of radiotracer (>95%) used in PET and PET/CT scanning, with extensive uses in oncology as well as neurology.

2.2 DECAY EVENT

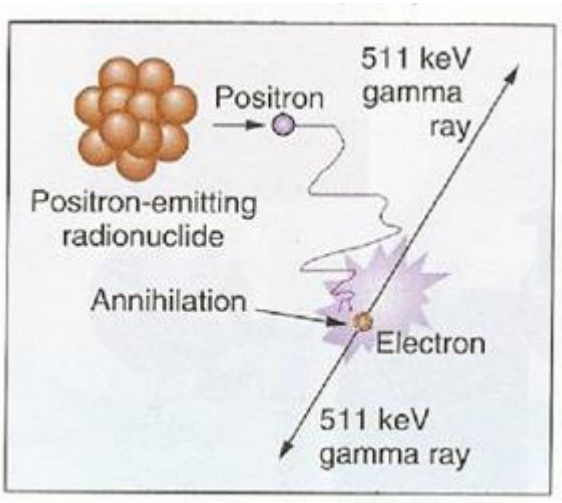

Figure 2. 3. Basic Physics of Positron Emission Tomography[14].

After being absorbed by the tissue of interest, the radioisotope inside the tracer undergoes positron emission decay. A positron is an antiparticle of the electron with opposite charge. As shown in the figure, the emitted positron travels in tissue for a short distance (typically less than 1 mm, depending on the isotope), and then interacts with an electron. The encounter leads to the annihilation of both the positron and the electron, producing a pair of 511 KeV gamma photons, which travel away at an angle of 180° with one another. This makes it possible to localize their source along a straight line of coincidence (also called the line of response, or LOR). In this way, positional information is gained from the detected radiation without the need for a physical collimator. This is known as electronic collimation. The coincidence events are the events detected from these simultaneously emitted photons. In practice, the LOR has a finite width as the emitted photons are not exactly 180 degrees apart.

2.3 PHOTON SCINTILLATION

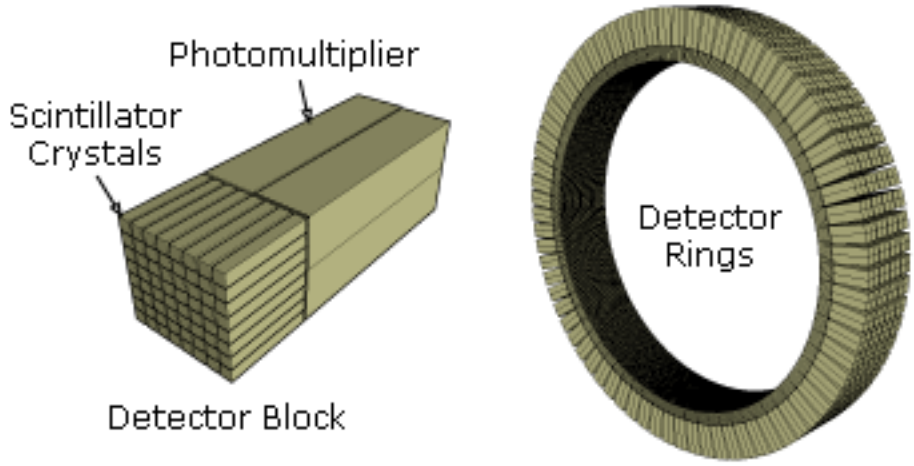

Figure 2. 4. Detector Rings Arrangement [2].

The amount of energy possessed by a 511KeV makes it easy for it to pass through many materials, including body tissue. Though it helps in observing the photon outside the body, but still it has to be stopped before the actual detection can take place. This is the job of the scintillator. Scintillation process is the transformation of high-energy photons into visible light through interaction with a scintillating material, and consists of the following steps [15]:

1) A photon incident on the scintillator creates an energetic electron, either by Compton scatter [16] or by photoelectric absorption.

2) As the electron passes through the scintillator, it loses energy and excites other electrons in the process.

3) These excited electrons decay back to their ground state, giving off light as they do so.

Scintillators can have different density, wavelength of maximum emission and timing characteristics depending on the materials they are composed of, including plastics, organic crystals, inorganic crystals and organic liquids. One common scintillator crystal is $Lu_2SiO_5(Ce)$, or LSO, which is an organic crystal.

2.4 PHOTODETECTORS

The visible light photons need to be converted to electronic pulses, in order to be processed. This is the job of the photodetectors, which follow the scintillators in the system. In the past, most of the photodetectors were photomultiplier tubes (PMT), which consist of a vacuum tube with a photocathode, several dynodes (series of electrodes within the PMT), and an anode that has high gains to allow very low levels of light to be detected. The emerging photodetector technologies, based on solid-state detectors, are considered the most promising candidates to replace the PMT because of their features – high quantum efficiency, high gain, operation at low bias voltages, and insensitivity to magnetic fields, excellent time resolution, robustness and compactness. In addition to their operating features, the ability to fabricate them with CMOS technology has created potential for the integration of the data acquisition and pulse processing electronics on the same substrate [17][18]. This helps in eliminating issues like the parasitic capacitance of interconnects and the large addition of noise. Solid state detectors are known by different names, like single photon avalanche diodes (SPADs), silicon photomultipliers (SiPMs) or multi-pixel photon counters (MPPC), but they are based on the same technology. They are reverse biased p-n junction diodes, with the bias voltage higher than the breakdown voltage. As a result, the electric field developed in the depletion region is higher than $3x10^5$ V/cm. In this bias condition, a single carrier injected into the depletion region can trigger a self-sustaining avalanche. This mode of operation is known as Geiger-mode Avalanche (GM), differentiating it from normal avalanche mode where

the bias voltage is close to, but less than the breakdown voltage of the semiconductor. In PET detection systems, the incident photon initiates the avalanche breakdown. In the SiPM, each diode is segmented into tiny micro-cells (each working in GM) connected in parallel to a single output, as shown in the Figure 2. 5(a) [19]. When activated by an incident photon, the current response is similar for all the microcells, making the output signal proportional to the number of cells hit by a photon. The number of micro-cells limits the dynamic range of the SiPM. Also, depending on the size of the micro-cell, 2 or more photons can hit the same microcell, reducing the dynamic range further. There are mainly two equivalent circuits for the SiPM available in literature. The difference between the two circuits is the way the firing micro-cells are represented. Corsi et al. [20] employ a current source, while Seifert et al. [21] and Claudio Piemonte [19] modeled the avalanche following a breakdown event using a voltage source V_{br} in series with a resistor R_S and a switch Sw, as shown in Figure 2. 5(b). Here V_{br} is the breakdown voltage and V_{bias} is the operating voltage. Initially the diode capacitance R_S is charged to $V_{bias} > V_{br}$ through the quenching resistance R_Q. When an avalanche discharge is initiated due to the incoming photon, the switch is closed, C_D discharges to V_{br} through the resistor R_S. As the voltage on C_D decreases, the current flowing in the quenching resistor R_Q tends to the asymptotic value of $(V_{bias} - V_{br})/(R_Q + R_S)$. R_Q being of the order of few hundreds of kΩ, this diode current is so low that a statistical fluctuation brings the instantaneous number of carriers flowing through the high-field region to zero, quenching the avalanche. The switch is again open and the circuit is in its initial configuration. The diode capacitance gets recharged back to V_{bias}, so that the diode is ready to detect the arrival of a new photon. A common arrangement of SiPM is an 8x8 array of 3 mm x 3 mm cells. Each cell has a density of about 10^3 diodes per mm^2.

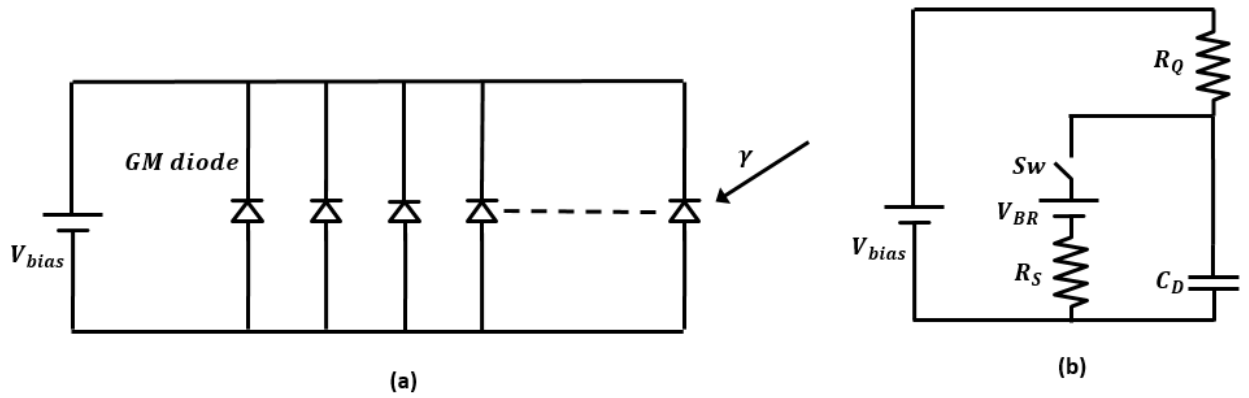

Figure 2. 5. Equivalent Circuits of (a) a single SiPM and of (b) a single GM-APD[19].

2.5 DATA ACQUISITION SYSTEM

Most of the information needed to create a PET image is contained in the photodetector pulses, like the location of the photon event and the time of interaction with the scanner. The next step is the processing of the pulses to extract this information. This is done with the data-acquisition system (DAQ). The roles of a DAQ system in PET are (1) to collect single photon events, (2) to identify coincidence events, and (3) to send the coincidence events to the image reconstruction PC. As explained before, coincidence events are the events detected from the simultaneously emitted photons. The coincidence events are identified using a parameter called the coincidence timing window, as shown in Figure 2.6. The choice of the timing window depends on the timing resolution of the system and the reduction of random coincidences.

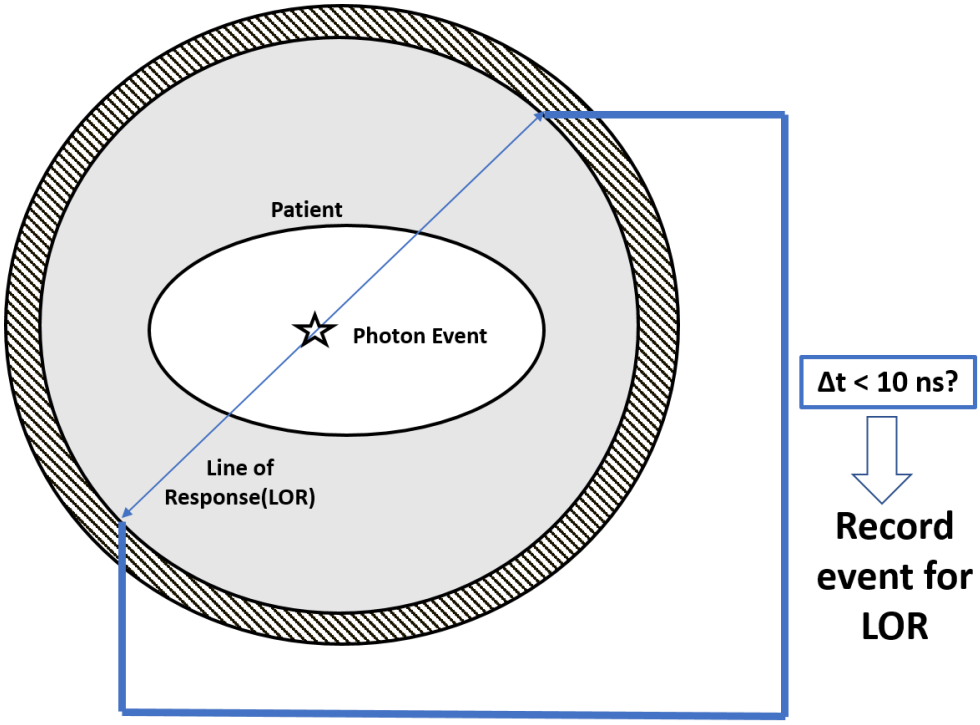

Figure 2.6. Coincidence Timing Window of 10 ns.

The design of the data paths of a DAQ system can be categorized into four parts - multiplexing, event generation, DAQ board interconnection to detect coincidences, and transmission to image reconstruction PC. For a PET imaging modality, the number of channels required varies depending on the application. For example, 400-600 channels are present in a small animal PET system, while that for a brain PET is ~4500. Specifically, the reduced size of the SiPM devices compared to PMTs implies an increase in the detector density, resulting in a proportional rise in the number of read out channels which interface to the digital backend. With the advent of 3D positioning architectures, X, Y, and Z components of an event can be captured, improving both spatial and image resolution. However, 3D positioning architectures lead to further increase in the array density, and hence the number of read channels also grows proportionally, requiring significantly more amplifiers and Analog-to-Digital Converters. With such a large number of channels, multiplexing is necessary to significantly reduce the number of connectors between the front-end

electronics and the backend DAQ boards, and also reduce the number of DAQ boards required. But, multiplexing can lead to degradation of energy resolution as well as timing resolution. The energy resolution can be degraded if the noise added in the multiplexing circuit is similar or larger than the original scintillation crystal. Pulse pile-up can also be an issue with large multiplexing ratios as more signals get merged together. All of these factors should be considered together before designing a multiplexing circuit. The signals from the front-end electronics are a stream of analog signals. After digitization in the back end ADC, the DAQ system is responsible for identifying a single event and extracting the timing and energy information of the event. Once the information of the event is acquired, it is stored in the form of an event packet and can be sent to other DAQ boards or stored into a local memory. The next step is identification of the coincidence events from the event packets generated from all the DAQ boards. The last data path in the DAQ design is the network connection to the image reconstruction PC. The network speed of the connection should be high enough to ensure no data loss. The required speed will be minimized if the DAQ system does all of the data processing. A possible alternative to replace the network connection is to provide a low power high frequency radio to provide bi-directional control and transfer between the DAQ and the image reconstruction PC. A separate radio will be needed on the image reconstruction PC to act as a receiver for this channel.

2.6 IMAGE RECONSTRUCTION

Image reconstruction begins after the collection of all the coincidence events in the host computer. Each coincidence event represents the line of response (LOR) for a particular positron emission event. Coincidence events are grouped into projection images, depending on the angle of each view and tilt (for 3D images). These projection images are known as sinograms. Back projection algorithms are then used to reconstruct images from these projections. But before that,

pre-processing of the data is required- correction for random coincidences, estimation and subtraction of scattered photons, detector dead-time correction and detector-sensitivity correction. An example of a PET scan image is shown in the Figure 2. 7. As the computing power of PCs is improving rapidly with the help of multi-core CPU and GPU processor technologies, some of the DAQ event processing can be off-loaded or post-processed in the image reconstruction PC. In the PC, events can be processed with more flexibility with high computing power and large memory size. In order to post-process events at the PC, more information needs to be transmitted to the PC.

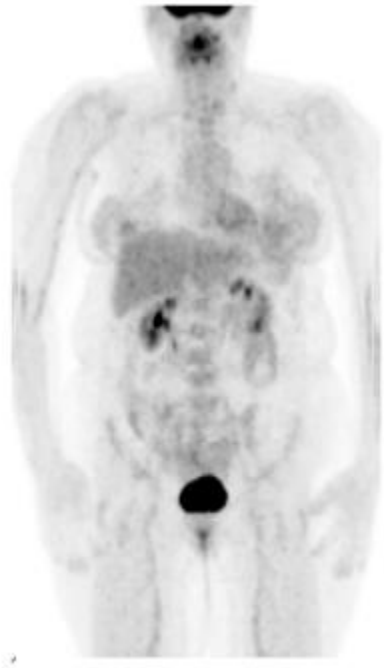

Figure 2. 7. Whole body PET scan image using [F-18] FDG. Notice all of the body has some radioactivity because glucose is utilized in many cells. Notable 'hot' spots are in the abdomen, the bladder near the bottom of the image (excess glucose is excreted in the urine), and the brain[23].

2.7 USES OF PET

Oncology – Fluorine-18 (F-18) fluorodeoxyglucose (FDG) is a radioactive tracer analogous to glucose. As a result, it is taken up by glucose-using cells and trapped there, until it decays. In

clinical oncology, PET scanning with FDG is used in radiolabeling of tissues with high glucose uptake, such as the brain, the liver and most cancers. FDG-PET can be used to diagnosis and treatment of patients with Hodgkin's lymphoma, non-Hodgkin lymphoma, and lung cancer.

Neuroimaging – Blood flow in different parts of the brain is believed to be correlated with the areas of high radioactivity in the brain. This has been measured using the tracer oxygen-15. However, because of its short half-life (2 minutes), it is difficult to use in practical systems. But since the brain pathologies like Alzheimer's disease can reduce the brain metabolism of both glucose and oxygen to a large extent, FDG-PET can be used successfully for early diagnosis of Alzheimer's disease. In addition, it can be used for localization of seizure focus.

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Chapter 3. SYSTEM DESIGN

SiPM devices have been implemented in CMOS technology in recent years, thus potentially enabling integration of a significant portion of the interface electronics on the same substrate with the detectors, which would reduce interconnect parasitic capacitance and inductance, while lowering the system power consumption. With respect to readout channels for SiPM detectors in PET applications, a majority of the circuits have been derived from previous discrete or integrated implementations developed for PMTs[24][25][26]. In contrast, recent efforts have attempted to integrate the readout electronics on a single die with dedicated designs for use with SiPM detectors [27][28][29]. However, a number of challenges exist for highly integrated front-end detectors. As mentioned in the previous chapter, the miniaturization of detectors due to reduced form factors of SiPM devices has led to a proportional increase in the number of channels interfacing to the backend. In an effort to reduce the number of channels for high-element arrays, multiplexing techniques have been utilized. When multiplexing large number of elements together, there are several key considerations with respect to analog IC impairments. First, the impact of circuit non-linearity on timing and energy resolution needs to be understood. While analog circuits can be approximated by a linear model for small-signal operation, nonlinearities often lead to spectral regrowth and distortion in the time domain that are not predicted by a linear small-signal model. Second, the impact of electronic noise needs to be understood. Electronic noise from thermal, flicker and shot noise often limit the lower end of the dynamic range, thus limiting the minimum detectable signal. Third, channel bandwidth plays a critical role in determining the high-frequency behavior of the interface electronics as often times the sharp rising and falling edge of a SiPM pulse contains high-frequency information useful for timing and energy resolution. Further, the input impedance of the front-end electronics together with the impedance of the microcells not

undergoing any breakdown will change the loading of the readout electronics and alter its high frequency response. To date, relatively little modeling has been done to understand the impact of analog non-idealities on SiPM-based PET systems. This chapter explores the impact of analog performance on the mixed-signal interface between SiPM devices and the digital electronics. The chapter is based on the work presented in [30]. The objective is to provide sufficient understanding of the effect of analog non-idealities on PET imaging systems, to be used as a part of a design methodology for the SiPM-based interface electronics. As a test bench to evaluate the relationship between analog performance and the overall image quality, the impact of additive Gaussian noise, linearity with respect to harmonic and intermodulation distortion, and channel bandwidth has been modelled using MATLAB simulations. The interface between an 8x8 Silicon Photomultiplier (SiPM) array and the Phase II MiCES FPGA boards[31] is used as a test bench to understand the impact of analog circuit performance on the achievable energy resolution using the commonly accepted metric of Full Width at Half Maximum (FWHM), as shown in Figure 3. 1.

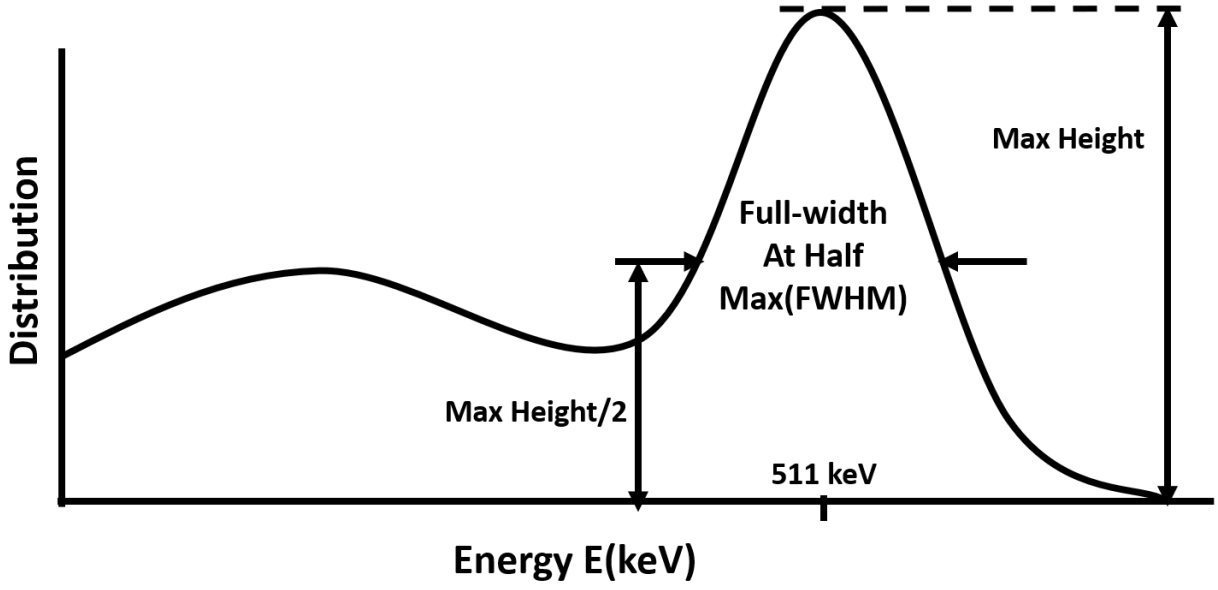

Figure 3. 1. Full Width at Half Maximum (FWHM) Energy Resolution.

The MATLAB simulation model for the front-end electronics is illustrated in Figure 3. 2. The blocks inside the dashed lines are used to emulate various analog impairments associated with the interface electronics including non-linearity, circuit noise and channel bandwidth. As a starting point, the MATLAB model uses a set of measured SiPM pulses. 2000 SiPM pulses were taken from a Zecotek Photonics MAPD-3N1 using a 511 keV Ge-68 radiation source as an input.Section 3.1 describes the impact of linearity using Intermodulation Intercept Points (IIPs). In section 3.2, additive white Gaussian noise has been used to model the impact of electronic noise on the system. Section 3.3 derives the impact of channel bandwidth on the system performance. Section 3.4 will describe a multiplexing architecture implemented in the first version of the ASIC in this project.

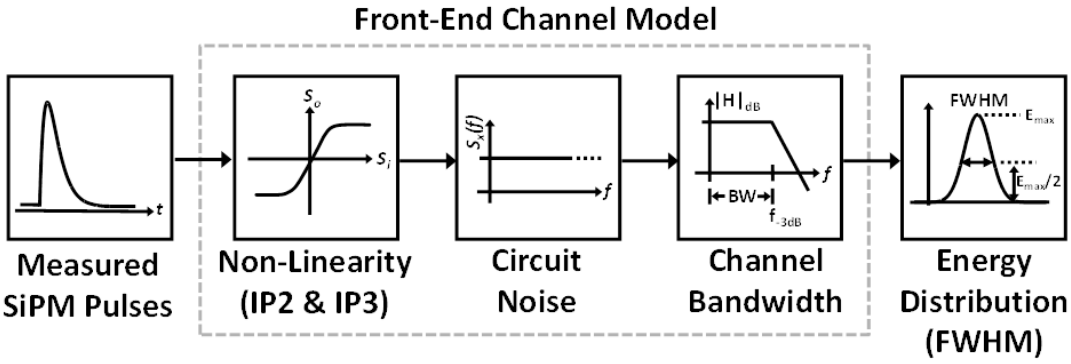

Figure 3. 2. MATLAB Simulation Model.

3.1 LINEARITY

The nonlinear behavior of a circuit can be viewed as variation of the small-signal gain with the input level. To model the nonlinearities of the channel, the circuit was assumed to be broad banded relative to the desired signal bandwidth. Stated differently, only resistive affects were considered and the circuit is assumed to be memoryless. This allows an approximation of the circuit nonlinearities in the channel using a Taylor Series expansion [32] as follows

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \ldots \qquad (1)$$

For small x, $y(t) \approx a_1 x$ indicating that a_1 is the small-signal gain in the vicinity of $x \approx 0$. The gain of the higher order terms can be related to common metrics of analog linearity performance in terms of the Input 2nd and 3rd order Intermodulation Intercept Point (IP2 and IP3) with the below expressions.

$$a_2 = \frac{a_1}{IIP2} \qquad a_3 = \frac{4a_1}{3IIP3}$$

The measured SiPM pulses were then applied to a Matlab model where the amplifier input referred linearity was defined using the above two expressions. The output of the amplifier blocks was then collected and energy resolution plots were constructed to help determine the FWHM as a function of linearity. The process was repeated with the IP2 and IP3 values swept from -30dBV to 0dBV. Figure 3. 3 shows plots of FWHM as a function of the amplifier IP2 and IP3, respectively. IP3 is seen to have negligible impact on the FWHM of the pulses. In large part, this is intuitively pleasing as the effect of circuit nonlinearities is to generate new spectrum, this is commonly referred to as spectral regrowth in power amplifier used in communication applications.

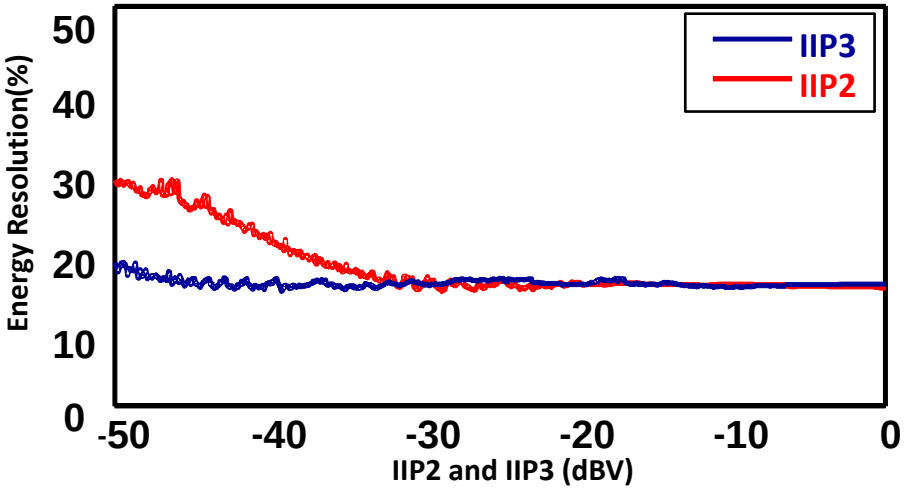

Figure 3. 3. Energy Resolution Vs Input Intercept Point.

Although nonlinearities will create new spectrum, the total energy associated with the analog signal is preserved, thus having minimal impact on the FWHM performance of the analog portion of the SiPM channel. This suggests that digitization of signals early in the interface chain is possible in future architectures. However, 2nd order nonlinearities are seen to have an impact on the FWHM.

3.2 NOISE

Assuming CMOS technologies are used to realize the SiPM interface electronics, there are a number of noise processes which may interfere with a detection pulse including thermal channel noise and flicker noise. Electronic noise corrupts the signal level, thus changing the energy associated with the signal. Another challenge associated with the row-column summation approach used in [33] is the potential accumulation of dark noise produced by each of the detectors connected on a row, column, or diagonal line, in addition to the thermal noise generated by the associated interference electronics. For the purposes of these simulations and modeling, additive white Gaussian noise was assumed to be the dominant source of noise. Scaling the noise floor in Matlab relative to the pulse amplitude was accomplished by estimating the signal power through simulation, then using the Signal-to-Noise Ratio (SNR) as a means to determine the variance of a noise source. Figure 3. 4 shows the energy resolution as a function of the SNR (dB) scaled relative to the magnitude of the SiPM pulses. The energy resolution begins to degrade for SNRs < 5dB suggesting a relatively modest noise performance required of the front-end electronics.

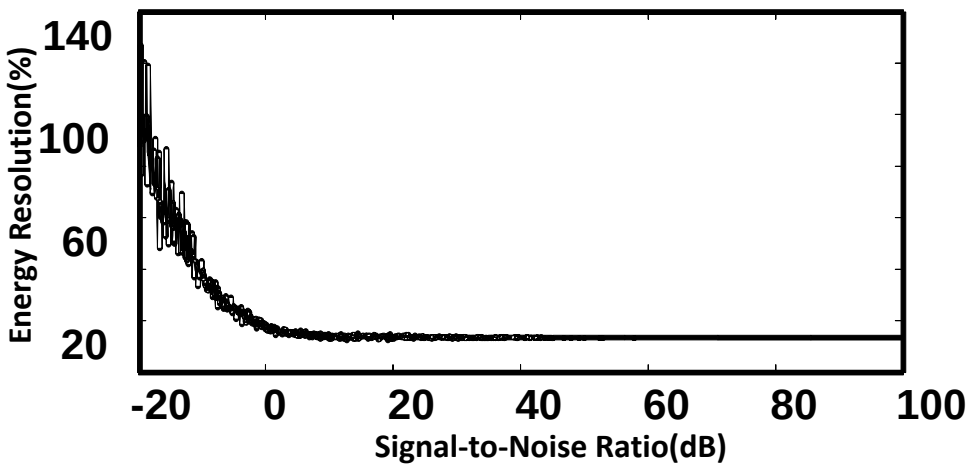

Figure 3. 4**.** Energy Resolution Vs Signal-to-Noise ratio.

3.3 CHANNEL BANDWIDTH

Although achieving constant open-loop amplifier gain up to several GHzs is possible using modern silicon processes, realizing similar bandwidths using closed-loop amplifiers becomes challenging above several hundred MHzs. Moreover, understanding the required signal bandwidth becomes crucial from the perspective of optimizing the overall power consumption of the front-end interface channel. The rise time of the SiPM pulses can be as fast as 20 ns. To understand the impact on energy resolution versus channel bandwidth, a 10^{th} order Butterworth filter was used in the Matlab simulation test bench to provide a sharp cutoff of the signal/channel bandwidth. The channel bandwidth was swept and the impact on the energy resolution was recorded. Figure 3. 5 shows that there is degradation in the energy resolution for cutoff frequency below 20 MHz. Although the bandwidth is relaxed in the case of detecting the energy resolution, higher bandwidths are required to detect the timing information for the proposed ASIC architecture[33] .This is because the anodes of all the SiPM devices in the array are shorted to a common node. This common anode signal is used to derive the time of arrival information for each SiPM pulse.

However, it is worth mentioning that only one common timing channel is required for the entire array.

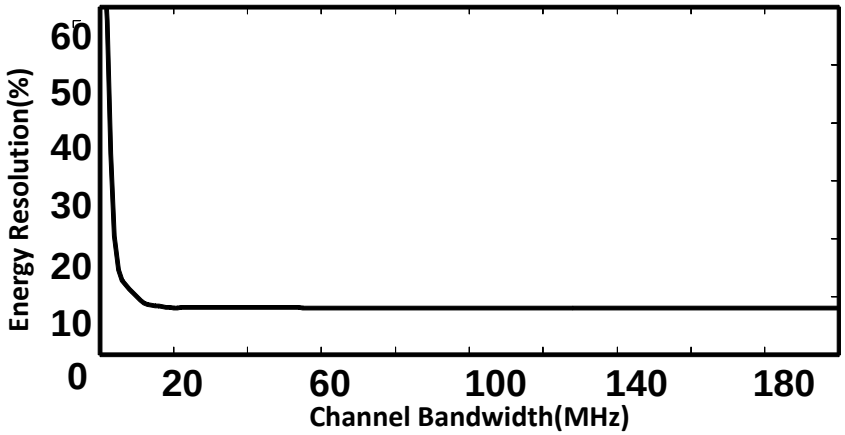

Figure 3. 5. Energy Resolution Vs Channel bandwidth.

3.4 ROW COLUMN SUMMING ARCHITECTURE (RCA)

Conventional readout electronics will dedicate an individual channel for each SiPM device in the array. Each channel consists of a SiPM detector which feeds either a current or transimpedance amplifier, after which the signal is driven off chip into a cable connected between the readout electronics and the ADC at the backend where digital signal processing takes place. For an N by N array, the channels are replicated N^2 times.

In the RCA approach, shown in Figure 3. 6, each SiPM detector output feeds a low-input impedance, programmable gain current amplifier. The amplifier interface is the only component of the readout electronics which is unique to each SiPM detector. The current amplifier has three output stages which feed a row output line, column output line and common pickoff line.

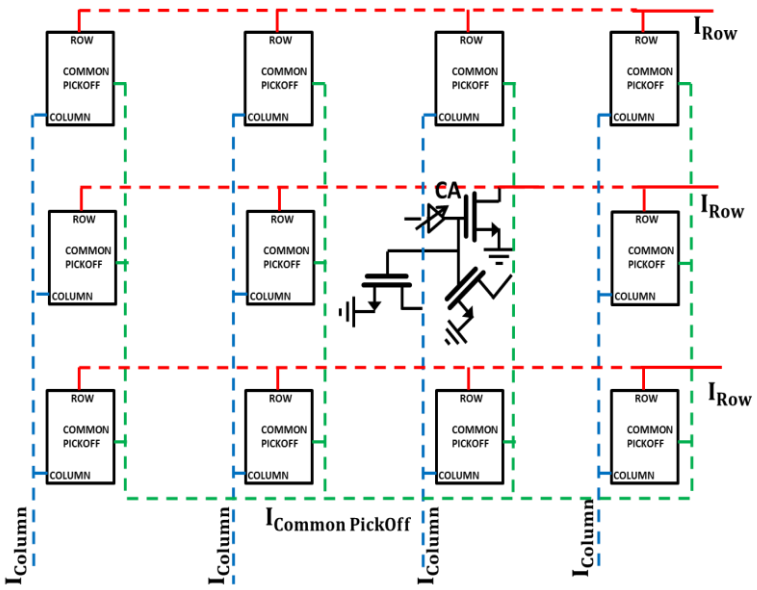

Figure 3. 6 Row Column Architecture (RCA).

The row and column channels provide spatial information of a detected event. The common pickoff channel, used as the timing channel, sums the output of all the array elements. This allows better timing information with respect to any individual SiPM event in the array, since it reflects the total current drawn by the array when multiple elements are fired. As all SiPM elements share this channel and the intent is to optimize timing, this particular channel needs significantly higher bandwidth as compared to the individual row and column readout (spatial positioning) channels. If there is a SiPM current at the input of any array element, there will be outputs across the corresponding row and column channels, as well as the common pickoff channel.

Each array element is implemented with a high speed current amplifier interfaced to the off chip SiPM device. The use of current amplifiers is motivated by the need to present low impedance from the perspective of the SiPM output, which reduces the current division between the amplifier input and the remaining SiPM cells. In addition, current mode circuits have significantly higher bandwidth compared to their voltage mode counterparts, thus facilitating wideband

implementations. The use of a single amplifier to interface the SiPM device has the additional benefit of reducing cross talk between the SiPM devices in the array. In addition, because a single amplifier (rather than three) is used to supply a row, column, and pickoff signal, the capacitance loading on the SiPM's cathode is minimized, further increasing the bandwidth of the detector-channel interface.

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Chapter 4. TIME OVER THRESHOLD (TOT)

Time over threshold (ToT) method directly converts pulse height into pulse width at an early stage of the front-end circuit. A comparator is used to determine whether the signal is above a pre-determined threshold. The comparator's output remains high during this duration and this information is digitized using a Time-to-Digital Converter (TDC), see Figure 4.1. The hope is that there is a strong correlation between the time a pulse is above a pre-determined threshold and the area under the curve of the pulse (i.e., the magnitude of the energy deposited in the crystal scintillator). This method helps to simplify system architecture, since it does not need complicated analog-to-digital converters to estimate the event deposited for a given pulse[34]. In this chapter, first we discuss how the number of thresholds impacts the performance of a ToT system (e.g., energy resolution of the photo-peak energy spectrum for a positron emitting radioactive source). Then we compare the power consumption of a ToT circuit and a conventional voltage domain digitizer.

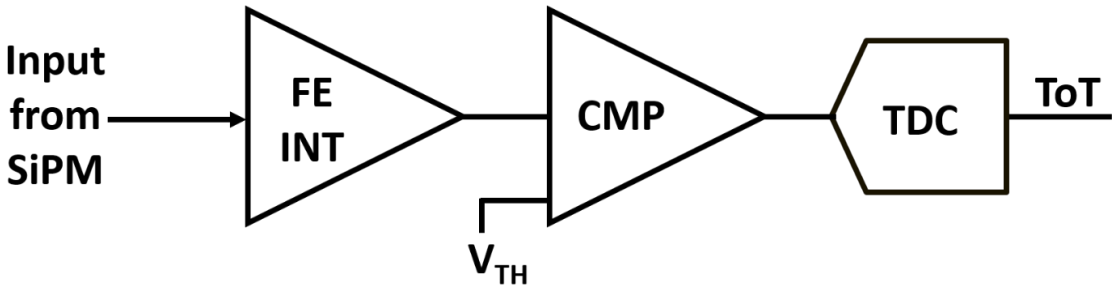

Figure 4.1. ToT architecture.

4.1 Data Acquisition(DAQ) for SiPM based PET Detectors

The design of the data acquisition(DAQ) and pulse processing electronics play a key role in determining the performance of a PET scanner. The signal from the photo-sensor carries

information about the energy, position and time of the photon event. In order to capture this, the readout electronics and signal processing needs a high bandwidth and low noise. Also, they have to accommodate a large number of channels (~1000) and a high event rate (~50M count/sec)[35] .The front-end electronics (FE INT) typically comprise analog/mixed signal circuits to process the detector signals, which are then passed on to the backend DAQ boards for further processing. A straightforward way to process the SiPM signals is to digitize the signals at an early stage of the readout electronics and acquire all required information from the waveform at the image reconstruction PC [36]. However, this implementation results in a significant area and power budget penalty, especially for Time-of-Flight (ToF) PET where high-speed digitizers (~2-5GSps) are required to sufficiently sample the fast signals[37][38]. Currently, majority of the PET systems employ an approach shown in Figure 4.2 where the signal is split in two different paths for extracting energy and time information. For the energy path a band-pass filter is used to remove unwanted noise and shape the pulse for digitization with a slow ADC to acquire energy information. The timing path has a wide bandwidth front-end amplifier to preserve the fast component of the detector signal for timing information. The sampling frequency for the digitizers used in the timing path have to be high enough to avoid aliasing effects and hence prevent loss of significant timing information, especially for ToF measurement, where acquiring the exact arrival times of photons is very important. Also, the sampling frequency affects the timing performance of the different timing algorithms used in the back-end digital electronics The two traditional techniques for timing algorithm are leading edge discriminators (LED)[39] and constant fraction discriminators (CFD) [40]. The leading edge method is very direct; once the signal has crossed the fixed threshold level, a trigger signal is generated but can give rise to timing errors such as time walk or time jitter. The cross-over timing method uses zero crossing of signal for time

measurements, which compensates for errors arising from amplitude walk but requires bipolar signals. In time-of-flight PET applications which use fast detectors, such as lutetium orthosilicate (Lu_2SiO_2 or LSO) or lutetium yttrium orthosilicate(LYSO) coupled to fast PMTs, the pulses produced have a rise time of about 2-3ns. For this case, a minimum sampling rate of 1.3GSps is required to achieve time resolutions of 200-300 ps FWHM for LED and CFD algorithms[41].

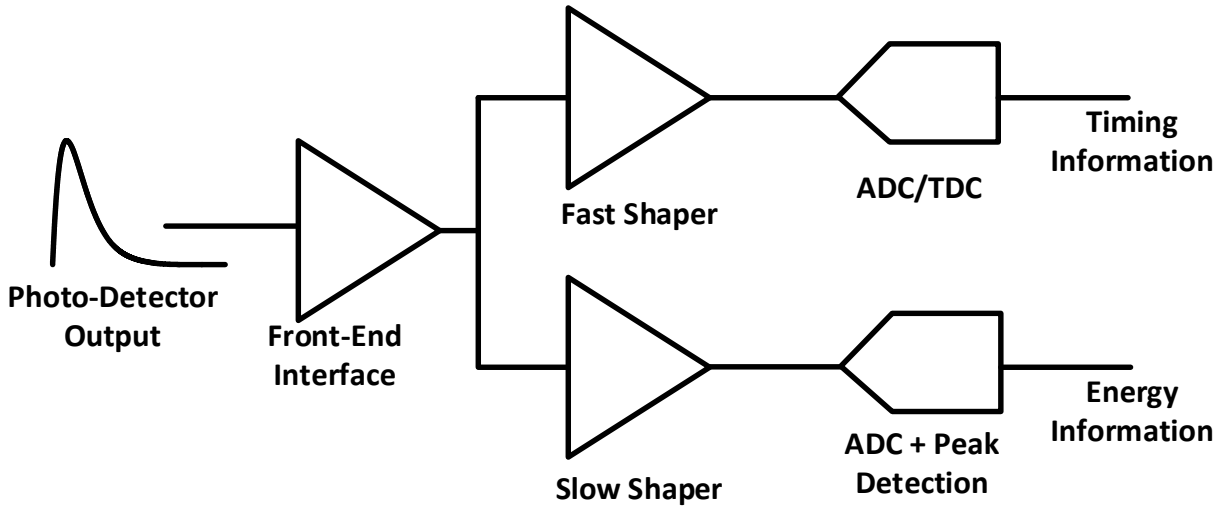

Figure 4.2. Traditional Data Acquisition Systems (DAQ).

4.2 TIME-OVER-THRESHOLD IMPLEMENTATION

Traditional ToT architectures [42][43] in high energy physics applications, use a single threshold level to determine the pulse width. Unfortunately, for SiPMs, the relationship between the pulse width and the pulse height is strongly non-linear, as evident from the pulse shape. Therefore, in conventional ToT systems for SiPMs, the pulse height information is usually corrected using a look-up table (LUT). However, this process requires a very precise time width measurement, because the time width varies only slightly for larger changes in pulse height. Increasing the number of thresholds helps to reduce this inherent nonlinearity. In dual threshold

systems [44][45][46], the low threshold is used for getting the accurate time stamp, while the higher threshold is used to report the energy information. The lower threshold is set as low as possible, just above the detector noise level. The high threshold is set below the 511 keV photo peak value at a level wide enough to reflect an energy window wider than the ones to be used for the final data analysis. When the input signal crosses the low threshold, the comparator output for the timing channel becomes high. If the input pulse crosses the low threshold but fails to cross the high threshold within a duration of time roughly equal to the rising edge of the pulse (16 ns in [46]) ,the energy channel doesn't turn on, resulting in no energy information and thus the event is discarded. The ToT data in the energy channel is recorded only when the signal crosses the high threshold with positive as well as negative slope, see Figure 4.3. The high threshold is set high enough to mitigate the problem of low dynamic range in falling edge threshold crossing time that typically accompanies ToT.

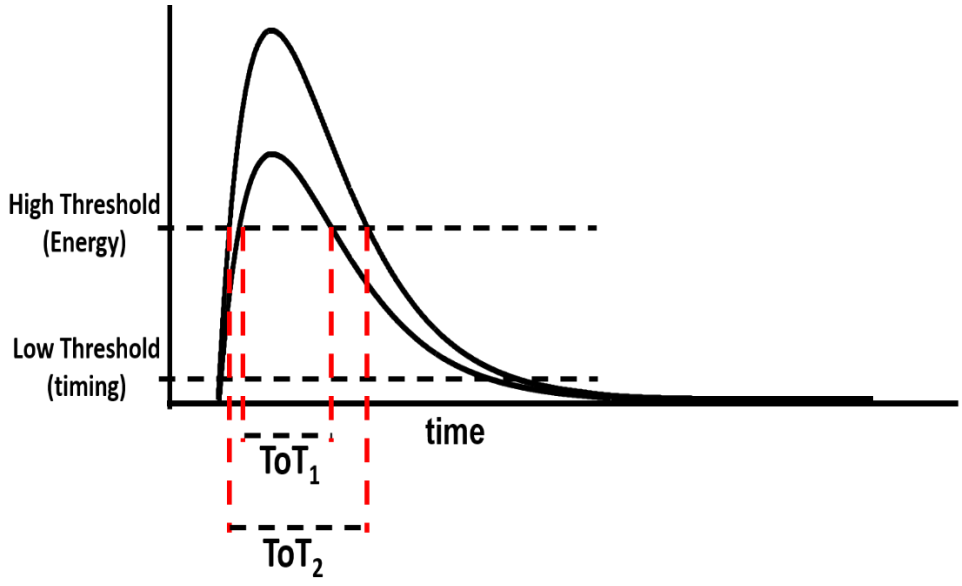

Figure 4.3. Dual ToT.

Although [46] shows an improvement in performance for dual threshold systems compared to single threshold systems, the system has been implemented using discrete components on a Printed Circuit Board (PCB). The target of this work is to implement a ToT system in a CMOS ASIC, so that the simplified architecture and low power consumption of ToT systems can be used to integrate large number of channels on a small CMOS chip. There have been previous efforts which implement CMOS dual ToT systems in 130nm [45]. In this work, the aim is to implement a Multi-Time-over-Threshold (MToT) system. MToT based systems have been already implemented in high energy physics applications, although all have been realized on PCBs using discrete components or for PET Systems with PMT detectors [47][48].

In multi threshold systems, the choice of the threshold voltages greatly effects the system performance. Time information is extracted by the time stamp of the lowest threshold on the rising edge of the signal. This technique is susceptible to variations of the trigger time with the amplitude of the pulse, in addition to the pulse shaping due to the interface electronics. To overcome this, the current implementation of the multi-threshold ToT system has several options utilizing the additional TOT threshold trigger time stamps. For example, we can use a simple extrapolation of the first three triggers to estimate when the leading edge rose above the noise floor of the photo-sensor. More advanced techniques are also under development building on some prior experience in our laboratory with digitized pulse wave forms (ref the FPGA algorithm work to estimate timing). One such approach is to use a model pulse that is fitted to the TOT data (trigger times and widths) and then use the model pulse to determine both the timing and integrated pulse value. Other approaches based on various statistical estimation techniques and machine learning algorithms are also being investigated.

For this thesis work, we tested the linear extrapolation approach using a pulse generation model for SiPMs generate 1000 signals at the input of the front-end amplifier. These pulses were for events at 511 keV, with a Poisson noise added. The output pulses were used to generate the time stamps using different thresholds in MATLAB and then the distribution was plotted. A threshold of 2-3 p.e. (~50 uA) generates a full width half maximum resolution of 200ps, as can be seen in Fig. 4.3.

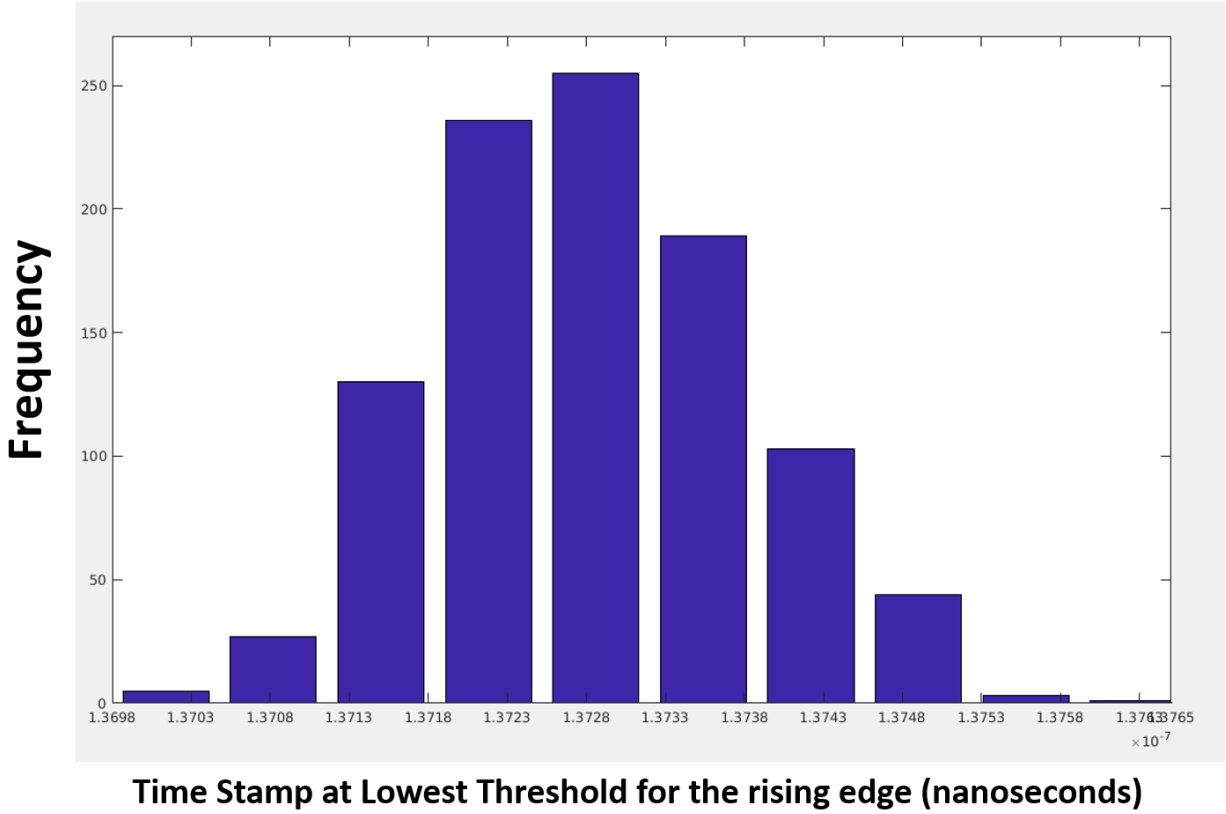

Figure 4.4. Distribution of time stamp from the lowest threshold.

The highest threshold will determine the energy resolution of the DAQ system. At the same time, it is important to note the non-linearity of pulse duration with respect to the pulse amplitude while choosing the highest threshold. The same 1000 pulses, as described above from the pulse generation model, was used to determine the ToT values for two thresholds – 25% and 30% of the

maximum amplitude for 511 KeV photon event. The distributions are shown in Figure 4.5 and Figure 4.6.

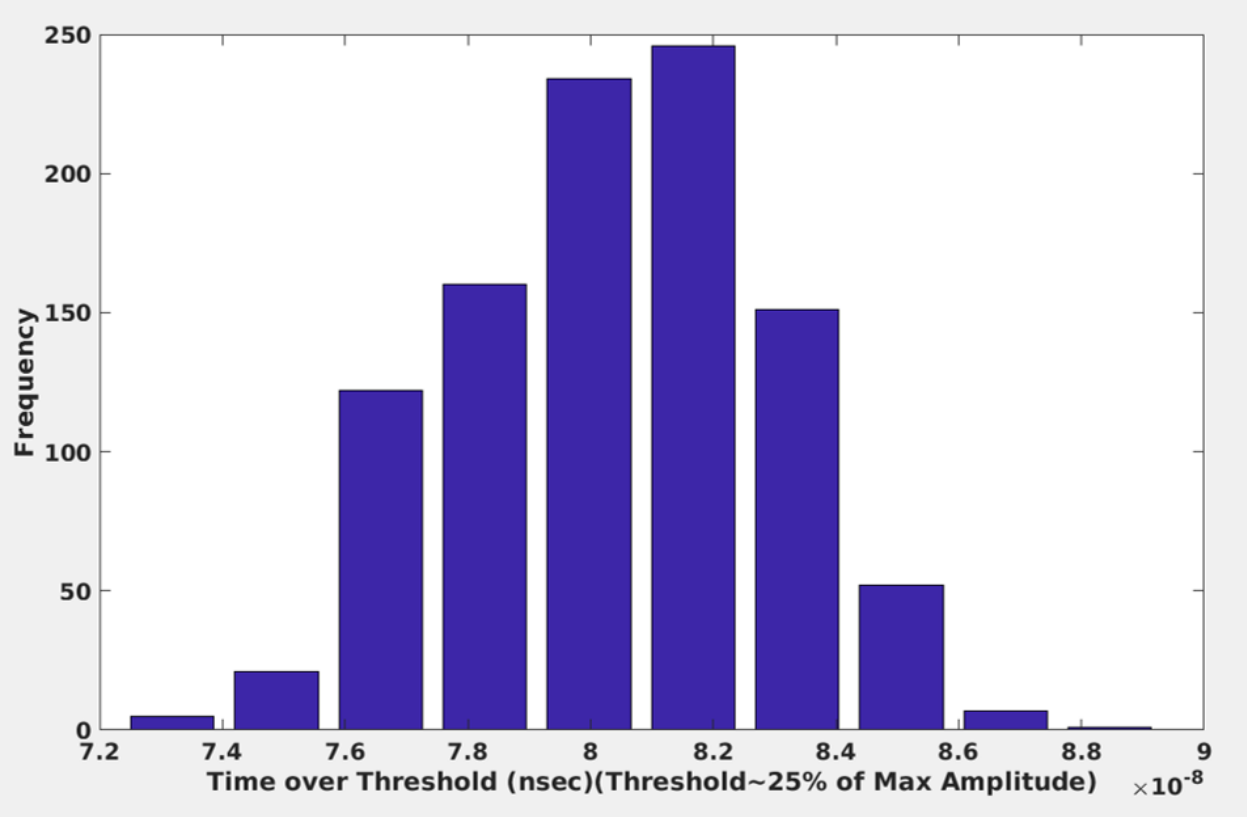

Figure 4.5. Distribution of Time over Threshold for threshold = 25% of maximum amplitude.

The threshold with 30% of the peak amplitude was then used to simulate the time over threshold for different energy photon events. This was done to investigate the linearity of the ToT data with the energy of the events. The energy events ranged from 200 KeV to 700 KeV, as shown in Figure 4.7.

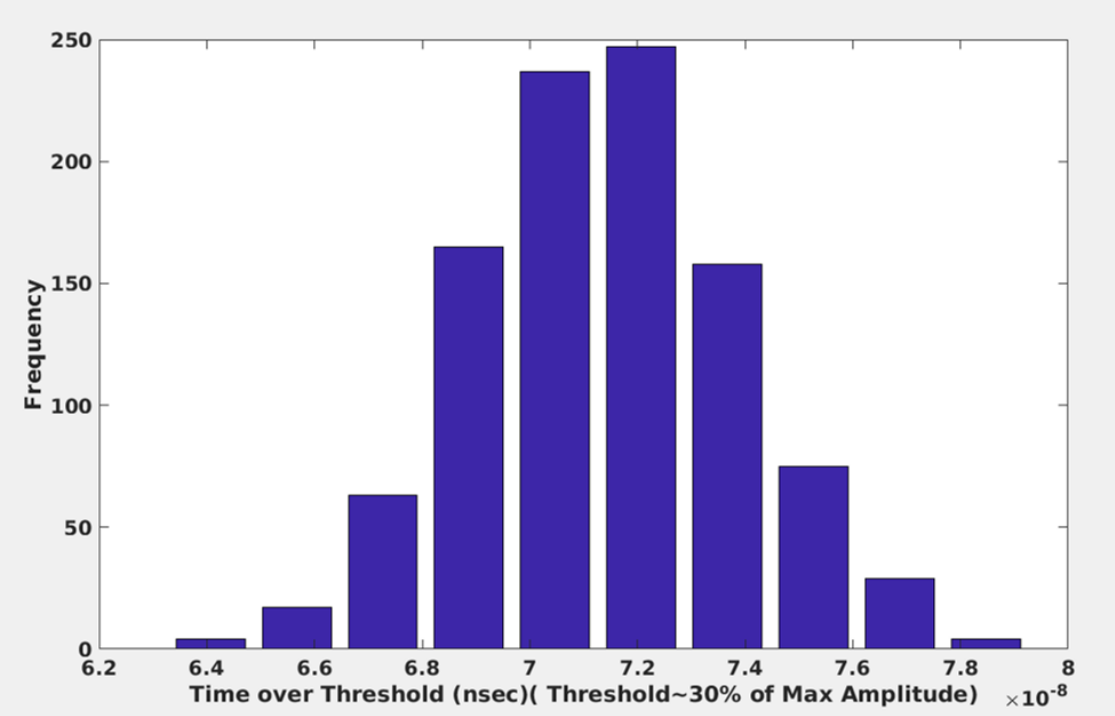

Figure 4.6. Distribution of Time over Threshold for threshold = 30% of maximum amplitude.

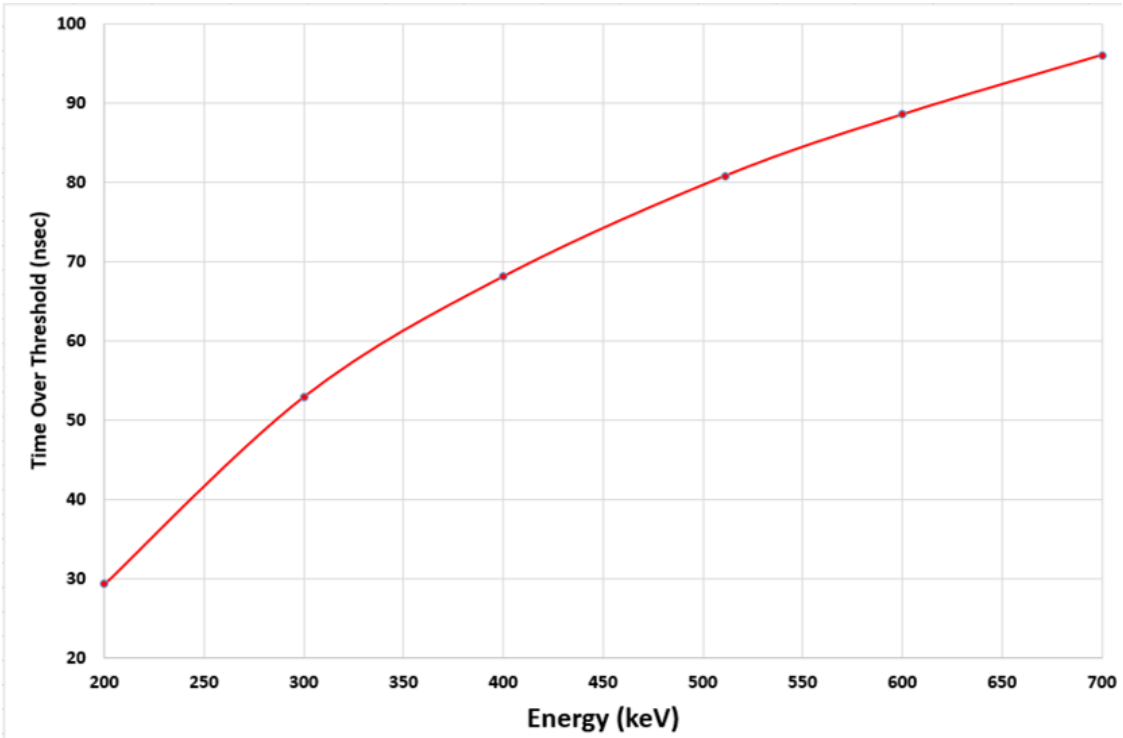

Figure 4.7. Time-over-Threshold versus Photon Energy.

4.3 POWER DISSIPATION BOUND FOR TOT

The main contributors to power consumption in a ToT circuit are the comparator and the TDC. For the TDC power estimation, we use a basic delay line based TDC, as shown in Figure 4.8. The delay line is comprised of identical buffers, BUFF. The TDC resolution is one buffer delay t_d.

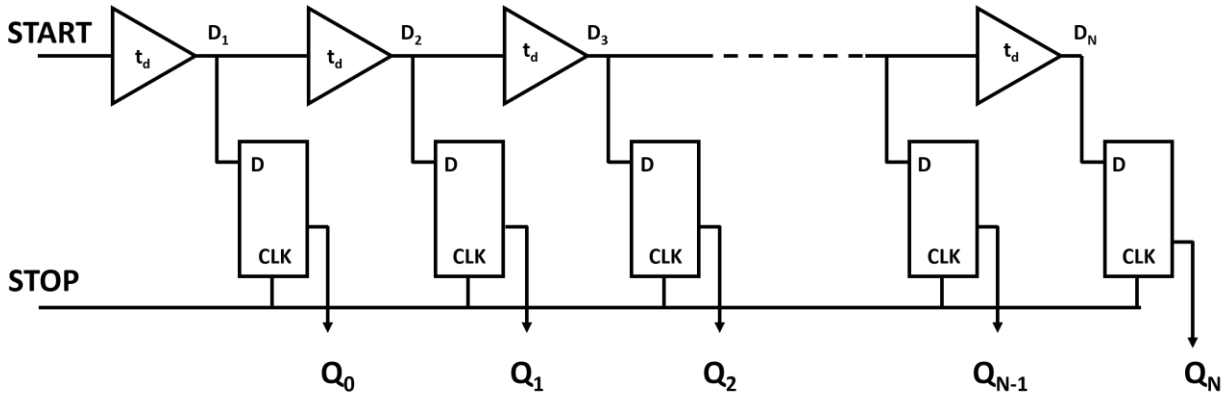

Figure 4.8. Delay-line based TDC.

The buffer outputs are the inputs of a series of D-flipflops. The rising edge of the *stop* signal latches the state of the flipflops, resulting in a thermometer code representation of the time difference between the start and stop rising edges. The total power consumption of the TDC is given by

$$P_{TDC} = P_{Buffer} + P_{FlipFlop} \tag{4.3.1}$$

For the purpose of comparing this power dissipation with a conventional ADC architecture, we take the example of a voltage domain flash ADC and develop an equivalent time domain flash TDC architecture from the delay line based TDC shown above [49]. The flash domain TDC architecture in a ToT implementation is shown here, Figure 4.9. The dynamic comparators are the flipflops. They are clocked by the stop signal. One of the inputs is tied to mid-rail voltage, while the other is connected to the output of the buffers. The outputs of the comparators are initially pre-charged to VDD. With the rising edge of the stop signal, the comparators enter the evaluation

phase and the outputs are either discharged to ground or maintained at VDD depending on the differential input of the comparators.

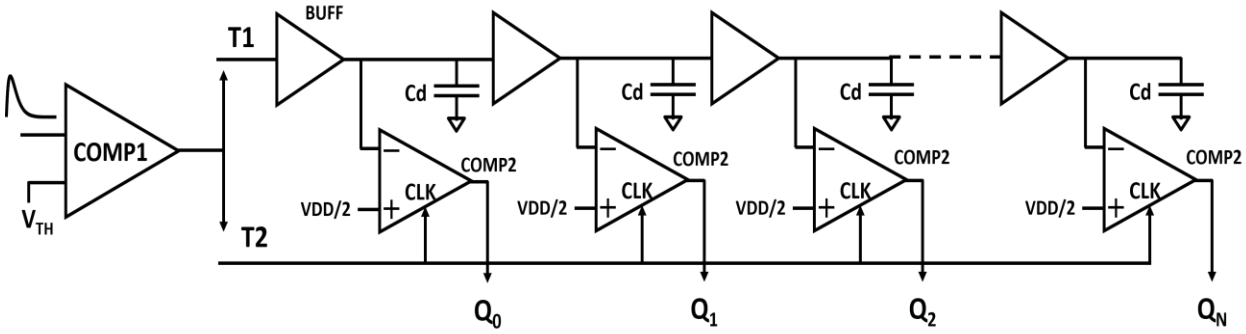

Figure 4.9. Flash domain TDC architecture in a ToT implementation.

In a ToT implementation, there will be an extra comparator needed to generate the start and stop signals for the threshold voltage Vth. The total power dissipation for the implementation is given as follows –

$$P_{TOT} = 2^N * P_{BUFFER} + P_{COMP1} + 2^N * P_{COMP2} \qquad (4.3.2)$$

For comparison, the minimum power consumption of a thermal noise-limited flash ADC and a thermal noise-limited pipeline ADC, derived in [50], have been used. The results are shown Figure 4.10. For very low resolution (number of bits < 4), the power dissipation of ToT is comparable with the traditional ADC architectures. But, as the number of bits increases, the ToT approach will consume considerably less power. Thus, as stated before, for PET imaging channels requiring a high dynamic range ADC, the ToT architecture provides an attractive low-power for SiPM based PET Imaging systems.

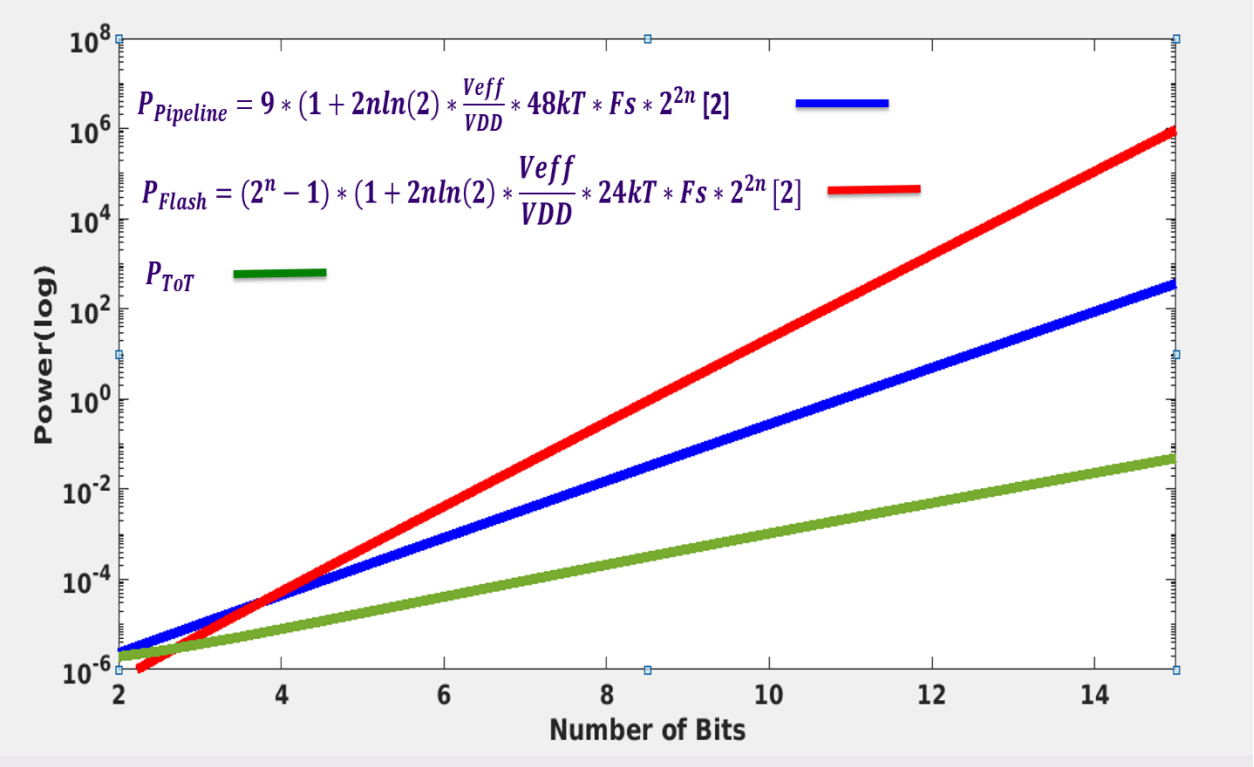

Figure 4.10. Power Dissipation comparison.

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Chapter 5. FRONT-END INTERFACE DESIGN

The large number of parallel microcells found inside a SiPM effectively reduces the complex impedance seen at the input of the front-end interface, making it essential to have a low input impedance front-end. This chapter begins with a description of a SiPM model to motivate the need for low input impedance interface electronics, followed by a description of the current amplifier architecture used in the first version of the ASIC. This will be followed by a discussion about the current mode threshold detection circuit implemented in the ASIC for dark noise mitigation. Finally, the front-end architecture used in the 2nd and 3rd versions of the ASIC will be described. Also, measurement results for both the front-end architectures will be presented.

5.1 SIPM EQUIVALENT MODEL AND SIPM-ASIC INTERFACE

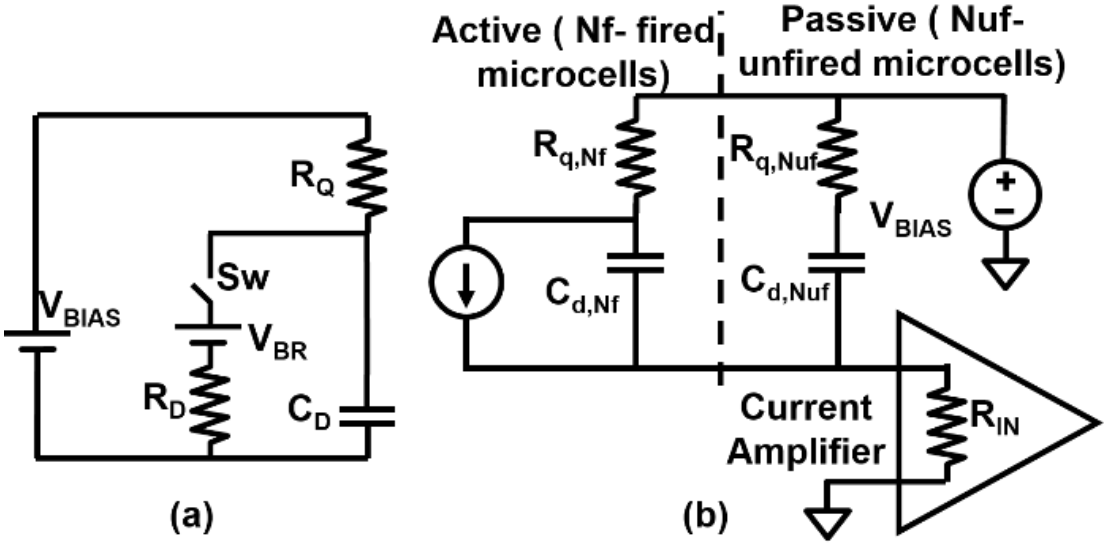

Figure 5.1. (a): SiPM equivalent model (V_{BIAS} is the operating voltage) and (b) SiPM- Front-end Amplifier interface.

The electric field developed in the depletion region of a SiPM device is higher than $3x10^5$ V/cm, due to the bias voltage being higher than the breakdown voltage. This region of operation is known as Geiger-mode Avalanche (GM), differentiating it from normal avalanche mode, where the bias voltage is less than the breakdown voltage. In PET detection systems, the incident photon initiates the avalanche breakdown. A SiPM diode is segmented into tiny micro-cells (each working in GM) connected in parallel to a single output. When activated by an incident photon, the current response is similar for all the microcells, making the output signal proportional to the number of cells hit by a photon. The equivalent circuit for a SiPM device [51] models the avalanche processes leading to a breakdown event using a voltage source, V_{BR} (the breakdown voltage), in series with a resistor, R_S, and a switch Sw across the diode capacitance $C_{D,}$ as shown in Figure 5.1. R_Q, a resistor on the order of few hundred kΩ, is used to reduce the current across the diode after the photon event, thus quenching the avalanche. The table below shows the values for the different elements in the model of a Hamamatsu SiPM device (N is the total microcells)[52].

Model Parameters	MPPC-S10362-11-25u- Hamamatsu N= 1600
V_{BR}(V)	68.8±1.5
C_D(fF)	15±1.2
C_Q(fF)	4.3±1.2
R_Q(kΩ)	179±1
C_G(fF)	7.5±1.9
R_D(kΩ)	1

Table 5.1. SiPM Model Parameters

The equivalent circuit simulating the discharge of N_f cells in a SiPM which consists of a total number of N_{tot} microcells and N_{uf} (= N_{tot}–N_f) unfired microcells, is illustrated in Figure 5.1(b). The equivalent resistor and capacitor values in the active (fired) and passive (unfired) part of the circuit are given by,

$$C_{d,Nf} = C_d * N_f, R_{q,Nf} = R_q / N_f \quad (5.1.1)$$

$$C_{d,Nuf} = C_d * N_{uf}, R_{q,Nuf} = R_q / N_{uf} \quad (5.1.2)$$

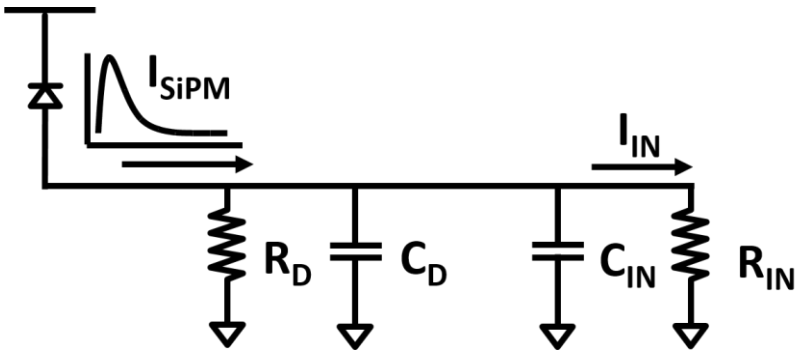

Figure 5.2. SiPM-ASIC Interface model.

$$I_{IN} = I_{SiPM} /(1 + R_{IN} / R_D + s(C_D + C_{IN})R_{IN}) \quad (5.1.3)$$

The SiPM ASIC interface is shown in Figure 5.2. Here, RD and CD model the SiPM impedance, while RIN and CIN model the input impedance of the front-end. The expression for the input current (5.1.3) clearly shows that a low input impedance front-end in the ASIC will prevent current sharing and extend the bandwidth at the interface. Current mode circuits have predominantly low impedance nodes, making them more favorable than their voltage-mode counterparts. Many of the existing current amplifier topologies have a direct tradeoff between the input impedance and bandwidth. A common-gate (CG) transistor with a large transconductance gm can be used at the expense of either a large device or a large amount of current. Shunt feedback can be used to

increase the effective gm, as is done in regulated cascode buffers (RGC)[53]. The limited voltage gain from a common source (CS) stage implies lower loop-gain, and thus, a limited Z_{in} reduction. The two versions of the front-end interface amplifier used in this work have been modified from the RGC architecture.

5.2 FRONT-END INTERFACE IN 1ST VERSION OF THE ASIC

This design includes an extra common gate (CG) stage in the feedback loop of the RGC buffer[54], Figure 5.3. In addition to increasing the loop gain, the CG stage decreases capacitive loading at the input and increases the available DC headroom as compared to a CS stage. However, the presence of two poles within the feedback loop requires attention. R_1 and C_1 compensate the frequency response of the loop with a zero, maintaining loop stability. The CG stage introduces noise at higher frequencies, but a signal-to-noise ratio of 5 dB at the output of the interface electronics is enough to maintain the full width at half maximum (FWHM) energy resolution of the SiPM pulses[30]. As a result, relatively modest noise performance is required of the front-end interface electronics in a SiPM based PET Imaging system.

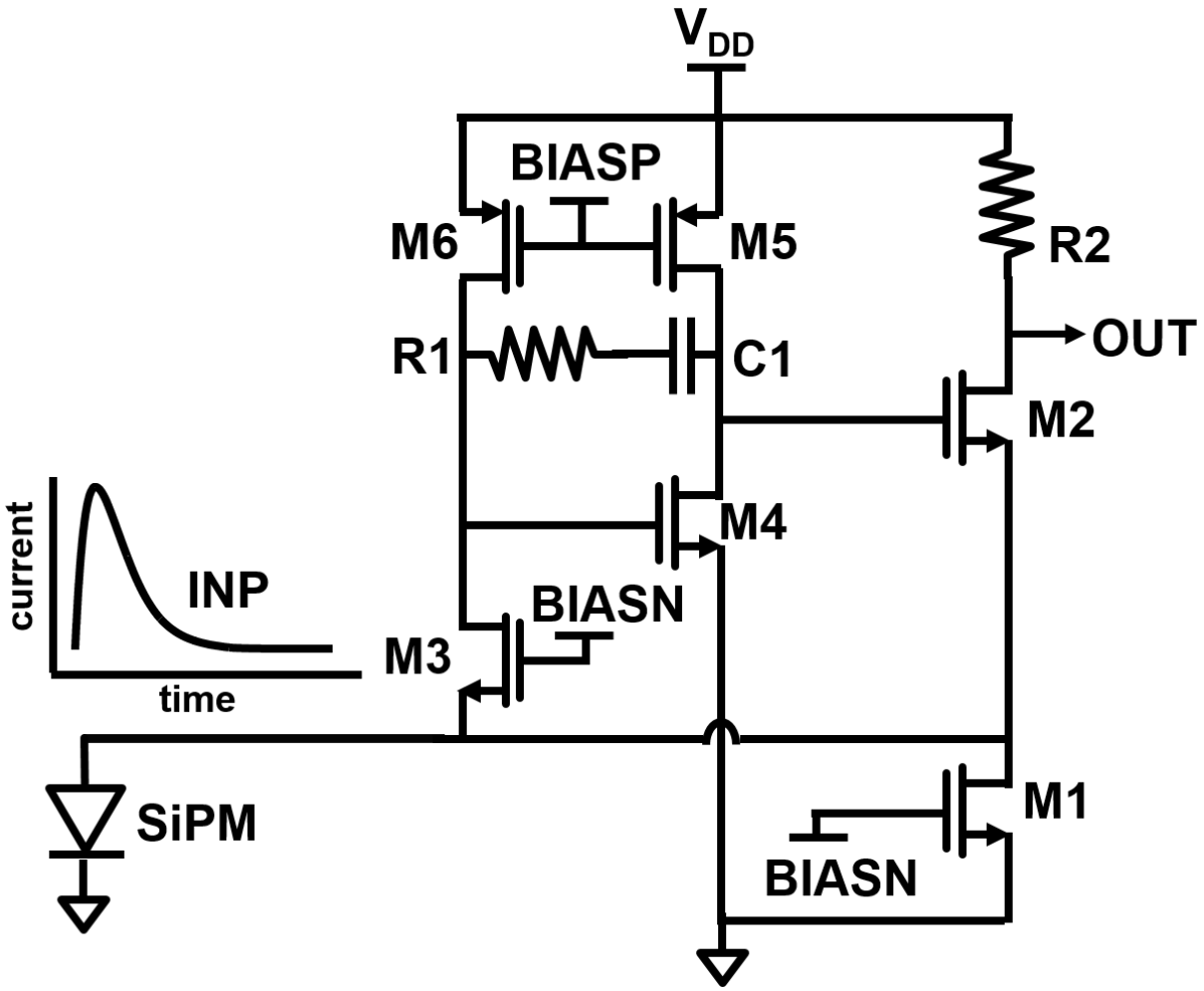

Figure 5.3. Modified RGC based Front-End Current Amplifier.

The high electric field used to bias a SiPM device can lead to avalanche breakdown due to non-photo generated carriers. Known as dark noise, this results from carriers, trapped during the discharge and released after a pulse event, or carriers generated by photons emitted during the discharge of neighboring photodiodes (optical cross-talk). As more channels are multiplexed or combined, as with the RCA architecture in the first version of the readout chip, dark noise becomes a major design front-end challenge. The situation is illustrated in Figure 5.4, where the dark current generated in an individual SiPM device is shown to accumulate with other detectors, sharing a row

or column output line. When the noise is added at the output, there is an increased chance of false triggering as compared to a single-channel readout of individual SiPMs, as the accumulated noise from the row or column output, is likely to be comparable to a desired signal.

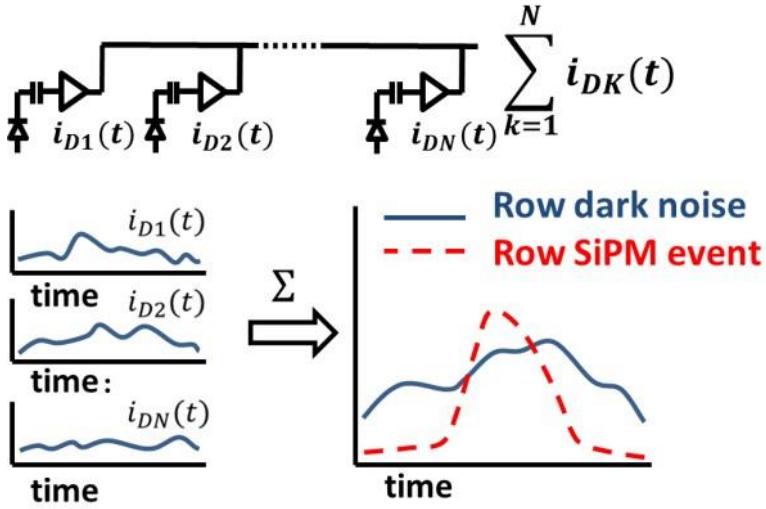

Figure 5.4. Dark Noise Accumulation across a single row.

To counter this, the readout chip utilizes a threshold detection circuit embedded with the front-end current amplifier to reduce dark noise events. The input SiPM pulse is compared with a programmable threshold, Figure 5.5. In its default state, the switch is open and the output of the amplifier is disconnected from either a row, or column output. If the input signal is more than the threshold, the switch is closed to connect the front-end amplifier with the output stage.

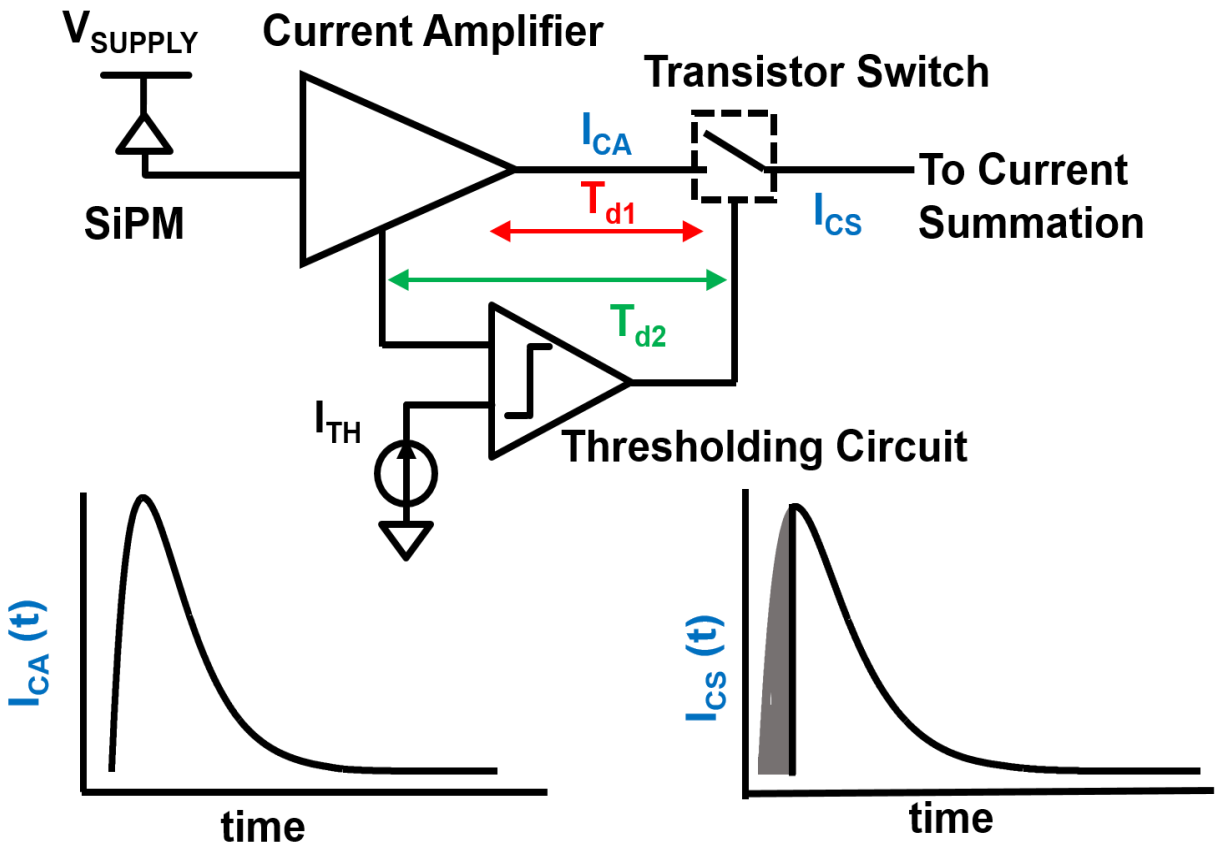

Figure 5.5. Illustration of clipping on a SiPM pulse rising edge.

This considerably reduces the overall noise at the output, thus enhancing the SNR for backend processing. There are several design aspects of this particular threshold detection circuit. First, different SiPM operating conditions require an adjustment of the threshold level, thus the circuit must be made tunable. Second, it is critical that the threshold detection circuit is fast enough to capture as much energy as possible associated with a real photon detection event. As the threshold detection circuitry takes longer to enable the readout signal path, more energy is lost from a single SiPM pulse, as is evident in Figure 5.5. In short, any mismatch between the delays TD1 and TD2 will clip the rising edge of the SiPM pulse, at the amplifier output. The SiPM pulses have a

considerably shorter rise time as compared to the fall time, and preserving the rising edge is critical to retain timing resolution in the overall PET system.

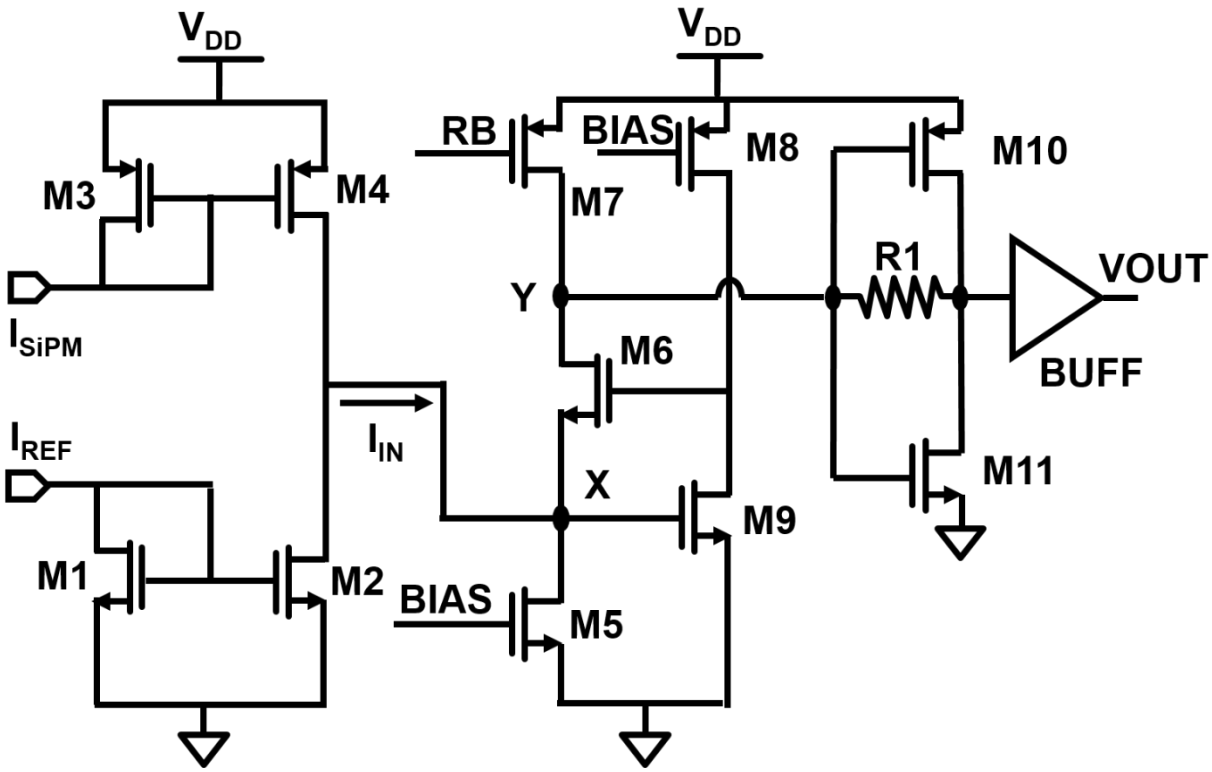

Figure 5.6. Current Comparator.

A current comparator is utilized to realize the threshold detection circuitry, shown in Figure 5.6. Traditional high-speed current comparators[55], are composed of three parts- the input stage, the current positive feedback circuit and slew rate enhancement circuits. Shown in Figure 5.6, the input stage is realized with current mirrors (M1-M2 and M3-M4), where the SiPM current is compared with a reference threshold current. The current fed to the second stage, IIN is simply the difference between ISiPM and IREF (IIN = ISiPM – IREF), see Figure 5.6. The reference current is tunable from 100μA to 1.5mA, allowing for a variable threshold, tunable for various SiPM devices. The second stage is a current comparator used to amplify the current difference from the first stage. Normally this is done using a source follower stage [56] where a low input impedance

allows detection and amplification of the current difference. In this work, a regulated cascode stage is used (M5-M9). The shunt feedback reduces the input impedance by a factor equal to the loop gain, resulting in a lower impedance than a source follower stage, making it more sensitive to changes in IIN. In the third stage, an inverter chain is used which amplifies the threshold detection signal forcing it to run rail-to-rail. A replica bias circuit (RB in Figure 5.6) is used to force the DC bias voltage at node Y to VDD/2. When there is no SiPM current, the threshold current mirrored by the transistors M3-M4 flows into the regulated cascode stage, thus bringing down the voltage of node Y from VDD/2. This drives the output of the comparator low, which turns off the transistor switch. When there is a photon event, transistors M3-M4 mirror the SiPM current to node X. If the SiPM current is lower than the threshold current, the comparator output retains the default operating condition as before, thus no signal pass through the current amplifier. However, when the SiPM delivers a current more than the threshold current, the voltage at node Y becomes higher than VDD/2. As a result, the output of the comparator is high, enabling the transistor switch (Figure 5.6). The inverter with resistive feedback (M10-M11) allows the transistors to operate in the saturation region, thus having a very high voltage gain and less propagation delay. Also, biasing node Y at mid-rail reduces the propagation delay by holding the inverter input bias voltage near the comparator tripping point. The low input impedance of the regulated cascode, followed by the high gain of the inverter, ensures that any change in IIN is propagated without delay to the output of the comparator, even at high frequencies.

The channel architecture for the readout chip is shown in the Figure 5.7. A low input impedance, high-output impedance current amplifier interfaces the SiPM device and produces a current which is shared with other SiPM devices along a row, column, or diagonal line. The current amplifier is designed to produce the lowest input impedance possible to improve the bandwidth at

the SiPM-Current Amplifier interface. Each amplifier has an additional high-speed current output that supplies a common timing signal. In order to minimize the accumulation of “dark current “produced by the SiPM devices, a current comparator is used in parallel with the main signal path and either enables or disables the output of the current amplifier. This comparator output goes high, and enables the current amplifier when the SiPM output reaches a predetermined threshold. A transimpedance amplifier acts as the interface between the summing lines and the off-chip ADC and FPGA by converting the single-ended current signal to a differential voltage. Analog line drivers are used to tune the channel output impedance over a range of loading conditions (50Ω - 200Ω) presented by a variation in the Firewire lengths, shape, etc., all of which influence the load impedance presented to the ASIC output.

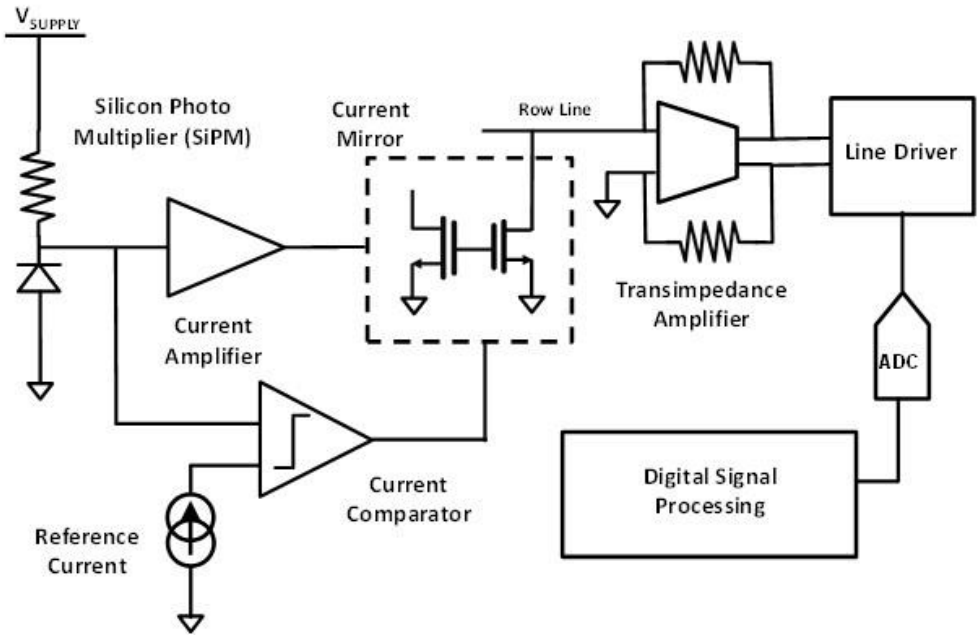

Figure 5.7. Channel Architecture.

5.3 FRONT-END INTERFACE IN 2ND AND 3RD VERSIONS OF THE ASIC

RGC based front-end interface helps to reduce the input impedance, but the presence of common gate stage in the feedback loop increases the power budget and makes the loop less stable. Also, the single-ended architecture leads to poor power supply rejection and common mode noise suppression. This can be improved by using a pseudo differential input stage, with the other input terminal connected to a dummy capacitive load. For the second version of the ASIC, a power supply voltage of 2.5V was used because of the back-end interface with the digitizers off-chip. So, a pseudo differential input stage would increase the power budget considerably for multiple channels. To counter this, the input stage was redesigned without a RGC stage. The second and third version of the ASIC are fabricated in 65 nm TSMC low power process.

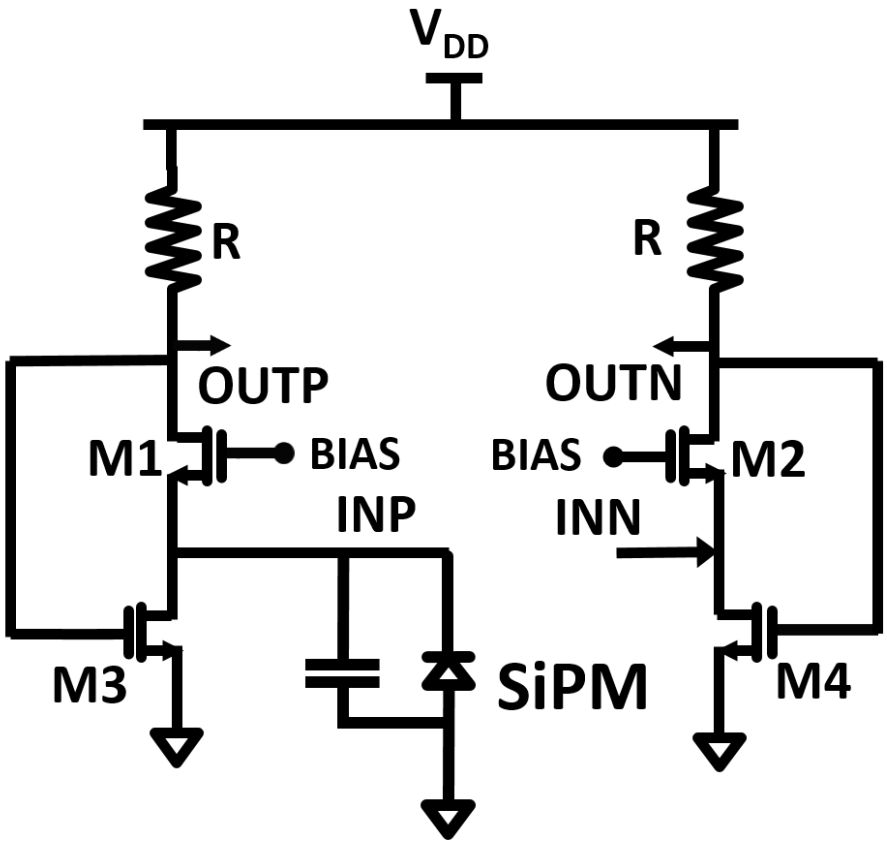

Figure 5.8. Current Buffer.

A more power-efficient current buffer has been designed using a modified version of the Wilson sense buffer (MWS)[57],Figure 5.8. M1 and R form a CG stage for the input current. M3 senses the output voltage and feeds it back to the input terminal INP. This shunt feedback loop lowers the input impedance. Similarly, M4 helps to reduce the input impedance at INN. This circuit has a better noise performance and less power consumption as compared to the previous design. Since the SiPM pulses are single ended, the negative input terminal INN is left open. This creates a pseudo-differential architecture, leading to improved power supply rejection and common-mode noise suppression. The input impedance of the current buffer can be described by –

$$Z_{IN} = 1/g_{m1,2}(1+g_{m3,4}*R) \qquad (5.3.1)$$

In the actual implementation (Figure 5.9), M5 and M6 are used as replica biased active loads to boost the loop gain of the shunt feedback, and hence reduce the input impedance even further. To account for any DC offset current from the diode, a high gain amplifier is used in a low bandwidth feedback loop as an offset cancellation circuit. A 10 % current offset is created between M5 and M6, while the residual DC current from the SiPM diode is compensated by using M7. The bandwidth of the loop is kept low using large capacitors to prevent signal loss at high frequencies.

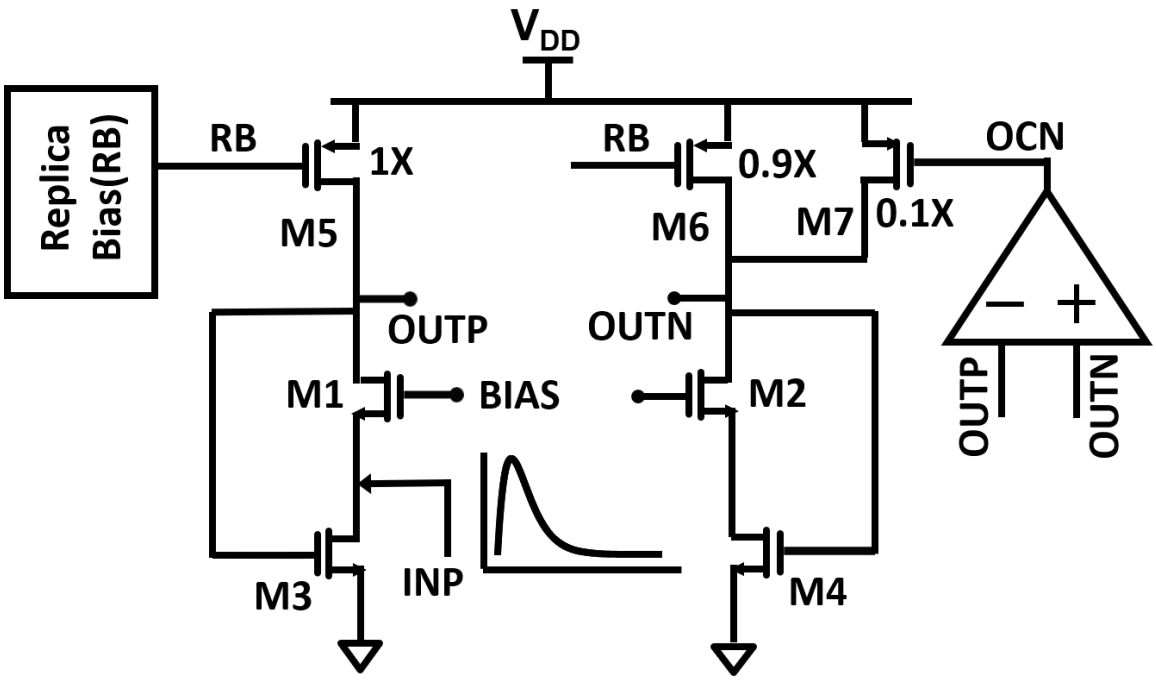

Figure 5.9. Front-End Interface implementation in the ASIC.

The channel architecture is shown in Figure 5.10. The channel architecture comprises – 1) a low input impedance Front-End Interface (FE INT) to interface with the SiPMs, 2) a programmable gain stage to amplify the SiPM signals and 3) output buffers to drive the off-chip digitizers. The core of the gain stage is based on a two-stage operational amplifier. To obtain a higher gain, the first stage incorporates cascade devices. The second stage allows large swings, to cover the entire dynamic range of the backend digitizers. The resistive feedback around the amplifier can be programmed using a shift register which tunes the channel gain over a range of 50-60 dB ohm according to the input signal amplitude. The tunable gain stage is followed by an output buffer to drive the digitizers off chip.

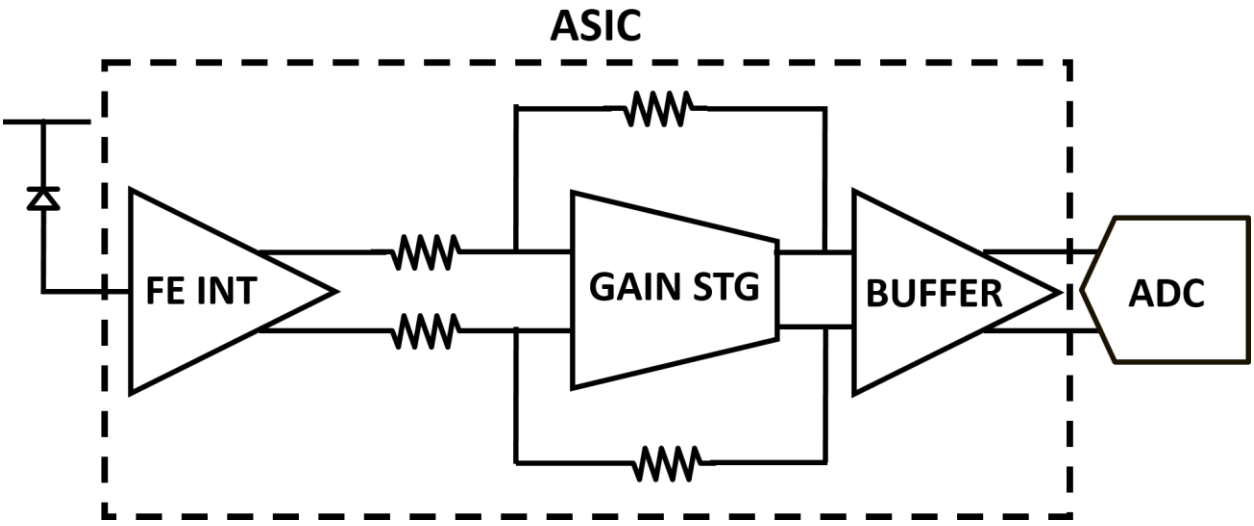

Figure 5.10. Block diagram of the Channel Architecture.

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Chapter 6. COMPARATOR DESIGN

In PET imaging applications, the rise time of the Silicon Photomultipliers (SiPMs) can be of the order of few nanoseconds, and in some cases even less than a nanosecond. The fast rising edge of SiPM pulse helps to extract the time-of-flight (TOF) information of the 511 keV photons during a positron annihilation. It is thus essential to extract the time stamp of the first photoelectron with a resolution of the order of 100 picoseconds. This requires the Time-over-Threshold (ToT) electronics to be fast as well as low noise. As explained previously, the first block in the ToT architecture is the comparator. This chapter will start with the description of the traditional dynamic comparator – Strong-Arm latch and discuss the limitations of this architecture. The design of an input driven self-clocked dynamic comparator architecture will be introduced with the transistor-level implementation of the proposed comparator for PET Imaging applications.

6.1 STRONGARM LATCH

Comparators are the basic building blocks of data converters. Broadly, comparators are classified into two categories – static and dynamic. Static comparators are high gain amplifiers operated in open loop condition. As a result, they clip to high or low voltage levels depending on the input differential voltage. The speed of these comparators depends on the input differential voltage, the input common mode voltage and the gain. As a result, the design of robust comparators tolerant to PVT variations is not straightforward. This problem is exacerbated for a multi-threshold ToT implementation across thousands of channels in a SiPM based PET Imaging system. Dynamic comparators have been widely used for analog-to-digital converters over the years as regenerative comparators. The most common topology for the dynamic comparator is based on the STRONG-ARM latch circuit [58], see Figure 6. 1. They provide an output after the transition of the clock.

The StrongARM latch topology finds wide usage as a sense amplifier, a comparator or simply a robust latch with high sensitivity. This topology has become popular for four reasons – 1) it has strong positive feedback enabling fast decisions, 2) it consumes zero static power, 3) it directly produces rail-to-rail outputs, and 4) its input-referred offset arises from primarily one differential pair.

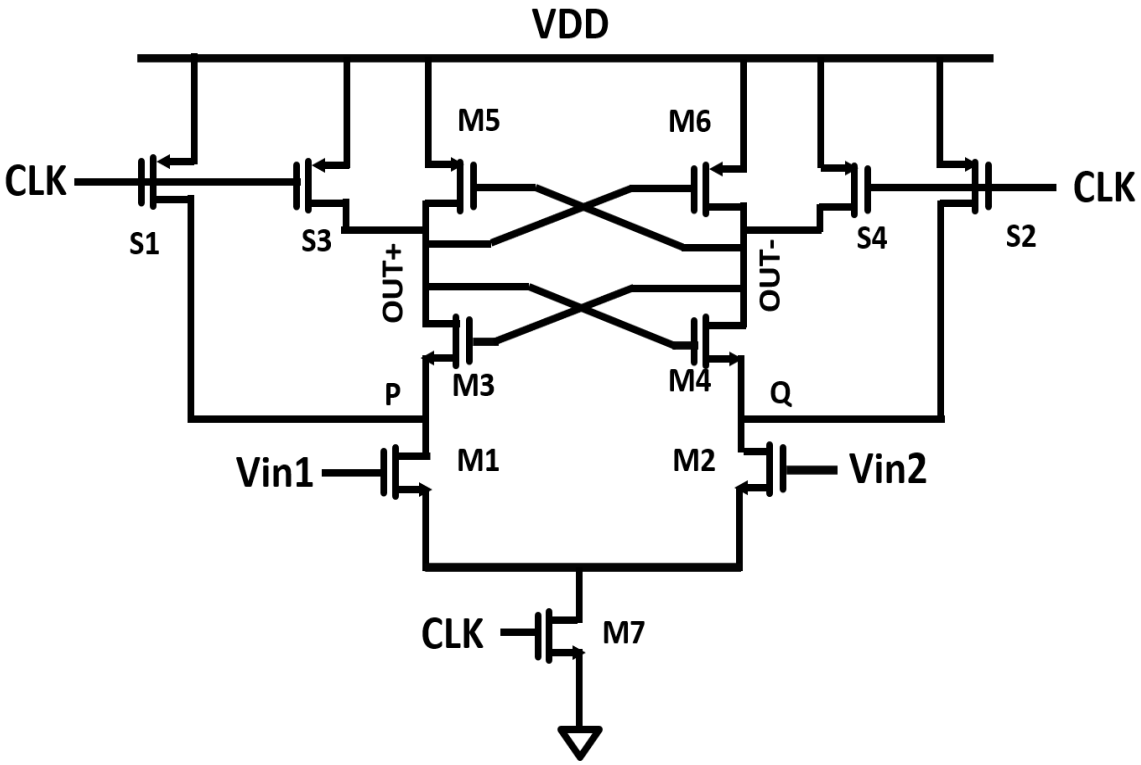

Figure 6. 1. Strong-Arm Dynamic Comparator.

The latch architecture consists of a clocked differential pair, M1-M2, two cross-coupled pairs, M3-M4 and M5-M6, an nmos tail device M7 and four precharge switches, S1-S4. M7 and the pre-charge switches are controlled by the CLK signal. Depending on the polarity of Vin1-Vin2, the circuit provides rail-to-rail outputs at OUT+ and OUT-. The circuit operation can be divided into two phases – reset and comparison, as shown in Figure 6. 2. In the reset phase, CLK is low and switches S1-S4 charge the nodes P, Q, OUT+ and OUT- to VDD. This phase ends and the

comparison phase begins when CLK turns high. The precharge switches are turned off, while M7 turns on providing current paths for M1 and M2. M1 and M2 turn on, drawing a differential current proportional to |VIN1 – VIN2|. This current starts to discharge nodes P and Q, and thus |VP – VQ| grows. When VP and VQ fall below VDD – VTHN (VTHN is the threshold voltage of M3 and M4), the nmos cross-coupled pair turn on and starts to discharge nodes X and Y. When VX and VY fall below VDD - |VTHP| (|VTHP| is the threshold voltage of M5 and M6), the pmos cross coupled pair turn on and the circuit enters the latch phase. The positive feedback around the cross coupled pairs eventually bring one output back to VDD and allows the other to fall to zero. Again, the cycle repeats when CLK becomes low.

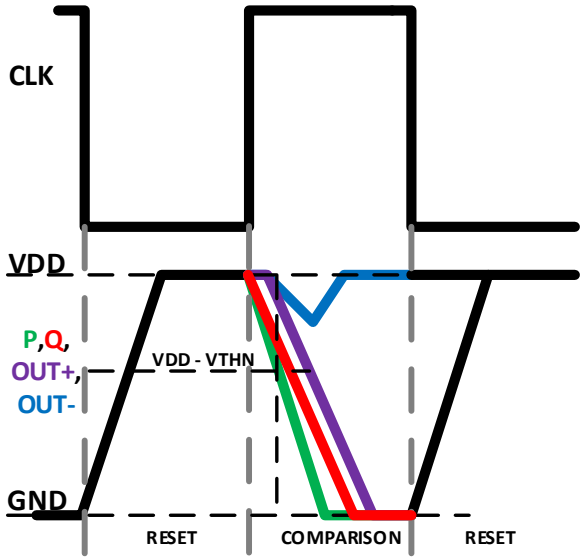

Figure 6. 2. Operation of a dynamic comparator.

6.2 Input Driven Self-Clocked Dynamic Comparator

The power consumed by the strong-arm latch arises primarily from the charging and discharging of the capacitances- mainly, $CV_{DD}^2 f_{CLK}$ losses, where f_{CLK} is the clock frequency, C is the capacitance and V_{DD} is the supply voltage. A number of methods have been proposed to reduce this switching power [59][60][61]. Most of these techniques attempt to reduce the signal swings

across the nodes. This work presents a novel way to reduce the switching power using an input driven self-clocking mechanism. Figure 6. 3 shows the difference between the traditional dynamic comparator and the proposed technique. In Figure 6. 3(a), a dynamic comparator is operated using an external clock. Because of the switching states of the clock, there is continuous charging and discharging of the capacitance irrespective of the voltage difference at the input (VIN – VREF). But if the clock is enabled when the voltage difference is less than a certain voltage (|VIN-VREF|<Δv) and disabled otherwise, the switching activity can be reduced, as shown in Figure 6. 3(b). The proposed method accomplishes this using a pre-amplifier stage and a feedback loop around the comparator, which causes it to oscillate, as shown in Figure 6. 4. The oscillation stops when VIN>VREF on the rising edge and VIN<VREF on the falling edge, as shown in the Figure 6. 4. This novel comparator architecture[62] has switching power dissipation due to $CV_{DD}^2f_{CLK}$ clocking losses only over a narrow amplitude of the input signal, instead of using a constant clock to driver the comparator which would producing a continuous switching activity and $CV_{DD}^2f_{CLK}$ losses independent of the input signal amplitude.

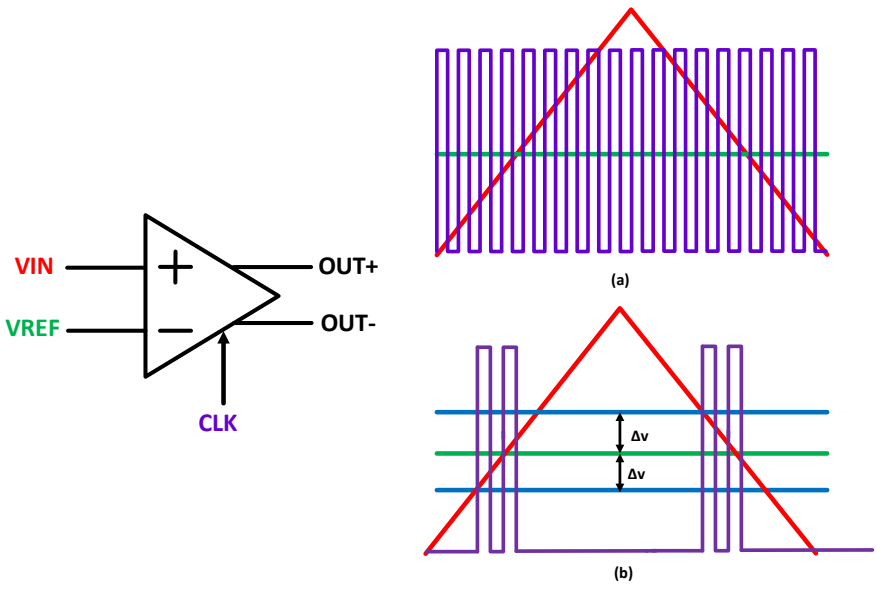

Figure 6. 3. (a) Traditional Dynamic Comparator (b) Proposed Comparator.

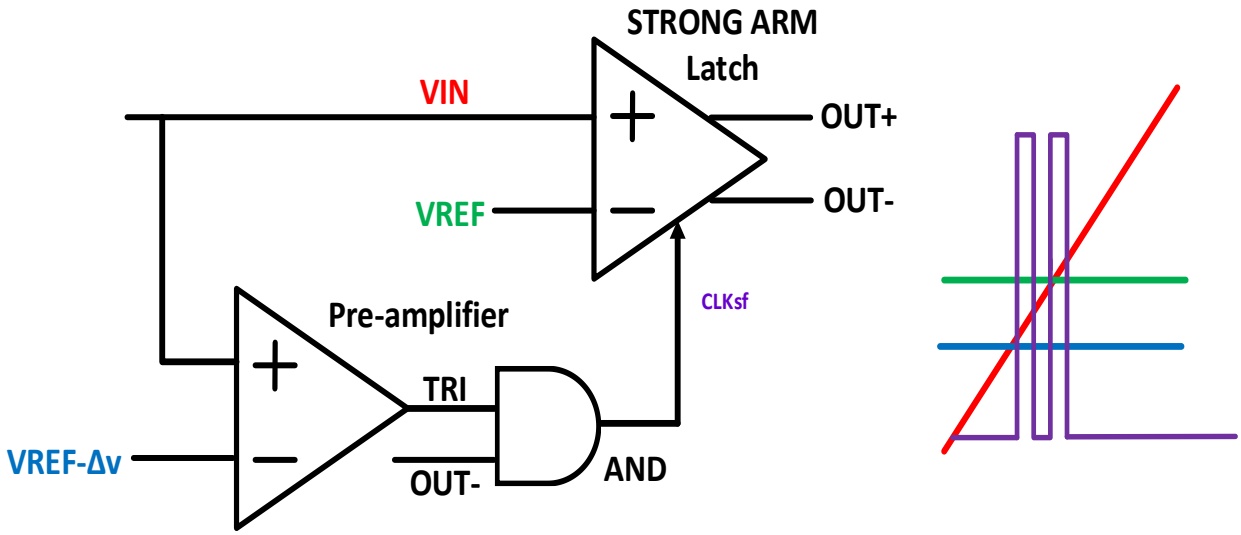

Figure 6. 4. Input Driven Self-Clocked Dynamic Comparator.

The key aspects of the technique shown in Figure 6. 4 are – the clock signal, the magnitude of Δv and whether it works for the both the rising as well as the falling edges of the input signal. This analysis will first consider the rising edge of the signal. In the proposed technique, the self-clocked dynamic comparator has an AND gate in addition to a traditional STRONG-ARM latch comparator. Figure 6. 5 shows the operation of the comparator. The AND gate generates the clock signal CLK_{sf} for the comparator and it is driven by one of the outputs, OUT- in this case, and an enable (EN) signal. When EN is low, CLK_{sf} is low and the switches charge the nodes P, Q, OUT+ and OUT- to VDD. When EN is high, CLK_{sf} becomes high. This turns M7 on and the switches S1-S4 off. This starts the comparison phase. Nodes P and Q are discharged by M1 and M2 depending on |VIN – VREF|, and as before when they fall below VDD-VTHN, the NMOS cross coupled transistors are turned on. This starts discharging nodes X and Y, and when they fall below VDD-|VTHP|, the PMOS cross coupled pair turns on. As long as VIN<VREF, OUT- gets discharged to zero while OUT+ gets restored to VDD. OUT- becoming zero makes CLK_{sf} zero as well. So, the PMOS switches are turned on again and the nodes are charged back to VDD. OUT-

becomes VDD again, and this makes CLK_{sf} high. Thus, the comparator is ready for evaluation again. This cycle continues until VIN becomes sufficiently higher in magnitude than VREF, and OUT+ gets discharged to zero at the end of the latch regeneration phase. When this happens, OUT- gets restored to VDD and hence, CLK_{sf} stays high. This stops the comparator operation and prevents any more power draw from the supply. For the falling edge, an extra pre-amplifier is used, as shown in Figure 6. 6 This pre-amplifier generates a trigger signal when the input signal goes below (VREF + Δv), shown in Figure 6. 6. This trigger signal is then ANDed with OUT+. The two AND gates are then combined using an OR gate. The output of the OR gates serves as the clock signal CLK_{sf} for the comparator. As shown in the Figure 6. 6, the comparator is clocked for a narrow range on the input signal around the reference voltage, and rest of the time it's disabled. This helps in reducing the switching power dissipation because of charging and discharging of capacitance. The self-clocking circuit is contained within the comparator itself, thus this obviates the need to route the clock to another circuit block. As such, the parasitic capacitance loading the self-clocking circuits is minimized and negligible as compared to a traditional comparator using an externally generated clock. Therefore, the self-clocking dynamic comparator may improve the decision speed of the dynamic comparator by having a higher clock speed, than a traditional comparator using an externally generation clock, due to the fact that parasitic capacitance has been minimized with the self-clocking technique.

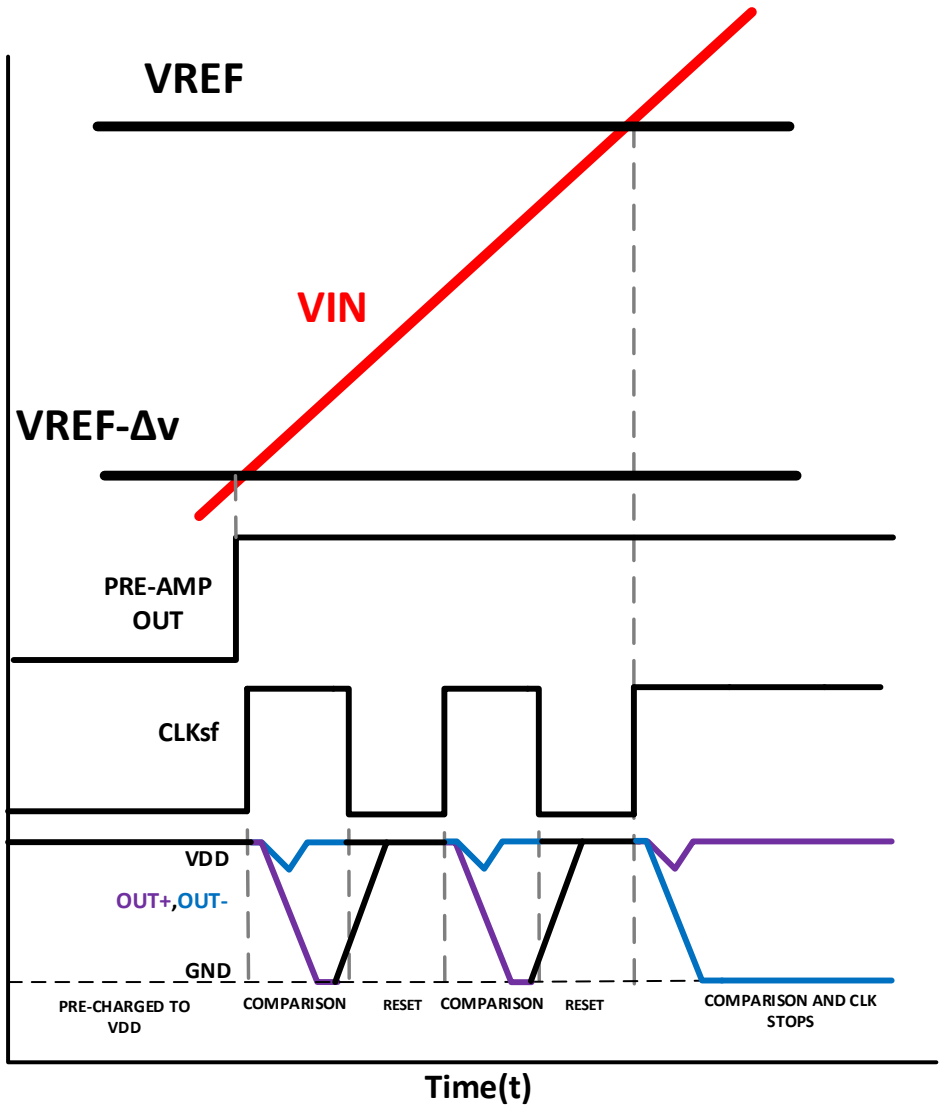

Figure 6. 5. Operation of input driven self-clocked dynamic comparator.

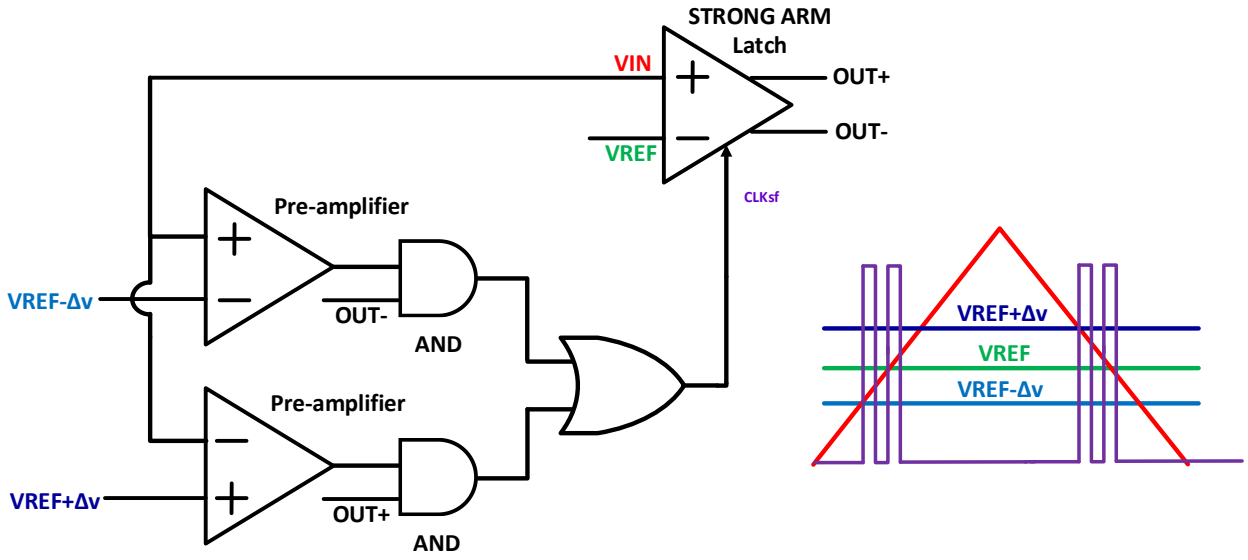

Figure 6. 6. Input driven self-clocked comparator operating on rising and falling edge of the input signal.

For validation, the self-clocked comparator and the strong-arm comparator were simulated with same input signal and reference voltage. The input signal had a rise time of 1 nanosecond, ramping from 800 mV to 1.2V. The reference voltage for the test bench is 900 mV and Δv is 50 mV. The clock for the strong-arm comparator had the same frequency as the oscillation frequency of the clock generated by the proposed technique, which is 7GHz in this setup. This frequency is determined by the delay across the comparator and the AND gate. The transient simulation results are shown in Figure 6. 7 and Figure 6. 8. The pre-amplifier generates a high output (EN) when the input signal becomes greater than 850 mV(VREF-Δv) and enables the comparator. Before that, OUT+ and OUT- are both charged to VDD and the comparator is ready for evaluation. Once EN triggers the comparator, OUT- gets discharged at the end of every latch phase until VIN is less than VREF. When VIN exceeds VREF and the difference is enough to discharge OUT+, the AND gate output remains high and the clock stops, as shown in Figure 6. 7. This stops the comparator and therefore, no longer draws current from the power supply. But for a strong-arm comparator,

the evaluation continues for the entire duration, as shown in Figure 6. 8. The nodes get pre-charged and discharged with every CLK cycle, unlike the input driven self-clocked comparator.

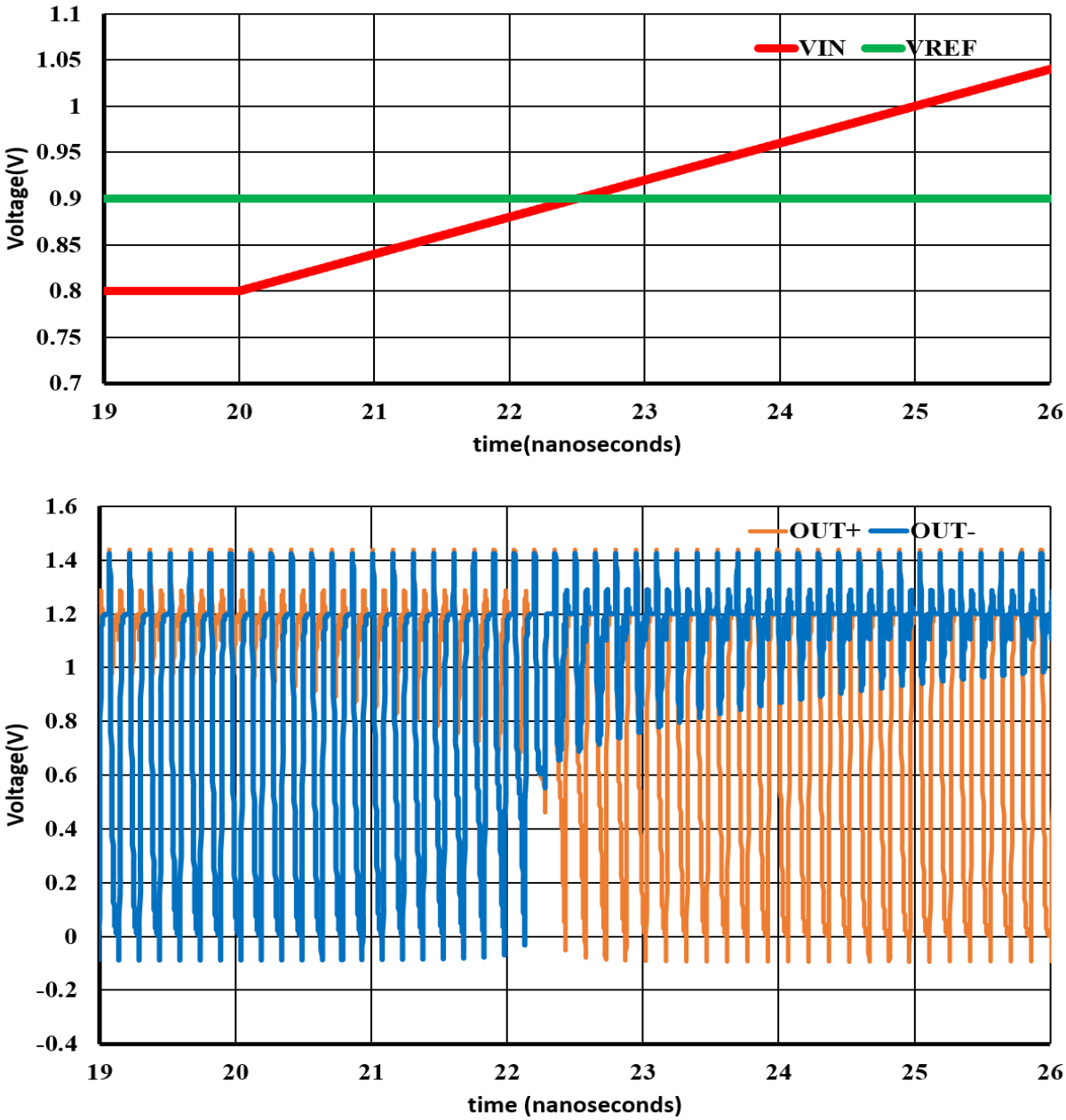

Figure 6. 7. Transient simulation results of Strong Arm Latch Comparator.

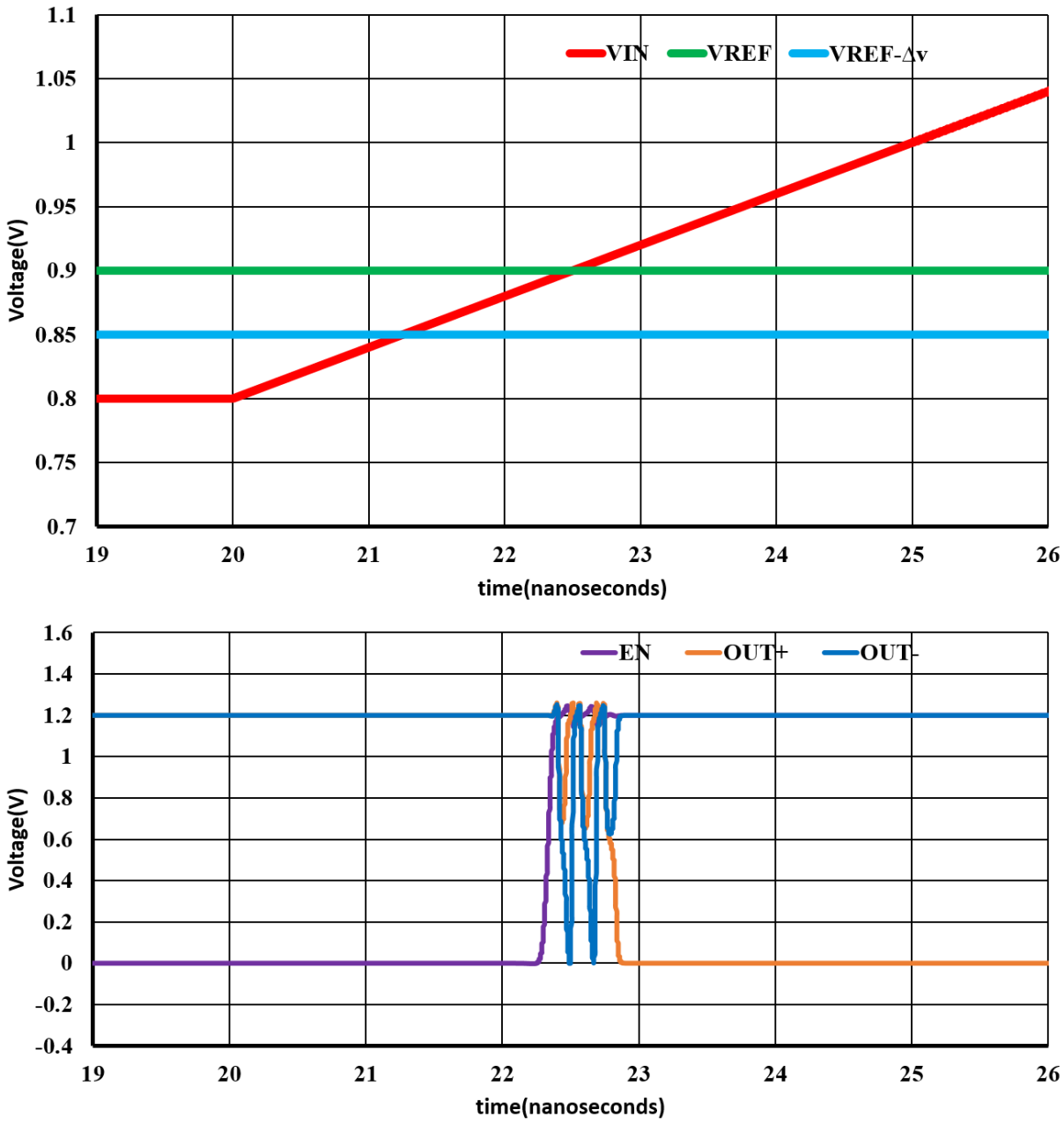

Figure 6. 8. Transient simulation results of Self-Clocked Comparator.

Figure 6. 9 shows the current drawn from the power supply, for the strong arm comparator and the self-clocked comparator using the same simulation testbench. For the self-clocked comparator, there is no current consumption until the EN signal triggers the comparator. Once the self-clock

starts operating and the comparator starts evaluating, the current drawn from the supply fluctuates depending on the charging and discharging of the nodes. It stops after the evaluation and doesn't start until it gets triggered by the EN signal again. For the strong-arm comparator, the current drawn from the power supply happens continuously for the entire duration, as shown in Figure 6. 9. For an ASIC with multiple comparators, this architecture will help in reducing the decoupling capacitance compared to a traditional dynamic comparator because of the relatively low number of switching transients from the power supply.

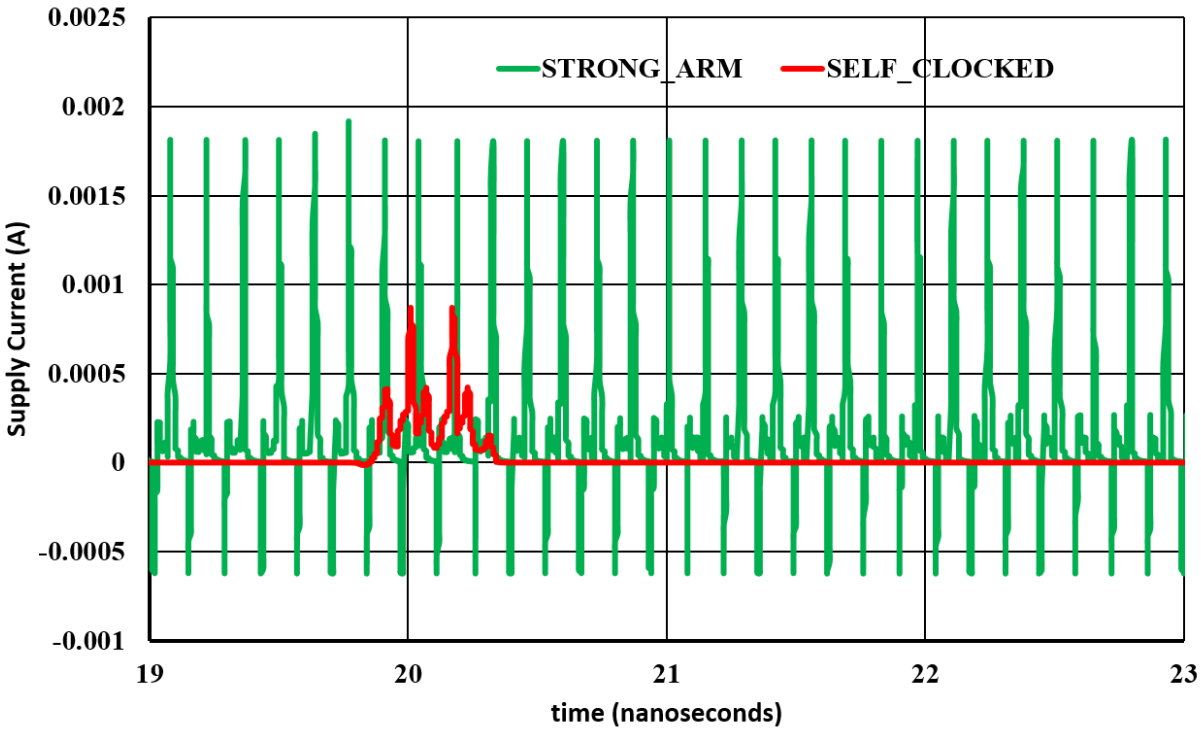

Figure 6. 9. Current drawn from power supply for SELF-CLOCKED and STRONG-ARM comparator.

6.3 COMPARATOR IMPLEMENTATION IN TOT

As explained before, every threshold in a ToT implementation needs its own dedicated comparator. Hence, the number of comparators scales linearly as the number of thresholds is increased for high resolution ToT systems. For a PET Imaging system with thousands of channels, the design of power efficient readout electronics depends a lot on the comparators, because comparators consume the majority of the energy consumption in any analog-to-digital converter based system. For example, 50-60 % of the energy consumption in a Successive approximation register (SAR) ADC comes from the comparator [59][60]. With technology scaling, this problem becomes more acute due to the low voltage operation which imposes stringent requirements on the quantization noise of the comparator. The input driven self-clocked comparator architecture, as described in the last section, consumes considerably less switching power compared to a traditional dynamic comparator, and hence can be used to reduce the energy consumption in the readout electronics for a PET Imaging system. Also, the implementation can be modified for a multiple threshold based ToT system to reduce the number of pre-amplifiers needed for all the comparators. This is shown in the Figure 6. 10 for the rising edge of the input signal.

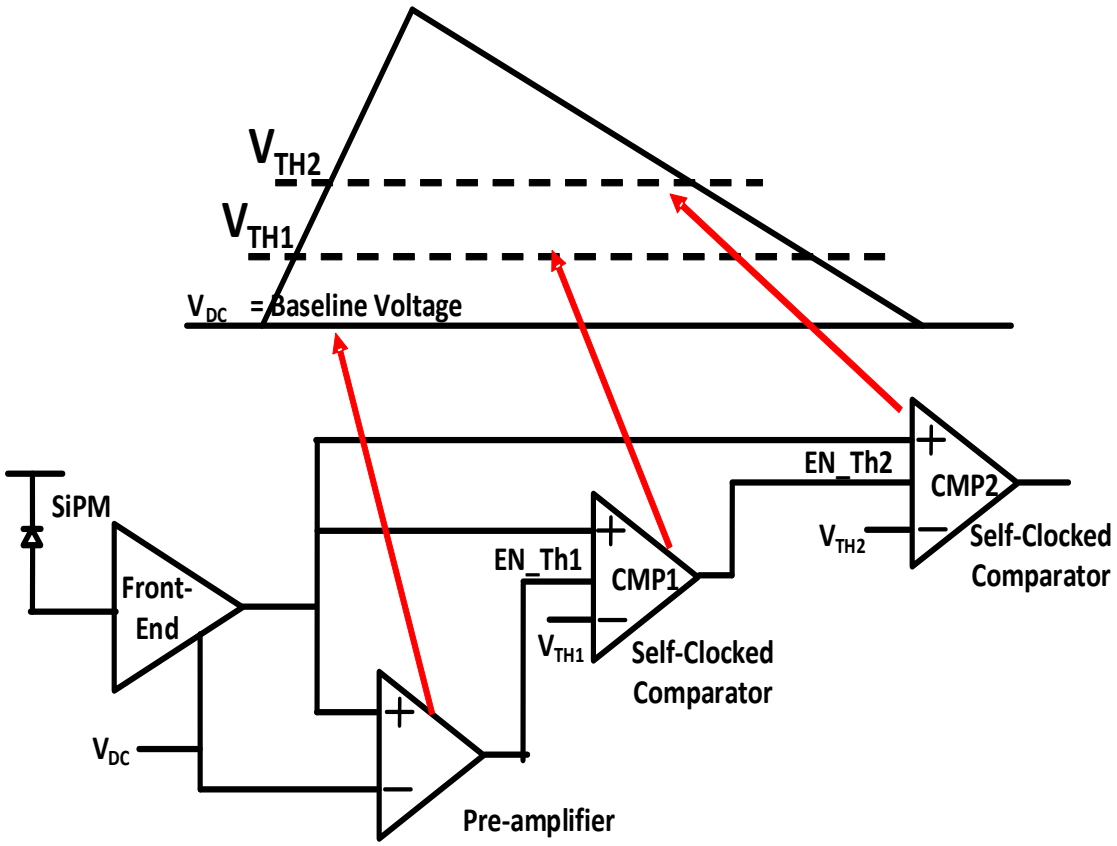

Figure 6. 10. Multi-threshold Comparator implementation for rising edge of the SiPM signal.

The preamplifier triggers the first comparator, as explained in the last section. The reference voltage of the preamplifier is the baseline voltage for the signal, which is the same as the common mode voltage of the front-end output. The two dynamic comparators have threshold voltages, VTH1 and VTH2 (VTH2>VTH1). The first comparator changes its output state when the signal becomes greater than VTH1, and this triggers the second comparator. Hence, the self-clocking mechanism of the second comparator is enabled only when the first comparator has finished its evaluation. As a result, the number of clock oscillations for the second comparator is reduced. This technique is extended for all the comparators, as shown in the Figure 6.11 and Figure 6.12 below. The second comparator enables the third comparator, and so on. For the falling edge, the first

comparator(VTH4) is enabled by the last comparator(VTH4) on the rising edge. As a result, the number of clock oscillations for this comparator is the highest among all the comparators, but still it is considerably less than a comparator which is on for the entire duration of the signal. The second comparator on the falling edge (VTH3) is triggered by the first comparator (VTH4) and so forth.

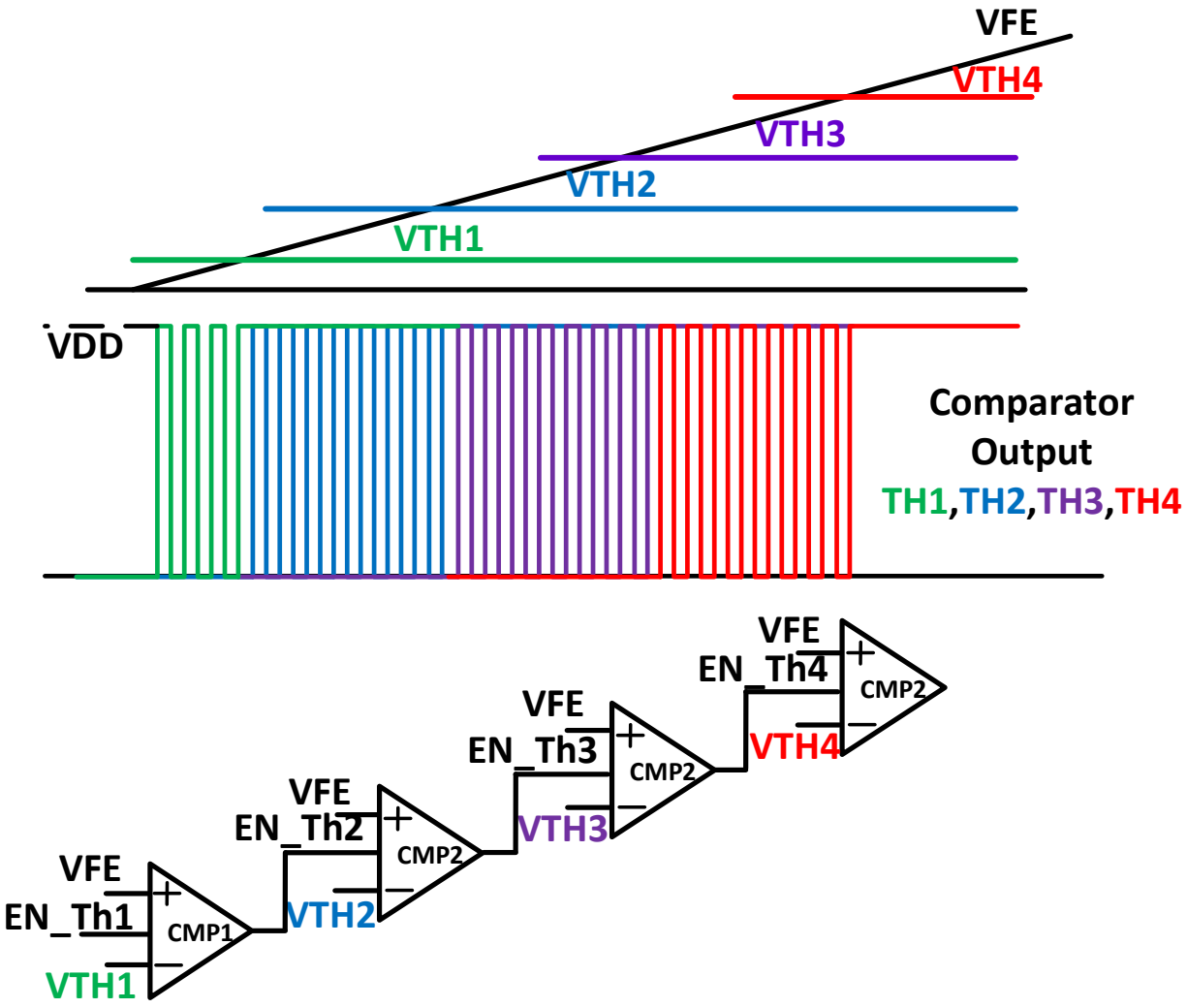

Figure 6.11. Multi-threshold Comparator implementation for the rising edge of the SiPM signal.

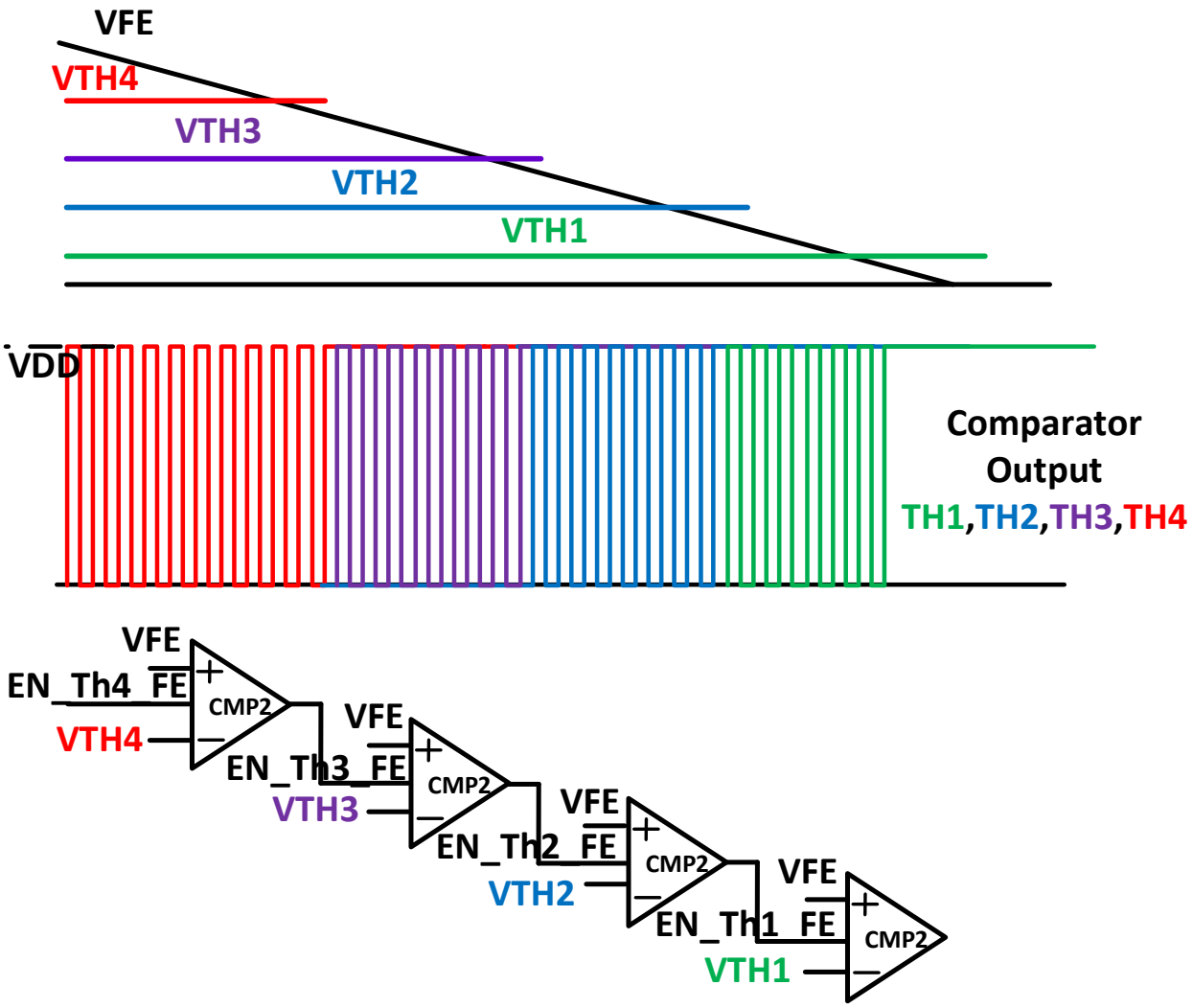

Figure 6.12. Multi-threshold Comparator implementation for the falling edge of the SiPM signal.

Figure 6. 13 shows the simulation result for the multiple thresholds. The test-bench consisted of the front-end amplifier, the pre-amplifier and the comparators. For the input signal, a pulse collected in the lab using a Broadcom SiPM detector was used. The baseline voltage is set at 800 mV, and the four threshold voltages are 850 mV, 900 mV, 950 mV and 1V. The front-end amplifier is operated from 2.5V power supply, while the comparators and the pre-amplifier are using 1.2V power supply.

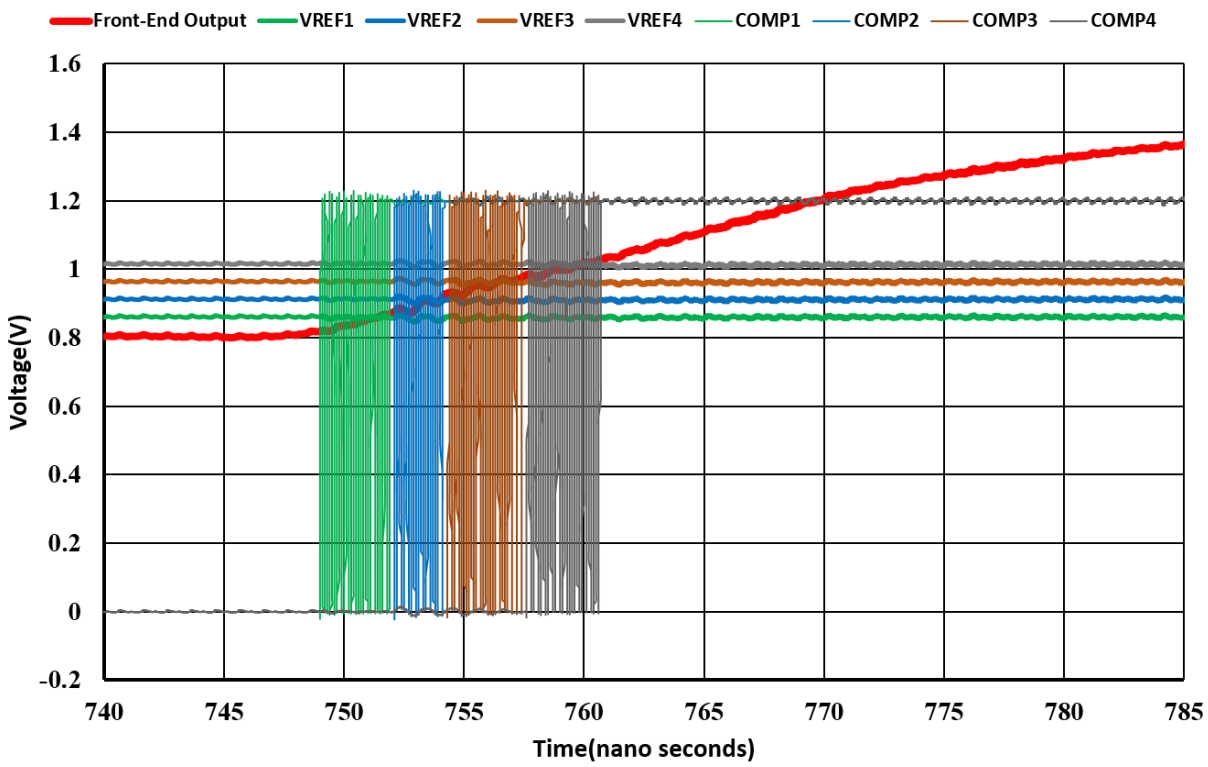

Figure 6. 13. Simulation result of the multi-threshold comparator operation with SiPM signal collected in the lab.

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Chapter 7. TIME-TO-DIGITAL CONVERTER(TDC)

The timing performance or accuracy of a PET detector is determined by its timing resolution. The timing (or temporal) resolution of the detector can be defined as its ability to record the minimum time difference between two subsequent photon events and differentiate between them efficiently[63]. In PET imaging systems, the timing resolution is usually measured for a pair of detectors and reported as the full width half maximum (FWHM) of the distribution of the Time of Flight (ToF) difference between the detectors. The timing resolution of modern conventional PET systems ranges from 2 ns to 10 ns, and commercial ToF-PET systems are known to achieve time resolution in the range of 500 ps to 700 ps [64] but a timing resolution of 390 ps (per crystal timing performance) has been reported with a prototype commercial system[65]. The timing resolution for a ToF-PET system depends on a number of factors but is predominately determined by the detector and readout electronics. In a ToT implementation, the Time-to-Digital Converter (TDC) plays a key role in determining the timing resolution of the system. This chapter will start with the description of the different TDC architectures and compare their performance. This will be followed by the design of TDC architecture used in this work. Finally, the system level implementation of the ToT architecture with the comparator, TDC and back-end memory will be presented.

7.1 BACKGROUND

TDC systems are widely used in digital storage oscilloscopes, logic analyzers, high-energy particle physics experiments and time-resolved imaging [66]. The simplest form of a TDC implementation consists of a high-frequency clock and a counter incremented at each clock edge.

In such a case, the resolution of the TDC is determined by the clock period, and the accuracy of the measurement which is determined by the stability of the clock and of the clock stopping method. A simple Phase-locked Loop (PLL) can guarantee a stable clock at high frequency and it is available as a standard cell in many CMOS processes. In this simple implementation a clock frequency $f_{clock}=1/\Delta t$ is needed for a resolution Δt. For example, Δt =100 picoseconds imply an f_{clock} = 10 GHz. While this frequency has been achieved in some recent CMOS radio-frequency circuits, its use and distribution across a large array of TDCs for thousands of PET imaging channels, poses several problems at various levels, particularly noise, crosstalk, and power dissipation. An alternative is the use of a TDC based on CMOS delay line [67]. Logic buffers can be used as the elementary delay unit and the resolution of the delay line is given by the buffer's gate delay. These TDCs require nothing more than a standard digital CMOS process and with the advancement of technology, their time resolution gets better despite the reduction in voltage supply. Most of the state-of-the-art TDCs are based on this buffer delay approach, but they employ different techniques to further improve the performance of the TDCs. The next sections will give a brief overview of these TDC architectures.

7.2 DIGITAL DELAY LINE TDC

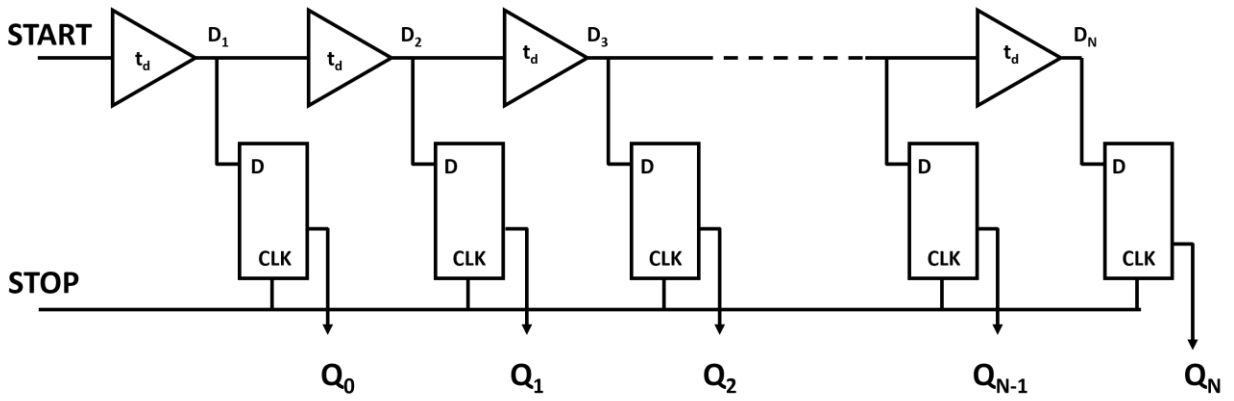

Figure 7.1. Delay line TDC.

Figure 7.1 shows the principle of a digital delay line based TDC. The goal is to measure the time interval between two events indicated by the signal edges: *start* and *stop*. *Start* and *stop* mark the beginning and end of the time interval, to be measured, respectively. *Start* propagates in a delay line composed of a series of buffers $D_{1.....N}$. The buffer outputs are the inputs of a series of D flip-flops, see Fig 7.1. The flip-flops are latched by the *stop* signal. The D flip-flops output form a thermometer code showing the distance between *start* and *stop* rising edges. The time resolution is determined by the buffer delay, which improves with modern deep-submicron CMOS processes. To stabilize the buffer delay against process, temperature and power supply variations, the buffers can be embedded inside a delay-locked loop (DLL) [68] or they can be implemented as a voltage-controlled delay cell.

Device mismatch leads to random variations in the delay elements, resulting in differential non-linearity (DNL) as well as integral non-linearity (INL). Also, meta-stability issues may arise in the delay lines in case the pulse propagation is stopped during the switching of a buffer. To increase the robustness of the TDC in the worst-case scenario, the individual buffer delays must

often be increased from their nominal minimum value, therefore reducing the intrinsic timing resolution.

7.3 VERNIER DELAY LINE TDC

The gate delay of the buffers, described in the last section, is limited by the speed of the fabrication technology in use. Hence, the resolution of a delay line based TDC is dependent on the technology. To improve the timing resolution, a Vernier delay line can be implemented using two delay lines with different delays [69][70][71][72][73]. The basic configuration is shown in Figure 7.2. The buffers in the upper chain have a delay of t1, which is greater than the delay of the buffers in the lower chain, t2. *Start* propagates in the upper delay chain, while *stop* propagates in the lower delay chain. The flip-flops are latched by the outputs of the buffers in the lower delay chain. The position '*n*' in the delay line at which *stop* catches up with the *start* signal, shows the time distance between *start* and *stop* as

$$d = n * t_R, t_R = t_1 - t_2$$

t_R is the time resolution of measurement and theoretically can be made very small, irrespective of the CMOS technology used. In practice, a very small t_R requires a long delay chain, which can lead to significant integral non-linearity (INL).

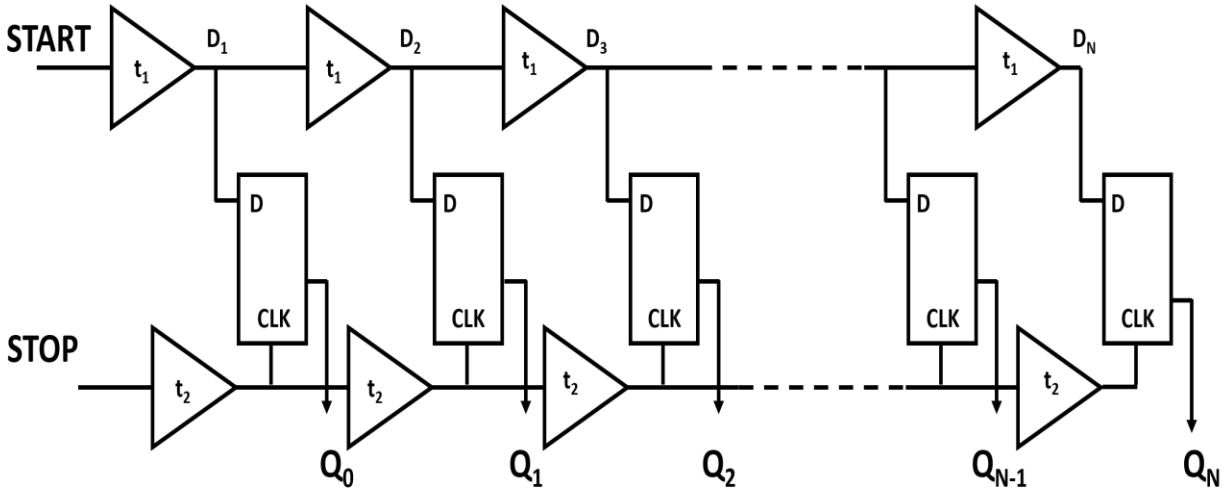

Figure 7.2. Vernier delay line TDC.

7.4 VERNIER OSCILLATOR TDC

The Vernier Oscillator TDC is based on two ring oscillators, using inverters, running at two different frequencies [69][70][71]. The time resolution of the TDC is determined by the difference in the oscillation frequencies. The oscillators are triggered by *start* and *stop* signals, as shown in the Figure 7.3. The oscillation periods, t_{start} and t_{stop}, are a function of the buffer delay and the number of inverter stages in the ring oscillator. For successful operation of the TDC, t_{start} is designed to be higher than t_{stop}. As a result, the phase of the *stop* oscillator gradually catches up with phase of the *start* oscillator, and the time it takes for this to happen is the measured time interval. As shown in the Fig 7.4, *Tin* is the time interval between *start* and *stop*. After N_1 cycles of t_{stop} and N_2 cycles of t_{start}, the two rising edges of the oscillators will be aligned and $Tin = N_2 X t_{start} - N_1 X t_{stop}$.

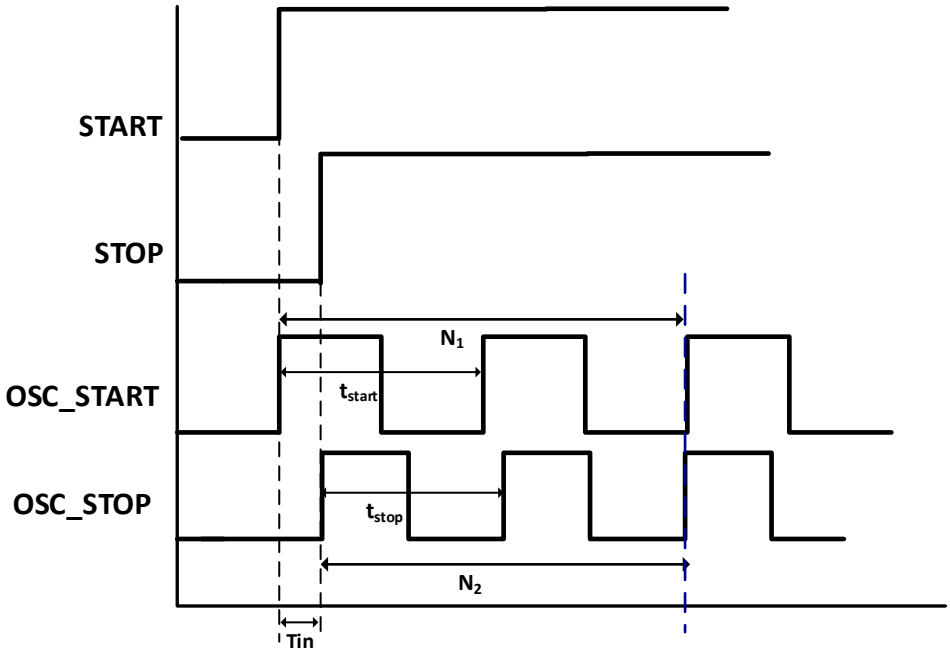

Figure 7.3. Vernier oscillator based TDC.

7.5 HYBRID TDC

The delay line TDCs can be used to measure a short time interval with high resolution. When used to measure a long period of time, the length of the delay line increases significantly. This results in degradation of INL, and hence the resolution needs to be longer than individual buffer delay. For the ring oscillator based vernier TDC, even though the number of delay stages required may be less than a delay based TDC, but still it would require a large number of counter bits to measure a long period of time. As a result, these TDCs are not optimal to be used in applications requiring measurement of wide time range with high resolution. The TDC architecture for these applications is a combination of a course quantizer using a clock edge counter and a fine quantizer using a delay line TDC [74][75][76]. This is shown in Figure 7.4. The time interval to be measured is divided into two parts - *tm*, which is measured by a counter clocked with a clock

period *tc*, and *td*, measured by a delay line TDC. The coarse time measurement is dependent on the clock frequency (*fc*) and the fine time measurement is related to the gate delay of the buffers.

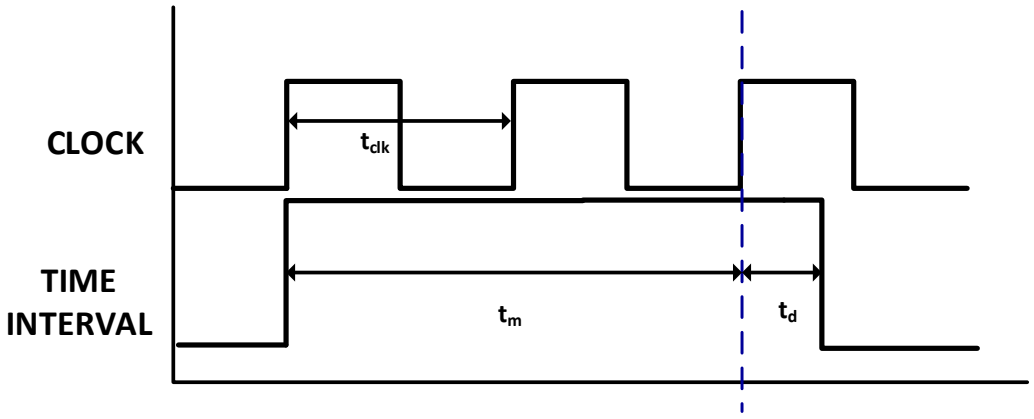

Figure 7.4. Hybrid TDC operation.

7.6 TDC ARCHITECTURE

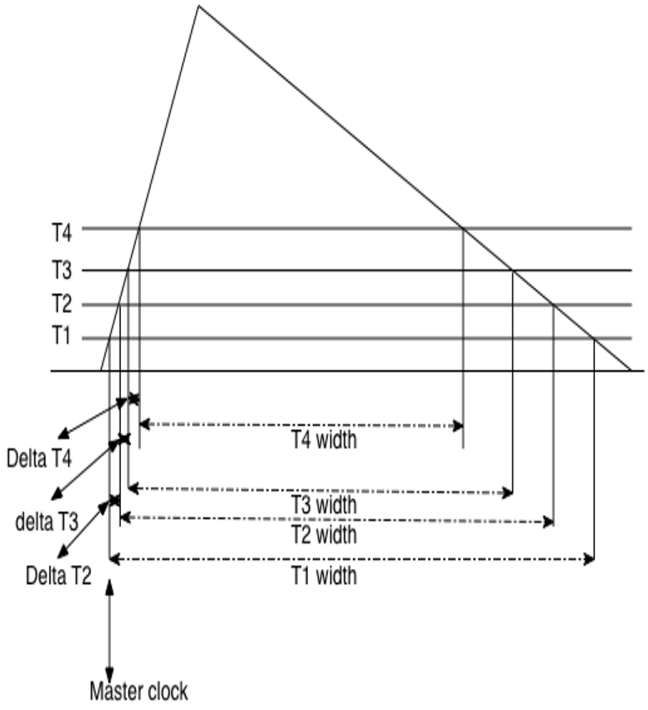

Figure 7.5. Time measurements for a single channel.

Before going into the details of the TDC architecture used in this work, it is important to list the time measurements to be performed in this system, as shown in Figure 7.5. For the four thresholds, the time-over-threshold (shown as widths, in the figure) are measured for the energy resolution of the system. For the timing resolution, the goal is to capture the time intervals between the thresholds and use those time intervals (shown as delta in the figure) to extrapolate the first electron timing point. To synchronize all these time measurements, a free running clock is used to time stamp the first threshold crossing on the rising edge. So, to summarize the time measurements in this system for thresholds Th1, Th2, Th3 and Th4 (see Figure 7.6) are as follows –

1. Time over Threshold (ToT) – $ToT_n = Th_nT2 – Th_nT1$
2. Delta Time – $dT_n = Th_nT1 – Th_{n-1}T1$
3. Delta Time for Th1, dT_1 = Clk_Edge – Th_1T1

The time resolution of the delta dT_n and time widths ToT_n are different. For the ToTs, the maximum width is of the order of 100 ns, so a time resolution of the order of 1 ns is enough to capture the energy information. But the requirement for the delta times is more stringent. This is because the rise time of the SiPM signals are of the order of few nanoseconds. As a result, the timing resolution needed is of the order of tens of picoseconds.

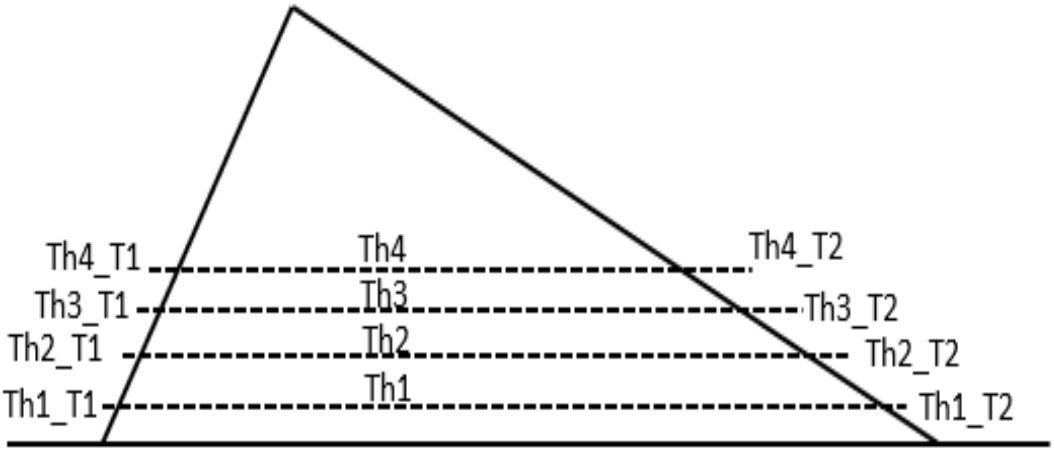

Figure 7.6. Time Stamps for individual thresholds.

Two separate TDCs are used to measure the ToTs and the delta time intervals. The Time-over-Threshold (ToT) measurement scheme is shown in Figure 7.7. The counter has a free running clock with a frequency of 1 GHz, giving a resolution of 1 ns. The 8-bit counter is enabled by the output of the comparator. It is reset by the output of the baseline preamplifier, as explained in the last chapter on the comparator design. With the free running clock, the resolution of the ToT measurement can be improved by increasing the clock frequency. An H-bridge clock distribution scheme has been used to transmit the clock signal across all the channels on the chip. The clock buffers have been optimally designed to be extremely power efficient for high frequencies. To prevent kickback noise paths from the clock network to other parts of the channel, specially the comparator, bypass capacitors were used to provide a low impedance for the switching transients from the clock signal.

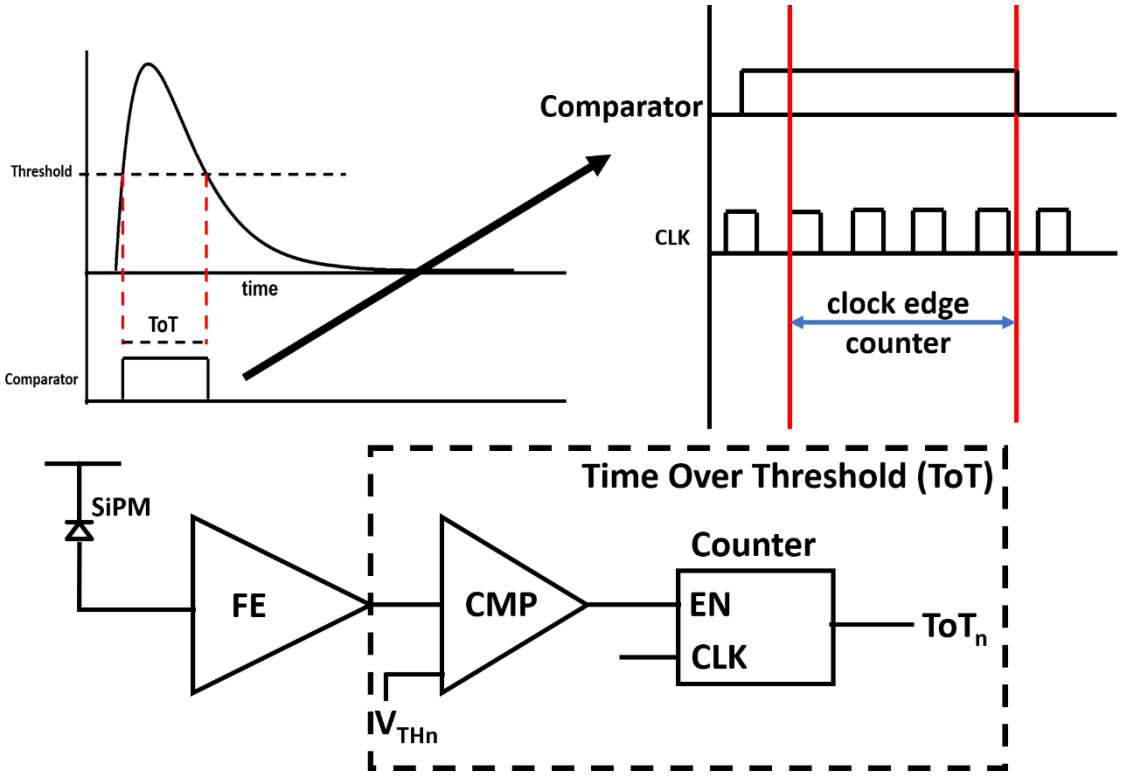

Figure 7.7. Time over threshold measurement method.

As mentioned before, the timing resolution required for the delta time measurements is on the order of tens of picoseconds. This can be achieved by using a free-running clock with a frequency greater than 10 GHz. The main drawback of this technique is the high clock frequency required and the excessive power consumption for clock distribution, scaling quadratically with the supply voltage and linearly with the clock frequency and the load capacitance. The TDC architecture for the delta time measurements was designed keeping the above considerations in mind. It consists of a two-step interpolator using a ring oscillator based TDC, as shown in Figure 7.8. The loop starts oscillating when the event starts (START becomes high). The counter starts incrementing with every rising edge of the oscillating output of the last inverter element. It stops when the event ends (STOP becomes high), thus providing a course interpolation of the time interval. At the same time the rising edge of the STOP signal latches the state of the delay line, thus generating a

thermometer code showing the distance between the last oscillation cycle counted by the counter and the STOP rising edge. This quantization has a resolution given by the delay across the inverter, resulting in a finer interpolation. The ring oscillator has a 16 element delay line, in addition to the NAND gate. A delay line consisting of inverters guarantees the fastest propagation speed and resolution. Using TSMC 65 nm process, the delay across each inverter is designed to be around 10 ps. With 17 delay stages, the time period of oscillation is around 340 ps, resulting in a clock frequency of 3 GHz. The counter has 4 bits, so it has a range of (15x340psec=) 5.1 ns, therefore making sure it covers the time intervals on the rising edge of the SiPM pulses. The timing resolution of the TDC is given by the inverter delay, which is going to be degraded by the mismatch between the inverters. This is not going to be an issue for this system, because the START and STOP signals are generated by the self-oscillating clock, described in the last chapter, and the clock frequency for that is around 7 GHz. Even then, significant attention was placed on the layout of the delay chain. Dummy cells were used to guarantee all the elements have the same load and the transistors are all placed in the same direction. In addition, the power supply grid was carefully designed in order to minimize IR drops, while *di/dt* effects were minimized by the use of decoupling capacitance for individual inverter elements. The TDC output is converted into a binary code using a thermometer to binary encoder. The TDC, including the 4-bit counter was reset using the baseline pre-amplifier (explained in the last chapter), thus making it ready for computation every single time there is a valid SiPM event in the Imaging system.

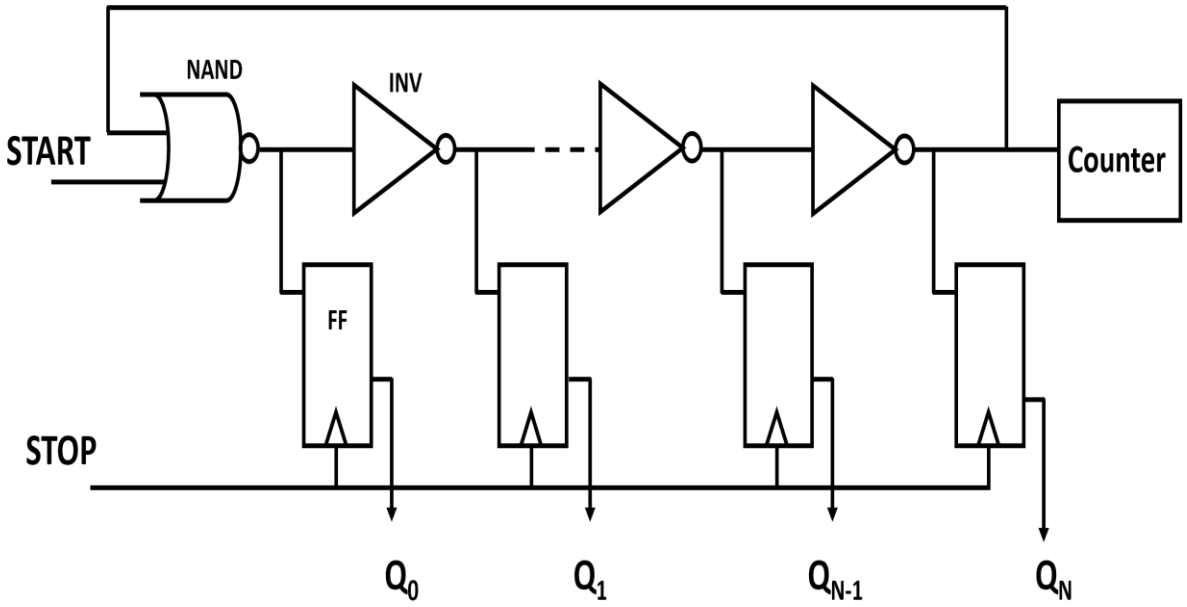

Figure 7.8. Ring Oscillator based TDC.

The TDC delta time measurement has two different implementations, depending on the inputs. As explained before, for the first threshold V_{TH1}, the time interval is measured with respect to the free running clock signal. This helps to synchronize the measured time intervals with the free running clock. As shown in Figure 7.9, the flip-flop samples the first clock edge after the comparator changes its output state, and feeds it as the STOP signal for the TDC. For the other thresholds, the fine time interval is measured between the comparator outputs of V_{THN} and V_{THN-1}, as shown in Figure 7.10. The output digital codes are converted into a serial bit stream with a data rate of 5 Mbits/sec using a latch based serializer. The serializer has two external clock signals acting as read and write enables, respectively.

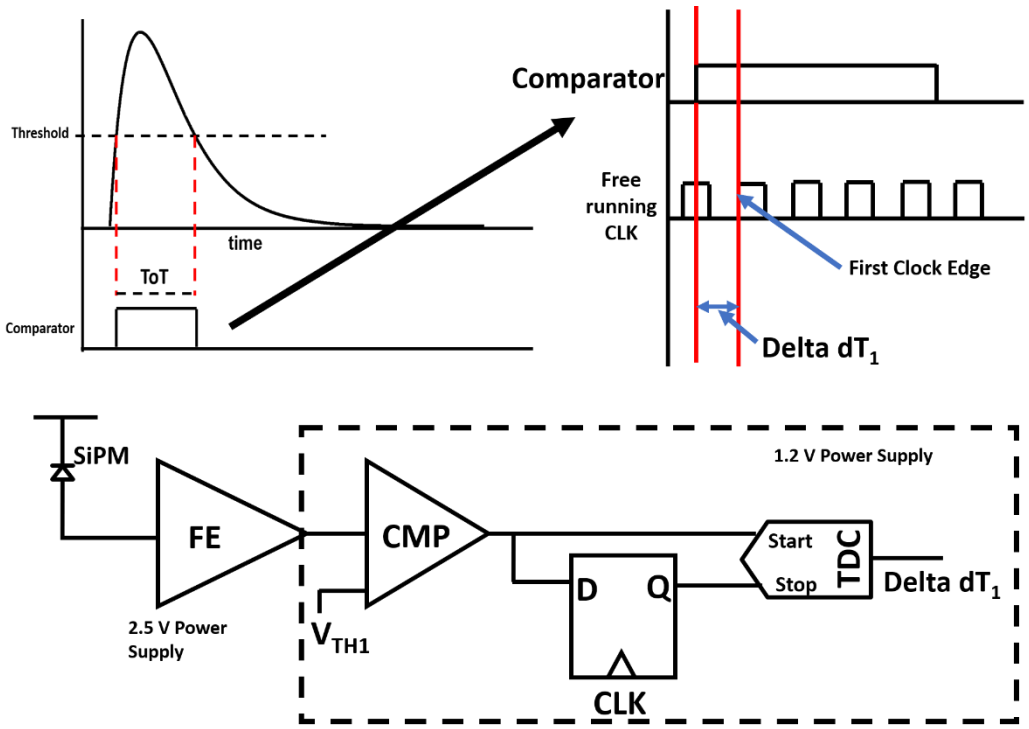

Figure 7.9. Delta time interval for lowest threshold on the rising edge.

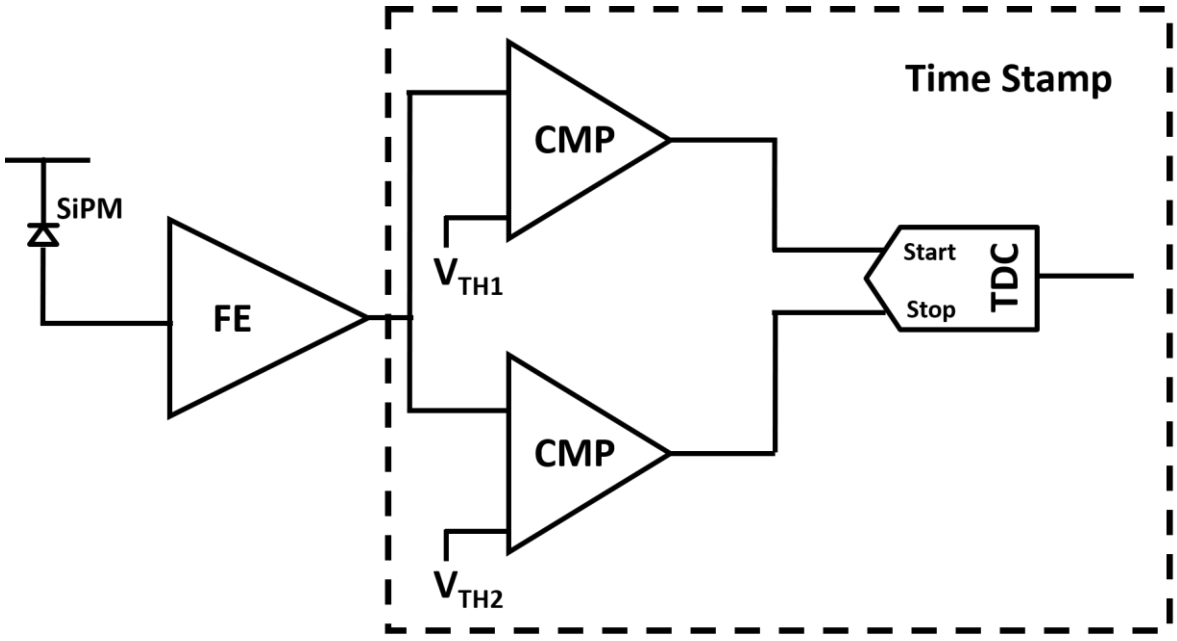

Figure 7.10. Delta time interval for higher thresholds on the rising edge.

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Chapter 8. MEASUREMENTS AND SIMULATION RESULTS

To validate the different ideas and concepts presented in this work, three different versions of the interface ASIC were fabricated. All of these chips were characterized using different experiments with SiPM devices. This chapter will discuss the findings and results of those experiments as well as present some simulation results for the final interface version this chip which has just arrived from the fabrication house, as of the writing of this thesis.

8.1 ROW COLUMN SUMMING BASED READOUT ASIC

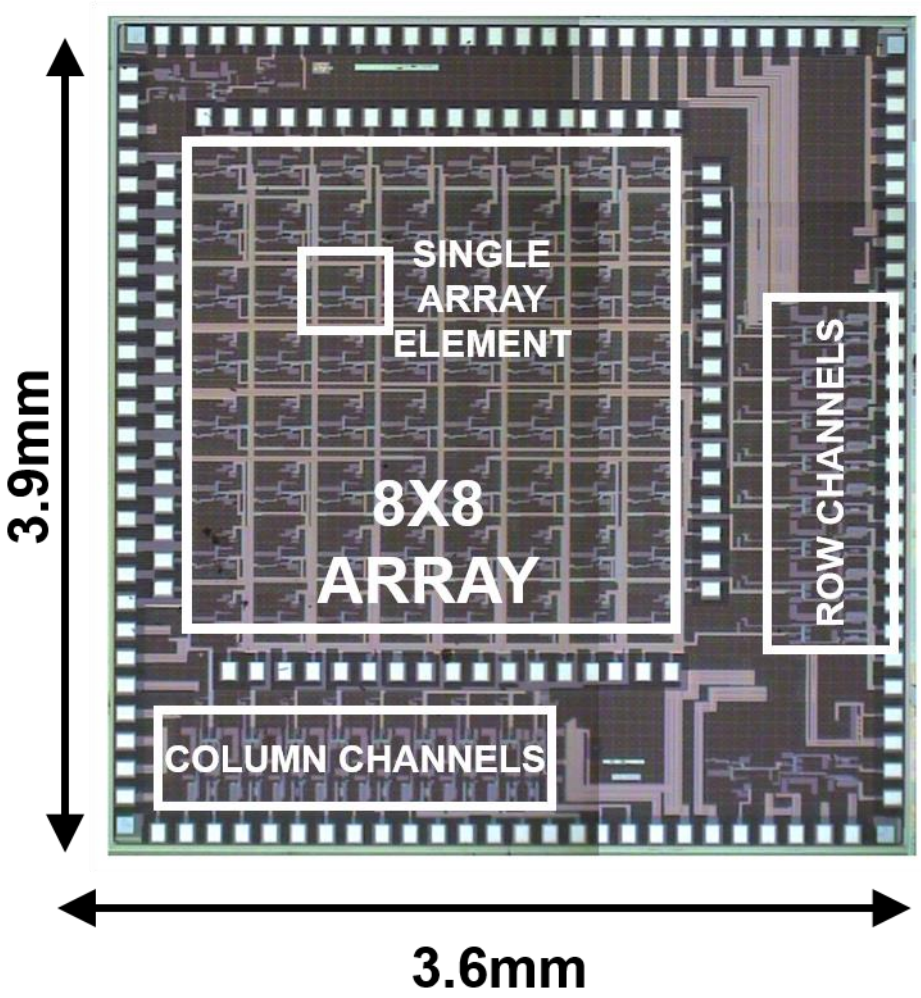

Figure 8. 1. ASIC 1st version Die Photo.

The first version of the readout chip was fabricated in a 130nm 6-layer metal stack STMicroelectronics HCMOS9GP process, see Figure 8. 1. The chip dimensions are 3.9mm x 3.6mm. It has 64 channels in an 8x8 array. The row column summing architecture is used to reduce the number of output channels to 16 (8 rows and 8 columns) and one timing channel. The chip was verified on a detector test bench with a SiPM array as well as with a BNC (Berkeley Nucleonics Corporation) Fast Tail Pulse Generator, Figure 8. 2. The inset shows the system response to both the pulse generator and the SiPM array.

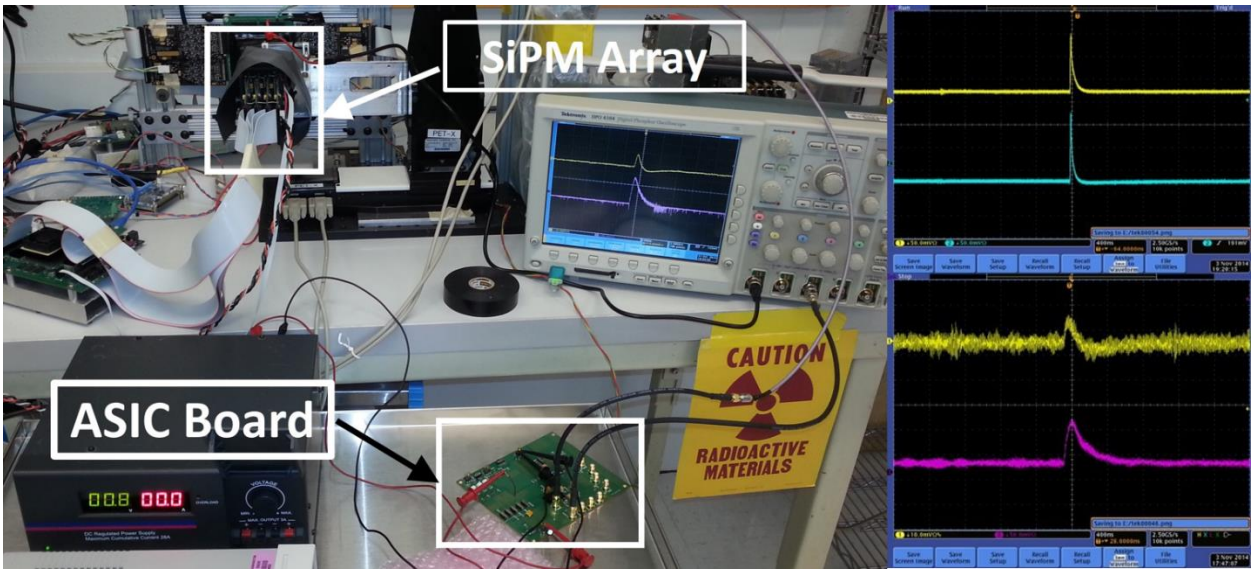

Figure 8. 2. Left - Test board mounted on a detector test bench, Right - (top) Data from pulse generator, Right - (bottom) data from the detector test bench.

Measurement data was acquired using the pulse generator to verify the threshold detection circuitry performance, shown in Figure 8. 3. When the threshold current is zero, the output of the channel maintains the energy as well as the timing information of the input pulse. However, as the threshold current level is increased to 1.2 mA and 1.5mA, the channel output becomes disabled, thus validating the functionality of the current comparator circuit. The negative spike for the 1.2

mA current threshold is due to the switching transients generated by the current comparator. The switching transients coupled with the propagation delay across the current comparator can lead to clipping on the rising edge of the pulse.

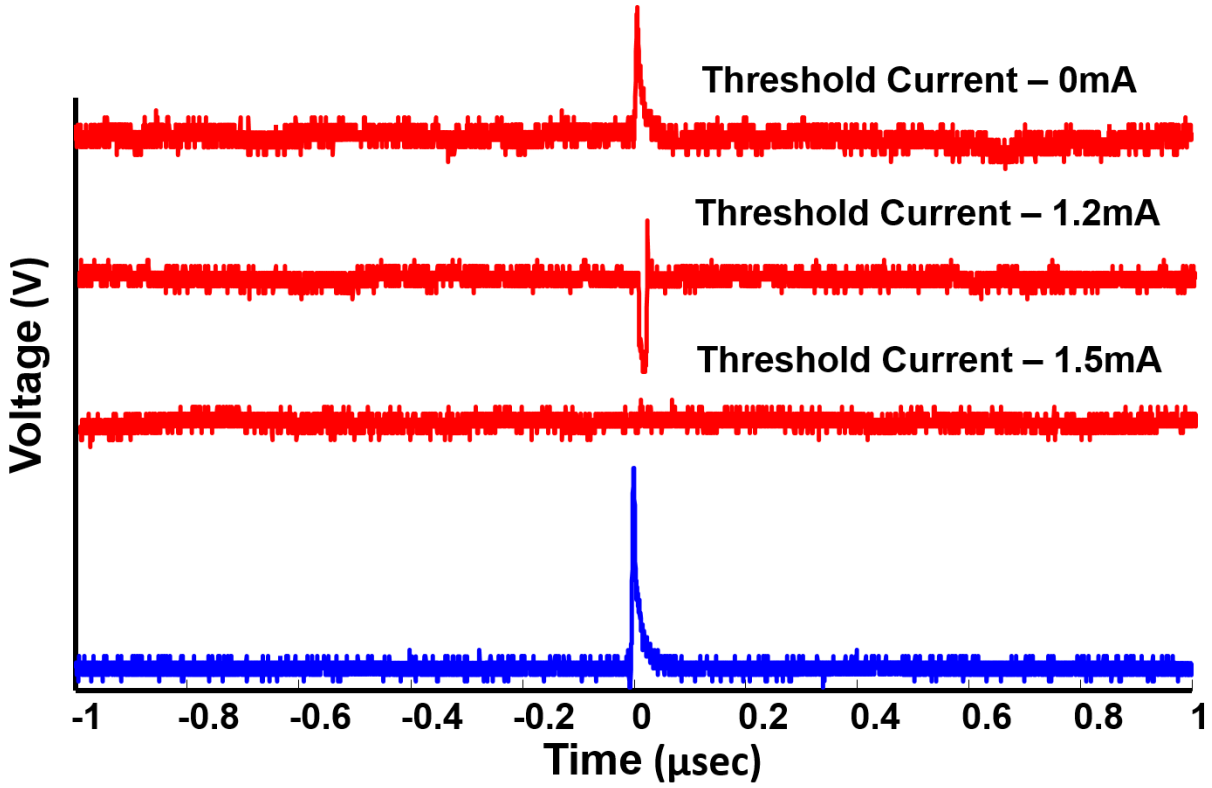

Figure 8. 3. Threshold Detection using different reference current levels (Blue- Input, Red – Output).

To investigate this, the clipping was noted at different threshold current levels, Figure 8. 4. The offset at a zero threshold level, 0.4ns, is the propagation delay through the channel alone. The minimum propagation delay measured across the current comparator is (0.7 -0.4 =) 0.3ns for a threshold current of 100 µA.

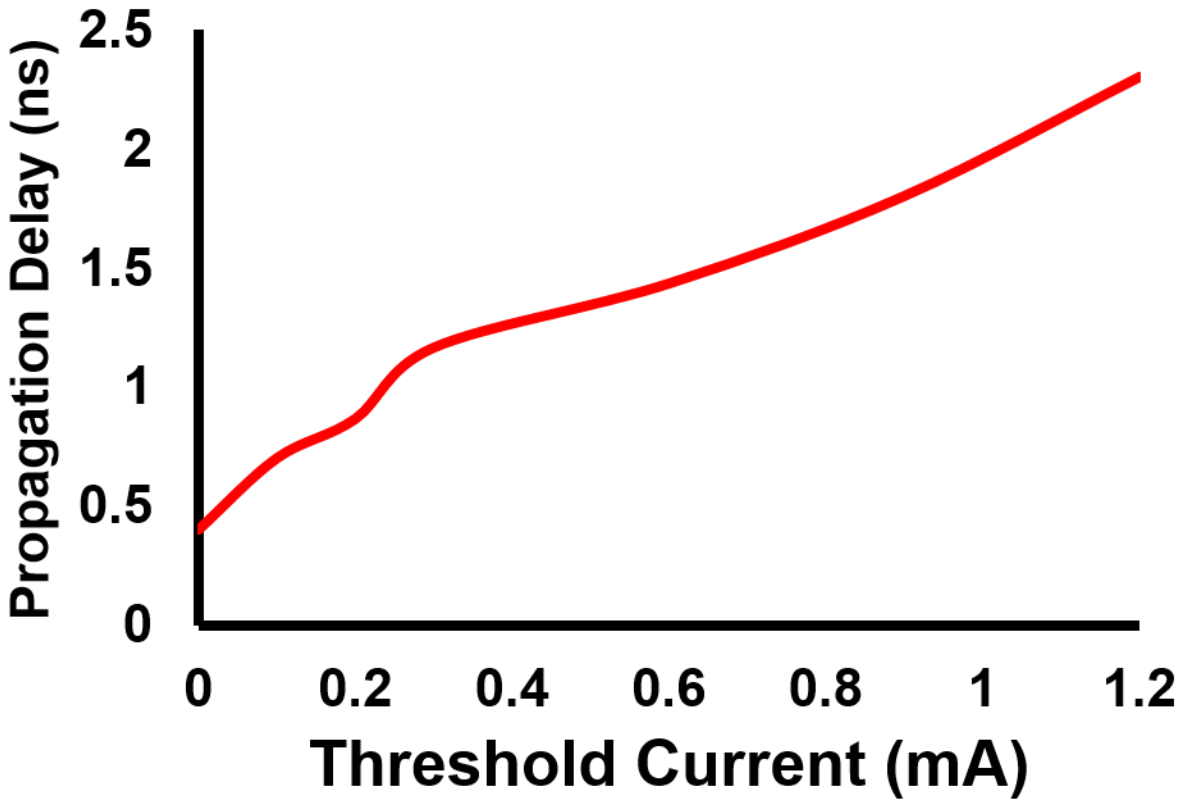

Figure 8. 4. Propagation Delay and clipping of rising edge.

8.2 Regulated Cascode based Readout ASIC

The die photo of the second version of the readout chip is shown in Figure 8. 5. For fabrication, TSMC 65nm 9-layer metal stack Low Power process has been used. With an area of 2mm x 2mm, it has 32 channels arranged in 4 quadrants. Each individual channel has an active area of 0.0375 mm^2. The bias circuits generate a set of currents to bias the individual channels. The bypass capacitors prevent high frequency noise from getting coupled into the active circuits.

A N5247APNA-X Network Analyzer is used to measure S-parameters of the channel. The input impedance derived from the real part of the S11 measurement is 5 ohms at low frequencies. At higher frequencies, the gain from the shunt feedback loop decreases, and hence the input

impedance increases to 14 ohms at 500 MHz, Figure 8. 6. The frequency response of the channel was measured using a spectrum analyzer. With the buffers enabled the bandwidth of the channel was 150 MHz with a transimpedance gain of 60 dBΩ.

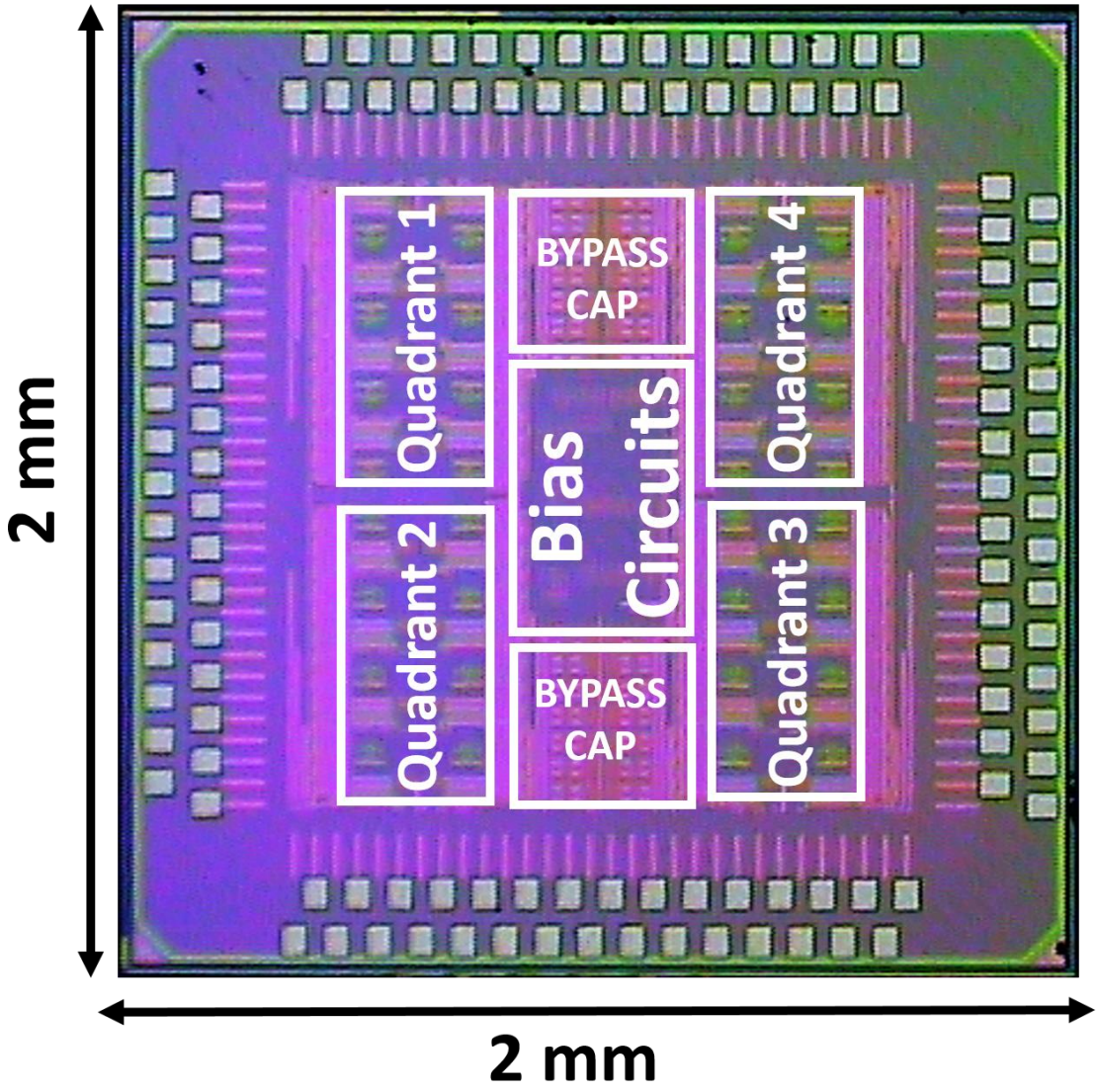

Figure 8. 5. Die photo of the 2nd version of the ASIC.

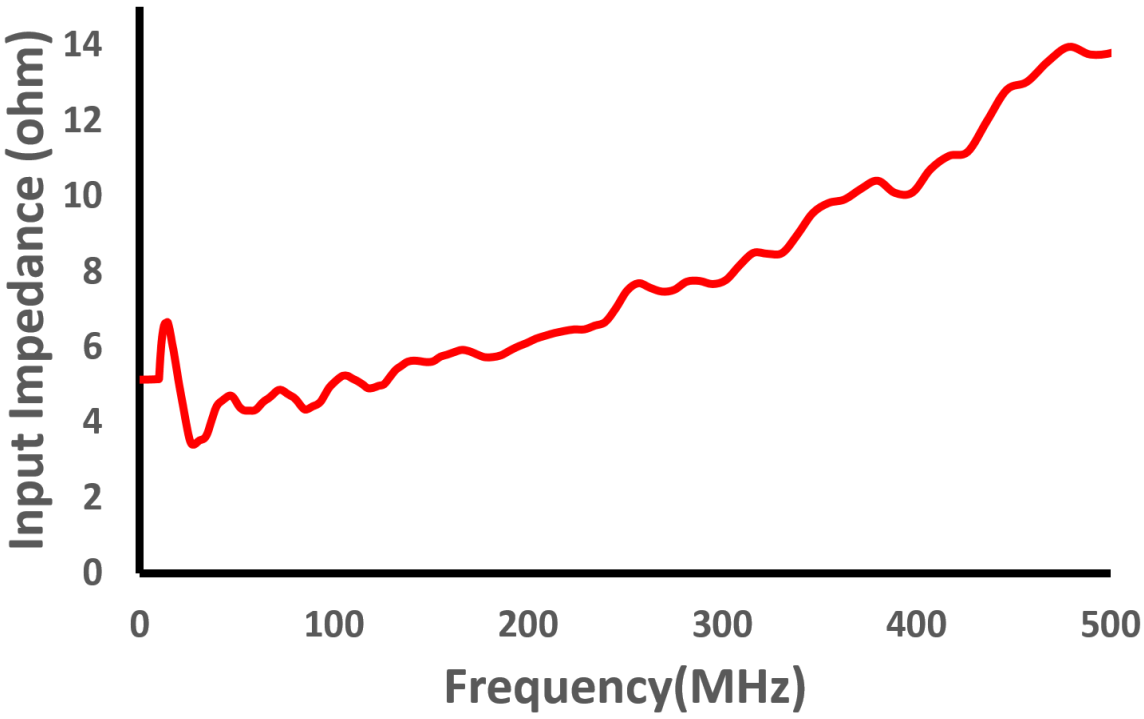

Figure 8. 6. Measured Input Impedance of the Front-End Interface.

To evaluate the performance of the chip with a SiPM device, experiments on energy resolution are performed with the setup shown in Figure 8. 7. The radiation source used is 511 keV Ge-68. The chip was mounted on a test board and interfaced with a Hamamatsu device. The FPGA is used to program the on-chip shift register for gain tuning each channel individually. To measure the energy resolution, a set of 1200 pulses was collected for individual channels. MATLAB is used to calculate the energy resolution from the collected data. Figure 8. 8 shows the energy histogram for one channel. The measured FWHM energy resolution is 12.39 %. The experiment was repeated for other channels, and the energy resolution was found to be ~11-13 %.

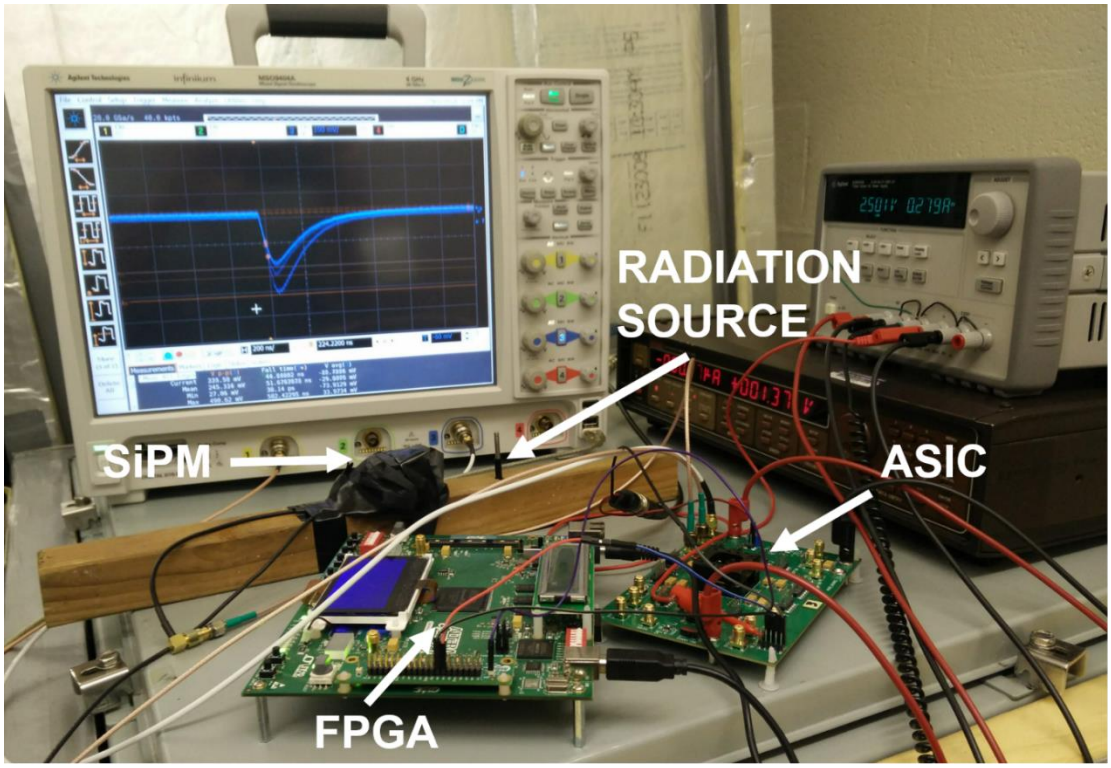

Figure 8. 7. Test board mounted on a detector test bench.

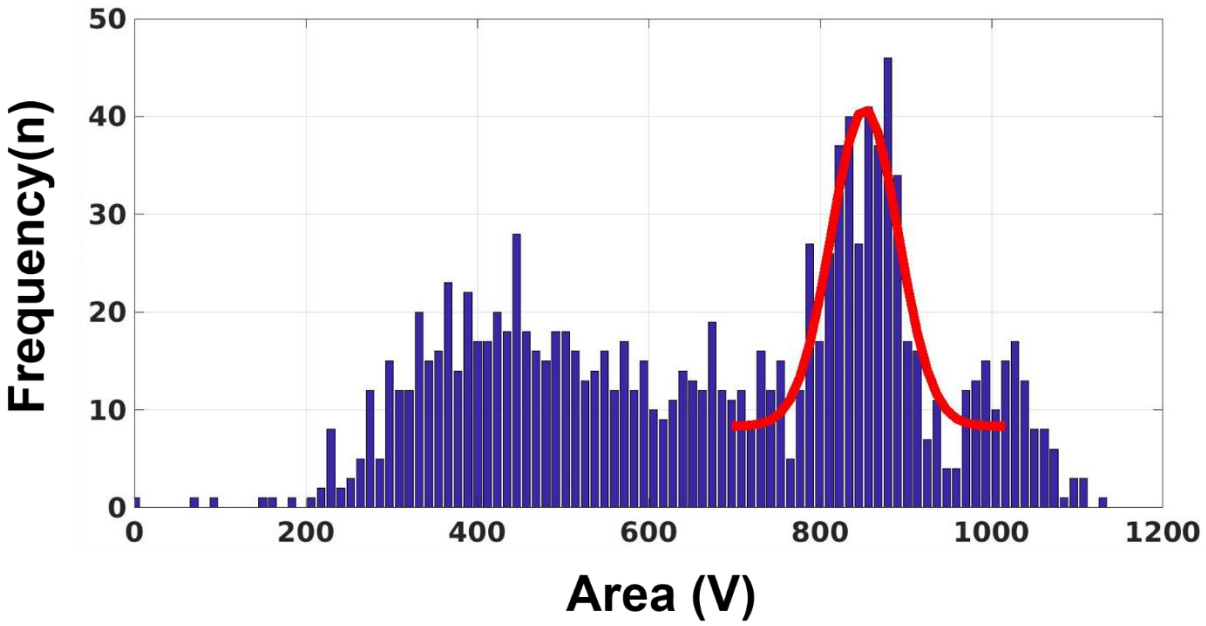

Figure 8. 8. Energy Histogram for a single channel.

8.3 TIME-OVER-THRESHOLD BASED READOUT ASIC

The die photo of the third version of the readout chip with the Time-over-Threshold(ToT) digital acquisition system is shown in Figure 8. 9. For fabrication, TSMC 65nm 9-layer metal stack Low Power process has been used. With an area of 2mm x 2mm, it has 16 channels arranged in 4 quadrants. The channel architecture comprises of the front-end interface, input driven self-clocked comparator and the time-to-digital converter (TDC). As explained before, the front-end interface architecture is the same as that of the second version of the ASIC.

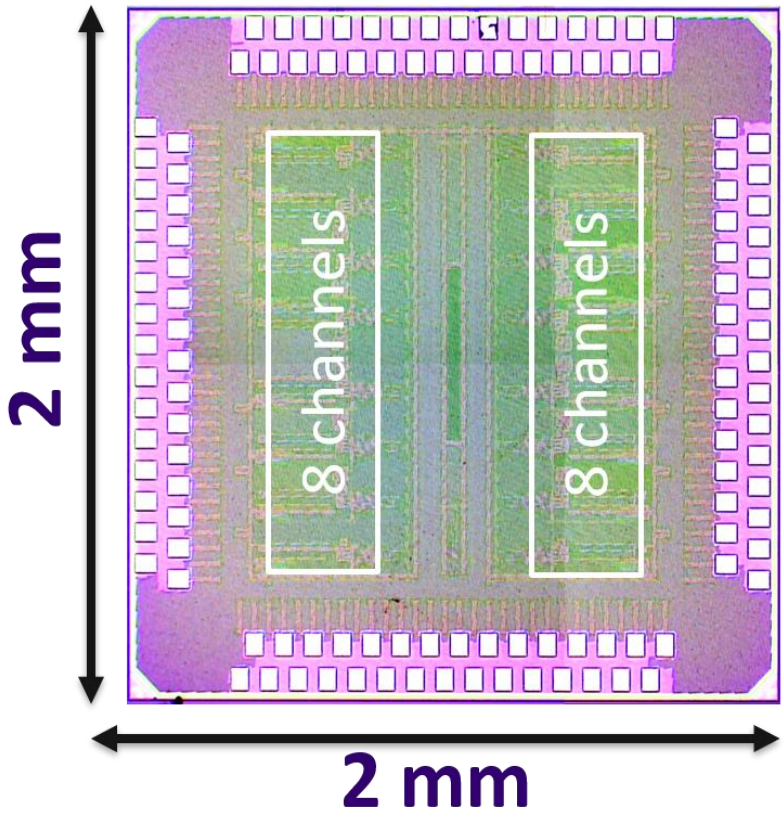

Figure 8. 9. Die photo of the 3rd version of the ASIC.

To validate the system architecture, a pulse generation model for SiPMs was used to feed signals at the input of the channel. The thresholds for the channel was controlled using a digital-to-analog converter(DAC). The output ToT values from the TDC were then collected to generate

a histogram for the measured energy values. Figure 8. 10 shows the ToT distribution when the threshold voltage is selected at 25 % of the maximum amplitude. The distribution has a mean of 80.83 ns and a standard deviation of 7.138 ns. This results in a FWHM resolution of 20. 79 %. Figure 8. 11 shows the ToT distribution when the threshold voltage is selected at 30 % of the maximum amplitude. This generates a FWHM resolution of 22. 61 %.

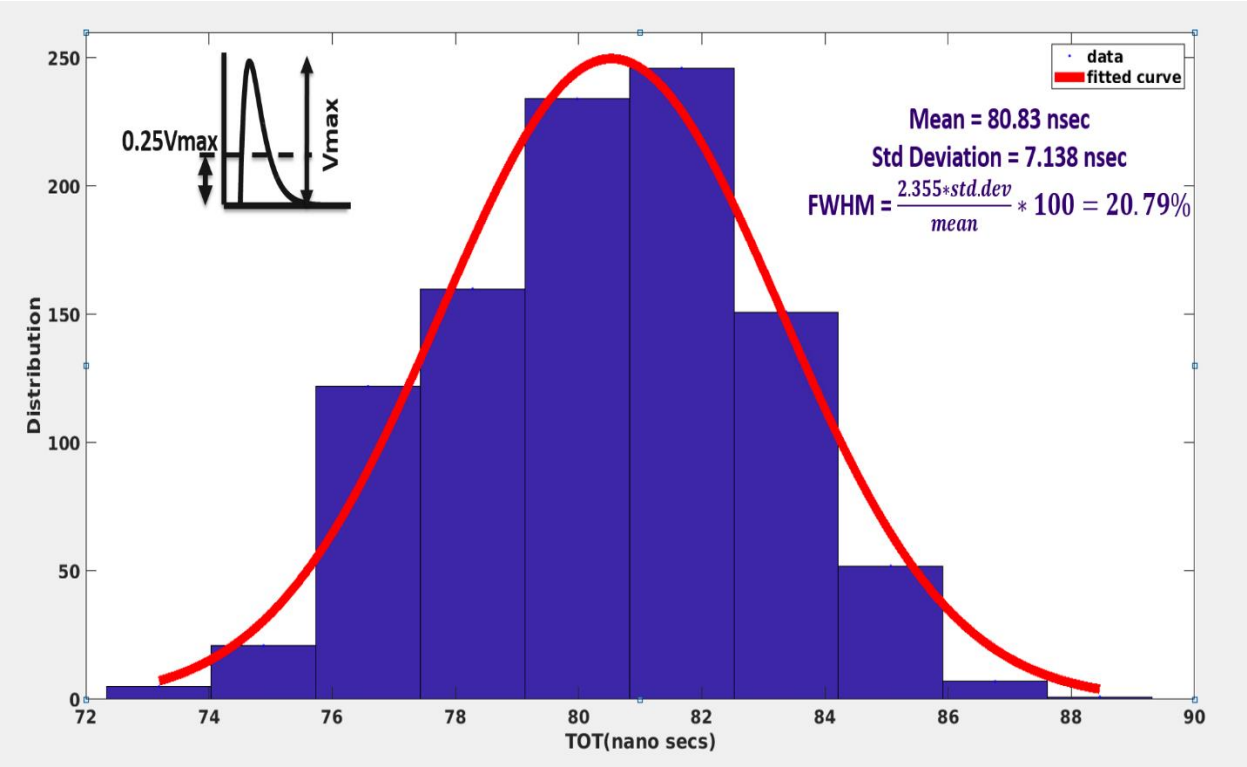

Figure 8. 10. Time over Threshold distribution at 25% of the maximum SiPM pulse amplitude.

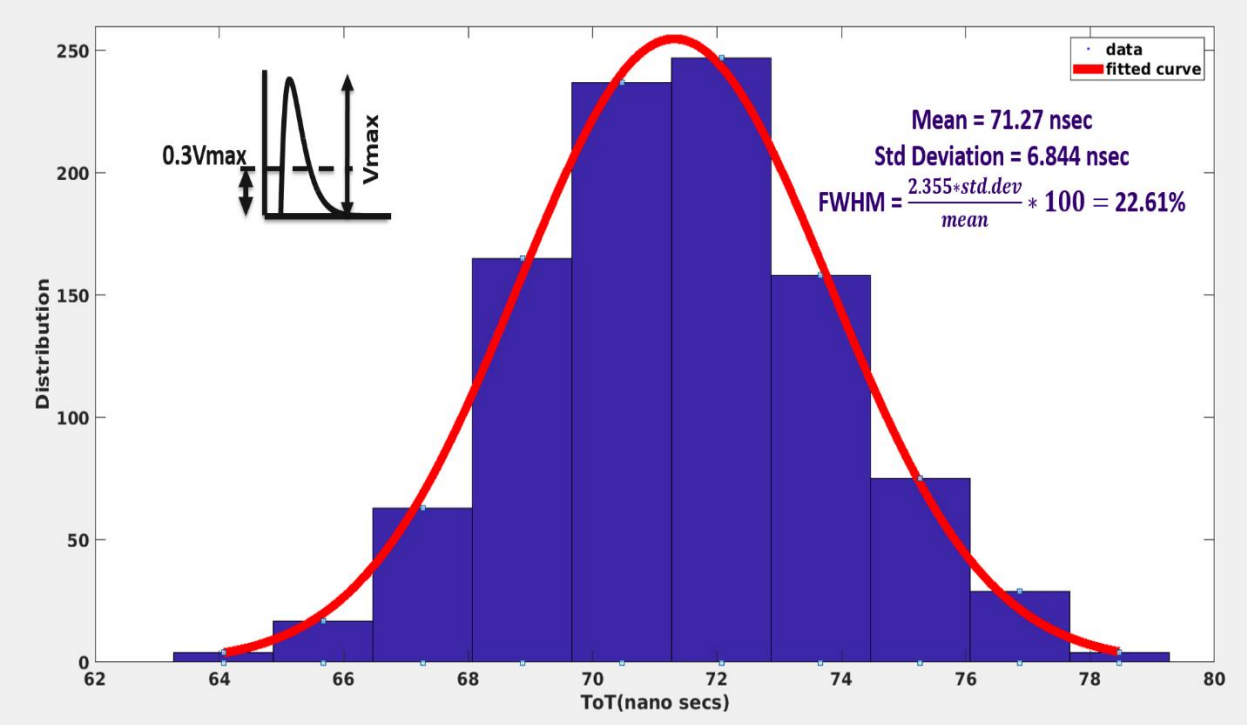

Figure 8. 11. Time over Threshold distribution at 30% of the maximum SiPM pulse amplitude.

To evaluate the timing resolution of the system, a distribution of the coincidental time stamps for the SiPM pulses was simulated. First coincidental data sets were created from every pair of pulses. Then, the time of arrival of each of those two pulses were estimated by extrapolating the time stamps calculated by the TDC. The time difference between those arrival times is the coincidence timing, and the distribution of the coincidence timings for all the data sets gives the timing resolution of the channel, shown in Figure 8. 12.

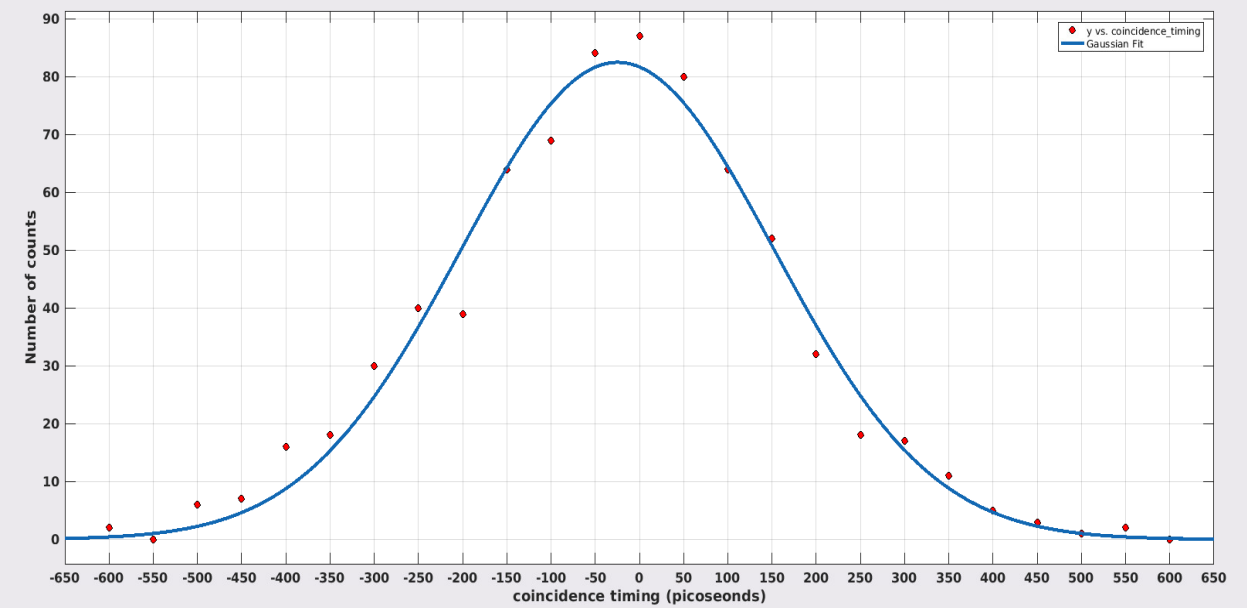

Figure 8. 12. Coincidence Timing Resolution.

The chip was verified on a detector test bench with a BNC (Berkeley Nucleonics Corporation) Fast Tail Pulse Generator. Figure 8.13 shows the consecutive input signals from the pulse generator and the comparator output for the lowest threshold voltage. The measured Time-over-Threshold from the comparator output is 570 ns.

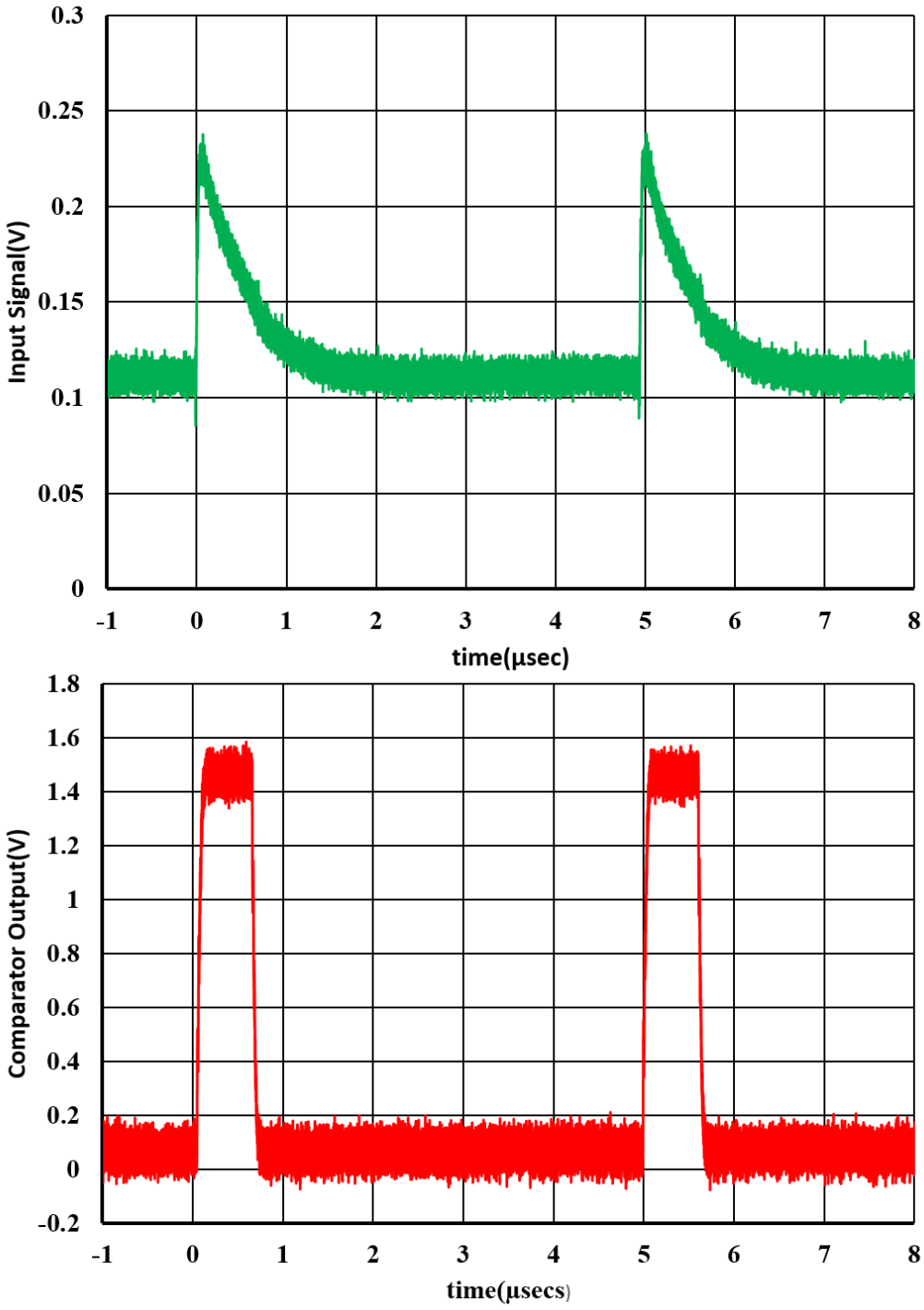

Figure 8.13. Input signal from the pulse generator(top) and the comparator output(bottom).

Chapter 9. CONCLUSIONS AND FUTURE WORK

Until a few years ago, ASIC implementations of readout electronics for SiPM diodes were mostly focused on optimizing the front-end interface. But, the amount of data produced in the modern PET scanners is increasing considerably, as a result of the increased density of the detector arrays and the continuous push towards improved timing resolution for Time-of-Flight measurement. Conventional digitizing techniques are not suited for such large scale operation because of the high power budget. Ultra-low power readout electronics for these systems have been a topic of prevailing research over the last few years. Towards that goal, the ideas implemented in this work using Multi-Time over Threshold based data acquisition can be a major landmark for PET Imaging systems. The Time-over-threshold (ToT) method directly converts pulse height into pulse width at an early stage of the front-end circuit. A comparator is used to determine whether the signal is above a pre-determined threshold. The comparator's output remains high during this duration and this information is digitized using a Time-to-Digital Converter (TDC). This method helps to simplify system architecture, since it does not need complicated analog-to-digital converters. This work presents the design of a novel Multi-threshold Time-over-Threshold based readout ASIC dedicated to PET imaging systems which facilitates the integration of the SiPM with the front-end electronics. The implemented digitizing methodology using Time-over-Threshold helps in simplifying the channel architecture for SiPM readout electronics. A low input impedance high bandwidth current amplifier interfaces with the photo diodes in the front-end. The front-end amplifier, based on the regulated cascode current buffer, has an input impedance of less than 10 ohms for a bandwidth of 500 MHz. The amplifier is followed by individual comparators for each threshold voltages. In PET imaging applications, the rise time of the Silicon Photomultipliers (SiPMs) can be of the order of few nanoseconds, and in some cases

even less than a nanosecond. This fast rising edge helps to extract the time-of-flight (TOF) information of the 511 keV photons during the positron annihilation. It is thus essential to extract the time stamp of the first photoelectron with a resolution of the order of 100 picoseconds. A novel input driven self-clocked comparator architecture has been implemented in this work. The self – clocking mechanism makes it easier to integrate multiple readout channels on the same substrate, because there is no need for an external clock generation scheme. Also, because it is input driven, the comparator is disabled when there is no valid photon event, and hence, there is no unnecessary switching power dissipation because of charging and discharging of internal nodes within the comparator. Followed by the comparator is the time-to-digital converter (TDC) to output the ToT values and the time intervals on the rising edge. The TDC architecture is composed of two blocks - one for measuring the ToT and the other for measuring the time stamps for all the thresholds on the rising edge. For the ToT measurement, a clock edge counter is used to quantize the time during which the comparator output is high, using a free running clock. For the time stamps, a TDC architecture comprising a fine and a course quantizer is used. The fine quantizer is based on a delay line based ring oscillator TDC. The course quantizer counts the number of clock edges of the ring oscillator output.

9.1 SUGGESTIONS FOR THE FUTURE RESEARCH

Time-over-threshold (ToT) based digitization techniques are promising for future research in Imaging systems, due to their low power and small area. To better exploit the advantages of ToT, the ideas presented in this work can be extended further, as follows –

1. The comparator topology can be extended to applications requiring ultra-low power ADCs and high quality factor filter design, like biomedical, security and autonomous navigation. A majority of the power consumption in the Analog-to-Digital converters (ADCs) is used

in these areas comes from the continuous switching power dissipation of the comparators. The input driven self-clocked comparator technique can serve as an excellent candidate for making those systems highly power efficient.

2. Further improvements like time-multiplexed TDC techniques can be added to the multi-threshold ToT architecture, which will make it possible for the data acquisition electronics to be even more power efficient.
3. Being a digitally intensive architecture, if implemented in advanced technology, this system can improve the timing resolution of the data acquisition system even further.
4. The multi-threshold ToT system has several options utilizing the TOT threshold trigger time stamps on the rising edge. For example, a simple extrapolation of the first three triggers can be used to estimate when the leading edge rose above the noise floor of the photo-sensor. More advanced techniques based on various statistical estimation techniques and machine learning algorithms can be used for image reconstruction.

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