Integrating Bidirectional Brain-Computer Interfaces in Low-Voltage CMOS

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A dissertation

submitted in partial fulfillment of the

requirements for the degree of

Doctor of Philosophy

University of Washington

2020

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ABSTRACT

Integrating Bidirectional Brain-Computer Interfaces in Low-Voltage CMOS

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Realizations of small-form factor, ultra-low power bidirectional brain-computer interfaces (BBCIs) will enable treatment of chronic neurophysiological disorders and allow new modes to investigate brain function. Neural stimulators have been shown to effectively alleviate the symptoms of various neurological disorders, and development of closed-loop bidirectional neural interfaces will increase therapy effectiveness by adapting to real-time measurements. This dissertation studies implementation of neural interface functionality in a single chip consuming minimal power and silicon area with two novel techniques: a. Time-multiplexed, mixed-signal artifact cancellation for simultaneous stimulation and sensing; b. Compact integrated stimulators

with on-chip resonant charge pumps. The following paragraphs enumerate the two proposed techniques and their associated challenges and advantages.

First, integrated artifact cancellation allows uninterrupted recording of neural signals during stimulation pulses in adjacent tissue. Existing low-frequency signals can be preserved, and an artifact-immune recording system can quantify the body's immediate response to stimulation. Cancelling artifacts is complicated by the magnitude difference between stimulation pulses and neural signals of interest. Stimulation artifacts are several orders of magnitude larger than the upper dynamic range of typical recording systems, so a canceller requires specialized front-end electronics. Stimulus artifact cancellation has been demonstrated with digital adaptive filters interfacing with a switched-capacitor analog recording front-end. On cue from the stimulator, the adaptive filter learns the artifact shape based on recording output and subtracts the full stimulus artifact waveform from the recording input. The technique was first prototyped with an FPGA-based adaptive filter interfacing with standalone recording and stimulation chips. Later, the algorithm was optimized for power-efficient operation over multiple stimulation and recording channels. It was then integrated into a multi-channel bidirectional interface capable of cancelling artifacts from four independent stimulators on four recording channels. The power-efficient canceller was fabricated in the 65nm TSMC low-power CMOS process, allowing use of low-voltage supplies for the calculation back-end. This enabled 60dB of artifact suppression with a full-scale limit of ±125mV while only consuming 49nW per channel.

Second, effectively stimulating neural tissue through low form-factor electrodes requires high voltages to drive current through large electrode impedances. These stimulation voltages often exceed the maximum voltage ratings of the high-density CMOS technologies desired for compact neural interfaces. Stacked charge pumps are often used to generate large voltages with multiple

low-voltage stages, protecting CMOS electronics. Standard charge pump implementations pump charge with large capacitors at low frequencies to maintain power efficiency. In these cases, charge pump capacitor area dominates the system size. The proposed stimulator uses resonant clocking techniques to maintain efficiency with small charge pump capacitors clocked at high frequencies. An integrated inductor creates a resonant tank with the charge pump capacitors, compensating for switching losses in the circuit. This technique was demonstrated in a multi-channel BBCI chip. Four independent differential stimulators were integrated with a 64-channel recording system and the previously mentioned artifact cancellation back-end in a 4mm² 65nm CMOS chip. The stimulators source up to 2mA of stimulation current with a range of ±11V. The internal charge pumps supply power with a DC-DC efficiency of 38%, as compared to the possible 6% of a theoretical non-resonant topology of equal size.

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ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor, Dr. Jacques Rudell. This degree has been a long journey full of failures, successes, and challenging ideas and problems. His patience and guidance has brought this project from a dream five years ago to a silicon-proven reality. Professor Rudell's stringent eye for quality in data, presentations, and publications has driven my development as an engineer and peer-reviewed researcher. The integrated circuit projects coming out of our lab would not be possible without his wealth of experience and driving motivation. Additionally, I am grateful for his willingness to undertake unconventional research projects. This neural interface work was new for both of us, and we developed a wealth of knowledge and experience to nearly become experts.

I would also like to thank Dr. Visvesh Sathe for his support and advice throughout my degree. The system built in this work would not have been possible without the collaboration between our two groups and the close supervision provided by Professor Sathe. I am always able to go to him for technical advice or to bounce complicated ideas around. I'm also grateful for how he would bring challenging questions to the table during design reviews, exams, and discussions. Professor Sathe is the ideal example of a critical thinker, and I hope I can develop my skills to achieve his level of engineering prowess.

I owe my introduction to integrated circuits to Dr. Jerry Lopez, of Noise Figure Research. During my undergraduate, I took his microelectronics class and found my first research experience in the Silicon Systems Research Lab, managed by Dr. Richard Shi. Jerry's close mentorship and willingness to put in the hard work gave me a perfect start in IC design. I would not have made it into or through grad school without the discipline and mentality I learned under his tutelage. I have Jerry to thank for starting on the path to become a "rock star" of Electrical Engineering.

Membership in the Center for Neurotechnology (CNT) opened the door to partnerships with other departments in the University of Washington. Dr. Steve Perlmutter has been an invaluable resource and co-investigator in this work. Thank you for the feedback and access. This project would not be successful without the connection to the neuroscience community that you have provided. Steve has always been available for discussions and help with publications, and I am grateful for your support with our in-vivo experiments. Dr. Chet Moritz, co-director of the CNT, has always been a strong proponent and supporter of our work. Thank you for being a committee member for my final exam. Thank you also, Dr. Azadeh Yazdan, for helping with my final exam and opening our University to the fascinating realm of optogenetics.

Thank you, Dr. Patrick Boyle, for your help with the doctoral examinations. You were a strong and fun addition to the committees.

The final validation of any biomedical interface is in-vivo animal studies. It was a pleasure working with Richy Yun and Brian Mogen in the lab. Everyone learned a lot, and I am very impressed by the medical research labs run at the UW.

Thank you to the many lab-mates I've had throughout the years. It all started with Bijan Shirazi-Wu during the late years of our undergraduate at UW. He taught me how to have fun doing research. Working in Dr. Shi's lab with Aili Wang was my first foray in graduate-level research. Thanks, Aili, for all the shared learning along the way. I'm glad we both made it!

Eric Pepin introduced me to neural interfaces. Thanks for your hard work starting this project. Eric was a welcome companion in the trenches, working on the first H-bridge stimulator.

William Smith and I worked closely together developing the recording system used in this chip. Thanks for being such a good friend.

The guys in the FAST lab have all been a pleasure to work and grow with. We've had a great collection of engineers in our lab, and I wish them all the best. Dr. Tong Zhang was an exemplary researcher and valuable resource. Kun-Da Chu has been a good friend and brings a lot to our lab. Samrat Dey has been a fantastic compatriot, working through grad school and TA responsibilities together.

Lastly, I would like to thank all the people from my personal life that have supported me through the long journey of grad school. Melaney and Cliff Uehlin, my parents, have given me all the opportunities in the world. I wouldn't have been inspired to pursue graduate school without their excellent example. More importantly, I wouldn't have survived life in the city without their help.

Thank you, Monika Grinbergs, for putting up with me in the last, long years of my PhD.

Chapter 1: INTRODUCTION

Realizations of small-form factor, ultra-low power bidirectional brain-computer interfaces (BBCIs) will enable treatment of chronic neurophysiological disorders and allow new modes to investigate brain function. Neural stimulators have been shown to effectively alleviate the symptoms of Parkinson's disease [1], epilepsy [2], depression [3], and obsessive-compulsive disorder [4]. Development of closed-loop neural interfaces with simultaneous recording and stimulation capabilities will increase therapy effectiveness by adapting to real-time measurements of the modulated neural tissue without input from a practitioner [5], [6]. Additionally, a sufficiently complex closed-loop interface could be used to reanimate paralyzed limbs or drive neuroprostheses with sensorimotor feedback [7]. In addition to clinical applications, simultaneous stimulation and sensing opens new research opportunities for neuroscientists, including study of neural plasticity [8] and low-latency neural mapping [9].

In order to increase the efficacy and accessibility of potentially life-changing treatments, BBCI implants must be developed with minimal cost, size, and power use. A single-chip BBCI implementation minimizes area and power consumption by reducing the number of interconnects. Additionally, standard scaled-CMOS technology offers dense and power-efficient digital devices for complex BBCI therapy protocols. A single-chip CMOS BBCI front-end requires integration of recording, stimulation, and power generation electronics on the same substrate along with a sophisticated digital back-end. Figure 1-1 shows the necessary components of a single-chip BBCI front-end. Additionally, resilient operation in chronic implants requires the capability to continuously adapt to a slowly varying environment to maintain desired stimulation and recording function.

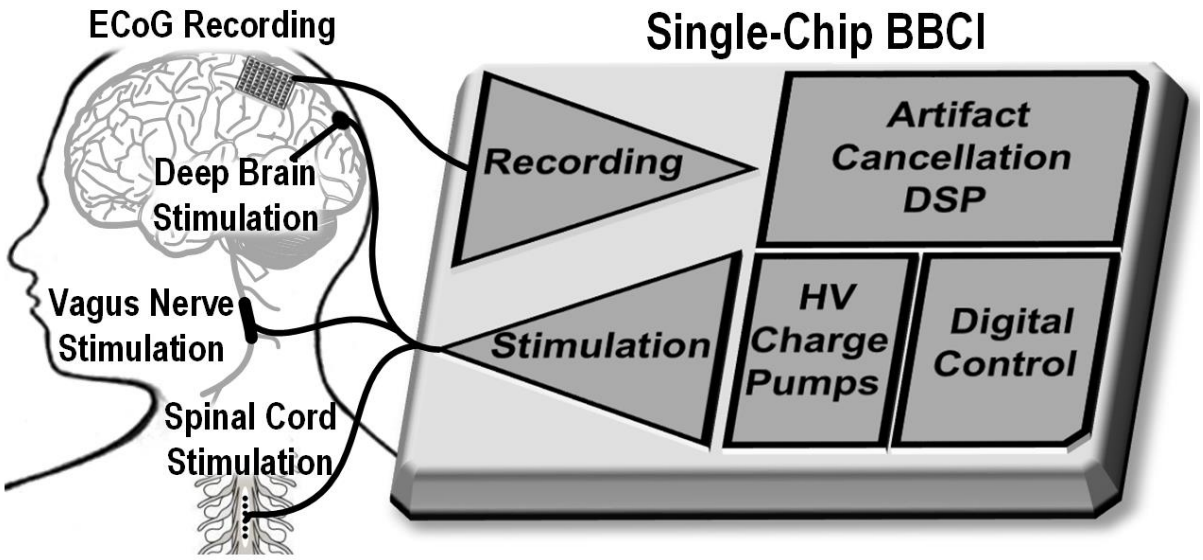
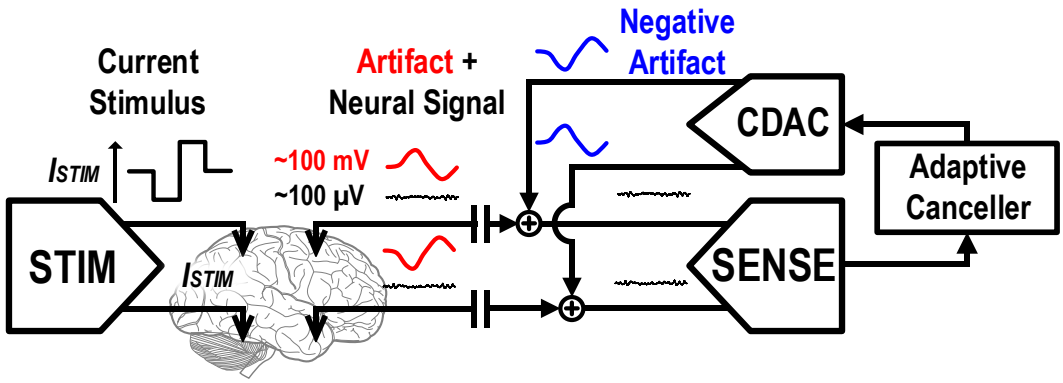


Figure 1-1. Example integrated bidirectional neural interface.

Critical challenges remain before the vision of implantable single-chip BBCI neural interfaces become a reality. First, electrical stimulation creates in-band artifacts that are several orders of magnitude larger than signals targeted by neural recording front-ends (~100mV vs ~100µV) [10], as in Figure 1-2. Second, voltages generated at the stimulator–electrode interface (Figure 1-3 (a)) regularly exceed acceptable gate oxide breakdown limits (<1.5V) for reliable operation in advanced, scaled CMOS technologies [11], as in Figure 1-3 (b). These two challenges are addressed with a single CMOS test chip.



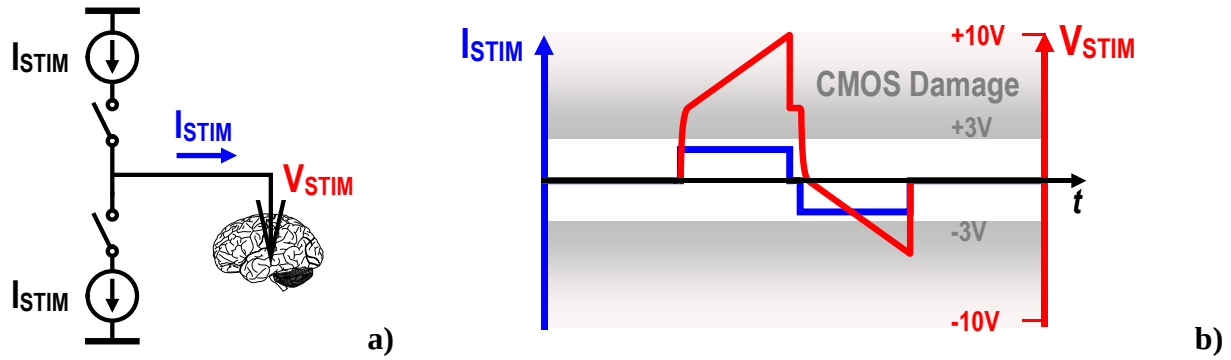


Figure 1-3. A simplified constant-current stimulator (a) demonstrating high voltages at the tissue-electrode interface exceeding CMOS maximum ratings (b).

High-voltage stimulation compliance (±11V) is achieved using stacked circuits in low voltage scaled CMOS. A stacked driver architecture enables constant-current stimulation through a large range of electrode impedances from the same chip as a complex, efficient digital back-end. Charge pumps are typically used to create above-V_{DD} stimulation voltages, and the pumping capacitors dominate system area. This work minimizes the charge pump area using integrated inductors to reclaim power while operating at a high charge pump clock frequency to reduce area overhead [12].

The time-division multiplexed recording architecture from [13], [14] is integrated on the same chip to provide closed-loop adaptive feedback for stimulus artifact cancellation on multiple channels. Canceller computation hardware is also time-multiplexed to reduce power and area consumption. The resulting monolithic 65nm CMOS chip includes all the necessary components to allow simultaneous 64-channel recording and 4-channel stimulation for BBCI-clinical applications.

1.1 RESEARCH OBJECTIVES

This dissertation will focus on furthering integration of implantable bidirectional neural interfaces by addressing the two aforementioned challenges:

1. Cancellation of stimulation artifacts to allow undistorted, uninterrupted recording of low-amplitude neural signals during stimulation events. The goal is to integrate artifact cancellation capabilities for multiple recording and stimulation channels while minimizing power and area overhead.
2. Compact and efficient generation of stimulation power to drive multiple milliamps of current with at least 10 Volts of driving voltage. The goal is to explore methods to increase the charge pump density in low-voltage silicon circuits while maintaining efficiency and without using external components.

The implemented test chips in this dissertation are fabricated in advanced standard bulk CMOS technologies to demonstrate the universal applicability of the described techniques. The multiplexed artifact canceller and resonant charge pump architectures are intended for fine-line CMOS technologies, and the proposed techniques would be well suited for any further advanced technology nodes.

1.2 OVERVIEW AND ORGANIZATION

The remainder of this dissertation is organized as follows:

Chapter 2: This chapter describes currently accepted practices for neural stimulation and recording, as well as current methods of stimulus artifact cancellation. State-of-the-art neural interfaces are discussed with their advantages and shortcomings. The author's previous work on artifact cancellation and stimulator front-ends is also discussed.

Chapter 3: The artifact canceller and high-voltage stimulator are analyzed. Theoretical derivations for the canceller adaptive filter and stimulator charge pump are described in detail.

Canceller discussions include comparison of adaptation algorithms, adaptation stability, and scalability. Stimulator discussion focuses on optimization of charge pump area and efficiency.

Chapter 4: This chapter describes implementation details of the fabricated 65nm bidirectional neural interface test chip. System and block-level architectures are described, as well as the associated design decisions. Insights into low-power, mixed-signal schematic and layout design are given in this chapter.

Chapter 5: Measurement results from the implemented test chip are described. Results are compared to the theoretical values derived in Chapter 3, as well as the state-of-the-art.

Chapter 6: This chapter gives a summary of the dissertation and lays out future directions for research on single-chip neural interfaces. This discussion comments on application of the proposed circuit techniques to other integrated circuit technologies, lessons learned during the design, and possible improvements to the implemented systems.

Chapter 2: EXISTING NEUROMODULATION SOLUTIONS

Electrical neuromodulation platforms are designed to measure the activity of neurons *in-vivo* while having the ability to safely manipulate neural activity. A neuromodulator measures neural activity with a recording data converter connected to tissue by metal electrodes. The microvolt-level electrical signals emitted from neural tissue are converted into digital signals for processing and analysis. Electrical stimulation can cause neurons to activate or deactivate by depolarizing cell membranes through charge injection [15]. A neural stimulator sends charge into tissue by passing a controlled current through electrodes.

2.1 THE TISSUE-ELECTRODE INTERFACE

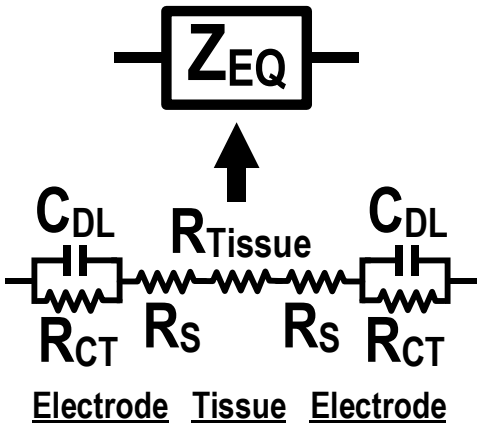


Figure 2-1. Differential electrode-tissue interface model used for stimulation analysis

While neural tissue itself is low impedance, the biocompatible electrodes used to connect circuits to tissue have large series capacitive and resistive components. This large impedance complicates recording and stimulator designs. Figure 2-1 shows the reduced-order electrode-tissue interface model [16]. C_{DL} is a double-layer capacitance formed by the ion bilayer at the interface between metal and solution. This capacitance can range from 100pF to 10nF depending on the size of the electrode contact area. R_{CT} is a charge transfer resistance on the order of GΩ, modeling

leakage across C_{DL}. R_S is a solution resistance on the tissue side of the interface. This resistance can range from tens of kΩ to several MΩ and changes slowly over time as tissue reacts to the electrode [17]. Maintaining signal integrity during neural recording depends on recording amplifier input impedances being significantly larger than electrode impedances. A low recording input impedance attenuates signal amplitudes at low frequencies, where neurons operate. Additionally, stimulation therapy currents as low as 10μA can still create large voltages by accumulating charge on series capacitances.

2.2 NEURAL STIMULATION METHODS

There are several different methods for injecting current into neural tissue to perform stimulation. The resulting current flow through the neural tissue is the same but use of various current sources and voltage supplies affect how voltage is distributed across the electrodes and tissue. There are a few key features common to each stimulator. First, each stimulator has a current-controlled sink to ground for the leading phase of the current pulse. Where the current is sourced varies among topologies. Second, a high-voltage supply drives current through the electrode-tissue load. High voltages are necessary to source up to milliamps of current through relatively high electrode impedances. High-voltage supplies are typically 10V to supply milliamps through electrodes with tens of kilo-ohms of DC impedance, as common for electrodes in muscles or on the surface of the brain [18]. Differing HVDD placements affect the DC bias of the neural tissue and the appearance of voltage artifacts. This section discusses how each stimulator topology generates voltage at the electrode interfaces. Propagation of stimulation artifacts through neural tissue will be discussed later.

Ground-Return Stimulators

The ground-return stimulator is the simplest stimulator configuration. There is an active electrode that performs the controlled current sink and source. A common return electrode is held at a DC voltage to provide the current return path for both phases. In benchtop configurations, the return is typically held at ground, while the current sources are operated on positive-negative supplies. However, in integrated systems, a single supply necessitates that the return electrode is held at HVDD/2, as shown in Figure 2-2 [19], [20]. This topology is preferred for high-channel count stimulation, as each channel only requires one dedicated electrode, with a shared return electrode. Integrated ground-return topologies bias the neural tissue to an intermediate DC voltage, which complicates DC-coupled recording front-ends without a shared reference voltage.

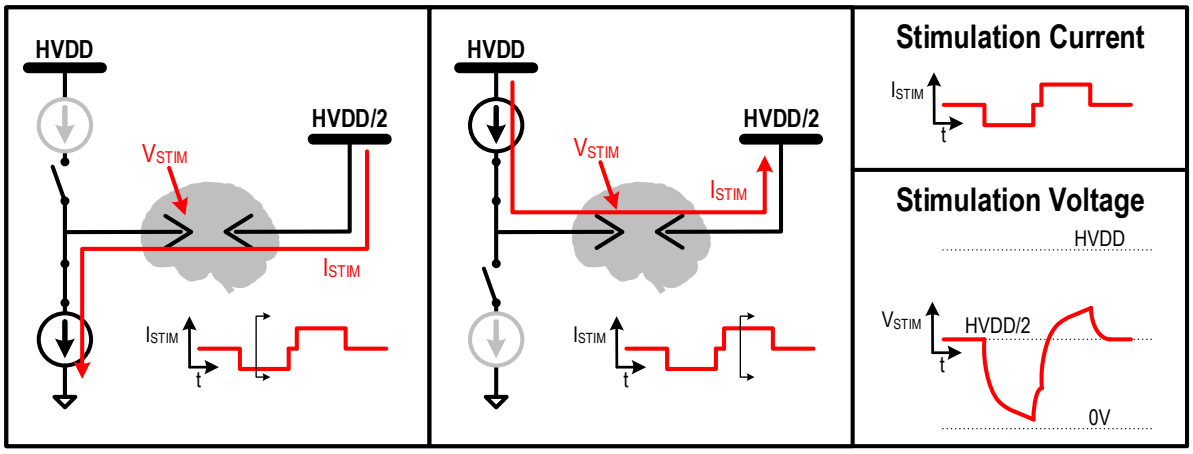


Figure 2-2: The ground-return stimulator topology.

Differential Stimulators

A fully differential stimulator connects a regulated current source to each active and return electrode, one side sourcing and the other sinking for the first phase and visa-versa for the second phase, as shown in Figure 2-3. This is a common configuration for single-channel stimulators, as

charge balancing is easily accomplished with standard CMOS matching practices. Additionally, the effective voltage compliance of the differential stimulator topology is double that of the ground-return configuration. Each electrode sees an equal and opposite voltage change for all stages of stimulation, with the range of HVDD to ground for each electrode, as can be seen in Figure 2-3. The main difficulty in designing differential stimulators is matching source-mode and sink-mode current sources [21]. This is especially difficult for high-voltage-compliant stimulators, as the source-mode current source will be biased above the normal voltage rails of a given process, modulating impedances and increasing control complexity. Additionally, both electrodes must be pre-charged to a mid-rail DC value to ensure reliable current source operation. This presents the same DC-coupling issue as with the ground-return topology.

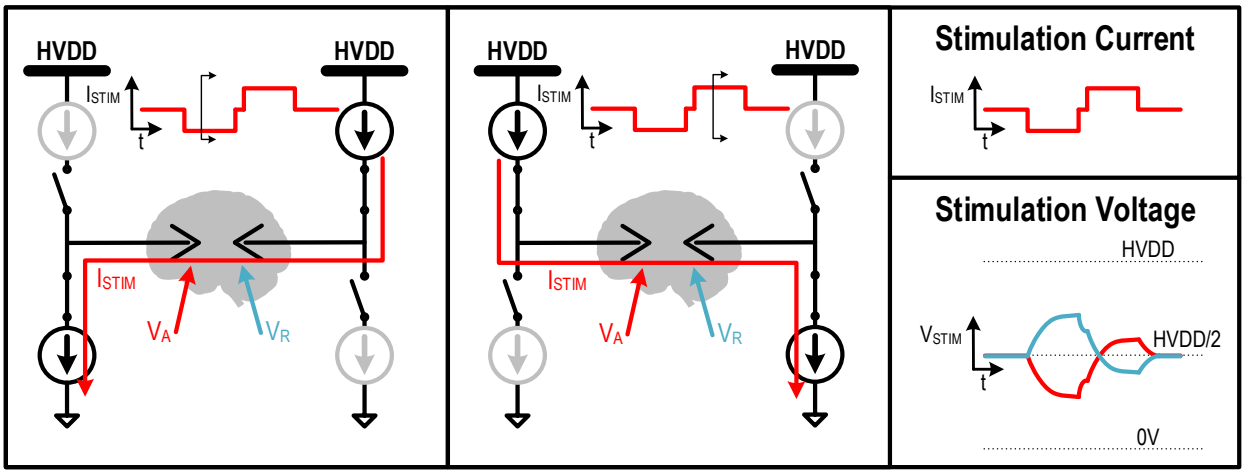


Figure 2-3: The fully differential stimulator topology.

H-bridge Stimulators

The stimulator topology implemented in this work is an H-bridge, similar to the general architecture in [22], [23]. The implemented H-bridge stimulator described in this thesis uses only sink or source-regulated current supplies, easing the matching concerns of the differential stimulator. The high-voltage supply is used to directly bias the neural tissue during stimulation,

decreasing system complexity by eliminating the mid-rail supply. During stimulation, one electrode is connected to HVDD while the other sink-regulates current to ground. The opposite could be done, connecting to ground and source-regulating from HVDD, but it is much easier to design and control ground-connected current sources. Like the differential stimulator, the effective voltage compliance is doubled as compared to the ground-return configuration. The H-bridge stimulator does generate unique artifacts, as the electrode voltages are monopolar and unbalanced.

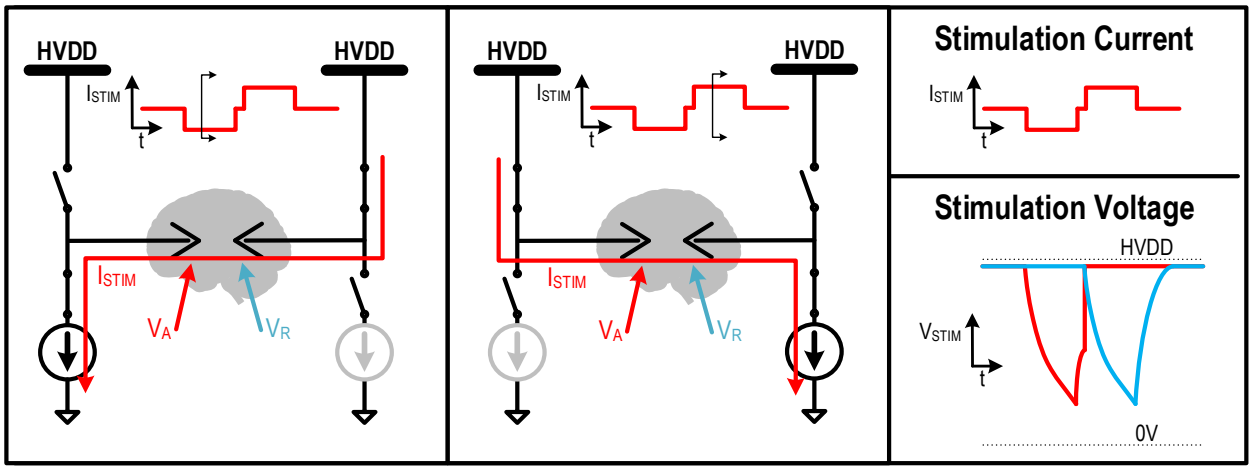


Figure 2-4: The H-bridge stimulator topology.

State-of-the-Art High-Voltage Stimulation

In any stimulation topology, the maximum stimulation voltage is limited by the voltage tolerance of circuit devices used in the stimulator driver. Although advancing the state-of-the-art in energy efficiency [24]–[27] and form-factor [28], [29], most bulk-CMOS neural stimulators published to-date have voltage compliance that is impractically low for many BBCI applications ($VDD_{DEVICE} \leq 3.3V$). Off-the-shelf neural interfaces typically integrate the stimulator front-end in specialized high-voltage processes to avoid voltage headroom issues. Several academic neural interfaces have moved all circuitry to high voltage CMOS [28], [30], [31] at the cost of chip area and digital processing power efficiency.

Several bulk-CMOS stimulators have been developed with unique designs that safely enable elevated voltage compliance [32]–[34]. These works employ an on-chip DC-DC converter to generate a voltage several times greater than the VDD_{DEVICE} (e.g. [35]–[37]), and use specialized front-end circuits to allow the stimulator to sink and source current at these high voltages. The multi-stage circuits consume considerable silicon area, particularly cascaded high-power charge pumps. This work optimizes the H-bridge topology developed in [23] to minimize area by increasing the DC-DC converter clock frequency and employing resonant clocking techniques.

Using inductors to recover lost reactive energy is a well-known technique in low-frequency power converters [38], [39]. More recently, similar techniques have been applied to gate drivers for high-frequency on-chip clock distribution [40]. Driving an inductor in parallel with the capacitive clock-tree load creates a resonant tank that undergoes damped oscillation, as shown in Figure 2-5. The clock driver must then only replenish the energy dissipated in the real-part impedance of the resonant tank, greatly reducing power consumption. Oscillation frequency is set by the tank inductance and capacitance and is tuned by switching in banks of capacitors. This technique allowed clock drivers operating at several gigahertz with greatly reduced power consumption, at the cost of inductor area overhead.

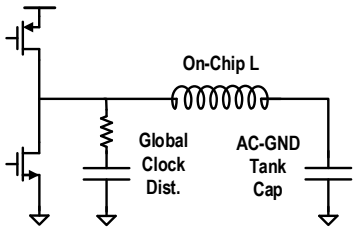


Figure 2-5. Resonant clock drive scheme from [40].

This technique was first applied to integrated neural stimulators for power harvesting [41]. A large integrated inductor was created around the perimeter of the chip, in parallel with a large

capacitor, tuned to match the stimulator DC-DC converter frequency. In this configuration, the inductor creates a resonant tank for energy conservation as well as a receiving antenna for applied RF energy. While this approach allows efficient stimulation, the inductor consumes too large of an area when tuned for the stimulator DC-DC frequencies. The implementation in [41] uses a 3mm x 3mm coil to provide 150µA of stimulation current at 3.3V, not nearly enough current or voltage for medically relevant stimulation. The power limitations of this energy harvesting technique are set by the maximum safe energy that can be radiated through the human body, approximately 10µW/mm² at hundreds of MHz [42].

The high voltages generated by current-mode stimulation in neural tissue also propagate to any adjacent neural recording electrodes. This interference can distort or obscure desirable naturally occurring signals. The next section describes the nature of these artifacts and methods currently used to prevent stimulation artifact interference in the recording system.

2.3 STIMULUS ARTIFACT CANCELLATION METHODS

Artifact Propagation

There are two components to the stimulation voltage artifact: common-mode voltages that propagate to all connected neural tissue due to stimulation voltages at the electrode-tissue interface and voltage differences between two locations in neural tissue due to current flowing through the tissue impedance. Both types of artifacts affect the recording front end: common-mode artifacts change input biasing conditions (especially for open-loop amplifier topologies) and differential-mode artifacts will saturate any high-gain amplifier.

The common-mode artifact is highly dependent on stimulator topology. Once past the electrode-tissue interface, neural tissue is relatively low impedance, consisting of a nearly

homogenous, distributed series-R, shunt-C network. The common-mode artifact seen at all terminals of the recording architecture is then a superposition of the stimulator's active and return electrode voltages, depending on the particular recording electrode's position with respect to the stimulator electrodes. Typically, the electrodes for differential recording are close enough together that this "common-mode" signal will propagate to the positive and negative inputs equally. However, if there is any difference in distance between the two recording electrodes and the stimulation electrodes, the common-mode superposition of the two stimulator electrode voltages will be imbalanced and manifest itself as a differential signal [43].

Figure 2-6 shows an example of the superposition of the two electrode voltages as a resulting common-mode artifact. For the ground-return stimulator topology, a slightly attenuated version of the single active electrode voltage is seen at all points in the neural tissue. As the recording electrodes approach the active electrode, the signal will get larger. The opposite is true for the AC-grounded return electrode. The differential stimulator ideally generates no common-mode artifact, however any non-symmetrical electrode configuration will still result in a small common-mode artifact. The H-bridge stimulator produces a unique artifact shape. As each of the electrodes is driven up (or down) in voltage, a monophasic common-mode voltage artifact is generated. The other electrode is held at HVDD for the other electrode's stimulation phase. So, assuming differential recording electrodes are equidistant to the stimulator electrodes, the common-mode artifact should be half the size of each electrode's peak voltage

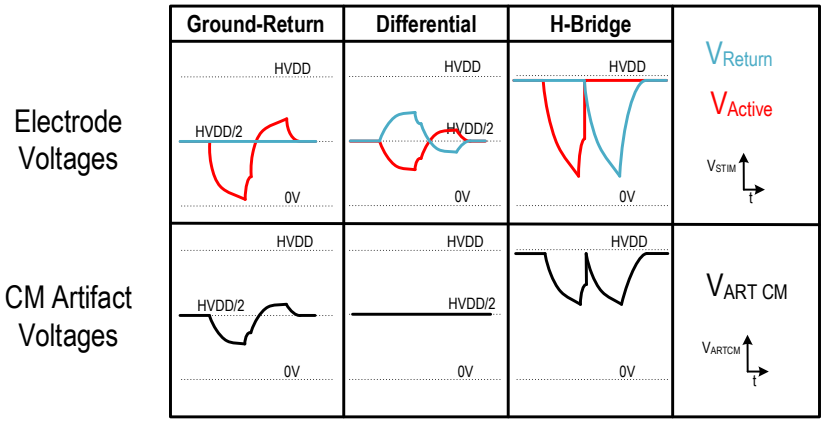


Figure 2-6. Common-mode artifact superposition examples.

In addition to the common-mode artifact caused by all neural tissue moving with the stimulator electrode voltages, there is a differential-mode artifact induced by stimulator currents flowing through the neural tissue itself. Any tissue space between differential recording electrodes presents a mostly resistive impedance. As the stimulator current propagates between stimulator electrodes, it radiates throughout the neural tissue, which is a distributed impedance created mostly by the saline solution between living cells [15]. Based on measured artifacts during experiments, the internal tissue impedance seen by the stimulation current once in the tissue is mostly real, with a distributed shunt capacitance to ground. This tissue impedance creates a small voltage difference between the differential recording terminals, presenting itself as a differential-mode artifact. These artifacts are orders of magnitude smaller than the common-mode artifacts described above (approximately 10mV compared to ~1V common-mode artifacts). Based on measurements, the equivalent Z_{TISSUE} for differential stimulation across one millimeter of neural tissue with recording electrodes in parallel two millimeters away is approximately 15Ω with negligible shunt capacitance to ground. The low-pass effects of the neural tissue itself are overpowered by the parasitic capacitances in the electrodes, wires, and interconnects.

State-of-the-Art Artifact Cancellation Methods

Many efforts have been made to solve the stimulation artifact problem. Stimulators have been configured to reduce artifact amplitude via pulse shaping [44], [45], power domain isolation [46], and use of orthogonal stimulation modes [47], [48]. Several recording systems have been designed to be artifact-immune with fast-restart input amplifiers and increased dynamic range. Finally, artifact cancellation methods have been developed in post-processing and recording front-ends.

Input Saturation Recovery

Early bidirectional systems accepted amplifier saturation during stimulation and focused on decreasing saturation recovery times after stimulation [21]. This means that all neural signals occurring during stimulation and shortly afterwards are lost. This was considered acceptable because the latency between stimulation and resultant neural activity is typically on the order of milliseconds. The recovery time from amplifier saturation varies, depending on the amplifier topology. Consider the traditional closed-loop neural amplifier, shown in Figure 2-7. This amplifier topology is well optimized and ideal for matching gain and bandwidth between multiple channels. Matching integrated resistors and capacitors is much easier than matching process-sensitive amplifiers [49].

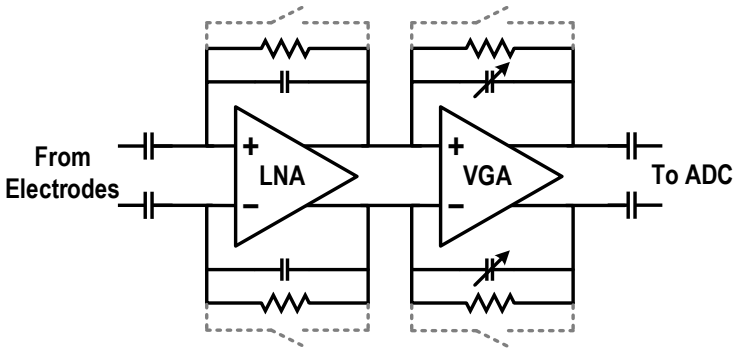


Figure 2-7. A traditional closed-loop neural amplifier (feedback reset switches shown in grey).

The bandwidth of ECoG and single neuron acquisition systems is typically 1Hz to 1kHz and 100Hz to 32kHz. This means that the loop bandwidth of the closed-loop amplifier in Figure 2-7 could be as low as 1kHz. Therefore, recovery from amplifier saturation could take between $1/f_{HP}$ and $1/f_{LP}$ to recover, the inverse of the transfer function high-pass and low-pass corners. To speed up the process, reset switches are placed across the feedback caps, temporarily speeding up the amplifier response time during stimulation. This reset zeros out the differential amplifier gain during stimulation, but recording can resume as soon as the switches are opened once again. Open-loop amplifiers used for chopper-based recording configurations have much lower settling times, so extra methods are not necessary for rapid amplifier recovery.

Increased Input Dynamic Range

Recent silicon front-ends have been implemented with dynamic ranges that can tolerate full-scale stimulation artifacts. The first implementation, from UCLA, relaxes front-end gain to keep stimulation artifacts within the linear range [50]. The system is chopper-stabilized to shape the heavy flicker noise at low frequencies, compensating for low gain. All filtering and noise shaping is done in the analog domain, with transconductance stages and switched capacitor/resistor networks for gain and filtering. This implementation trades an increase in power consumption for increased dynamic range, active filtering, and an input impedance boosted through feedback.

The same group proposed another novel solution, using a high dynamic-range voltage controlled oscillator (VCO) as the input stage [51]. The input voltage is buffered with a moderate amount of gain and then used to bias a ring oscillator. This approach has highly nonlinear gain which is compensated by estimating and cancelling the frequency-to-voltage transfer function nonlinearity with a 5^{th}-order polynomial fit. High frequency artifacts would create many

intermodulation products and harmonics when passed through a nonlinear transfer function, which may not be completely suppressed by a 5^{th}-order inverse function.

Post-Processing

Digital artifact cancellation was first developed as a post processing method to remove artifacts from pre-recorded data using a computer. Most neural recordings from clinical settings are taken with robust benchtop equipment that can easily handle and record the multiple millivolts presented by stimulation artifacts. In this case, because the front-end amplifiers are not saturated, the stimulation artifacts are merely superimposed on the underlying neural signal in the final recording. After determining the shape of the artifact, one can easily subtract it from the recording at each stimulation instant [52]. The art in post-processing is developing an automatic method for determining the artifact shape, rather than manually creating a "template" by visual inspection, a method called template subtraction [53].

Because the stimulator current waveform is always tightly controlled by the user, there are several different ways to infer the artifact shape from a recording. Local curve-fitting methods automatically generate accurate templates for each stimulation instance, relying on the known stimulation waveform as a boundary condition for the solution space [54]. This approach is computationally expensive, which is negligible in benchtop applications. More subtle methods have been developed that rely on the spectral properties of the artifact and the underlying neural signal. Neural signal power is highly concentrated below 2kHz and artifacts can have content in the hundreds of kilohertz. By selectively bandpass filtering the corrupted recording, decomposing, weighting, and summing its parts, an automatic template subtraction scheme can be created with relatively inexpensive digital signal processing (DSP) techniques [55]. Knowing the stimulation amplitude and timing, the artifact shape can be "learned" with filter-training regression techniques

made popular in inter-symbol interference (ISI) cancellers for communications circuits. Discrete implementations of this training method can use complex self-training filters, such as the Weiner filter, having no computational bottleneck [52]. However, in integrated implementations, every operation costs power and area, so complex DSP algorithms are not appropriate.

Recent efforts with integrated, high dynamic range recording systems have moved the back-end post processing on-chip. Blind normalized LMS (least mean square) algorithms have been implemented on chip with a VCO-based recording architecture[56]–[58], achieving fast canceller convergence time at the cost of digital power and area. This approach requires approximately 60-times more arithmetic logic than the proposed canceller architecture and an additional recording channel for calibration, all for the sake of fast convergence and stimulator-"blind" operation.

Front-End Cancellation

Systems for recording signals in the nervous system have high gain to allow quantization of small natural signals with a certain signal-to-noise ratio (SNR). This high gain leads to a small input-referred dynamic range for systems integrated in bulk CMOS. Limits to the maximum supply voltage for the recording quantizer constrain the input-referred dynamic range to approximately V_{REF}/A_{IA}, where V_{REF} is the analog-to-digital converter (ADC) full-scale reference voltage and A_{IA} is the voltage gain of the instrumentation amplifier (IA) before the ADC. In the implemented system, the ADC reference voltage is 500mV with an IA voltage gain of 2000, leading to an input-referred dynamic range of 250μV (not accommodating for delta-sigma feedback) [12]. The limited dynamic range in integrated systems means that voltage artifacts must be cancelled before the gain stage. Suppressing the artifact voltage to within the input-referred dynamic range prevents saturation at the IA output or ADC input.

A front-end artifact canceller was implemented at the University of Michigan, integrating 4-channel (8-channel) stimulation (recording) interface in 0.18µm CMOS with an adaptive equalizer [59]. Each recording channel has a dedicated input decoupling network, LNA, ADC, simplified LMS equalizer, and DAC for equalizer output. The area per recording channel is large, with several multi-picofarad integrated capacitors per channel. This system also falls short in voltage compliance in both stimulation and recording. The stimulators are limited to ±0.5V and artifact suppression is performed on single-millivolt-scale artifacts, rendering the system unsuitable for most neural stimulation applications.

2.4 PREVIOUS WORK

Standalone H-Bridge Stimulator Test Chip

The stimulation and artifact cancellation experiments that influenced this dissertation were performed with a previously developed 65nm stimulator test chip, designed by Eric Pepin. The overall H-bridge architecture in this work draws heavy inspiration from the previous design [23].

The single-channel stimulator is an electrode-invariant, ±12V-compliant H-bridge topology designed in the TSMC 65nm GP CMOS process. The stimulator delivers between 50µA and 2mA of biphasic, charge-balanced current pulses with active and passive discharge. A highly simplified block diagram of the stimulator is shown in Figure 2-8. The unique topology used in this design employs standard 1.2V and 2.5V CMOS devices in highly robust configurations to allow ±12 volts of swing at the electrode output terminals. High-voltage adapters (HVAs) act as current buffers to level shift the high electrode voltages to safe operating voltages for the sensitive, well-matched 1V current source. To save power during the stimulation process, dynamic voltage supplies (DVSs) track the voltage changes across the high-impedance electrode-tissue load, delivering only as much

power as necessary to charge the tissue and maintaining the proper biasing to prevent current source saturation.

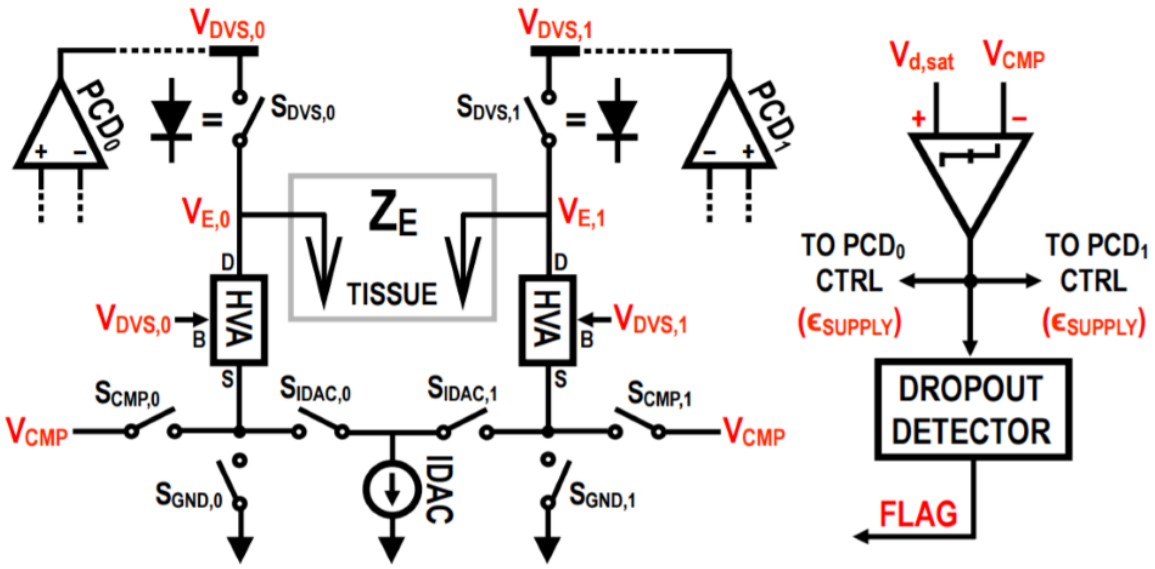


Figure 2-8. Simplified H-bridge stimulator block diagram.

The electrode voltages are dynamically scaled with a negative feedback structure outlined in Figure 2-9. The positive current drivers (PCDs) are ideally represented as op-amps to clearly demonstrate the feedback architecture. As one side of the H-bridge sinks current through the electrode-tissue load (steps 2 and 5), a voltage drop across the load forces the sinking side voltage down and the supply side voltage up. To prevent the current source from saturating, a PCD is used in feedback to raise the supply side voltage to track ΔV across the load. The stimulator then follows a strict break-before-make scheme to avoid sudden transient currents. The previously sinking side is connected to ground while the previously sourcing side is connected to the current source (steps 3 and 4). The high-side switches are implemented with integrated diodes, as high-side CMOS switches face reliability and control complications. These diode switches are forced off by the same PCD tracking loop, forcing the supply voltages to track the electrode voltages exactly, forcing a voltage bias of zero across the diodes.

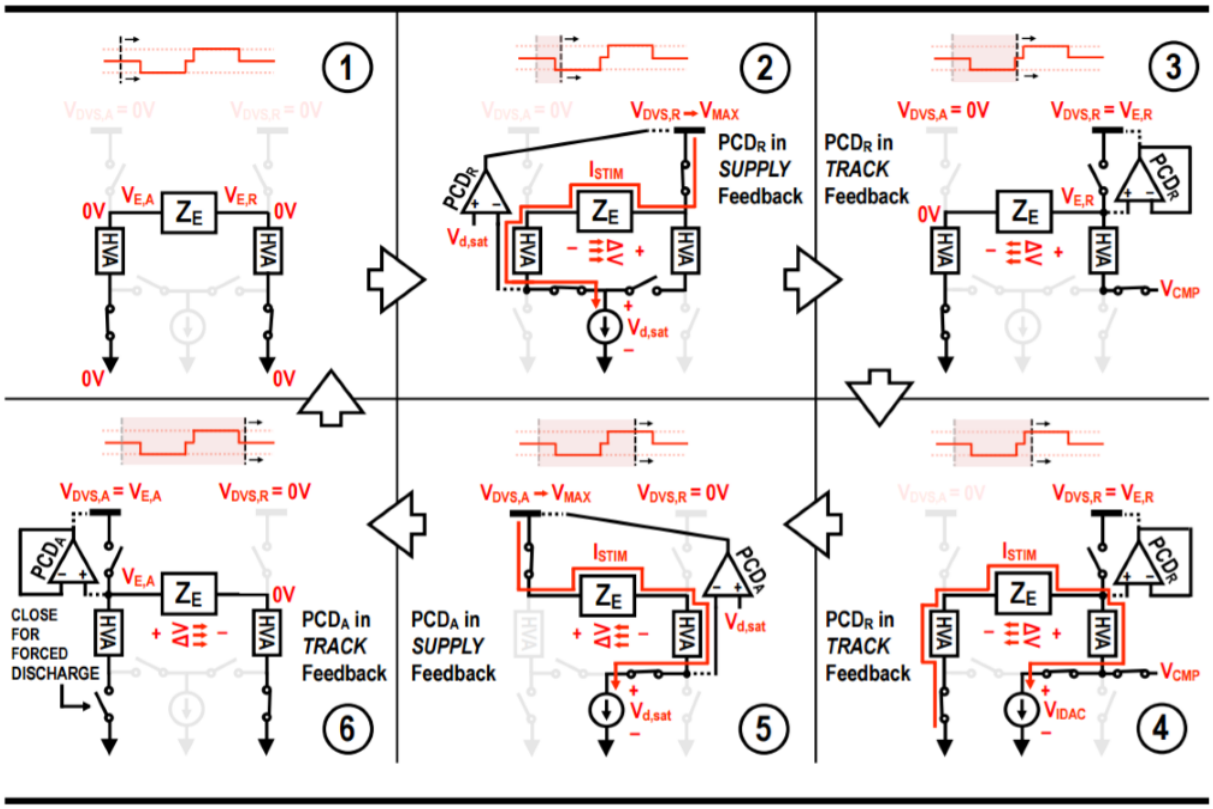


Figure 2-9. H-bridge stimulator state and dynamic voltage supply feedback demonstration.

The HVA circuits are implemented with stacks of 2.5V CMOS devices incrementally biased to accept a full 12V across seven stacked common-gate devices. Capacitive division of the PCD output voltage keeps the entire stack biased and protected during high-voltage stimulation events. The PCD circuits are comparator-based feedback control networks that feed clocks into the DVS. The bandwidth of the feedback architecture is sufficient to track rapid changes in the electrode voltages, such as the near-instantaneous $\frac{\Delta V}{\Delta t}$ presented by a purely resistive load. The DVS is a capacitive charge pump, whose capacitors dominate the chip area. To view the intricate circuit details of the stimulator, see Pepin et al 2016 [23].

Use of a dynamic voltage supply solves one problem fundamental to traditional H-Bridge stimulators, the inherent bias of connected neural tissue to HVDD. In this case, the dynamic supply voltage tracks the necessary ΔV across the electrode-tissue impedance to supply the necessary

stimulation current. In contrast with the stimulation voltage profile shown in Figure 2-4, where the active electrode is driven down from HVDD while the sourcing electrode is held at HVDD, this H-Bridge stimulator follows a voltage profile similar to that shown in Figure 2-10. The resting bias to ground facilitates interaction between this stimulator and DC-coupled recording architectures.

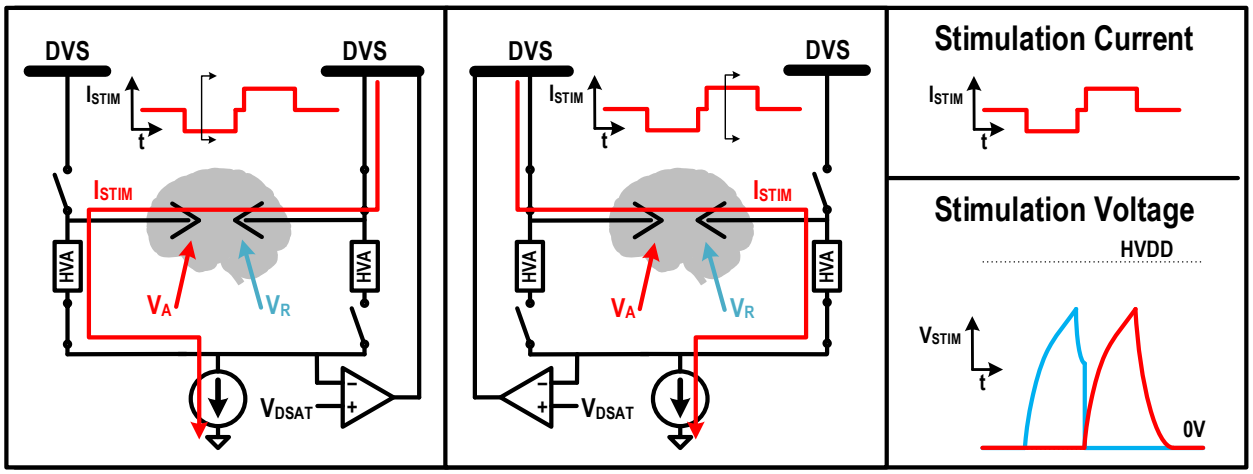


Figure 2-10. Dynamic voltage supply effects on H-bridge stimulator voltage profile.

This stimulator has been used extensively in benchtop and in-vivo tests. Both versions of the stimulator, the first a standalone SoC and the second an integration with the recording and artifact cancellation system, operate robustly and predictably. This is especially important when there is direct electrical coupling between the stimulator and recording electronics. Stimulators that are not well designed and verified have a chance of sourcing or sinking unwanted currents due to unreliable switching architectures. The resulting voltages are unsafe for any in-vivo subject and can also trip the electrostatic discharge (ESD) protection of the recording front end. The stimulator

summarized above has been silicon verified to stimulate at high electrode voltages without reliability issues. A summary of an in-vivo verification experiment is shown in Figure 2-11.

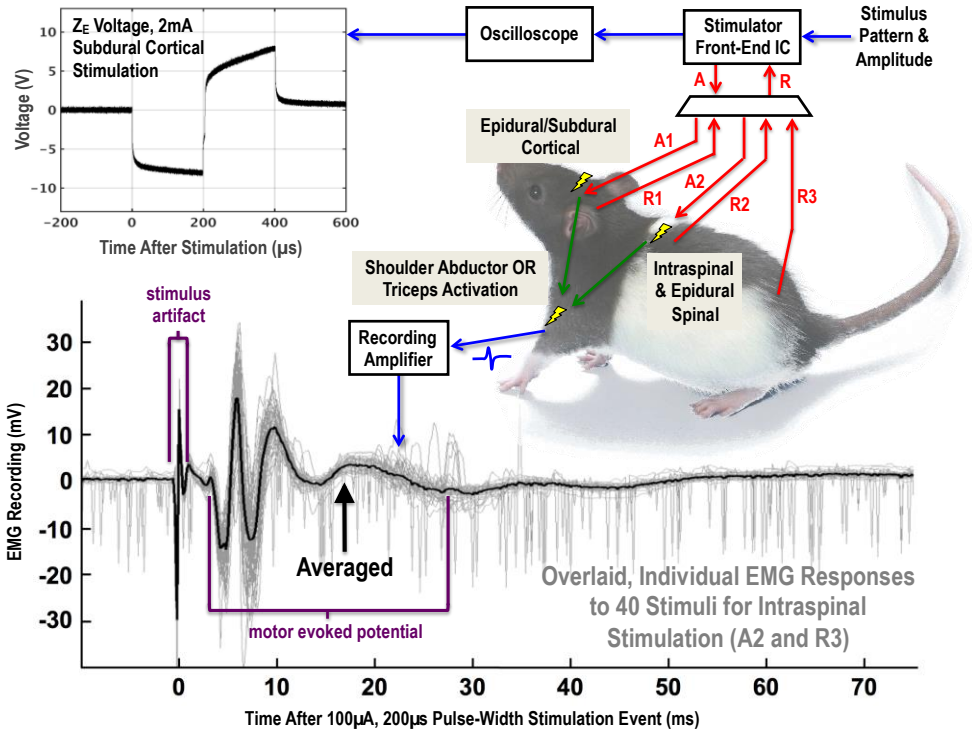


Figure 2-11. In-vivo demonstration of the standalone H-bridge stimulator, including invoked potentials

The standalone H-bridge uses a stack of seven 2.5V charge pumps to generate 2mA of output current at 12V. The flying capacitors of the charge pump stages take up approximately 800µm x 600 µm, as shown in the die photo in Figure 2-12 [23]. The high-density Metal-Oxide-Metal (MOM) capacitors are switched at 108MHz to maintain output voltage while delivering a high stimulation output current (multiple mA). This switching frequency is much higher than typical charge-pump-based stimulators [60], which use large off-chip capacitors, switched in the kHz. The charge pumps in this particular stimulator implementation dwarf the size of other BBCI components such as the recording front-end or digital back-end. The charge pump technique

proposed in this dissertation compresses the entire functionality of the chip shown below into a fraction of the size.

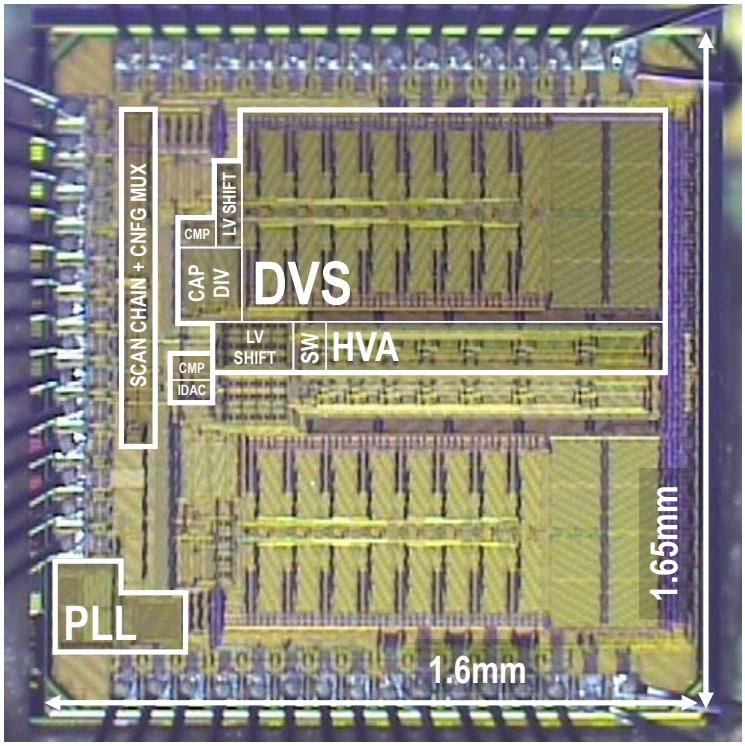


Figure 2-12. Standalone H-bridge stimulator chip (2016) die photo.

Time-Domain Multiplexed Recording Front-End

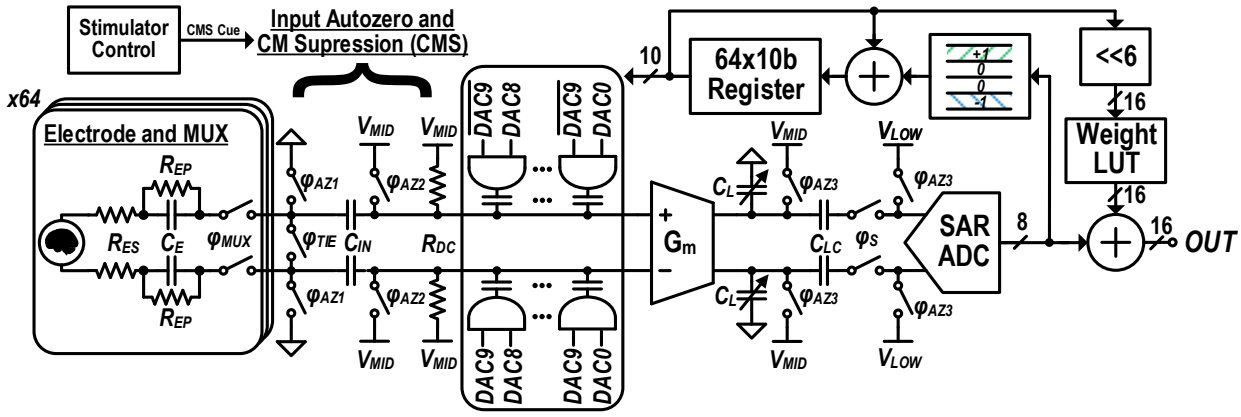


Figure 2-13. Detailed block diagram of the multiplexed recording front-end.

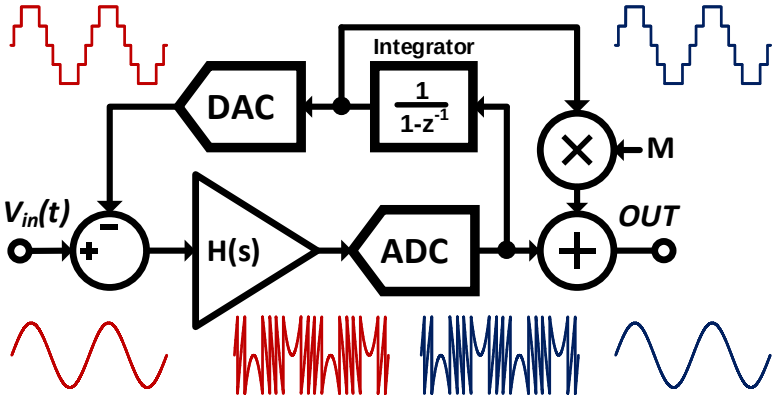


Figure 2-14. Delta-encoding feedback example. Large steps are encoded in the DAC integration look. Small differences are captured by the ADC.

This work also leverages a recording system previously developed by William (Anthony) Smith. The time-domain multiplexed front-end represents the state of the art in minimizing power and area consumption per recording channel [13]. The recording front-end, shown in Figure 2-13, uses digital delta-encoded feedback to relax the noise and dynamic range constraints of the analog subsystems, taking advantage of the 1/frequency² spectral characteristics of neural signals [61]. As the input signal slowly drifts due to large low-frequency signal content, a capacitive DAC adds or subtracts charge from the recording inputs to keep the low-resolution ADC in its dynamic range,

as shown in Figure 2-14. This digital feedback scheme facilitates artifact cancellation by introducing a convenient injection point for subtracting the synthesized artifact, at the point of digital-to-analog feedback, as shown in Figure 2-13. Furthermore, the time-domain multiplexed nature of the front-end can be extended to simultaneous artifact cancellation across many channels.

In 2017, this recording front-end was integrated onto a 65nm CMOS test chip, along with the previously described single-channel H-bridge stimulator, as shown in the die photo in Figure 2-15. The recording front-end and artifact canceller on this test chip had critical issues that prevented full functionality. Breakdown in multiple domains of level shifters prevented communication between the integrated canceller and the recording digital logic.

Regardless, the silicon-proven stimulator topology worked. This allowed us to verify that the analog components of the recording front-end (visible through test buffers) were able to operate during stimulation pulses without through-chip interference or ground bounce. This was one of the primary fears in integrating a high-voltage stimulator with sensitive low-voltage recording circuits.

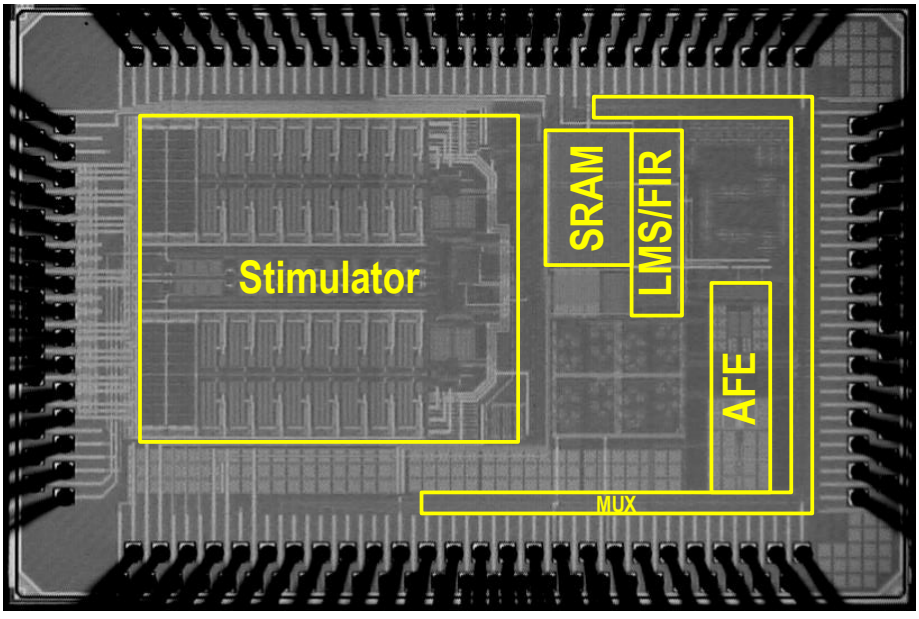


Figure 2-15. 2017 BBCI test chip die photo, 3mm x 2mm.

First Integrated Adaptive Artifact Canceller

The first implementation of the proposed artifact cancellation system was integrated in 65nm bulk CMOS on the die shown in Figure 2-15. The system consists of a full 32-tap adaptive FIR filter with 7 bits of FIR tap depth, time-interleaved adaptation, and operation over 64 independent channels. The artifact canceller contains a dedicated processing block with multipliers and adders for calculating each FIR tap update. Time interleaving is enabled by a custom 14.336-kilobit static random access memory (SRAM) used to store FIR taps. A complete block diagram is shown in Figure 2-16.

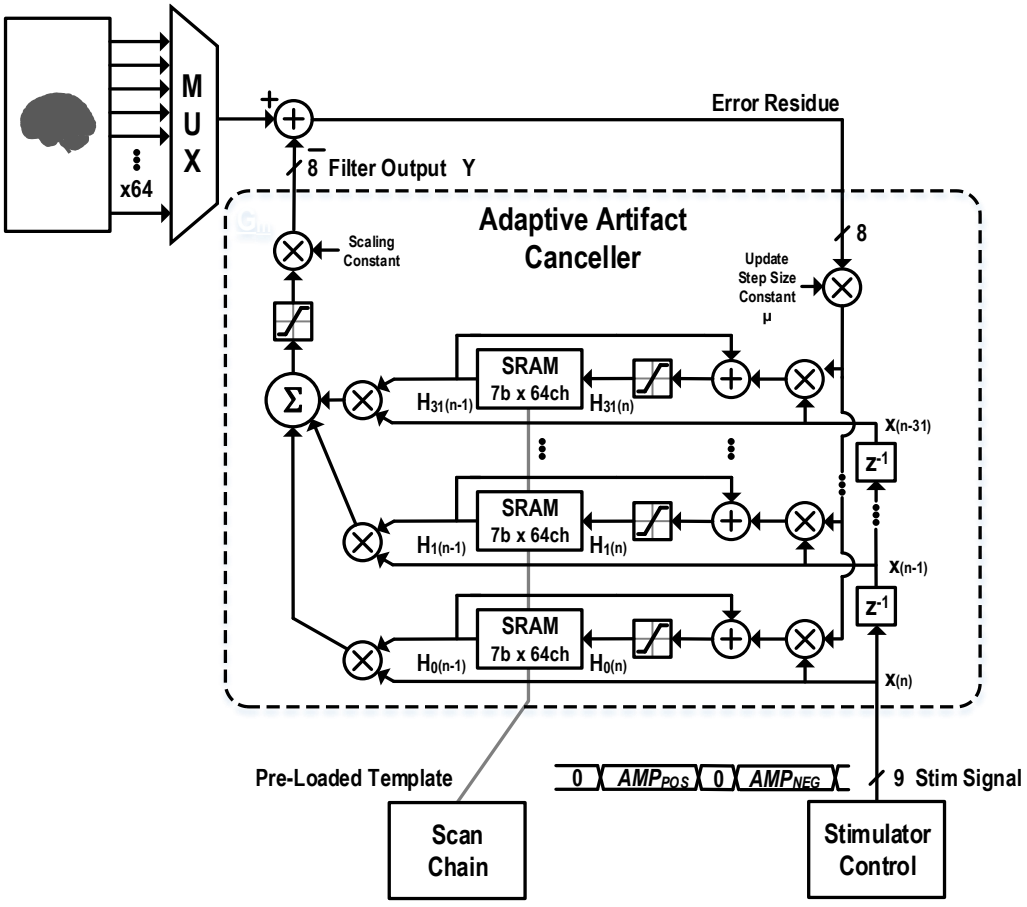


Figure 2-16. Block diagram of first, non-multiplexed integrated artifact canceller.

The heart of the adaptive canceller is the LMS weight update algorithm that estimates the channel response to a given stimulation pulse. In Figure 2-16, the update algorithm is represented by each row of in-line multipliers, adders, saturation blocks, and SRAM modules. In the integrated implementation, each FIR tap was designed with dedicated computation hardware, with 32 weight update modules in total. The block diagram representation above implements the following update function:

$$h_i(n) = \begin{cases} -63 & h_i(n-1) + \mu x(n-i)e(n) < -63 \\ h_i(n-1) + \mu x(n-i)e(n) & -63 \le h_i(n) \le 63 \\ 63 & h_i(n-1) + \mu x(n-i)e(n) > 63 \end{cases} \quad \text{2-1}$$

The weight update and FIR functions are time-interleaved between 64 channels, which is enabled by the dedicated SRAM. By latching the ADC error signal and corresponding input data at the previous interleaving period, the FIR update log has a full 1/128kS/s=7.8125μs to compute, more than sufficient time for the multiplier, adder, and memory write critical path.

The SoC implementation of the LMS algorithm was unable to converge to a stable cancellation solution in noisy neurological experiment environments. On a controlled benchtop with ideal input signals, the input noise power was sufficiently low to allow filter convergence. However, relying on bitwise shift-based division did not allow a small enough step size parameter to mitigate the effects of large transient noise caused by 60Hz interference and physical manipulation of electrodes during an in-vivo experiment. The specific challenges and their solutions are explained in the next section. The FPGA-based prototype addressed this issue with additional noise mitigation methods.

FPGA-based Artifact Cancellation

The first implementation of the artifact canceller was not able to converge to a solution in realistic recording environments. Specifically, stabilizing methods in the filter update algorithm were insufficient to compensate for the large transient noise present experimental conditions. In order to move forward and develop robust artifact cancellation methods, a revision of the integrated recording system enumerated above was fabricated on its own CMOS die. This implementation includes a serializer interface for injection of an artifact cancellation signal into the CDAC data path. This allows rapid prototyping of an off-chip adaptive artifact canceller to test numerous adaptation methods with a real analog interface.

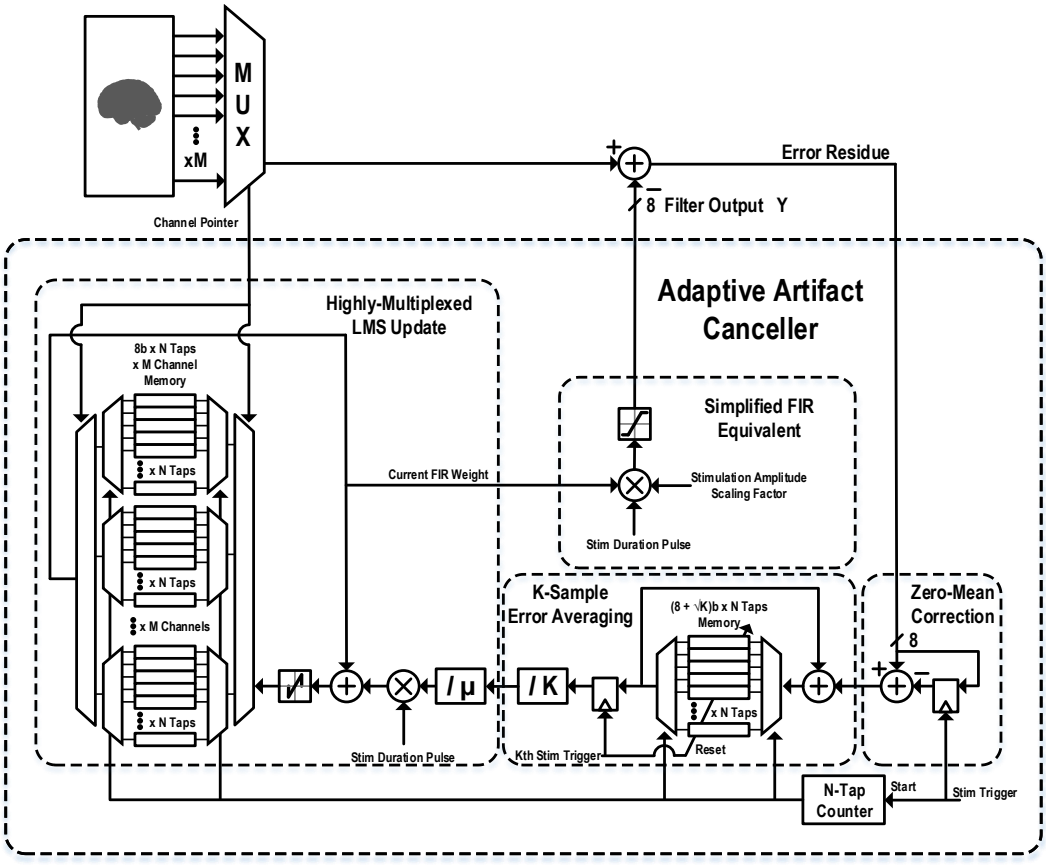


Figure 2-17. FPGA-based adaptive artifact canceller block diagram.

The canceller was programmed using an Altera Cyclone V FPGA. This canceller includes significant improvements in algorithm modularity and several advanced noise mitigation techniques, reducing system complexity and achieving robust LMS algorithm convergence. A functional system diagram is shown in Figure 2-17. Implementation of a digital canceller with rapid prototyping capability allowed the author to test various features to assist artifact canceller stability. These include windowed mean subtraction, multi-sample averaging, and various bit depths in the associated arithmetic. Specific information on the development, analysis, and testing of these methods can be found in [43]. The lessons learned in this prototype filter testing led to the design enumerated in the later chapters.

Chapter 3: Analysis and Derivations

This chapter explores the analysis performed in designing the resonant charge pump stimulator and multiplexed artifact canceller topologies. This analysis includes area and efficiency tradeoffs in the resonant charge pump, derivation of the simplified artifact cancellation algorithm, and stability analysis of the artifact canceller.

3.1 Stimulator Charge Pump Efficiency and Area

This work uses an H-bridge stimulator topology to double the voltage compliance range for a given maximum output voltage. The stimulator output is ground-referenced, and each differential side has a dedicated charge pump to supply positive voltage as needed to each side of the load. A comparator-based negative feedback loop enables the charge pumps to prevent the IDAC from dropping out of (constant current) regulation, generating only as much power necessary to drive current through the tissue-electrode load. A symbolic representation of H-bridge operation is shown in Figure 3-1 (a) and (b). As compared with a fixed-supply stimulator [30], [62]–[64], dynamic voltage supplies save energy when stimulating below the maximum output voltage, as is conceptually illustrated in Figure 3-1 (c).

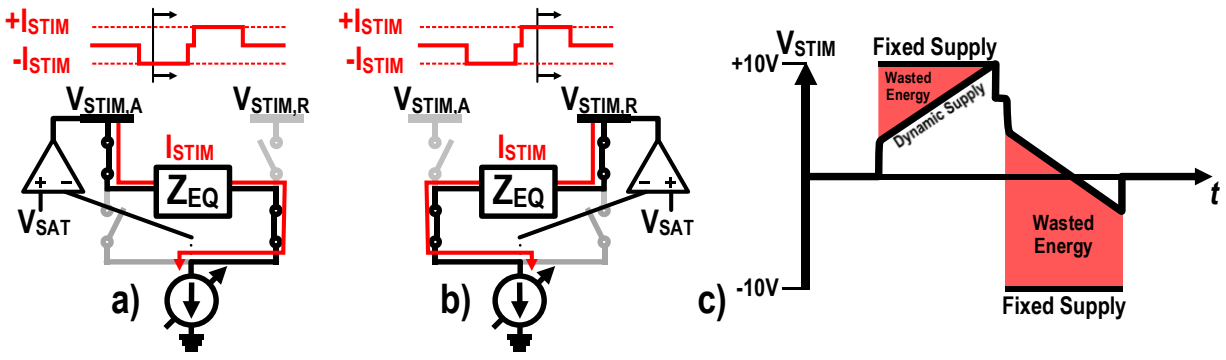


Figure 3-1. H-bridge stimulator interface descriptions. a) H-bridge supplying active current. b) Discharging current pulse. c) Comparison of constant-current stimulation of capacitive loads from a fixed and dynamic voltage supply.

Resonant Charge Pump Voltage Supplies

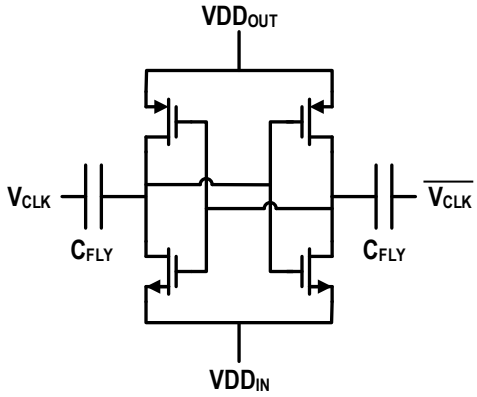


Figure 3-2. Cross-coupled CMOS voltage-multiplier charge pump.

This work uses a modified version of the cross-coupled switched capacitor charge pump presented in [65], which is well suited for use in triple-well, deep sub-micron integrated CMOS processes. The charge pump draws current from an input voltage, V_{IN}, and adds voltage proportional to the number of cascaded stages, n, and the clock voltage swing, V_{CLK}, applied to the flying pump capacitors, C_{FLY} (Figure 3-2). The output voltage, V_O, droops for a given output current, I_O, in proportion to the clock switching frequency, f_{CLK}, and the flying capacitor size at each stage. This gives the following output voltage characteristic:

$$V_O = V_{IN} + n\left(V_{CLK} - I_O/f_{CLK}C_{fly}\right) \qquad 3\text{-}1$$

Switched capacitor charge pumps are typically implemented with large switches and capacitors at low frequencies, mitigating frequency-dependent reactive losses. Milliampere-level stimulation current with clock frequencies on the order of 10s of Megahertz requires large capacitors (~100 pF) in the charge pumps, thus dominating the overall stimulator silicon area.

Existing commercial stimulators often use large (~1 nF) off-chip flying capacitors switched at low frequencies (~1 kHz). This work reduces the silicon footprint dedicated to the charge-pump flying capacitors by increasing f_{CLK} to maintain output power levels while implementing the charge

pump using significantly smaller capacitor sizes. Efficiencies afforded by resonance ensure that the f_{clk} increase does not adversely impact switching losses. A significant reduction in charge-pump capacitance allows for single-chip implementations that include multiple stimulation sites. This work integrates eight resonant charge pumps dedicated in pairs to realize four fully integrated stimulators on a single chip. Each stimulator runs from a 500mV V_{DD} and is capable of independently delivering up to 2mA of current, while ramping to a maximum driver voltage of 11V. During normal operation, the LC tank forms a free-running oscillator, obviating the need for a phased-locked loop.

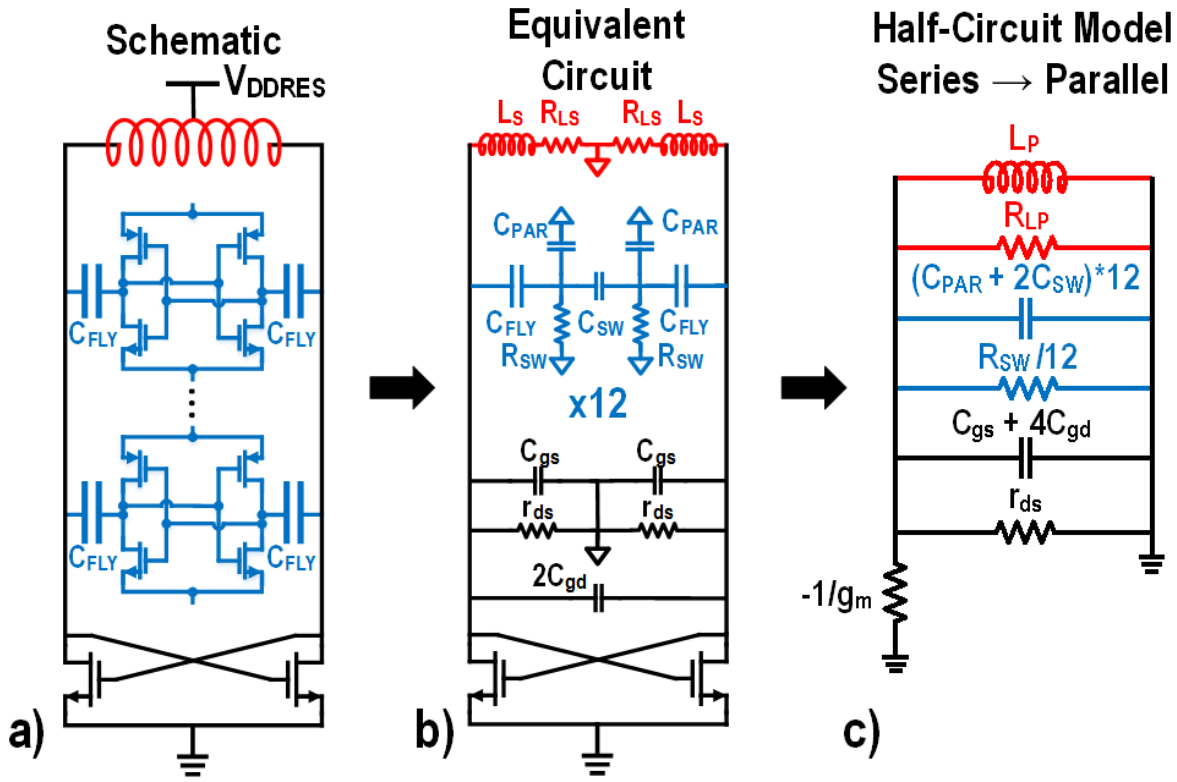


Figure 3-3. Transformation of a) the resonant charge pump schematic into b) an equivalent steady-state model and c) equivalent half-circuit model for efficiency calculations.

The capacitance associated with a twelve-stage cascaded charge pump is placed in parallel with a single differential inductor to create a resonant oscillator, as shown in Figure 3-3. Large, cross-coupled NMOS devices generate a negative impedance, compensating for resistive losses in

the LC-tank to ensure oscillation. An inductor center tap set to V_{DDRES} results in a $2 \cdot V_{DDRES}$ voltage swing at the charge pump clock input. This differential oscillator topology was originally proposed for microprocessor clock generation in [66]. Here, a similar clocking concept is used to drive a capacitive charge pump, as opposed to a clock distribution network. Resonant gate drivers are typically implemented at low oscillation frequencies [67] to maintain high power efficiency. This work optimizes the power efficiency for a severely area-constrained use case, implantable systems.

Optimizing the charge pump in the context of an LC tank requires a steady-state model to estimate the tank quality factor and the resulting charge pump efficiency. Calculating the charge pump efficiency begins by finding the DC current necessary to generate enough negative impedance in the cross-coupled NMOS pair to sustain a free running oscillator. Resonating parasitic capacitances with an inductor mitigates CV^2f losses. As such, the DC bias current of the oscillator drivers and resistive losses in the series charge pump stages dominate the stimulator power loss.

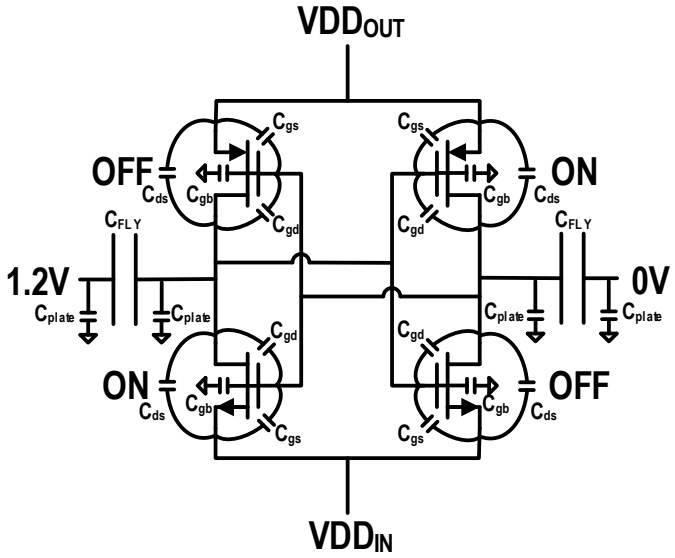


Figure 3-4. Charge pump stage model including device parasitic capacitances ($C_{gs}, C_{gd}, C_{gb}, C_{plate}$).

The steady state model in Figure 3-3 begins with estimation and combination of parasitic capacitances in the voltage multiplier charge pump of Figure 3-2. During steady state operation, it can be assumed that cross-wise PMOS and NMOS devices are on or off at any given time. Figure 3-4 shows a voltage multiplier stage and all parasitic capacitances associated with the charge pump switches. Estimated values for the implemented design are given in Table 3-1.

Parasitic	NMOS ON	NMOS OFF	PMOS ON	PMOS OFF
Cgs	48fF	16fF	96fF	32fF
Cgd	16fF	16fF	32fF	32fF
Cds	12fF	12fF	24fF	24fF
Cgb	16fF	16fF	32fF	32fF

Table 3-1. Implemented switch parasitic values.

The steady-state model in Figure 3-3 (b) assumes that each intermediate node between charge pump stages is an AC ground. Two complimentary switches are "on" at any given time in each stage, this is represented as R_{SW}. C_{FLY} combines in series with the much smaller switch capacitances, so C_{FLY} is not included in this model. The remaining parasitic capacitances are represented by C_{PAR}, which contain the average of both state-dependent gate capacitance (depletion region $C_{gs}^{P,N,OFF,ON}$) and state-independent capacitances ($C_{gb}^{P,N}$, $C_{ds}^{P,N}$, and capacitor bottom plate capacitance C_{plate}). The total capacitance to AC ground, averaged between all clock states, is given by:

$$C_{PAR} = 2C_{plate} + \frac{C_{gs}^{P,OFF} + C_{gs}^{N,ON} + C_{gs}^{N,OFF} + C_{gs}^{P,ON}}{2} + C_{gb}^{P} + C_{gb}^{N} + C_{ds}^{P} + C_{ds}^{N} \quad 3\text{-}2$$

The capacitance between differential clock terminals, C_{SW}, is given by the gate-drain capacitance of the switches:

$$C_{SW} = 2C_{gd}^{P} + 2C_{gd}^{N} \quad \text{3-3}$$

The cross-coupled NMOS devices also introduce their own parasitic resistance and capacitance, represented by r_{ds}, C_{gs}, and C_{gd}.

Transforming the series impedances in Figure 3-3 (b) into a set of parallel impedances yields a simplified expression to calculate the driver g_m. Inductor quality factor used to calculate an equivalent series resistance and transformed into a parallel resistance at the resonant frequency. With all impedances in parallel form, the LC tank can be further simplified into a half-circuit, as in Figure 3-3 (c). Equation 4 results from this model and gives an estimate of the negative impedance necessary to sustain oscillation.

$$g_m > g_{ds} + \frac{R_{LS}\left(12(C_{PAR} + 2C_{SW}) + C_{gs} + 4C_{gd}\right)}{L_S} + \frac{12}{R_{SW}} \quad \text{3-4}$$

The g_m/I_D ratio for a given operating regime and process technology determines the minimum DC current for oscillation. Oscillator startup begins in the subthreshold region, with $g_m/I_D = 25$ in 65nm CMOS. With translation into DC current, Equation 3-4 quantifies oscillator/charge pump efficiency as a function of switch, flying capacitor, and inductor size.

Figure 3-5 graphically represents the resonant charge pump efficiency as a function of inductor size and self-oscillation frequency. The tank resonant frequency includes switch and capacitor sizes via the following expression:

$$f = \frac{1}{2\pi\sqrt{L_S\left(12(C_{PAR} + 2C_{SW}) + C_{gs} + 4C_{gd}\right)}} \quad \text{3-5}$$

The calculated efficiency surface in Figure 3-5 includes the frequency-dependent inductor quality factor, simplified in the above analysis as R_{LS}. The parallel combination of the charge pump with an integrated inductor gives an efficiency peak in the low-GHz.

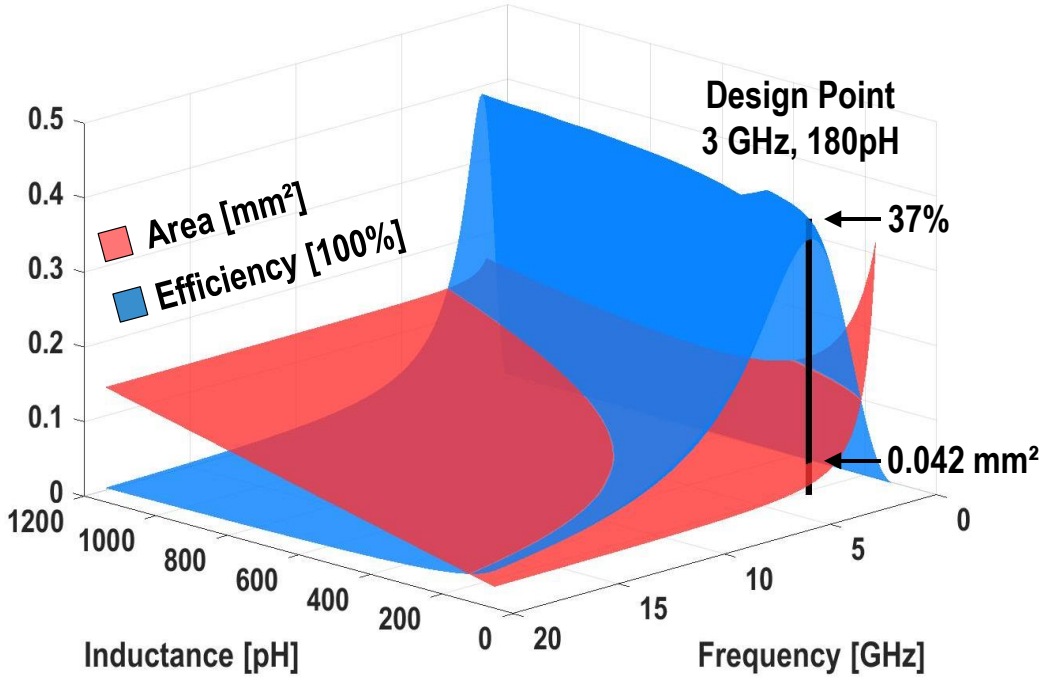


Figure 3-5. Stimulator charge pump area and efficiency over frequency and inductor size. This analysis assumes a constant output current of 2mA at 11V from 12 cascaded stages, with the oscillator center tap drawing current from a 500mV supply. Inductor quality factor, capacitor sizing, and switch optimization are based on PDK models and simulation.

Figure 3-5 also includes an estimate of the overall area occupied by the resonant charge pump. This LC-tank model assumes the flying capacitors and integrated inductors dominate the overall area, and that the switches are sized to ensure the total parasitic capacitance is less than 10% of the flying capacitance. Maintaining this sizing limits clock amplitude reduction arising from series capacitive division.

The implemented resonant charge pump was designed at the minimum area point along the

efficiency peak for various inductor sizes, shown in Figure 3-5. This optimum lies at a 3GHz free-running frequency using a 180pH integrated differential inductor. The 0.42 mm^2 charge pump area estimate matches the silicon area of the actual charge pump (including the inductor) in the fabricated device. The measured DC/DC converter efficiency of 31% has good agreement with 37% power efficiency predicted by the LC-tank resonant charge pump model [12].

Compared to prior work with charge pumps clocked at 100MHz [23], this architecture achieves similar losses in a 6x smaller form factor with a 3GHz charge-pump clock frequency (31% vs 40% efficiency). Using larger, non-integrated inductors with a higher quality factor would enable higher efficiency with this topology, at the expense of larger board form factor.

3.2 ARTIFACT CANCELLATION ALGORITHM DEVELOPMENT

Modern communications technologies use adaptive equalization techniques to predict the characteristics of an unknown channel by observing the response to a known (or predictable), given input signal. In the earliest examples of adaptive channel equalization, the input signal consisted of a modulated sinusoid transmitted over a dispersive, non-linear medium. This was typically a radio-frequency transmission through air from one antenna to another [68]. The channel in this case consists of the direct transmission path as well as reflections off various surfaces. These reflections result in inter-symbol interference (ISI), where a transmitted symbol earlier in time affects the information currently being received. The adaptive equalizer in this case convolves the received signal with an approximation of the transmission channel's inverse transfer function to recover the originally transmitted signal. The inverse channel is approximated by minimization of an optimization function. The techniques developed for communication channel estimation can also be applied to predicting the transmission of stimulation signals through neural tissue. The same approach used to isolate the original signal by attenuating its delayed components can be

extended to attenuate all signals correlated to the stimulation pulse. Additionally, the characteristics of the input stimulation pulse are completely known, allowing for more guided approaches than those typically employed in blind channel estimation [69].

Training an adaptive filter based on a known input signal significantly reduces the computational complexity of the adaptive algorithm. However, estimating the channel response of neural tissue based on periodic stimulation pulses will create a trained set of filter coefficients that includes any signal content co-periodic with the stimulation pulse frequency. This can be problematic when studying responses to stimulation in the neural tissue that occur shortly after the stimulation pulse. Essentially, the canceller would zero out any input voltage that is correlated with stimulation pulses. This attribute of guided filter training creates two conditions for the filter to prevent cancellation of desired signals. First, the recording front-end and canceller combined must be able to cancel the artifact immediately after the stimulation pulse. This allows limiting of the pulse length in time and the number of adaptive filter taps to not overlap responses happening shortly after stimulation. Second, guided artifact cancellation is best suited for use with open-loop recording front-ends, where recovery from large voltage artifacts at the input occurs by the next time-domain sample.

The adaptive filter in this work most closely resembles a Decision Feedback Equalizer (DFE), where a decision function evaluates the equalizer output and updates filter coefficients to converge to a goal [70]. Figure 3-6 shows the DFE architecture in the context of cancelling neural stimulation artifacts. The stimulator creates a current waveform that propagates through the electrode-tissue "channel," where it is converted to voltage with an unknown transfer function. Noise is also added in the form of neural signals, electrode noise, and circuit noise. The resulting signal is denoted $\bar{x}(n)$. The ideal digital representation of the stimulation waveform, $x(n)$, is used

as the input of the FIR filter and as a guide in the coefficient update algorithm. The output of the FIR equalizer, $y(n)$, is a convolution of the input signal $x(n)$ and the adaptively updated set of coefficients, $h(n)$, given by $y(n) = \sum_{i=0}^{N} h_i x(n-i)$. The error signal is a subtraction of the filter output from the channel output, given by $e(n) = \bar{x}(n) - y(n)$. Note that the error signal seen by the coefficient update algorithm is subject to saturation and other recording system non-idealities.

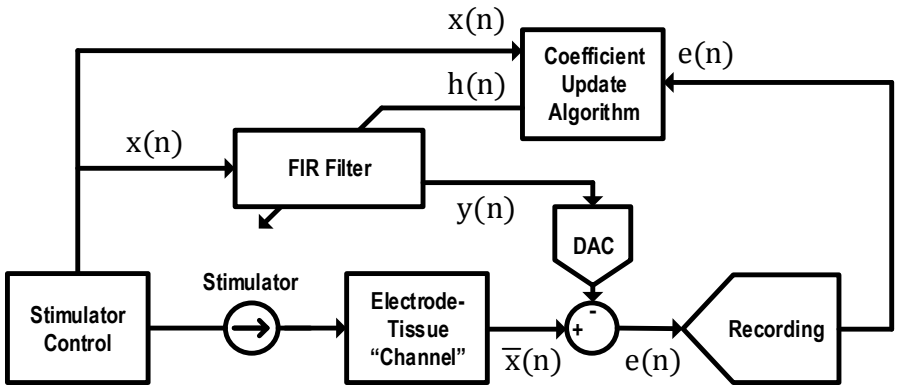


Figure 3-6. Adaptive equalizer block diagram.

Least Mean Squared Error Minimization

The least mean squared (LMS) adaptation method was first developed in the early 1960's in Bell Telephone Labs by Floyd Becker, Erich Port, and Robert Lucky [71]. This method of filter coefficient estimation is widely used for its quick convergence, ease of implementation, and high noise tolerance. In its simplest form, the LMS update algorithm is given by:

$$h_i(n+1) = h_i(n) + \mu x(n-i)e(n) \qquad 3\text{-}6$$

This update algorithm assumes a known input signal, $x(n)$ (digital representation of the stimulator input current). μ is a scaling factor that affects stability and convergence. This algorithm, upon sufficient stability criterion, will cause the decision feedback equalizer to

converge to a solution that minimizes the sample-by-sample error, $e(n)$. This translates to suppression of all voltage artifact components correlated with the stimulator input current.

Stability and Convergence of the Basic LMS Update Algorithm

Ensuring that an adaptive equalizer will converge to the optimum solution is a matter of tuning the step-size parameter, μ, to match the error signal power. In the sample-by-sample example that was just enumerated, it is difficult to analyze the statistics of convergence, as the coefficient update algorithm is a highly non-linear system. However, by abstracting the update to arbitrarily small step sizes over an infinite number of averaged samples, general properties emerge.

To categorically ensure convergence, the step-size parameter must be chosen so that it is the inverse of the product of the total normalized error signal power and number of filter taps. The error signal power in this case includes both the channel response correlated to the input signal and all additive noise. The normalized maximum captures the maximum transient error magnitude with respect to the average error power magnitude. The derivation in [72] assumes a continuously non-zero input function, so all N taps of the filter contribute to the output, and an increasing number of taps engaged at once contributes to algorithm instability. This leads to the convergence criterion [68], where the integration period, T, defines the known set of error values:

$$\mu\, N \max \left| \frac{e(n)^2 \cdot T}{\int_{-\frac{T}{2}}^{\frac{T}{2}} e(n)^2} \right| \leq 1 \qquad 3\text{-}7$$

It follows that smaller update step sizes are required for increased noise or signal power. This will always slow convergence. In systems with limited computational accuracy, the divisions made necessary by very small update step sizes alters this ideal convergence criterion. Truncation

of less-significant bits and digits can cause overshoot or undershoot in the weight update step, hindering convergence speed and stability.

The update algorithm can be further simplified by limiting the amount of information known about the input signal and the error signal. The numerical accuracy of $x(n)$ and $e(n)$ can be limited to only contain information about signal polarity. This slows convergence speed but grants a degree of noise immunity and reduces computational complexity. These methods are called the sign-data or sign-error LMS algorithms. By thresholding the input signals to sign information, MSE and noise must take up the full range of the input quantizer to cause stability issues.

Scalability and Efficiency

Even in its most limited form, the LMS algorithm still involves several multiplications, additions, and a division, non-negligible computations in custom digital blocks. These operations must be performed multiple times for each weight update iteration, which may happen at frequencies approaching 1MHz. An example of the computational complexity necessary for a fully adaptive FIR filter is given by the block diagram in Figure 4-5. Each filter tap requires four multipliers, two adders, and multiple memory elements. Storing enough information to cancel millisecond-long artifacts for many, many channels then becomes a considerable task of memory management. This work implements a simplified adaptation algorithm that can be scaled between CMOS processes, operating frequencies, and increasing channel counts.

Chapter 4: Implementation Details

A block diagram of the full system implemented is shown in Figure 4-1. Four integrated H-bridge stimulators are independently tunable with digitally programmable current waveforms. Resonant charge pumps generate up to 11V to drive up to 2mA of sink-regulated current through the electrode-tissue load. The shared IDAC is switched between the two sides of the H-bridge.

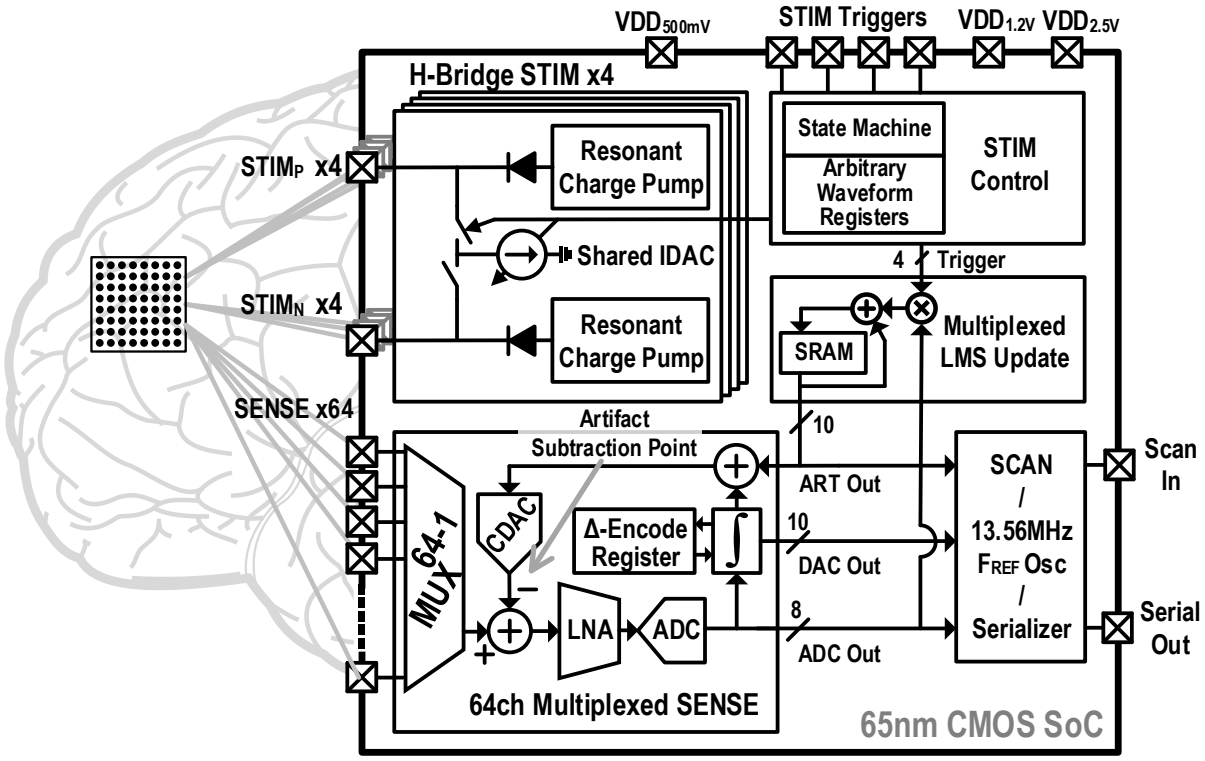


Figure 4-1. Functional block diagram of the BBCI chip architecture.

A time-multiplexed, delta-encoded recording front-end [13], [14] records 64 channels using a single recording chain. A multiplexer routes all channels to a shared input capacitive DAC (CDAC), front-end amplifier, and SAR ADC. A digital integration loop increments the CDAC at the recording amplifier input to subtract low frequency signal content. Such a delta-encoded loop creates a frequency-shaped dynamic range well suited for the colored spectral shape of neural signals [61]. The system targets 64-channel electrocorticography recordings at 2kS/s.

The digital back-end implements an adaptive artifact cancellation filter. A simplified Least Mean Squared (LMS) algorithm processes recording output and stimulator control signals into a time-domain reconstruction of unwanted stimulus artifacts. The artifact voltage is subtracted using the CDAC at the recording amplifier input. The canceller computation hardware associated with adapting the filter is time-multiplexed between channels, and the filter coefficients are stored using an on-chip dedicated SRAM.

The particulars of each constituent subsystem will now be described in detail.

4.1 RESONANT CHARGE-PUMP-BASED H-BRIDGE STIMULATOR

The resonant charge pump described in Chapter 3.1 fits into the H-bridge architecture as shown in Figure 4-2. The H-bridge switching structure is formed with diodes and distributed current buffers to overcome the low, 1.2V voltage tolerance of individual CMOS devices.

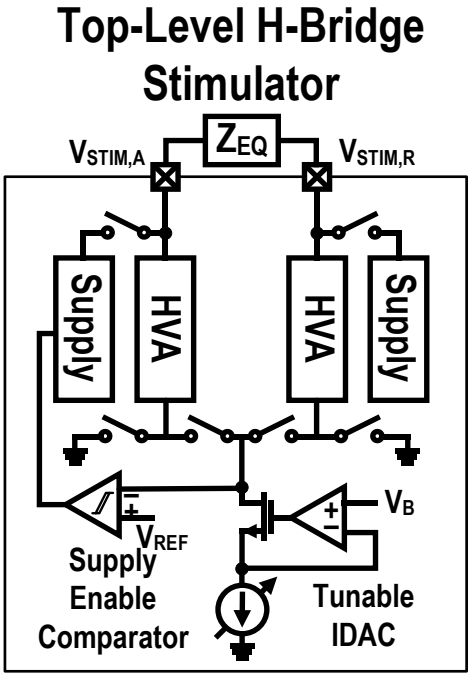


Figure 4-2. H-bridge stimulator top-level block diagram.

The high side switches are implemented with deep N-well diodes. Dynamically controllable

charge pumps allow the diodes to be selectively forward biased to source current. Discharging the pumps reverse biases the diodes and turns the switches (diodes) "off." Capacitive dividers at each side of the diode level shift the stimulator output swing to a low-voltage comparator, which detects and ensures the diode is reverse biased. The tracking detector circuit and detailed charge pump configuration is shown in Figure 4-3.

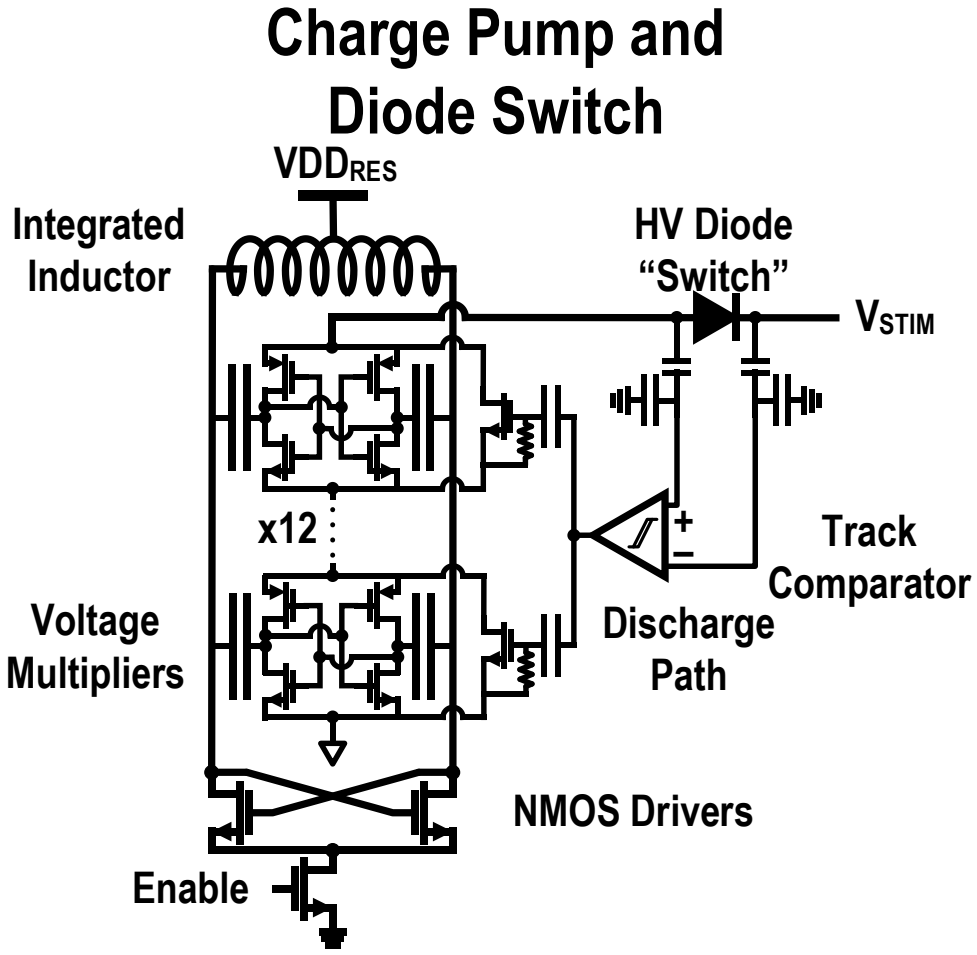


Figure 4-3. Detailed charge pump and high side switch schematic.

While one side of the H-bridge supplies voltage across the electrode-tissue interface, current flows through a high-voltage adapter (HVA) into the current-controlling IDAC. A schematic of the HVA is shown in Figure 4-4. The HVA is a multi-stage cascode operating as a current buffer, protecting the 1.2V IDAC from large voltages as seen at the stimulator-electrode interface. The

charge pump output voltage is capacitively distributed across the cascode gates to ensure no transistor sees more than 1.2V across its terminals. The HVA also allows current to sink from the positively charged side of a capacitive electrode-tissue load, after reversal of the stimulus current.

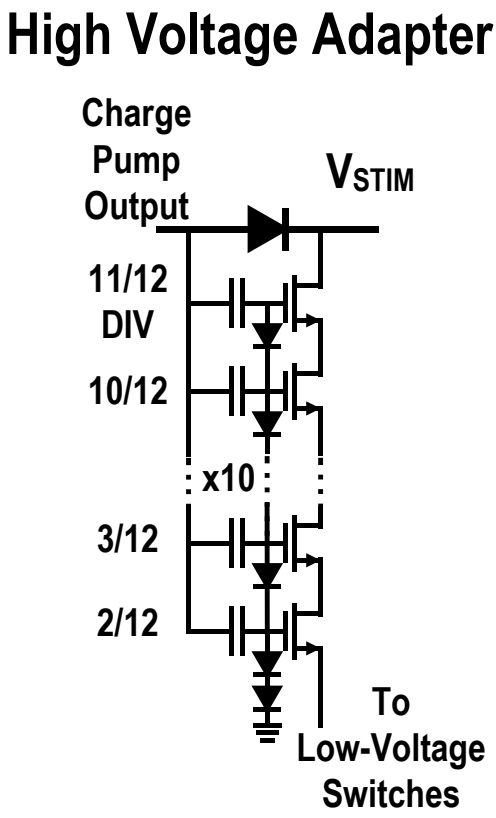


Figure 4-4. Detailed high-voltage adapter (HVA) schematic.

The sinking IDAC has 8 bits of resolution with a tunable least significant bit, nominally 10μA. An active cascode at the IDAC output provides a high output impedance of 600 MΩ (simulated). A comparator above the active cascode compares against a dropout reference voltage. Charge pumps are selectively enabled based on this comparison when the IDAC approaches a voltage where the current will no longer be constant (e.g. devices in the IDAC go into triode). This comparator feedback loop improves efficiency by enabling the charge pumps just enough to drive current through the load.

4.2 MULTIPLEXED ADAPTIVE ARTIFACT CANCELLER

Figure 4-5 shows an adaptive canceller algorithm where finite impulse response (FIR) filter coefficients are adapted using a least-mean squared (LMS) algorithm. For a FIR-based canceller implementation, the filter input signal, $x(n)$, is a time-domain representation of the stimulation current pulse. This input is convolved with a set of coefficients, $\{c_0, c_N\}$ to create the filter output, $y(n)$. The coefficients are trained based on the recording system output, $e(n)$, which is the residual artifact and neural signal remaining after subtracting the FIR filter output from the input signal, $y'(n)$. The FIR coefficients can be trained with an LMS algorithm, where the update coefficient, μ, tunes the step size at each update interval. The notation for a full FIR-based LMS algorithm is given below:

$$c_N(n+1) = c_N(n) + \mu\, e(n)\, x(n-N) \qquad 4\text{-}1$$

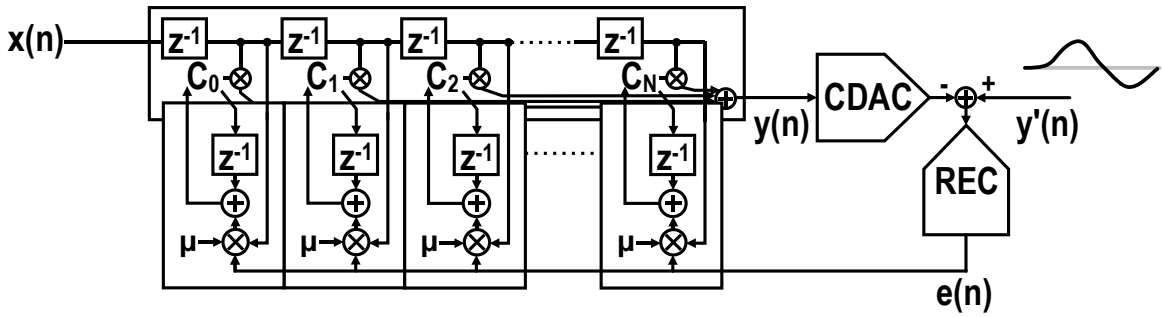


Figure 4-5. Behavioral block diagram of a full LMS-based artifact canceller

Implementing the full LMS/FIR adaptive filter shown in Figure 4-5 requires power and area-intensive hardware. Each tap of the FIR filter requires two multipliers, two adders, and two delay cells. This cost is multiplied by the number of implemented filter channels. This work proposes a simplification of this adaptive filter that dramatically reduces the necessary hardware for similar functionality and performance across multiple channels.

The Impulse-based Adaptive Filter

The end-goal of the adaptive filter is a time-domain representation of the stimulation voltage artifact. The FIR coefficients in the previously described approach are an intermediate step, quantifying the channel which changes stimulator output current into the voltage artifact at the recording channel input. This intermediate step can be removed by changing the filter input into a discrete delta function. The FIR coefficients can be trained to a time-domain representation of the artifact voltage waveform, with several added benefits: most multiplicands become unity, the update hardware can be multiplexed, and the tapped delay line can be removed.

With a discrete delta input signal propagating through the FIR filter, only one tap of the filter is active at a time. This removes the need for a sum at the filter output. Additionally, the multiplication of each tap coefficient with the delayed filter input, $x(n)$, is replaced with multiplication by zero or unity as the discrete impulse input propagates through the filter. The LMS update hardware is similarly only updating one coefficient at a time in this implementation.

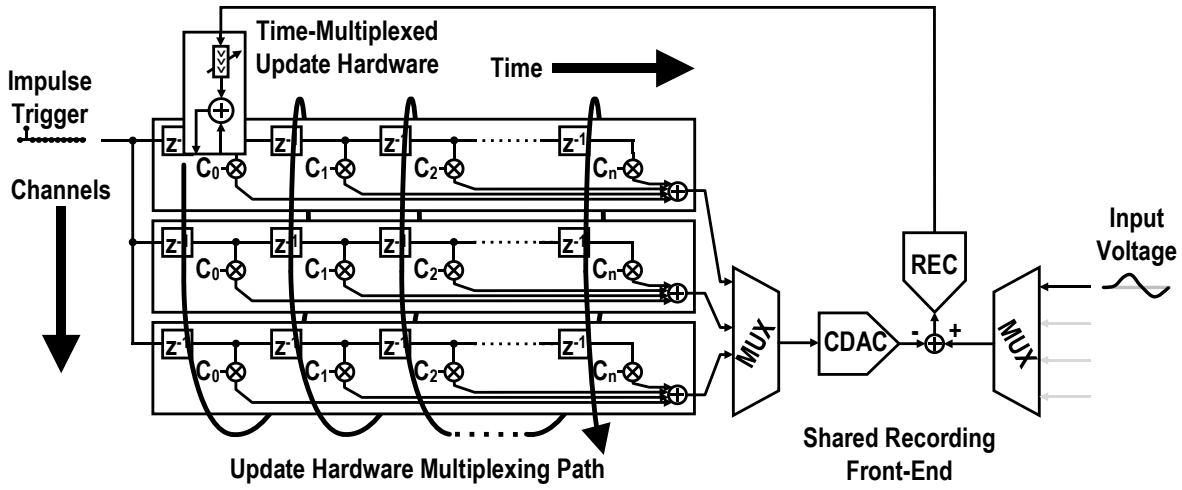


Figure 4-6. Demonstration of artifact canceller multiplexing in the context of a full FIR-based adaptive filter.

Given the high-speed logic available in scaled CMOS and the low sampling frequencies necessary for adequately representing neural signals, it is possible to time-domain multiplex *one set of LMS update hardware between all filter taps*. Furthermore, the time-domain multiplexed recording architecture lends itself well to the multiplexing of filter hardware between multiple stimulation-recording channel pairs. A representation of this multiplexing is shown in Figure 4-6. While the filter coefficients are adapting, the scaling of the error signal used in LMS adaptation is simplified to a division via a bitwise shift. The update operation first rotates through the recording channels before progressing down the time-domain taps of the impulse response filter, as indicated by the helical spiral in Figure 4-6. Somewhat noteworthy is the fact that although the adaptation hardware is being reused between different channels, the filter response for each stim-sense combination is adapted uniquely. Each artifact produced at one stimulation site propagates to each recoding site and has a unique artifact response and a dedicated set of coefficients. The distribution of unique stored artifact values is illustrated in Figure 4-7.

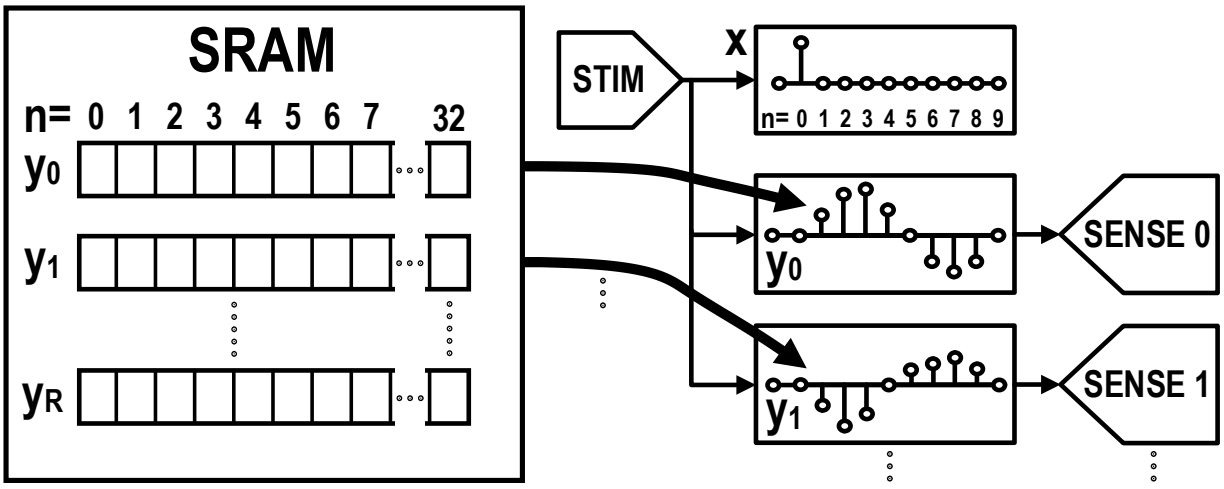


Figure 4-7. Translation of SRAM values to multiple channels and time samples.

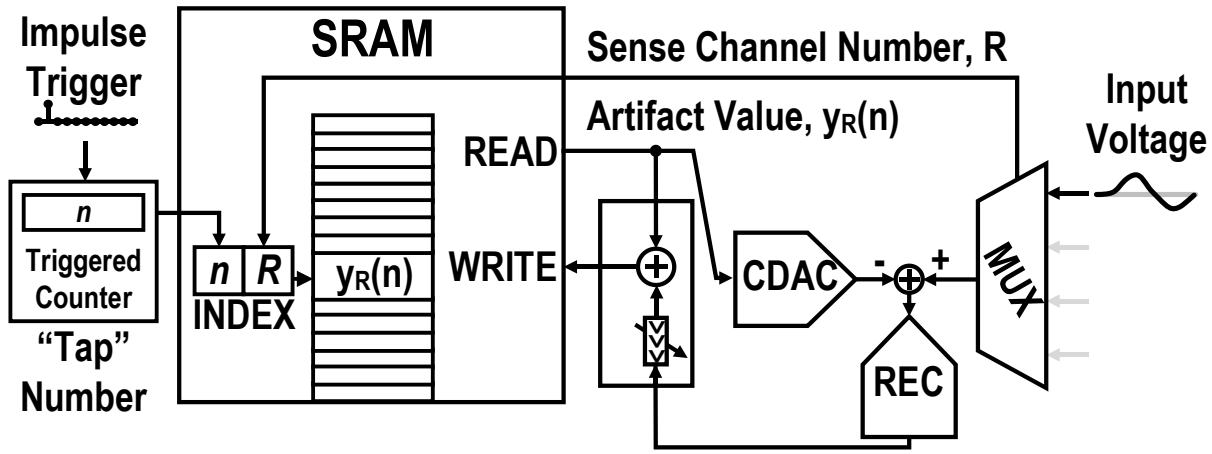


Figure 4-8. Implemented lookup-based adaptive filter architecture.

The filter can be further simplified to remove the tapped delay line. Only one tap is active at a time, so the only functionality required is the storage and recall of filter values. This work uses a writable lookup table to replace the FIR filter, removing the power-consuming delay line. An integrated SRAM stores filter values, which are indexed by the filter tap number and recording channel, shown as $y_R(n)$ in Figure 4-7. The previously stored coefficient for a given index is read out of the SRAM to an update operation block and written back for storage until the next sample. The overall architecture of the lookup-based topology can be seen in Figure 4-8.

The four stimulators operate independently, so multiple artifacts can overlap on the same recording channel. In order to accommodate overlapping artifacts, canceller hardware is physically multiplexed for the four stimulators, while it is time-domain multiplexed across recording channels. This work implements four separate canceller back-ends, one for each stimulator, with each time-domain multiplexed between four recording channels. The CDAC sums all four canceller outputs before subtracting from the input. This operation assumes that overlapping artifacts linearly superimpose.

When processing recording data at 2kS/s for 16 stim-sense pairs with 40 stimulation pulses per second, the canceller dissipates a total of 780nW, or ~50nW per channel. In contrast, the full LMS

method in [73], with multipliers for each filter tap, dissipates 910nW per channel.

The adaptive artifact cancellation hardware readily scales with the number of recording channels by simply expanding the amount of SRAM integrated on chip. This implementation includes reconfigurable on-chip memory for 16 possible stim-sense artifact combinations, each with 32 10-bit taps. The 5120-bit low-voltage custom SRAM occupies 250µm x 300µm. The canceller can also interface with off-chip memory through source-synchronous serialized communication.

The artifact cancellation depth is limited by the digital-to-analog interface. In this work, a 10-bit CDAC gives a possible 60dB of cancellation with a ±125mV full scale. Additional off-chip post-processing can achieve increased cancellation depth above the 60dB provided by this chip.

Chapter 5: MEASUREMENT RESULTS

The proposed system was fabricated in TSMC 65nm LP 1P9M CMOS and evaluated both on the bench and *in vivo.* These *in vivo* measurements were performed in ketamine-sedated macaque monkeys with silicon Utah Arrays (Blackrock Microsystems, Salt Lake City, Utah) or platinum-iridium microwire electrodes chronically implanted in motor cortex. Benchtop measurements involved emulating the electrode-tissue load using discrete resistors and capacitors. Resistive dividers translate stimulator output voltage to a differential artifact voltage, coupled into the recording inputs with various test tones. The bench test configuration is shown in Figure 5-1. The impedances were selected to replicate a microwire electrode array.

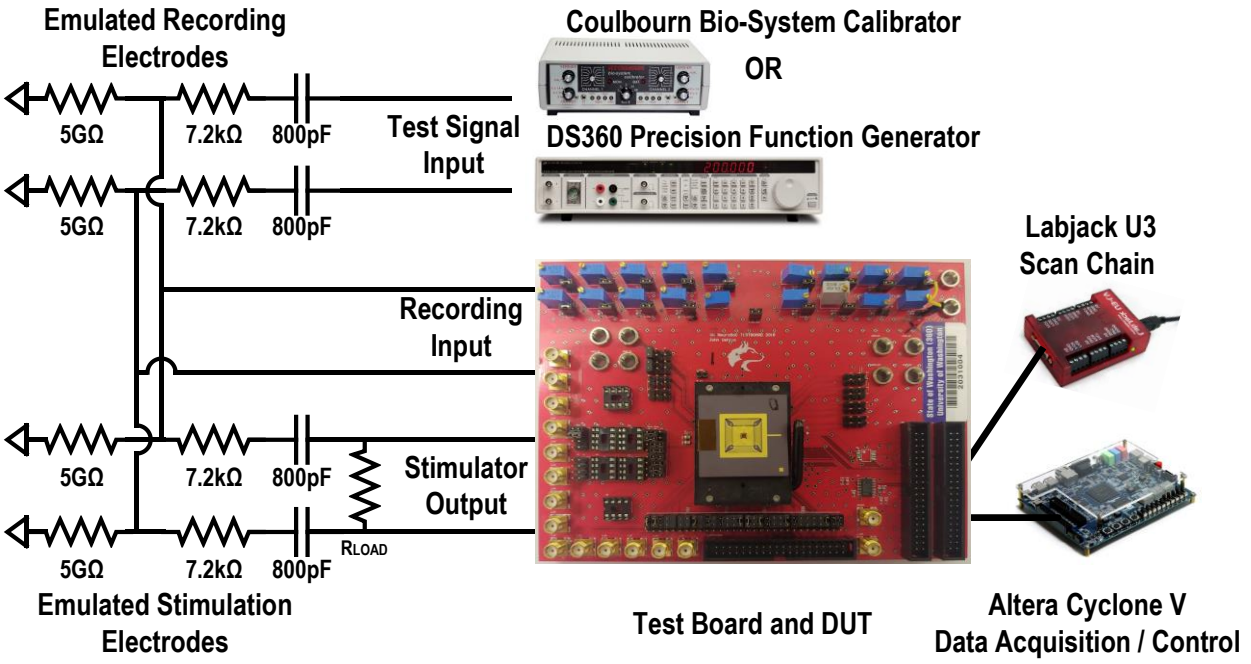


Figure 5-1. System verification and measurement setup. Emulated electrode loads couple test signals to the on-chip recording inputs along with artifacts generated by the on-chip stimulator. The electrode model is altered to DC bias the recording input to ground; the 5GΩ resistors are shunted to ground rather than in parallel with the model capacitance.

The resonant stimulation driver topology has a measured ±11V voltage compliance while driving up to 2mA of output current. The stimulator charge pumps have a measured 31% power

efficiency while delivering maximum output current (2mA, 11V), as shown in Figure 5-2. Transient-domain demonstration of the H-bridge output voltages is shown in Figure 5-3 with 10μs-wide, 2mA constant-current pulses sent into a 5kΩ load.

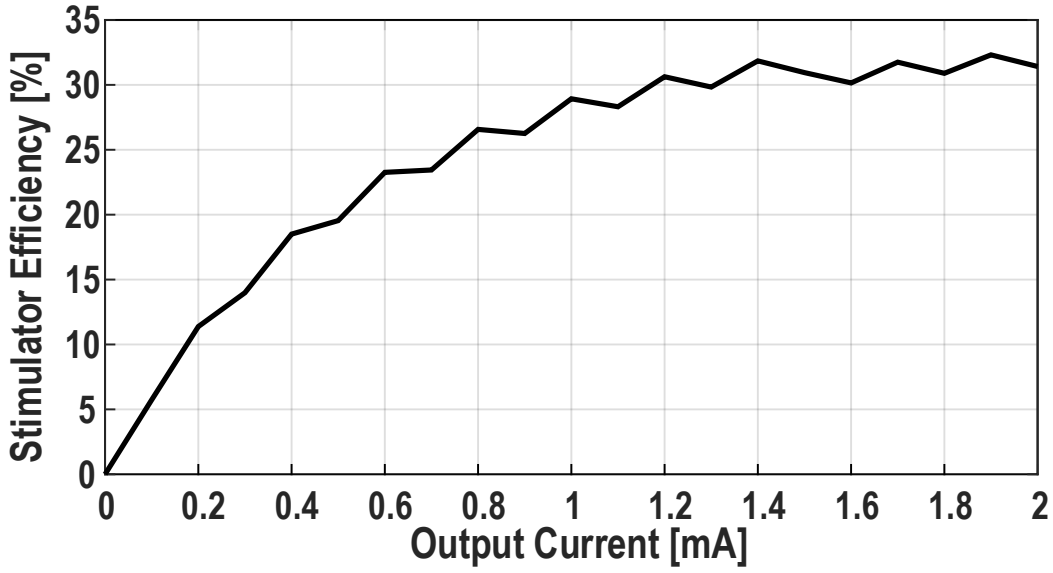


Figure 5-2. Measured charge pump power efficiency, operating with DC output currents.

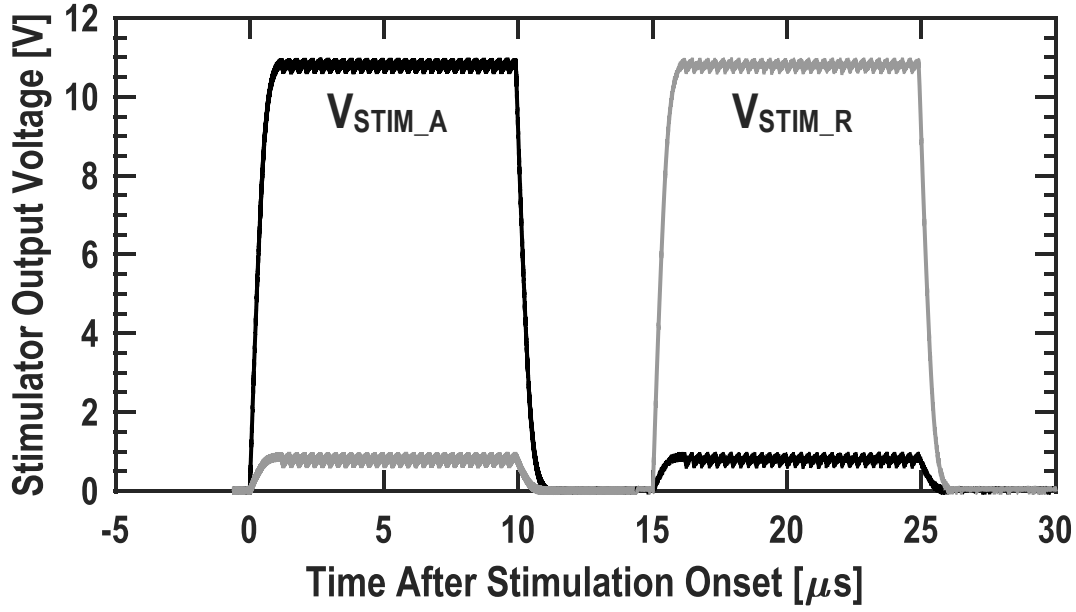


Figure 5-3. Demonstration of stimulator transient performance. 2mA constant-current pulses into a 5kOhm resistive load.

A bench demonstration of multi-channel stimulation and the ability of this chip to deliver programmable current shapes is shown in Figure 5-4. The four stimulators were programmed to produce the following current wave shapes: 1) rising exponentials 2) half-sines 3) square waves 4) decaying exponentials. Stimulation with non-constant-current waveforms changes the frequency content of the injected pulse and how much energy propagates through the high-pass neural tissue. This lessens artifact amplitude for current pulses with spectral content concentrated at low frequencies. This concept is a hypothesis based on literature [74], and is yet to be verified.

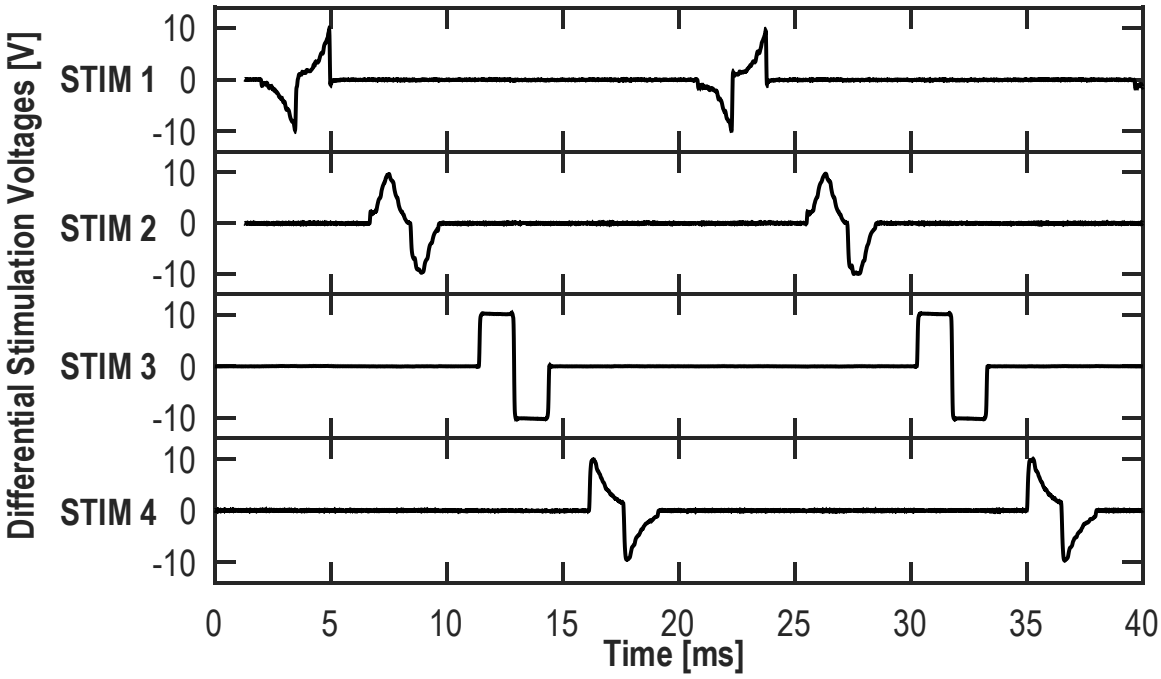


Figure 5-4. Measured output waveforms of all four stimulators concurrently delivering peak currents of 2mA with equal 5kΩ resistive loads. Stimulator current waveforms programmed with the following shapes: 1) rising exponentials 2) half-sines 3) square waves 4) decaying exponentials.

The measurement shown in Figure 5-5 illustrates artifact suppression *in vivo*. Recordings are shown of local field potentials (LFPs) in the motor cortex of a sedated non-human primate with a bandwidth of 10 Hz to 1 kHz. Recordings are shown (a) without stimulation, (b) during stimulation

without artifact suppression, and (c) during stimulation with artifact suppression. Biphasic, differential stimulation of ±150µA at 5 pulses per second were applied to differential microwire electrodes 2mm away from differential recording electrodes on the same array. Evoked potentials are seen in response to many of the stimulus pulses, but the magnitude of these physiological potentials is much small than the stimulus artifacts." ±50mV differential artifacts were observed at the recording channel input via oscilloscope, which the canceller suppresses to within ~100µV at the recording amplifier input. Note that artifacts in Figure 5-5 (b) are subject to recording front-end saturation, reducing the post-recording amplitude to ~±2mV.

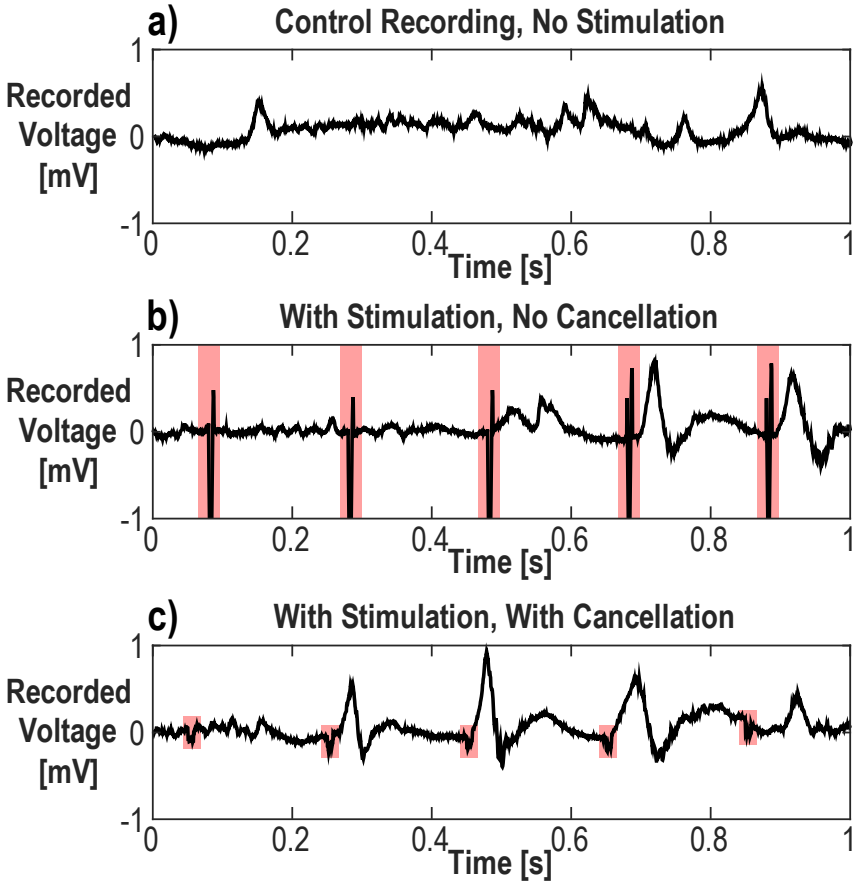


Figure 5-5. Measured in-vivo local field potential recordings a) without stimulation-evoked potentials, b) with stimulation-evoked potentials and artifacts, and c) with stimulation-evoked potentials and cancelled artifacts.

Figure 5-6 shows an example of filter convergence and cancellation of full-scale artifacts with bench recordings at 2kS/s. A ±125mV artifact was generated at 40 pulses/s using the on-chip stimulator driving an emulated electrode-tissue load (as in Figure 5-1). This artifact was combined with a 10µV, 50Hz test tone. Figure 5-6 (a) shows the full convergence progression. Figure 5-6 (b) shows the saturated artifact and the beginning of filter training during the first 200ms after reset. Figure 5-6 (c) shows the recording and filter output after convergence. The power spectral density (PSD) plot in Figure 5-7 shows signal integrity after artifact cancellation through the preservation of the 10µV, 50Hz test tone in the presence of full-scale artifacts.

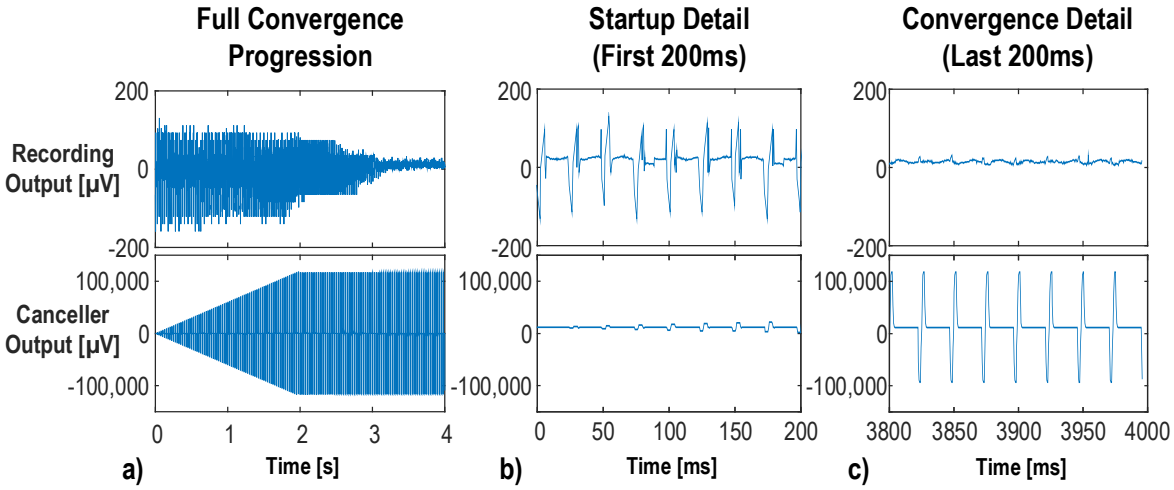


Figure 5-6. Bench measurements of closed-loop artifact canceller convergence, with ±125mV artifacts at 40 pulses/s coupled with a10µV, 50Hz sine wave. a) Convergence to a ±125mV input-referred artifact within 120 stimulation pulses. b) Detail of the first 200ms after reset. c) Detail of the last 200ms after convergence.

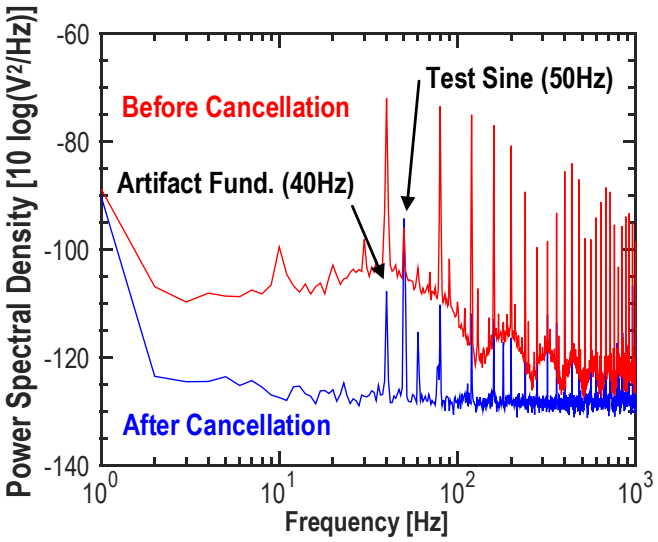


Figure 5-7. Power spectral density of recording output before cancellation and after cancellation.

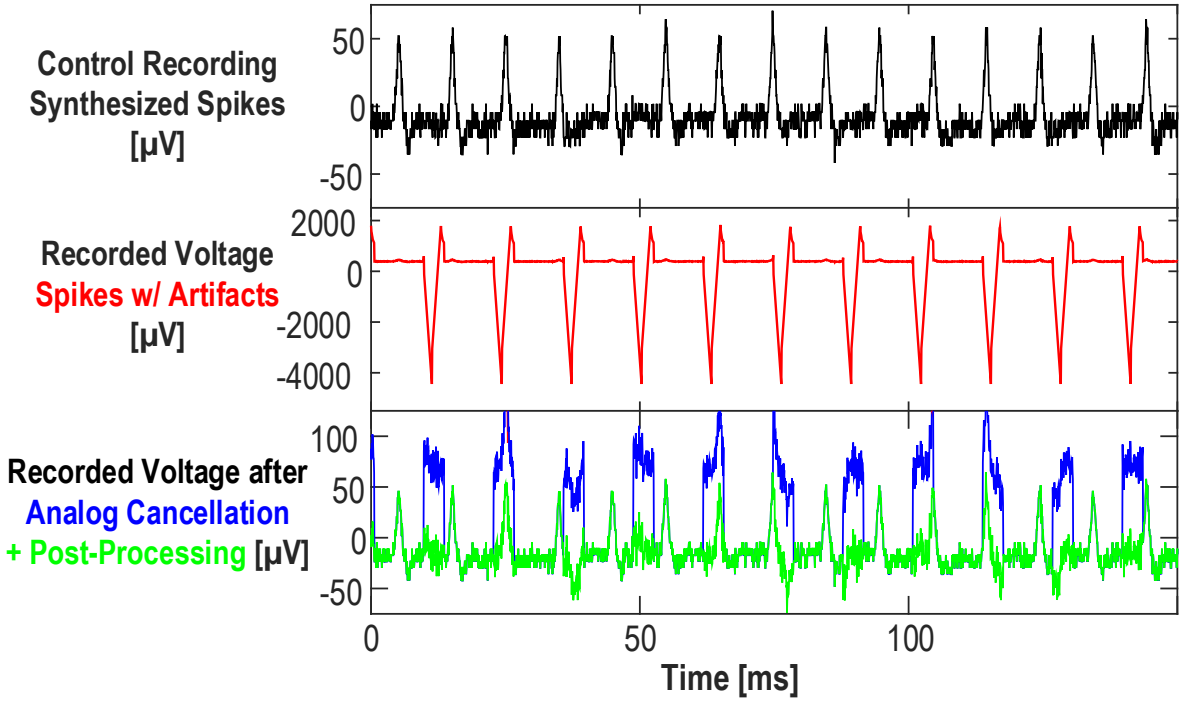


Figure 5-8. Measured bench-top transient recordings demonstrating artifact cancellation at 16kS/s. Signals recorded before stimulation, during stim. without cancellation, and post-cancellation with and without post-processing.

Figure 5-8 shows bench testing of artifact cancellation while recording at 16kS/s. Synthesized neural "spikes" are coupled into the recording input with voltage artifacts generated from an on-

chip stimulator. The control signal is a series of 50µV neural spikes at 100 spikes/sec from a Coulburn Bio-Signal Calibrator. Stimulation artifacts are ±125mV in amplitude at 77 pulses/sec, avoiding co-periodicity. Figure 5-8 shows recording measurements under the following conditions: 1) transient signal recording without stimulation, 2) with stimulation and artifact cancellation disabled, and 3) artifact cancellation hardware enabled and post-processing for further cancellation. The residual signal after post-processing is non-correlated stimulator noise. Figure 5-9 shows the corresponding PSD of each signal, demonstrating 60dB of voltage cancellation on the artifact fundamental at 77Hz and corresponding harmonics. Note, back-end post-processing provides an additional 30dB of cancellation.

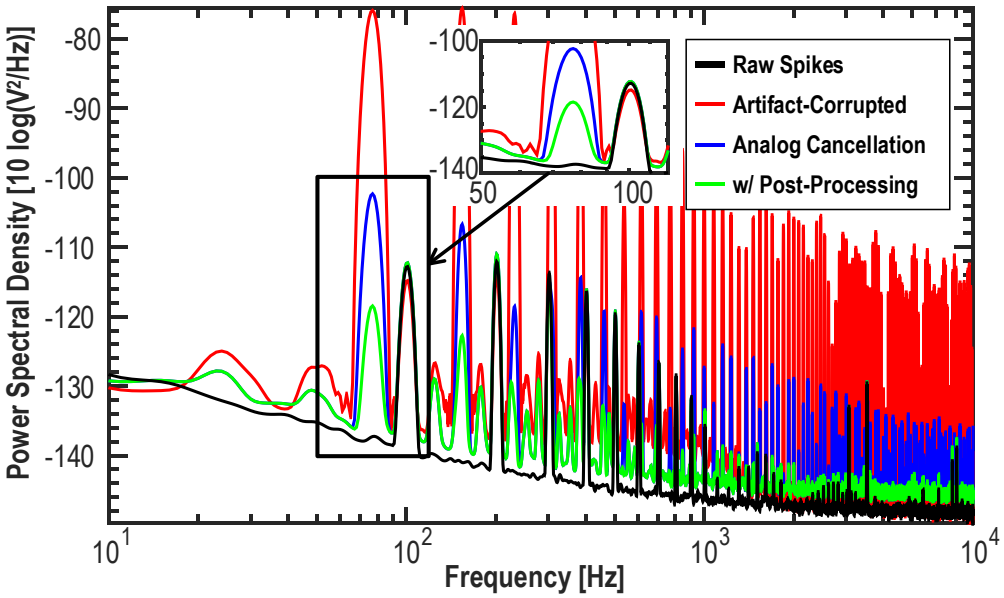


Figure 5-9. Power spectral density profiles for 16kS/s neural spike recordings.

Apart from the stimulator output stages, the test chip consumes 620µW while operating 64-channel recording at 2kS/s, multiplexed artifact cancellation, and the four stimulator back-ends. Stimulator output power is generated as needed by the on-chip resonant supplies. A die photo of the fabricated 65nm LP test chip is shown in Figure 5-10 with a chip area of 4mm^2.

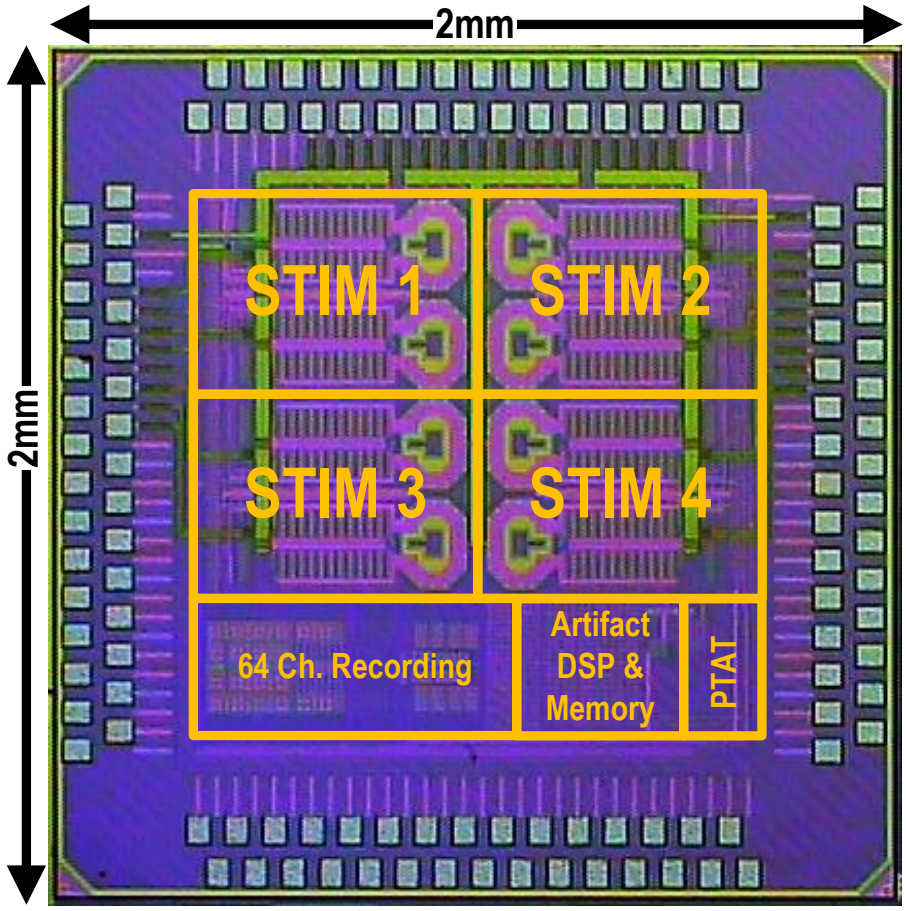


Figure 5-10. Micrograph of fabricated 65nm test chip.

A comparison with state-of-the-art solutions is shown in Table 5-1. This work condenses stimulation power generation into minimal silicon area, as compared to other works which require external high-voltage supplies or charge pumps. The high-voltage stimulation power train is integrated on the same standard CMOS substrate as a high-efficiency digital back-end utilized for closed-loop artifact cancellation, opening the way for multi-application single-chip BBCIs.

TABLE 5-1
COMPARISON WITH STATE OF THE ART

	ISSCC'16	VLSI'17	JSSC'17	SSCL'18	ISSCC '18	ISSCC'19	THIS WORK
Technology / Voltage	HV180nm	HV180nm	130nm 3.3V	65nm 1V	65nm 0.8V	130nm 3.3V	65nm 1.2/2.5V
Artifact Suppression	None	Fast Recovery	None	77dB†	92dB†	Fast Recovery	60dB
System Power (mW)	18▼	0.7	1.07	-	-	-	0.62
Chip Area (mm^2)	25	11.52	4.98▲	5.14	1	11▲	4
# of Ch.	16 SENSE 40 STIM	64 SENSE 4 STIM	64 SENSE 64 STIM	64 SENSE 2 STIM	16 SENSE	64 SENSE 64 STIM	64 SENSE 4 STIM
Stim Compliance	±12V	±12V	3.1V	-	-	High-Freq E-Field	±11V
Efficiency	From Supply	From Supply	From Supply	-	-	From Supply	31%
Area/Ch (Stim, mm^2)	-	-	w/ Sense	-	-	w/ Sense	0.36mm^2
Istim Shape	Pulse	Arbitrary	Arbitrary	-	-	Arbitrary	Arbitrary
Area/Ch (Rec, mm^2)	-	-	0.013	0.18	0.024	0.018	0.0025
Ch. Power (Rec, µW)	5.4	8	0.63	2.7	0.8	0.79	3.21
IRN (μV_{rms})	7.68	1.6	1.13	8.2	0.73	2.1	2.9‡
Bandwidth	7kHz	500Hz	500Hz	8.3kHz	5kHz	500Hz	Tunable <32kHz
Max DM Range	-	100mV_{pp}	13mV_{pp}	200mV_{pp}	260mV_{pp}	Rail-Rail	110mV_{pp}
ADC Type	10b Pipeline	ΔΣ OSR 1024	$\Delta^2\Sigma$ OSR 100 ENOB 11.7	10b Nyquist	$\Delta^2\Sigma$ OSR 32 ENOB 10.7	$\Delta^2\Sigma$ OSR 10k ENOB 10	Nyquist Δ- Encode ENOB 14

▼Includes stimulation power ▲Reported area includes Wireless Power/TX or DSP † AFE dynamic range ‡ Calculated over 1-1kHz BW

Chapter 6: CONCLUSIONS AND FUTURE DIRECTIONS

Integration of bidirectional neural interfaces into monolithic silicon chips will pave the way for interfacing with more channels with smaller device footprints, leading to less invasive surgeries. Co-integration of high-power stimulator electronics with dense, low-power recording systems is one of the remaining roadblocks to this integration effort. This dissertation proposes two techniques that further the goal of a true single-chip bidirectional interface: a. Time-multiplexed, mixed-signal artifact cancellation for simultaneous stimulation and sensing; b. Compact integrated stimulators with on-chip resonant charge pumps.

6.1 SUMMARY

A 65nm test chip has been designed, fabricated, and tested to validate the resonant charge-pump stimulator topology and integrated adaptive artifact canceller. This test chip builds off of previous UW efforts in standalone stimulator and recording system technology, representing a culmination of many students' work.

The compact resonant charge pump topology compresses two 24mW charge pumps and all other electronics for a single stimulator into 720μm x 430μm. The charge pumps operate at 3GHZ and have a measured DC-DC efficiency of 31%, dramatically increased from the theoretical value of 6% for a standard clocked pump at 3GHz. The stimulator achieves ±11V of voltage compliance at up to 2mA of output current using only 1.2V devices.

The multiplexed adaptive canceller topology demonstrates 60dB of analog artifact suppression with an optimized, template-based LMS update algorithm. Stability and convergence have been shown with *in-vivo* and benchtop measurements. Free-running calculation of an artifact for a single channel only consumes 49nW of power, approximately 10x less than comparable full-LMS architectures. This canceller architecture, having been verified, is scalable to many more channels.

6.2 FUTURE DIRECTIONS

The proposed work is a significant step towards full integration of all necessary components for a medically relevant BBCI. The path forward is to increase system modularity by further integrating the components used to test the system. This includes moving all voltage regulation and bias generation on chip, reducing pad/pin count to reduce package size, and simplifying digital control for increased compatibility.

The architectures themselves could also be improved with additional circuit techniques. The resonant charge pump could be further compressed by co-layout of the integrated spiral inductor and the metal finger capacitors. The inductor, as it is on the upper ultra-thick metal layer, could be placed over the capacitors with little change in performance. As the main source of power loss are the charge pump switches, reducing the inductor quality factor should have little effect. This would reduce the charge pump area by a further 30%.

The proposed artifact canceller was optimized for minimal power consumption, at the expense of robustness. The averaging and mean-zeroing methods explored in the FPGA-based canceller are area and power intensive but give stability and increased data fidelity in the presence of a noisy recording environment. Future chips with larger memory arrays and digital back-ends should include these measures for improved applicability.

The near-term goal for this chip is to re-spin the 65nm CMOS die to address system bugs and increase modularity. Then, the chip will be worked into existing wireless power/data PCB designs by other groups at UW. The goal is to make a useful neural research platform for free-moving animal experiments.

This system has several key advantages over the currently used commercially available parts. First, the stimulator power supply is on chip and only enabled on demand. Current

implementations require constant generation of high-voltage supplies, with several milliseconds of start-up latency. This creates a DC current draw, where the proposed system draws stimulation power only when sourcing current. Additionally, the integrated artifact canceller enables simultaneous stimulation and recording, where commercially available parts have latencies of 1-5ms for recording after stimulation.

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