Dedication

This Dissertation is dedicated to my family-

To my parents,

Anand Vaidya and Jyotika Vaidya

For defining my *life.*

To my sister

“Adita” - Vaishali Amonkar

For teaching me to *live* it.

And to my Grandmother

“Mai” - Kamala Vaidya

For her unwavering *pride, faith* and *love* for me.

I cherish my first years with you.

Efficient micro-Power Management for Solar Cells with Time Domain Array Reconfiguration

Vaibhav Vaidya

A Dissertation
submitted in partial fulfillment of the
requirements for the degree of

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Graduate School

This is to certify that I have examined this copy of a doctoral dissertation by

Vaibhav A Vaidya

and have found that it is complete and satisfactory in all respects,
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Abstract

Efficient micro-Power Management for Solar Cells with Time Domain Array Reconfiguration

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The goal of this dissertation is to demonstrate improvements to micro-power solar energy harvesting with a scalable approach. The improvements are demonstrated through a microchip designed to harvest energy optimally from a miniature, partially shaded Photovoltaic (PV) array with an adaptive, light weight, high efficiency power converter. The power converter dynamically reconfigures the array to operate each cell at its individual maximum power point using a new technique termed 'time-domain array-reconfiguration' (TDAR) to extract maximum energy from the miniature PV array.

Directly harnessed solar power is an attractive primary energy source for integration into fully wire-free, self-sufficient, portable electronic devices. Photovoltaic cells are most efficient at harvesting when operated at a particular voltage and current, termed ‘maximum power point’. Density of harvested energy increases and cost per watt decreases when PV cells are operated efficiently, requiring dedicated PV management electronics.

For both high power and portable applications, arraying PV cells increases voltage and current output. However, simply connecting PV cells in parallel or series leads to inefficient topologies where the weakest cell limits the output capacity of the array. The research challenge in PV power systems is thus to develop better power management techniques to boost PV efficiency. Portable PV arrays are small, low voltage, and subject to varying illumination and mechanical stress. Due to the additional constraints on portable systems, efficient PV management for portable and low-power systems presents a significant design challenge.

This work addresses technical challenges of micro-power array management in the context of a portable sensor aimed at 1 gram system weight and 100 micro-watt average power. Energy is stored in a Lithium-polymer battery. Only 2-3 PV cells are available, and illumination is expected to vary quickly. The system is thus designed to efficiently boost PV voltage to charge the 3.7V-4.1V battery while tracking individual PV maximum power points, and keeping power components under 0.5 grams. Efficient analog power tracking and TDAR are leveraged to meet these significant design challenges, and constitute the contribution to the state of art.

Contents

List of Figures

List of Tables

1

Solar Power: Large-scale to Micro-scale

1.1 Introduction

The goal of this dissertation is to demonstrate a novel hardware-based approach to increasing the efficiency of solar energy harvesting under partial shading in micro-power systems. Improvements in efficiency of up to 80% are made possible through both a new approach to management of shaded solar cell arrays and the use of low-power analog computational circuits to implement the approach. These advances in hardware and system design are demonstrated through a microchip that optimizes the way in which energy is harvested from a miniature, partially shaded photovoltaic (PV) array.

This chapter begins with a summary of the importance of improving efficiency in solar energy harvesting systems, from large scale to micro scale. An overview of solar harvesting at the system level then exposes challenges in operating PV cells efficiently. These challenges, intuitively evident for large-scale systems, are translated to the micro-scale context of ultra-portable devices. Understanding these solar energy harvesting challenges lays the foundation for the approach used in this dissertation to address this problem at the micro scale.

Following the identification of the challenges involved in improving solar energy harvesting, Chapter 2 highlights current state-of-the-art approaches to PV cell management that have been used at a variety of scales to improve efficiency in photovoltaic arrays. Chapter 3 presents the improved system design targeted toward improving efficiency in solar energy harvesting systems by 80% or more under partial shading. In Chapter 4, the analog circuits used to implement the system design are described, followed by experimental results at both circuit and system level in Chapter 5. Implications to micro-scale systems as well as

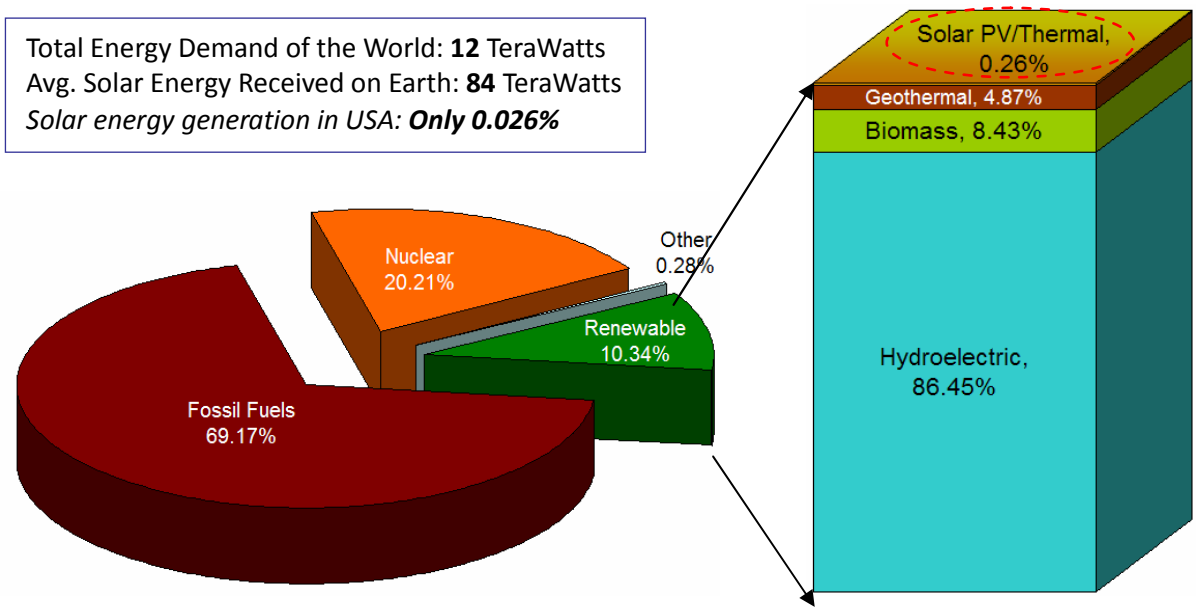

Figure 1: ***Energy Sources in 2009, USA*** *- Solar power is 0.26% of renewables, 0.026% of overall energy production* *(source: Energy Information Administration, a part of the US Department of Energy)*

larger-scale (grid) systems are discussed in the summary of Chapter 5.

1.2 The Importance of Solar Energy Harvesting

The sustainability of the worldwide energy budget directly affects future quality of life and the sustenance of the human species. With the depletion of fossil fuels and man-made climate change combined with continuing increase in per-capita energy consumption by populations in developing countries, sustainable and renewable energy is urgently imperative to pursue sustainable energy sources to provide for global consumption needs.

As shown in Figure 1, the current energy budget in the United States is highly skewed toward fossil fuels. In combination, non-renewable energy sources based on fossil fuels (mainly natural gas and coal) and nuclear energy account for 89% of US energy production. The dependence on non-renewable energy sources is a global phenomenon and the United States, as the highest energy consumer per capita of energy in the world, exemplifies the heavy dependence on fossil fuels to meet energy demand.

Fossil fuels are considered a *secondary* energy source meaning they have absorbed and stored energy from a primary source such as the sun, usually over considerable time. Other

sources of energy such as the sun and nuclear power, on the other hand, are primary energy sources, meaning that their energy is directly and readily available for human use. Among these primary sources of energy, the sun, geothermal, and nuclear energy are most abundant. In current energy usage terms, 69% of all US electricity is derived through secondary sources that *rely on solar energy*. However, only 0.026% is derived by *direct solar harvesting*. In meeting future energy sources, solar energy, since it is plentiful and accessible through a variety of conversions, will remain the top source of energy in the world, whether through renewable or non-renewable sources.

Solar irradiation on earth's surface, averaged over the year (approximately 85TW), is close to an order of magnitude greater than the worldwide average demand for energy (approximately 15TW in 2008, according to the International Energy Agency). Despite the sun being a plentiful source of energy, only 0.026% of energy used worldwide is *directly* converted from this vast source. Some losses are inevitable in the conversion of solar energy to electrical energy. However, many losses can be improved through corresponding improvements in harvesting technology. The potential for meeting global energy demand by harvesting solar energy more effectively is both economically and environmentally attractive. Research is slowly catching up to this potential, but there is a great deal of distance to be covered in this field to make solar power (energy harvesting) work as well as fossil fuels in meeting global energy demand.

1.3 Direct Solar Harvesting Technology

Solar energy is presently harvested directly in two major ways:

a. Through an intermediate conversion to heat in solar collector systems: Solar collector systems rely on focusing solar radiation to heat a substance (such as a metal oxide) that then releases energy thermally or mechanically. This energy is ultimately converted to electricity. Solar collector systems are not as scalable as photovoltaic (PV) systems because they need a minimum amount of illuminant energy to be efficient, making them more suitable for isolated installations in well illuminated areas away from civilization.

b. By conversion to electricity in Photovoltaic (PV) systems: Photovoltaic (PV) cells harness

solar radiation directly as electricity. This process of “photo” to “voltaic” conversion means that the energy from photons in light gets converted to an electric voltage and current. This process of conversion occurs when incident photons have just the right energy range to ‘charge’ atoms or molecules in the PV cell, and when the PV cell is setup to ‘discharge’ through an external electrical circuit the converted energy can be delivered to the external circuit. Rather than molecules of a single materials, light absorption and separation best occurs at junctions of materials within PV cells. Hence improving the ‘photo to voltaic’ conversion in a PV cell involves managing the interfaces of the constituent layers of a PV device such that 1> the ‘energy to separate charges’ is matched to the energy of light photons being absorbed, 2> once generated, the charges don’t discharge internally in the cell, and 3> the movement of the charge out to the connecting terminals of the PV cell is efficient. Motion of this charge by current flow in an external electric circuit in turn improves the electrical energy output derived from the impinging photons.

Whereas the above three conditions define the internal efficiencies of the PV cell, the efficiency of energy delivery from the PV cell is also limited by the external circuit itself. For example, if the external circuit tries to draw more current from the PV cell than it can produce optimally, the efficiency of the PV cell drops. Similarly, if the external circuit draws too little current, the PV cell voltage rises and efficiency, again, drops. In fact, PV cells need to be managed continuously such that the power demand on them *always* matches the power they can optimally produce at any given time and this fact gives birth to the paradigm of PV power management.

This work addresses the efficient management of PV cells, both, individually and relative to other PV cells in a solar harvesting system. Specifically, the circuits and system developed in this dissertation have the dedicated job of governing the operating point of PV cells in a series string by changing and optimizing the power drawn from them.

1.4 Selection of Photovoltaic (PV) Cells

The materials and technology effort in PV cells concentrates on cost-effectively optimizing each of the individual processes involved in the energy conversion from photon to output electric power at the PV electrodes. PV device technology optimizes photon absorption,

charged species generation and lifetimes, charge collection, device stability and processing costs. The present state of PV technology in the context of available cell types and relevant applications is analyzed next.

PV cells are used in various applications, ranging from power generation for mainstream consumption, such as domestic grid-connected solar systems and industrial solar systems, to ultra-portable applications such as powering small electronics by energy scavenging. Different PV technologies are available, with Crystalline, Thin Film and Gratzel cells being the highest level classification. Each technology has an application niche where it achieves the best price-performance, and the trends of adoption change with new advances in newer technologies. According to the IEA Open Energy Technology Bulletin, Nov. 2007, the installed PV capacity worldwide is growing exponentially, at 40% a year.

Higher power installations have naturally attracted the use of inorganic crystalline cells which have higher efficiency and durability. However, thin film electronics has been gaining market share steadily due to low cost and applicability to portable applications, as shown in Figure 2.

Organic PV (OPV) cells are well suited to compete in the thin film solar power market, with their potential for very low cost manufacturing by printing, and compatibility with flexible substrates promising a roll to roll process. The External Quantum Efficiency (EQE) of OPV cells is now consistently reported above 5% [1], including small-molecule[2], polymer[3] and

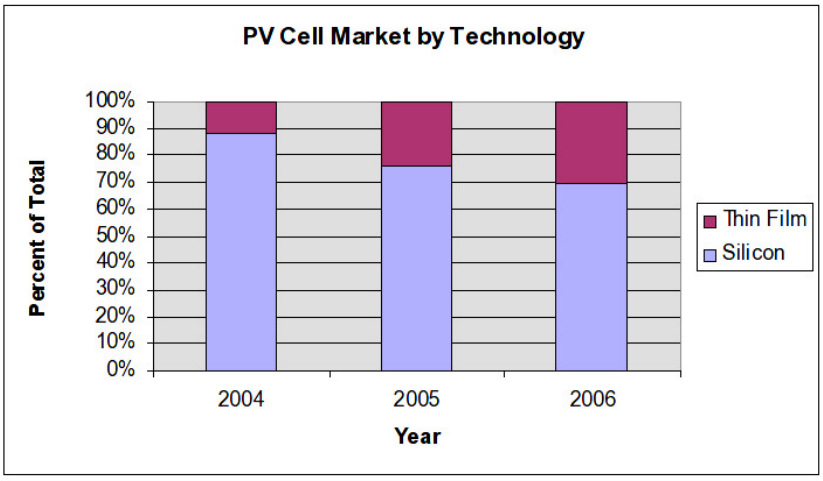

Figure 2: ***Market share of thin-film PV cells*** *- is increasing every year.*

tandem cells [4], and is projected to increase to over 10% in the near future. Although the efficiency of OPV cells is still shy of the efficiencies in crystalline solar cells which achieve more than 20% EQE in commercial versions [5], the materials and processes involved in OPVs are cheaper, making OPV cells competitive in terms of cost. With potential improvements in OPV cell lifetime through techniques such as encapsulation and inverted cells, OPV cells have the potential to achieve a better cost per watt than crystalline silicon cells. Further, OPV cells can be made on light, flexible substrates making them attractive to portable applications. For their promise of customized, low cost, light weight and flexible energy harvesting, organic PV cells are evaluated alongside crystalline PV cells in this dissertation to elicit potential advantages.

1.5 Management of PV cells in a Solar Energy Harvesting System

Whether organic or inorganic, crystalline or thin-film, large area or small, most practical PV cells have a diode-like current-voltage characteristic such as the one in Figure 3b, with a voltage between 0.3V to 0.6V where the slope of the characteristic is unity. Optimal power harvesting occurs at this unit-slope voltage. Since the voltage of a single PV cell is too low to power conventional electronics, it is common to connect individual cells in series strings to

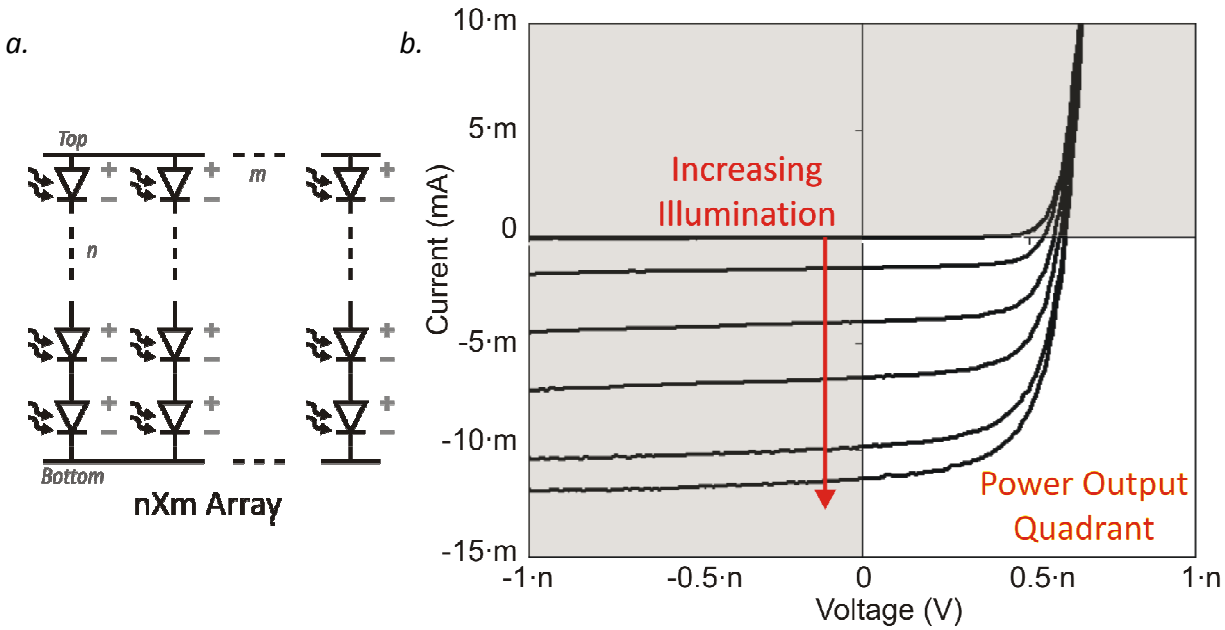

Figure 3: ***A typical nXm PV array*** *- a. Connection b. Characteristic scaled by m and n*

provide higher output voltage. Further, to increase current capacity, such strings can be wired in parallel. Thus a typical PV power source might look like the one in Figure 3a, with the I-V characteristics scaling with number of PV cells in parallel and series.

Two characteristics of PV power sources are apparent from Figure 3:

1> A PV cell changes its operating point based on input light and

2> Series/parallel connections cause electrical interaction among PV cells while delivering power.

In the nXm array, if all PV cells are matched, the array voltage will be n times the voltage of a single PV cell, while the current output of the array will be m times a single PV cell as shown in Figure 3b. If the cells were mismatched in current or voltage, the cell with the lowest current decides the current capacity of each series string, and the output load splits unequally between parallel strings depending on the mismatch in their open circuit output voltages [6]. Both these phenomena can cause the array to put out less power than the sum of powers from constituent PV cells. To extract power efficiently from a PV array then, the management electronics needs to *actively control* at least one or both, the *operating point* and the *interconnection* of cells.

Active control of an array of PV cells prevents a load from passively determining power output at an arbitrary level which is almost always sub-optimal. Instead, active control optimizes the energy harvested from a PV system for changing environmental conditions (illumination change and shadows). Active control of PV cells implements one or more of the following tasks depending on the sophistication of the system:

1> Managing a single PV 'entity': *Power output of a PV cell can vary widely depending on how much load is presented to it, and the harvesting electronics needs to ensure the PV cells are operating reasonably efficiently.* Power optimization of a single PV cell or a series string is the most basic and essential of harvesting management tasks.

2> Managing a collection of PV cells: When PV cells are interconnected as in Figure 3a, their power production can interact in sub-optimal manner. Series cells can be

considered together to optimize the overall power, or parts of a single array can then be treated separately to ensure efficiency. For example, PV cells with unequal output can be *re-wired intelligently* on the fly to collectively produce the maximum possible power.

3> Managing load requirements: The operating point of the harvesting system can be optimized with load requirements for specific applications. For example, 'Inverter' systems used with commercial solar power installations ensure constant output alternating voltage while supplying maximum possible current.

4> Power conversion: The majority of photovoltaic harvesting systems supply load electronics that operates at a different voltage level than the generated PV voltage. Hence an efficient power converter stage is an essential part of most PV systems, either a dc-dc converter or a dc-ac converter (inverter).

Research into PV power management systems has the goal of achieving better performance implementing one or more of the above techniques, while favorably trading off the cost/complexity overhead of the management electronics. The majority of PV power management research deals with power management for large, fixed arrays.

1.6 Challenges in Designing PV management systems

Practical implementations of power management systems for PV cells face the following challenges:

1> True MPP tracking and overall efficiency: Tracking the optimal operating point of a solar cell is a challenging problem especially with multiple cells in an array. Cell conditions can change quickly and require complex power-balancing techniques to achieve high efficiency [7]. MPP tracking is covered in detail in Chapter 2 with a review of techniques published in literature. The design of the PV array also needs to consider the blocks in the power chain that follow the PV cell, such as boost converters and inverters, to ensure high overall efficiency of the energy harvesting chain.

2> Accuracy, drift and speed of response: The first tradeoff in tracking true MPP is caused by the fact that different conditions of PV harvesting change over a range of time-scales, from a few seconds for passing shadows, to many years for drift in the cells themselves. The power management system needs to accurately track the optimal power across these time scales. The speed of the system thus needs to be quick enough to respond to quick changes, and the power tracking algorithm needs to successfully compensate for slower changes such as daily sunlight variation, soiling of the PV array or even degradation in the PV cells. Different management schemes are thus developed to achieve a better overall tradeoff between accuracy, drift immunity and speed of response. Hill Climbing [8] and Fuzzy logic control [9] are examples of algorithms that explore this tradeoff.

3> Performance and Cost: The more obvious trade-off in PV management systems is that between performance and cost. A complex power management architecture that uses high performance control systems can improve power tracking but at a high cost. A technique that exemplifies this tradeoff is array reconfiguration [10], which can boost PV efficiencies significantly but requires a complex switching matrix adding cost to the PV system.

The challenges and their solutions in PV management can be application specific. For a large scale PV system, such as a utility power plant, power balancing across geography becomes viable. Passing clouds only occlude a part of the array since it is spread across a large area, thus allowing the rest of the PV system to compensate [11]. Mechanical systems to track the sun during the day can be implemented[13][12]. For smaller scale systems such as rooftop installations on the other hand, simpler microprocessor controlled operating point algorithms that control a single inverter are better suited. The optimal power management trade-off thus can be scale and environment dependent. In the next section, power management trade-offs are examined particularly in the context of micro-power PV systems which are gaining popularity in research and industry.

1.7 Portable PV harvesting

Recent research into portable microsystems for environmental monitoring, consumer electronics and military applications has brought increased interest in portable energy

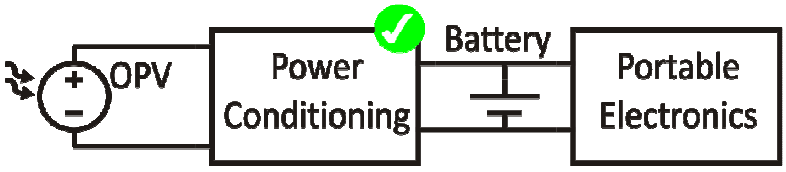

Figure 4: ***Parts of a typical portable light harvesting microsystem***

harvesting, with the promise of wire-free devices. With the sun still the most abundantly available natural source of energy for portable systems, portable PV harvesting is increasingly relevant to electronic microsystems that are gaining functionality without an increase in size [14]. Although the scale of PV harvesting is much smaller for portable applications, with a power budget ranging from microwatts to a few watts, many electronic challenges of PV power management translate to portable systems directly from high power systems. Although mechanical or geographical issues play a reduced role, portable PV systems can borrow extensively from large-scale PV management concepts.

A few reasons for the similarity in management include the fact that PV cells are linear in their response to incident light levels over quite a few orders of magnitude, a fact used to advantage in concentrated photovoltaics [15]. Thus PV management in bright sunlight can scale well to low-light or indoor portable applications. Further, the spatial frequency of transient illumination variation is high enough to justify both maximum power point tracking, and relative management of interconnected PV cells even at centimeter scale applications [16]. Thus PV management also scales well in terms of PV source size, and all major PV management tasks outlined in section 1.4 are applicable to micro-power devices, with a few additional challenges.

Load requirements in portable devices are usually different from grid-scale systems, largely centering on charging a battery of energy storage cells. Due to low voltage PV sources, portable systems require dc-dc power conversion to meet load requirements, rather than

dc-ac conversion in grid-level applications.

As enumerated in Section 1.5, power management systems for PV cells address the challenge of optimizing several tradeoffs. Portable systems present similar challenges, with some additional constraints. The trade-offs enumerated in section 1.5 are revised here for a portable systems context:

1> True MPP tracking becomes a more urgent problem, as the PV cells are exposed to a wide variety of shadowing, soiling and environmentally diverse conditions. In such environments if PV cells are connected in an array, MPP trackers are very likely to encounter local maxima in the power curve of a PV array that are less efficient than the target global maximum.

2> The speed of response is a more stringent constraint in portable systems compared to fixed arrays. Since the PV array itself is on a moving platform in a portable system, changes in orientation, ambient light and passing shadows can be much quicker than a fixed installation. In particular, the system in this work is designed for an airborne application, and the response time is required to be in the tens of milliseconds. Drift tolerance is important to preserve efficiency in the face of slow changes. A portable system also needs to achieve as high an efficiency over many light levels as possible, since the amount of light available is of unpredictable intensity and duration with minimal battery backup [17]. Thus fast, accurate MPP tracking is very valuable for portable systems.

3> Perhaps the largest constraint on portable systems is that of size and weight. A small and low weight PV harvesting system implies that the complexity of power management is limited. For example, even when a microprocessor is available in a portable system, the scarcity of available CPU cycles can put the harvesting system outside the microprocessor's control realm, precluding firmware-based MPP tracking methods. Finally, the cost of most portable systems can be a limiting factor. Although niche applications may tolerate high unit-cost, many important applications such as environmental monitoring and personal electronics require low unit-cost portable systems that cannot support a complex and expensive energy harvesting solution.

Since practically feasible high-functionality portable systems are relatively recent, and because large-scale harvesting has a larger economic value, much of the research in PV power tracking electronics has a traditional focus on large-scale PV harvesting rather than on portable systems. Since many of the power tracking requirements translate from high power systems to portable systems, development of scalable technology that can serve both portable and high power PV harvesting systems is potentially a high-value area of PV systems research. Achieving

1> individual MPP tracking,

2> intelligent PV array management,

3> load matching and

4> power conversion

in a cost effective, low complexity, accurate and fast system is the holy grail of PV power management. *This work is among the first to explore performing all four PV management tasks at micro-power levels for an ultra-portable energy-harvesting application; with high efficiency and low complexity.*

1.8 The Portable Microsystem

The ideological framework for PV harvesting electronics has been developed in previous sections, and the rest of this work is performed in a micro-power context. The system and circuit ideas developed next have been designed in the context of a practical low-power portable microsystem 'Encounternet' developed by the Wireless Sensing Lab at the University of Washington [18], and scale well both, to other portable PV harvesters, and to higher power systems. Unique challenges of microsystems are addressed, a solution developed and the scalability of this work is discussed to conclude the treatment of the concepts which are introduced next.

Portable PV power has the same need for power management as large scale systems, with a few differences. Voltage conversion ratios are usually in the low single-digits, and the output

is direct current (DC) rather than alternating. Available power headroom, size and weight are also much lower than high power systems, which places limits on system complexity and size of passives in power conversion. On the load side, energy storage is often in the form of a battery, while on the source side, the variation in illumination and its non-uniformity are also significantly higher than in large scale systems.

The focus of this work is on energy harvesting parts of a system of the type in Figure 3. The application is a wire-free, ultra-portable sensing platform designed to achieve system weight less than *1gm* and a footprint less than $1cm^2$ [18]. In this microsystem, the energy harvesting components are charged with generating sufficient *average* power to keep the battery charged. In return, the battery compensates for the lack of synchronization between available light energy and power demand of the sensor system over a daily cycle.

The sensor system is expected to perform functions such as sensing, pre-processing and transmission of data over radio frequencies, in an arbitrary sequence. The power demand of this sensor thus has large variations over a short time, depending on which function it is performing at any moment. Various configurations of the Encounternet system are in the research phase, the upper bound on overall power budget for the system considered for this project is set at 100µW.

Variation in the sensor's power demand is averaged by the (lithium-polymer or Li-Po) battery. The goal of the power conditioning circuit thus becomes charging the Li-Po battery optimally, as and when ambient light is available for conversion to electrical energy. Since ambient light varies significantly, the power electronics is designed for achieving high efficiency at power transfer levels which are an order of magnitude greater than the average sensor power, or approximately 5mW.

Among competing approaches to power such a sensor system, battery charging can be achieved by off-the shelf components [19], and single-solar-cell power converters are also available [20]. However, a custom solution for this system promises to reduce both system weight and cost, while optimizing for custom PV arrays to increase efficiency. Further, designing the output voltage of the PV cell(s) to complement the following power converter

can yield a significant benefit to overall harvesting efficiency. Thus there is benefit in co-designing the PV cell, management electronics and power converter into a custom portable solution.

Organic PV (OPV) plastic substrate solar cells are good candidates for this application due to their potential for light weight durable plastic substrates and ease of custom fabrication. State of the art OPV cells used for reference design values in this work were developed by Professor Alex Jen's research group at University of Washington's Material Sciences department [21].

In summary, the challenges of designing a portable system for sub-1gm weight, incorporating the ability to tackle partial shading, and minimizing solar cell size translate to design constraints of limited weight of passive components low, achieving a power/complexity efficient MPP tracker resilient to partial shading, and minimal dissipation in the power electronics.

1> A single-inductor based design was selected for dc-dc converter, to achieve high efficiency over a large dynamic range of ambient light.

2> To keep the dc-dc converter operating at high efficiency, the boost ratio needs to be as small as possible without increasing PV array size. A 3-PV cell array was selected, with an efficient MPP tracker for each PV cell.

3> Time domain array reconfiguration (TDAR) was developed to maximize power efficiency under partial shading with minimal electronic complexity. The system thus developed is discussed in Chapter 3.

4> The final piece of the puzzle was developing low power analog processing circuits that replace power and area hungry digital processing which are described in Chapter 4. Chapter 5 presents the results of the proof of concept microchip developed for this application.

First, to understand the motivation for a TDAR system, the next chapter reviews literature on the state of the art in PV MPP tracking and partial shading.

2

Technology Review and T.D.A.R.

2.1 Technology Review

The conceptual foundation of solar cell management is first established in this chapter, along with a review of the current state of art in PV cell and array management. Based on this foundation, a novel approach to PV cell and array management is proposed to achieve a better efficiency/complexity tradeoff, motivating the concept and design of Chapter 3.

2.2 Maximum Power Point (MPP) Tracking

The amount of light incident on solar cells changes every moment. For a static installation of solar cells installed on a roof for example, the change is due to the daily light cycle, passing clouds and fixed objects such as chimneys that alter the shading of the array. Fluctuations from the atmosphere alone are significant, as is shown in the daily insolation variation for a partly sunny spring day shown in Figure 5, as measured on the Atmospheric Sciences building at the University of Washington. Changes in output, impacted by both insolation and shading, are thus significant and frequently variable even for a static cell.

For moving cells, such as those found in portable arrays for wearable electronics and wireless microsystems, variation in insolation can be higher and more frequent. The situation is more dynamic as both the solar cell and its surroundings move and change unpredictably. A change in the orientation of the solar cell with respect to incident light changes the photon flux significantly in a short amount of time, as do passing shadows and any surface adherents to which the cell is exposed.

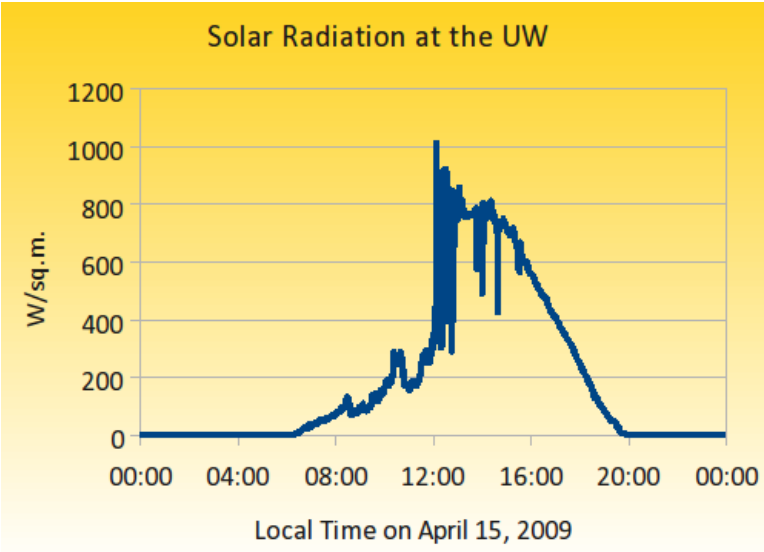

Figure 6: ***Insolation variation*** *- at the top of the Atmospheric Sciences building at the University of Washington on a partly-sunny spring day*

A change in the amount of light incident on a solar system changes the output voltage and output current (V-I) characteristic of the component PV cells. The part of the V-I curve where the cell harvests energy most efficiently (the maximum power point) also changes with insolation. In Figure 6, a typical V-I characteristic for an organic PV cell reaches maximum harvesting efficiency at different voltages for different amounts of insolation. For example, when the cell is exposed to a 100W/sq.m, the best harvesting efficiency occurs at 0.5V, while when the cell has 1W/sq.m insolation, the optimal operating voltage is 0.4V with

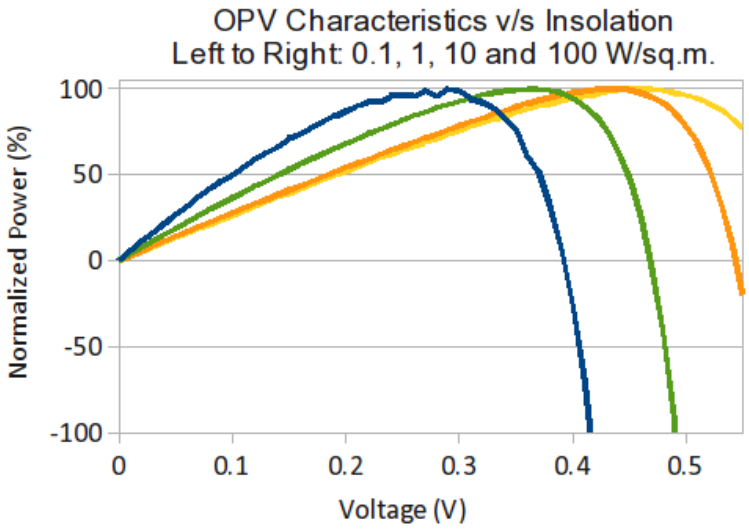

Figure 5: ***Power-Voltage Characteristics of PV cells vs. Insolation*** *- For each level of insolation, the power harvested is highest for a particular terminal voltage of the PV cell. These cells characteristics are measured for Organic PV cells produced by the Jen group at the University of Washington's Material Sciences department, using a standard AM 1.5 light.*

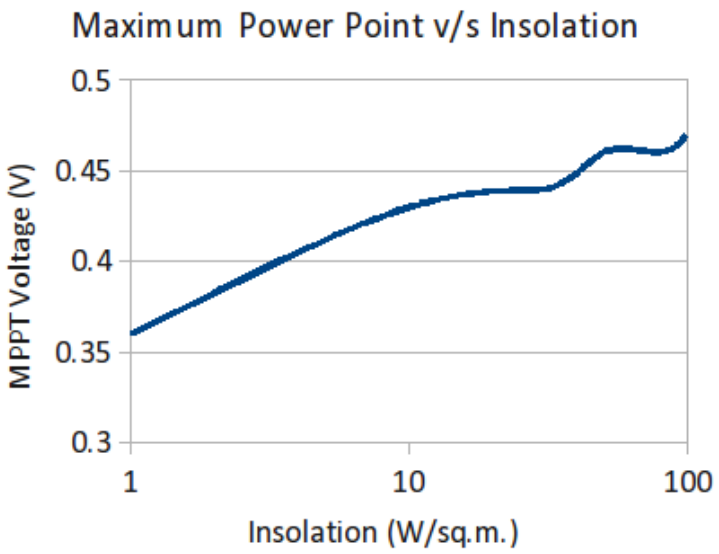

Figure 7: ***Variation of the MPP voltage solar cells*** *- almost linear vs. logarithm of insolation*

200% efficiency loss at 0.5V. These results were measured from stable, state of the art (Organic) PV cells on a glass substrate [21]. The voltage at the point of maximum power harvesting is extracted and plotted separately in Figure 7 for clarity.

When the solar cell is used in an energy harvesting application where insolation fluctuates, its operating point must be changed as insolation varies in order to keep its external quantum efficiency (EQE) close to the maximum. Power converters designed to work with energy harvesting systems often incorporate circuitry to track this maximum power point (MPP). Such power converters are an active area of research, with different methods of MPP tracking offering varying levels of cost, complexity, speed and accuracy. Esram and Chapman have an excellent review of the MPPT techniques currently in vogue [7]. As Figure 5 shows, for a single PV cell with a given insolation, there is only one MPP in its characteristic.

In a straightforward approach, the MPP can be found by changing the operating point (voltage or current or load) of the PV cell in the direction of increasing power until the highest power is reached. 'Hill Climbing' [24][23][22] and 'Perturb and Observe' (P&O) [25] are two classes of MPP trackers that implement this method. Typically, since the solar cell is followed by a power converter, the load on the cell and hence it's operating point can be changed by changing the duty cycle of the power converter. Hill-climbing algorithms change the duty cycle to achieve maximum power point. P&O methods on the other hand,

artificially perturb the Voltage or Current of the PV cell to find the direction of increasing power, and then adjust the harvesting system for maximum power. Both Hill Climbing and P&O algorithms thus have the same basic advantage of simple implementation, and their disadvantages also correlate well. For example, if the incident light on PV cells changes quickly, both algorithms can lose track of MPP. The most significant tradeoff for both algorithms is between sampling resolution and speed of response, with a higher sampling resolution giving better tracking but slowing response time. Research on these algorithms attempts to improve on this tradeoff by using digital processing based techniques such as two-step and fuzzy-logic control as detailed in [5]. Though the basic Hill Climbing and P&O algorithms can also be implemented in the analog domain, digital implementations are more common in the context of large arrays. A comparison of Hill Climbing and P&O methods is found in the paper by F. Liu et al [8].

Another method that lends itself well to DSP and microprocessor control is working with the first derivative of the power-voltage curve (dP/dV). The intention is then to maintain this first derivative at 0, which corresponds to the maximum of the power curve. Derivative minimization can be performed by directly [26] feeding back the slope of the P/V curve under perturbation to the control circuit. The incremental conductance method in [27] [28] is an example of indirect derivative minimization, and uses the relation P=VI so that seeking the equality of conductance to incremental conductance, (I/V)=-(dI/dV), indirectly achieves dP/dV=0.

Still other methods for finding the MPP, also digital in nature, such as fuzzy logic control [29][5] and fractional voltage or current [7][8] are designed either to improve the speed/accuracy tradeoffs achieved by the basic power tracking and derivative MPP methods, or to minimize the number of sensed parameters. For example, the fractional I/V methods rely on existing knowledge of the PV system to reduce the number of parameters extracted from the cell during runtime. Some digital algorithms available to track MPP, are enumerated in [30] and [31].

A few methods for finding the MPP lend themselves better to implementation in the analog rather than digital domain, and are thus more relevant to a low-complexity portable MPP

tracking system such as the one considered in this work. The analog domain affords several advantages including faster response with lower power consumption, and lower circuit complexity. Thus MPP methods with a smaller logical decision depth and real-time response work well with analog systems. Of particular note are ripple correlation control (RCC) [32] [34][33] and load current/voltage optimization [14][35]. Ripple correlation is an opportunistic method that uses incidental voltage/current ripple present on the PV cell as a perturbation to track MPP using. This ripple is usually the by-product of a subsequent power-converter stage. The difference from traditional P&O is that the ripple is usually a very fast perturbation, faster than any sampling clock in the system. Thus the MPP control occurs in real-time using the analog domain time-differential of power and voltage of a PV cell.

Load current/voltage optimization is an orthogonal approach to most other MPP tracking concepts in energy harvesting. By leveraging the possibility that the best conditions for the load may occur at an operating point different than the PV cell's MPP, load I/V optimization measures and optimizes the load parameter of interest such as the charging current of a battery. For example, if the battery is at a low voltage level, it might be more beneficial to maximize current drawn from the PV cell to charge the battery at a fast rate, although the PV cell might be below its MPP voltage. As the battery voltage rises, the efficiency tradeoff might shift in favor of operating the PV cell at its maximum power point. Load I/V optimization is well suited for optimizing a 'global' variable such as load current or voltage instead of individual PV cell parameters.

Comparing the two analog domain techniques, RCC is offers true MPP tracking in a high speed, low complexity package. However, it requires both voltage and current sensors, which can be expensive for high power applications. Load I/V optimization is potentially lighter on sensors and particularly applicable to portable sensor systems. It is a low complexity method which is also fast, and can optimize the battery charging current directly instead of tracking solar cell MPP.

RCC and Load I/V optimization are both strong candidates for use in this work. RCC was chosen for implementation because of the use of Time Domain Array Reconfiguration (to be

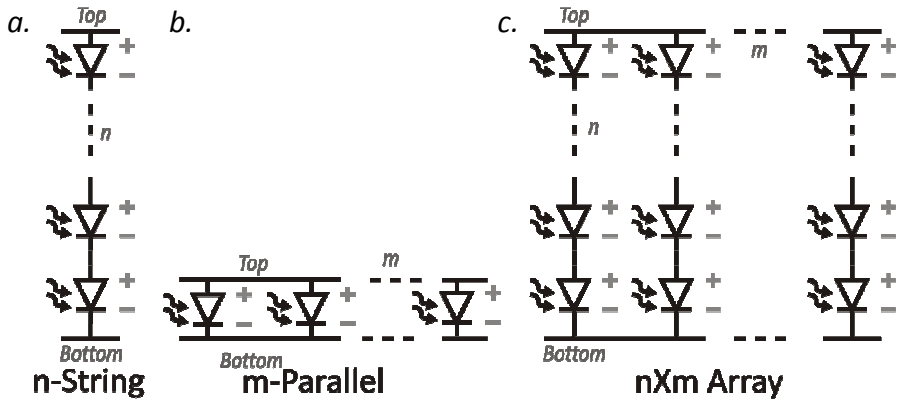

Figure 8: ***Connecting PV cells together*** *- a. n-series string, b. m parallel cells, c. nXm Array*

introduced in Chapter 3) in this system, in which the optimization variables are local and on the input side (each PV cell's MPP) rather than global and on the output side (charging current).

Thus far in this chapter, the discussion about MPP tracking has focused on tracking a single MPP in the PV power-voltage curve, albeit with a few mentions of multiple MPPs. The input PV cells have been considered as a single entity, with no treatment of what happens when the power output of the PV cells in an array is heterogeneous rather than matched. In the next sections, the discussion is extended to mismatched solar cell outputs, multiple MPPs, and tracking methods that specifically address the problem of partial shading. But first, a look into the need for PV arrays is presented next.

2.3 Arraying PV cells

Single PV cells are limited in their voltage output by constituent material properties, and in their current output by how large their area is. For energy harvesting applications, from portable to grid-sized, voltage and/or current requirements are typically higher than what single PV cells can provide. The solution to meet the higher requirements then, of course, is to make arrays of PV cells. PV cell arrays simply sum the voltage and current output of PV cells, to multiply the values for both. Series connections sum voltage, and parallel connections sum currents. Figure 9 illustrates series and parallel connections of PV cells.

For grid systems voltage summation is irreplaceable, since the power inverters driving the grid need to generate over 100V. The efficiency of inverters drops as the ratio between grid

voltage and PV array voltage increases. Hence grid applications use series PV strings with higher voltage outputs, the nominal voltage for most PV arrays being 12V or more. Achieving this voltage implies connecting more than 20 PV cells in series. Grid systems also require high power, which means several series strings are connected in parallel to yield higher current than what a single PV cell can provide.

In portable systems, alternatives such as dc-dc converters which harvest energy from a single solar cell are actively pursued [15] since they make it easier to deploy a system using off-the-shelf single solar cells. However the efficiencies of single-cell converters rarely exceed 60% for inductor-based converters due to conduction losses at low-input-voltage, high-current levels. Charge pump converters can achieve higher efficiencies, but with a limited dynamic range of current [36]. With voltage summation, higher voltages from the PV cells can boost overall harvesting efficiencies in both cases, providing an improved harvesting tradeoff.

More treatment on optimal array configurations depending on application can be found in [37] and [6]. The next section returns to MPP tracking in the context of this new dimension of combining multiple PV cells and considering PV arrays as a heterogeneous collection of cells rather than a single entity.

2.4 Partial Shading

Further challenging in the selection of array configurations and design of the power converter is the problem of partial shading of an array, whether large (grid scale) or small (microsystem). To optimize harvesting efficiency beyond the basic design of the PV cell and material and the array aspect ratio, further attention can be paid to optimizing efficiency when the illumination of the array is not uniform. In partial shading situations, substantial power can be lost from the array by a power converter design or array configuration that is not designed to handle partial shading, and thus there is a definite opportunity for research to improve performance of array-based systems.

The problem of partial shading can be illustrated with a simple example of several PV cells arranged in a series string (Figure 9). In the case where the cells are all matched and equally

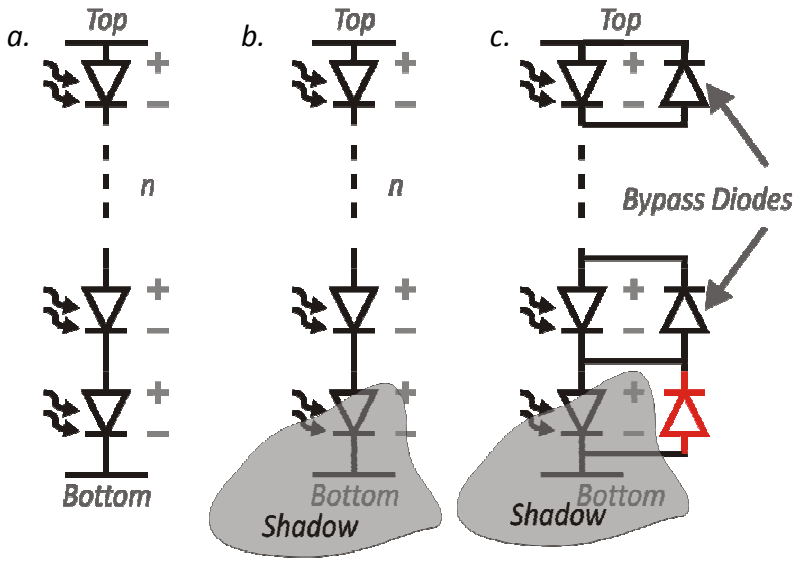

Figure 9: ***Partial shading and traditional PV strings*** *– a. unshaded string b. partially shaded string c. bypass diodes to conduct string current across shaded solar cells*

illuminated, the power converter tracks the entire string and optimal power is produced. The string voltage and current are given by the equations:

$$V_{string} = n \cdot V_{PV} \qquad \ldots(2.4.1)$$

$$I_{string} = I_{photo} - I_0(e^{\frac{qV_{PV}}{kT}} - 1) \qquad \ldots(2.4.2)$$

However, even if one cell is shaded (Figure 9), the current capacity of the string is limited according to the level of shading on the one cell. The V-I characteristic is then given by the equations:

$$V_{string} = (n-1) \cdot V_{PV} + V_{PV,\,shaded} \qquad \ldots(2.4.3)$$

$$I_{string} = I_{photo} - I_0(e^{\frac{qV_{PV}}{kT}} - 1) = I_{photo,\,shaded} - I_0(e^{\frac{qV_{PV,\,shaded}}{kT}} - 1) \qquad \ldots(2.4.4)$$

Unfortunately, the current balance of the entire series string is now upset by the single shaded cell, and limited by $I_{photo,shaded}$. The rest of the string will reduce its current and drop more voltage across the shaded cell until its leakage current rises to match the new current balance. In the simplest case, the string current drops to match $I_{photo,shaded}$. Evidently, a significant loss in generated power is possible in such a situation.

To mitigate this problem, series connected PV cells are frequently bypassed by reverse

diodes, as shown in Figure 8. Any excess current that the shaded cell blocks then simply passes through the diode. The new operating point is then defined by the intersection between forward diode characteristics and the rest of the PV string as governed by equations:

$$V_{string} = (n-1)\cdot V_{PV} + V_{PV+diode} \quad \ldots(2.4.5)$$

$$I_{string} = I_{photo} - I_0(e^{\frac{qV_{PV}}{kT}} - 1) = I_{photo,shaded} - I_0(e^{\frac{qV_{PV,shaded}}{kT}} - 1) + I_{0,D}(e^{\frac{qV_{PV,shaded}}{kT}} - 1) \quad \ldots(2.4.6)$$

with the additional exponential '$I_{0,D}$' term permitting a higher string current. Note that V_{PV} is probably still negative in this case such that the bypass diode is forward biased. Thus the diode can conduct significant forward current, but the voltage output is equivalent at least to one PV MPP voltage + one diode forward drop. A system setup with bypass diodes can have multiple peaks in its power-voltage curve, requiring an MPPT tracker to follow the global MPP and not get stuck in local maxima as discussed in [39][38]. Current sweep [40] and digital algorithms can be configured to find this global maximum, but this doesn't completely alleviate the underlying problem of power loss.

Even with MPP tracking of the entire string, a dual loss of efficiency occurs: Not only does

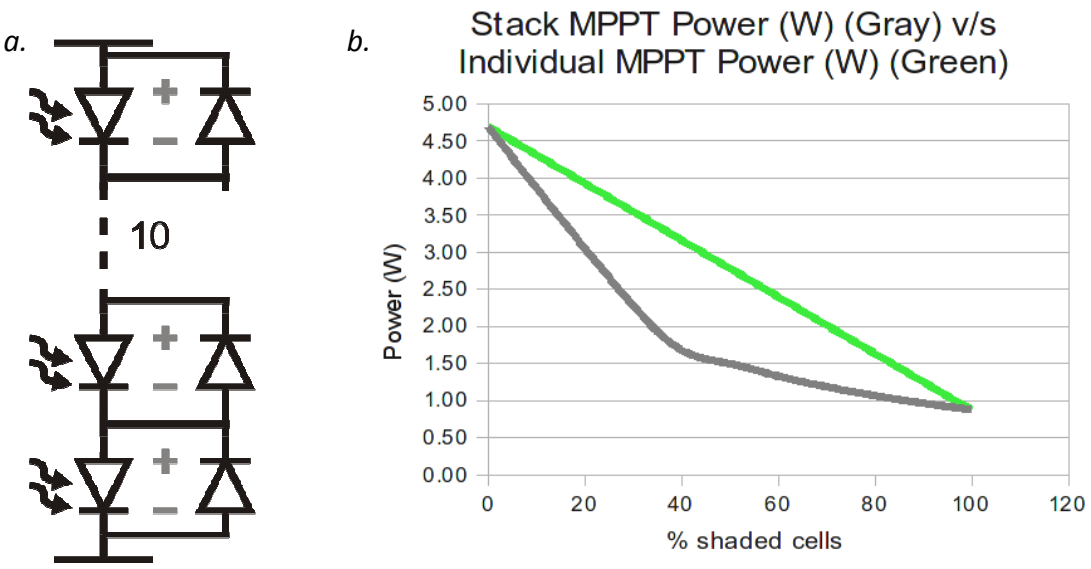

Figure 10: ***Power available from PV cells v/s the power actually delivered*** *– a. a diode-bypassed PV string of 10 cells b. power output under progressive partial shading*

the bypassed PV cell not contribute positive power to the string, but the bypass diode actually consumes some energy depending on its terminal voltage. This loss can become significant as a higher percentage of the string is shaded.

To obtain an estimate of possible losses, a simulation was setup with 10 solar cells bypassed by diodes. Solar cell parameters were taken from commercial cells [41]. The number of cells shaded by 80% was increased, and the power delivered at MPP was tabulated and plotted as the gray curve in Figure 10b. As the gray curve shows, the power drops sharply as the number of mismatched cells increases, eventually stabilizing as all the cells get shaded. Individually, however, the PV cells can generate as much power as shown by the green line, which drops linearly with number of shaded cells. The discrepancy between the green and gray lines shows that the mismatch in cells causes some of the power to be lost in current-balancing of the series PV string. Thus, even with the use of schottky bypass diodes, in partially shaded conditions the PV array can lose significant amounts of capacity, 50% in this simulation but up to 80% in reported cases [42].

In summary, the challenge of partial shading is that the overall MPP of the string is achieved at a different current than the MPPs of each of the cells in the string, shaded and unshaded. In effect, some of the cells operate at lower quantum efficiency, while some get completely bypassed. The green line in Figure 9 shows the opportunity cost (lost power) of global MPP management approaches. Kobayashi et al attempt to solve this problem by tracking individual MPPs for a two-PV cell system in [42]. Although their power converter design improves the power harvested from the system by up to 80% (estimated), the MPP design requires a power converter for each cell. In a larger array, a power converter for each cell would prohibitively increase the footprint and cost of the system, and for microscale systems, a single converter is often the only available option. Finally, to balance strings in parallel, blocking diodes are employed where if the open circuit voltage of the string drops to lower than the power rails, the string is completely cut-off, further degrading harvesting efficiency.

Mismatch in Tandem cells- *Tandem solar cells are compound cells where two or more cells that absorb different parts of the solar spectrum are stacked with a common electrode in*

between [43]*. Though the common absorption area of the two cells precludes partial shading, quantum efficiency mismatch in the two cells and change in the color composition of incident radiation causes the weaker cell to block current from the stronger cell. Loss due to mismatch is the greatest contributor to efficiency loss in tandem cells. Tandem cells are a 'two-string' by construction, with the same active absorption area and a common electrode, traditional diode-bypass methods don't apply since both cells are required to be active simultaneously to achieve the benefit of tandem operation. Tandem cells are revisited in Chapter 3 with a solution to matching their capacities.*

Partial shading can be effectively tackled electrically by array reconfiguration, which is presented in the next section.

2.5 Array Reconfiguration

Array reconfiguration addresses these key challenges identified in PV cell arrays:

1> Weaker cells blocking stronger cells in a partially-shaded string

2> Loss of power from the weaker cells in a diode-bypassed string

3> Loss of power from weaker strings in arrays with blocking diodes

The problems above with mismatch in energy production of PV arrays are caused because the cells are interconnected in a way that causes bottlenecks under mismatch. Array reconfiguration allows the interconnection among cells to be dynamically reconfigured to remove bottlenecks in the energy harvesting process [44].

In the most basic form of reconfigurable array, PV cells are connected to a switching matrix that can be integrated either with the array or with the power converter. The switching matrix is controlled such that cells producing similar current output are connected in series as shown in Figure 11. The connections are reconfigured as required, in contrast to a fixed array where cells next to each other in the series direction are always connected in series. A reconfigurable series connection prevents any partially shaded cells from limiting current through stronger cells. Then, series strings of cells producing similar current output are

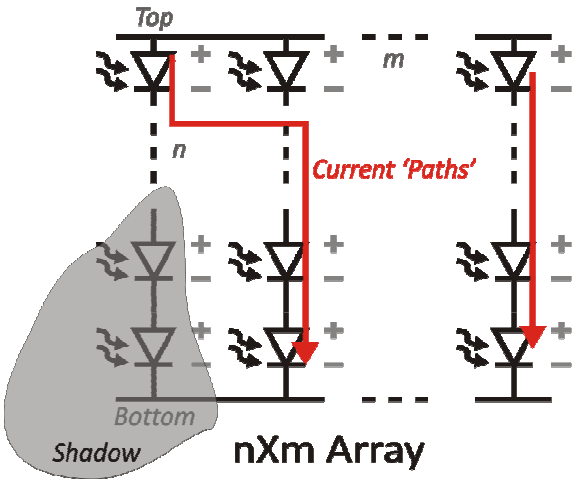

Figure 11: ***Array Reconfiguration*** *– alternative current paths to bypass the shaded cells*

connected in parallel so that the strings in an array all produce a similar output voltage. This is again, in contrast to a fixed array wherein the same strings are connected in parallel with the help of blocking diodes irrespective of their voltage. A reconfigurable parallel connection prevents weak strings from being blocked, allowing most of the array to produce power directly correlated with the amount of incident light. Thus a reconfiguration scheme allows much reduced power losses under variable lighting conditions and PV cell mismatch. However, the changing interconnections in these reconfigurable systems are complex and require some sort of an intelligent sorting algorithm to implement, increasing cost for large arrays and becoming prohibitively complex for ultra-portable systems.

The benefits of array reconfiguration, however, are hard to ignore. Lost energy is recovered under variable lighting conditions at levels comparable to no other approach to solar cell system design. In fact, array reconfiguration is the only technique to recover energy lost in bypass diodes and in the partially shaded PV cells. The design challenge for array reconfiguration is one of capturing these benefits while reducing cost, real-estate, and power penalties to acceptable levels. This work does exactly that by using switching over time (duty cycle) rather than space (location in the array) to obtain the benefits of reconfigurability. The method, called Time Domain Array Reconfiguration, achieves the benefits of reconfigurable interconnections (traditional approaches to reconfiguration) while drastically reducing the complexity and overhead. The TDAR approach is explained in

Chapter 3 at the system level and proposes to improve the state of the art of PV-array energy harvesting by achieving the following three goals:

1> Track the maximum power points of each cell in the array

2> Simplify the switching matrix used in array reconfiguration

3> Use simple analog control loops and processing circuits to reduce power and complexity overhead in the power management system

By using time rather than space to capture individual MPPs, the TDAR uniquely optimizes energy harvesting efficiency in PV array (solar) systems. The next chapter introduces TDAR and examines the tradeoff it provides in PV array management.

3

TDAR System Design

3.1 Introduction

This chapter develops a system design to realize array reconfiguration in a micro-power harvesting system with low power loss and low complexity suited to portable applications. The concept of time domain array reconfiguration is outlined first, and the expected advantages in tackling partial shading are estimated. System design for a prototype microchip is addressed subsequently, and various standard circuit blocks that constitute the system are described. The novel propositions at the circuit level are presented in the next chapter.

3.2 Time Domain Array Reconfiguration (T.D.A.R.)

a. Challenges of Traditional Array Reconfiguration: Portable PV harvesting systems exemplify the challenges encountered in implementing a traditional array reconfiguration system. In a portable system, the harvesting electronics usually operates a small set of PV cells at an optimal voltage (or current) while maximizing battery charging and protecting against overcharge. The energy available for the harvesting electronics to operate on is a fraction of the total system power, usually precluding complex microprocessor and DSP based power control systems. Traditional array reconfiguration is thus prohibitively complex in a micro-power system; however the problems of partial shading that array reconfiguration could solve are still present. In the absence of array reconfiguration, the choices are to either to treat partial shading at an array level rather than cell level with global MPP tracking [45], or to use a single PV cell/parallel cells instead of an array as the energy source [46]. Both alternatives cause loss in harvested energy, in the former case due

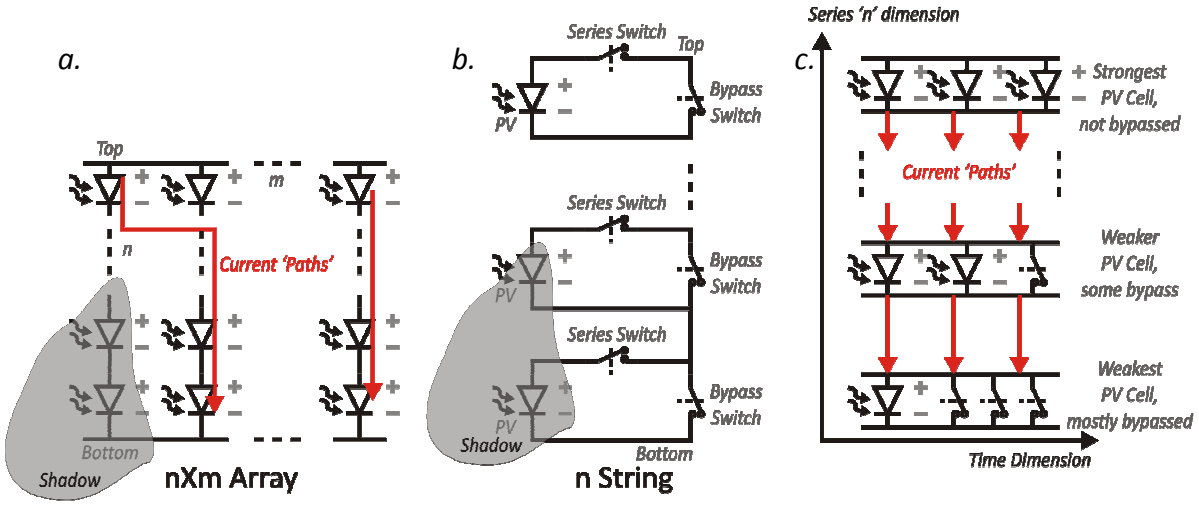

Figure 12: ***TDAR Concept*** *– a: Traditional Array Reconfiguration, b: A TDAR String, c: Conceptual schematic of time-domain routing*

to current mismatch and in the latter, due to low voltage output respectively. In such a system, time domain array configuration (TDAR) presents a new choice with a better three-way trade-off among system complexity, efficiency of each individual PV cell, and overall PV array output voltage. TDAR provides a way to achieve array reconfiguration with a simplified switching matrix and minimal power overhead.

b. 'Stretching' PV cells in the time-domain: When traditional array reconfiguration changes array connections dynamically, it relies on finding a best case path for PV current spatially across the PV array's cell matrix to match strong cells with strong ones and weak cells with other weak cells. Current re-routing inherently requires two dimensions, so that a mismatch along the series dimension can be compensated by routing the current in the parallel dimension to find another series path. The second dimension, however, does not need to be spatial, but can be temporal instead. To illustrate temporal routing, the array can be collapsed in the parallel direction, into a single string of PV cells. Now array reconfiguration is impossible in the parallel spatial dimension, yet TDAR demonstrates that reconfiguration can instead be achieved in the temporal dimension.

Conceptually, with the parallel spatial dimension collapsed, each PV cell can instead be electronically 'stretched' or cloned in the time dimension with the addition of two switches, one that switches a PV cell in/out of circuit, and another that can bypass the PV cell in circuit to keep current continuity in the series dimension. Instead of spatially quantized routing in

the parallel direction in traditional array reconfiguration, the single string of PV cells can now be stretched on a continuous temporal scale. The PV cells with higher power output occupy a longer section of the time scale, while the PV cells with lower power output are extended onto a short section of the time scale. In relation to the 'widest' cell, the 'rest' of the time scale in parallel with every cell is occupied by the corresponding bypass switch. Time Domain current routing is illustrated conceptually in Figure 12c.

Re-routing the string current in time thus makes it spend more time in the stronger PV cells and less in the weaker ones, passing instead through the bypass switches for the weaker cells. Thus although the shaded PV cells are not able to carry the full string current for the entire time, they do so for a fraction of the time required to add their power output to the string power. The average current through each PV cell is then proportional to how much power it generates.

Since each cell can now be scaled on a continuous (time) scale, MPP tracking for individual cells is now possible without sacrificing current continuity, by managing the series and bypass switches. The complex spatial rerouting problem of array reconfiguration is thus collapsed with TDAR into a single-string duty-cycling problem, with each cell simply being in circuit for a time proportional to its power output. Reconfiguring the 'array' thus in the time-domain using a single spatial (or string) and a temporal dimension reduces the switching matrix and control decisions and provides a simpler alternative to traditional array reconfiguration.

c. Maintaining individual cell MPPs: A practical TDAR array consists of a set of PV cells attached to switches and placed in series. If the cells have different power outputs, the switches will connect and disconnect the cells from circuit, bypassing the cells when they are not in circuit. The overall voltage of a PV string controlled by a TDAR system is thus a stepped-voltage waveform with step size equal to the voltage of individual cells, and step timing following switching events in different cells. The voltage never reaches zero, as the strongest PV cell can be in circuit for 100% of the time maintaining a 'floor' voltage level. Thus the strongest cell decides the operating current of the PV string, equal to its MPP current. Every other PV cell is in the series string for a time-fraction proportional to its

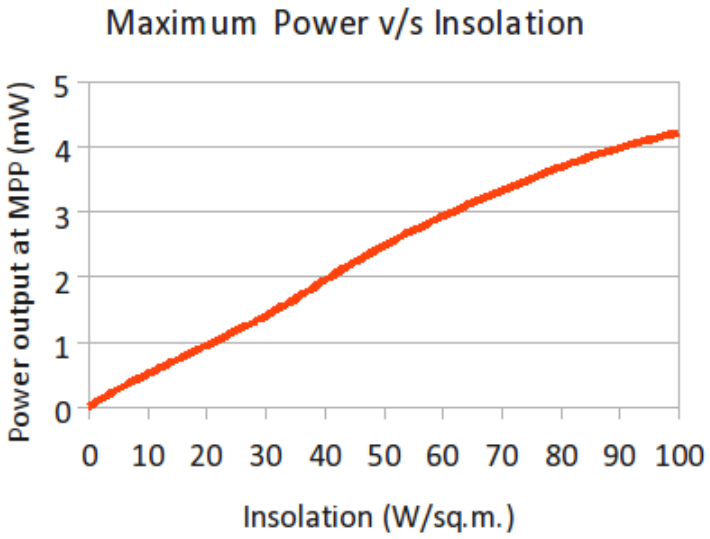

Figure 13: ***Power available in OPV cells v/s Insolation*** *- PV output is almost linear with photon flux over multiple orders of magnitude*

maximum power point and bypassed for the rest of the time, so that the average current through *each series unit* (cell + switches) is still maintained equal to the MPP current of the strongest cell.

To reduce current fluctuations in each PV cell, a capacitor is added in parallel to each cell. The current through each PV cell ripples about its own MPP current, and whenever the cell is switched into the string, any difference in cell and string current is supplied by the parallel capacitor. The capacitor recovers the lost charge from the PV cell when it is switched out of the string.

To illustrate TDAR switching, consider a string of 4 PV cells operating at approximately 0.45V (MPP) each, similar to Figure 12b & 12c. The nominal output of this string is 1.8V at MPP. Say the bottom cell is the best illuminated, and (due to shadows and/or soiling) the other cells are only fractionally illuminated. If the power outputs of these cells are in the ratio 100% : 80% : 45% : 25%, then the voltage output of the string with TDAR enabled could look like Figure 15. Assuming all TDAR cells switch synchronously, for the first part of the duty cycle only the '100% cell' is in circuit. The other cells are switched into circuit as duty cycle progresses, depending on how much they are shaded and how that affects their photovoltaic output as per Figure 13.

Considering 100% illumination to correspond to 100W/sq.m., the duty cycle for each PV cell

will be as per Table 1.

Table 1: ***A partial shading example***

OPV Cell #	*Insolation*	*Power Out*	*Duty Cycle*
1	**100** W/m^2	**4.3** mW	100%
2	**80** W/m^2	**3.7** mW	86%
3	**45** W/m^2	**2.4** mW	56%
4	**25** W/m^2	**1.3** mW	30%

Considering V_{out} for each cell to be 0.45V (Figure 6) in this example of 4 PV cells,

Maximum Output voltage of array if all cells were lit equally = 0.45*4 = 1.8 V

Average Output voltage of 100/85/45/25% shaded string = 0.45*(1+0.86+0.56+0.3) = **1.224 V**

which is about 66% of the maximum voltage output of the array. Note that if a traditional diode-bypass were used, array output voltage would be lower, with strongly shaded cells contributing no voltage and each active bypass diode dropping up to 0.3V (Schottky).

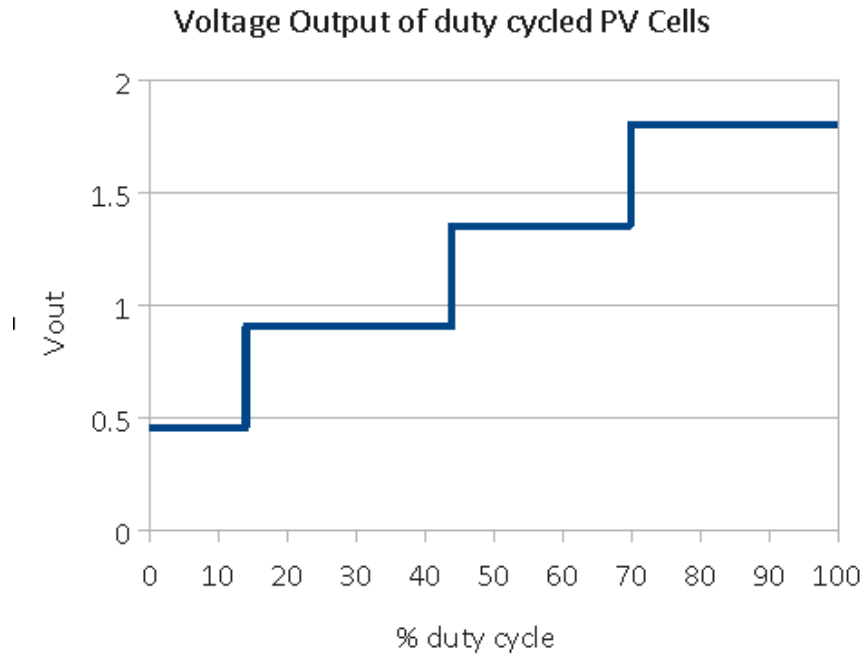

Figure 14: ***Voltage output of duty cycled PV array*** *– assuming the power capacity values of Table 1, time domain array reconfiguration would cause cells to switch into the string one after the other, yielding the above waveform if switch clocks were synchronized.*

Section 3.3 analyzes efficiency gains in this example. This work implements TDAR for a 3-string of PV cells, although this concept can be extended to more complex arrays as discussed next.

d. Extension to parallel cells and tandem cells: TDAR is only a current-equalizing solution for a single string; it doesn't perform voltage-matching for multiple strings. Thus connecting strings in parallel to boost current capacity is not feasible in a basic TDAR system. Instead, to achieve higher current, the fact that a PV cell's V-I characteristics are skewed is used to advantage. Parallel cells are less prone to partial shading than series cells, because current of a PV cells changes proportionally more than cell voltage as a cell is shaded, at operating points close to the MPP. Cell voltages for a strong cell and a weak cell are thus closer in value than cell currents for the same two cells, and consequently when weaker cells are placed in parallel with stronger cells the power loss is much lower than when they are placed in series [6]. Hence to extend the TDAR string back into an array for larger currents, it is possible to simply add cells in parallel to each cell in the string as shown in Figure 14a. The individual

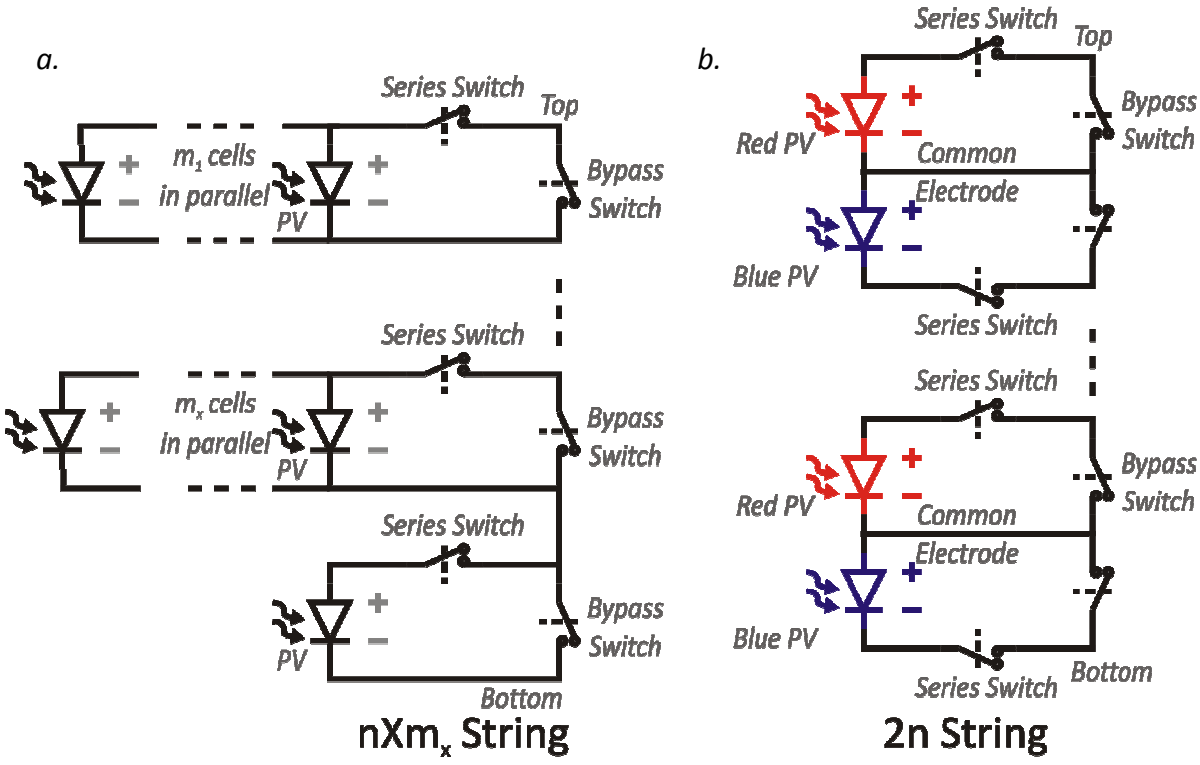

Figure 15: ***TDAR Extensions*** *– a: arbitrary parallel cells balanced by TDAR switching, b: String of 2-tandem cells corrected for mismatch and color-balance changes of illumination*

cell MPP tracker can now track the MPP of this parallel connection of PV cells instead of the original single cell, without a significant loss in efficiency. Different number of cells could also be added in parallel in each TDAR cell, since duty-cycling automatically compensates for power mismatch. This permits flexibility in building the array with an arbitrary number of cells instead of a fixed *n*X*m* configuration as shown in Figure 14a, and can be relevant to portable applications that are size-constrained and use off the shelf PV cells of a fixed size.

As a special case, TDAR can also be easily extended to balance tandem cells which have two constituent cells as shown in Figure 14b. Tandem cells have the unique challenge that one electrode is common between two constituent cells [43]*, with the two cells usually being mismatched in power output. With TDAR power balancing, the 'top' cell can be paired with switches in its cathode connection, while the bottom cell can accommodate switches in its anode as shown in Figure 14b. Thus, say if a 'red-absorbing' cell that was in series with a 'blue-absorbing' cell generated twice the power of the blue cell, the red cell could be in circuit for the whole time while the blue cell is switched at a 50% duty cycle. If the color balance of the input light shifted toward the blue end of the spectrum, the red cell could be operated under variable duty cycle instead, keeping both constituent cells at their MPP. To extend this to a cell string, a series string of tandem cells can also be power balanced, by cascading one pair of MPP trackers per tandem cell as shown in Figure 14b.*

3.3 Expected performance improvements from TDAR

The illustrative example in Section 3.2c lays the ground for several inferences about TDAR:

1> Output voltage of a TDAR system is a stepped waveform.

2> Average voltage from a TDAR string is proportional to the energy being harvested in the string.

3> Individual MPPs can be tracked in a TDAR system independently.

Next, the three types of power gains in the TDAR system are illustrated. When using a conventional diode-bypassed system, the best-case scenario referring to Table 1 is that Cell #4 gets bypassed, and the rest of the array stabilizes at the current flow through Cell #3

(56% of full illumination). Assuming 0.3V is lost in the bypass diode (typical voltage for a schottky diode), the array power output would be the sum of equalized Cells #1, #2 and #3 less the V·I power lost in the diode:

$$P_{byp} = 2.4mW + 2.4mW + 2.4mW - 0.3V \cdot \left(\frac{2.4mW}{0.45V} \right) = 2.52mW$$

However, considering each cell individually, the string can generate upto:

$$P_{MPP,shaded} = 4.3mW + 3.7mW + 2.4mW + 1.3mW = 11.7mW$$

The above two equations illustrate the three types of power lost in a diode-bypassed system:

1> Power lost due to current blocking: In the example, (4.3-2.4)mW and (3.7-2.4)mW are lost in Cells #1 and #2 respectively

2> Power lost from bypassed cell: 1.3mW is lost from Cell #4 when it gets bypassed

3> Power lost in bypass diode: 0.3V·2.4mW/0.45V = 1.6mW is lost in the diode.

All three types of power can be recovered in an ideal TDAR system, preventing a loss of

$$100 \cdot \frac{(11.7mW - 2.52mW)}{11.7mW} = 78\%$$

in this example. A real TDAR system can, of course, expect conductive and capacitive losses in the switches. However this is much lower than the passive losses in a traditional bypassed array calculated above.

An alternative approach to solve the problem of series cells is to simply have a single cell system, or a set of cells in parallel. This eliminates any partial shading problems and MPP tracking can be implemented for the single cell. However, this approach simply transfers the problem of loss in efficiency to later stages in the power harvesting chain. Since single cell voltages are lower than what most contemporary electronics require, a boost converter is added after the PV cells to step the voltage up. Since PV current can vary widely, inductor-based converters are used more often than switched capacitor converters (which are only

efficient for a small range of currents). Most inductor based boost converters have very poor efficiencies at voltages smaller than 1V, effectively losing the efficiency gained by using a single cell approach.

Thus a TDAR system can potentially provide efficiency gains in portable systems. However, a real-world TDAR system would have the following caveats:

1. The quiescent power in the support and control circuits, and the losses in the power path in the power converter should be a low fraction of the power budget.

2. Under partial shading, the average voltage of the PV array will drop as illustrated above. Any boost converter in the following power stages will thus need to tolerate a range of input voltages while being efficient.

3. A TDAR system requires a custom PV array, with both terminals of each PV cell accessible. Series connection of PV cells is through switches in the TDAR systems, which can be a problem in higher power systems.

Table 2: ***Comparison of MPP techniques for portable applications***

Reference	***MPP type***	***Features/Drawbacks***
This Work (Duty Cycling)	**RCC or Load I/V, TDAR**	**Works for both, single OPV strings and larger arrays; simpler than array reconfiguration**
Array Reconfiguration[1,2]	Array Reconfiguration	Complex switching; only applicable to larger arrays
Single PV cell power converter	Multiple options	Simplest, but power converter is inefficient
Integrated battery/OPV cell[3]	Multiple options	Overall low weight; could use time domain reconfiguration!

1 D. Nguyen etal [10] **2** Velasco etal[11]; **3** G. Dennler etal [47]

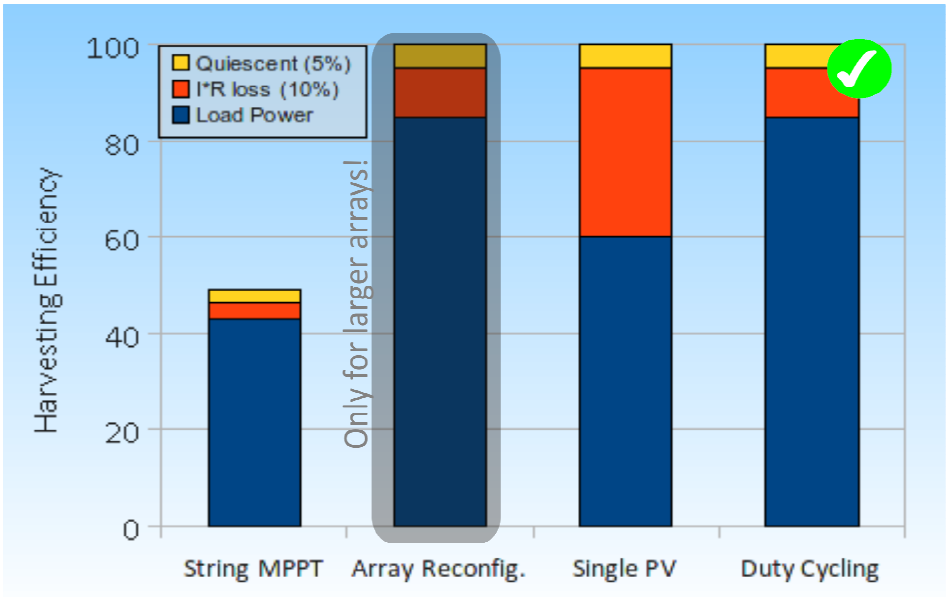

Figure 16: ***The losses in competing MPPT schemes*** *- assuming 5% loss in control circuits (quiescent) and an average of 10% in power switches and inductor resistance. For single string arrays then, duty cycling (TDAR) promises improved efficiency.*

In summary, *Table 2* recounts the major features and drawbacks of this TDAR system when compared to possible alternative approaches.

The bar graph in Figure 18 visually summarizes the types of losses encountered in different MPP tracking methods under partial shading. Quiescent loss is considered an equal proportion of power transferred for all systems. First, as a best-case estimate, fixed-array techniques are considered to convert 50% of the power harvested by the PV cells, although the particular partial shading scenario presented in the previous section puts the losses up to 78%. Next, array reconfiguration can recover this lost energy by pairing cells with similar power outputs, but is not applicable to a single string of a few PV cells. Time domain array configuration is applicable to both single strings and large arrays and hence is most applicable for a portable microsystem powered by a single string of PV cells.

The practical implementation of the micro-power TDAR system is discussed next.

3.4 System Design of the TDAR micro-Power Converter

TDAR can be implemented in a modular system shown in Figure 17. Each solar cell has a dedicated MPP tracker, and the MPP trackers connect into a series string. The input to the

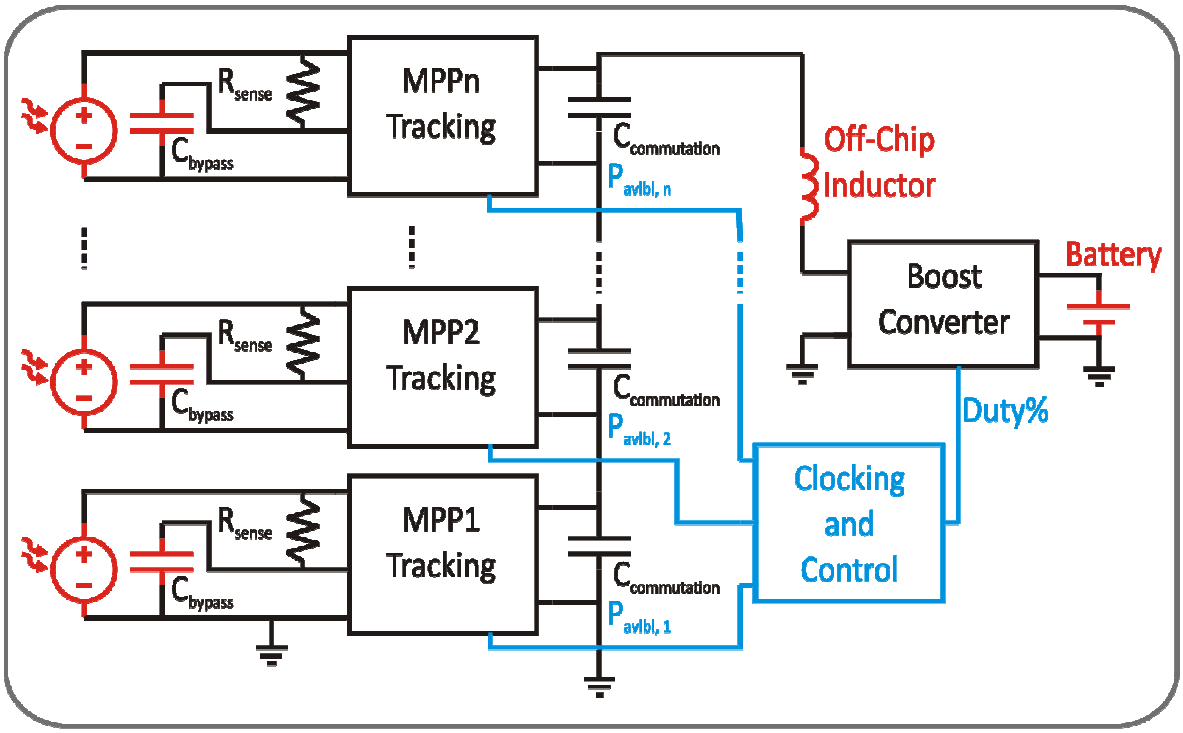

Figure 17: ***PV Power Management TDAR System*** *- A string of n cells is shown. Power path is in* ***black****, control path in* ***blue*** *and off-chip components in* ***red****. In the prototype, n=3 cells.*

boost converter stage is from the top of the TDAR string. Each MPP tracker has a single status output that indicates whether the corresponding PV cell is generating more power than the power demand from the string or whether it is being duty-cycled. The power balance information from all cells is used by the boost control circuitry in conjunction with the battery charge termination detection to control the power switches of the boost converter.

In Figure 17, the off-chip components are indicated in red. Although an integrated system would be ideal for portable applications, the low frequency operation of the MPP trackers pushes some passive components off-chip. The power inductor is off-chip for high-Q and of large value (10mH) to limit operating current. The bypass capacitors for the PV cells are also large enough (1µF) to be off-chip because they filter TDAR switching currents up to 1mA at close to 10kHz with a few millivolts of ripple. The next section discusses the remaining off-chip components in the harvesting chain, which are the solar cells and the battery.

3.5 Power: Source and Sink

a. Power source - Solar Cell: The TDAR system is immune to the type of solar cell being used, as long as the voltage and current capacities are matched to the system. Both Silicon and Organic PV technologies can be used in the system, with potential niche applications. Higher efficiency silicon cells can provide a higher energy per cell area; while organic cells can be lighter in weight, lower in cost, and easier to manufacture in custom arrays on flexible substrates.

While matching PV cells to a TDAR system, power bounds are the primary consideration. The lower power bound is set by losses in the control system and high frequency switching paths, while the upper bound on power transfer is typically set by the resistance and saturation current of the power inductor, and by the 'ON' resistance of the power switch. The prototype TDAR microchip developed in this work can transfer between 100uW and 5mW, with up to 80% electrical efficiency (Figure from Chap 5). This corresponds to an output current of 1.2mA, or an input current greater than 4mA.

Another important parameter while choosing the PV cells is the typical voltage output required. In this work, a 3.7V Lithium-poly battery is charged by the boost converter, and converter efficiency is highest when the input voltage from the PV cells is between 0.9V and 1.8V. Thus a series string of 3 PV cells is selected since at their nominal MPP voltage, the series string provides between 1.25V and 1.5V.

b. Power sink - Load battery and sensor: The load expected in this system is designed for is a portable sensor that runs from a battery. Battery charging rates and sensor power consumption thus determine power specifications of the harvesting system. The power demand of a portable sensor can be erratic as described by Damaschke in [17]. To keep the sensor system operational, battery selection is then governed by two parameters: 1> the highest instantaneous current required by the sensor and 2> the energy capacity required to sustain the sensor system through a typical charge-discharge cycle. For example, a fixed outdoor installation would require the battery to sustain through the night on the charge acquired in daylight hours.

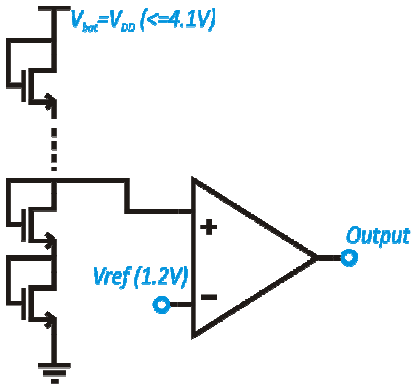

Figure 18: ***Battery Overvoltage Protection*** *- Battery voltage is also V_{DD}. A diode connected MOS ladder steps down V_{DD}, and equals the reference 1.2V when V_{DD}=4.1V*

The average power budget for the portable sensor systems (tags) in the Encounternet project is only 100µW, but temporary demands in power are significantly higher, with current draws greater than 10mA. Lithium-polymer cells [48] are the batteries of choice for the Encounternet project, with high energy density and high charge/discharge currents. Also notable in choosing Lithium-polymer batteries for portable applications are efforts to integrate them with organic PV cells, leading to significant savings in system weight as demonstrated in [20]. The requirements of variable power demand and a high charge current battery, exemplified by the Encounternet project, are common for a majority of portable applications; and the system developed for this application can be scaled easily to most portable PV harvesting systems.

With the selection of a high capacity battery, the permitted charging current of the battery in a typical portable system is higher than the solar cells which fit within the corresponding size constraint can supply. This is especially true for the Encounternet system, with the solar system expected to generate currents that are an order of magnitude lower than the capacity of the battery. Thus the charging profile for the battery in the TDAR harvesting system is simplified to a constant-voltage charge-termination with current-foldback. In effect, when the battery is discharged, the system charges the battery with as much current as the PV cells will supply, and when the battery reaches approximately 4.1V, the system reduces the duty cycle of the boost converter to maintain battery terminal voltage at 4.1V. The 4.1V cutoff voltage detection circuit is shown in Figure 18 and operates by dividing the battery voltage down and comparing the result with a 1.2V reference. Since the battery

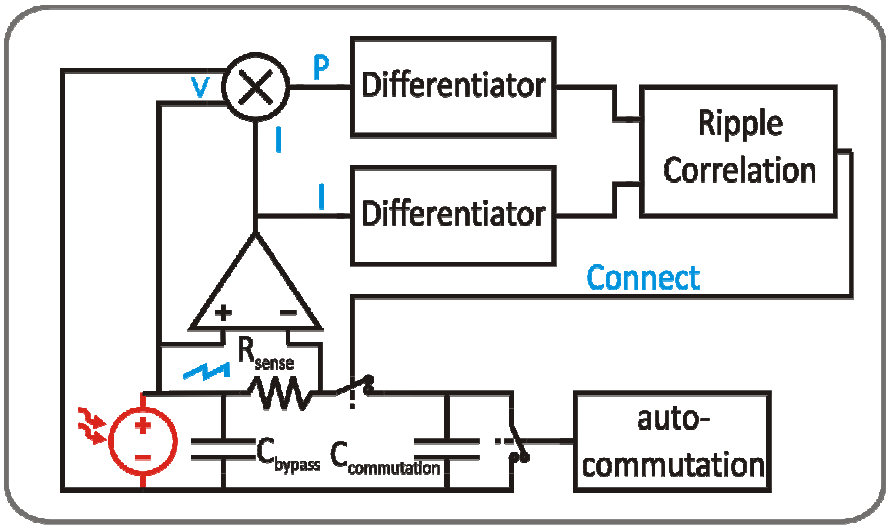

Figure 19: ***TDAR cell architecture*** *– A TDAR cell consists of: commutation and bypass switches and capacitors; a multiplier-differentiator path for power trend-calculation; a differentiator path for current-trend calculation; and a ripple correlation block to digitally correlate the two trends and make control decisions. The auto-commutation block bypasses the commutation capacitor when its voltage falls to 0V.*

voltage doesn't need to be accurate, a simple low-current MOSFET divider is used to divide the battery voltage down to 1.2V. To ensure that the MOSFET divider is sufficiently accurate, Monte-Carlo simulations were run on the divider with process/temperature variations to ensure that the worst-case spread of detected cutoff voltage was within 4.0V-4.2V.

3.6 MPP Control and Array Reconfiguration with TDAR Cells

a. Reconfigurability: The power switches needed to realize time-domain string reconfiguration are setup as shown in the system diagram in Figure 16. The only 'constant' string is the chain of commutation capacitors, from the top of which the boost converter takes its input. Each individual MPP tracking TDAR switching element in Figure 16 is identical, and represented at the block level in Figure 19.

b. Auto-Commutation: Each PV cell is paired with a switch to connect it to the corresponding commutation capacitor in the string, imposing a positive voltage on the commutation capacitor which adds to the string voltage. While the PV cell is in circuit, the string current flows through the PV cell and its bypass capacitor. When the PV cell is disconnected from the string however, the string current switches to the commutation capacitor, discharging it. When the voltage on the commutation capacitor drops to zero, the

bypass switch turns on to shunt the string current and prevents the commutation capacitor from developing a reverse voltage. The turn-on of the bypass switch is achieved by the 'auto-commutation' circuit block.

When the PV cell comes back into circuit, the bypass switch is still on and can short out the PV cell and bypass capacitor. To prevent the bypass switch from shorting out the PV cell, the auto-commutation block monitors the connect signal and ensures that there is a (very short) dead time between when the bypass switch opens and the PV switch closes. During this dead time, the string current again passes through the commutation capacitor, developing a slight negative 'glitch' voltage '$V_{deadtime}$'. A negative voltage across the commutation capacitor leads to a higher swing across its terminals, increasing TDAR switching losses. Hence the commutation capacitor is clamped at 0V by the bypass switch.

Since the PV voltage only ripples about its MPP, the commutation capacitor is the charge storage device that experiences the highest voltage change during a PV switching event. Thus the size of the commutation capacitor directly determines the switching losses during array reconfiguration. If the commutation capacitor is large, TDAR can become inefficient. If the average TDAR switching frequency for a MPP tracker is f_{avg}, the commutation losses are quantified by equation 3.4.1:

$$P_{commutation} = C_{commutation} \cdot \left(V_{PV,MPP} - V_{deadtime}\right)^2 \cdot f_{avg} \qquad \ldots(3.4.1)$$

The size of the commutation capacitor is determined by the maximum expected string current, typical MPP voltage and the the input-offset voltage, gain and response-time of the auto-commutation circuit. A higher string current discharges the capacitor faster, a lower MPP voltage gives the capacitor a lower voltage to discharge from and the input offset, gain and response time of the auto-commutation circuit determines the value of $V_{deadtime}$. In this work, the capacitance value was set through simulation at 1nF, permitting integration on-chip.

c. Current ripple in the PV cell: The bypass capacitor across the PV cell averages the current demand on the cell during the switching commutation events. Thus, the PV current itself ripples about the MPP current, while the bypass capacitor current switches between discharging (string current-PV current) and charging (PV current. The TDAR switching occurs

at close to 10kHz, and to keep ripple within 10% of $V_{PV,MPP}$, the value of the bypass capacitor needs to be 1uF (from the linearized estimate $C=I\cdot\Delta T/\Delta V$). The large size pushes this capacitor off-chip in addition to the inductor. Although the size of the capacitor is large compared to other capacitive nodes in the circuit, the switching losses associated with this capacitor are small due to the small voltage ripple across it.

d. Ripple Measurement: TDAR switching events generate a voltage and current ripple in the PV cell, which is a fortuitous side effect for MPP tracking. The ripple acts as a measure of the trend in power of the PV cell, giving information as to whether the power of the PV cell is increasing or decreasing with a change in current. The control circuit can then change the operating point of the cell to achieve and maintain MPP. As in Figure 19, a 'power ripple' is calculated from the PV cell during commutation as follows: The voltage ripple is measured directly across the PV cell, while the current ripple is measured across a sense resistor. Multiplying the voltage and current waveforms gives the power ripple. The trend of this ripple in correlation to the current and voltage ripples gives information about whether the PV cell is above or below its MPP, as described by Esram et al in [33]. Hence TDAR switching events are not just sufficient, but necessary to maintain each PV cell at its MPP in this system and thus the duty cycle of each PV cell in the system is prevented from saturating at 100% by increasing the power demand from the boost converter whenever a cell reaches higher than 80% duty cycle. Multiplier and differentiator circuits used to calculate power ripple are critical low-power circuits, introduced in Chapter 4.

e. Control strategy for MPP tracking: Switching a particular cell in or out of the harvesting string can either be done with a clocked, pulse-width modulated signal, or asynchronously using the power ripple for direct switching. Since fixed frequency power switching cycles decrease system efficiency at low power levels, and since switching requirements in this system change as a function of relative power levels in the PV cells rather than absolute values, hence an asynchronous switching paradigm was chosen to track MPP in this work.

The goal of the MPP control block is to drive the power switches such that the PV cell's power is always approaching MPP. A decreasing trend in power thus dictates a change in the state of the controlling logic. If the decreasing trend is due to lack of power demand from

the boost converter, the MPP controller can also enable an external 'power available' signal to signal an increase in string current. Assuming then that the string current is always maintained greater than I_{MPP} such that the cell is being duty cycled, the control rules that govern connection of a cell into the string (Connect=1 means cell is in circuit) are in Table 3.

*Table 3: '**Connect' Decision Making***

Rule	***Reasoning***	***sgn(dP/dt)***	***sgn(dI/dt)***	***Connect***
***Maintain** connect if P rising, I falling (V rising)*	Either cell recovering (disconnected), or Power supply exceeds demand (connected)	1	0	***0 → 0, 1 → 1***
***Connect** if P falling, I falling (V rising)*	Cell is under MPP, but power supply still exceeds demand	0	0	***0/1 → 1***
***Disconnect** if P falling, I rising (V falling)*	Power demand exceeds supply, cell is dropping from MPP, put cell in 'recovery'	0	1	***1 → 0***
***Connect** if P rising, I rising (V falling)*	Power demand exceeds supply, but cell will cross MPP (how quickly it crosses decides its duty cycle)	1	1	***0/1 → 1***

Two analog computations are correlated for the connect/disconnect control decision. The first is the power calculation, wherein the multiplier computes the power of the system and the differentiator following it measures its trend (rising or falling). The second path can be either a current or voltage path, with a second differentiator calculating trend. In this system, since a current sense amplifier required by the multiplier is re-used as the input to the second differentiator as shown in Figure 19. Power and current trends are then compared to ascertain required changes in the PV cells operating point. The outputs of both differentiators are digital, and simple asynchronous logic is used to compute the connect/disconnect decision based on a logically reduced form of the rules given in Table 3.

3.7 Boost Converter and Clocking

a. Boost Converter: Voltage boost is realized with a synchronous boost converter, shown in Figure 20. The inductor acts to transfer energy between the input, nominally between 0.5V and 2V, and the output, between 3V and 4.2V for a Lithium-polymer battery cell. The amount of energy transferred is decided by the duty cycle of the switch and the input/output voltage levels. The duty cycle of the gate waveform of the nFET is thus the control variable to be optimized depending on external inputs.

A synchronous design is chosen for the power converter to reduce power loss and voltage drop in the output. The output diode of a standard boost converter is thus replaced by an actively driven pFET with a parasitic body-diode. This 'active-diode' circuit is realized with a fast op-amp that detects the direction of current flow through the pFET and turns it on in the forward direction, and a NAND gate that, in conjunction with a clock delay chain driving the main switching nFET, helps ensure dead time between the pFET turn off and an incoming positive clock edge to prevent crowbar current. The entire boost converter, including the clock and the fast active-diode circuit is up to 88% efficient at 500µA output charging current (Figure 34).

In no-load conditions with a lossless power converter, the output terminal voltage would

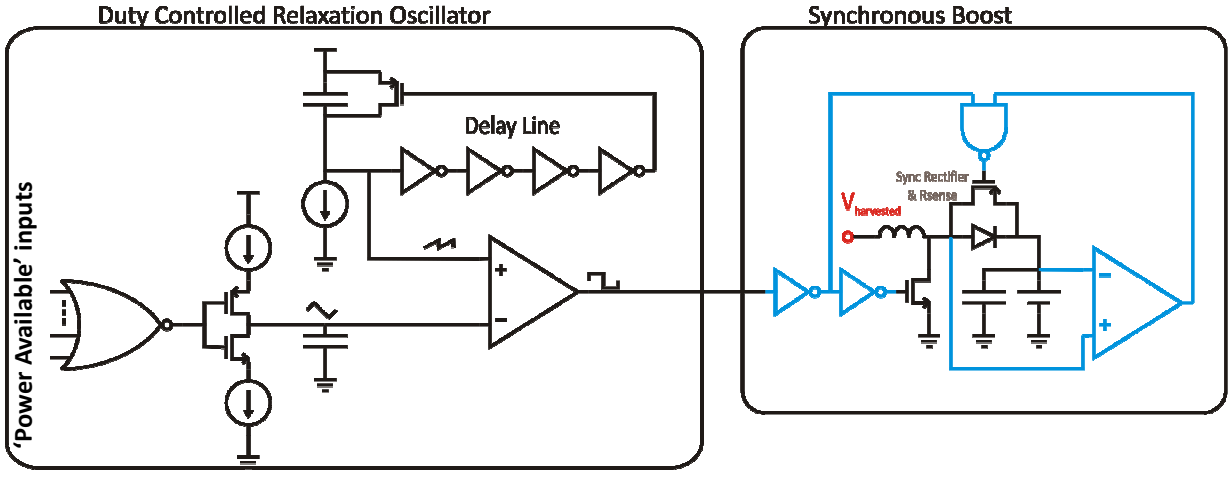

Figure 20: ***The boost converter*** *– A synchronous boost converter, whose duty cycle controls the power transfer from PV cells to battery. The control path in the boost converter is shown in* ***blue*** *and power path in* ***black****. A relaxation oscillator provides a ramp to the comparator which generates the duty cycle controlled clock based on the input control voltage. The control voltage is generated by charging/discharging a capacitor based on PV and battery status.*

depend predictably on the duty cycle. For a battery load with a low equivalent series resistance such as a Lithium-polymer cell however, the output voltage is the battery's terminal voltage. Thus instead of regulating output voltage, the duty cycle of the boost converter effectively controls charging current of the battery.

b. Clocking: The free-running duty-cycle controlled clock for the boost converter is generated on-chip by a relaxation oscillator. The oscillator shown in Figure 20 generates a recurring ramp waveform at approximately 1MHz, which is then compared to a quasi-static PWM control voltage to generate an output rectangular wave with quasi-static duty-cycle. The oscillator is designed to operate at low power, with 1µA current consumption.

The PWM control voltage for the oscillator is either increased or decreased depending on the 'power-available' outputs from the MPP blocks and the charge-termination detection circuit. The duty cycle is always changing, with an average constancy achieved by oscillation about a desired value. The PWM control voltage is thus designed to either rise or fall at a fixed rate that determines the speed of response of the control loop. Control voltage change is achieved in circuit by charging and discharging a capacitor in response to the digital control inputs from the MPP and charge termination blocks. The charging/discharging currents are roughly matched, and their value determines how fast the PWM control voltage can change. Since the control loop is governed by status outputs from the MPP blocks, the speed of response of the PWM control loop is set to be about 10x slower than the MPP control loops, making it the slowest control loop in the harvesting system.

The following rules dictate any changes in boost converter duty cycle in this system:

1. MPP tracking is by ripple correlation control (RCC), deciding the fraction of time the PV cells are in circuit. RCC is able to track the true MPP of PV cells only as long as a ripple is present on the PV cells. This means the PV cells ideally never go to a 100% time in the string, and hence each MPP block is designed to keep the PV cell in circuit for a maximum of roughly 80% duty-cycle. *The duty cycle of the PWM is thus increased if any of the MPP blocks asserts the 'power-available' signal.*

2. The battery charge level decides whether the power converter operates in voltage-

limited mode. As mentioned before, the maximum charging current the battery can take in a typical portable system exceeds the PV harvested current. Hence charging is only limited during charge-termination. A maximum-current/constant-voltage method is thus chosen for output regulation. Constant-voltage means the charging current will be folded back rather than cut-off when the battery charges to its maximum voltage (~4.1V). The monitoring circuit is presented in Figure 18. W*hen the battery monitoring circuit asserts its output, the duty cycle of the PWM is decreased.*

The boost converter duty cycle is thus either increasing or decreasing. This causes small oscillations in operating point about the optimal value, but ensures that the system is resilient to drift that affects many hill-climbing systems. Control loop stability is required to ensure system stability during this operating point oscillation. Table 4 summarizes the operating modes of the system. The rules are implemented by the control circuit realized in Figure 19. The low power multiplier and differentiator circuits required to compute the operating point of the PV cell are introduced in the next chapter.

Table 4: ***Power transfer*** *(duty-cycle) change table for boost converter*

PV ***MPP*** *duty cycles*	*Battery Voltage < 4.1V*	*Battery voltage >= 4.1V*
Either *greater than 80%*	Increasing	Decrease until Voltage <4.1
All *Lower than 80%*	Decreasing until at least one cell >80%	

4

Low power circuits: 'C.L.M.' Multiplier & Differentiator

4.1 Introduction

In a micro-power photovoltaic harvesting system, implementation of control and measurement circuits is a challenge due to limited available energy and limited chip/circuit board real estate. Power and weight constraints make analog signal processing a good choice over more complex digital signal processing for the MPP tracker system. This chapter continues describing the TDAR system outlined in Chapter 3, with a focus on the critical low-power multiplier and differentiator circuits that are at the heart of individual maximum power point tracking in this work. The MPP tracker is a modified ripple correlation control (RCC) system, which yields itself to implementation with analog signal processing and simple control loops. RCC [49] correlates the power-ripple with either the voltage or the current-ripple, as shown in Figure 30, to decide whether the PV cell is below or above the MPP. Usually, the ripple is caused by a following power converter independent of the control loop. Typical power converters generate a ripple of frequency in the 100kHz-1MHz range.

The RCC control loop in this system, shown in Figure 30, is implemented differently. To reduce both operating power and precision required for ripple measurement, the 1MHz ripple introduced by the boost converter in this system is ignored and filtered by the bypass capacitor. Instead, the ripple caused by the TDAR switching is used for correlation, affording a significant saving in power. TDAR switching of a PV cell in and out of circuit occurs in the range of 10's of kHz in this system, and the change in PV voltage is of the order of 10's of mV. This provides a lower frequency and higher amplitude signal to the RCC measurement circuits compared to the 1MHz boost converter ripple, relaxing performance constraints on the measurement circuits.

Since the 'ripple' or voltage/current changes in the cell are actually caused by the control

loop itself, rather than being a by-product of the following switching stage, the system can thus be considered to be an analog-domain 'derivative feedback' MPP system rather than a pure RCC system. A control decision occurs every 'half cycle', when the cell is connected or disconnected, and the ripple is not of a fixed frequency. However, a regular switching action is required for this system to operate, which differentiates it from a pure derivative feedback system, and introduces similarities with RCC systems. Further, due to the available option of using regularly clocked TDAR switching and constant-frequency switching, this work continues to treat the system as a variant of ripple correlation control.

Referring to the system in Figure 30, a multiplier to measure power and a differentiator to compute the direction of power and voltage change for ripple-correlation are the key circuit blocks that transform the analog PV operating point into digital ripple-correlation decision variables, enabling correlation in asynchronous logic.

4.2 Channel Length Modulation (CLM) based Multiplier

a. Principle: For ripple correlation, the power waveform of the PV cell needs to be calculated, given the voltage and current waveforms. The channel length modulation (CLM) multiplier performs this task of current-voltage multiplication. Multiplying PV cell voltage and current defines specific challenges for the multiplier, which the CLM multiplier is well suited to handle as described next.

PV current is usually measured across a resistor placed in series with the PV cell. Since the PV terminal voltage is a few hundred millivolts, this current sense resistor can only drop a few millivolts for full-scale measurement to prevent significant power loss during measurement. Thus the sense voltage is a 'small-signal' waveform. The other half of the power ($P=V\cdot I$) expression is the PV cell voltage which ranges from 0.3V to 0.6V, and is a 'large-signal' waveform from CMOS circuit considerations. A multiplier that calculates PV power thus needs to have asymmetrical inputs with one small-signal input (a small voltage on the order of millivolts) and one large-signal input (on the order of half a volt). Both inputs need to be differential, since measuring PV voltages and currents in a string configuration means that the sense and PV voltages are differential, with a common-mode offset that

depends on the position of the PV cell in the string. The voltage on a PV cell's terminals can range from the 'bottom' of the string (measuring 0 to 0.6V) or the 'top' of the string (for a three-cell string, this could mean measuring 0.9 to 1.2V). The common-mode input range of both differential current and voltage inputs of the multiplier thus needs to be from 0V to the maximum PV string voltage, close to 1.2V for this work. These voltages can vary both quickly and gradually, precluding simple ac-coupling to remove the common mode. Thus the multiplier inputs need to be robust differential inputs.

Finally, in order to ensure high efficiency, micro-power MPP tracking needs measuring circuits that are at least an order of magnitude lower in power consumption than the power transferred by the system. Thus for this work, the power budget of each multiplier in the MPP circuit is of the order of 1-10µW, which is a challenging metric. While saving power, the speed of the measuring circuit still needs to be fast enough so that the response of the MPP control loop is accurate and stable in response to changes in light conditions, in this case, on the order of 100µs. Multipliers are discussed in [50] and present problems with power consumption and input voltage swing. Linear multipliers that depend on variable transconductance or linear-region MOS channel 'resistance' accept input voltages at either the gate or source terminal of FETs, and thus tend to have a 'small-signal' input range. Instead, a drain-input was considered for the PV voltage input in this work, giving rise to the idea of a channel length modulation based multiplier. The difference in the small-signal and large-signal nature of current and voltage measurements in PV power measurement can be resolved effectively by a 'channel-length-modulation' based multiplier circuit, where the small signal input (the current measurement) controls current through an FET from its gate and the large signal voltage (representing the PV cell voltage) is imposed on its drain to modulate this current as shown in Figure 21.

For a single FET, the two inputs lead to the following relation (approximated considering a linear channel length modulation effect, nonlinearities are discussed later in the chapter):

$$I_d = k \cdot (V_{gs} - V_t)^2 \cdot (1 + \lambda \cdot V_{ds}) = I_{d,0} \cdot (1 + \lambda \cdot V_{ds}) \qquad \ldots(4.2.1)$$

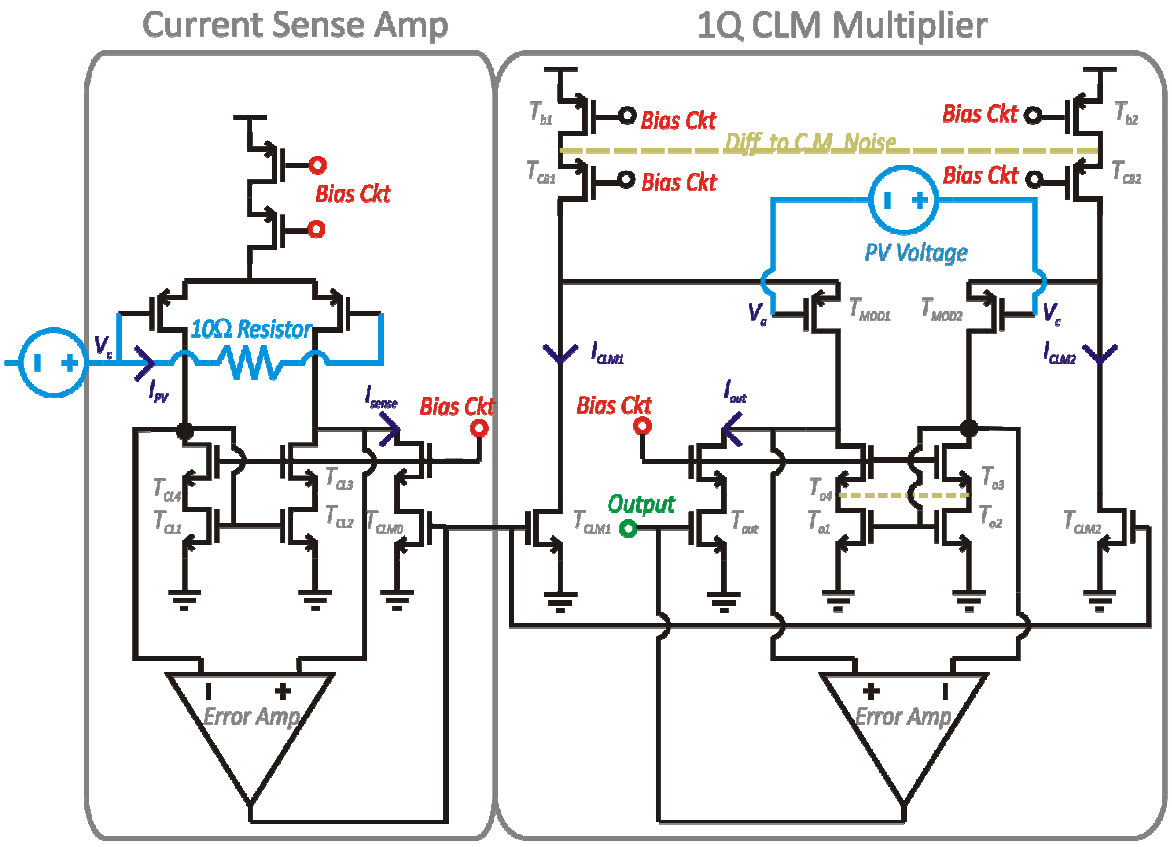

Figure 21: ***The channel length modulation based multiplier*** *– A current sense amp mirrors a current proportional to the PV current into $T_{CLM1,2}$. The PV voltage is differentially applied to the drains of $T_{CLM1,2}$ and multiplies with the current due to channel length modulation. This differential product current is then extracted into T_{out} and mirrored into the next block as output. Error amplifiers keep the load current mirrors accurately balanced.*

Where λ is the linearized channel length modulation parameter and $I_{d,0}=k\cdot(V_{gs}-V_t)^2$. It is evident from the right-hand-side of the equation that a proportional term ($I_{d,0}$) and a product term ($\lambda\cdot V_{ds}\cdot I_{d,0}$) combine to form the final drain current of the transistor. If the proportional term is balanced out by a differential topology, the product term can be isolated, yielding the pure multiplied product as an output current. V_{ds} represents the voltage across the PV cell, $I_{d,0}$ is proportional to PV current. The exact relation of $I_{d,0}$ and V_{ds} to PV current and voltage respectively is discussed later; it is sufficient to assume here that they are both linear functions with constant multipliers. The parameter λ is also assumed a constant multiplier, and variation of λ is addressed separately.

Since V_{gs} and V_{ds} are both required to be positive values, a single CLM multiplication is single-quadrant. Extension to more quadrants requires either a base offset in both inputs, or

a differential topology. However, in PV power measurement for MPP tracking, the voltage and current are unidirectional, making it a single-quadrant problem as long as the PV cell is generating power. Thus a single-quadrant CLM multiplier is developed first before discussing extension to more quadrants.

b. Operation: The novel CLM multiplier circuit developed for this work is presented in Figure 21. In the scheme of multiplier classification as presented in [50], this multiplier would classify as a voltage-current, saturation-mode, programmable-transconductor multiplier. In fact, the CLM multiplier is the only circuit that falls under this classification, and is hence uniquely suited to this application over other topologies.

In Figure 21, T_{CLM1} and T_{CLM2} are transistors that implement channel length modulation as described by equation 4.2.1. A current proportional to the current through the PV cell is mirrored through the transistors by the current sense amplifier, and the PV voltage is then imposed on the drain nodes of the CLM transistors through the common-drain action of the folded cascode 'modulation' transistors T_{MOD1} and T_{MOD2}. T_{CLM1} sees the anode voltage at its drain and T_{CLM2} has the cathode voltage applied to its drain. Both drain voltages are offset by the threshold voltages of $T_{MOD1,2}$. These threshold voltages are assumed to be equal, which is easily ensured by making the transconductance of the $T_{MOD1,2}$ transistors high compared to the drain impedance of $T_{CLM1,2}$. With a high transconductance, the change in drain current from $T_{CLM1,2}$ due to channel length modulation generates very little change $\Delta V_{GS}=\Delta I_D/g_m$ for transistors $T_{MOD1,2}$, essentially operating them at matched gate-drive voltages.

The drain currents of $T_{CLM1,2}$ are a sum of the gate-induced current and the channel-length-modulated product of the current and a single ground-referenced PV terminal voltage (anode or cathode) as explained in equations 4.2.2 and 4.2.3. The proportional gate-induced term needs to be removed to isolate the product term, which is achieved by taking the differential of currents from $T_{CLM1,2}$. Since the two branches are matched, the gate induced currents are equal and hence cancel in the difference as shown in equation 4.2.4. Taking the difference of the two currents also achieves the task of removing the common mode voltage from the PV terminal voltages applied to the gates of $T_{MOD1,2}$. The differential of the two drain currents, is thus purely proportional to the product of the PV current and voltage with

proportionality factors of the gain of the current-sense amplifier and the channel length modulation coefficient 'λ'. If PV anode and cathode voltages V_a and V_c are imposed on the gates of $T_{MOD1,2}$ respectively, then

$$\because I_{CLM1} = I_{CLM0} \cdot [1 + \lambda \cdot (V_a + V_{gs,MOD1})] \quad \ldots(4.2.2)$$

and

$$\because I_{CLM2} = I_{CLM0} \cdot [1 + \lambda \cdot (V_c + V_{gs,MOD2})] \quad \ldots(4.2.3)$$

$$\therefore I_{out} = I_{CLM1} - I_{CLM2} = \lambda \cdot (V_a - V_c) \cdot I_{CLM0} \quad \ldots(4.2.4)$$

where $V_{gs,MOD1}$=$V_{gs,MOD2}$ as explained earlier. I_{CLM0}=I_{sense} is proportional to PV current by action of the current sense amplifier, thus making I_{out} proportional to the product of the PV voltage and current (equation 4.2.4). I_{out} is extracted into T_{out} by action of the differential cascode load on $T_{MOD1,2}$, formed by transistors $T_{o1\text{-}4}$. In the absence of the error amplifier and T_{out}, the impedance of the differential cascode load would generate an output voltage at the drain of T_{O3} that is proportional to the difference of the current in the two branches, I_{CLM1}-I_{CLM2}. However, this voltage now forms the input of the error amplifier, which drives T_{out} to shunt any excess current in the T_{CLM1} branch out of the differential load, keeping the load balanced. This converts the voltage mode output back into a current mirror output. Since T_{out} is only able to shunt current with a zero initial bias, the circuit is limited to single quadrant operation.

c. Voltage Input: To keep all the FETs in the CLM multiplier circuit in the saturation region, the voltage swing for the PV voltage input is limited at the low end by the nonlinearities in the $T_{CLM1,2}$ transistors which makes the maximum drain voltage approximately 0.25V, making the voltage at the gate of the $T_{MOD1,2}$ transistors approximately equal to -0.15V, and at the higher end by the drain saturation voltage of the current source and the threshold voltage of the modulation transistors (approximately V_{DD}-0.5V). In this work, the multiplier operates from the output Li-poly battery, thus V_{DD} is at least 3.5V, putting the upper limit to PV voltage at 3V. This is sufficiently large for an input PV string of up to 5 cells.

d. Current Input: The current mirrored into $T_{CLM1,2}$ ($I_{CLM1,2}$) is generated by a differential transconductance amplifier that linearly transforms the differential voltage across a sense resistor to an output current in T_{CLM0}. The on-chip sense resistor is designed to be nominally R_{sense}=10Ω so that with a PV current range of 0-1mA, the resulting voltage across the sense

resistor will be a 10mV full-scale. The transconductance gain (G_s) of the current sense amplifier is of the order of 1µS, generating a 10nA full scale of differential output current in the output load T_{CL1-4}. This differential output current is shunted as I_{sense} into T_{CLM0} by the error amplifier in a similar fashion to the multiplier circuit. Thus

$$I_{sense} = I_{PV} \cdot R_{sense} \cdot G_s \qquad \ldots(4.2.5)$$

Because the sense resistor voltage is small-signal, the linearity between the output differential current I_{sense} and PV current is high. In this work, the multiplier circuit is biased to handle 80nA full-scale I_{sense}. This value of I_{sense} is larger than the expected typical output of the sense amplifier, to accommodate the range of possible PV currents comfortably with P,V,T variation and deviation in PV cells from expected values.

Channel length modulation can cause mismatch between the T_{CLM0-2} current mirror transistors. The drain of T_{CLM0} is thus set close to 0V, to minimize channel length modulation on its drain. Thus the current mirrored into $T_{CLM1,2}$ is directly proportional to the current through the sense resistor, with 0A offset and 50nA full scale.

Since the channel modulation parameter is of the order of 1%, I_{out} is close to 1nA full-scale due to summation of currents from both $T_{CLM1,2}$. From equations 4.2.4 and 4.2.5, then, I_{out} is proportional to the product of PV voltage and current, without any offset:

$$I_{out} = R_{sense} \cdot G_s \cdot \lambda \cdot I_{PV} \cdot V_{PV} \qquad \ldots(4.2.6)$$

I_{out} the ideal multiplier output from the CLM multiplier. Thus R_{sense} allows for higher current scaling of the circuit, when either larger PV cells or parallel connected PV cells are used in higher power applications. In this circuit, the expected value of the multiplier gain is $G = R_{sense} \cdot G_s \cdot \lambda = 10^{-7} V^{-1}$. For a given current in the PV cell, R_{sense} is limited by the voltage it can drop while preserving efficiency (few mV). Hence a change in the overall multiplier gain can be achieved by increasing G_s or introducing gain in the current mirror T_{CLM0-2}.

I_{out} is mirrored into the next stage, which is the differentiator circuit dealt with later in the chapter. Non-linearities in I_{out} are discussed next.

e. Non-Linearities: So far, the equations given above assume a linear channel length

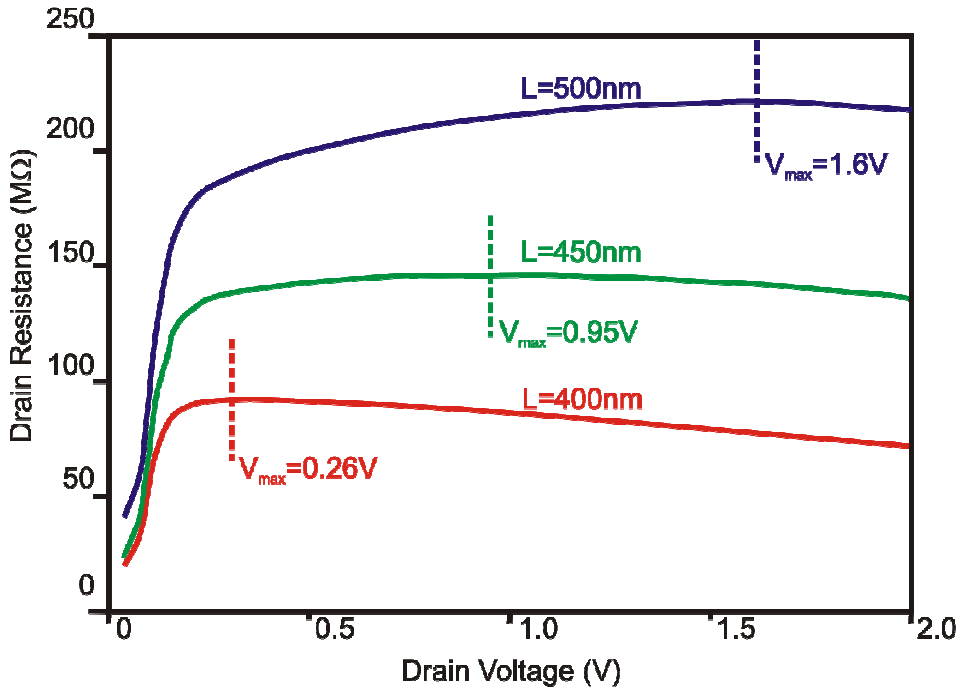

Figure 22: ***Drain 'resistance' r_{out} vs. transistor channel length*** *- L=450nm shows the least variation across a voltage range of 0.5V-2V, implying modulation parameter λ is most constant for L=450nm in the IBM13 process technology.*

modulation parameter 'λ', applicable at micron-scale transistor geometries. At sub-micron scale, however, the channel length modulation parameter is typically non-linear albeit of a higher value. The non-linearity of channel length modulation can be significant, and needs to be addressed in the design of this multiplier based on this effect. Channel length modulation causes an effective differential drain resistance r_{out} to appear at the drain of the transistor. This r_{out} is plotted against drain voltage for different values of channel length in Figure 22.

The variation of r_{out} with drain voltage is more than 33% across the 0.5V to 2V range for transistors with channel length 500nm and 400nm in the IBM13 technology as shown in Figure 22. The key redemptive factor then, that still enables linear CLM circuit design in sub-micron, is that the first derivative of the CLM voltage coefficient changes sign at a voltage that is dependent on channel length.

As seen in Figure 22, the switch in the first derivative of r_{out} is at a 0.26V for a channel length of 400nm and at close to 1.6V for a channel length of 500nm, indicating that an intermediate channel length might put the critical voltage in the middle of the 0.5-2V

voltage-range of interest. For IBM13, this length was found to be 450nm through simulation. As shown in Figure 22, the switch in the trend for the channel length modulation parameter across the 0.5V to 2V voltage range occurs at close to 0.95V for a 450nm transistor, reducing the overall change in channel modulation coefficient to only 4% in the 0.5V to 2V range. The constancy in the channel length modulation parameter translates to a linear multiplier characteristic. Thus $T_{CLM0\text{-}3}$ were given a 450nm channel length, yielding maximum multiplier linearity. A caveat to this selection of critical channel length through simulation is that it is dependent on how accurately the V_{ds}-related non-linearities are modeled in the BSIM model supplied by the technology vendor.

Non-linearity also occurs in the output transistors T_{CLM0} and T_{out} at low current levels, when the non-linear V_{gs}-I_d relationship is not sufficiently compensated by the feedback of the error amplifier. In this work, non-linearity due to low current was only observed in simulation when current values dropped below 10pA in T_{CLM0} or T_{out}, which is less than 1% of full scale. The harvesting system in this work is not setup to transfer power efficiently when at less than 1% of the rated power, thus this non-linearity does not affect performance of the control loop.

f. Stability: The error amplifiers are the only closed loops in the multiplier, and need to be compensated for stability due to high-gain in the loop. Since the amplifier still needs to respond to changes in the kHz range to enable power tracking, compensation was selected accordingly. A miller capacitor was added to the error amplifier circuit to achieve stability with minimal capacitance area. After stabilizing the error loops in the CLM multiplier, the frequency response was over 100kHz which is sufficient for MPP tracking in portable systems.

g. Noise: Since the multiplier operates at very low currents at which the subsequent circuits are noise sensitive, noise reduction is a significant concern in this system. Given a signal level, noise reduction in a CMOS process is typically achieved by adjustments to the transconductance (shot noise, which increases with g_m) and transistor geometry (flicker noise, which reduces with larger transistors) of the transistors. Although the geometry of most transistors in the CLM multiplier itself is variable due to the self biasing nature of the

folded cascode topology, the bias current-source PMOS transistors $T_{B1,2}$ are sized based on global biasing current-mirror transistors and are less adjustable. Since these bias transistors are part of the signal path in the original CLM multiplier, they cause significant contributions to noise in the circuit.

On the other hand, the cascode bias transistors $T_{CB1,2}$ in the PMOS sources are degenerated by the current sources, and hence have minimal contribution to noise. To reduce the noise contribution of the PMOS current sources $T_{B1,2}$ to the circuit, the differential current sources were merged into a single current source as shown by the dashed lines in Figure 21. This changes the bias noise sources $T_{B1,2}$ from differential to common mode, eliminating their contribution to noise figure. The now-source-connected $T_{CB1,2}$ cascode transistors isolate the two signal branches.

Since the cascode transistors $T_{CB1,2}$ are now source-coupled, T_{CB1} is a common-gate load to T_{CB2} and vice versa. Thus $T_{CB1,2}$ are no longer source-degenerated and thus become the noise contributors in lieu of $T_{B1,2}$. However, unlike $T_{B1,2}$, $T_{CB1,2}$ can be adjusted in geometry. Their size can be increased to reduce flicker noise and hence overall noise figure at 10kHz.

A similar differential-to-common-mode change was made in the cascode differential load. The drain terminals of the load transistors $T_{L1,2}$ are maintained at almost the same voltage by the cascode transistors $T_{CL1,2}$. Hence, connecting the drains together as shown by the dashed line in Figure 21 maintains circuit function, and eliminates the noise contribution of the load transistors $T_{L1,2}$ without sacrificing differential load action. The new noise sources are again, the cascode transistors $T_{CL1,2}$, which can then be made larger without significant consequences to the circuit. The ($g_m.r_{out}$) value of the cascode transistors does reduce with increase in length, causing a loss of cascode transistor action, which places limits on increasing their geometry significantly. In this design, the size of the transistors was increased by 10x to reduce noise. Between the bias transistors and load transistors, significant noise figure reduction was achieved by converting differential noise sources to common mode sources.

h. Layout for matching, noise immunity: The layout of the CLM multiplier needs careful attention for two reasons:

1> The differential elements need to be matched as closely as possible to ensure removal of proportional and quiescent terms from the final multiplied output and

2> The low operating currents (on the order of nA) make the circuit sensitive to substrate noise, requiring careful layout to reduce substrate coupling.

Transistor interleaving, dummy transistors at the end and V_{dd}-gnd guard rings around matched pairs were all techniques used in the layout of the multiplier. Matching interconnect lengths was less of a concern due to low frequency, low power operation. The layout of $T_{CLM1,2}$ is shown in Figure 24 as an example. The outermost 'blue' metal half-rings are connected to transistor drains, while their sources form the common ground terminal. Two diffusions are utilized to realize the transistors and to reduce the dimension along the length of transistors for closer matching. The transistors are fingered (divided into multiple parallel transistors) and interleaved (each successive finger is alternately T_{CLM1} or T_{CLM2}). Dummy fingers with grounded gates are added at the ends of each diffusion, as the end transistors in a diffusion area tend to match the worst with the central fingers. This transistor has a ground guard ring, which prevents stray noise currents flowing in the p-

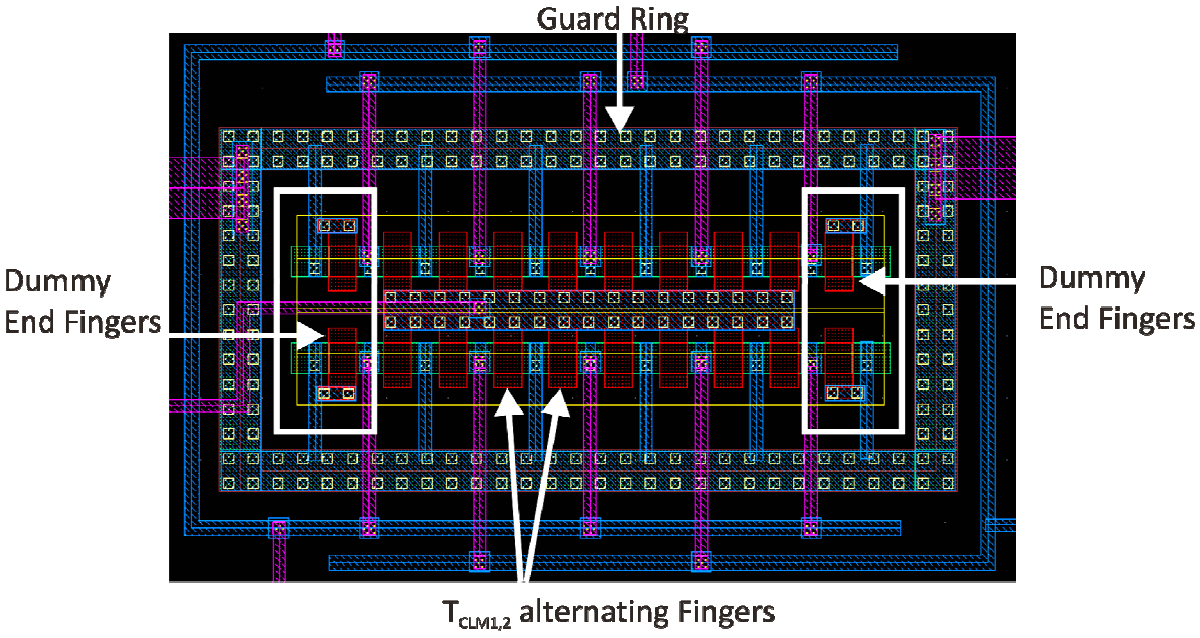

Figure 23: ***Layout for matching and noise immunity*** *– Interleaved fingers, dummy diffusion-ends and guard ring*

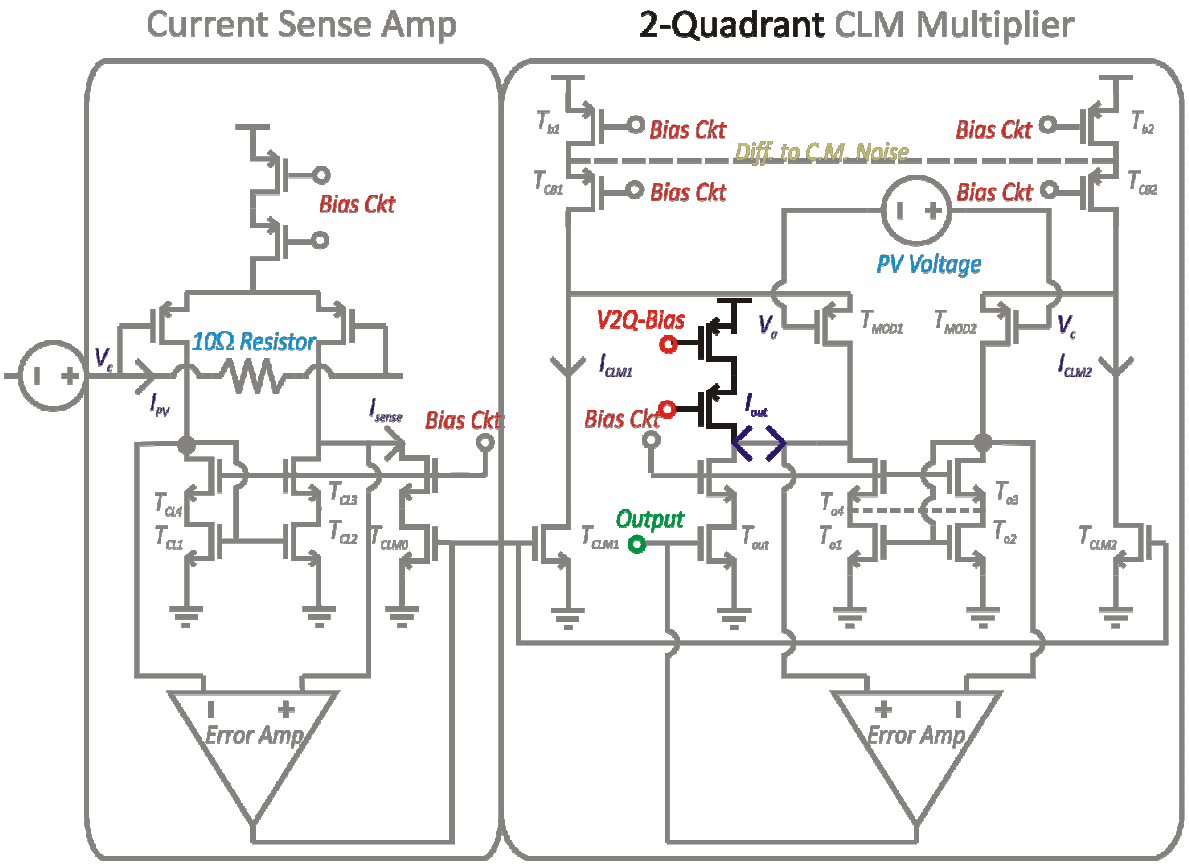

Figure 25: ***The 2-Q I-V multiplier*** *– Addition of a current source at the output stage converts the CLM multiplier to a 2 quadrant multiplier accepting 'negative' voltage inputs.*

substrate from contaminating the signal currents flowing through the two transistors.

i. Conversion to two-quadrant multiplication: The multiplier implemented using this unique channel length modulation approach to obtain a product is a single quadrant multiplier, which is applicable to a PV power measurement application. The multiplier by itself can also be useful in other applications which require low-power current-voltage multiplication. Extending to 'negative' current values can be challenging with this multiplier due to proportional terms that need extra CLM branches to balance out, but extension to two quadrants for the voltage input is easily achieved. The only factor limiting two-quadrant operation is the fact that the output stage of multiplier is set-up as a current sink with '0' offset, in the form of T_{out}. If this was changed to a current source/sink, or an offset current was added as shown in Figure 25, two-quadrant operation could be achieved with a known output offset.

j. Four-quadrant multiplication: Extension to four quadrants can be achieved by introducing additional CLM branches to balance the dc-offset in the input current, as shown in Figure 26. The critical caveat in this circuit is the matching of all CLM transistors and of the two I2Q-Bias current sources. The 4Q-Bias setting on the output branch is a range-setting value to prevent clipping of the output, rather than being an accurate bias current. If the DC offset current in T_{CLM0} is I_B, then the equations 4.2.1 through 4.2.5 modify thus:

$$\because I_{CLM1} = I_{CLM2} = I_{CLM0} = I_{sense} + I_B$$

$$\because I_{CLM4Q1} = I_{CLM1} + I_{CLMB2}$$

$$= (I_B + I_{CLM0}) \cdot [1 + \lambda \cdot (V_a + V_{gs,MOD1})] + I_B \cdot [1 + \lambda \cdot (V_c + V_{gs,MOD2})]$$

and

$$\because I_{CLM4Q2} = I_{CLM2} + I_{CLMB1}$$

$$= (I_B + I_{CLM0}) \cdot [1 + \lambda \cdot (V_c + V_{gs,MOD2})] + I_B \cdot [1 + \lambda \cdot (V_a + V_{gs,MOD1})]$$

$$\therefore I_{out} = I_{CLM4Q1} - I_{CLM4Q2} = \lambda \cdot (V_a - V_c) \cdot I_{CLM0}$$

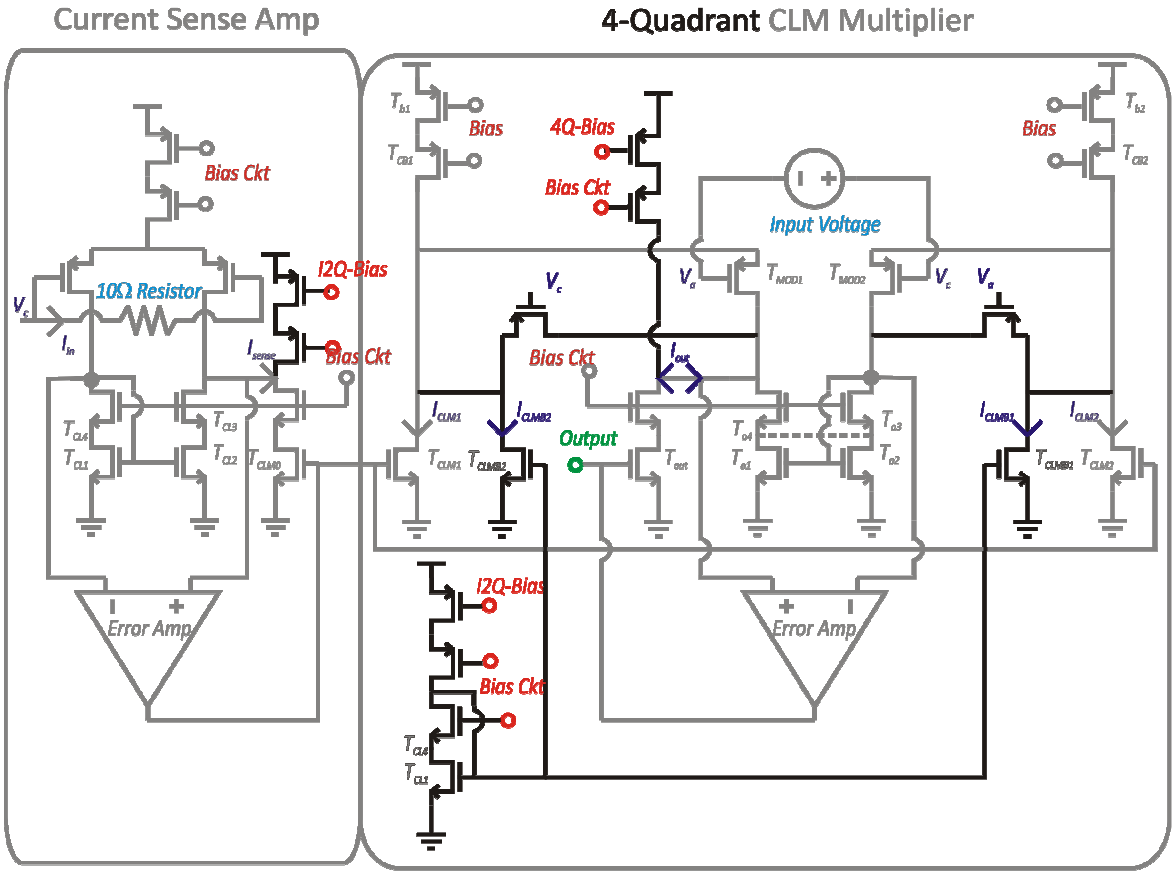

Figure 26: ***The 4-Q I-V multiplier*** *– Four-quadrant multiplication requires additional current sources in both T_{CLM0} and T_{out} branches, and two additional CLM branches to balance-out the modulation of the new bias current sourced into T_{CLM0}.*

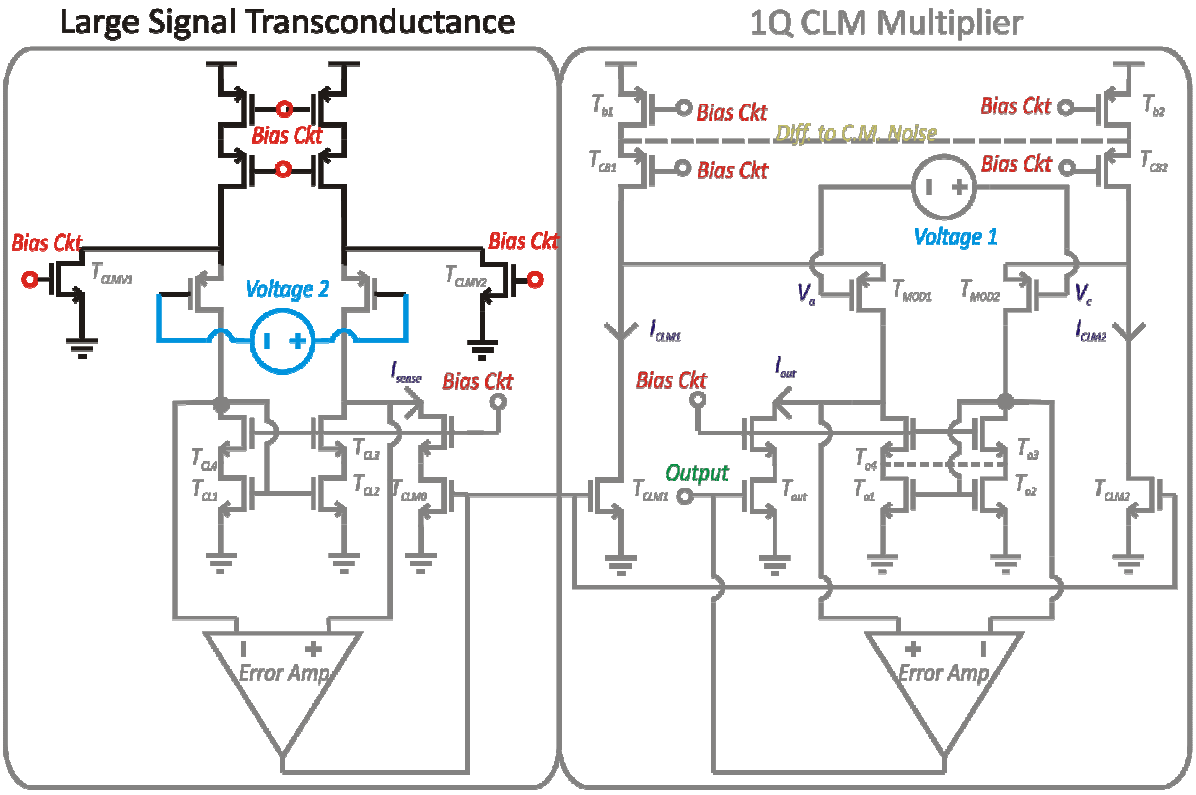

Figure 27: ***The Voltage-Voltage CLM multiplier*** *– The current sense amplifier is converted into a large-signal voltage-sense block by replacing the differential input stage with a folded-cascode channel-length modulation stage.*

The output current is thus maintained as the multiplied product.

k. Conversion to large-signal voltage input using CLM: The multiplier can be converted to a large-signal, voltage-voltage multiplier, by changing the current sense amplifier to a differential current-mirror setup similar to $T_{CLM1\text{-}2}$ as shown in Figure 27. Channel length modulation could then provide the linear transformation from input voltage to a small signal current mirrored into the multiplier. This brings up the notion of generalizing the multiplier to a multi-input cascaded system, where subsequent stages would each add one input to the multiplication. The advantage of this system would be the ease of maintaining signal swing and bias for a multi-input multiplication, with disadvantages of low current gain (1%) and thus added noise at each stage. 4-quadrant multiplication can also be extended in a similar manner, with careful cancellation of bias current at each stage.

i. Advantages and Pitfalls: The CLM multiplier performs current-voltage multiplication at

low power levels, and can accept a large dynamic range of input current as well as an input voltage swing close to both power rails. The tradeoff between noise immunity and operating power can be tuned at runtime by simply adjusting the bias currents in the current sense and CLM branches. However, the main drawback of this design is the low channel modulation coefficient, which is only about 1% even for the more 'non-ideal' sub-micron technology nodes such as 0.13µm. The CLM coefficient also becomes non-linear, and linearizing the amplifier requires careful design. Elimination of common-mode and proportional terms are the major layout and bias design challenges that this circuit presents. In this work, the CLM branches were biased with 100nA current while the current sense amplifier was biased with 200nA.

4.3 Nano-amp differentiator

a. Operation: The output of the CLM multiplier is: 1> a single-ended current-mirror output and 2> generates a current output between 1nA and 10nA full-scale. Considering that this full-scale current is only reached for the maximum power the circuit can measure, the current changes that the differentiator needs to respond to for MPP tracking are one or two

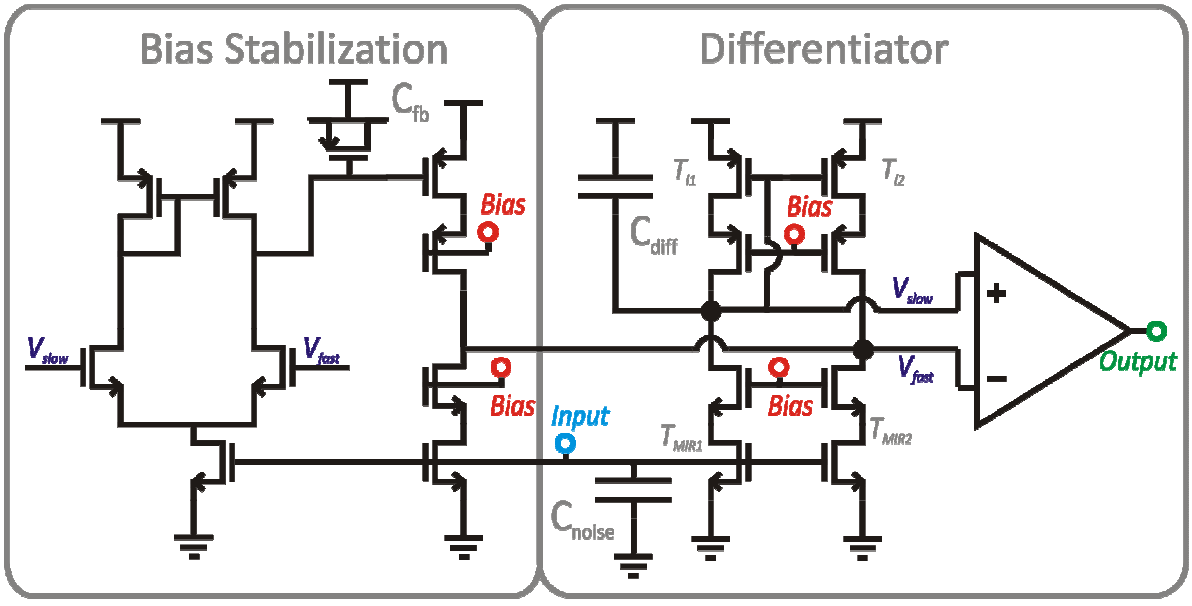

Figure 28: ***The differentiator*** *– The current mode differentiator uses a capacitor and current mirror load to introduce a time-delayed current-mismatch at a high impedance node. The comparator acts as both, a gain stage and a buffer. Bias stabilization is required to counter mismatch and variation in input quiescent point.*

magnitudes lower in value than full scale (on the order of nA or tenths of nA). The differentiator in this work is optimized to respond to 200pA of current change at 10kHz in presence of noise. A reasonable choice of differentiator such as the type described in [51] failed to satisfy sensitivity requirements in this application due to limits on the output impedance of the FETs in IBM13. Thus the custom current differentiator presented in Figure 28 was designed to meet the given constraints.

The custom differentiator matched to the constraints of the CLM operation consists of a dual cascode current-mirror driving a cascode current-mirror load. $T_{MIR1,2}$ source the input current to both branches, filtered by C_{noise} to limit high frequency switching events due to noise injected in previous stages.

The capacitor C_{diff} shunts any quick changes in current in the V_{slow} branch and thus dampens voltage changes at the V_{slow} node as long as its conductance dominates the transconductance of diode-connected T_{L1}, i.e. $s \cdot C_{diff} >> g_{m,L1}$. In other words, the charge/discharge of C_{diff} makes the current in the load current-mirror $T_{L1,2}$ insensitive to the input current. Thus the load current can be expressed as a fraction of the input current as:

$$i_{L2} = i_{L1} = \frac{g_m \cdot \partial i_{in}}{(g_m + s \cdot C_{diff})} \qquad \ldots(4.3.1)$$

$$\therefore i_{L2} = i_{L1} \approx \frac{g_m \cdot \partial i_{in}}{s \cdot C_{diff}} \qquad \ldots(4.3.2)$$

which is small if $s \cdot C_{diff} >> g_{m,L1}$. The lag of current through T_{L2} compared to T_{MIR2} causes a current imbalance at the previously balanced V_{fast} node in response to input current change, causing a voltage change across the output impedance at the V_{fast} node.

$$\therefore v_{fast} = (\partial i_{in} - \partial i_{L2}) \cdot r_{out} = \frac{\partial i_{in} \cdot (s \cdot C_{diff} - g_m) \cdot r_{out}}{s \cdot C_{diff}} \qquad \ldots(4.3.3)$$

$$\therefore v_{fast} \approx \partial i_{in} \cdot r_{out} \qquad \ldots(4.3.4)$$

for signals of frequency where the capacitive reactance is much smaller than the transconductance (most of the input current flows into the capacitor), $s \cdot C_{diff} >> g_m$.

At the V_{slow} node, the voltage is decided simply by the load impedance:

$$v_{slow} = \frac{\partial i_{in}}{\left(g_m + s \cdot C_{diff}\right)} \quad \ldots(4.3.5)$$

$$\therefore v_{slow} \approx \partial i_{in} / s \cdot C_{diff} \quad \ldots(4.3.6)$$

again for signals where reactance shunts input current. The new difference in voltage across V_{fast}-V_{slow} causes the output comparator to indicate the direction of current change by switching V_{diff} 'high' or 'low'.

$$v_{diff} = \text{sgn}(v_{slow} - v_{fast}) \quad \ldots(4.3.7)$$

$$\therefore v_{diff} \approx \text{sgn}\left(\partial i_{in} / s \cdot C_{diff} - \partial i_{in} \cdot r_{out}\right) \quad \ldots(4.3.8)$$

$$\therefore v_{diff} \approx \text{sgn}\left(-\partial i_{in} \cdot r_{out}\right) \quad \ldots(4.3.9)$$

again for signal frequencies where $s \cdot C_{diff} >> g_m$. Thus the differentiator action is achieved when the differentiating capacitor is able to dominate the transconductance of the load transistor. Higher (noise) frequencies will also see a high differentiator gain as mentioned before. To achieve a balance between high gain and noise immunity, the value of C_{diff} was fixed at 1pF and the transconductance of the load transistors $g_{mL1,2}$ was adjusted through simulation.

Although equation 4.3.9 looks simply like a gain equation, the important difference from a simple amplifier derivation is that this gain occurs only for a *change* in the input current, for $s \cdot C_{diff} >> g_m$. 'High' frequency changes see the differential transresistance gain r_{out} as derived above, while the low frequency signals see a differential gain of ($1/g_{m,L1}$) (obtained through similar derivation). Since for all transistors in circuit, $g_m \cdot r_{out} > 1$,

$$\begin{aligned} \therefore r_{out} &= \left(g_{m,CL2} \cdot r_{out,CL2} \cdot r_{out,L2} \,||\, g_{m,CM2} \cdot r_{out,CM2} \cdot r_{out,MIR2}\right) \\ &>> \left(1 / g_{m,L1}\right) \end{aligned} \quad \ldots(4.3.10)$$

i.e. we have the differentiation 'gain' dominate the dc gain. Further, the bias stabilization amplifier reduces the low frequency gain by a factor equal to its gain at low frequencies,

further increasing the low-frequency rejection ratio.

For lower frequencies, differentiator gain drops and phase changes, causing lesser difference in the slow and fast node voltages. The load and source currents are balanced, and the bias-stabilization circuit equalizes the two nodes. In this case, the output of the comparator is decided solely by offsets in the system, and doesn't change with time.

b. Challenges due to typical on-chip values: From equation 4.3.5, C_{diff} introduces a pole-zero pair in the frequency response of the differentiator, with a zero at dc and a balancing pole decided by the transconductance of the load. The high frequency gain of this circuit is r_{out}, and is reached at the pole decided by the ratio of C_{diff} to g_m. For realistic on-chip capacitance and transconductance values (e.g. 1pF and 1μS), the pole frequency is greater than 1MHz. The differentiator in this circuit processes signals at close to 10kHz, which is in the filtered band. This bandwidth limitation causes two problems: 1> r_{out} needs to be higher to achieve differentiation at 10kHz and 2> the circuit becomes sensitive to high frequency noise because the higher frequency signals (noise) experience a higher gain than the signal frequencies. To mitigate the effect of noise, the input current is filtered by C_{noise} and the comparator frequency response is limited, however some high frequency artifacts are still present in the measured switching waveform from the chip (Figure 33).

c. Bias Stabilization: The high impedance output of the circuit is stabilized by the bias stabilization circuit which makes the differentiator insensitive to sub-kHz changes in current, and equalizes the output voltage at the V_{slow} and V_{fast} nodes to compensate for any Process-Voltage-Temperature mismatches. Equalizing the $V_{slow,fast}$ nodes is essential to stabilize this current-mode differentiator. The bandwidth of this amplifier again needs to be limited to improve the response of the differentiator to kHz frequency signals. The amplifier's frequency response is set by the capacitance of the PMOS capacitor and the g_m of the input differential pair. Typical on-chip values for these two quantities can put 10kHz well within the frequency band of the amplifier, making the differentiator unable to work at MPP tracker frequencies. The g_m of the input pair is thus severely limited by setting their bias current to a few nano-amps, thus forcing the bandwidth down to less than 10kHz. Keeping the quiescent current in the amplifier at a low value also serves to increase the impedance

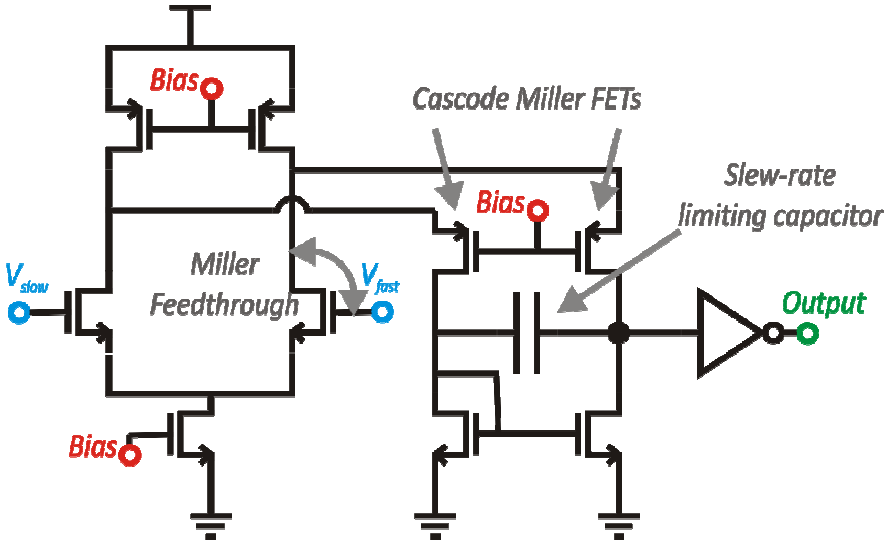

Figure 29: ***Output comparator for the differentiator*** *– Cascode FETs reduce the miller effect on the input differential pair and slew rate is limited by an output capacitor to reduce charge feedthrough to the input from switching events.*

of the compensation output transistors and hence reduce loading on the high-impedance V_{fast} node.

d. Charge Feedthrough: A subtle charge feed-through problem arises in this circuit topology that can cause spurious switching events and oscillation. When the switching events occur in the comparator, the gate-drain miller capacitor across the '-' input differential FET of the comparator feeds some charge back to the high impedance node V_{fast}, causing high frequency oscillations during a switching event. This problem is mitigated in two steps:

1> The slew rate of the first stage of the comparator is limited to reduce the feed-through current and

2> Cascode transistors are used in the input stage of the comparator to reduce the miller coupling from the input differential pair to the switching nodes.

The folded cascode, slew-rate-limited comparator is shown in Figure 29.

e. Advantages and Pitfalls: The differentiator described above has high sensitivity, with a transresistance gain of over 10^8. Current mode operation gives the circuit more immunity to noise in the circuit, and permits it to self bias to accept a large dynamic range of input currents without any external adjustments which works well in a PV harvesting system

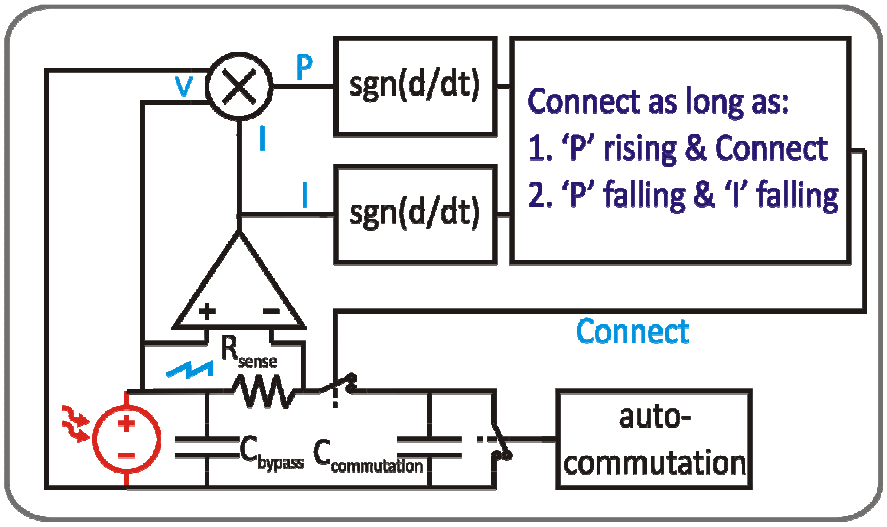

Figure 30: ***The TDAR MPP tracker*** *– with decision logic revealed.*

where charging current can vary widely. However, the quality of high gain also causes instability in the operation of the differentiator, requiring a bias-stabilization feedback circuit and high noise suppression at the previous stages. Any noise can cause glitches while switching. The differentiator was observed to respond to 200pA of current change at 10kHz in simulation.

4.4 Connect/Disconnect decision making

The multiplier and differentiator fit into the system of Figure 30 to form two analog computation paths that are then correlated for the connect/disconnect control decision. Figure 30 also illustrates the decision logic. The first channel is the power path, wherein the multiplier computes the power of the system and the differentiator following it computes the trend (rising or falling). The second path can be either a current or voltage path. Since the current sense amplifier transforms the PV current to a mirrored output similar to that of the multiplier, this output is re-used as an input to another differentiator to form the current differential path as shown in Figure 30. The outputs of both these paths are digital, and the rules used to compute the connect/disconnect decision are explained in Table 3. The conceptual rules are reduced to fewer logical rules shown in Figure 30, which are then implemented by asynchronous logic consisting of 2,3 input NAND and NOR gates.

Results from the first prototype are detailed in the next Chapter.

5

Results and Conclusions

5.1 Prototype TDAR systems

The TDAR system developed in Chapter 3 was implemented in hardware in two forms:

1> A discrete implementation of a single TDAR cell: A single PV-MPP tracking string-reconfiguration block was implemented using off-the-shelf integrated circuits (ICs). This discrete TDAR block was designed from the system-level schematics in Figure 30. The multiplier and differentiators were designed around the Analog Devices AD632 multiplier and the LM324 National Semiconductor opamp IC. 74HCxx logic ICs replaced all the control logic gates in Figure 30. The TDAR switches were implemented with the ADG451 Analog Devices low-resistance switch IC. Both, the TDAR concept and its implementation using the control loop and switching circuits developed in Chapters 3 were validated with this discrete system. Test results validating TDAR and the control loop are presented in section 5.4. Although the discrete system served well for basic validation, the system itself was not designed to

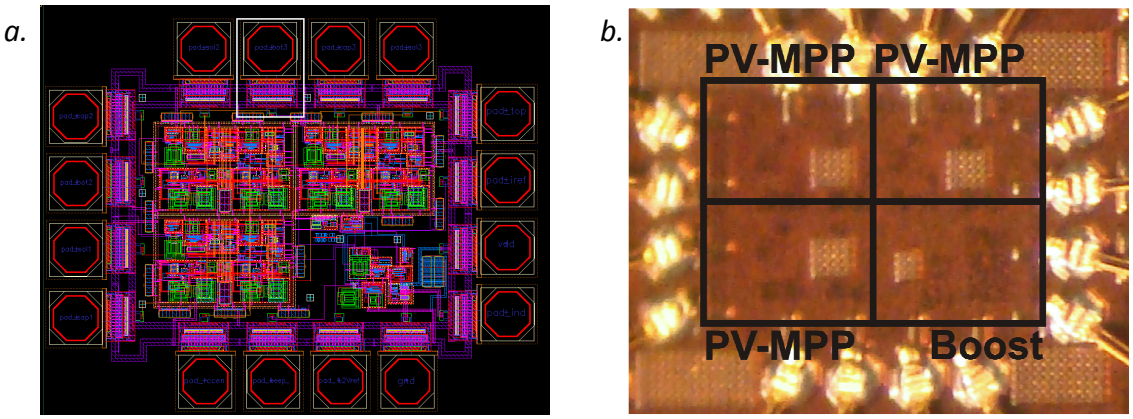

*Figure 31: **TDAR Microchip** - a. Layout screenshot and b. Photograph of bonded chip. The chip is ~700µmX600µm including bond pads.*

run from the harvested solar power. Due to the discrete nature of this implementation, the power consumption of all the ICs together is on the order of 150mW while the PV cells used for testing deliver only 1mW-4mW. To demonstrate the feasibility of the TDAR system as a self-sufficient system that runs off harvested PV energy and yet delivers most of the energy harvested to the output, the micro-chip was developed and tested.

2> The fabricated TDAR microchip described in chapters 3 and 4 is shown in Figure 31: This prototype microchip was fabricated in the IBM 0.13µm standard CMOS process. IBM 0.13µm is a 1.8V V_{DD} process, while the chip needs to charge a 3.7V Li-poly battery. Thus thick-oxide FETs available in the process were used for the entire design. The chip-photograph in Figure 31b shows the four major blocks in the chip: three identical PV controller blocks to implement a reconfigurable string of 3 PV cells, and one boost converter block (bottom, right) to up-convert PV voltage to a level sufficient to charge a Li-ion battery. Off-chip components required for the chip are a power inductor and a capacitor bank to filter the PV cells and output currents. The power inductor is a CoilCraft EPL2010-103MLB, and the capacitor bank is in a 0805 SMD package. The chip, power inductor and capacitor bank with a PCB to support them cumulatively weigh an estimated 0.4 grams. This first prototype TDAR IC also requires some additional components to support operation, such as current and voltage references, which can be integrated in future versions without significant performance/area penalties.

The bare-die IC was bonded to a test PCB, encapsulated in epoxy and tested. The finished PCB is shown in Figure 32. The connector on the bottom-edge interfaces to three solar cells, while the connector on the right-edge provides bias current and voltage, control signals, auxiliary power for the potentiometers and the battery output.

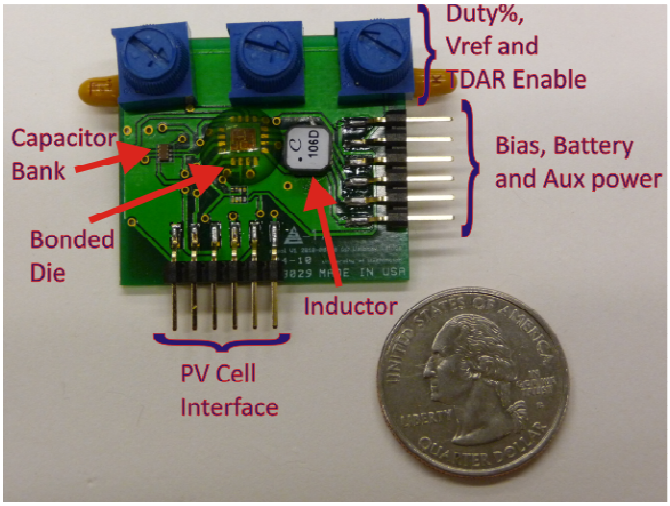

Figure 32: ***The microchip test PCB*** *- A capacitor bank with 4 1μF capacitors and a 1mH inductor are the only required external passives. Additional potentiometers give manual duty cycle control, V_{ref} control and enable/disable for TDAR switching. Connectors interface to the PV cells, battery, current bias, and auxiliary power supply for the potentiometers. A US quarter dollar coin is shown for size-reference.*

The central portion of the PCB shows the bonded die encased in epoxy, with three potentiometers on the top edge.

The potentiometers from left to right are meant for:

1> Manual control of the duty cycle of the boost converter: The boost clocking circuit runs as part of the overall control loop if the potentiometer voltage is VDD, however when voltage drops one threshold voltage, to V_{DD}-V_{TP}, the duty cycle is forced to be a linear function of input voltage.

2> Control of the reference voltage for the TDAR IC: V_{ref} is nominally 1.2V, but can be changed with this potentiometer. During testing, V_{ref} was maintained at 1.2V.

3> An ON/OFF control for TDAR duty-cycling: This potentiometer simply acts to replace a switch to enable/disable duty cycling. When duty-cycling is disabled, all PV cells are continuously connected in series.

The PCB is a 2-layer board that measures 1.6”X1.2”.

The connection between the energy harvesting chain and the on-chip boost converter is

external, through pins brought out on the connector on the right board edge. Opening the power path thus allows the input and output parts to be tested separately. Chip validation was separated into boost converter testing (5.3a), and TDAR testing (5.4).

5.2 TDAR Representative Results

From a testing perspective, TDAR is demonstrated when partial shading of a PV cell in the string causes the string output waveform to break from a steady voltage into a variable pulse-width wave. The pulse waveform is caused by the TDAR duty cycling of the shaded cell, and rides on top of the DC offset from the cells which are not shaded. This first such test waveform from the TDAR microchip is shown in Figure 33. When the topmost cell in the input PV string was shaded progressively, the duty-cycle in the waveform decreased as a consequence. Several characteristics of the implemented TDAR loop are evident in the figure. The pulse edges are at non-uniform intervals due to the asynchronous nature of the control loop. The rising slope of each pulse is shaped by the charging of the commutation

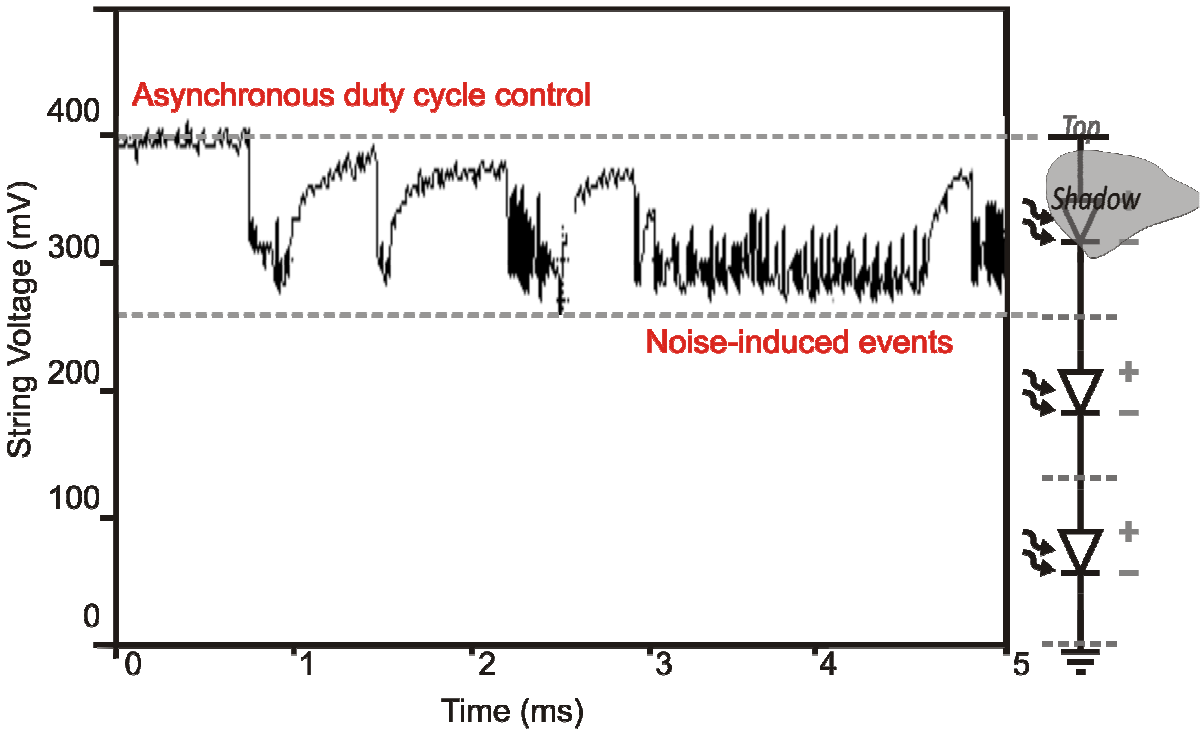

Figure 33: ***First Test Waveform*** *– An oscilloscope capture that depicts the output of the PV string when one cell is being switched by TDAR. The DC base level of the waveform equals the voltage of the other two PV cells in the string, and the average duty cycle depicts what ratio of the cell is shaded. The system is operating at a low V_{DD} of 1V, causing harvested PV voltage to drop accordingly to 0.6V instead of 1.25V.*

capacitor from the PV cell, and finally noise induced partial switching events are visible in the waveform, as short spikes in the 'off' time of a cell. With this basic demonstration of TDAR, power efficiency and performance measurements were performed next.

5.3 Power chain validation and efficiency

The power chain consists of the three TDAR cells strung in series, a synchronous boost converter that steps up the TDAR voltage to the power rails, and the components that draw power from the rails power namely the chip itself and the load battery. Power loss occurs in three ways:

1> losses in the boost converter during voltage conversion

2> quiescent dissipation of the microchip circuits

3> losses during TDAR PV power management

The efficiency of the boost converter and the quiescent dissipation thus decide the maximum efficiency of this microchip, when illumination is uniform and TDAR is not required. Boost converter efficiency is examined first, and the overall quiescent consumption of the microchip is measured next. Since the chip power rails are common with the output of the boost converter, the boost converter efficiency is ultimately linked to measured quiescent consumption of the chip and vice versa.

a. Boost Converter: The boost converter is designed to charge a 3.2V-3.7V battery with a 0.9V-1.5V input. The power transfer occurs at approximately 1MHz, governed by an internal oscillator. Power losses by the circuits in the chip and during transfer in the lumped and parasitic passive elements limit the power delivered to the load to a fraction of the input power. The design goal of this system was achieving a system efficiency for power delivery of 75%. The measured efficiency of the boost converter in this chip with a fixed 3.9V output voltage and output current of 0.5mA is plotted against input voltage in Figure 34.

Thus the boost converter achieves over 78% efficiency for the typical 0.9V-1.5V range of inputs expected from the PV array.

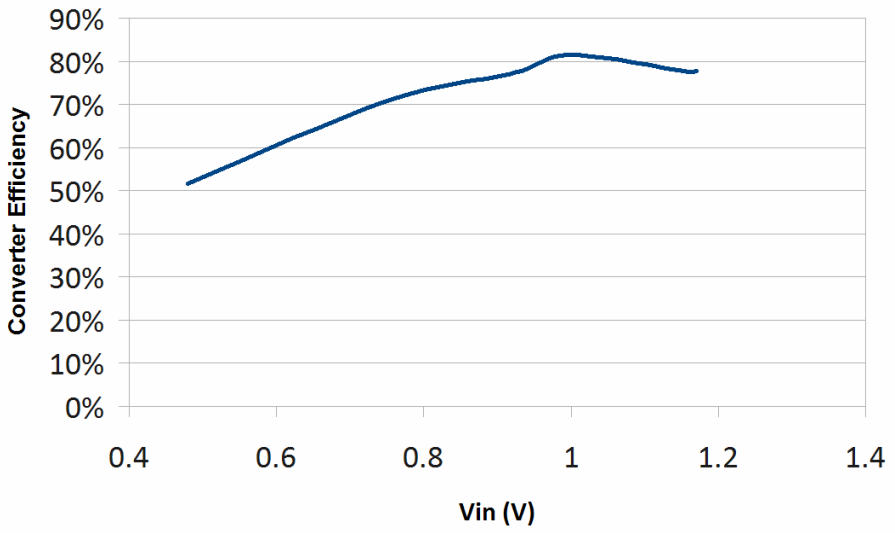

Figure 34: ***Boost Converter Efficiency –*** *The boost converter is more than 78% efficient for the range of voltages expected from the PV string at 0.5mA output current.*

b. Quiescent Power Consumption:

Since the power rails are common between the microchip and the load, quiescent consumption was measured as the power drawn from the PV cells when output current is zero. When output current is zero, switching losses in the passive components in the power

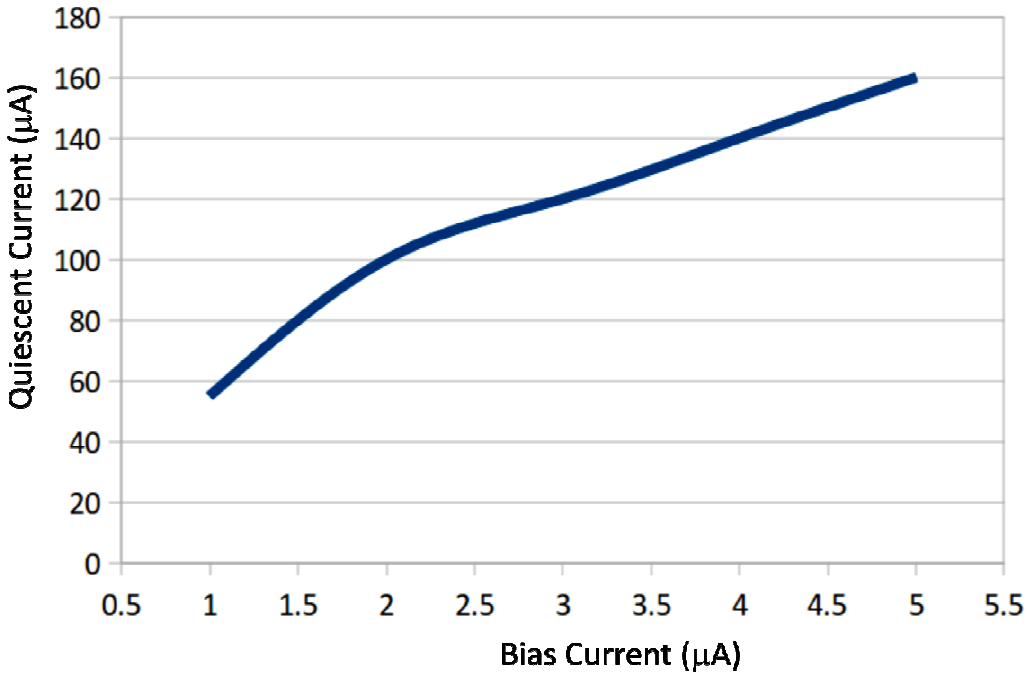

Figure 35: ***Quiescent Consumption v/s bias current –****The current drawn from PV cells just to run the microchip is plotted against bias current to the microchip. The chip power*

path are minimal and the power transferred by the boost converter from the input goes wholly in supplying the quiescent power of the chip. Although this figure overestimates quiescent losses by including some losses in the boost converter, it is a useful practical number that showing the minimum illumination required in the PV cells for the chip to start providing energy to the load. Quiescent consumption of the chip varies with bias current, and is thus plotted against bias current in Figure 35.

From Figure 35, the TDAR microchip is demonstrated as among the first reports of sophisticated photovoltaic array management at the micro-scale, with a rated power consumption of only 165µW at 3V, and 220µW at 4V while supplying up to 4mW (1mA at 4V) to the output load.

5.4 TDAR validation and efficiency

Although the power chain and boost converter achieve high efficiency, the efficiency of the system under partial shading is determined by the efficacy of power management using TDAR. Efficiency of power management again has two components, efficacy of TDAR itself for power-balancing cells and how effectively the designed control system implements TDAR. TDAR efficacy is addressed first and the control system performance is presented next.

a. TDAR Efficacy:

To measure the TDAR efficacy, the TDAR microchip was setup with a string of three PV cells with the top cell partially shaded. The output waveform under shading was similar to Figure 33. As a representative result, current output to the load was measured at 3V output voltage. Next, TDAR switching was forced off by turning the control potentiometer on the test PCB. The boost converter was still operational, transferring power from an array which was not bypassed. The current output dropped 78%, indicating that the active bypass provided by the TDAR system in addition to recovered power from the PV cell contributed to 78% efficiency gains over traditional, fixed arrays under shading. The same set of PV cells were then connected to the discrete system for detailed efficiency measurements. The discrete system permits manual intervention at more levels than the microchip, and results

obtained at different levels are plotted in Figure 36.

Improvements over PV string: TDAR demonstrates two improvements in harvesting efficiency afforded by a duty-cycled string over a fixed PV string. The first is alleviation of current blocking by partially shaded cells and the second is utilization of the energy generated by the active area of the partially shaded cells. Switching losses during TDAR power tracking can reduce overall system efficiency. Figure 36 permits a detailed analysis of system performance:

1> No TDAR: The orange curve in Figure 36 represents power output from the 3-cell string with TDAR disabled. From the trend of the curve, it is evident that power output from the entire string drops when just the top cell is shaded. The power generated from the unshaded cells is hence lost, and the cell output voltage drops quickly with shading.

2> Shaded cell is bypassed: The yellow curve represents the power generated by the unshaded cells. If the top cell were bypassed permanently, the power output of the TDAR string would be indicated by the yellow curve.

3> External TDAR control: Since the discrete TDAR system allows intervention, an external duty cycle controlled pulse waveform was introduced to control the connection/bypass of the shaded cell into/out of the string. For each level of shading, the duty cycle was manually adjusted until maximum power output was approximately obtained. The power output of the string with manual TDAR indicates efficacy of the TDAR switching system with an 'ideal' control loop and is shown by the green curve. The power output of the string drops progressively with shading, but instead of the entire string's power being compromised, now the only power loss is in the shaded cell. Thus with progressive shading, the power output of the string asymptotically approaches the power of the unshaded cells. When shading of the top cell is 100%, the output of the string is equal to the power of the unshaded cells. In addition, when shading is partial, the shaded cell contributes power to the output, raising the string output above the two-cell yellow curve.

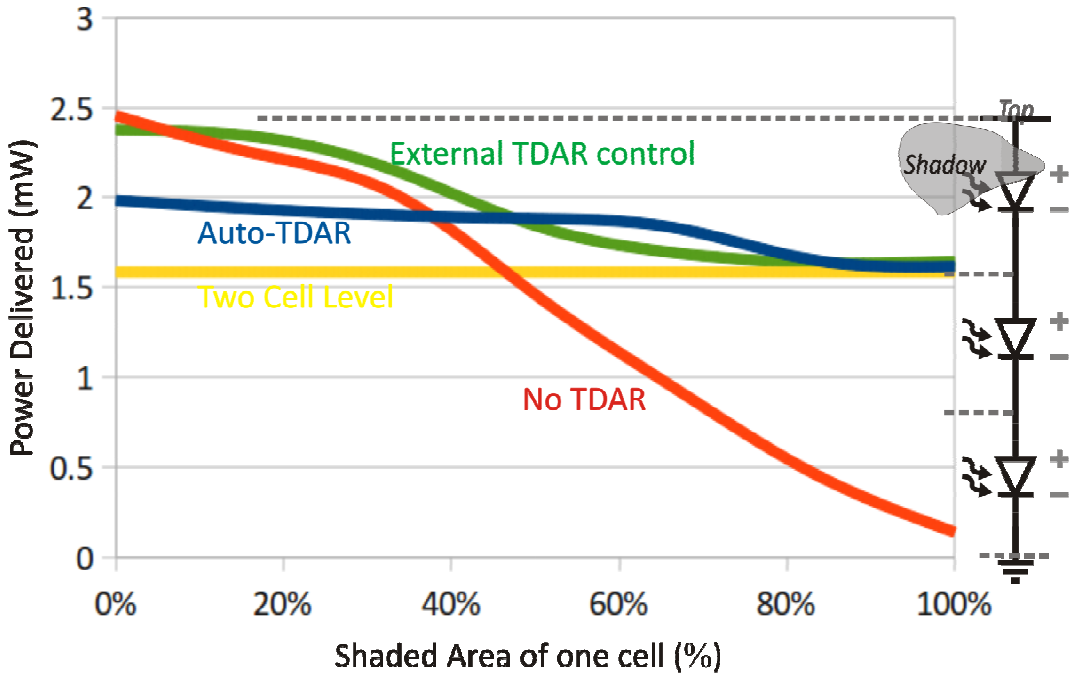

Figure 36: ***TDAR system performance*** *– Manually controlled TDAR optimized for every level of shading drops system output power smoothly from three cells to two cell level, while a static string loses power with single-cell shading much quickly. The discrete system developed in this work implements TDAR.*

4> Performance of the TDAR control loop: The power output under automatic TDAR is shown by the blue curve. If the control loop were ideal, this curve would overlap the green curve. Non-idealities are primarily observed at low shading levels, wherein the duty cycle of the TDAR switched cell doesn't reach 100%. When shading exceeds 80%, the system closesly mirrors the manual TDAR control curve and drops power linearly to the unshaded cell level. Overall, the automatic TDAR system gives a power gain of over 80% at 90% shading. For shading from 40%-60%, the TDAR system also provides additional power from the duty-cycled cell to improve string power output. The externally controlled TDAR system proves more efficient all the way down to 20% shading.

b. TDAR improvements over single-PV cell systems: The previous section deals with efficiency gains of the TDAR system under partial shading, over systems that use fixed strings. Another solution adopted to counter partial shading in portable applications is to use just a single PV cell to harvest energy, preventing the problem of current mismatch in

series cells. However, a single cell harvester can be inefficient compared to a TDAR string. The improvement in efficiency of a TDAR string over a single cell system comes mainly from the efficiency gain in the boost converter stage. Boost converters that employ inductors typically lose efficiency for voltages less than 1V. Using the boost converter implemented in this work for example, the efficiency of the converter from Figure 34 at the two-cell voltage of 0.9V is more than 25% higher than the single cell voltage of 0.45V. Under partial shading, this efficiency improvement in TDAR is even higher for the same given shaded area and the same load voltage/current. The next section investigates the performance of the two TDAR systems compared with ideal performance, and suggests methods to improve the ideality of the control loop.

5.5 A Perspective on Performance

a. TDAR system performance: The efficiency gains provided by a TDAR system depend on how accurately the control system implements it. In Figure 36, External TDAR control provides the ideal case scenario with the best power benefit. To achieve the power trend

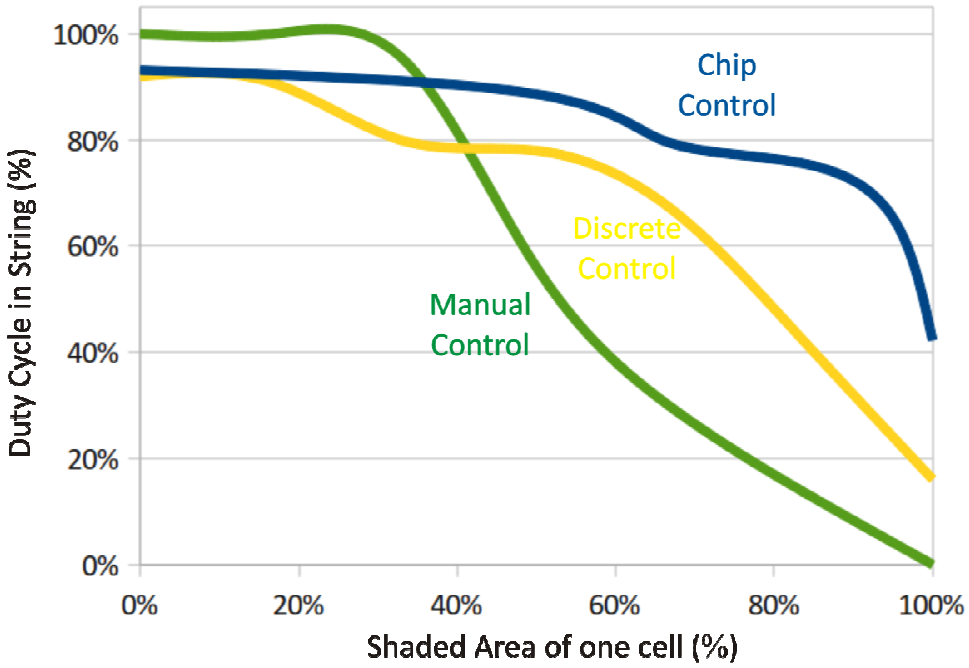

Figure 37: ***Comparison of TDAR duty cycling*** *– Manually controlled TDAR optimized for every level of shading, v/s discrete system v/s integrated system showing challenges in control loop stability over the entire duty cycle.*

presented in Figure 36, the duty cycle of the external pulse waveform was varied as indicated by the green curve in Figure 37. Some initial non-linearity in the duty cycle eventually gives way to an almost linear relationship between the shaded area of a cell and the TDAR duty cycle. The flatness of the curve between 0%-20% indicates that the PV cell was operated above its MPP voltage, leading to no drop in output current with shading of the cell.

The discrete MPP control loop achieves the duty cycle trend indicated by the yellow curve. As can be seen from the curve, the duty cycle never reaches 100%, indicating that the asynchronous control loop oscillates at low shading levels. Though non-linear, the rest of the curve indicactes a monotonically decreasing duty cycle with increase in shading, again stopping short of a 0% duty cycle.

The microchip that implements TDAR is able to vary duty cycle in a shorter window, between 40% and 80% as indicated by the blue curve. Major changes in the duty cycle occur only after 60% shading, implying that the microchip needs a larger variation in PV power to detect deviation from the MPP. Thus, improving the gain of the microchip while compensating for self-oscillation and instability can broaden the range of duty cycles the control loop achieves, and bring the automatic control closer to the ideal duty cycle trend.

d. Challenges with micro-power TDAR: Although the discrete system presented a tunable test-bed to validate and improve the asynchronous TDAR feedback loop, designing the system into the TDAR microchip introduces further challenges. Guaranteeing stability and noise immunity of the sense circuits is just such a challenge when operating at low power levels. The already low bias current of the multiplier circuit couple with low channel length modulation coefficients imply that a higher input swing, or higher change in PV power is required before the multiplier is able to generate sufficient current swing to drive the differentiator. Evident from Figure 38, the microchip permits a larger change in output power from the duty-cycled PV cell compared to the discrete system.

Between 60%-100% shading, TDAR switching of the microchip was demonstrated. Since the duty cycle was not as low as the external TDAR or discrete control system, some negative voltage developed across the switched cell periodically, reducing harvesting efficiency.

Switching losses in the microchip are expected to be lower than the discrete system, due to lower commutation capacitances. Improving the duty cycle range of the microchip TDAR control loops thus has the potential of even higher efficiency gains as compared to the discrete TDAR system.

The demonstration of TDAR with low-power circuits opens the door to achieving a high-efficiency micro-power array management system by stretching the range of duty cycles to occupy the entire 100%-0% range under partial shading. Options to the TDAR control loop such as a synchronous design with a variable pulse width clock, or a fractional-voltage controller can potentially ensure a better range for the duty cycle compared to an asynchronous design.

In summary, TDAR was demonstrated at the discrete and microchip levels. Discrete implementations achieved upto 80% gain in efficiency under partial shading compared to fixed strings, and over 25% compared to single-cell systems. Microchip TDAR design suffered inaccuracies in duty-cycle tracking, but nevertheless demonstrated the feasibility of achieving three TDAR tracking systems with a total quiescent current of only 150μA. Efficient low power analog MPP tracking systems were developed with efficient multiplier and differentiator circuits, opening the door to sophisticated power management at the micro-scale. Future directions of research that naturally spawn from this work are discussed next.

5.6 Future Work

The demonstration of a basic modular, low power, high efficiency PV harvesting system opens the discussion on exploring the limits of scaling PV harvesting to low power, low form-factor systems. Various parts of the PV harvesting system can be individually scaled and optimized:

a. Current and Voltage scaling: Current scaling in the TDAR system is easily achieved by changing the value of the sense resistor and increasing the capacity of the power switches. Current can also be scaled by placing PV cells in parallel, without significant change to the TDAR control loops. For voltage scaling, the modular nature of the TDAR architecture enables the addition of more series TDAR cells to the system.

b. Multiplier circuit: The low-power multiplier developed for PV power measurement is applicable in general to many analog signal processing subsystems. The TDAR system is well within the gain-bandwidth performance limits of the multiplier, and higher speed applications that require a high input voltage swing can be investigated for applications of the multiplier.

Two quadrant and four quadrant multiplication is also discussed as extensions to the basic single quadrant multiplier architecture. Improvements to the design of the multiplier can yield better noise/stability performance for systems that choose to integrate analog signal processing blocks.

c. Alternative TDAR control strategies: TDAR performance depends on how accurately the control system can track the ideal duty cycle through the entire range of cell shading. This work implements a modified ripple correlation control loop. Another possibility that can be explored is using a simpler fractional-voltage [52] MPP tracker with a variable pulse-width clock scheme for TDAR switching.

An important third option that can be explored for the control strategy is to maximize battery charging using load current optimization [35]. Since load-current is a global variable, each local TDAR loops would need modification to follow the common goal of optimizing overall current. However, this additional complexity has the potential advantage of finding an operating point for the PV cells that makes the entire energy harvesting chain efficient, instead of just the PV cells themselves. A simple fractional-voltage MPP tracker can be modified by making the voltage fraction variable, controlled by the global load-current maximization control loop.

d. Light weight solar cells: Integration of low-weight, flexible-substrate organic PV cells and organic FET switches is a research goal with many possibilities for hybrid organic-silicon circuits, leveraging performance benefits of both material types to provide new tradeoffs for energy harvesting microsystems. TDAR systems stand to benefit from switch integration with the PV cells, permitting custom-tailored array configurations to each microsystem.

5.7 Conclusion

Time Domain Array Reconfiguration is a new technique added to the PV system designers toolkit, to improve photovoltaic power management with a minimal complexity overhead. Time domain array reconfiguration has a significant research potential for development in the context of both portable and large-scale energy harvesting systems.

Low power multipliers and differentiators developed for this work add to the microsystem circuit repository that achieves low power analog signal processing. The CLM multiplier presents the first multiplier circuit with a saturation-mode drain terminal as input. This sub-family of one, two and four quadrant analog multipliers begs investigation for usability in both low and high-speed applications.

In conclusion, this work demonstrates sophisticated photovoltaic power management in the microwatt to milliwatt power regime, enabling integration of a smart photovoltaic energy harvesting source with portable electronic microsystems.

Acknowledgments and Bibliography

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The following authors contributed to my knowledge on the subject and provided the grounding on which this body of research is based.

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VITA

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