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Characterization of Nafion-based Resistive Switching Devices

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Abstract:

Characterization of Nafion-based Resistive Switching Devices

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The development of computers in the modern era has escalated the race towards the development of powerful and efficient memory devices. By using advanced miniaturization techniques and new materials, we have been able to dramatically reduce the size of the memory devices while increasing the storage capacity and computing performance. However, we are reaching a point of slower growth in the computing performance of MOSFET-based nonvolatile memory devices. It becomes increasingly difficult to further decrease the size of memory devices. Hence, the next generation memory technology must have the following features to meet the high computing performance in the era of artificial intelligence: low-power consumption, fast switching, non-volatile, high-density fabrication. Resistive Random-Access Memory Devices (ReRAM) meets all those requirements; hence, is considered as one of the promising candidates for the next generation memory technologies.

In this research, a ReRAM device with Nafion as a switching layer was fabricated. To characterize the resistive switching performance, Nafion was annealed at three

different temperatures: 30°C, 60°C, and 90°C. In order to study the effect of different electrode, we used two different bottom electrodes (Au and Cu) and Al as a top electrode. The devices with Cu as a bottom electrode exhibited good resistive switching properties while the device with Au as a bottom electrode showed little or negligible switching performance. We found that the performance of switching was best when Nafion was annealed at 60°C. However, the experiment shows a wide variation of device performance even in the same substrate, indicating the importance of uniform film thickness and quality of Nafion.

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LIST OF SYMBOLS:

ReRAM	Resistive Random-Access Memory
IC	Integrated Circuit
FET	Field Effect Transistors
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Silicon Field Effect Transistors
SRAM	Synchronous Dynamic Random-Access Memory
DRAM	Dynamic Random-Access Memory
LRS	Low Resistance State
HRS	High Resistance State
MIM	Metal – Insulator- Metal
SL	Switching Layer
VD	Vapor Deposition
I_c	Compliance Current
V_{set}	Voltage at which set process occurs.
V_{reset}	Voltage at which reset process occurs.
IV curves	Current – Voltage Graphs
V_{read}	Reading Voltage
TE	Top Electrode
BE	Bottom Electrode
Cu	Copper
Al	Aluminum
Au	Gold

OxRAM	Oxygen vacancy based random access memory
CBRAM	Conductive bridge random access memory
IPA	Iso Propyl Alcohol
H_3PO_4	Phosphoric Acid
Al_2O_3	Aluminum Oxide
ZrO_2	Zirconium dioxide
ITO	Indium Tin Oxide
TiO_2	Titanium dioxide
MnO_2	Manganese dioxide
MgO	Magnesium oxide
kA°	kilo Angstrom
mA	mill Amperes
µm	micrometers

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CHAPTER 1: Introduction

1.1 History and evolution of memory devices

With the advent of digital computers, the need for reliable and efficient data storage started to feel more and more obvious. The need to store and compute data led us towards the invention and evolution of modern digital computers. Towards the end of second world war, several electromechanical computing devices were invented. The earliest batch of the computers were electro mechanical machines that used electrical switches to perform different calculations [1]. These machines were very soon replaced by computers that used vacuum tubes for data storage. This generation of the computers were capable to compute 22- bit calculations at a digital frequency of 5-10 Hz [6]. The vacuum tubes were then replaced by magnetic core memory [7]. These memory devices comprised of magnetic rings that stored data using the magnetic hysteresis [8]. Magnetic core memory took up large spaces and used large source of power and was an expensive technology [9]. The biggest challenge in the evolution of the modern computers was the lack of expandable memory devices.

The biggest jump in the computing power of the computers came after invention of the transistors. William Shockley created the first working transistor in 1947 [1]. Shockley then went on to produce Bipolar Junction Transistors (BJTs) in 1948 [1]. Eventually, Metal Oxide Semiconductor Field Effect Transistors (MOSFET) was constructed by Mohamed M. Atalla and Dawon Kahng in 1959 in the Bell lab [10]. This made it possible for the electronics to use these compact devices for computing and data storage. This invention resulted in the birth of Synchronous Dynamic Random-Access Memory (SRAM). John Schmidt made the first SRAM using MOSFETs in 1964 [1]. The first Dynamic Random-Access Memory (DRAM) was

commercialized by IBM in 1970 while Synchronous Dynamic Random-Access Memory (SRAM) was commercially produced by Samsung in 1992 [10]. During these two decades of period, we went from using bulky magnetic drums as memory devices to using compact transistor-enabled devices. Figure 1 shows the progress we have achieved in the field of non-volatile memory devices.

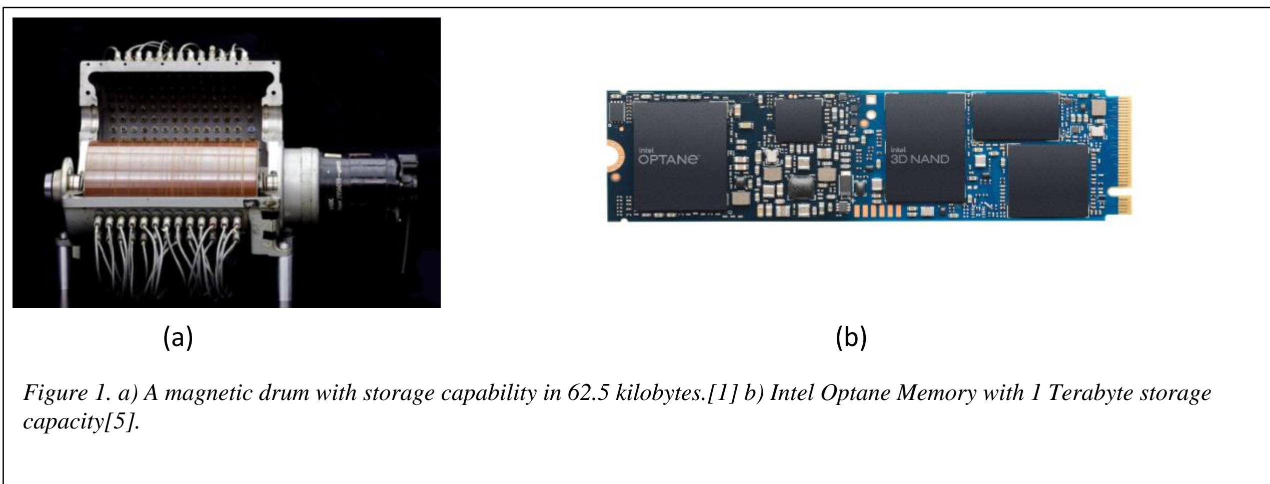


Figure 1. a) A magnetic drum with storage capability in 62.5 kilobytes.[1] b) Intel Optane Memory with 1 Terabyte storage capacity[5].

1.2 Current state of memory devices

The most prevalent memory technologies used in computing devices today are SRAM, and FLASH memory. These memory technologies have increased our computing and data storage capacity exponentially over the recent decades. FLASH memory devices are non – volatile memory devices and can store data for an extended period of time [11]. On the other hand, SRAM are volatile memory devices.

FLASH memory devices use a floating gate cell design to remember the state of the device making it a non-volatile memory device [11] . These devices are passive and do not require electricity to hold information. FLASH devices use modified transistors to store the data [11]. An

additional floating gate is sandwiched in between the control gate and the substrate [3]. This makes the production of the devices very difficult and costly. Due to the added floating gate, there is a limitation to the size and scalability of the FLASH devices [12].

SRAM technology is widely used in the semiconductor industries today because of their scalability and ability to achieve miniaturization [13]. From the invention of the SRAM till present day, we heavily rely on the SRAM devices as our primary random-access memory devices . On one hand, the passive nature of these devices has led us to make power efficient SRAM devices . On the other hand, the basic building element, MOSFET has been shrinking from a size of 100 μm in 1965 [14] to an astonishing 5 nm in 2020 [15]. This has led us to make more compact SRAM devices in the recent decades. Figure 2(a) below shows the number of transistors devised in any single processor over the last four decades. The density of transistors per processor has almost doubled every two years[16] . This has led to the doubling of computing power in our devices every two years [17]. The cost of production also has been decreasing by the same rate as the technologies has matured. The progress in the scalability has been an impressive feat of achievement. The development of new and more efficient transistors is dictated by the Moore's law which indicates that the number of transistors per unit area double every two years [14]. The figure 2(a) below depicts the growth of density of transistors over the last four decades.

However, as the size of each unit of SRAM decreases, and as the node thickness of its building block gets smaller, the power consumption of the devices increases drastically due to the quantum tunneling effect [18]. The behavior of the electrons also become more and more unpredictable as the nodes get smaller. So, it is believed that the MOSFET-based memory technology might not be the best option to support next generation electronics. This has led the

scientific community to look for alternate technologies that can replace MOSFETs in the future. Because of all the drawbacks of the SRAM and FLASH memory technologies, the study of Resistive Random-Access Memory (ReRAM) has been gaining momentum. ReRAM technology is emerging as one of the most viable technologies in the development of non – volatile memory devices [19]. The ability to retain information in off- state because of the use of low and high resistance as the “on” and “off” state makes such devices very plausible candidates as the substitute to current technology . Besides that, ReRAM devices have a very simplistic Metal-Insulator- Metal (MIM) structure. This makes ReRAM devices extremely easy to industrially produce and quantify [3] . Due to the structure and the principle of resistive switching, the ReRAM devices are faster than SRAM and FLASH devices and have higher endurances over large cycles [20]. Because of these qualities and backward compactivity with CMOS technology, ReRAM devices are believed to be the next generation of memory devices.

Hence, in this research, we will explore different components that can be used to build ReRAM devices and research the impact of different fabrication process.

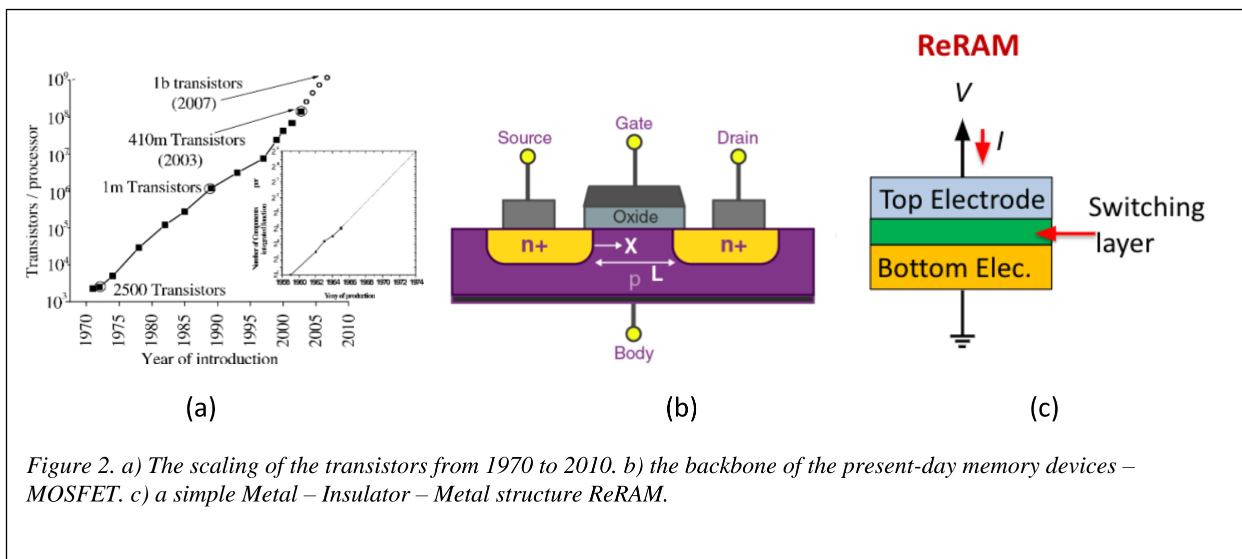


Figure 2. a) The scaling of the transistors from 1970 to 2010. b) the backbone of the present-day memory devices – MOSFET. c) a simple Metal – Insulator – Metal structure ReRAM.

CHAPTER 2: Background and Motivation

2.1 Introduction to Resistive Random-Access Memory devices

As discussed above in the introduction section, the need for new technologies as a substitute for MOSFET has started to feel imminent. ReRAM devices have the potential to be substitute for MOSFETs as the de-facto storage device. Even though the first study of ReRAM was conducted in 1960 [21], the research on these devices have only intensified in the last 20 years. A ReRAM device can store data in the form of resistance: Low Resistance State (LRS) and High Resistance State (HRS) [3] . These states can be changed by applying Set and Reset voltages for a certain period and read by applying a small voltage, typically less than 0.1V . A ReRAM is also well known as a non-volatile technology as the information is stored in a passive resistor [22]. In other words, the information stored in a resistor can last several decades without supplying a power . The ability to store data without active power consumption is one of the greatest characteristics of ReRAM devices [3] . It also features a superior reading speed and low power consumption by accessing information through the measurement of resistance states [23] .

ReRAM devices have seen an increasing use in the field of memory devices and sensors. A typical ReRAM device has a simplistic Metal Insulator Metal structure [22] . Various metals have been used as the top and the bottom electrode [3]. These electrodes are mostly transition metals. The insulating layer in the middle is used as a resistive switching layer. The insulating layer can be made up of transition metal oxides, metalloid oxides, and reactive non-metal oxides [24] . Besides the metal oxides, in the recent applications, some researchers have started using different type of inorganic solvents like PEDOT:PSS, Graphene, and Nafion as well for the insulating layer [25]. These insulating layers exhibit resistive switching properties upon the

application of appropriate voltages(set and reset voltages). The resistive characteristics of the switching layer can vary widely depending on the nature of the top and bottom electrodes [26]. Table 1 shows the variety of ReRAM devices with different electrodes and switching layer combinations.

Table 1. Most commonly researched ReRAM devices along with the electrodes, switching layer materials, ratio of resistances and set/reset voltage [3].

Top Electrode	Switching Layer	Bottom Electrode	HRS/LRS ratio	V_{set} (V)	V_{reset} (V)
Ti/W	TiO_x/MgO	Ru	< 32	1.4 V	-1.8 V
Cu	TiO_2	Pt	~30	0.8 V	-1.5 V
Al/Ti	MnO_2	Pt	>10	1.5 V	2.0 V
Au	ZrO_2	Ag	10^4	-0.5 V	0.6V
Ti	ZrO_2	Pt	Not significant	1V	-1.5 V
Ag	MnO/Ta_2O_5	Pt	10^6	0.8 V	-1.1 V
Ti	Ta_2O_5	Au	2370	0.7 V	-0.7 V
Pt/Ti	Al_2O_3	Pt	Not significant	1V	-1.5 V
Al/Ti	Al_2O_3	Pt	> 10	1.5 V	-2.0 V
Pt	ZnO	Pt	> 100	1.1 – 2.3 V	0.4 – 1 V
Au	ZnO	ITO	10^4	-0.5 V	0.6 V
TiN	HfO_2	Pt	10^6	-4.3 V	6.0 V
W/Zr	HfO_2	TiN	Not significant	0.5 V	-1.25 V
Pt	NiO	Pt/Ti	Not significant	1 V	-1.5 V
Al	HfO_x	Al	10^4	1.8 V	0.8 V
Pd	HfO_x	TiN	10^3	2.2 V	-2.2 V
Au/Ti	TiO_{2-x}	Au	> 10^4	1 V	-1 V
Pt	TaO_x	TiN	Not Significant	-2 V	-1 V

The simple Metal-Insulator-Metal structure in ReRAM devices has enormous advantages in the research and production of ReRAM devices. In the recent decades, scientists have been exploring the effect of different types of metal electrodes and the insulating material in the resistive properties of ReRAM devices. Metal electrodes can be easily substituted and have a huge impact in the resistive property of the ReRAM devices [27]. Some of the most common electrodes used in the past are – Al, Ti, Cu, Ag, W and Pt. [3]. Most of the ReRAM devices researched in the past have used some form of metal oxides as the switching layer [22] . The table below shows the different types of used metal oxides as resistive switching layer alongside with the top and bottom electrodes of the resistive devices [3]. The table also summarizes the ratio of the resistances alongside the set and reset voltages.

Devices that use combination of electrochemically active elements like Ag, Al and Ti as their electrodes exhibit better switching properties compared to elements like Pt, Ru and W [28]. In an experiment, Shuang Goa et al found that devices with a structure ITO/P3HT:PCBM/Cu structure displayed a 10^3 magnitude difference between LRS and HRS [28]. When the same structure was used, but replacing the Cu electrode with Pt electrode, the gap between HRS and LRS disappeared. The electron affinity of the active metal contribute to a better resistive switching property [28]. In our research, we intend to explore the impact of organic switching layer, type of electrodes and anneal temperature in the resistive property of the ReRAM devices.

Material scientists have found that some metal oxide insulators are able to change their resistances under application of low voltages [3]. As a result of these properties, binary metal oxides have been widely used as a resistive switching layer [3]. Table I shows the variety of switching layers used by the different researchers over the last two decades. Reactive nonmetal oxide like SnO_2, GeO, SiO_2 and transitive metal oxides like FeO, CuO and ZrO_2 are the most

used switching layers [29]. These metal oxides when used with active metal electrodes like Ag and Al tend to exhibit good resistive switching properties.

As we can see in Table 1, most of the ReRAM device research has been concentrated in the fabrication of Metal/Metal Oxide/Metal structured ReRAM devices. Some organic compounds are also found to have resistive switching properties. Organic compounds are widely used for optoelectronic devices such as solar cells and sensors [25]. But there have been very few instances where organic compounds are used as resistive switching layers for a ReRAM device. The use of organic chemical compounds as a resistive switching layer has been an area of immense interest in the scientific community. Although there have been several uses of resistive memory devices in the field of sensors and fuel cell technologies, there have been only a few studies that have used organic materials to make resistive memory devices. In this research, we intend to explore the resistive characteristics of ReRAM devices made up of organic compound as switching layer and the impact of the different types of electrodes in those types of devices.

2.2 ReRAM Switching Mechanism

ReRAM devices can display two different resistive states – HRS and LRS. This phenomenon is possible because of the formation of conduction filament in the switching layer . When a positive setting voltage is applied – a channel of conducting ions or valence electrons align [3]. This causes the device to be conductive, hence achieving a low resistance state. On the contrary, when a opposite polarity of voltage is applied to the electrodes, the conduction filament dissociates and hence resulting into a high resistive state. Figure 3 shows a process of the formation and dissociation of the conduction filaments.

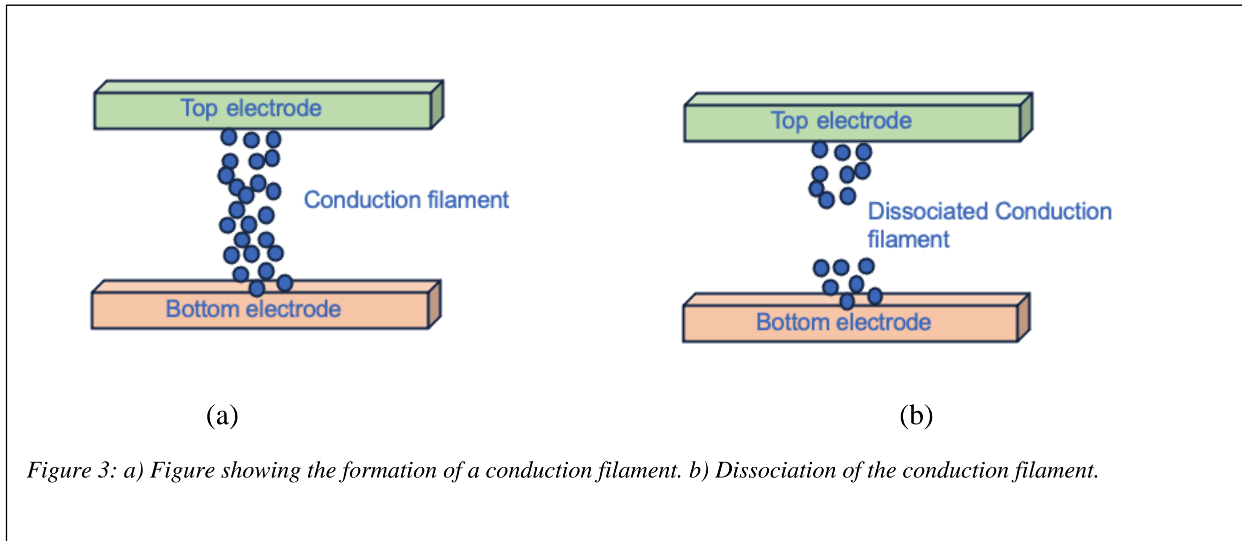


Figure 3: a) Figure showing the formation of a conduction filament. b) Dissociation of the conduction filament.

The conduction filament is mainly formed by two different mechanisms. In some ReRAM devices form the conduction filament is formed by the accumulation of the metal ions present in the electrodes [3]. The filament formed by the channeling of these ions is called conduction bridge filament. The ReRAM devices that operate with this principle are called Conductive bridge random access memory (CBRAM) [30]. Conduction bridges are usually formed in ReRAM devices with electrochemically active top electrodes and relatively inert bottom electrodes. Some of the electrode pairs capable of forming the conduction bridge are Ag/W, Cu/Al, Cu/Pt and Cu/W [31]. These types of ReRAM devices are generally faster in responding to the voltage change.

Some ReRAM devices form an oxygen valency filament as a conduction channel. In these devices, when a voltage is applied to the electrodes, oxygen valences are created in the switching layer. The ReRAM devices that operate with this type of conducting mechanism are called Oxygen vacancy filament based random access memory (OxRAM) [32]. This causes the switching layer to attract electrons forming a conduction channel. The oxygen valency is formed in the metal oxide-based switching layers [30]. ReRAM devices with transition metal oxides

usually change their resistive states depending on the negative or positive polarity of voltage is applied. These types of ReRAM devices are slower in speed but are known to have a higher endurance.

2.3 Organic Compounds as Resistive Switching Layers

Organic compounds are easy to synthesize and can be used in solution form. Contrary to metal oxides as mentioned above organic compounds can be deposited into different type of surfaces in several different ways: vapor deposition, spin-coating, blade coating, and screen printing . Among them, spin-coating technologies have been widely used in a laboratory scale as they are the most cost-effective costing method and provide precise thickness control in a small form factor [33]. Many organic compounds like Nafion, PEDOT:PSS are also soluble in polar solvents as well as several organic solvents [25]. These properties make it easy for the scientist to try mixing several different compounds for tailoring the properties of organic compounds. Hence, it becomes very easy and common to modify the composition of the resistive layers with organic compounds to any desired extent to test different characters of the devices. Therefore, being able to produce organic compound bases switching devices can be crucial towards development of next generation of memory devices.

Organic compounds have seen a growing intertest in the field of sensing applications and in the fuel-cell membrane structures. Some organic compounds such as PEDOT: PSS and Nafion, have found their use as a resistive switching layer in the field of biosensors as well [25]. For example, highly effective and cost-effective biosensors have been developed by using the MIM structure with polymers like graphene, PEDOT and Nafion [25] where the polymer layer serves simultaneously as a sensing layer [4], but also as an information storage. The switching layers

used in these sensors operate in the principle of the change of resistance upon applying voltage, i.e., they produce different resistance phases while different voltage is applied.

In this research, we explore the use of Nafion as a switching layer, and the impacts of different electrodes and the impact of anneal temperature in Nafion based devices. The main purpose of this research is to characterize resistive switching of Nafion-based memory devices by studying the effect of annealing temperature of Nafion and pairing different metal electrodes.

2.4 Background on Nafion

Nafion is a synthetic polymer organic compound invented by Walther Groth in late 1960's. The chemical formula of Nafion is $C_7HF_{13}O_5S$. C_2F_4 and is shown in Fig. 4 [34]. Nafion has a high a melting point of around 200 °C and is soluble in alcoholic solvents as well as polar solvents like water.

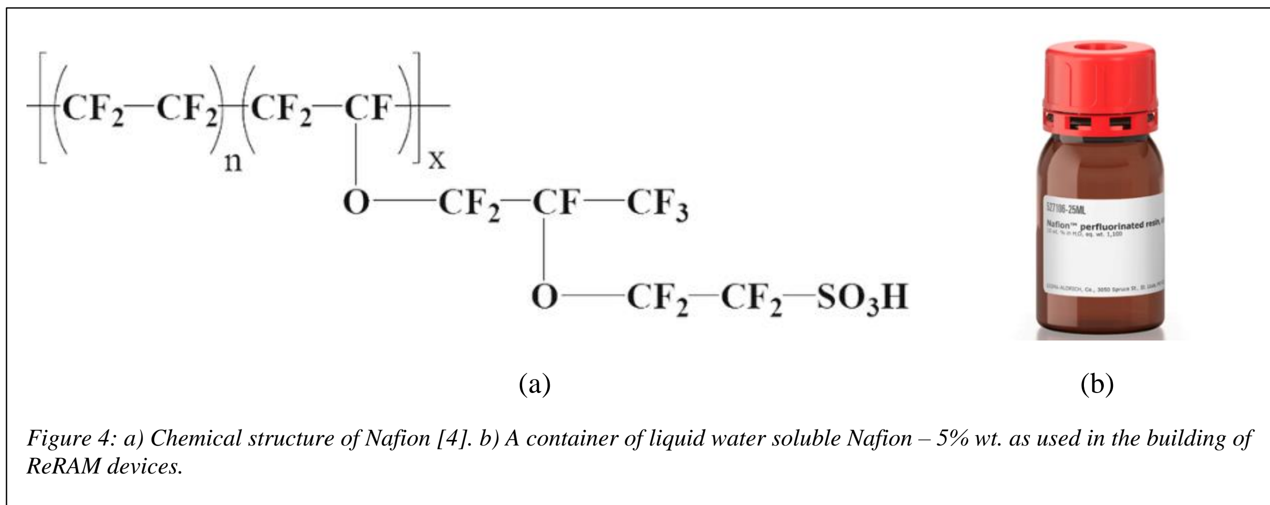


Figure 4: a) Chemical structure of Nafion [4]. b) A container of liquid water soluble Nafion – 5% wt. as used in the building of ReRAM devices.

Nafion is a sulfonated tetrafluoroethylene-based polymer with some conductive properties . It is known to have high hydrophobic properties and hence can be modified to make different types

of resistive materials [35]. Nafion has been used in sensor applications and several fuel cell applications. Nafion is a cation exchange polymer, and hence blocks anionic particles from reaching the conductive surface [25]. When the concentration of water in the Nafion molecules is changed, it sways the anionic particles more towards the surface [36]. This creates a larger path for conductance, thereby making it more conductive . Because of a moderate melting point and a high solubility, it is a great candidate to produce organic resistive switching devices.

Nafion consists of a perfluoroalkyl-based main chain and sulfonic acid group chains. Due to its unique structure, this material exhibits a distinct phase separation between the hydrophobic and hydrophilic domains [37]. These domains are very versatile and change their structure depending on the amount of humidity. Nafion's morphology and crystalline structure are greatly affected by thermal annealing temperature [38], hence, different resistive switching behavior can be obtained by changing the anneal temperature. In this research, we examine the effect of different anneal temperature and the effect of the different metals for top and bottom electrodes for a Nafion-based ReRAM device.

2.5 Definitions

a) *High Resistance State (HRS):*

   During a voltage sweep, the ReRAM devices initially show high resistance which is called as HRS and the slope of the IV curve is small. This is the state of the device which can be used as the OFF state or a 0 for digital state. Figure 5 shows the vertical structure of ReRAM devices and the I-V curve to show various parameters.

b) Low Resistance State (LRS):

When a ReRAM device reaches the set voltage, a conducting channel is formed between the two electrodes, decreasing the resistance of the switching layer. The state where the resistance of the ReRAM devices is very low is called LRS (Fig. 5 (b)). This is the state of the device which can be used as the ON state or a 1 for digital state.

c) Set Voltage (V_{set}):

Set voltage is the voltage where, an abrupt change of resistance occurs and a conductive path is formed. The resistance of the device changes from high resistance state (HRS) to a low resistance state (LRS) at this voltage point. Figure 5 (b) shows the set voltage for a typical resistive switching device.

d) Reset Voltage (V_{reset}):

Reset voltage is the voltage at which the resistance of the device changes from low resistive state (LRS) to a high resistive state (HRS) [39]. In bipolar devices the set and

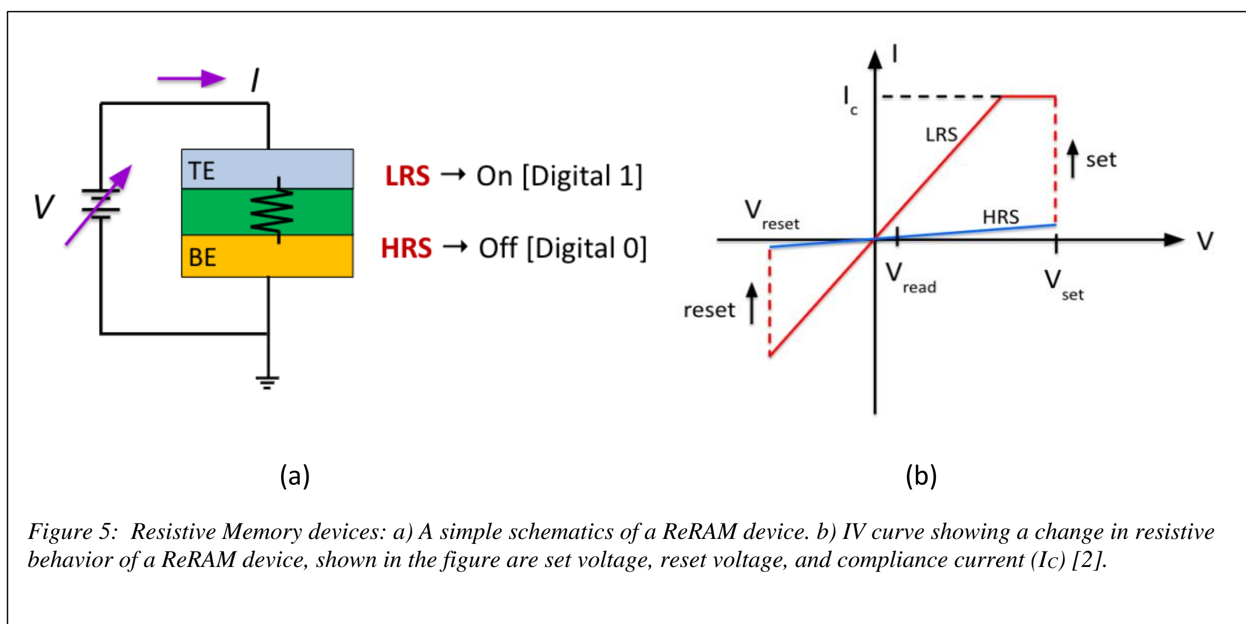


Figure 5: Resistive Memory devices: a) A simple schematics of a ReRAM device. b) IV curve showing a change in resistive behavior of a ReRAM device, shown in the figure are set voltage, reset voltage, and compliance current (I_C) [2].

reset voltages are present at oppositive polarities. Once this voltage is achieved the device can stay at a high resistance state and can be assigned a digital value of 0.

e) *Reading Voltage (V_{read}):*

A small voltage, called as a reading voltage, is applied to measure the amount of current at HRS and LRs. V_{read} must be small enough not to trigger the resistive switching between HRS and LRS and to lower power consumption as well. In general, its magnitude is about 0.1V or less. In our experiment a reading voltage of 0.1 V is used. Once the current is measured at the V_{read}, Ohm's law is used to calculate the resistance value. A good resistive switching is achieved by showing good separation between LRS and HRS and this ratio is called as ON/OFF ratio and considered as one of the important merits of ReRAM.

f) *Forming Voltage:*

ReRAM devices, in general, have a very high resistance in the beginning and often require a higher voltage to form a conductive channel before exhibiting any switching characteristics. Once a high forming voltage (5V – 10 V) is applied, the holes and the electrons in the device line up towards their counterpart electrodes, creating a conductive channel. The voltage that is applied to form this type of conductive channel is called a forming voltage. After the forming process, ReRAM devices show resistive switching at lower voltage, i.e., the set/rest voltages are lower than the forming voltage.

g) *Compliance Current (I_c):*

A current is set to prevent the ReRAM devices from allowing excessive current. When a large current conduct through the resistive switching layer, ReRAM devices can have a

permanent damage and no longer exhibit a resistive switching behavior. To prevent this, instrument can set a limit on the current which is called as a compliance current. It is useful when a forming voltage or set voltage is applied where a large current is expected.

CHAPTER 3: Design, Fabrication and Characterization Techniques

3.1 Device Structure

Conventionally, there are two types of device structure of memory devices built for ReRAM devices: a) Lateral Structure and b) Stack (vertical) structure [2]. The model of lateral and stack structure is shown in Figure 6.

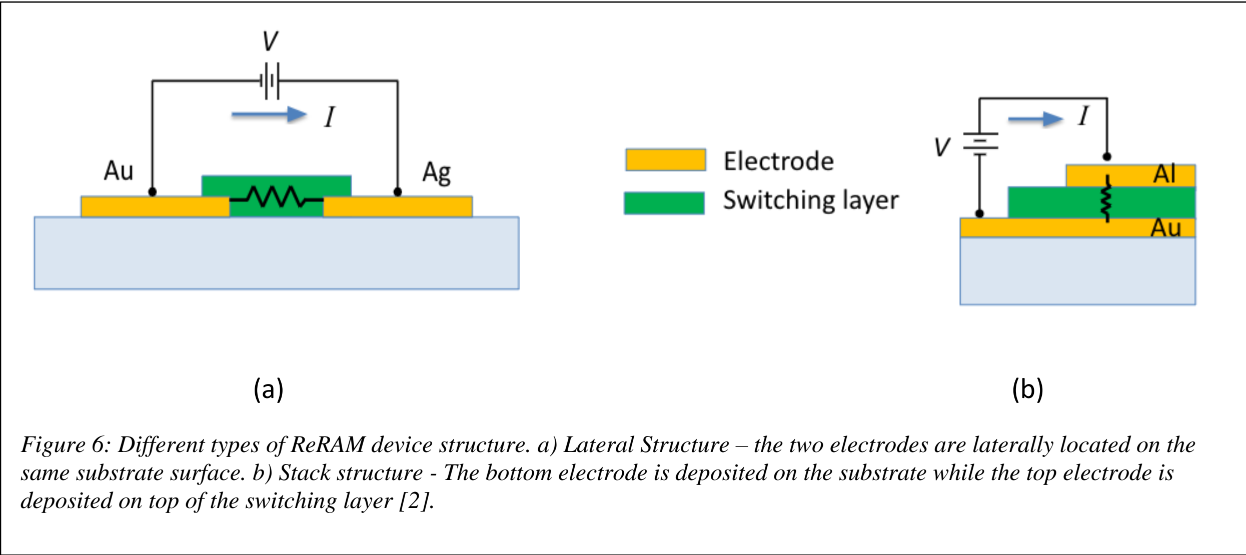


Figure 6: Different types of ReRAM device structure. a) Lateral Structure – the two electrodes are laterally located on the same substrate surface. b) Stack structure - The bottom electrode is deposited on the substrate while the top electrode is deposited on top of the switching layer [2].

In a lateral structure, both positive and negative electrodes are deposited on the lateral surface. After cleaning the glass substrate, the metal electrodes are patterned via photolithography process and the resistive switching layer is deposited uniformly using either vapor deposition in a vacuum chamber or spin coating method. While shadow masks are typically used to deposit the resistive switching layer only on the selective area in the vapor deposition process, the layer can be easily patterned by swabbing down the layer with a swab for the spin coating method.

Stack Structure of ReRAM is the most widely used device structure because of the easiness in its fabrication process. In our experiments, we designed and fabricated the stack structured devices.

3.2 Device Components

a) Bottom Electrode (BE):

In our experiment, two sets of three devices are prepared with different bottom electrodes. The first three devices have Copper (Cu - 99.99% pure) as the bottom electrode. The other set of three devices have Gold (Au – 99.99 % pure) as our bottom electrode. The BE is deposited on our glass substrate using vapor deposition method. The glass substrate is cleaned thoroughly and treated with plasms prior to the deposition of the BE. Before deposition of the Cu as the BE, a 20 nm Chromium (Cr) is deposited. The layer of Chromium provides adhesion between the Cu layer and the glass substrate and prevents the BE from peeling off. The Cr layer is only deposited for the Cu devices. Cr, Cu, and Au are deposited inside the vacuum chamber at about 3×10^{-6} Torr.

b) Resistive Switching Layer (SL):

Our resistive switching layer is a Nafion (5 wt. % dissolved in water purchased from Sigma Aldrich), a trademarked organic compound that is known for its ion-selective barrier and semiconductor like properties. During the course of several experiments, a variety of composition of Nafion solution were tested. Other solutions for the SL tested were Nafion – 10 wt. % solution, and a combination of Nafion with different pH solutions. The 10 wt. % Nafion solution had several solute coarse particles, which upon spin coating created non-uniform surface area. Nafion – 5 wt. % solution seemed to have a consistent and predictable properties, and hence was chosen as the SL. A 0.45 µm filter was used for the filtration of the 5 wt. % Nafion to

achieve a consistent SL. The SL was then coated on the Cu or Au electrode by using a spin coating method.

c) Top electrode (TE):

Aluminum (99.99%) metal is used as our top electrode on all of our devices. A thermal evaporator (Angstrom Engineering Covap II) is used to deposit 200nm of Al on top of the resistive switching layer through the metal shadow mask in a vacuum chamber. Over the course of our research, we used different types of TE for some of the experiments: Silver (Ag), Gold (Au), and Aluminum (Al). Among them, Al showed the most promising switching property and hence was chosen as our TE.

3.3 Types and Size of the devices and their nomenclature:

Three different sizes of ReRAM devices are developed for our experiments. All the devices produced have a circular top electrode pattern with a diameter of mm, mm, and mm. The final set of our experiment consisted of 9 cells as shown in figure xx. Each device was fabricated on a 1”

Table 2. Nomenclature of devices with their components and temperature developed in the lab.

Device #	BE	(SL)	TE	Anneal Temperature(°C)
1 and 2	Cu	Nafion – 5% wt	Al	60 °C
3	Au	Nafion – 5% wt	Al	60 °C
4	Au	Nafion – 5% wt	Al	90 °C
5 and 6	Cu	Nafion – 5% wt	Al	90 °C
7	Au	Nafion – 5% wt	Al	30 °C
8 and 9	Cu	Nafion – 5% wt	Al	30 °C

× 1” glass substrate and contained a total of 3 large devices, 6 medium devices and 9 small devices. Table 2 shows the naming conventions used for the final set of cells.

3.4 Fabrication of the Nafion-based ReRAM devices

The first step of fabricating the devices is the preparation of the substrate. Our substrate for this experiment is a regular glass slab with a thickness of 1mm. The glass slab is first cut into small 1” × 1” samples using a glass cutter. We prepared a total of 9 glass substrate with the intention of producing 4 - Au/Nafion/Al and 5- Cu/Nafion/Al samples. The glass samples are then cleaned using a clean paper towel. The glass substrate is then transferred to a fume hood and treated with a series of chemical cleaning solvents to get rid of all organic and inorganic compounds. The cleaning process took place in a fume hood (see Figure 7).

In our experiment, the glass samples are first treated with acetone for 50 minutes. A 50 ml beaker is filled half the way with acetone solution and put inside an ultrasonic cleaner. The samples are then immersed inside the acetone solution and sonicated for 50 minutes. The

Figure 7: The fume hood in the clean room. Spin coating & annealing is performed in this chamber.

samples are then transferred to a beaker with similar amount of Iso Propyl Alcohol (IPA). They are then sonicated for another 50 minutes inside the ultrasonic cleaner. The samples are then placed in a beaker with De Ionized (DI) water for 15 minutes inside the ultrasonic sonication machine. Finally, the samples are taken out of the water beaker and blown by the Nitrogen gas present in the chamber. The glass substrates are then left to dry out in room temperature inside the fume hood.

The glass substrate samples are then inspected under the microscope to determine if they are clean or not. The treatment of the samples with the acetone and IPA ensures that the removal of organic contaminants from preparing the samples. In some cases, if the substrate has residues, they are treated with concentrated phosphoric acid (H_3PO_4). The glass samples are immersed in the (H_3PO_4) solution. The beaker is then placed in the ultrasonic cleaner for 5 minutes. Then the samples are rewashed with DI water and dried using N_2 gas.

The cleaned samples are then transferred to the plasma cleaner. The samples are treated with air plasma at 20 Watts for 2 minutes for additional cleaning of the substrate. The samples are then brought back to the globe box and respective metal electrodes are deposited. Our samples consisted of 2 sets of devices, 1 set with Cu as the BE and the other set with Au as the BE.

Table 3. Table summarizing the types of devices produced in the lab.

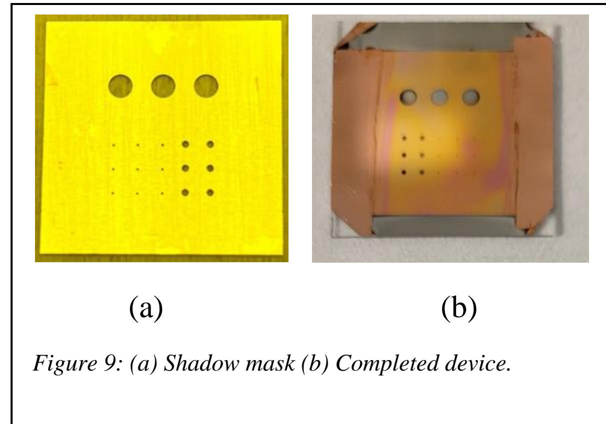
Bottom Electrode	Annealing at 30°C	Annealing at 60°C	Annealing at 90°C
Au	Au (bottom) / Nafion / Al (top)		
Cu	Cu (bottom) / Nafion / Al (top)		

Table 3 summarizes the types of the device built for this research. For the devices with Au as the electrode, vapor deposition is performed under the pressure of 3.1×10^{-6} Torr at a rate of 2 Å/s to achieve the thickness of 200 nm. However, for the devices as Cu as the BE, a thin layer (20 nm) of Chromium is deposited to increase adhesion. After the Cr deposition, a 300 nm layer of Cu is deposited at the same pressure by the method of vapor deposition. The top and the bottom electrodes were deposited in the glass in the globe box located in the lab (see Figure 8).

Figure 8: Globe box is used for vapor deposition and other chemical processes.

The devices are then taken out of the globe box to the fume hood for spin coating of the Nafion. First, Nafion is filled in a 50 ml syringe with a 0.45 µm filter. Nafion is then dropped smoothly into each device while they are on the top of the spin coater chuck. The spin coater is then set for a rotational speed of 1000 rpm for 40 seconds. A uniform layer of Nafion is eventually coated on the samples. The samples are immediately annealed on a hotplate at 100° C for 20 minutes. The

samples are further annealed in a pre-heated oven overnight for 22 hours at 30° C, 60° C and 90° C respectively. After the annealing process is completed, aluminum top electrode (200nm) is deposited through the metal shadow mask. The completed devices are named, labeled and then stored in a humidity free chamber for further testing and characterization. The pictures in Figure 9 (a) and (b) show the shadow mask and the completed Nafion-based ReRAM device. Each individual device contains 3 large, 6 medium and 9 small memory cells. Table 3 summarizes the annealing process and the type and electrodes and the general composition of our ReRAM devices.



(a) (b)

Figure 9: (a) Shadow mask (b) Completed device.

3.5 Characterization of ReRAM devices

The ReRAM devices are characterized by applying a sweeping voltage between -3V to + 3V with a 10 mV step in a dual sweep mode using a Keithley 4200 semiconductor analyzer. A compliance current (I_{CC}) of 100 mA is set for each cycle of IV sweeps. Before the initial sweep of ReRAM devices, the devices are inspected to see if the forming process is required. In order to do so, a -5V to +5V dual sweep in conducted. The I-V curve of such a sweep did not show any drastic change, so it was concluded that the devices did not require any forming process. Hence, we performed a -3V to +3V sweep on the devices individually.

A device is concluded to have resistive switching properties if there is a sudden change in resistance in this voltage range. Figure 10 (a) and (b) show the IV curve of the devices without a

resistive switching and with resistive switching, respectively. In order to test long term stability, we performed a cycling test in which devices are tested for 50 cycles of the voltage sweep.

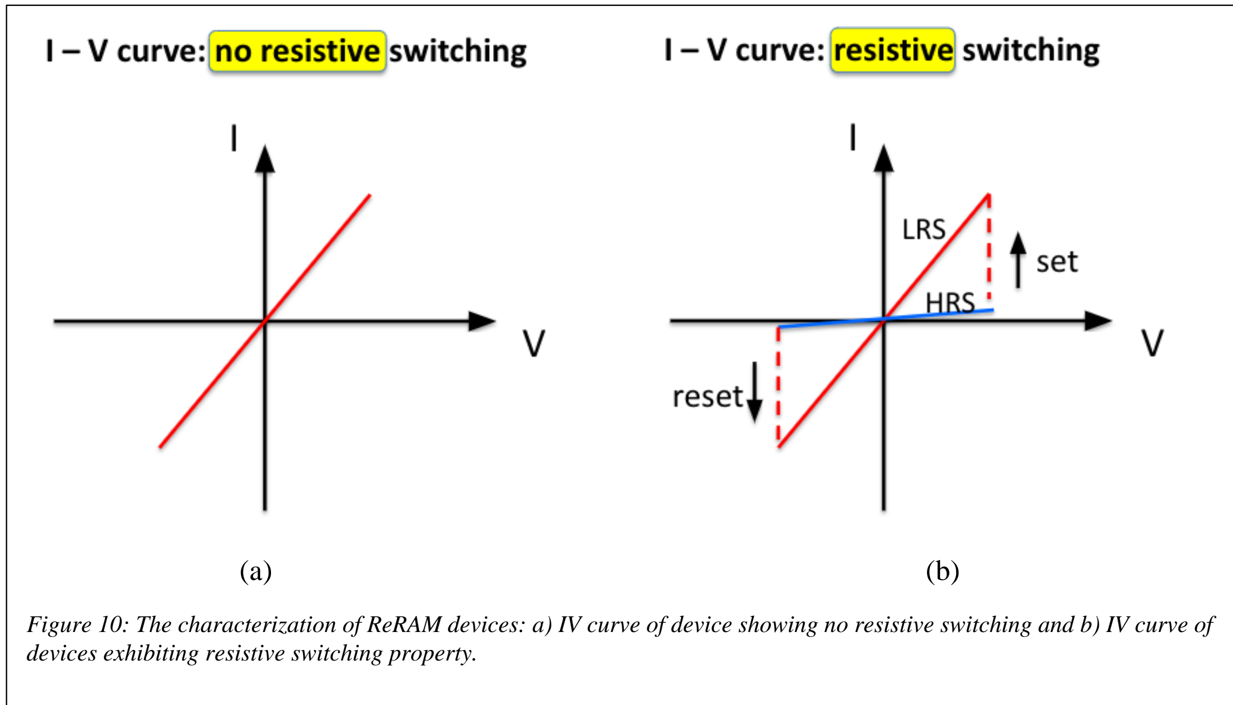


Figure 10: The characterization of ReRAM devices: a) IV curve of device showing no resistive switching and b) IV curve of devices exhibiting resistive switching property.

CHAPTER 4: Results and Discussions

The resistive properties of any memory devices rely on the type of electrode, the property of the switching layer and the conditions of formation of the devices. In our research, we wanted to evaluate and analyze the resistive property of our devices depending upon the type of electrodes as well as the annealing temperature of the switching layer. Hence, half of the devices built in the lab were of the structure of Cu(bottom)-Nafion-Al(top) and the other half devices were Au-Nafion-Al. All these devices were fabricated under the same lab conditions and same protocol. These two sets of devices were then annealed at 30°C, 60°C, and 90°C temperature inside an oven to compare the difference in resistive switching properties and their dependence on the types of electrodes.

A dual voltage sweeps of -3V to +3V (-3V → +3V → -3V) was performed on each device first for 3 cycles to ensure consistency. A compliance current of 100 mA was set to avoid any permanent damage to the ReRAM devices. The devices were then subjected through the same voltage range for additional I-V measurement for 50 cycles. Each type of device (i.e., large, medium, and small) were characterized using the same setting and standards. The measured data was graphed and analyzed using OriginLab's Graphing and analysis tool. 1st cycle and 50th cycle of the I-V sweeps are graphed separately along with the 50 cycles of the I-V curves.

The resistance values (HRS and LRS) are calculated at a reading voltage of 100 mV by using the Ohm's law. These resistances are plotted over the 50 cycles to show the stability of the device switching behaviors. The HRS and LRS are clearly visible in some of the devices whereas some other devices show a very small or no difference between HRS and LRS. In this research, the difference of the width in between HRS and LRS for different devices is analyzed. The average

resistance of the devices with gold vs copper electrode at different annealing temperature in an oven is plotted to analyze the resistive switching.

4.1 Effect of different annealing temperature in Cu/Nafion/Al devices

In this section we discuss how the resistive switching behaviors of the ReRAM devices are affected by different types of electrodes (Cu vs. Au) and different annealing temperature (30 °C, 60 °C, and 90 °C) in an oven. The same parameter of analysis is applied to three different sized devices (large, medium, and small) in this research. The devices are then subjected to a +3V to a -3V voltage sweep for several cycles. The compliance current is set to 100 mA under the step time of 10 Number of Power Line Cycles (NPLC). A moderately large NPLC(in the range of 5-10) increases the AC noise integration time and hence increases the resolution of our measured current and accuracy of measurement [40]. We choose NPLC of 10, because our measured current is in the order of milli Amperes. Using a 10 NPLC provides a consistent reading of the current. A single cycle, 50 cycles of voltage sweeps and their respective resistances at reading voltage are graphed, analyzed, and discussed below.

4.1.1 I-V characteristics at 30 °C, 60 °C, and 90 °C

Figure 11 shows a single I-V curve of the device annealed at 30 °C, 60 °C, and 90 °C in an oven, respectively. All three different sized devices are tested using the Keithley 4200 semiconductor characterizer to generate I-V curves. The hysteresis becomes large as the annealing temperature of the devices increases. However, the most pronounced hysteresis is obtained in the devices that

are annealed at 60 °C temperature. The hysteresis gets narrower for device annealed at 90 °C across all three different sizes.

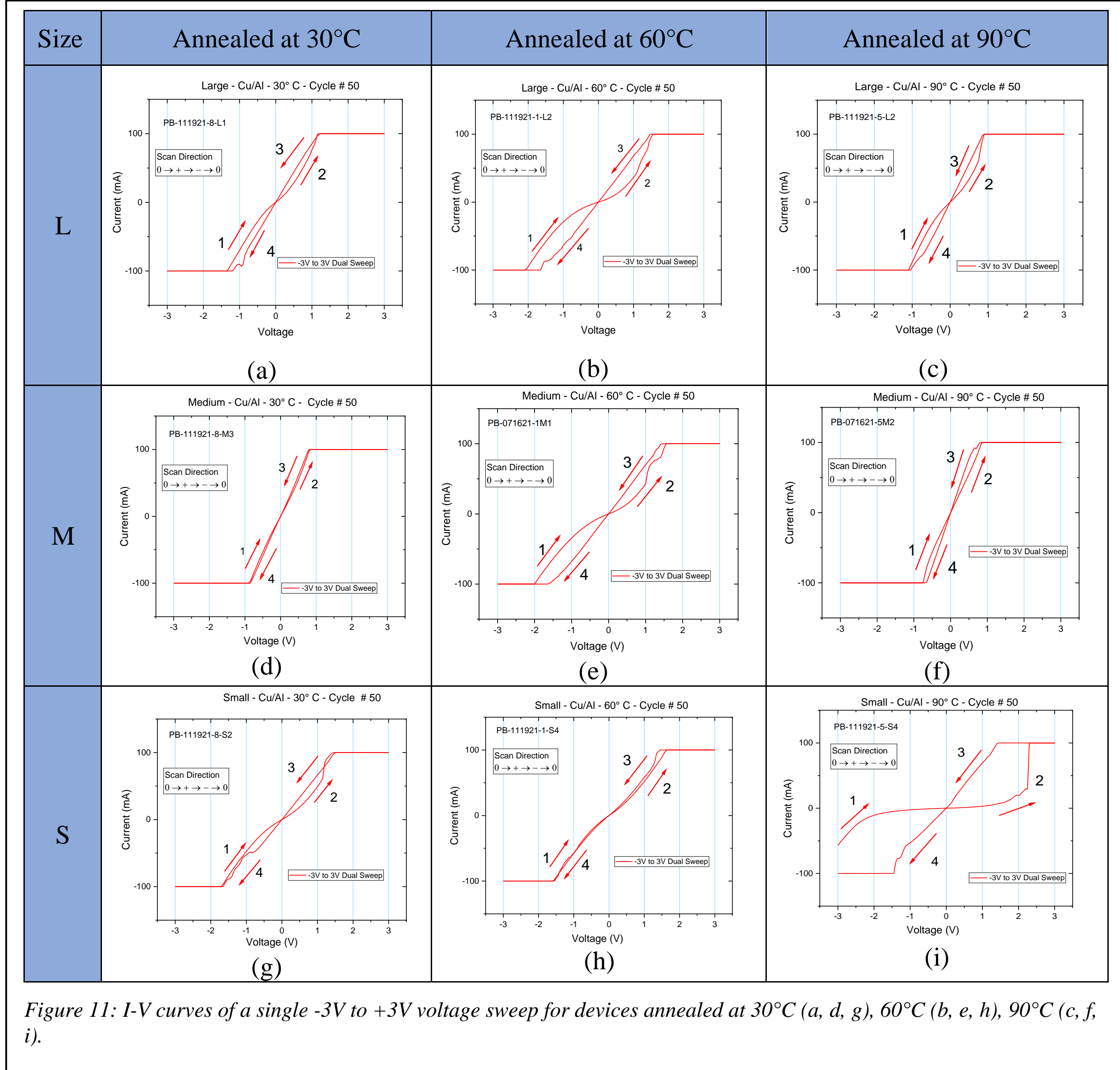


Figure 11: I-V curves of a single -3V to +3V voltage sweep for devices annealed at 30°C (a, d, g), 60°C (b, e, h), 90°C (c, f, i).

4.1.2 Hysteresis of the I-V curves for 50 cycles

Figure 12 shows small, medium and large Cu/Nafion/Al devices, plotted for a sweep of -3V to +3V for a total of 50 cycles. Over the 50 cycles of the voltage sweeps, the devices show consistent hysteresis patterns. The hysteresis gap seems to remain constant over the 50 cycles. The device annealed at 60 °C again shows the best hysteresis behaviors over 50 cycles. This means that the devices annealed at 60 °C retain the HRS and LRS values well over the 50 cycles, hence suggesting a better resistance switching. While the hysteresis curves are well overlapped

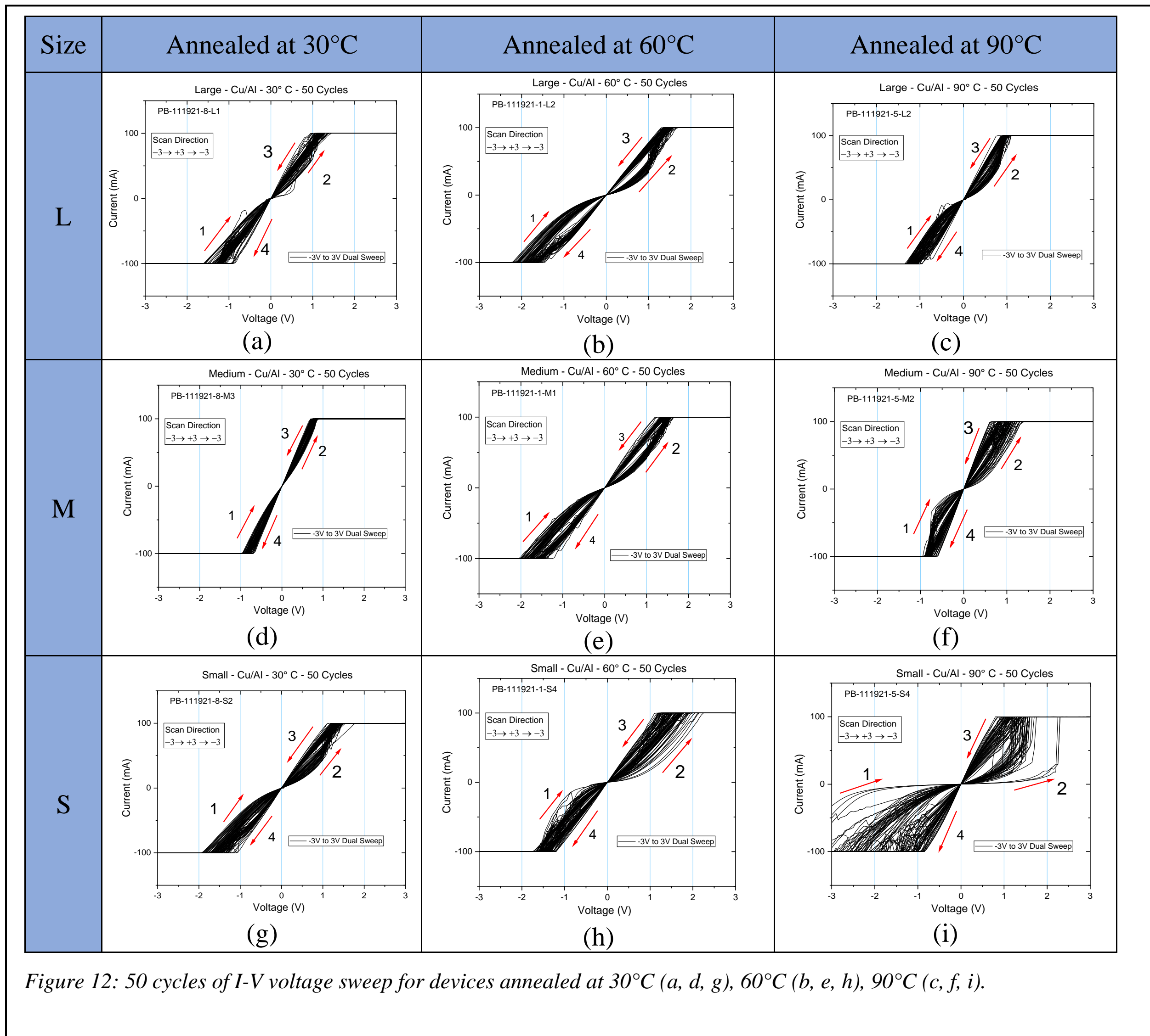


Figure 12: 50 cycles of I-V voltage sweep for devices annealed at 30°C (a, d, g), 60°C (b, e, h), 90°C (c, f, i).

for the most of devices, the smaller cell size annealed at 90 °C shows a rapid decrease of the hysteresis for the first few cycles but become stable after those cycles (Fig. 12 (i)).

4.1.3 HRS and LRS changes over 50 cycles

In this section, we characterize the resistances of different sized devices with Cu/Nafion/Al structure at different annealing temperatures. The resistance was measured at the reading voltage of 100mV while the devices were in "SET" and "RESET" states as defined above in the

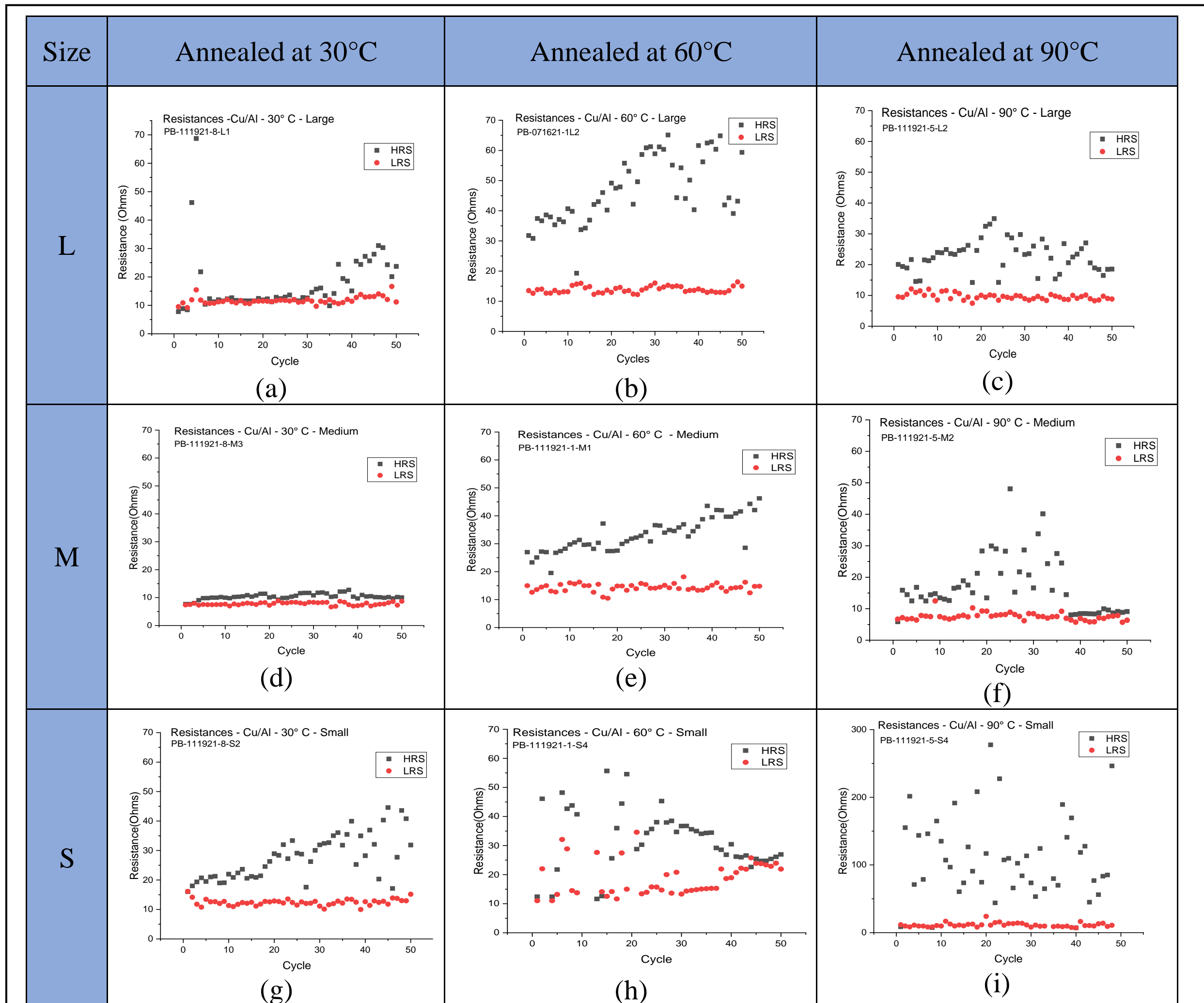


Figure 13: HRS and LRS over 50 cycles for devices annealed at 30°C (a, d, g), 60°C (b, e, h), 90°C (c, f, i).

definitions. HRS and LRS were then plotted for fifty cycles of voltage sweep with the same scale except the Fig. 13 (i).

For the devices with medium and large cell size, annealing temperature at 60°C exhibits the largest separation between HRS and LRS and the devices annealed at 30°C do not show a clearly distinguishable separation between them (Fig. 13 (a, d)).

Table 4 summarizes the resistances at HRS and LRS for the Cu/Nafion/Al devices. When the large and medium devices annealed at 30°C and 60°C are examined we can see that the HRS/LRS gap in the devices approximately doubles. Thus, among all sized devices the anneal temperature of 60°C produces the best hysteresis gap which is also indicated by the larges HRS/LRS ratio except the small cell size device annealed at 90°C. Larger and medium devices

Table 4. Table showing the average values of high and low resistive states of Large Cu-Nafion-Al devices annealed at different temperatures.

Size	Resistance (Ω)	30 °C	60 °C	90 °C
Large	LRS	11.72 ± 1.31	13.88 ± 1.07	9.63 ± 1.02
	HRS	17.45 ± 10.52	47.08 ± 10.92	22.76 ± 5.01
	HRS/LRS	1.49	3.39	2.36
Medium	LRS	7.78 ± 0.52	14.34 ± 1.36	7.51 ± 1.20
	HRS	10.38 ± 1.02	33.29 ± 6.03	17.23 ± 8.96
	HRS/LRS	1.33	2.32	2.29
Small	LRS	12.43 ± 1.10	18.60 ± 5.78	11.26 ± 2.99
	HRS	27.57 ± 7.51	33.08 ± 11.75	110.69. ± 60.80
	HRS/LRS	2.21	1.78	9.82

are also characterized with a smaller standard deviation suggesting that they have the most consistent performance compared to the small devices.

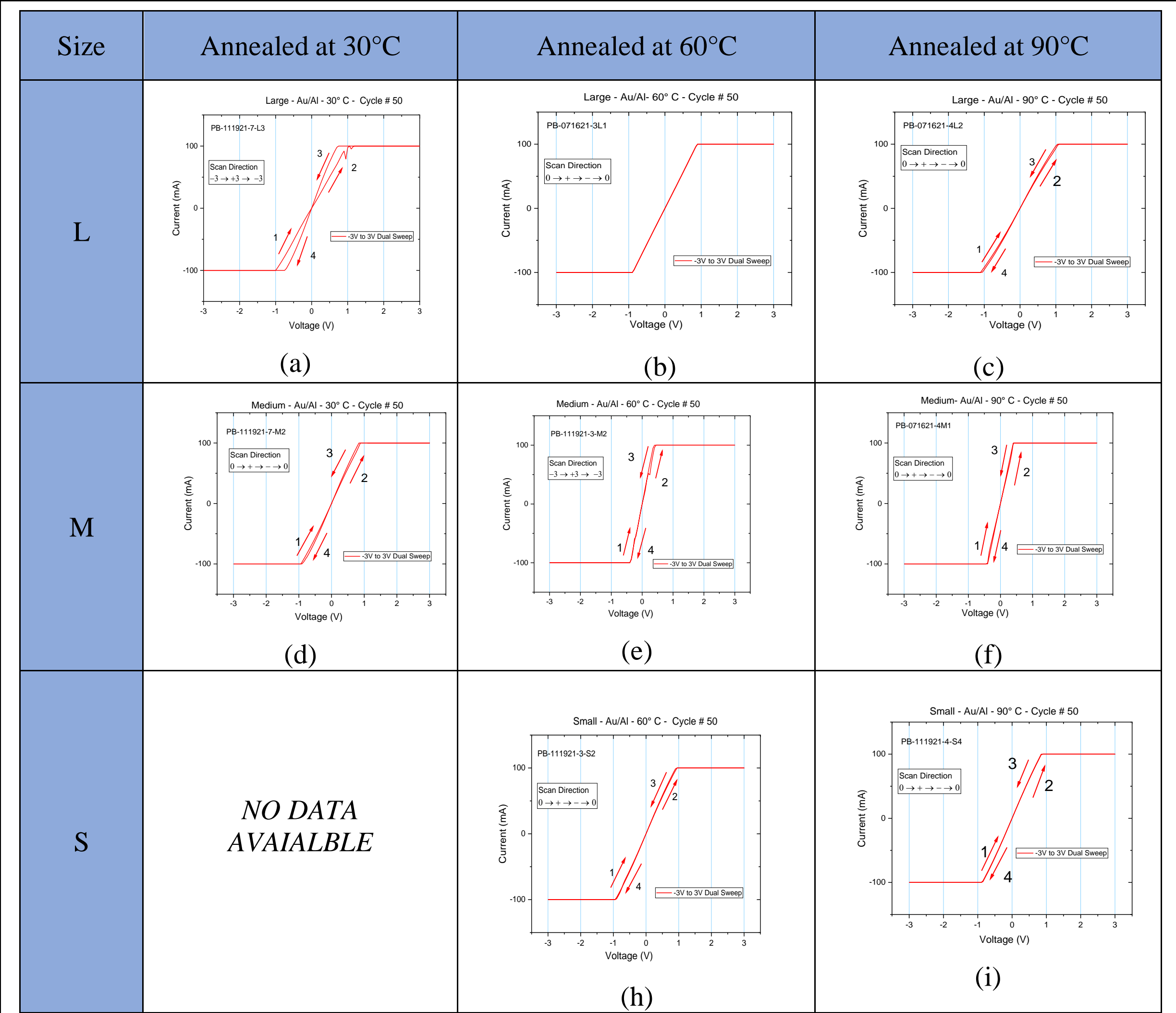
However, the clearest difference in the HRS and LRS is calculated for the small devices annealed at 90°C. The resistance at 100 mV is calculated to be 110.69 and 11.26 Ohms, hence creating a HRS/LRS ratio of 9.82. This result can be attributed to the distribution of the switching layer during the fabrication of the small devices. The higher standard deviation in the small devices also gives credence to the inconsistency of small devices. This also suggest that the Nafion thickness must be optimized for the best resistive switching performance.

4.2 Effect of Different Annealing Temperature in Au/Nafion/Al devices

In this section, we characterize different sized Au/Nafion/Al devices prepared at different annealing temperatures.

4.2.1 I-V characteristics at 30 °C, 60 °C, and 90 °C

The I-V curve for Au electrode devices was generated and plotted. The ReRAM devices with Au electrode showed very small to zero hysteresis across different sizes. The devices were annealed at 30°C, 60°C and 90°C, all showed very insignificant difference between HRS and LRS. Figure 14 shows the I-V curve of Au/Nafion/Al devices of different sizes and different annealing temperatures. All devices were tested under the -3V to +3V voltage sweep while keeping the same characterization condition. The plot below shows the graph of single cycle of Au/Nafion/Al devices produced at different annealing temperatures.



Size	Annealed at 30°C	Annealed at 60°C	Annealed at 90°C
L	Large - Au/Al - 30° C - Cycle # 50 (a)	Large - Au/Al- 60° C - Cycle # 50 (b)	Large - Au/Al - 90° C - Cycle # 50 (c)
M	Medium - Au/Al - 30° C - Cycle # 50 (d)	Medium - Au/Al - 60° C - Cycle # 50 (e)	Medium- Au/Al - 90° C - Cycle # 50 (f)
S	*NO DATA AVAIALBLE*	Small - Au/Al - 60° C - Cycle # 50 (h)	Small - Au/Al - 90° C - Cycle # 50 (i)

Figure 14: I-V curves of a single -3V to +3V voltage sweep for devices annealed at 30°C (a, d), 60°C (b, e, h), and 90°C (c, f, i).

4.2.2 Hysteresis of I-V curves for 50 cycles

All of the Au/Nafion/Al devices were put through 50 cycles of -3V to + 3V voltage sweep with a compliance current of 100 mA. Figure 15 shows the graphs for 50 cycles for devices annealed at 30°C, 60°C and 90°C. The hysteresis of these devices stayed the same across all 50 cycles. No significant improvement or degradation was observed over the 50 cycles of the voltage sweep.

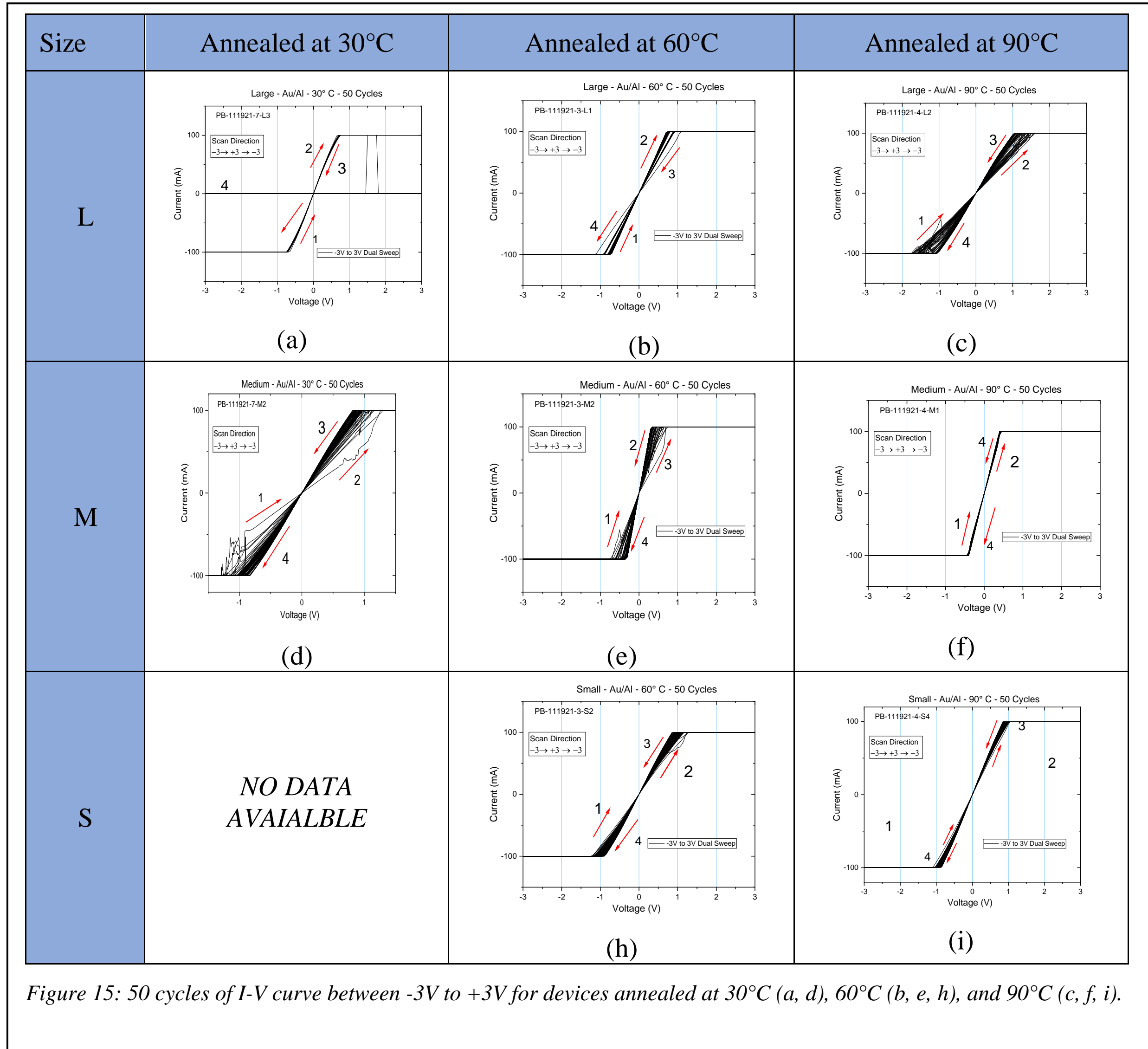


Figure 15: 50 cycles of I-V curve between -3V to +3V for devices annealed at 30°C (a, d), 60°C (b, e, h), and 90°C (c, f, i).

4.2.3 HRS and LRS changes over 50 cycles

The HRS and LRS at the reading voltage of 100 mV were calculated and plotted. The resistance obtained at both “SET” and “RESET” state was extremely close to each other. Across all the sizes and all the annealing temperature, the LRS and HRS stayed closed to each other. However, the large device annealed at 30°C (Fig. 16 (a)) showed an anomalous behavior. The HRS and LRS both were at a 10^5 factor higher than all other devices; hence this memory cell is considered

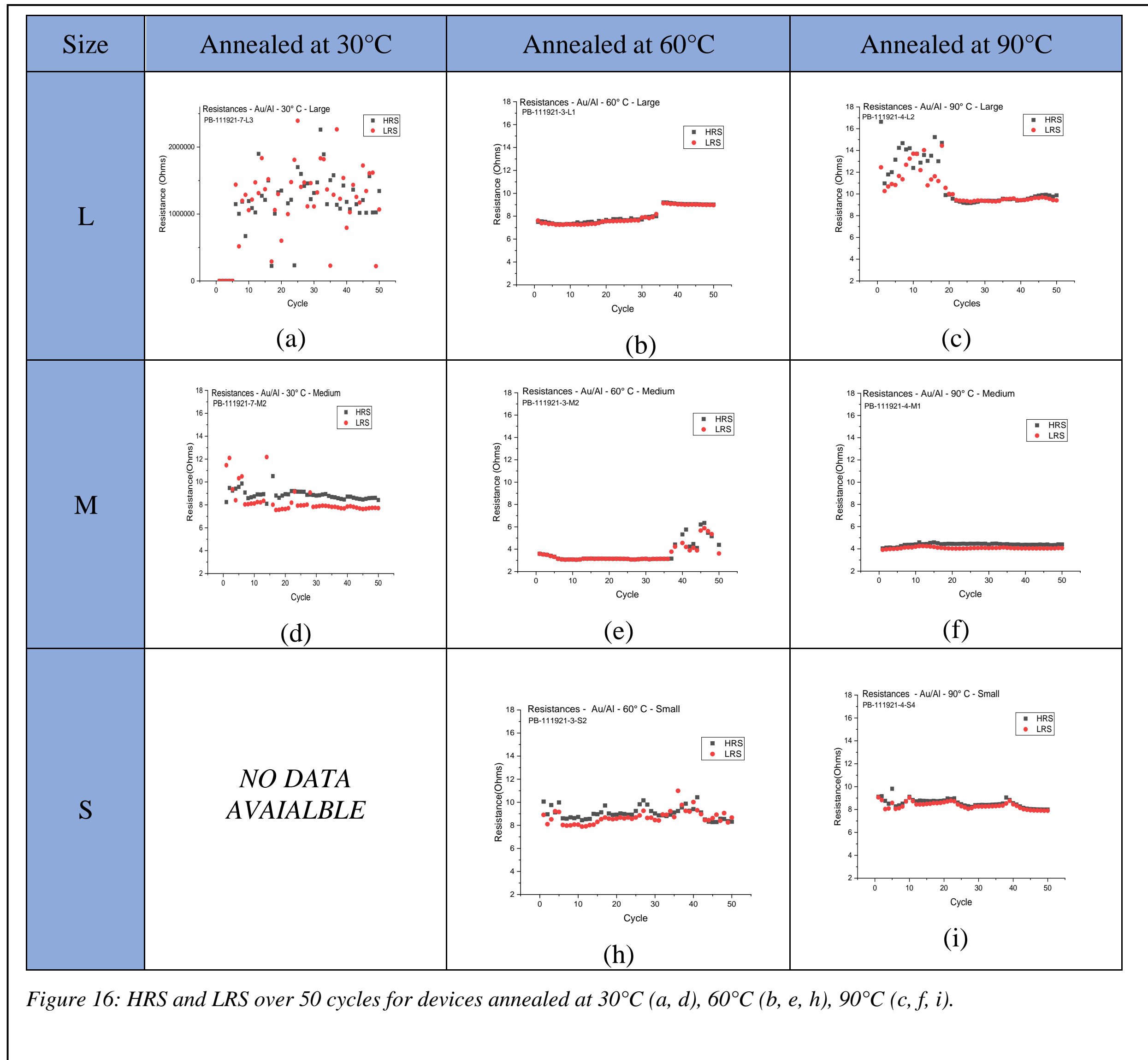


Figure 16: HRS and LRS over 50 cycles for devices annealed at 30°C (a, d), 60°C (b, e, h), 90°C (c, f, i).

to be defective. The resistance graph indicates that Au electrode devices show poor hysteresis and are highly inconsistence compared to the devices with Cu as a bottom electrode.

Table 5 shows the LRS and HRS of Au/Nafion/Al devices annealed at 30°C, 60°C and 90°C. Even though the data was centered around the mean for all the devices, the HRS and LRS were extremely close to each other. Indeed, the ratios of HRS to LRS for all devices are very close to 1. The resistance values indicate that Au electrode devices do not show any type of consistent hysteresis compared to the device with Cu.

Table 5. The average values of high and low resistive states of large, medium and small Au/Nafion/Al devices annealed at different temperatures.

Size	**Resistance (Ω)**	**30 °C**	**60 °C**	**90 °C**
Large	LRS	1130158.55 ± 513415.90	7.97 ± 0.72	10.43 ± 1.46
	HRS	1241617.11 ± 815714.83	8.03 ± 0.74	10.97 ± 2.11
	HRS/LRS	1.10	1.01	1.05
Medium	LRS	8.31 ± 0.41	3.66 ± 1.03	4.08 ± 0.07
	HRS	8.86 ± 1.12	3.69 ± 1.13	4.39 ± 0.11
	HRS/LRS	1.07	1.01	1.08
Small	LRS	*No Data*	8.69 ± 0.58	8.36 ± 0.30
	HRS	*No Data*	9.04 ± 0.53	8.56 ± 0.37
	HRS/LRS		1.04	1.02

The average HRS/LRS ratio of large Cu/Nafion/Al devices annealed at 60°C is 3.39 compared while the large Au/Nafion/Al devices have an average HRS/LRS ratio of 1.01. Similarly, the average HRS/LRS ratio of medium Cu/Nafion/Al devices annealed at 60°C is 2.32 while the medium Au/Nafion/Al have a HRS/LRS ratio of 1.01. This result suggests us that devices with Copper electrode have a distinctive HRS and LRS ratio compared to the devices with Gold electrode.

CHAPTER 5 Conclusions

The analysis of our data shows that Cu/Nafion/Al devices show a superior resistive switching property compared to the Au/Nafion/Al devices. Copper electrode devices in general exhibit a wider hysteresis. Cu/Nafion/Al devices were also found to be more consistent throughout 50 cycles of voltage sweeps. When the devices are compared for the effect of annealing temperature, the increase in temperature is seen to tend to improve the switching properties of the devices. The optimal annealing temperature of the memory devices is 60°C as they produce the largest measurable differences in HRS and LRS when Nafion is annealed at 60°C.

As discussed at the beginning, Nafion has a unique ability to change crystal structure upon exposure of the humidity. The sulfonic acid groups contained in Nafion has the capacity to form unique fringe rod like structures at appropriate temperatures [37]. Due to these rods like crystal structure, the metal ions are allowed to pass through the Nafion layer when appropriate voltage is applied.

The devices with copper as a bottom electrode exhibit better resistive switching behaviors compared to the device with gold electrodes. Copper is an electrochemically active metal and hence can form better conductive paths to create two distinct resistive states while gold does not have that ability. Due the ability of Cu electrodes to form Cu^{+} ions readily, The Cu/Nafion/Al devices can form stronger conduction filaments by the mobilization of the Copper ions [3]. Nafion is an active proton exchange [37] and when it is used with electro chemically active metals like Cu, the devices are able to form conduction channels, and hence we observe a better switching phenomenon.

Au/Nafion/Al devices have a very inconsistent performance. These devices in overall exhibit very poor switching properties. The HRS and LRS are very close to each other and often indistinguishable. This can be attributed to the characteristics of Au. Au is a passive and inert electrode, meaning that it does not involve in the facilitation of any type of conduction channel. As discussed in the beginning, because of the electrochemical nature of Au/Al pair,

Even though this research successfully demonstrated the resistive switching of Nafion, the switching performance can be further improved by optimizing the switching layer characteristics. This includes Nafion's concentration, thickness, and annealing conditions. Using the knowledge from this research, having a controlled electrode and anneal temperature with various concentrations and thickness of Nafion can be a great area of research.

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