Highly Tunable Integrated Self-Interference Cancellation Techniques for Intelligent Full-duplex Radios

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Abstract

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The growing demand for wireless connectivity in both defense and commercial applications, such as autonomous vehicles, smart cities, industrial IoT, and augmented reality (AR) / virtual reality (VR), continues to drive research towards increasing date rates in mobile transceivers while simultaneously reducing power consumption, form factor, and costs. With the advent of fifth generation (5G) and the ongoing development of sixth generation (6G) technologies, the increased utilization of the limited wireless spectrum, particularly in the S and C bands, for higher bandwidth and data rates has posed significant interference challenges among transceivers. In-band Full-duplex (FD) communication offers a solution by increasing spectral efficiency by enabling a radio's transmitter and receiver to operate simultaneously on the same channel frequency. This capability is particularly valuable for 5G/6G applications that require high data rates in congested wireless networks. However, a major challenge in FD systems is self-interference (SI), where the radio's transmitter signal interferes with its own receiver, degrading the radio's performance. This dissertation explores and implements integrated FD radio front-end solutions designed to mitigate SI and enhance data rates. The research focuses on developing SI cancellation techniques with high tunability, broad cancellation bandwidth, deep cancellation depth, and fast configuration speed. These innovations aim to enable practical radio hardware solutions for true FD operation,

addressing the challenges of wireless network congestion in 5G/6G communications.

This dissertation begins with a theoretical analysis of the design considerations for a feedfordward canceler for broadband SI cancellation, supported by circuit simulation and measurement results. A testbed including an integrated electrical balanced duplexer (EBD) coupled with a finite impulse response (FIR) filter-based feedforward canceler is used to evaluate the efficacy of the proposed design guidelines. Next, a linearity model is developed to examine the generation of nonlinearties from common- and differential-mode SI at the input of FD radio receivers, providing a strategy to minimize SI-induced distortion from nonlinear receiver impedance. These design considerations are then applied to the implementation of two FD transceiver front-end integrated circuits (ICs) featuring SI cancellation capabilities.

The first IC is a FD transceiver front-end designed to achieve broadband SI suppression, with cancelers calibrated for enhanced linearity and the ability to cancel long-delay spread SI. Fabricated in a TSMC 40 nm CMOS process, this chip integrates an EBD with a tuned impedance matching network (Z_{Bal}), two broadband complex 5-tap continuous-time FIR-based RF cancellation filters, and a mixed-signal baseband cancellation path operating with a Xilinx RFSoC to address long-delay spread (τ=+174 ns) SI. This design achieves a measured SI suppression of 62 dB across a +120 MHz bandwidth for delay spreads between 0-0.28 ns, and SI cancellation of 23 dB across +120 MHz bandwidth for delay spreads between 0.4-174 ns. The RF canceler, calibrated using digitally-controlled current DACs, demonstrates a maximum input-referred third-order intercept point (IIP_3) of +42 dBm. The receiver has a measured noise figure of 6.8 dB and an IIP_3 of -21 dBm at the maximum gain setting of 40 dB. Additionally, an integrated harmonic-rejection power amplifier (PA) achieves a measured maximum output power (P_{Sat}) of 19.1 dBm and power-added efficiency (PAE) of 27%.

The second IC demonstrates a highly tunable SI canceler augmented with a machine-learning-based adaptation loop for deep cancellation, enhanced linearity, and accelerated

convergence time. This prototype 2.4 GHz canceler chip, fabricated in a 40 nm CMOS process, features extensive tuning capabilities in filter coefficients, delay spread, and linearity. It operates in concert with a neural network (NN) algorithm implemented on a Xilinx RFSoC evaluation kit to optimize the canceler's adaptation process. Designed as a discrete add-on, this canceler IC can be integrated with transceiver chips from different manufacturers. The chip, implemented as a 6-complex tap finite impulse response filter, achieves a measured maximum SI cancellation of 32 dB over a 40 MHz bandwidth and an IIP_3 of +38 dBm. The proposed NN computes the initial settings for the canceler, followed by a local optimization process, achieving a convergence time of about 10 miliseconds in real-world wireless environments.

The combined techniques proposed in this dissertation, focusing on enhancing tunability of SI cancellation, demonstrate a potential to achieve deeper cancellation depth, broader cancellation bandwidth, higher canceler linearity, and faster adaptation convergence for FD radios. These advancements enable new opportunities to increase wireless network capacity, addressing the growing demands of future 6G applications.

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Chapter 1

INTRODUCTION

Over the past decades, wireless communication systems have seen a significant increase in data rates, driven by the growing demand for applications such as Wi-Fi, cellular networks, and the Internet of Things (IoT) devices. Currently, both cellular and Wi-Fi technologies achieve data rates of up to 5 Gbps [1]. As fifth- and sixth-generation (5G/6G) networks continue to evolve, the demand for even higher data rates and lower latency will become increasingly critical to support emerging data-intensive applications, including autonomous vehicles, immersive virtual reality (VR) / augmented reality (AR) devices, and distributed edge computing. According to [1], as illustrated in Fig.1.1, 6G communication systems are expected to achieve data rates to 200 Gbps for cellular networks and 10 Gbps for Wi-Fi, with end-to-end latency below 1 ms by 2030. These developments will be crucial for enabling evolutionary technologies such as ultra-responsive industrial automation and smart city infrastructure, redefining the capabilities of wireless connectivity.

Despite the rapid growth of wireless communications, the available radio spectrum remains a finite and highly valuable resource, with limited allocation for specific applications and users. In the United States, the frequency range (FR) 1 (1–7 GHz), which provides an optimal balance between propagation characteristics and available bandwidth, has an estimated total acquisition value exceeding 1.5 trillion US dollars, based on the 2021 auction of 300 MHz spectrum at 3.8 GHz [2]. As the number of devices operating within this spectrum continues to grow with the expansion of 5G and the emergence of 6G technologies, the potential for interference among these devices also increases. While 5G and 6G systems have introduced new opportunities in the millimeter-wave (mm-Wave) frequency range (FR2, above 24 GHz) [3], providing wider bandwidths, these systems are constrained by high

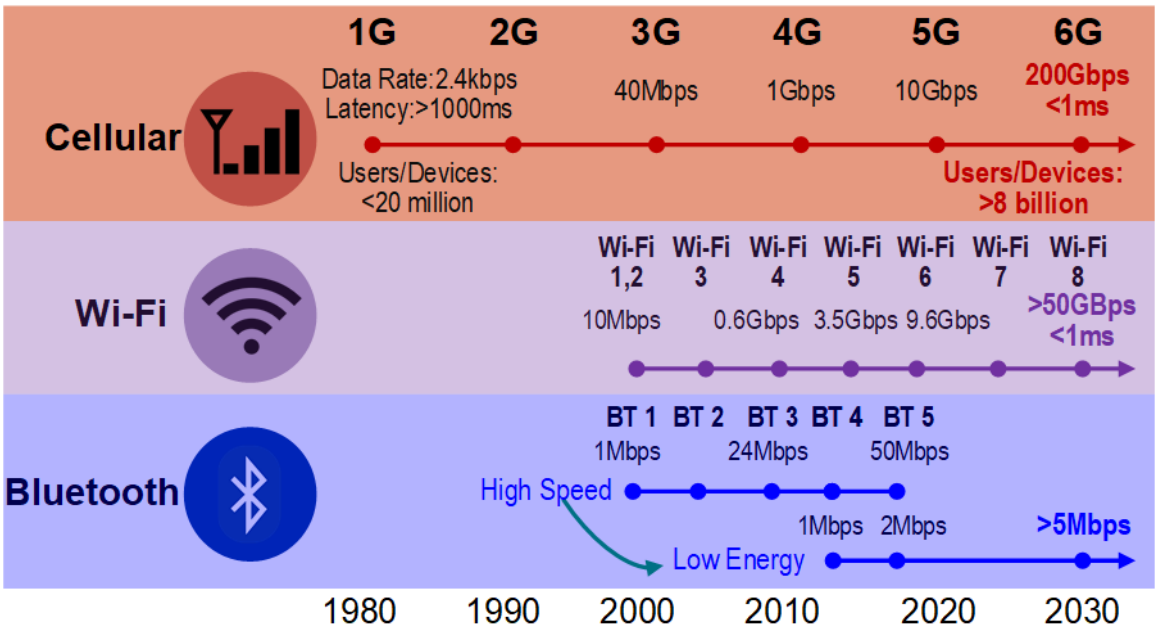


Figure 1.1: Increased wireless data rates and reduced latency over the past few decades for cellular, Wi-Fi, and Bluetooth systems.

free-space path loss and susceptibility to blockage from obstacles. Additionally, commercial factors such as infrastructure costs and network compatibility often lead wireless providers to prioritize deployments within the FR1 spectrum [4].

To address FR1 spectrum congestion and improve spectral efficiency, more effective spectrum-sharing techniques among different users and applications are needed. One potential approach is in-band full-duplex (FD) communication (see Fig.1.2), which allows simultaneous transmission and reception of data on the same carrier frequency — unlike traditional frequency-division duplex (FDD) systems that use separate frequencies to wirelessly transmit and receive. By allowing both transmitting and receiving on the same channel, FD communication increases spectral efficiency and helps meet the growing demand for higher data rates in congested wireless networks [5–7], effectively increasing the value of the available spectrum. However, implementing practical FD radios presents two major challenges.

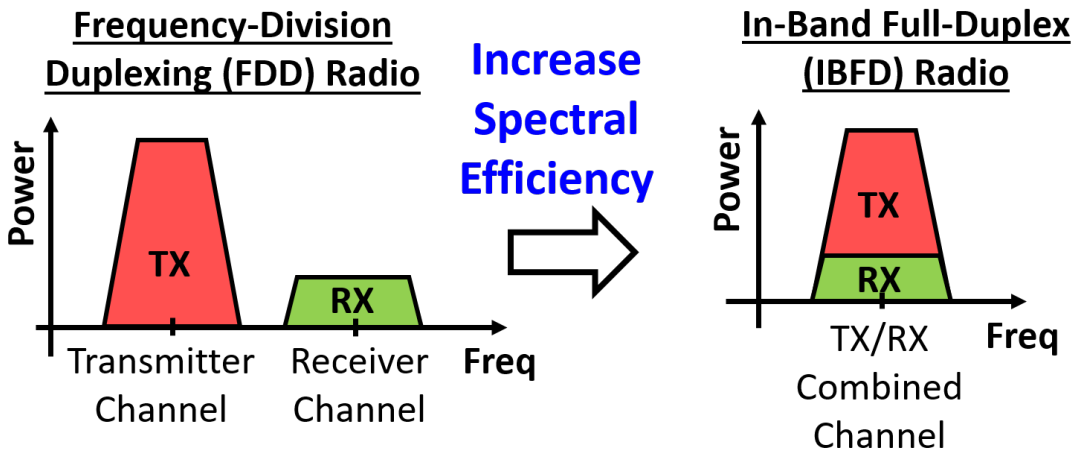


Figure 1.2: Comparison of full-duplex wireless communication with conventional frequency-division duplexing communication.

First, self-interference (SI) originating from a radio transmitter poses a significant challenge in FD radio systems, as it can saturate the receiver (RX)front-end and degrade its sensitivity, particularly when the transmitter (TX) delivers a high-output power signal. The significant power difference between the maximum TX output signal and the minimum RX sensitivity, combined with the fact that both TX and RX operate on the same frequency in FD radios, makes SI mitigation one of the most critical challenges in implementing FD radio systems. For example, in Wi-Fi 802.11ax [8], the TX output power is typically more than 100,000 times higher than the RX sensitivity, necessitating a collection of techniques to effectively suppress SI and enable FD operations.

Second, the time-varying nature of SI requires numerous tuning parameters and rapid adjustments to achieve optimized radio performance. In real-world wireless environments, SI characteristics and frequency response can frequently vary due to factors such as movements of nearby and distant objects, changes in antenna positions, and user interactions with antennas. Therefore, rapid adaptation of FD radios is crucial to achieve optimal SI mitigation performance. Longer tuning processes will increase communication latency, reducing the data

rates and spectral efficiency improvements promised by FD radios.

1.1 Research Objectives and Applications

The objective of this research is to develop and implement integrated solutions at both the system and circuit levels to mitigate self-interference in in-band FD radios. The dissertation focuses on two key aspects:

- Design and implementation of a highly tunable FD radio front-end chip with enhanced SI cancellation: This research explores the architecture and circuit design of an integrated SI cancellation network optimized for deep and broadband SI suppression by optimizing and extending any tuning vector. Key performance metrics such as cancellation depth, bandwidth, linearity, and delay spread are analyzed and optimized. The ultimate goal is to implement an FD radio front-end with an enhanced tuning range, capable of mitigating SI with various amplitude and delay profiles in diverse environments.

- Artificial intelligence (AI) - augmented SI cancellation for rapid adaptation: This work explores the utilization of AI algorithms with a highly tunable RF SI canceler chip to accelerate adaptation at an FD radio front-end. The focus is on developing intelligent parameter tuning strategies that minimize convergence time while optimizing SI cancellation performance, addressing the key challenge of dynamic SI in practical FD radio systems.

The proposed prototype chips are implemented using Taiwan Semiconductor Manufacturing Company's (TSMC) 40 nm CMOS process, which offers advantages such as lower cost, compact size, and the ability to integrate high-density digital circuits with the radio front-end on a single chip – an advantage over bulky discrete RF component solutions. While this research focuses on CMOS implementation, the proposed system and circuits can also be applied to other semiconductor technologies, such as SOI and bipolar processes. The solutions developed in this dissertation to enable FD radios can function as standalone systems

or complement other techniques to enhance wireless data rates and improve connectivity, such as MIMO and mm-Wave transceivers in both FD and FDD systems. Additionally, the approach of using AI algorithms to rapidly adapt an SI canceler can be extended to optimize other wireless radio performance metrics, including mitigating broadband interference, optimizing noise figure and linearity, and dynamically adjusting bandwidth and operation frequency, to support emerging applications that require extremely low latency and high programmability. These efforts can play a critical role in next-generation wireless systems by enabling more adaptive and high-performance transceivers.

Beyond wireless radios, the proposed SI mitigation techniques can benefit broad applications, including quantum controllers, [9, 10], DOCSIS 3.1 cable modems [11], and neural interfaces [12–14]. For example, the integrated circulator proposed in this dissertation (Chapter 5) could help isolate qubit readout circuits from transmitted signals [15], improving the fidelity and robustness of qubit state measurements (Chapter 7). Additionally, the introduced SI mitigation techniques can help enable simultaneous bidirectoional signaling in high-speed wireline communications, reducing form factor while increasing data rates per pin [16, 17]. More broadly, these techniques introduced in this dissertation are crucial for many simultaneous transmit and receive (STAR) systems, as they effectively mitigate strong SI and enhance receiver sensitivity.

1.2 Overview and Organization of the Dissertation

The rest of this dissertation is organized as follows:

Chapter 2: This chapter provides an overview of SI mitigation architectures used in FD radios and discusses key technical challenges with the implementation of integrated circuit solutions for SI mitigation. The chapter also reviews state-of-the art SI mitigation techniques, including both circuit implementations and adaptation algorithms.

Chapter 3: This chapter analyzes design considerations of feed-forward cancelers implemented as finite impulse response (FIR) filters for broadband SI cancellation. The design space and parameters of analog FIR filters are examined mathematically and verified through

circuit simulation and measurements. The outcome of this study provides design guidelines for SI cancellation using analog/RF FIR filters.

Chapter 4: The generation of nonlinearities from both the common- and differential mode TX-SI at the FD receiver input is explored and modeled. An often overlooked differential nonlinear component arising from SI modulating the nonlinear receiver input impedance is systematically studied and validated through simulations. This chapter concludes with strategies to enhance FD receiver linearity by suppressing SI common-mode leakage.

Chapter 5: A 2.4 GHz FD transceiver incorporating multiple SI suppression techniques for future wideband wireless communication is presented. The proposed FD radio features broadband SI suppression, cancelers optimized for enhanced linearity, and ability to cancel long-delay spread SI. A prototype chip, fabricated in a TSMC's 40 nm CMOS process, works with a Xilinx RFSoC evaluation kit to complete the adaptation loop for the radio analog front-end. This work demonstrates a measured SI suppression of 62 dB over a +120 MHz bandwidth for delay spreads between 0-0.28 ns, and SI cancellation of 23 dB over a +120 MHz bandwidth for delay spreads between 0.4-174 ns.

Chapter 6: This chapter presents an RF SI canceler chip with an enhanced tuning range. A custom-developed optimization algorithm leveraging machine learning techniques is implemented on an FPGA to adapt cancellation with accelerated speed. A prototype 2.4 GHz canceler chip, fabricated in a 40 nm CMOS process, achieves a measured maximum SI cancellation of 32 dB over a 40 MHz bandwidth. The canceler chip is adapted using a neural network (NN) - assisted gradient descent algorithm implemented on a Xilinx RFSoC, achieving a convergence time within 10 milliseconds in real-world wireless environments.

Chapter 7: This chapter summarizes the dissertation and discusses further work and applications. Additionally, it explores the possibilities to extend SI mitigation techniques in FD radios to qubit readout channels that is a critical step in the development of quantum computers.

Chapter 2

SELF-INTERFERENCE MITIGATION TECHNIQUES IN FD RADIOS

In-band FD radio is one promising solution to address the issue of congested wireless network capacity by combining the transmitter and receiver channels into a single frequency band. However, the radio transmitted signal becomes interference to its own receiver during simultaneous transmitting and receiving. The worst-case scenario occurs when the transmitter operates at maximum output power (sometimes more than +20 dBm in Wi-Fi systems [8]), while the receiver attempts to receive the desired signal at its lowest sensitivity (typically below -80 dBm). To minimize the desensitization of the receiver in FD radios, SI mitigation must exceed 100 dB, often demanding multiple SI suppression paths.

2.1 SI Mitigation Architecture

SI can be mitigated at various locations within a radio transceiver to achieve effective SI cancellation. Fig.2.1a-2.1d show multiple possible feedforward cancellation (FFC) paths within a FD transceiver chain, each with distinct purposes and different design considerations. One critical SI suppression path in FD radios is between the TX power amplifier (PA) output and the RX low noise amplifier (LNA) input (Fig.2.1a) [18–30]. This RF canceler path captures all noise and distortion from the PA while suppressing strong SI before it reaches the LNA input, preventing RX saturation and relaxing linearity requirements of the LNA and subsequent receiver blocks. However, the RF canceler in this path has the strictest noise and linearity requirements among all cancellation paths. Any noise or distortion introduced at the canceler output directly contributes to the RX noise floor, degrading receiver sensitivity. Additionally, a single RF canceler path is often insufficient to achieve more than 100 dB of

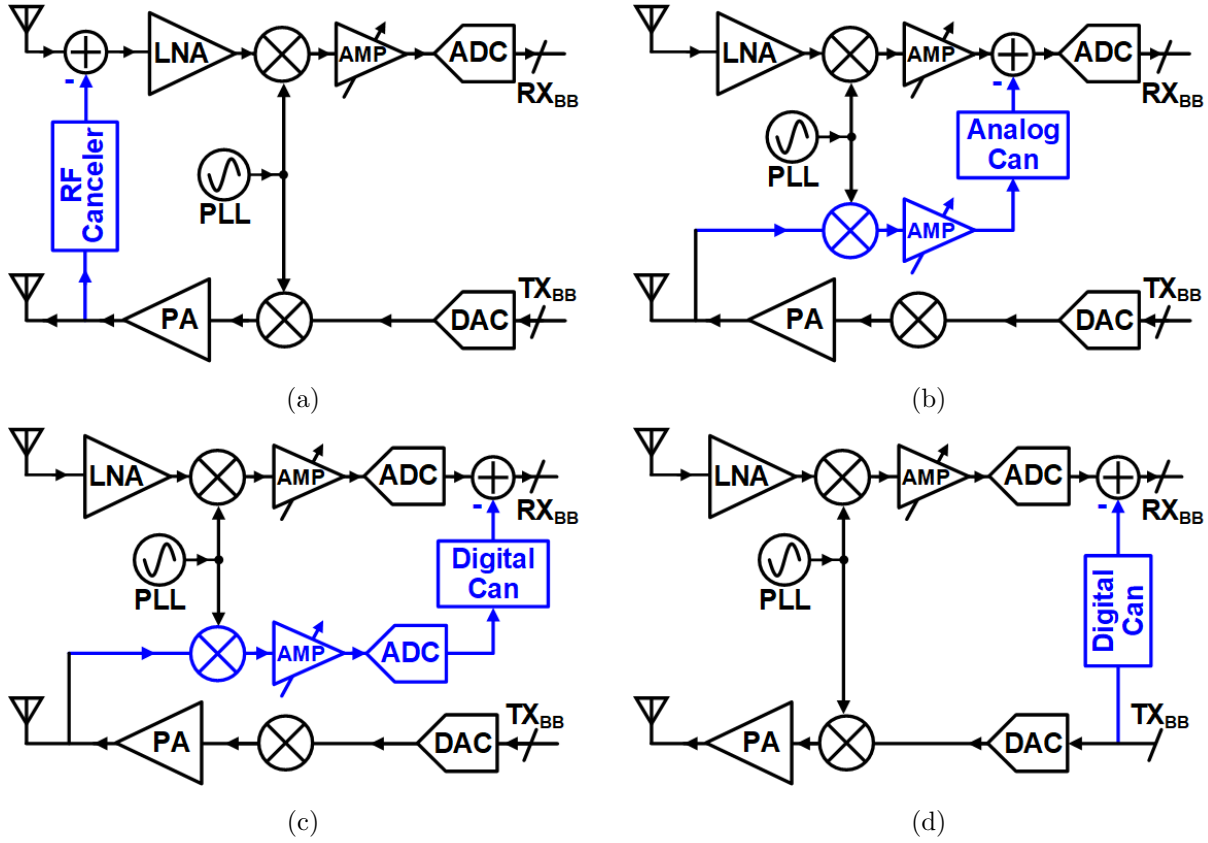


Figure 2.1: Various SI mitigation paths in FD radios: (a) TX output to RX input, (b) TX output to RX analog baseband, (c) TX output to RX digital baseband, (d) TX digital baseband to RX digital baseband.

SI suppression due to noise performance and power consumption constraint.

Another widely used SI cancellation path begins from the PA output to the RX analog baseband (Fig.2.1b) [20, 23, 24, 29] or digital baseband (Fig.2.1c) [18, 30]. These baseband cancelers provide additional SI suppression after the downconversion mixer, where the RX noise floor is raised by the LNA. Therefore, the noise and linearity requirements of the baseband cancelers are relaxed. Additionally, operating at lower frequencies allows baseband cancelers to generate longer delay spreads [31], enabling them to mitigate SI from environmental reflections with larger delay spreads. However, reciprocal mixing between the SI and

local oscillator (LO) phase noise before baseband cancellation introduces additional in-band interference, which limits the achievable SI cancellation depth of this path [32].

A cancellation path from the TX digital baseband to the RX chain is shown in Fig.2.1d. Since this canceler is implemented in the digital domain, various digital signal processing (DSP) algorithms can be employed [33–36]. This method leverages the high programmability of digital circuits to enhance SI suppression. However, when designing SI mitigation circuits, several critical considerations extend beyond maximizing SI cancellation:

- Minimal impact on transceiver input and output interfaces: The SI canceler should introduce negligible loading to the TX and RX chain to minimize insertion losses.

- Low noise and distortion: Any additional noise or distortion introduced into the receiver signal path must be minimized.

- Minimal area and power consumption: The canceler circuit should occupy minimal silicon area and consume minimal power.

- High flexibility and tunability: A wide tuning range is crucial for canceler circuits to support various radio operation modes in dynamic wireless environments.

In practice, FD radios often require a combination of multiple suppression paths, each serving a distinct purpose. To prevent RX saturation and relax receiver linearity requirements, SI mitigation must occur as close to the RX input as possible. Consequently, SI suppression circuits positioned between the PA output and the RX/LNA input are the most critical, and their suppression capability must be maximized. However, these must be complemented by additional canceler paths to further mitigate residual SI, achieving minimal overall desensitization of the receiver. This dissertation explores an integrated SI mitigation architecture to address key implementation challenges (discussed in the next section) in FD radios.

2.2 Integrated SI Mitigation Circuits Implementation Challenges

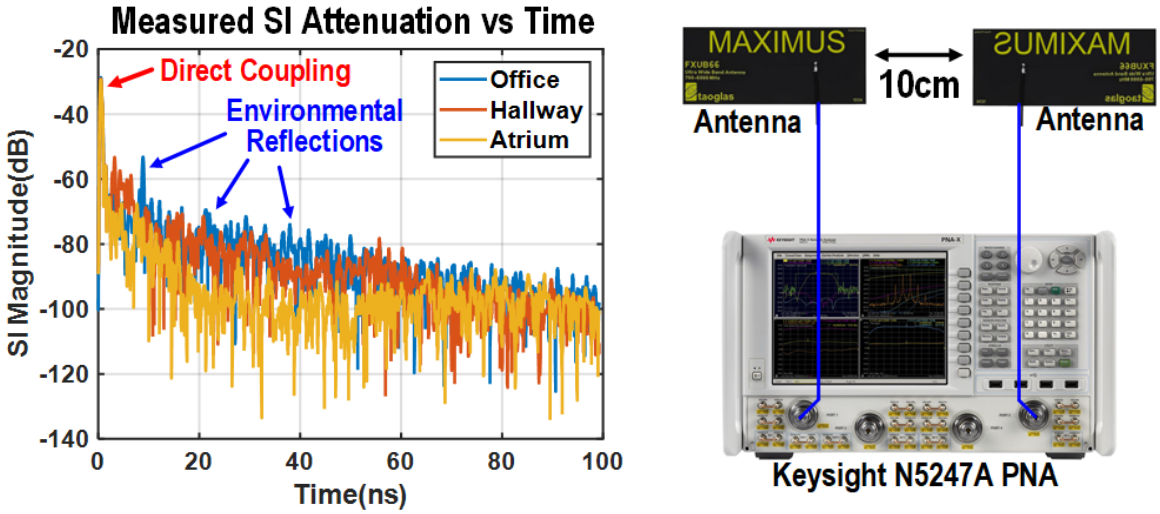
While in-band FD radios show a potential to improve spectral efficiency and data rates, effectively mitigating SI with integrated solutions remains a significant challenge. Despite efforts of using various cancellation paths discussed in the previous section, key technical challenges remain in implementing integrated SI suppression technologies.

2.2.1 Multi-path Self-Interference Suppression

One of the primary challenges in implementing an FD transceiver is addressing multiple TX-SI reflection paths varying delay spreads. TX-SI consists of a combination of direct TX-to-RX coupling and environmental reflections caused by SI bouncing off nearby and distant objects. Fig.2.2a shows measured SI amplitude as a function of delay spread, obtained using two broadband antennas placed 10 cm apart and a network analyzer (Fig.2.2b). Measurements were performed in three commonly found indoor environments: a hallway, an office, and an atrium. The strongest SI peaks observed in different environments originate from direct coupling between the two antennas. Subsequently, the received SI power rapidly decreases as the delay increases due to path loss. However, several SI peaks with longer delay spreads, as shown in Fig.2.2a, are associated with environmental reflections. These SI reflections can degrade RX sensitivity for durations exceeding 100 ns, depending on the TX output power. Therefore, a collection of SI mitigation techniques is necessary to address SI components across a wide range of delay spreads and power levels in FD radios.

2.2.2 Dynamic Self-Interference Cancellation

Since SI in FD radios originates from multiple environmental reflection paths, its frequency response, including amplitude, phase, and delay spread, varies over time due to factors such as transceiver motions and changes in the surrounding environment. Therefore, SI mitigation circuits within FD radio front-ends must have a highly tunable frequency response to adapt to these variations to maintain effective SI cancellation across key performance metrics,



(a) (b)

Figure 2.2: (a) SI-delay profile measured with two antennas in various indoor environments. (b) Antennas and network analyzer used for SI-delay profile measurement.

such as cancellation depth and bandwidth. Additionally, rapid tuning of the canceler's parameters is critical due to the dynamic nature of SI, since slow adaptation processes can disrupt normal RX operations, reducing data rates and increasing communication latency. For example, in Wi-Fi hotspot applications, the wireless channel typically changes every 60 ms [37], requiring SI cancelers to adapt at similar intervals and converge well within 60 ms to ensure optimal performance. Therefore, enabling practical FD operation requires a highly tunable SI canceler with rapid adaptation capabilities.

2.2.3 Demand for Highly Linear Integrated SI Canceler

Emerging wireless systems in 5G/6G and military applications, such as long-range communication and industrial IoT, utilize higher transmitted output power than many current wireless radios. For example, for example, ilitary transmitters can easily exceed +40 dBm output power [38]. SI mitigation circuits that sense signals directly from the PA output

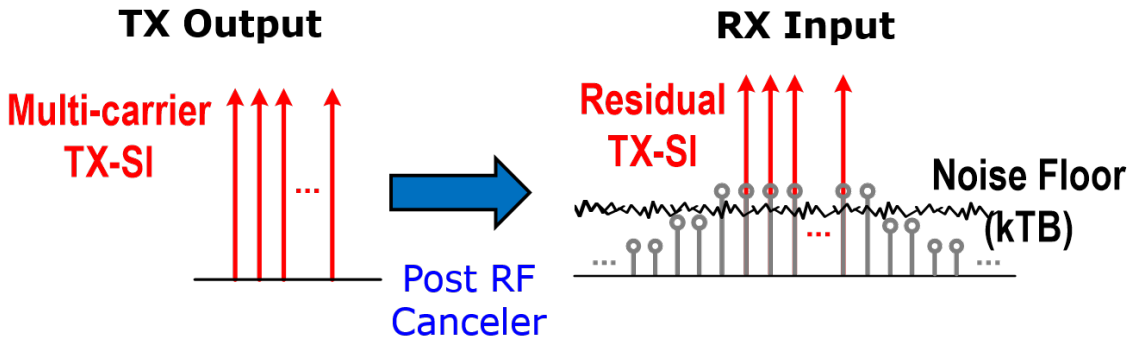


Figure 2.3: Intermodulation distortion generated at the RX input after the PA reference signal with OFDM modulation passes through the RF canceler (shown in Fig.2.1a).

must be capable of handling the large voltage swings from the PA output. While traditional circuits built upon discrete components using bipolar processes can sustain a voltage swing larger than 20 V [38], achieving this in integrated solutions is challenging due to the lower breakdown voltage of modern CMOS technologies, which prioritize power efficiency. Moreover, many modern wireless systems widely use orthogonal frequency-division multiplexing (OFDM) modulations. As the PA reference signal passes through the SI cancelers, OFDM subcarriers generate intermodulation distortion products (Fig.2.3), placing further demands on canceler's linearity. For example, in a Wi-Fi transceiver, consider a canceler between the PA output and the RX/LNA input. If the PA transmits a two-tone signal (10 dBm for each tone) and the RX has an input-referred noise floor of -85 dBm with a 6 dB margin, the third-order intermodulation (IM_3) products at the canceler out need to be below -91 dBm. With a canceler gain of -35 dB, the required input-referred third-order intercept point (IIP_3) for the canceler is calculated as:

$$IIP_3 = P_{TX} + \frac{P_{TX} + G_{Can} - IM_3}{2} = 43dBm \tag{2.1}$$

This requirement highlights the need for highly linear cancelers, particularly for RF cancelers (Fig.2.1a) to handle high-power multi-carrier modulation signals in 5G/6G and military

applications.

2.2.4 Broad Bandwidth SI Cancellation

Another major challenge in implementing SI mitigation circuits is the constant demand for broader bandwidth in evolving 5G/6G communications. For instance, the recently released Wi-Fi 7 (IEEE 802.11be) supports a maximum channel bandwidth of 320 MHz, which is eight times larger than that of IEEE 802.11n [8]. Both the channel bandwidth and data rates are expected to double in future Wi-Fi 8 systems [39], necessitating a proportional increase in SI suppression bandwidth for FD radios. However, variations in the SI frequency response, including amplitude and group delay, pose challenges in designing SI cancelers capable of achieving broadband suppression. To address the variations of SI frequency response within channel bandwidth, the canceler must provided higher tuning flexibility and a wider tuning range, which are particularly challenging to achieve in integrated RF/analog front-end solutions [27].

2.3 State-of-the-art Integrated SI Cancellation Techniques

Given the challenges described in the previous sections, numerous efforts have been made to investigate integrated techniques for mitigating SI. This section reviews state-of-the-art integrated SI cancellation techniques, with a primary focus on their tuning capabilities and adaptation algorithms. SI mitigation in FD radios typically begins at the radio antenna-air interface to provide initial SI attenuation to prevent receiver saturation. Common integrated solutions for antenna-air interface SI mitigation include integrated CMOS circulator [40–45], electrical balanced duplexers (EBD) [46–48], and directional couplers [49, 50]. Additional SI suppression is typically achieved through feedforward cancellation (FFC) paths, which are generally implemented using two types of cancelers: (1) Frequency-domain cancelers which create a tunable bandpass filter frequency response and (2) Time-domain cancelers that use multiple time-delayed paths with tunable amplitudes.

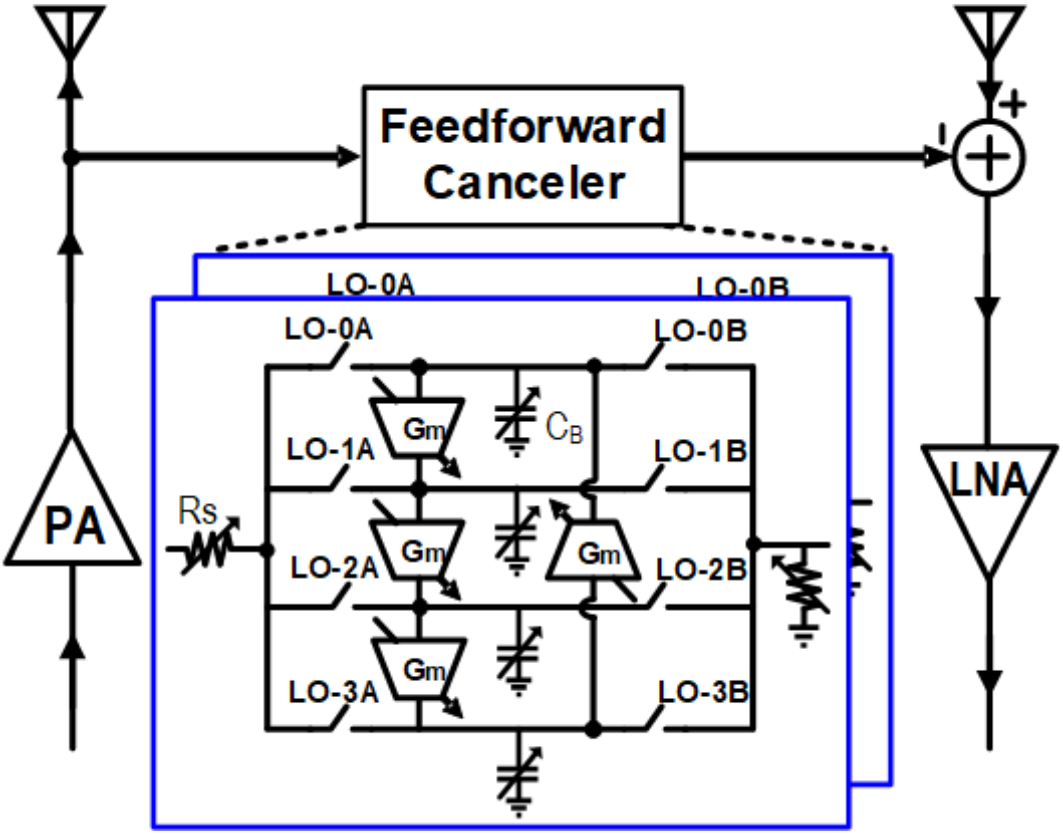


Figure 2.4: Frequency-domain cancelers implemented using parallel G_m-C based N-path filters [28].

2.3.1 Frequency-Domain SI Canceler

In [28], parallel G_m-C based N-path filters with a tunable band-pass frequency response were utilized to cancel residual SI prior to the RX/LNA input (Fig.2.4). Each filter path features four independent tuning parameter: gain, phase, center frequency, and bandwidth. For example, the gain of each filter is tuned by adjusting the resistance of R_s, while the phase and bandwidth are controlled by varying the capacitance of C_B. The combined frequency response of the canceler was tuned to achieve 20 dB of cancellation across a 25 MHz bandwidth at 1.37 GHz. However, the tuning range of each parameter is limited, with the gain tuning range being less than 20 dB. The resolution of tuning elements, such as the resistive ladder (R_s)

and LO phase differences, is sensitive to parasitics at higher carrier frequencies. Additionally, the use of G_m stages in the N-path filters degrades the canceler linearity, increases noise and power consumption.

Frequency-domain cancelers can alternatively be implemented as vector modulators using either active [19, 25] or passive components [22, 30, 51], allowing independent control of gain and phase to match the SI. However, since a vector modulator has only two independent tuning variables (gain and phase), it can match the SI frequency response over a relatively narrow bandwidth (typically less than 15 MHz), which is generally insufficient for wideband radio applications.

2.3.2 Time-Domain SI Canceler

Since the SI signal coupled through the antenna-air interface consists of multiple time-delayed paths (Fig.2.2a), SI cancelers can often be implemented in the time domain as multi-tap true-time-delay filters for SI cancellation. The amplitude of each filter tap can be controlled using digitally controlled trans-conductance (G_m) stages, which offer higher resolution and a broader tuning range than the frequency-domain canceler in [28] due to their larger bandwidth.

True-time delay can be realized using either discrete-time or continuous-time circuits. For example, finite-impulse response (FIR) filter-based SI cancelers using switched-capacitor circuits have been demonstrated in [23, 24] (Fig.2.5), achieving true-time delays of up to 7.75 ns at RF ($f_{Carrier}$=1 GHz) and 75 ns at analog baseband (f_{BB}=34 MHz). However, the maximum achievable delay spread in these designs is limited by the clocking period of the switched-capacitor circuits, while the circuit bandwidth is proportional to the clock frequency. This creates a trade-off between bandwidth and maximum delay, making this approach challenging to scale with increasing carrier frequencies. Additionally, this approach lacks independent phase tuning for RF cancelers [24] due to potential loading effects of polyphase filters (PPF) on the switched–capacitor circuits.

The implementation of delay lines in FIR filter-based SI cancelers within the continuous-

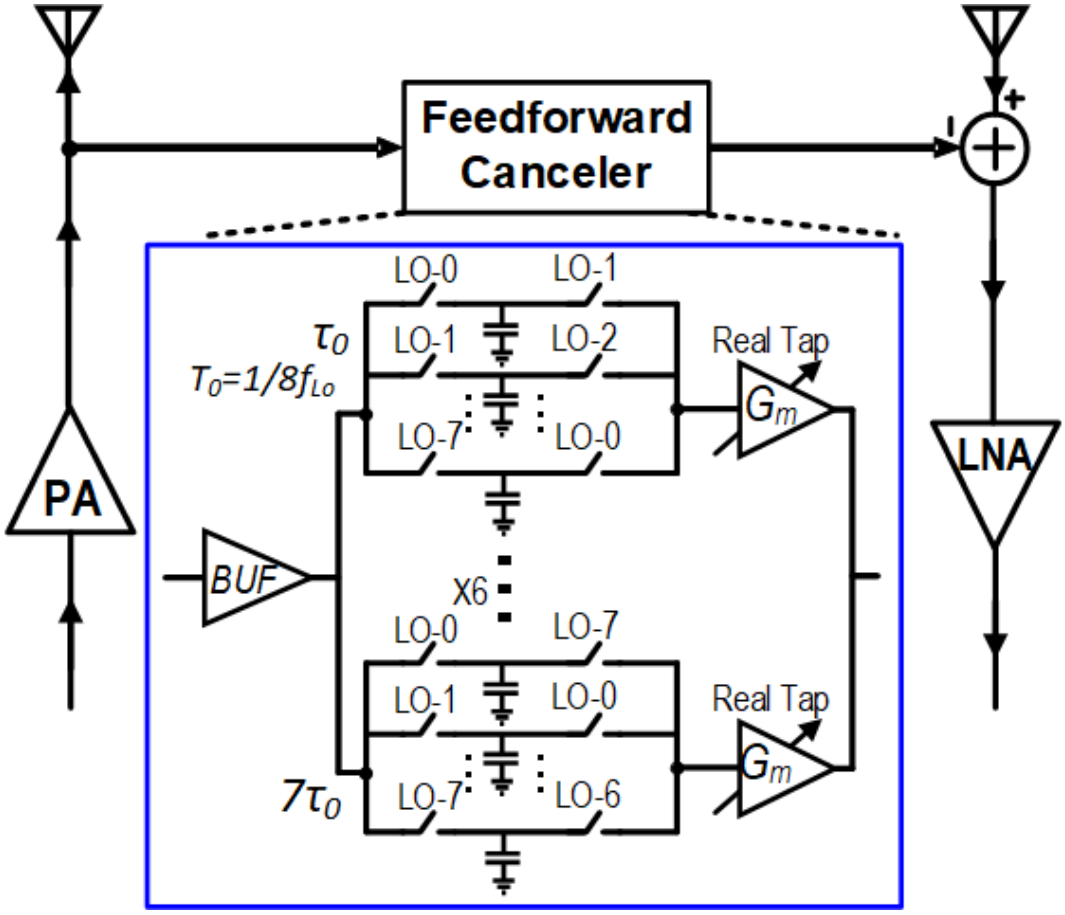


Figure 2.5: Schematic diagram of time-domain cancelers using switched-capacitor circuits [24].

time domain involves various circuit configurations, such as RC-CR all-pass filters (APF) [20, 21], LC circuits [52], and G_m-C APFs [20]. For example, the RF FFC in [21] (Fig.2.6) achieves a delay spread of about 0.2 ns. While the delay is smaller than the delay spread achievable with the switched-capacitor circuits in [24], continuous-time implementations offer significantly higher linearity due to the use of purely passive components in the delay line. Additionally, these methods typically occupy considerably less area (approximately 0.26 mm^2 for the RF canceler in [20] compared to about 1.6 mm^2 for the switched-capacitor-based canceler in [24]).

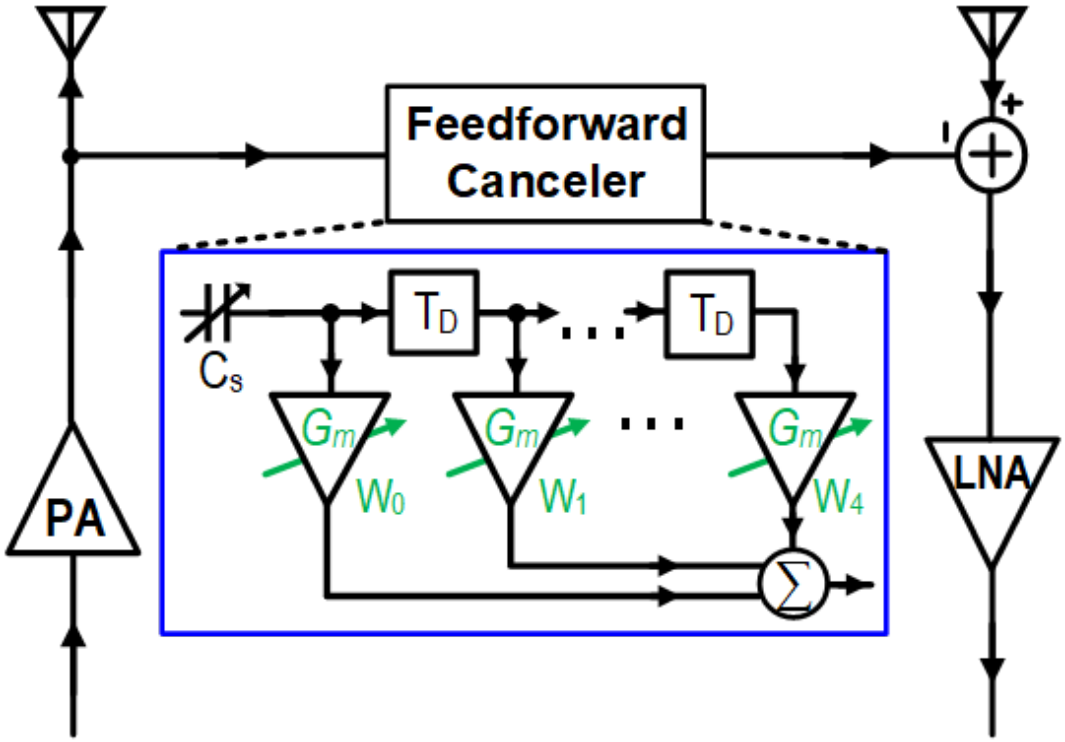


Figure 2.6: Schematic diagram of FIR filters in the continuous-time domain [20, 21].

True-time delay spreads have also been generated at lower frequencies using continuous-time RC low-pass filters (LPF) [26, 27, 29], which are then up-converted to the RF carrier frequency within RF cancelers (Fig.2.7). These methods provide independent tuning capabilities for filter tap delay, gain, and phase. While operating at lower frequencies allow longer delay spreads, these methods typically have fewer delay taps and limited delay spread coverage. Therefore, their SI cancellation performance may degrade when SI delay spread varies significantly in wireless environments. Additionally, the up-conversion mixer in RF cancelers introduces folded noise and image components during frequency conversion, which can degrade both SI cancellation and RX noise performance.

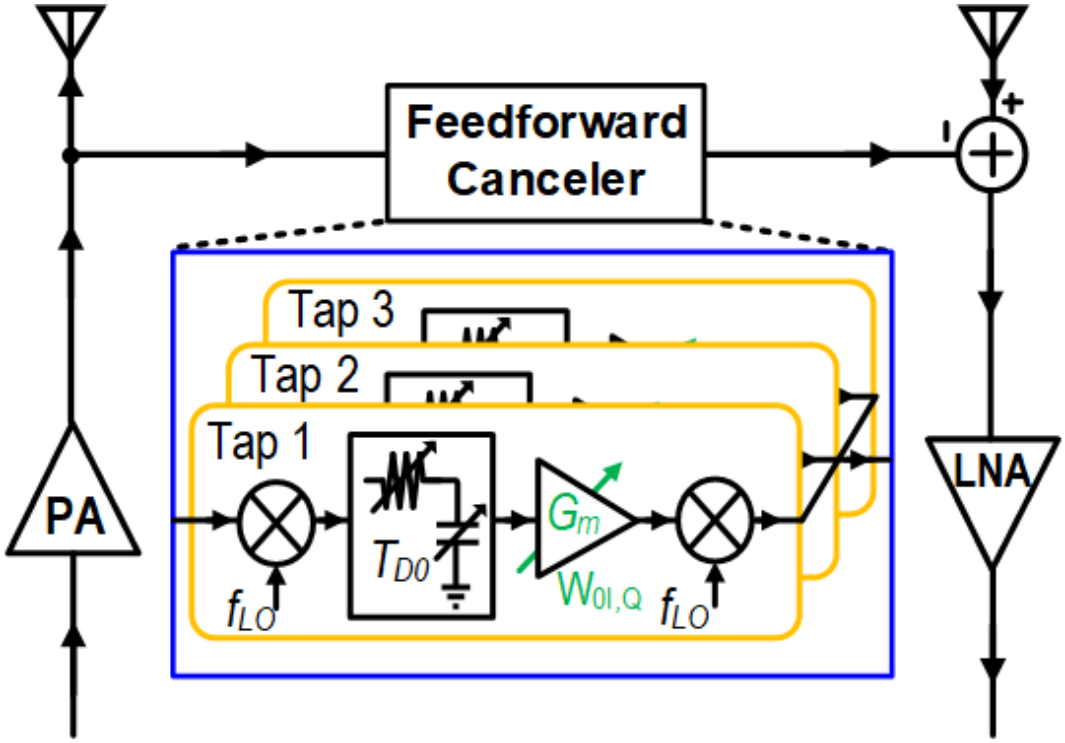


Figure 2.7: Schematic diagram of time-domain RF SI cancelers with delay generated at baseband [26, 27, 29].

2.3.3 Adaptation of SI Cancelers

Due to the time-varying nature of SI in diverse environments, the tuning parameters of SI cancelers, including gain, phase, and delay, must be frequently adapted to achieve optimal cancellation performance. Various strategies have been explored for adapting RF and analog cancelers. For instance, SI cancelers implemented with discrete RF components have demonstrated rapid adaptation times when using the least mean square (LMS) algorithm [53, 54]. However, this approach typically requires converting each RF filter tap output to the digital domain, which typically requires high-speed and power-hungry mixed-signal circuits. While analog LMS loops, as discussed in [55, 56], eliminate this need, the inherent distortion and noise of the adaptation circuitry can degrade canceler performance. In [57], the filter tap

values were calculated using a linear solver leveraging the linear nature of FIR filters. However, nonlinearities in gain and phase within each filter tap can introduce non-negligible computation errors, thereby requiring fine-tuning after the initial solution computed by the linear solver. Moreover, these methods are typically limited to adapting filter tap values and cannot directly optimize other critical tuning parameters, such as delay spread.

Alternative approaches [24, 27] have optimized SI cancelers by pre-measuring canceler settings and generating a look-up table (LUT), which significantly accelerates adaptation by leveraging a pre-measured SI frequency response. However, frequent recalibration of cancelers is needed due to variations in process, voltage, and temperature (PVT) conditions in real-world radio applications. This introduces additional adaptation overhead, particularly as the number of tuning variables increases. Additionally, while much of the prior work has focused on minimizing the number of adaptation iterations in the radio's digital back end (DBE), the time required to update the settings of integrated RF/analog cancelers from the DBE is often overlooked. This time can be non-negligible, particularly when the DBE is not integrated with the radio's analog front-end (AFE) chip.

The remainder of this dissertation explores methods to address the challenges and limitations of existing SI mitigation techniques. This begins with an analysis of design considerations for FIR filter-based RF SI cancelers in FD transceivers.

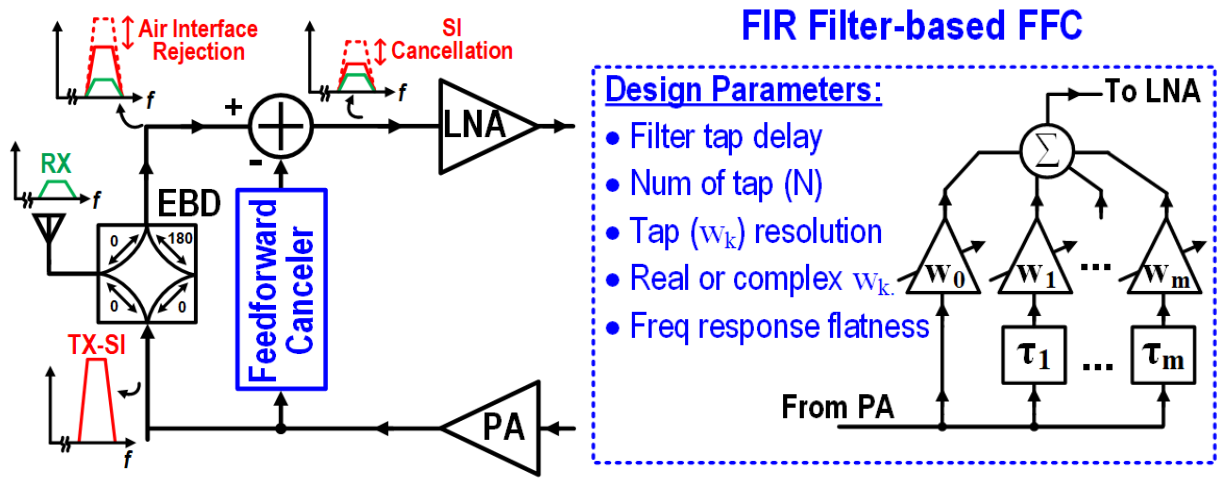
Chapter 3

DESIGN CONSIDERATIONS OF BROADBAND SELF-INTERFERENCE CANCELLATION FIR FILTERS FOR IN-BAND FULL-DUPLEX TRANSCEIVERS

As described in Chapter 2, time-domain cancelers for self-interference cancellation (SIC) are often implemented as finite impulse response (FIR) filters within a feedforward cancellation (FFC) path between a radio TX and RX [18,20,21,23,24]. These FIR filters mitigate SI leakage by adjusting delay spreads and amplitudes. This chapter explores the design space of FIR filters for SI cancellation, focusing on design parameters such as filter tap delay, number of taps, and filter tap resolution, to achieve broadband SI cancellation. The impacts of various FIR filter design parameters on SI cancellation depth and bandwidth are systematically studied and verified through circuit simulations and measurements in this work. The outcome of this study provides design guidelines for FIR filter-based SI cancelers for FD applications from the perspective of optimizing both SI cancellation bandwidth and depth.

3.1 FD Radio RF Front-end Interface

Although SI can be mitigated at numerous points along the receiver signal path from the antenna interface to the digital back-end, the reduction of strong SI prior to the low-noise amplifier (LNA) input is desirable from the perspective of minimizing the possibility of saturating the front-end and/or reducing distortion generated by later blocks in the receiver chain. As such, performing SI cancellation between the power amplifier (PA) output and the RX/LNA input in FD radios becomes essential. Fig.3.1a shows a typical FD transceiver RF front-end which consists of an antenna-air interface and an FFC path. An electrical balanced duplexer (EBD) [18, 21] acts as the antenna-air interface while providing initial SI



(a) (b)

Figure 3.1: (a) FD radio RF front-end with an antenna-air interface and a feedforward canceler. (b) Design parameters, explored in this chapter, for a true-time delayed FIR filter-based FFC includes filter tap delay, number of taps, filter tap resolution, real or complex tap coefficients, and frequency response flatness.

rejection; see Fig.3.1a. This is also emblematic of other antenna-air interfaces utilized in FD radios such as a circulator and separate antennas [20]. To provide additional SI cancellation, the FFC is implemented to match the SI leakage from the antenna-air interface. Then, the generated replica signal is subtracted from the receive signal path at the LNA input to cancel the residual SI (Fig.3.1a). While multiple FFC paths can be utilized to provide a total cancellation of more than 110 dB in FD radios [5], it is desired to maximize the SI cancellation at the RF front-end because it relaxes the linearity [58] required for the receiver and captures the PA noise as well as distortion products which arise in the entire TX chain.

Prior efforts have shown the SI signal originating from the transmitter to the receiver through multiple time-delayed paths with varying signal amplitudes and phase at the antenna-air interface [18, 20]. The FFC implemented as a multiple-tap FIR filter (Fig.3.1b) generates

a matched delay and scaled versions of the TX reference signal. Hence, FIR filter-based RF cancelers are considered as one effective approach for achieving SI cancellation. By controlling the reference signal path gain (w_k) from the PA output, with different delay spreads (τ_k) as shown in Fig.3.1b, a desired frequency response to match that of the SI leakage path can be obtained from an FIR filter in the FFC path. To maximize the SI cancellation, design parameters such as tap delay resolution and the number of taps of FIR filters as shown in Fig.3.1b need to be carefully chosen. More details about these design considerations are discussed in the next section.

3.2 FIR based FFC Design Considerations

As discussed in the aforementioned section, the effectiveness of the SI cancellation depends on how well the replica signal generated in the FFC path matches the SI leakage from the antenna-air interface and presented at the receiver input. In FD systems that utilize FIR filters for cancellation, the SI cancellation bandwidth and depth are directly influenced by the complexity of the FIR filter design. This section examines key design considerations of FIR filters, including filter tap delay, delay spread, and filter tap resolution. Additionally, we analyze the advantages of using complex weight values and assess how variations in SI amplitude and group delay (GD) over frequency impact SI suppression.

3.2.1 Filter Tap Delay and Number of Taps

The SI leakage from an FD transceiver antenna-air interface can be expressed as:

$$x_{SI}(t) = H_0 \cdot x_{PA}(t - \tau_{d0}) \tag{3.1}$$

when assuming the SI leakage has a constant attenuation of H_0 and GD of τ_{d0} across the signal bandwidth, where $x_{PA}(t)$ is the transmitted signal at the PA output. The cancellation signal at the FIR filter output in Fig.3.1b is described by:

$$y(t) = w_0 \cdot x_{PA}(t) + \sum_{k=1}^{m} w_k \cdot x_{PA}(t - \tau_k) \tag{3.2}$$

where we assume the delay resolution, $\tau_{r0} = \tau_k - \tau_{k-1}$, is a constant for different k. Performing SI cancellation with the use of an FIR filter can be viewed as a sampling and interpolation problem [5]. Based on the Nyquist sampling theorem [5], the FIR filter at an FD radio RF front-end is able to reconstruct the SI signal $x_{SI}(t)$ by adjusting the weight coefficients (w_k) when the filter tap delay resolution τ_{r0} satisfies the following condition:

$$\tau_{r0} < \frac{1}{2(f_c + f_{BB})} \approx \frac{1}{2f_c} \tag{3.3}$$

where the signal bandwidth f_{BB} is assumed to be much less than the carrier frequency f_c in (3.3). Given that the filter taps closet to the SI delay spread have the most significant impact on cancellation, the maximum delay spread (τ_m in Fig.3.1b) of the FIR filter must be greater than the SI GD τ_{d0}. The required number of filter taps (N) can then be determined based on the SI leakage GD (τ_{d0}) and the filter tap delay resolution τ_{r0} as given in (3.3):

$$N > \frac{\tau_{d0}}{\tau_{r0}} + 1 \tag{3.4}$$

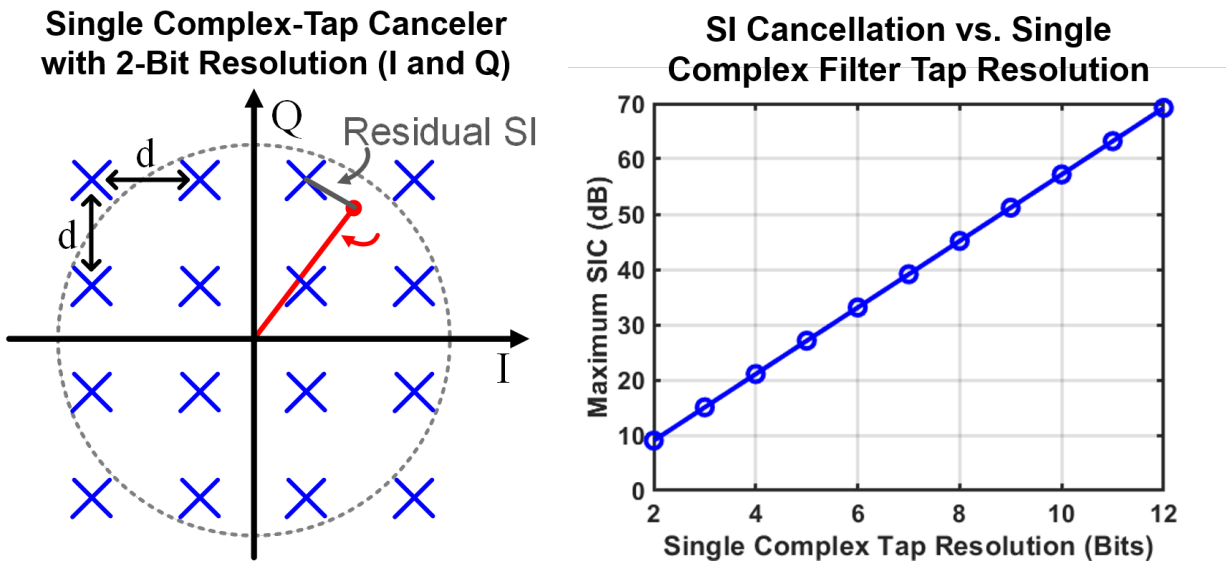
3.2.2 Complex Filter Tap

The weight coefficients (w_k) of each tap in Fig.3.1b can be implemented as either real or complex values in the design of an FIR filter. Previous studies [26] have shown that complex-tap FIR filters provide broader cancellation bandwidth when τ_{r0} does not satisfy the delay resolution requirement in (3.3). However, our analysis implies that complex weight values enhance the SI cancellation in scenarios where the SI GD varies within the bandwidth, due to a nonlinear phase response, which is often encountered at an FD radio antenna-air interface such as an EBD [18] or a circulator [20]. If the SI in (3.1) exhibits a frequency-dependent GD $\tau_d(\omega)$, its frequency-domain expression is:

$$X_{SI}(\omega) = H_0 \cdot X_{PA}(\omega) \cdot e^{-j\omega\tau_d(\omega)} \tag{3.5}$$

If we interpret $\tau_d(\omega)$ as an additional phase shift $\theta(\omega)$ added to a constant group delay ($\tau_d(\omega) = \tau_{d0} + \frac{\theta(\omega)}{\omega}$), (3.5) can be expressed as:

$$X_{SI}(\omega) = H_0 \cdot X_{PA}(\omega) \cdot e^{-j\omega\tau_{d0}} \cdot e^{-j\theta(\omega)} \tag{3.6}$$



(a) (b)

Figure 3.2: (a) Illustration of a single complex-tap filter with 2-bit resolution for both the I and Q paths, used to match the amplitude and phase of the SI signal. (b) Maximum SI cancellation as a function of the single complex-tap filter resolution in the FFC path.

When w_k in (3.2) is a complex number ($w_k = w_{i,k} + jw_{q,k} = |w_k|e^{j\theta_k}$), the phase θ_k of each tap in the FIR filter can be controlled by adjusting $w_{i,k}$ and $w_{q,k}$ independently to match $\theta(\omega)$ in (3.6), which is independent of the delay spread τ_k, thus increasing both the SI cancellation bandwidth and depth.

3.2.3 Filter Tap Resolution

The achievable SI cancellation of an FIR filter is also limited by the resolution of the filter tap (w_k). In this section, for the purposes of comparison, the SI cancellation is assumed to be performed by a single tap filter with complex coefficient w_k. The complex w_k is often implemented as a Cartesian-G_m stage [18, 19, 26, 27] where $w_{i,k}$ and $w_{q,k}$ can be tuned independently. Fig.3.2a illustrates the utilization of a single complex-tap filter with n-bits

(n=2) of resolution for both the I and Q paths in the FFC path, designed to match the amplitude and phase of the SI leakage signal from the antenna-air interface, assuming no phase mismatch between the I and Q paths. The SI leakage is represented by the red vector in Fig.3.2a. The constellation points in Fig.3.2a represent the FFC path reference signal for all of the available filter tap settings. The residual SI signal is the difference between the red SI leakage vector and its nearest constellation point. The maximum residual SI amplitude after cancellation (shown in Fig.3.2a) occurs when the SI leakage is positioned at the center of four constellation points, which can be calculated as $\frac{\sqrt{2}}{2} \cdot d$. Since the maximum canceler range is defined by the radius of the largest circle covered by the constellation points in Fig.3.2a, which is equal to $2^{n-1} \cdot d$, the theoretically achievable SI cancellation of a single complex-tap filter with n-bits of resolution is given by:

$$SIC(dB) = 20 \cdot log_{10} \frac{2^{n-1} \cdot d}{\frac{\sqrt{2}}{2} \cdot d} \approx 6n - 3 \tag{3.7}$$

The resulting SI cancellation as a function of the single complex filter tap resolution derived from (3.7) is presented in Fig.3.2b. One bit increase in the resolution of w_k improves the SI cancellation by 6 dB. As shown in Fig.3.2b, a SI cancellation depth of close to 70 dB is possible by using a 12-bit single complex-tap filter. However, most state-of-the-art cancelers [20, 21] have resolutions of fewer than 8 bits, which is limited by factors such as increased canceler noise, power consumption, device mismatches [27], and any undesired feed-through coupling paths.

3.2.4 Amplitude and GD Mismatches

The result derived in (3.7) represents the theoretical achievable SI cancellation at one frequency point. However, SI cancellation across a certain frequency band also depends on variations in SI amplitude and GD across the bandwidth, as illustrated by the red dashed lines in Fig.3.3a and 3.3b. Assuming linear deviations of the SI signal in contrast to a flat replica signal from the FFC path, for both amplitude (ΔA in Fig.3.3a) and GD ($\Delta\tau$ in Fig.3.3b) over a certain bandwidth (e.g., 2.4–2.5 GHz), the corresponding cancellation are

presented in Fig.3.3c and 3.3d, respectively. For this discussion, an 8-bit complex filter tap resolution is assumed, with only one variable (either amplitude or GD) varied at a time. As shown in Fig.3.3c and 3.3d (blue traces), with an amplitude deviation (ΔA) of 0.1 dB and a GD deviation ($\Delta\tau$) of 50 ps across a bandwidth of 100 MHz, the SI cancellation degrades from 45 dB to 35 dB and 36 dB, respectively. It is seen that for larger amplitude or GD variations, the achievable SI cancellation are significantly reduced with the increase in bandwidth. In practice, the frequency profiles of the SI amplitude and GD are determined by the antenna-air interface. Minimizing the amplitude and GD variations across the channel bandwidth for both the SI and cancellation signals will enhance the SI cancellation bandwidth.

3.2.5 Design Considerations Summary

The following conclusions can be drawn from previous analysis:

- The number of taps in an FIR filter need to satisfy both the delay resolution (3.3) and delay spread (3.4) requirements to achieve broadband SI cancellation.

- Complex tap filters increase both the SI cancellation depth and bandwidth as compared to real tap filters, particularly when the GD of SI varies with frequency.

- The maximum SI cancellation achieved by using an FIR filter is constrained by the resolution of the weight coefficient w_k.

- Minimizing gain and GD mismatches between the SI and cancellation signals across the bandwidth improves SI cancellation over a broad bandwidth.

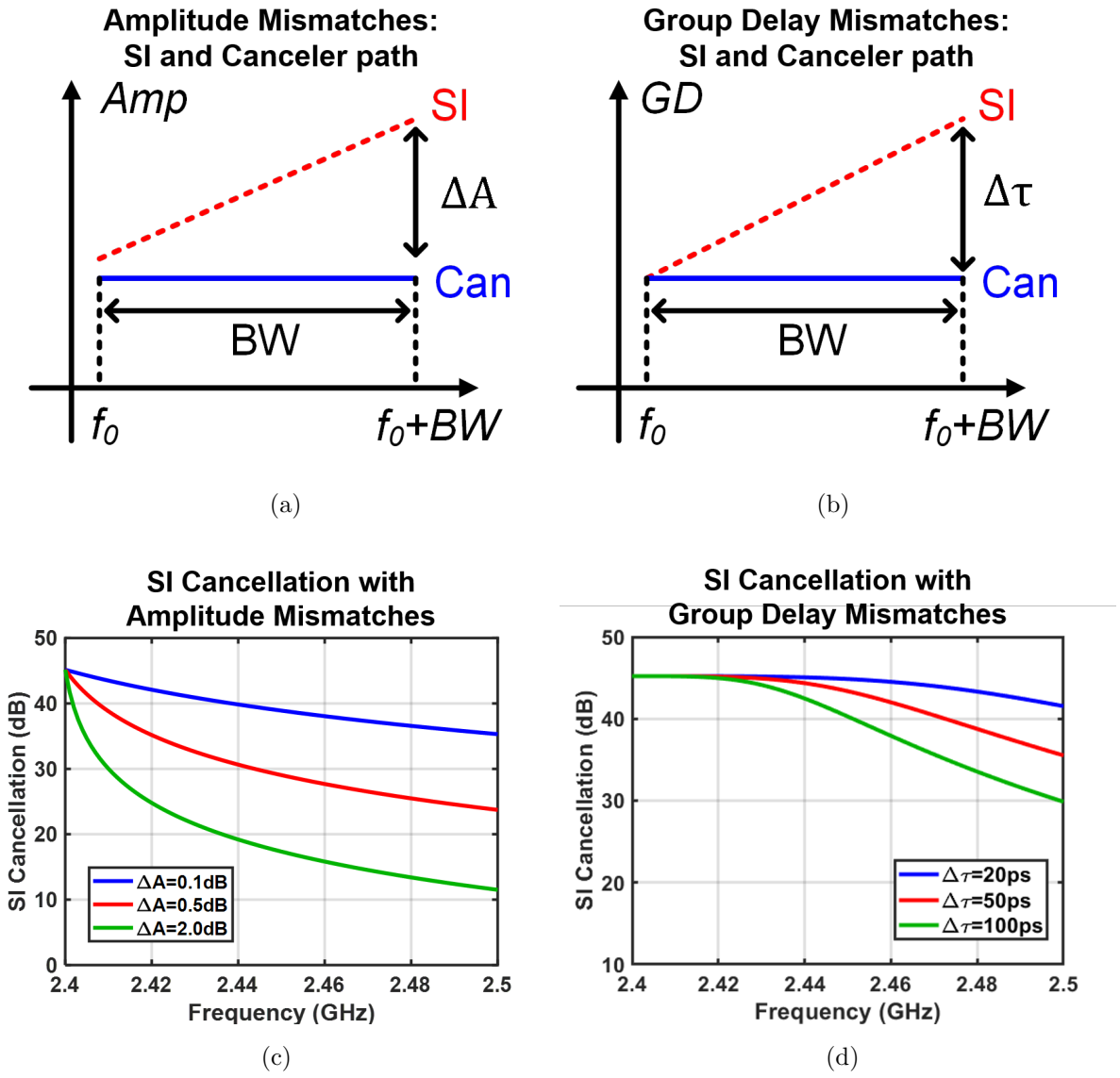


Figure 3.3: Illustrations of (a) amplitude and (b) GD mismatches between the SI leakage and the signal from the FFC path. Resulting SI cancellation as a function of bandwidth for varying (c) amplitude and (d) GD deviations.

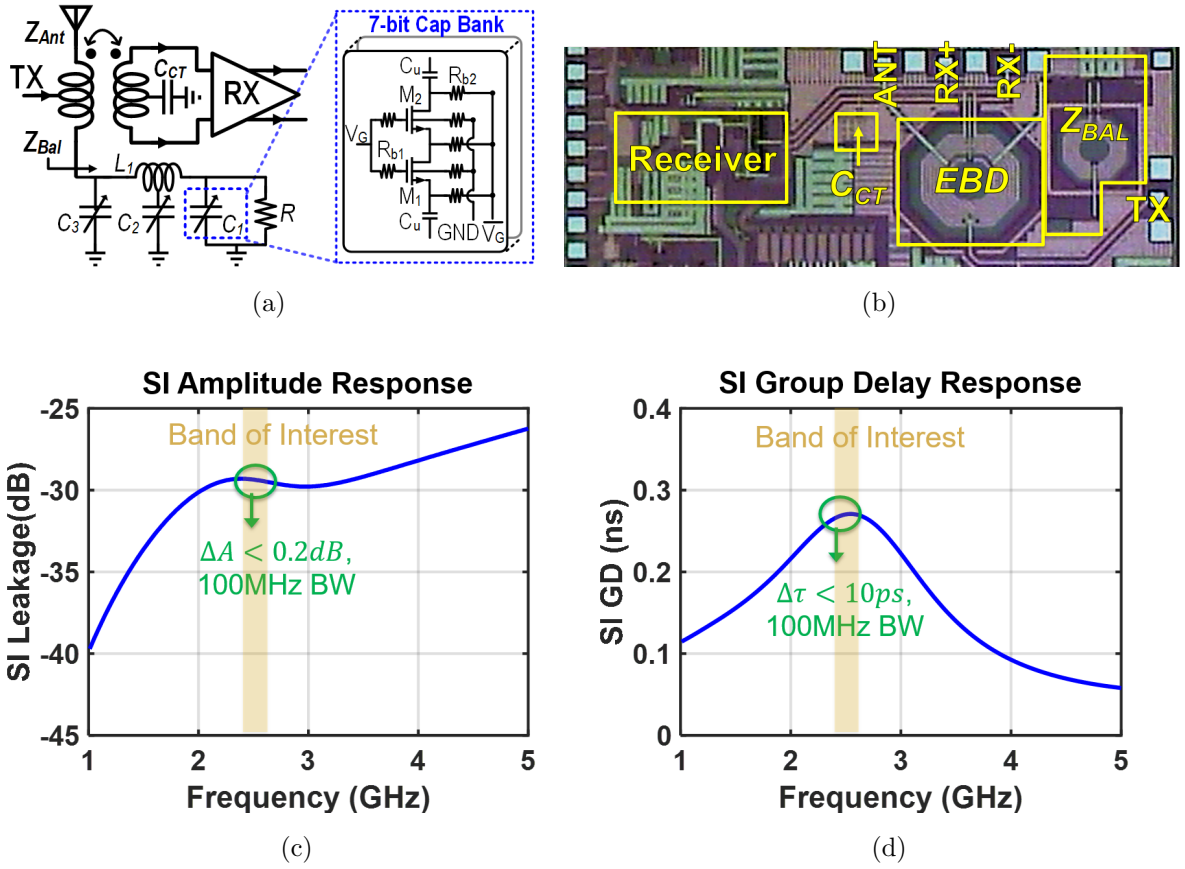


Figure 3.4: (a) Schematic diagram and (b) chip die photograph of the EBD with an Z_{Bal} [18]. (c) Amplitude response and (d) GD response of the EBD SI leakage.

3.3 Simulation and Measurement Results

3.3.1 Antenna-air Interface SI Leakage

To verify the analysis in Section 3.2, a series of simulations and measurements were performed. To this end, an FD radio front-end with an EBD as the antenna-air interface and a feedforward canceler shown in Fig.3.1a are used for the simulations and measurements. An EBD with a tuned impedance matching network Z_{Bal} (Fig.3.4a) is used to provide the first-stage SI rejection in the 2.4 GHz band at an FD transceiver antenna-air interface [18].

The die photograph of the EBD and the receiver implemented in a TSMC 40 nm CMOS process are shown in Fig.3.4b. A 4^{th} order Z_{Bal} in Fig.3.4a realized using three 7-bit tunable capacitor banks effectively mitigates the amplitude and GD variation of the SI leakage [18], which will increase the SI cancellation of the FFC across a broader bandwidth, as discussed in Section 3.2.4. The measured TX-RX SI leakage of the EBD (Fig.3.4c) is about 29 dB with an amplitude variation of less than 0.2 dB between 2.4-2.5 GHz. The SI GD (Fig.3.4d) is about 250 *ps* at 2.4 GHz with a variation of less than 20 *ps* over a 100 MHz bandwidth. The SI frequency response in Fig.3.4c and 3.4d will be utilized to simulate the SI cancellation of an FIR filter in the next section.

3.3.2 SI Cancellation of FIR Filters

The SI cancellation is simulated using behavioral-level models and varying the FIR filter settings. The measured EBD SI leakage shown in Fig.3.4c and 3.4d is used to represent the SI from the FD transceiver air-interface in these simulations. Fig.3.5a and 3.5b show the SI cancellation depth of the FIR filters as a function of the signal bandwidth for real and complex filter taps, respectively. All simulations used a multi-carrier 16-QAM modulated signal with varying bandwidths, and the filter tap coefficients w_k are adapted using a least-mean square algorithm. The w_k coefficients have 8-bits of resolution. The total delay spread of the filter is fixed at 400 *p*s while varying the number of taps, which exceeds the measured maximum GD of the SI leakage shown in Fig.3.4d. As illustrated in Fig.3.5a and 3.5b, increasing the number of filter taps and ensuring that the filter tap delay resolution τ_{r0} satisfies the requirement in (3.3), results in a significant improvement in the SI cancellation across a 100 MHz bandwidth. The SI cancellation depth improvement for a 100 MHz modulated signal bandwidth is approximately 10 dB and 15 dB for the real-tap and complex-tap filters, respectively, which validates our analysis in Section 3.2.1.

For the purposes of comparison, Fig.3.5c shows the simulated SI cancellation using a complex 5-tap and a real 10-tap FIR filter. With an equal number of tuning variables in the filter tap coefficients, the complex 5-tap filter approximately enhances the SI cancellation

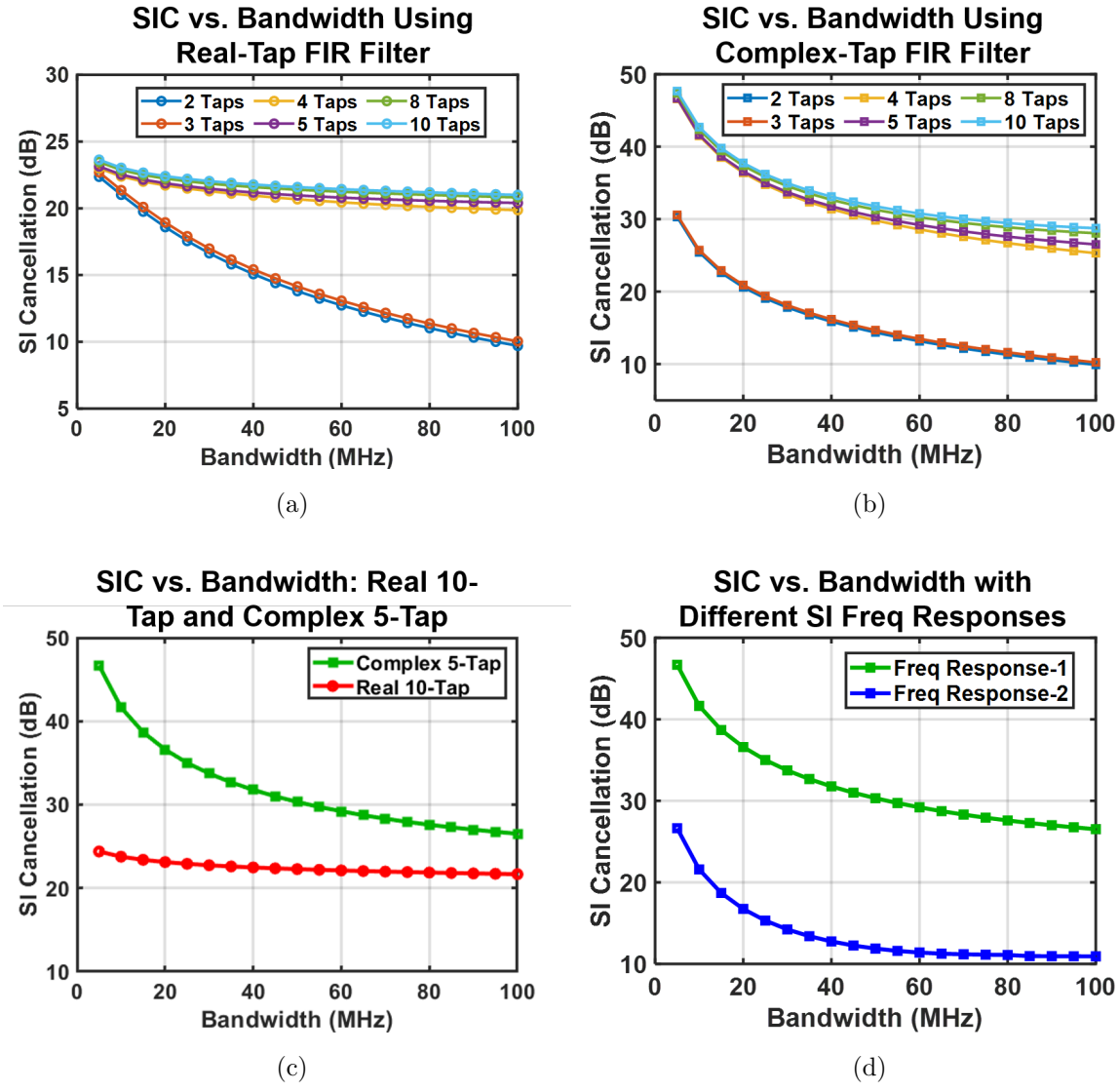


Figure 3.5: Simulated SI cancellation versus 16-QAM modulated signal bandwidth with different number of taps for (a) real-tap and (b) complex-tap FIR filter. (c) Comparison of SI cancellation between real and complex filter tap coefficients. (d) Simulated SI cancellation using a 5-tap complex FIR filter for two different SI leakage frequency responses.

by approximately 10 dB for a 40 MHz bandwidth modulated signal. This improvement is due to the complex-tap filter's ability to independently control the phase of the reference cancellation signal, allowing it to more closely match the SI leakage profile from the antenna-air interface to the receiver input, as compared to the real-tap filter. It is also noteworthy that while a complex-tap FIR filter implemented as a Hilbert transform ideally introduces a uniform 90° phase shift (θ_{can}) across all frequencies within the bandwidth, the SI signal itself may exhibit frequency-dependent phase shifts ($\theta(\omega)$) or GD variations, as shown in Fig.3.4d. Consequently, the complex-tap FIR filter can more accurately match the SI leakage, achieving a notably higher cancellation depth than a real-tap FIR filter, particularly when the signal bandwidth is small, as shown in Fig.3.5c.

Fig.3.5d shows the simulated SI cancellation of a complex 5-tap filter for two different SI frequency responses obtained from the radio antenna-air interface. Frequency response-1, measured in Section 3.3.1 exhibits smaller gain and GD variations within the bandwidth compared to frequency response-2, which is simulated using the EBD and Z_{Bal} implemented as a series RLC circuit, as described in [59]. The simulated amplitude and GD variations for frequency-response 2 are about 5 dB and 2 ns, respectively [18]. As shown in Fig.3.5d, reducing the amplitude and GD variations of the EBD SI leakage improves SI cancellation by more than 15 dB across a modulated signal bandwidth of 5-100 MHz, aligning with the discussion in Section 3.2.4.

Finally, in order to further verify our analysis, measurements were performed using a prototype complex-tap FIR filter chip implemented in a TSMC 40 nm CMOS process in [18]. Each tap has a measured delay of about 70 ps with 8-bit resolution. A pseudo-blind search algorithm [18] was used to adapt the filter taps to maximize the average SI cancellation depth across the bandwidth in the measurement. The measurement results are compared with the behavioral-level simulation using the same FIR-filter parameters, as shown in Fig.3.6. The measured SI cancellation of the complex 5-tap filter is 42 dB for a 5 MHz bandwidth modulated signal and 20 dB for a 100 MHz bandwidth modulated signal. Although the measured cancellation for the 100 MHz bandwidth signal is approximately 5 dB lower than

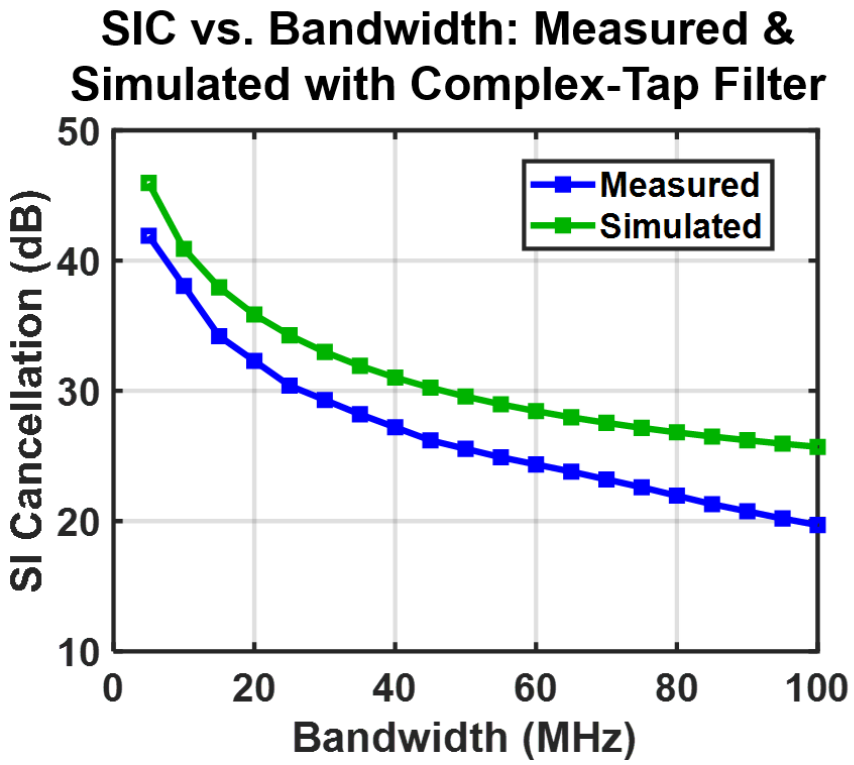


Figure 3.6: Measured and simulated SI cancellation of a 5-tap complex FIR filter, with 70 ps delay and 8-bits of resolution per tap.

the simulation results, it closely follows the same trend as the simulations. This discrepancy may be attributed to gain and GD variations between each canceler filter tap, adaptation errors, and other non-ideal circuit performance. Both the simulation and measurement results support the analysis in Section 3.2. These findings confirm that achieving deeper and wider bandwidth SI cancellation requires careful selection of the number of taps and filter tap delay in a complex-tap FIR filter, along with minimizing amplitude and GD variations of both the SI and cancellation signals in an FD transceiver.

3.4 Conclusion

This chapter examines the design parameters of FIR filters and their impact on SI cancellation in FD transceivers utilizing the FFC method. Design considerations, such as the filter tap delay, filter tap resolution, amplitude and group delay variations of the SI signal, are thoroughly analyzed. These considerations are subsequently validated through a series of simulations and measurements. A comprehensive understanding of these design factors is crucial for optimizing both the depth and bandwidth of SI cancellation for use in FD radios, which will be used in the following chapters to implement integrated SI cancellation for FD radios.

Chapter 4

EFFECTS OF RECEIVER INPUT IMPEDANCE ON NONLINEAR DISTORTION IN FULL-DUPLEX RADIOS

This chapter explores an often overlooked effect of self-interference (SI) in integrated FD radios, which is the generation of nonlinearities at the receiver input caused by crossmodulation between common- and differential-mode TX self-interference (SI) [58]. The analysis reveals that residual TX-SI can drive the nonlinear receiver input impedance(Z_{rx}), generating distortion products that degrade RX linearity. To suppress these distortion components below the RX noise floor, SI mitigation circuits at the FD radio RF front-end must provide at least 50 dB of common-mode isolation to achieve sufficient RX linearity, as supported by both theoretical analysis and transistor-level simulations.. The chapter concludes with a strategy to minimize nonlinearities at the RX input caused by residual TX-SI, which will be implemented in the integrated FD front-end design presented in the following chapters.

4.1 Introduction

As described in Chapter 2, ideal SI mitigation circuits must provide high SI suppression depth while maintaining high linearity, since any nonlinear distortion injected by these circuits degrades RX sensitivity. Recent research has reported highly linear SI mitigation circuits using all-passive integrated electrical balance duplexers (EBD) [46, 60]. However, most of these efforts measure the IP_3 of a standalone duplexer, which does not fully capture the practical scenario where the duplexer is interfaced to the RX chain. Traditional methods to measure distortion at the RX input consider the nonlinearities generated from both the RX chain and SI mitigation circuits. However, this chapter focuses specifically on the effects of nonlinear RX input impedance (Z_{rx}) presented at the differential receiver input in the

presence of strong residual TX-SI. The primary contributions to nonlinear Z_{rx} include the input device transconductance (g_m) of the LNA and the junction capacitance at the RX input.

The following sections investigate the effects of both differential- and common-mode residual SI on distortion generated at the RX input. Of particular interest is the often overlooked phenomenon where common-mode TX-SI generates differential intermodulation products. To the best of our knowledge, this was the first attempt to model and verify through circuit simulation the distortion generated by nonlinear Z_{rx} at the RX input. Understanding the intermodulation components generated right at the RX input is critical to evaluate the FD receiver performance in the presence of strong TX-SI.

4.2 TX-SI Induced Intermodulation at the RX input

While distortion generated by SI mitigation circuits at the RX input has been discussed in [46, 61], the impact of nonlinear receiver input impedance Z_{rx} on FD radio front-end design is often overlooked. This section examines the distortion generated from Z_{rx} in the presence of residual TX-SI. As shown in Fig. 4.1, SI mitigation circuits, including a duplex filter and a feedforward canceler (FFC), are implemented to suppress SI. An ideal FFC is designed with a high output impedance to minimize receiver insertion loss so that the small-signal impedance of Z_{rx} (typically 50Ω) dominates at the RX input. However, residual TX-SI can modulate the nonlinear resistance and junction capacitance of Z_{rx}, thereby creating IM_3 distortion components.

Distortion introduced by nonlinear Z_{rx} need to be considered, particularly when the residual SI power at the RX input is typically significanlly larger (by tens of dB) than the desired RX signal [20, 21]. Any distortion introduced by Z_{rx} will add to the nonlinearities produced by TX-SI passing through the SI mitigation circuits, as well as intermodulation products generated by the RX chain, which are referenced back to the RX input (Fig.4.1). To better understand the intermodulation products introduced at the RX input, a model is developed to analyze the nonlinearities associated with Z_{rx}. The residual SI voltage signal

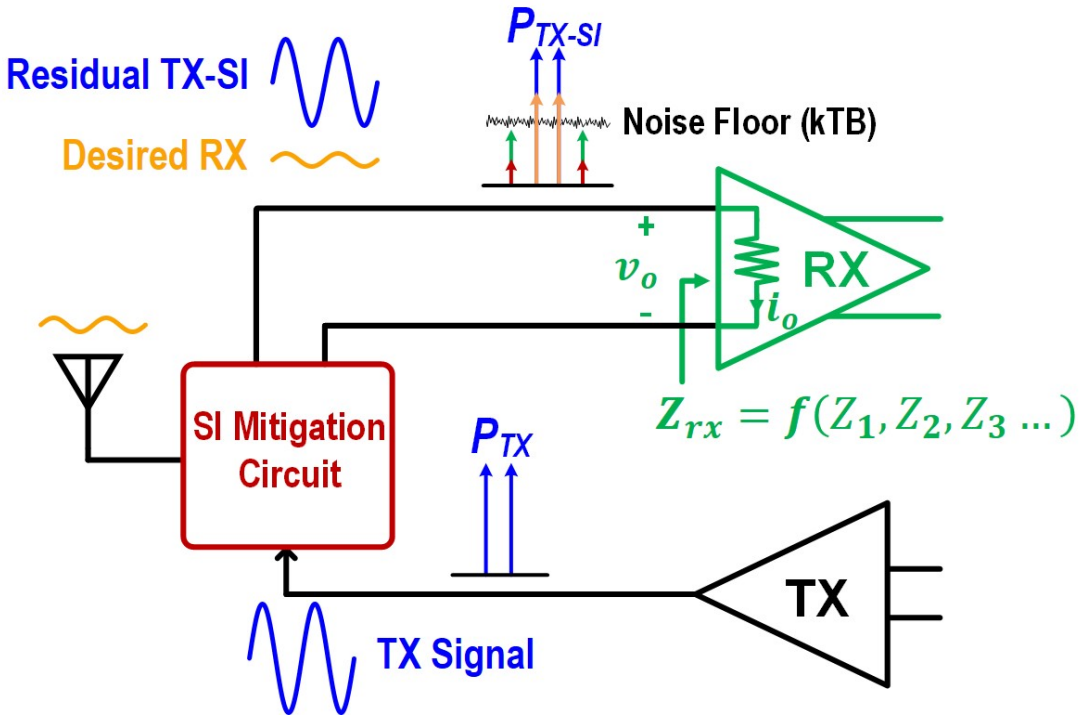


Figure 4.1: Intermodulation distortion generated at the RX input in the presence of TX-SI in FD radios. Intermodulation components in red originate from SI mitigation circuits, while those in green are introduced by nonlinear Z_{rx}.

at the RX input (v_o) can be expressed as a power series expansion of the SI leakage current (i_o) shunted into the receiver:

$$v_o = Z_1 i_o + Z_2 i_o^2 + Z_3 i_o^3 + \ldots \tag{4.1}$$

Here, Z_1 represents the small-signal impedance of Z_{rx}, while Z_2 and Z_3 are the 2$^{\text{nd}}$ and 3$^{\text{rd}}$ order coefficients of Z_{rx} which describe the corresponding nonlinear contributions to v_o, respectively. For example, in a common-gate LNA, Z_1 is equal to $1/g_m$ where g_m is the transconductance of the LNA input device. The values of Z_2 and Z_3 can be derived by using Lagrange's notation [62], which relates to the higher order transconductance nonlinear coefficients g_{m2} and g_{m3} [63]. Since the input impedance of most LNAs is a function of g_m,

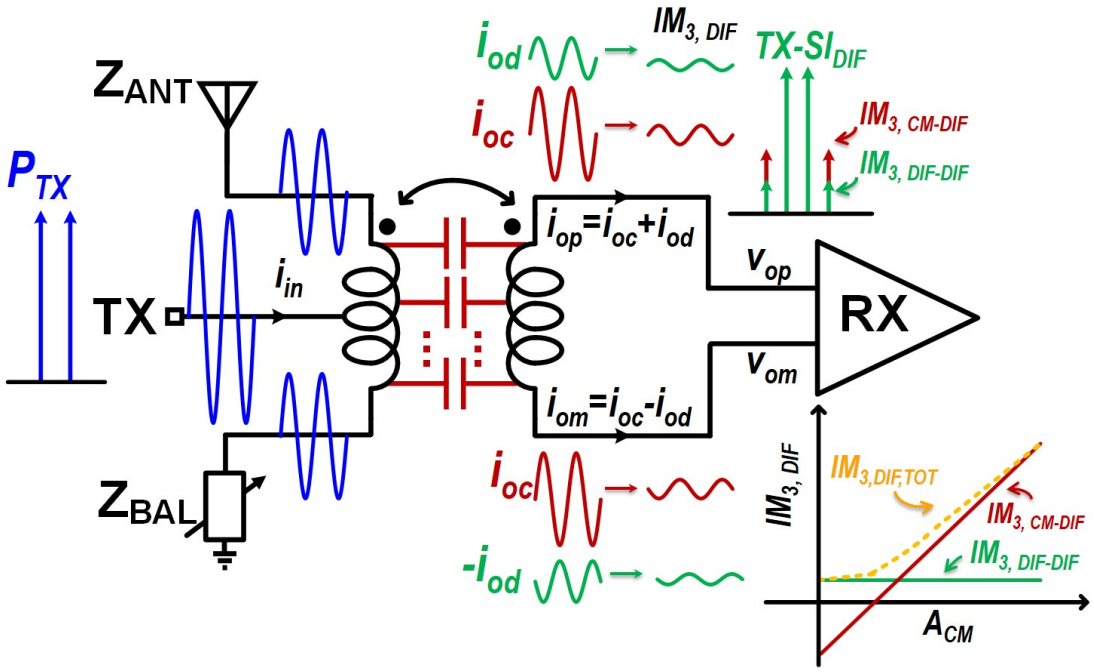


Figure 4.2: An illustration of both magnetic and capacitive coupling between transformer coils in an EBD. Both differential- and common-mode SI leakage current see a nonlinear Z_{rx}, introducing differential IM_3 at the RX input. Differential IM_3 associated with common-mode dominates when common-mode TX-SI leakage is large.

the effects of nonlinear impedance apply to various LNA topologies. Thus, unless the residual TX-SI at the RX input is sufficiently suppressed, Z_{rx} will introduce non-negligible distortion products. When designing SI mitigation circuits, both the amount of SI suppression and the nonlinear behavior of Z_{rx} should be carefully considered, as the cancellation circuitry interfaces directly with the nonlinear Z_{rx}.

4.3 Impact of TX Common-mode Leakage

To further explore the impact of TX-SI leakage on the linearity performance of FD radios, we consider the transceiver's antenna-air interface and assume the use of an integrated EBD. The EBD operates based on matching (electrical balancing) of two impedances – the antenna

and a balancing network (Z_{Bal}) – within a hybrid transformer. This allows splitting the TX output power between two primary coils, which then couple to a secondary coil on the receiver side, as shown in Fig.4.2. When the antenna and balancing impedance are well-matched, differential SI leakage is effectively suppressed at the RX port. However, while an EBD provides high isolation for differential TX-SI, it has poor common-mode isolation due to capacitive coupling between the primary and secondary transformer coils (Fig.4.2). This is problematic from RX linearity perspective, because the common-mode TX leakage will create crossmodulation at Z_{rx}, generating differential-mode intermodulation products (Fig.4.2).

A power series expansion of the nonlinear Z_{rx} was used to analyze the effect of common-mode signals at the differential receiver input. In the following analytical model, the EBD and Z_{Bal} nonlinearity are neglected. Signals at RX positive (v_{op}) and negative (v_{om}) inputs can be written as follows from (4.1):

$$v_{op} = Z_1(i_{oc} + i_{od}) + Z_2(i_{oc} + i_{od})^2 + Z_3(i_{oc} + i_{od})^3 \tag{4.2}$$

$$v_{om} = Z_1(i_{oc} - i_{od}) + Z_2(i_{oc} - i_{od})^2 + Z_3(i_{oc} - i_{od})^3 \tag{4.3}$$

where i_{oc} and i_{od} represent the common- and differential-mode SI leakage currents at the RX input, respectively. From (4.2) and (4.3), the differential RX input voltage can be calculated ($v_o = v_{op} - v_{om}$):

$$v_o = Z_1.2i_{od} + Z_2.4i_{oc}i_{od} + Z_3(2i_{od}^3 + 6i_{oc}^2 i_{od}) + ... \tag{4.4}$$

Next, we further assume $i_{oc} = A_{cm}i_{in}$ and $i_{od} = A_{dif}i_{in}$, where A_{cm} and A_{dif} represent the common- and differential-mode TX-to-RX SI leakage, respectively. Substituting these in to (4.4) gives:

$$v_o = Z_1.2A_{dif}i_{in} + Z_2.4A_{cm}A_{dif}i_{in}^2 + Z_3(2A_{dif}^3 + 6A_{cm}^2 A_{dif})i_{in}^3 + ... \tag{4.5}$$

We can now express the differential IM_3 generated by applying a current i_{in} with two tones of equal amplitude (S_i) as:

$$IM_{3,DIF} = \frac{3}{4}(2A_{dif}^3 + 6A_{cm}^2 A_{dif})S_i^3 \tag{4.6}$$

The second term ($6A_{cm}^2 A_{dif}$) associated with the TX common-mode leakage in (4.6) indicates that common-mode TX leakage A_{cm} introduces differential nonlinear distortion. The differential component of the residual TX-SI interacts with the common-mode residual TX-SI to produce differential IM_3 distortion. When the common-mode TX-SI leakage is much larger than the differential-mode TX-SI leakage ($A_{cm} \gg A_{dif}$), as is typically the case at the EBD output, the differential IM_3 associated with the common-mode leakage dominates at the RX input (shown in Fig.4.2), which will degrade the RX linearity. Since the TX common-mode leakage generates differential distortion at the RX input, simply designing an LNA and RX chain that are immune to common-mode signals [21, 64] is insufficient to improve RX linearity. Note that the model describing the differential nonlinear distortion arising from the TX common-mode leakage can be applied to any differential circuits which experiences a strong common-mode signal. Therefore, achieving high common-mode isolation when designing SI mitigation circuits between TX and RX is critical in FD transceivers.

4.4 Antenna-Air Interface Linearity Simulation Results

4.4.1 Circuit Simulation Model

To verify the effects of TX-SI common-mode to differential distortion conversion on RX linearity performance, a series of circuit-level simulations were performed. The assumed FD radio front-end (Fig.4.3) includes an EBD at the antenna-air interface to provide differential SI isolation. A tunable balancing impedance Z_{Bal} realized using a tunable resistor and capacitor bank controlled by integrated switches is necessary to track and match the varying antenna impedance [60]. The RX chain consists of an LNA [21], passive mixers, and a trans-impedance amplifier (TIA), which then feeds into the analog baseband. All components were modeled using transistor-level schematic simulations. The RF canceler is implemented as an adaptive FIR filter identical to the implementation given in [20, 21].

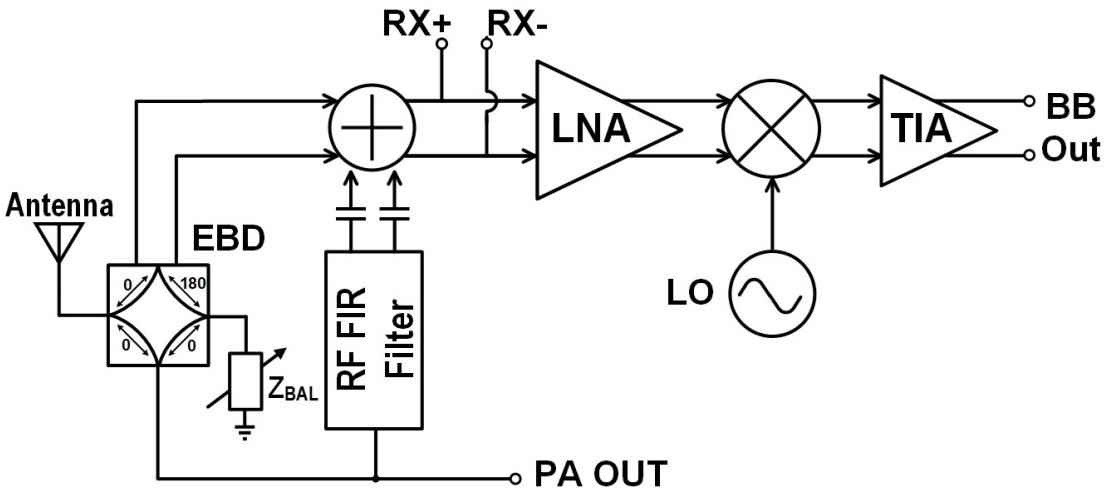
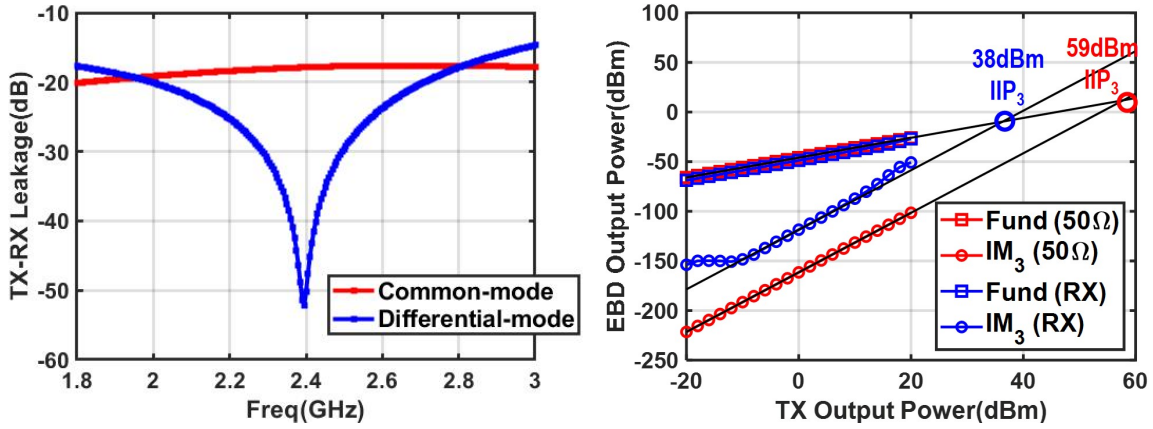


Figure 4.3: Block-level diagram of a FD radio AFE which includes an EBD, a feedforward canceler, and an LNA followed by a mixer driven by a synthesizer. Simulation results were generated using a transistor-level schematic implementation of this block diagram.

4.4.2 Simulation Results

The radio front-end (Fig.4.3) was implemented in a TSMC 40 nm CMOS process. Simulations were performed using Cadence Spectre combined with Peakview EM simulations to model the passive components. The RF canceler in Fig.4.3 was turned off in the simulations to model the effect of RX input nonlinear capacitive loading. The EBD Z_{Bal} was tuned to achieve maximum differential TX-RX isolation (Fig.4.4a). The differential SI attenuation provided by the EBD is higher than 40 dB over a 60 MHz bandwidth, while the common-mode SI suppression is only 18 dB which is significantly lower than the differential SI attenuation. To characterize the nonlinearity of the EBD and Z_{rx}, two in-band tones were applied to the PA output, and the EBD output voltage was simulated. Fig.4.4b shows the fundamental and IM_3 components in two configurations: the EBD interfacing to a 50Ω resistor and to the RX chain (Fig.4.3). When the EBD interfaces to a 50Ω resistor, nonlinearties are primarily generated by the EBD tuning switches in Z_{Bal}, and the IP_3 referred



(a) (b)

Figure 4.4: (a) Simulated differential- and common-mode TX-SI leakage provided by the EBD. (b) Linearity (IP_3) simulation of the EBD and Z_{rx} when the EBD interfaces to a 50Ω resistor or the RX chain with two tones at 2.4 GHz and 2.42 GHz.

to the PA output is about 59 dBm. However, when the EBD is connected to the RX chain and the FFC output, since the nonlinear Z_{rx} introduces IM_3 distortion at the EBD output, causing the IP_3 referred to the PA output degrade to 38 dBm, which degrades the FD radio front-end linearity performance.

To understand the distortion generated at the differential receiver input from residual common- and differential-mode TX-SI leakage current applied to a nonlinear Z_{rx}, an ideal hybrid transformer (Fig.4.5) is used in the following simulations to model the EBD. Both the residual differential- and common-mode SI current signals at the RX input can be controlled by adjusting R_{BAL}, C_1, and C_2. Fig.4.6a shows the simulated differential IM_3 at the RX input as a function of differential TX-to-RX SI leakage. C_1 and C_2 are set to zero, which eliminates any common-mode signal component at the transformer output. The TX output power is set to +15 dBm. The corresponding simulated IP_3 referred to the PA output versus differential SI leakage is also shown in Fig.4.6a. As the differential SI leakage increases,

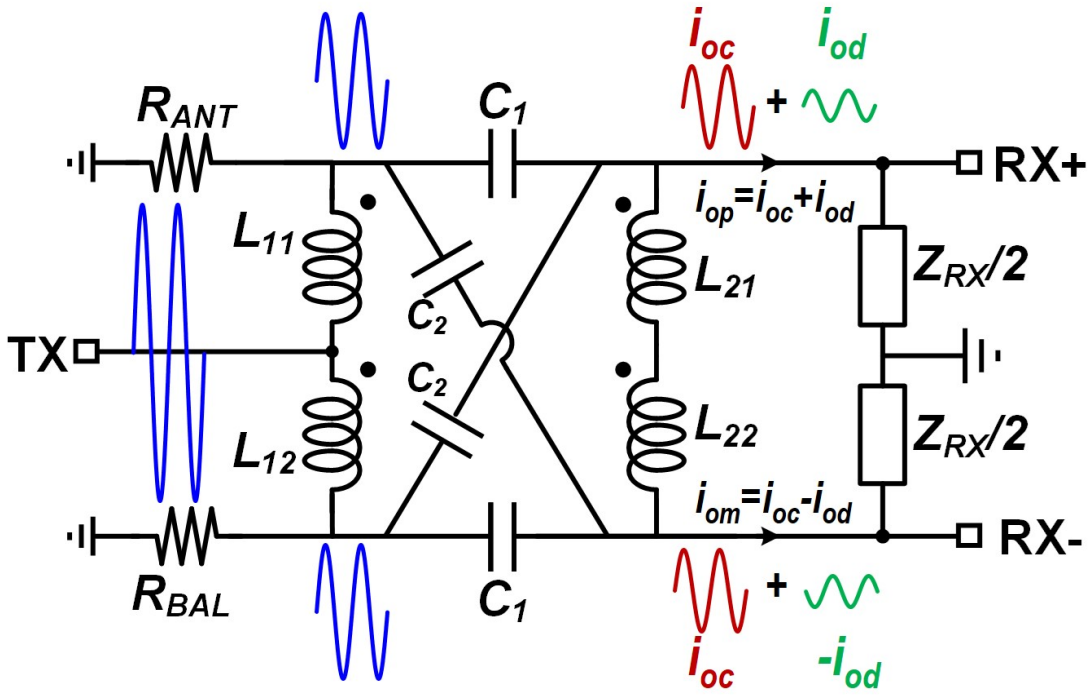
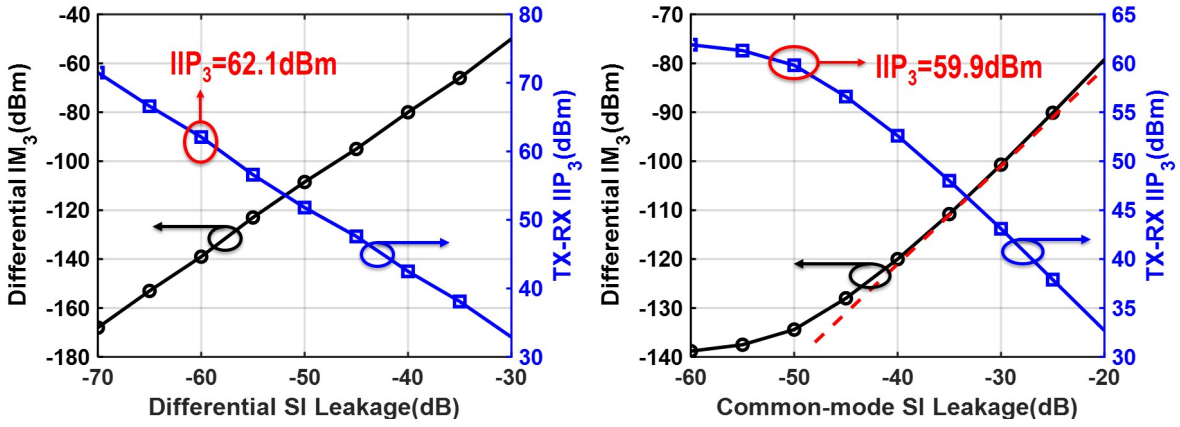


Figure 4.5: A hybrid transformer used to model the impact of residual TX-SI on differential IM_3. The capacitive-coupling in the transformer generates a common-mode residual TX-SI current which interacts with a nonlinear Z_{rx}, creating differential voltage-mode distortion.

the residual differential SI current also increases, which introduces more IM_3 distortion and degrades RX linearity. For example, in order to meet the linearity requirement of an FD transceiver (residual SI leakage introduced differential $IM_3 < -100dBm$), the differential SI suppression at the FD radio front-end interface must be higher than 50 dB.

To understand the effect of common-mode leakage on RX linearity performance, the differential IM_3 at RX input as a function of common-mode TX-SI was simulated, with results shown in Fig.4.6b. The differential SI leakage is set to -60 dB. When the SI common-mode leakage is larger than -40 dB, as the common-mode leakage increases by 1 dB, the differential IM_3 increases by approximately 2 dB, which agrees well with the relation in (4.6). The corresponding IP_3 referred to the TX output is also shown in Fig.4.6b, which further confirms the



(a) (b)

Figure 4.6: (a) Simulated differential IM_3 and the corresponding IP_3 referred to TX output versus differential SI leakage when common-mode SI leakage is 0. (b) Simulated differential IM_3 and the corresponding IP_3 referred to TX output versus common-mode SI leakage when differential SI leakage is -60 dB.

SI common-mode leakage introduces differential distortion at the RX input, degrading RX linearity. For example, to maintain sufficient RX linearity with differential $IM_3 < -110dBm$, a high common-mode isolation of greater than 40 dB is required. Circuit simulation results in both Fig.4.6a and 4.6b) also show that any residual TX-SI, particularly SI common-mode leakage at the RX input, will introduce nonlinear distortion, thereby degrading RX linearity performance. This highlights the importance of minimizing common-mode TX-SI when designing highly linear SI mitigation circuits (both the FFC and EBD).

4.5 Conclusion

This chapter explores and models the nonlinear distortion generated at the RX input in FD transceivers. An analytical linearity model which describes the degradation of RX linearity at the antenna-air interface, due to the RX input impedance, is validated through circuit

simulation. The results predict that both differential- and common-mode SI leakage at the RX input introduce differential intermodulation distortion. The model describing the generation of common-to-differential mode nonlinear distortion can be applied to any differential circuit that has a large common-mode component. These studies are critical for understanding RX performance in the presences of strong SI and provide guidelines to minimize both common- and differential-mode SI when designing the FD radio front-end, as discussed in the next chapter.

Chapter 5

A 2.4 GHZ FULL-DUPLEX TRANSCEIVER WITH BROADBAND, LINEARITY-ENHANCED AND LONG-DELAY SPREAD SELF-INTERFERENCE CANCELLATION

In order to address the technical challenges of implementing full-duplex (FD) radios discussed in Chapter 2, this chapter presents a 2.4 GHz FD transceiver which employs multiple self-interference (SI) cancellation techniques for future wideband wireless communication [18,65]. The proposed FD radio features broadband SI suppression, cancelers calibrated for enhanced linearity, and the ability to cancel long-delay spread SI. A prototype chip is fabricated in a TSMC 40 nm CMOS process and works with a Xilinx RFSoC evaluation kit to complete the calibration loop for the radio analog front-end (AFE). The FD AFE chip integrates an electrical-balanced duplexer (EBD) with a tuned impedance matching network (Z_{Bal}), two broadband complex 5-tap continuous-time finite impulse response (FIR)-based RF cancellation filters, and a mixed-signal baseband cancellation path operating with an FPGA to complete a long-delay spread (τ=+174 ns) SI canceler. A 4^{th}-order Z_{Bal} is employed to reduce SI group delay and improves the cancellation bandwidth when used with complex filters. This work reports a measured SI suppression of 62 dB across +120 MHz bandwidth for delay spreads between 0-0.28 ns, and SI cancellation of 23 dB across +120 MHz bandwidth for delay spreads between 0.4-174 ns. The EBD achieves an enhanced common-mode rejection exceeding 55 dB through the use of a center-tap capacitor (C_{CT}) with minimal additional area. The RF canceler, calibrated by digitally-controlled current DACs, demonstrates a maximum IIP_3 of +42 dBm. The receiver has a measured noise figure of 6.8 dB and an IIP_3 of -21 dBm at the maximum gain setting of 40 dB. An integrated harmonic-rejection power amplifier (PA) achieves a measured maximum output power P_{Sat}

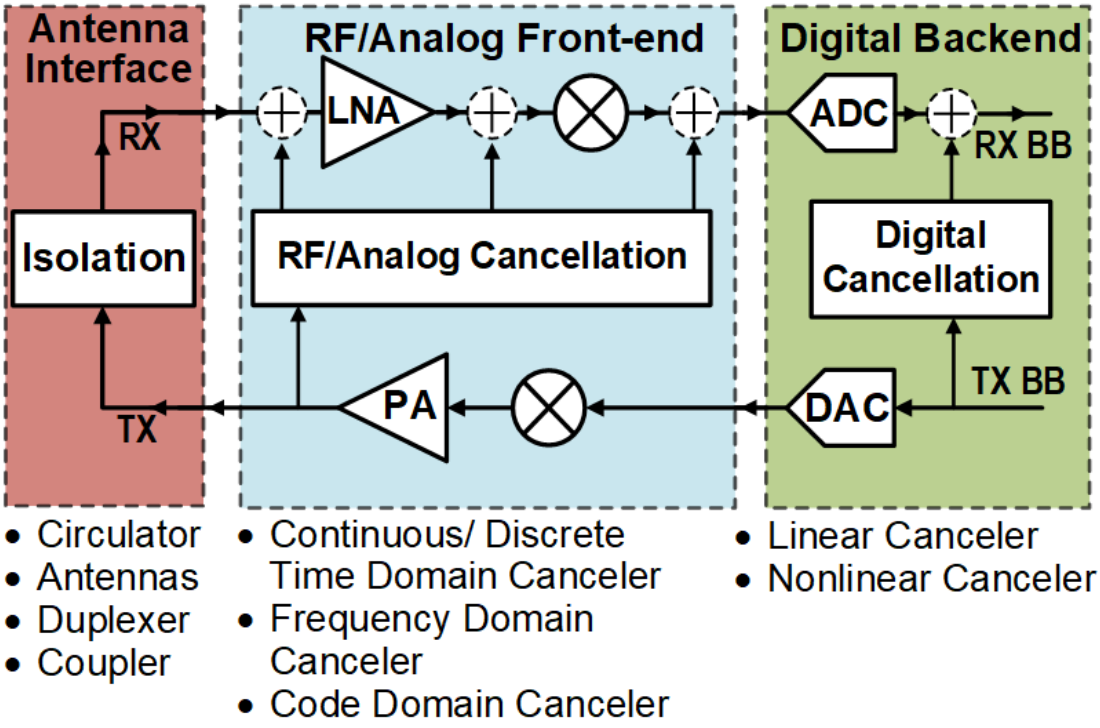


Figure 5.1: Multi-path SI suppression techniques [19–24, 26–28, 30, 33, 40–42, 46, 49, 50, 55, 66–70] distributed in a receiver.

and PAE of 19.1 dBm and 27%, respectively. The overall FD transceiver, including an integrated phase-locked loop, occupies an area of 3.2 mm^2 and consumes a total power of 373 mW/78 mW including/excluding the PA.

5.1 Introduction

The demand for higher data-rate wireless connectivity and the emergence of 5G applications, continues to motivate research on more efficient utilization of the highly congested S- and C-bands. In-band Full Duplex (FD) communication, which provides the ability to simultaneously transmit and receive on the same carrier frequency, is one technique to increase spectral efficiency and address the need for higher data rates in congested wireless networks [5, 6].

Various research efforts have made significant progress with respect to mitigating the undesired SI presented to the receiver. This includes the use of directional antenna pairs [6], integrated circulators [40–42], electrical balanced duplexers (EBD) [46,66,67], and quadrature couplers [49, 50] at the antenna interface, as well as cancellation filters [19–24, 26–28, 30, 55] in RF or analog baseband of the receiver (shown in Fig.5.1). Further SI mitigation efforts include code-domain modulation techniques [68, 69], and SI suppression at the digital back-end using linear and non-linear cancelers [33, 70]. However, there remain critical challenges to address before practical FD transceivers can be realized for commercial applications. In this work, we propose an FD transceiver with the following key contributions:

- Implementing cancelers that mitigate long-delay spread (+174 ns) SI resulting from multi-path reflections.
- Achieving broad bandwidth (+120 MHz) SI cancellation.
- Enhancing the linearity of SI cancellation circuitry.

As a key challenge surrounding the implementation of an FD transceiver relates to a wide range of SI characteristics in delay and amplitude, as described in Chapter 2, the SI cancellation networks need to cover the delay spread from hundreds of pico-seconds to hundreds of nano-seconds with varying SI strength. Delay spreads greater than hundreds of pico-seconds have been synthesized on-chip using transmission lines [71] or lumped LC delay lines [52]. However, these methods to generate delay often require a prohibitively large amount of silicon area. Recent research efforts utilize a cascade of G_m-C all-pass filters (APF) [20] or N-path switched capacitor networks [23, 24] to synthesize delays larger than $10ns$ in an FIR cancellation filter at the analog baseband. However, this implementation requires a large number of passive components and switching networks, again occupying significant silicon area. The delay and tap coefficients in the filter are tuned to match the delay and frequency response of one SI signal path. However, in real applications, SI with a longer time of flight are received in presences of multiple reflected components with a wide

range of delay spreads, which requires substantially more taps than what was implemented in [23, 24], thus, again, requiring a prohibitively large amount of silicon area. In [69], a code-domain modulation technique operates by allocating orthogonal codes to the TX and RX signal for code multiplication, which is capable of rejecting SI with a delay-spread larger than one code period. However, code multiplications spread the signal spectrum, degrading the spectral efficiency advantage promised by FD radios.

Another challenge of FD wireless systems is the constant demand for broader bandwidth solutions, thus requiring a corresponding increase in cancellation bandwidth. The maximum channel bandwidth in 802.11ax is 160MHz which is four times larger than the bandwidth in 802.11n. Finally, future 5G and 6G communication systems are increasingly using multi-carrier modulation [8] and higher TX output power which leads to one of the most challenging demands in FD radio design: the need for extremely high linearity performance in the RX analog front-end (AFE) circuitry. All the sub-carriers will generate inter-modulation distortion products as a multi-carrier modulated signal passes through the canceler, in addition to increasing the demand on the input-referred RX linearity [58].

The remainder of the chapter provides a detailed discussion on the implementation of a broadband SI cancellation network for both short- and long-delay spread SI, with a calibration method that enhances the canceler linearity. Section 5.2 describes the proposed radio AFE architecture and the role of each SI cancellation path. Section 5.3 presents detailed features of each cancellation path, which is followed by circuit implementation details in Section 5.4. Measurement results are given in Section 5.5, followed by concluding comments in Section 5.6.

5.2 In-band Full Duplex Transceiver Architecture

The proposed transceiver architecture employs multiple feed-forward cancellation (FFC) paths shown in Fig.5.2a, where each FFC path serves a different role to address a diverse set of challenges resulting from a large variation in delay spreads, amplitude, and frequency response associated with the SI. The first FFC path, at the RX air interface, uses an on-

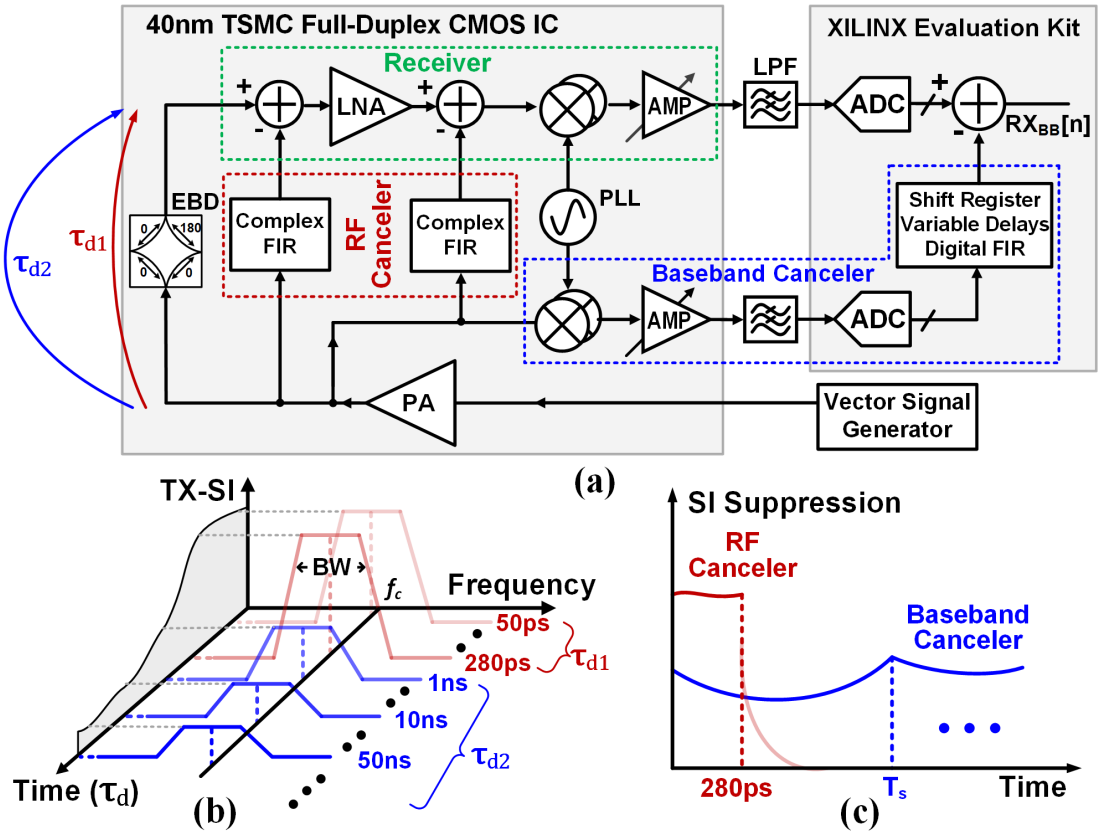


Figure 5.2: (a) Architecture diagram of proposed FD transceiver consisting of both the FD AFE chip and FPGA back-end with multiple SI cancellation paths. (b) Conceptual diagram of TX-SI amplitude with different delay spreads. (c) SI suppression provided by various cancelers in this implementation versus delay spread.

chip EBD with an integrated impedance-matching network that is digitally tuned to provide SI suppression close to the antenna, over a broad bandwidth. This is followed by both a pre- and post-LNA continuous-time FIR filter with five complex-tap coefficients, which exclusively suppress the short-delay spread SI (τ_{d1}<280 ps) arising from the direct coupling through the EBD. The pre- and post-LNA FFCs relax the linearity required of both the LNA and the subsequent RX components while reducing the reciprocal mixing products of the local oscillator (LO) phase noise with residual SI [21]. Between the two RF cancelers, the noise and linearity required of the second post-LNA canceler is relaxed as compared to the first canceler because the LNA gain will raise the RX noise floor.

The SI with a longer delay-spread (280 ps <τ_{d2}) is suppressed using a mixed-signal baseband cancellation path which derives a reference signal from the power amplifier (PA) output (Fig.5.2a). This signal is attenuated and down-converted to baseband where a variable gain amplifier (VGA) varies the reference signal amplitude before being taken off-chip and passed to the digital domain through ADCs on a Xilinx RFSoC evaluation kit. The VGA relaxes the dynamic range of the ADCs in the canceler paths as the reference signal is well-controlled from other interference. Variable delay is added to the baseband cancellation path in the digital domain through a shift register which time-aligns the reference signal to match the long-delay spread associated with numerous SI environment reflections. This mixed-signal cancellation path contains multiple-tap digital FIR filters to address a number of SI reflections, before being subtracted from the receive-signal path in the digital back-end. As the SI with a longer delay spread accrues more path loss, the required cancellation from the digital baseband begins to decrease, as illustrated in Fig.5.2c. Although challenging from a linearity perspective, using the PA output as a reference signal for cancellation has the advantage that the noise and distortion cross-products of the PA are captured, further facilitating the SI cancellation. An expanded description of each cancellation path is given in the next section.

5.3 Multi-Path Cancellation Network Features

This section discusses the three key novel contributions used on this FD radio transceiver:

- Cancellation of long delay-spread SI using a mixed-signal baseband cancellation path.
- Broadband SI suppression using an EBD with a flattened frequency response and FIR filters with complex-tap coefficients.
- Enhanced transceiver linearity by suppressing the EBD common-mode SI leakage and calibrating the canceler IP_3.

5.3.1 Mixed-Signal Baseband Cancellation Path

A mixed-signal baseband cancellation path (Fig.5.3a) was partially implemented on this chip to cancel long-delay spread SI. Previous efforts synthesized a long-delay on chip up to 130 ns using analog baseband cancelers [20,24], as shown in Fig.5.3b. However, increasing the length of the delay in the analog domain requires a number of passive components, significantly growing the size of the chip [23, 24]. This mixed-signal baseband canceler has a cascade of flip-flops which creates a digital delay line; see Fig.5.3c, while occupying negligibly small amount of silicon area as compared to an analog solution [23, 24]. The delay spread of the mixed-signal baseband canceler T_d=N/f_{clk} is primarily determined by the clock frequency (f_{clk}) and the number of flip-flops (N). A longer delay spread can be synthesized in the cancellation path by increasing the number of flip-flops, which breaks the delay-bandwidth limit described in [31]. In addition, the delay spread and the number of taps of the mixed-signal baseband canceler are significantly more programmable as compared to the equivalent analog implementation, allowing the canceler to address numerous SI reflection paths with widely varying delay spreads simultaneously, as shown in Fig.5.3c.

The mixed-signal cancellation path on this chip requires two additional ADCs (for a quadrature receiver), in addition to the receiver path ADCs, as compared to the pure-analog baseband solution [20, 24]. The dynamic range (DR) of the receiver path ADCs is set by the the residual SI power at the receiver baseband:

$$DR_{RX,ADC} = P_{TX,max} - Env_{Att} - (kT.BW.NF - 6dB) \tag{5.1}$$

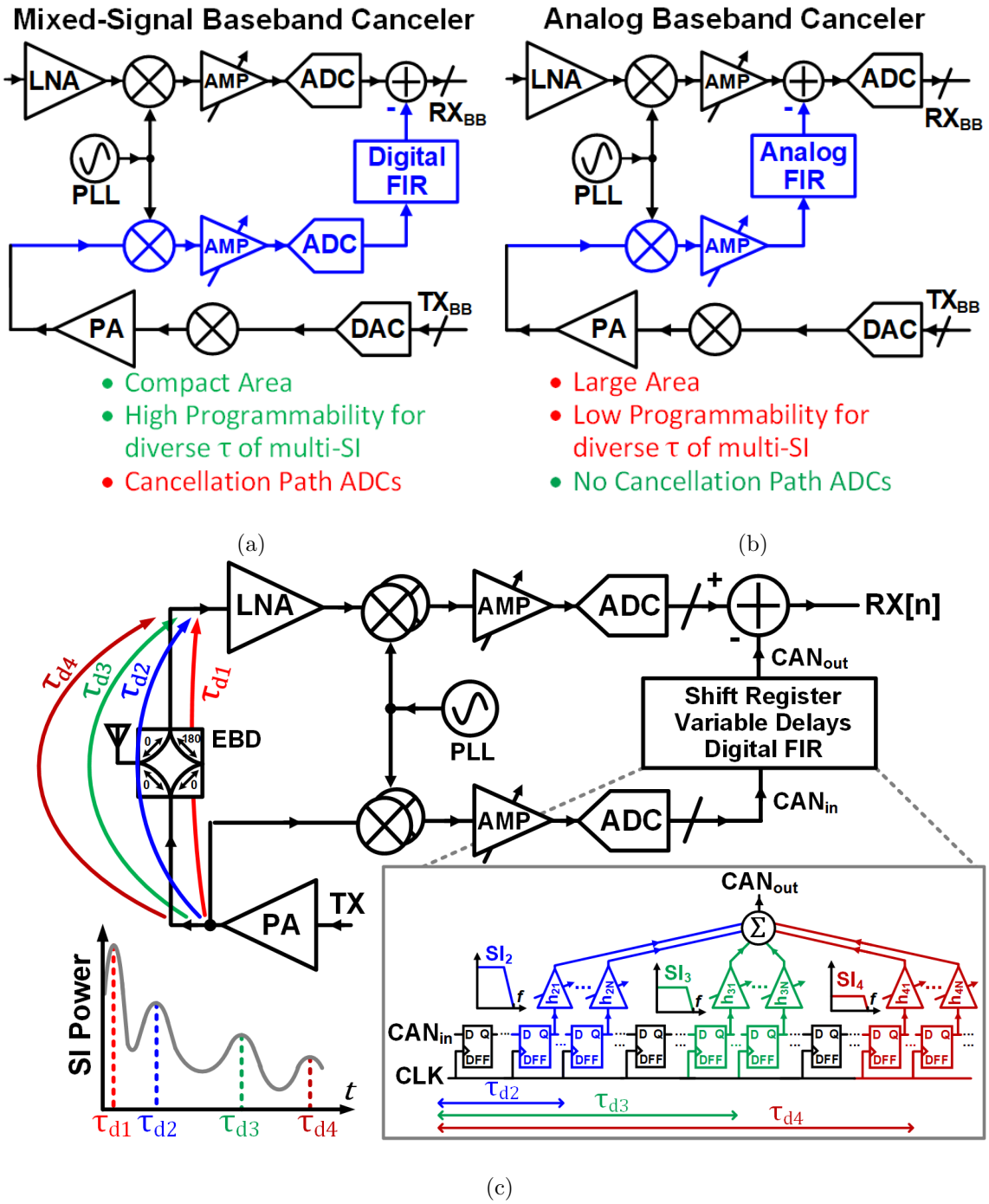


Figure 5.3: Comparison between (a) a mixed-signal and (b) a pure analog baseband canceler for long-delay spread SI cancellation. (c) Proposed mixed-signal baseband canceler to suppress multiple SI reflection paths with widely varying delay spreads (τ).

where the long-delayed SI from the environmental reflections is assumed to dominate the interference, as the direct-coupled SI is significantly suppressed by the EBD and two RF FFCs in Fig.5.2. Env_{Att} represents the attenuation of the long-delayed SI from various environmental reflections. For instance, consider a 802.11ax Wi-Fi transmitter operating with a $P_{TX,max}$ of 24 dBm [8], a 160 MHz bandwidth (BW), a 7 dB noise figure (NF), and an environmental attenuation Env_{Att} of 55 dB (from Fig.2.2a). Assuming a 6 dB margin, the calculated $\mathrm{DR_{RX,\ ADC}}$ is 60 dB. However, the required DR of the canceler path ADCs is significantly relaxed compared to the receiver path ADCs, due to the well-controlled reference signal amplitude taken from the PA output, then down-converted to baseband (Fig.5.3a). The VGAs in the canceler path adjust the reference signal amplitude, and quantization error cancellation techniques, such as the one described in [72], can be implemented at the digital back-end to mitigate the quantization noise of the canceler path ADCs, thereby relaxing their DR. While the same Xilinx RFSoC ADCs (14-bit/250 MSPS) were used for both the receiver and canceler paths in this design, custom-integrated ADCs in the canceler paths would allow lower resolution.

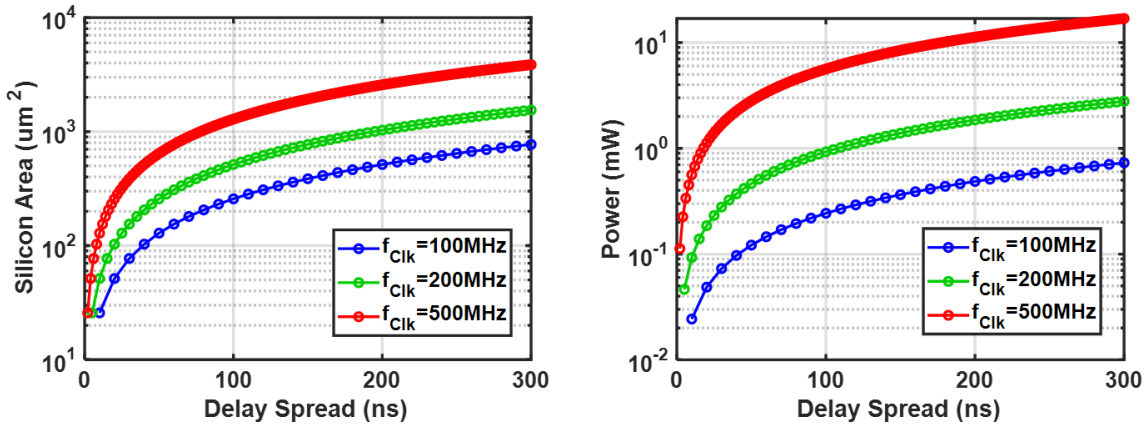
Although digital portion of the baseband canceler, which include shift registers to synthesize the long-delay spread, were not implemented with the AFE IC, their area and power consumption were estimated using Synopsys Design Compiler and Cadence Spectre tools in the 40 nm CMOS process. Fig.5.4a and Fig.5.4b show the estimated area and simulated power of the digital delay line, respectively, when the delay varies from $2n$s to 300 ns. These simulations only examine the digital delay line in the FIR filter. Clocks with different frequencies (f_{clk}=100, 200, 500 MHz) are considered for the flip-flops in the simulation. For a delay spread of $100n$s and f_{clk} of 200 MHz, the digital delay line's area and power consumption are negligibly small, which are about 500 μm^2 and 1 mW, respectively. To achieve broader bandwidth SI cancellation, the sampling frequency of the ADCs must be scaled accordingly. Assuming the same clock drives both the flip-flops in the digital delay line and the ADCs, when the signal bandwidth and f_{clk} are doubled, both the switching power and the number of flip-flops will increase by a factor of two with a constant delay spread, causing

the total power consumption of the delay line to increase by a factor of four, as illustrated in Fig.5.4b. Both the area and power consumption will improve with continued scaling to more advanced silicon technology nodes.

The cancellation performance of the mixed-signal baseband canceler is dependent on the resolution of the delay line and ADCs. A behavioral-level simulation was performed to simulate the SI cancellation of the mixed-signal baseband canceler. An eighth-order LMS-based adaptive FIR filter is implemented to match the SI in the simulation. In practice, the filter order is determined based on the SI delay spread and the delay resolution ($1/f_{clk}$) of the canceler. If the SI with multiple reflection paths exists, the filter order can be increased to achieve a broad bandwidth cancellation. Fig.5.4c shows the simulated cancellation as the SI delay varies and the same clock drives both the flip-flops (delay elements) and ADCs. The cancellation is maximized when the SI delay is a multiple of the clock period (M/f_{clk}, M=1, 2, ...). The cancellation signal, sampled at the PA output, then delayed by multiple clock periods in the flip-flops has an equal delay spread as the SI in the receiver signal path, providing maximum SI cancellation [30]. Conversely, the canceler achieves a minimum cancellation when the SI delay is half of the clock period ((M+0.5)/f_{clk}, M=1, 2, ...) where the maximum delay mismatch ($0.5/f_{clk}$) occurs. This implies that increasing f_{clk} of the flip-flops reduces the delay mismatch between the cancellation and the SI path, thus providing a more uniform suppression as the SI delay varies, which is shown in Fig.5.4c, using 200MSPS ADCs. Increasing the cancellation path ADCs resolution will also increase the cancellation depth as shown in Fig.5.4c which utilizes a pair of 12-bit ADCs with a power consumption penalty.

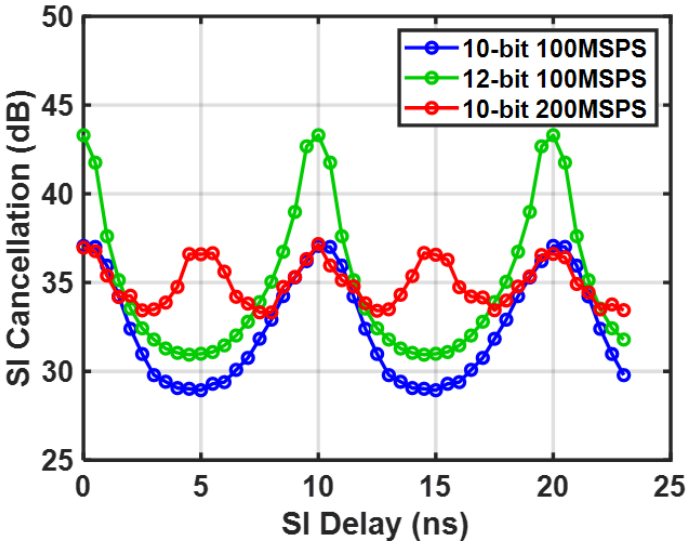
5.3.2 Broadband SI Suppression Techniques

To accommodate future wider bandwidth FD wireless systems, two techniques were applied on this chip to enhance the cancellation BW; the first of which was realized in the design of the EBD balancing impedance network (Z_{Bal}) and the second technique makes use of complex-tap analog FIR filters.



(a)

(b)

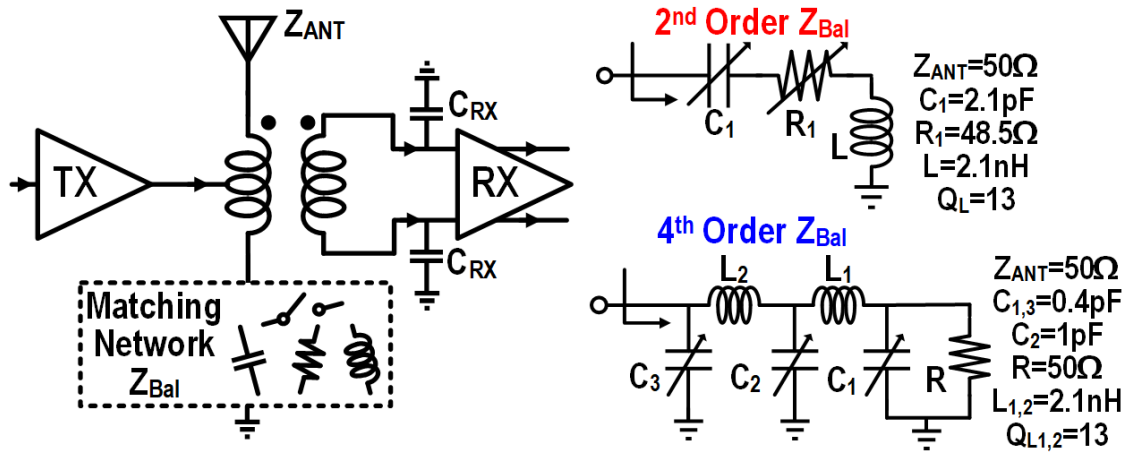


(c)

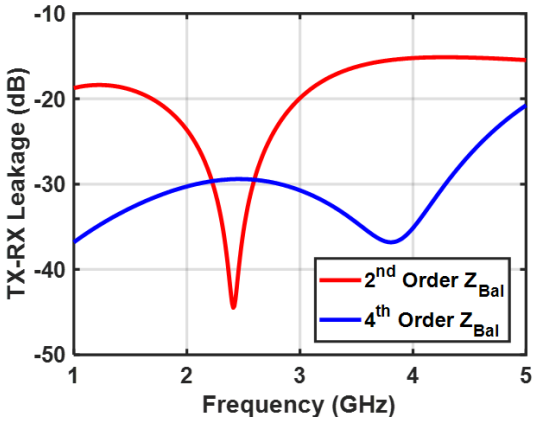
Figure 5.4: (a) Estimated area and (b) simulated power consumption of the digital delay line versus delay spread in 40 nm CMOS. (c) Simulated baseband SI cancellation with varying SI delay for different clock frequencies (f_{clk}) and ADC resolutions.

EBD with Tuned Impedance

The EBD provides SI attenuation based on the quality of the match between the Z_{Bal} in a hybrid transformer and the antenna impedance (Z_{Ant}). Previous efforts have mainly focused on increasing the SI attenuation of the EBD [46, 48]. However, the impact of the EBD frequency response, in particular the group delay variation, on the SI cancellation of the FFCs found further down the RX chain, is often overlooked. Two conventional on-chip Z_{Bal} topologies (shown in Fig.5.5a) were compared to understand their impact on the overall SI suppression. Fig.5.5b and Fig.5.5c show the simulated magnitude and group delay of the EBD TX-to-RX SI leakage, respectively. The EBD's transformer coil is modeled using PeakView's LEM tool, and a 2^{nd} and a 4^{th} order Z_{Bal} are simulated using the circuit component values shown in Fig.5.5a. As illustrated in Fig.5.5b, the magnitude response of the SI with the 2^{nd} order Z_{Bal} [59] shows a larger variation and smaller rejection bandwidth close to 2.4 GHz. This is attributed to the Z_{Bal} impedance which is rapidly varying close to the LC resonant frequency, leading to a maximum group delay of 4.5 ns, see Fig.5.5c. The large group delay makes the design of the following FFCs challenging since it requires a longer delay spread in the FFCs to match the delay of the SI leakage, which increases the area and power of the cancelers significantly. Conversely, when the 4^{th} order Z_{Bal} [73] is used, less variation is observed in the reject-band magnitude response which is desirable to achieve a wider cancellation bandwidth (Fig.5.5b). This EBD utilizes a 4^{th} order Z_{Bal} that produces two isolation resonant peaks. By utilizing phase changes near one resonant frequency to compensate for the phase response near the other resonant peak, the group delay variation from TX-to-RX ports can be minimized. From Fig.5.5c, the SI leakage group delay varies from 0.2-to-0.22 ns across a bandwidth of 200 MHz. The utilization of a 4^{th} order Z_{Bal} in this work differs from [73]. Instead of placing two isolation peaks close together to achieve a deep and narrow bandwidth TX-to-RX isolation [46] with a large group delay variation, this EBD produces two isolation peaks placed further apart in frequency, which results in a flatter frequency response with less SI rejection across a wider bandwidth. The EBD with minimal



(a)



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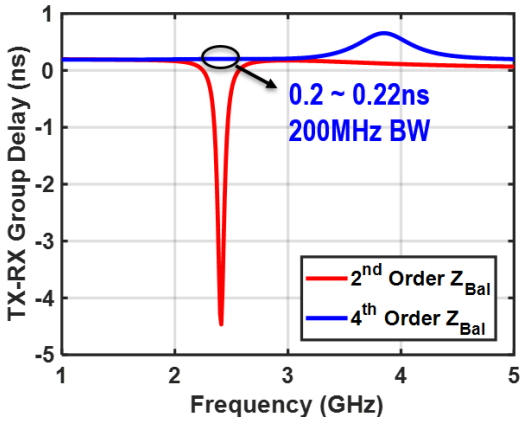


(c)

Figure 5.5: (a) EBD with two different tuned impedance networks: 2nd order Z_{Bal} [59] and 4th order Z_{Bal} [73]. Simulated (b) magnitude response and (c) group delay of EBD TX-to-RX SI leakage.

magnitude and group delay variation over the cancellation BW will facilitate matching the frequency response of the FFCs used later in the receiver chain, thus providing a deeper and broader BW SI cancellation.

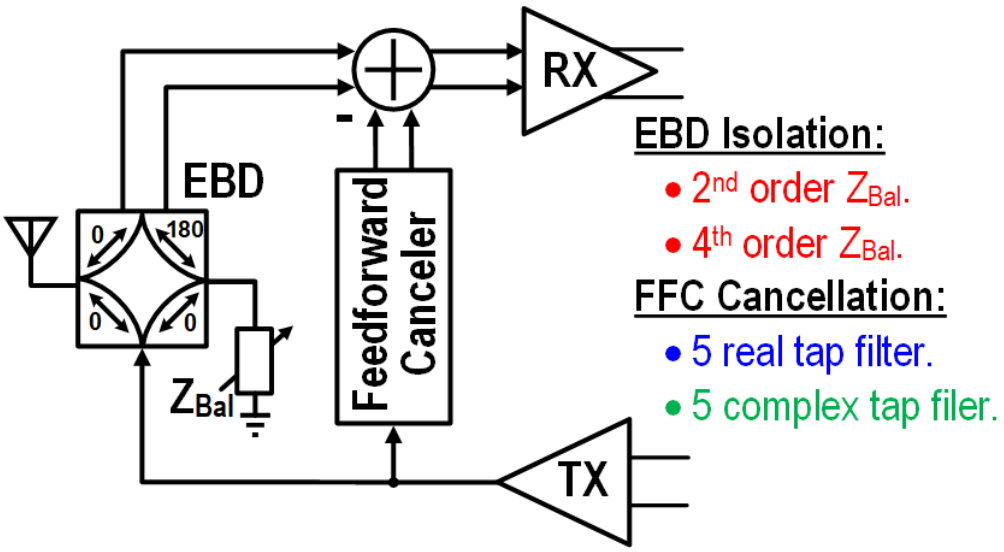
Behavioral-level simulations were conducted to evaluate the effect of Z_{Bal} on the overall SI suppression. In the simulation setup, shown in Fig.5.6a, an FFC is placed between the TX output and RX input to provide additional SI cancellation. The FFC is modeled as a five-tap FIR filter using either real-tap or complex-tap coefficients, with a $60ps$ tap delay between the filter coefficients. Fig.5.6b and 5.6c show the simulated SI suppression after both the EBD and the FFC for the case of real- and complex-tap filters using a 2^{nd} order and 4^{th} order Z_{Bal} in the EBD, respectively. For a cancellation bandwidth of 120 MHz in Fig.5.6b and 5.6c, the SI isolation provided by the EBD with the 2^{nd} order Z_{Bal} and the 4^{th} order Z_{Bal} are similar, 32 dB and 30 dB, respectively. However, notable differences are found in the cancellation of the real-tap (or complex-tap filter), where the cancellation is 8 dB (or 10 dB) when using the 2^{nd} order Z_{Bal}, which is much lower than the 20 dB (or 2 6dB) achieved with the 4^{th} order Z_{Bal}. Thus, a 4^{th} (or higher) order Z_{Bal} can flatten the frequency response of the EBD SI leakage, increasing the overall SI suppression over a broad bandwidth.

Complex-Tap FIR Filter

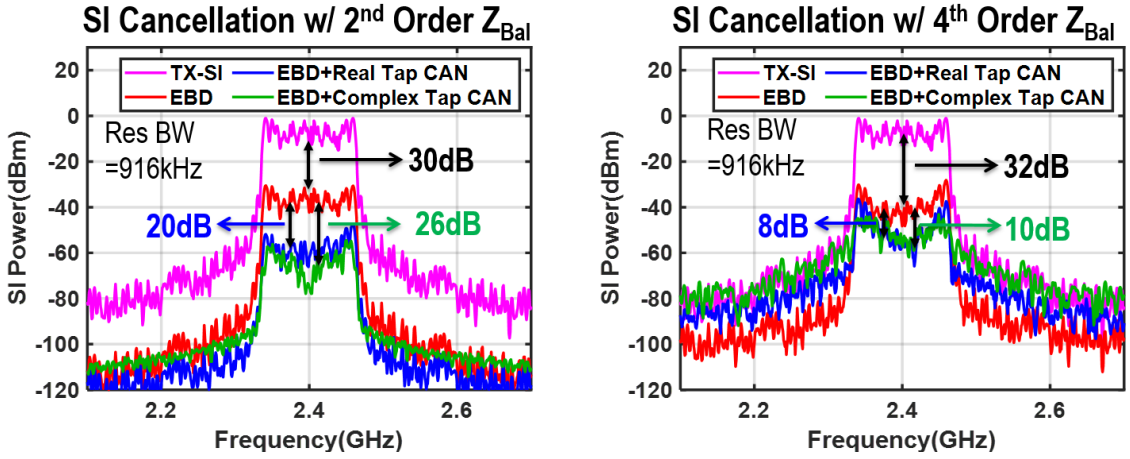
The FFCs on the transceiver chip were implemented as complex-tap analog FIR filters to further increase the SI suppression. Prior efforts have shown complex-tap filters increase the SI cancellation bandwidth while using fewer taps as compared to the real-tap filter equivalent [26]. However, this work employs complex filter taps to better match group delay variations across the band of interest. Assuming the SI leakage has a constant attenuation of H_0 and group delay of τ_{d0} across the cancellation band, the time- and frequency-domain SI leakage can be expressed as:

$$x_{SI}(t) = H_0.x_{TX}(t - \tau_{d0}) \tag{5.2}$$

$$X_{SI}(\omega) = H_0.X_{TX}(\omega).e^{-j\omega\tau_{d0}} \tag{5.3}$$



(a)



(b) (c)

Figure 5.6: (a) Behavioral-level simulation diagram with the EBD isolation and the FFC cancellation prior to the RX input. Simulated spectrum after EBD suppression and real-tap or complex-tap FFC cancellation with the (b) 2^{nd} order and (c) 4^{th} order Z_{Bal}.

The cancellation signal at the output of a true-time delayed real-tap FIR filter is expressed as (3.2). Assuming the constant group delay (τ_{d0}) remains within the total delay of the cancellation filter and the filter tap delay is less than $\frac{1}{2f_{sig}}$ [5], an FIR filter with real coefficients is able to reconstruct the leakage SI by adjusting the w_k. However, the SI group delay will vary with a nonlinear phase response as is found at the RX air interface. As illustrated in Fig.5.5c, the group delay of the EBD TX-to-RX SI leakage has a variation of 10% across the band, although a 4$^{\text{th}}$ order Z_{Bal} is used to flatten the SI frequency response. Other SI direct coupling from the chip, board substrate, and antenna reflections also impact the group delay profile within the channel bandwidth [20]. If there is a frequency-dependent group delay $\tau_d(\omega)$, a modification to (5.3) must be made as:

$$X_{SI}(\omega) = H_0.X_{TX}(\omega).e^{-j\omega\tau_d(\omega)} \tag{5.4}$$

As discussed in Chapter 3, the frequency-dependent group delay or nonlinear phase phase shift $\theta(\omega)$ of SI leakage in (3.6) can be addressed with an FIR filter that has complex-tap coefficients capable to match $\theta(\omega)$ by rotating the phase of the cancellation signal (θ_{can}) independent of the delay, thus increasing both the bandwidth and depth of the SI cancellation.

Fig.5.7 shows a comparison between the simulated SI cancellation depth versus bandwidth for a real 5-tap FIR filter and a complex 5-tap FIR filter. The 4$^{\text{th}}$ order Z_{Bal} described in Fig.5.5a is applied to the EBD to model the SI leakage. The FFC with complex-tap coefficients increases the SI cancellation by 6 dB for a bandwidth of 120 MHz. A complex-tap FIR filter ideally provides an equal phase shift (θ_{can}) to all frequencies within the bandwidth. However, the SI might present different phase shifts ($\theta(\omega)$) at different frequencies. As such, the complex-tap FIR filter matches the SI more closely, thus increasing the cancellation depth more notably than a real-tap FIR filter equivalent when the signal bandwidth is small, as shown in Fig.5.7. Note that complex-tap FIR filters also improve the cancellation depth and bandwidth relative to other air interface solutions such as a circulator and two antennas that have non-uniform group delays as the SI passes through these components.

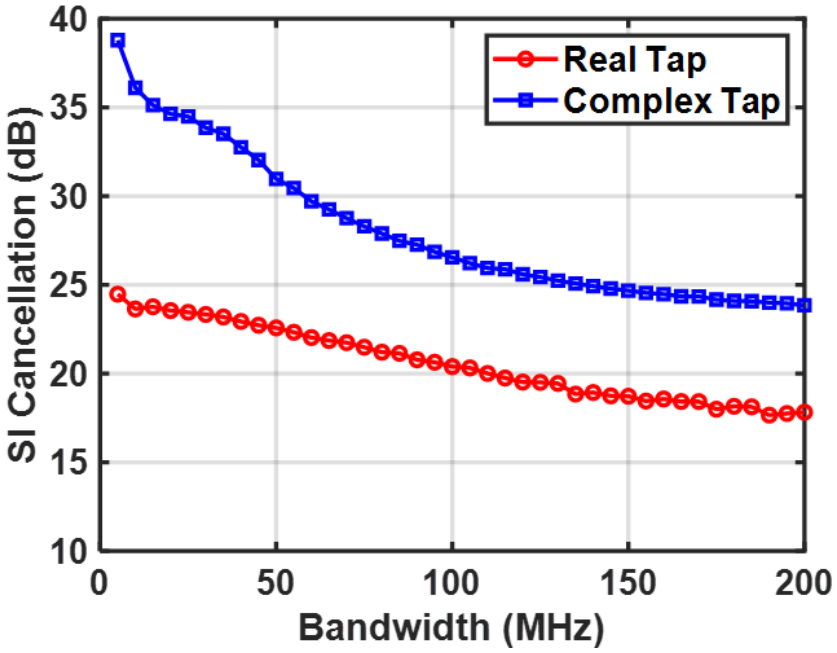


Figure 5.7: Simulated SI cancellation depth versus signal bandwidth derived from a behavioral-level model used for the comparison of a 5-real tap FIR and 5-complex tap FIR filter.

5.3.3 Suppression of the EBD Common-Mode SI Leakage

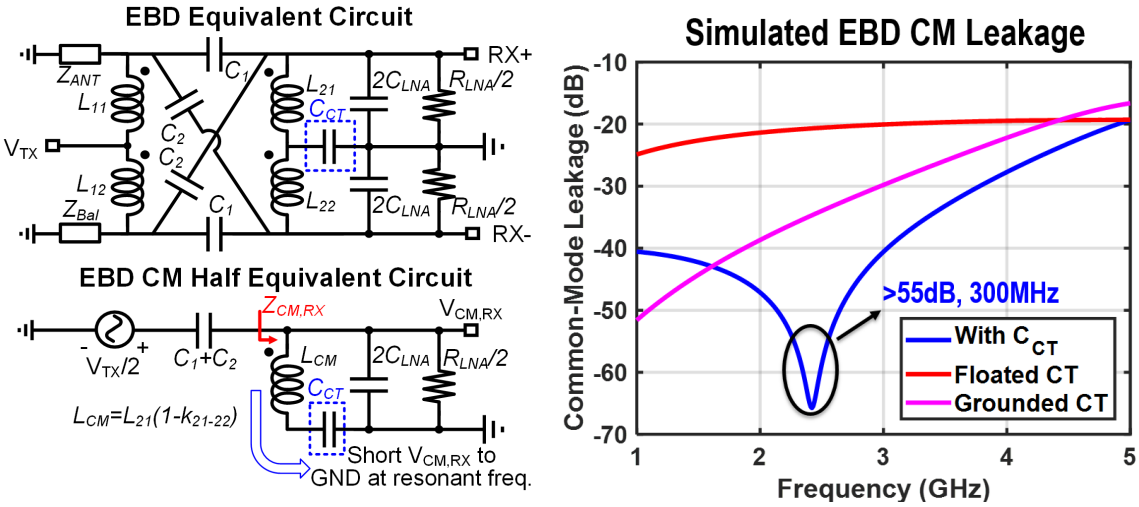
To accommodate a PA delivering multi-carrier signals with a large voltage swing, the linearity of the SI suppression circuitry between the TX output and the RX input is critical. Because both the EBD and FFCs derive their input signals from the PA output, the linearity of the EBD becomes as critical as in the case of the FFCs. As such, every effort was made to enhance the EBD linearity. Stacked switches were used in prior Z_{Bal} [46, 47] to enhance the TX-to-ANT and ANT-to-RX IIP_3 of the EBD. The proposed approach used for this EBD implementation focuses on minimizing the distortion generated at the RX input from the EBD common-mode leakage modulating the nonlinear RX impedance [58]. The capacitive coupling between the primary and the secondary transformer coils of an EBD results in strong

common-mode SI coupling to the RX input (Fig.4.2). As described in [58], the common-mode SI leakage can cross-modulate with the differential-mode SI, generating differential inter-modulation products at the RX input, as shown in Fig.4.2. The resulting differential IM_3 was described from (4.6) in Chapter 4:

$$IM_{3,DIF} = \frac{3}{4}(2L_{dif}^3 + 6L_{cm}^2 L_{dif})A_i^3 \tag{5.5}$$

where L_{cm} and L_{dif} are common- and differential-mode TX-to-RX leakage, and A_i is the amplitude of EBD input current (i_{in} shown in Fig.4.2). An EBD with common-mode isolation larger than 50 dB is required for sufficient linearity performance in FD radios intended for use in Wi-Fi transceivers [58]. A fully differential EBD [74] or an EBD with a single-ended output [46] has been proposed in prior efforts to mitigate the common-mode leakage. However, these topologies [46, 74] are realized at the expense of either an increased silicon area or higher even-order harmonic distortion.

The SI common-mode rejection is further enhanced in the proposed design by creating a common-mode short circuit to ground through a center-tap capacitor placed at the EBD secondary coil. If Z_{Bal} is equal to Z_{Ant}, the EBD equivalent common-mode half-circuit can be simplified as shown in Fig.5.8a. When the center-tap capacitor resonates out the common-mode inductance ($\omega = 1/\sqrt{L_{CM}C_{CT}}$), the RX common-mode input impedance looks like a short to ground, effectively eliminating the SI common-mode coupling. The EBD implemented on this chip has a strong coupling factor (k_{21-22}) between L_{21} and L_{22}, thus leading to a small inductance for L_{CM}. The low quality factor of the series LC resonant circuit in Fig.5.8a provides a high common-mode SI rejection across a broad bandwidth. This obviates the need to tune C_{CT} across the band of interest, thus requiring switches that will degrade the EBD linearity. The simulated EBD common-mode rejection is compared with two other prior methods: an EBD with a floated center tap [66] in the secondary transformer coil, and an EBD with a grounded center tap [67] in the secondary transformer coil, shown in Fig.5.8b. Adding C_{CT} enhances the EBD common-mode isolation by greater than 20 dB as compared to prior art [66, 67], achieving a common-mode isolation larger than 55 dB across



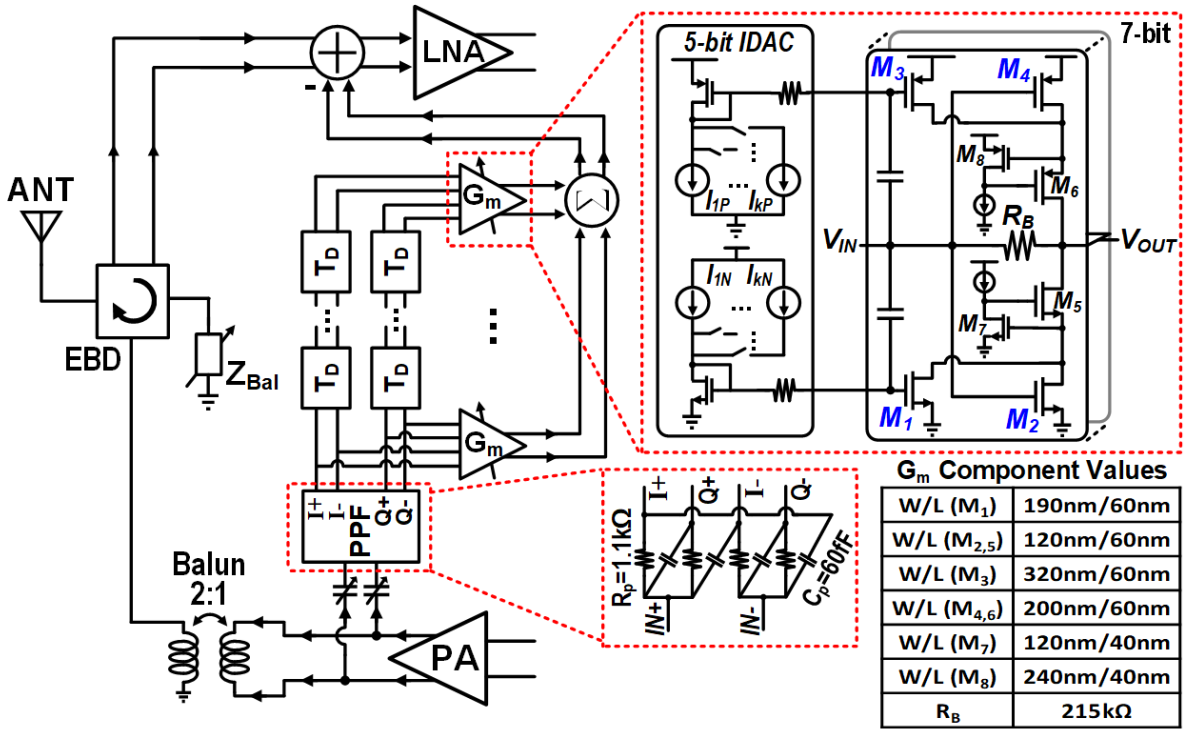
(a) (b)

Figure 5.8: (a) EBD equivalent circuit with C_{CT} and EBD common-mode half equivalent circuit under an impedance matched condition. (b) Simulated EBD common-mode SI Leakage for different center-tap approaches.

300 MHz bandwidth. If the EBD layout has excellent symmetry, which is not difficult to achieve, then C_{CT} will have minimal impact on the amplitude and phase imbalance of the differential signal at the RX input. When C_{CT} is used for the center tap, the simulated amplitude and phase imbalance are less than 0.7 dB and 6 degrees, respectively, between 2.2-2.5 GHz.

5.3.4 Feed-forward Canceler Linearity Calibration

A complex-tap analog FIR filter implements the RF FFC which consists of a passive poly-phase filter (PPF), passive delay cells, and an array of variable gain trans-conductance (G_m) stages (Fig.5.9). Any inter-modulation products generated along the cancellation path are summed and injected into the RX signal path with the cancellation signal, thus the importance of realizing a highly-linear FFC. The transistors used to implement the G_m



G_m Component Values

W/L (M_1)	190nm/60nm
W/L ($M_{2,5}$)	120nm/60nm
W/L (M_3)	320nm/60nm
W/L ($M_{4,6}$)	200nm/60nm
W/L (M_7)	120nm/40nm
W/L (M_8)	240nm/40nm
R_B	215kΩ

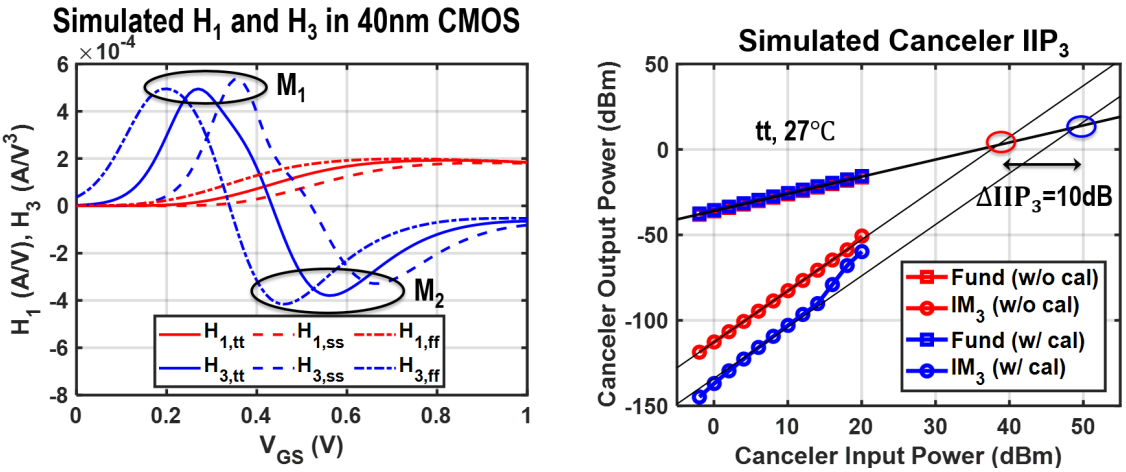
Figure 5.9: Transistor-level implementation of the 5 complex-tap FIR-based FFC.

stages and adjust the filter coefficient values serve as the linearity bottleneck for the entire FFC signal path. To reduce the IM_3 distortion, a linearity calibration method is employed in the G_m stage to enhance the filter's linearity performance. .

The drain current of a common source (CS) G_m stage can be modeled using Volterra series where up to the third order is shown as:

$$i_d = H_1(\omega_{p1}) \circ v_{in} + H_2(\omega_{p1}, \omega_{p2}) \circ v_{in}^2 + H_3(\omega_{p1}, \omega_{p2}, \omega_{p3}) \circ v_{in}^3 \tag{5.6}$$

The dependence of 3rd order nonlinear coefficient $H_3(\omega_1, \omega_1, -\omega_2)$ on the gate-source voltage V_{GS} was used to reduce the IM_3 in [75, 76]. Fig.5.10a shows the extracted $H_1(2\pi f_1)$ and $H_3(2\pi f_1, 2\pi f_1, -2\pi f_2)$ of an NMOS transistor (W/L=120nm/60nm) over different process corners in a 40 nm CMOS technology using the Cadence Spectre RF Harmonic Balance analysis tools. f_1 and f_2 are chosen to be 2.4 GHz and 2.41 GHz in the simulation, respectively.



(a) (b)

Figure 5.10: (a) Simulated $H_1(2\pi f_1)$ and $H_3(2\pi f_1, 2\pi f_1, -2\pi f_2)$ versus V_{GS} of a NMOS transistor in a 40 nm CMOS process. (b) Simulated IIP_3 of the FFC post-calibration using the typical process corner and at 27°C.

A transistor (M_1) in the G_m stage (Fig.5.9) can be sized and biased in the subthreshold region which produces a positive H_3 (Fig.5.10a). When M_1 is placed in parallel with transistor M_2 biased in the saturation region, with a negative H_3 (Fig.5.9 and Fig.5.10a), the total third order non-linearity and the resulting IM_3 of the G_m stage can be reduced. Fig.5.10b shows the simulated IIP_3 of the FFC using the typical process corner. One observes the IIP_3 improves by 10 dB post calibration. The gate voltage of both the auxiliary NMOS (M_1) and PMOS (M_3) can be digitally controlled using I-DACs in Fig.5.9 to maximize the canceler's linearity performance over process and temperature variations. This differs from approaches described in [75, 76]. The linearity calibration technique enhances the IIP_3 of the FFC by more than 9 dB in all process corners over a temperature range from -40°C to 100°C.

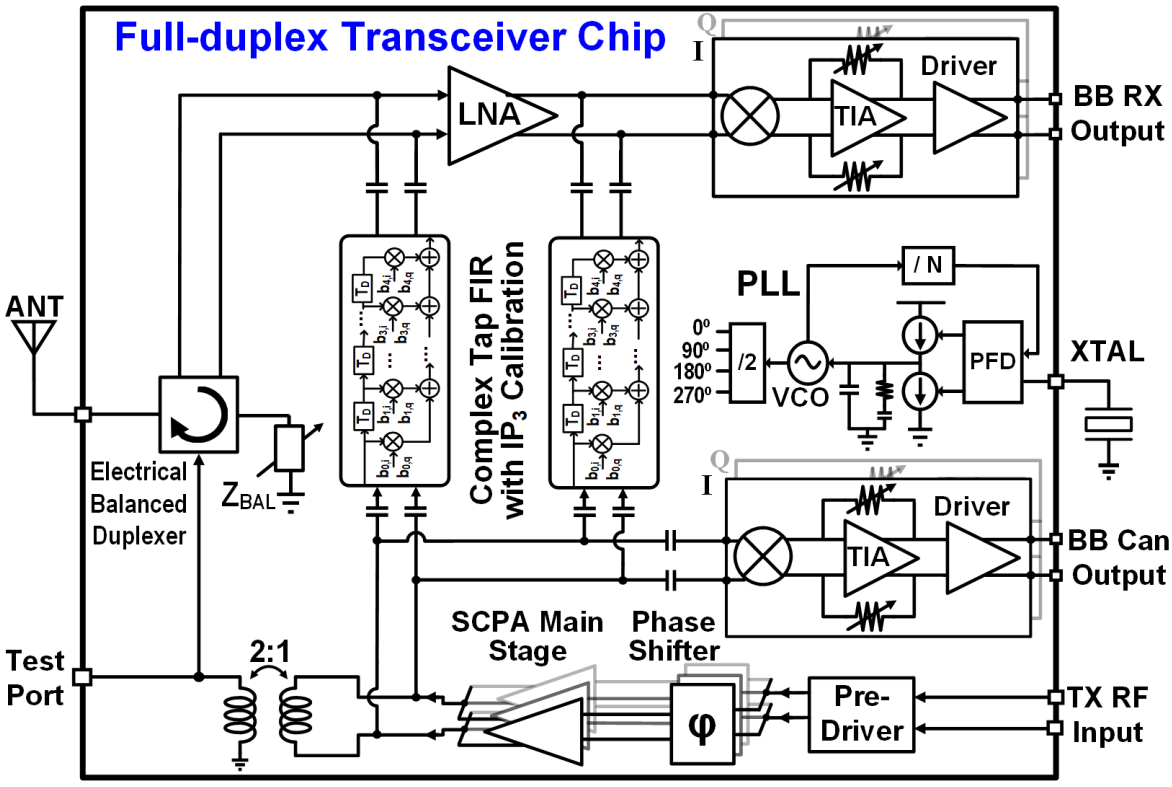


Figure 5.11: Block diagram of the FD transceiver AFE IC.

5.4 FD AFE Circuit Implementation

Fig.5.11 shows the block diagram of the FD transceiver AFE chip. An EBD with Z_{Bal}, two RF FFCs, and the analog portion of the baseband cancellation path are integrated on the chip with an RX chain from the LNA input to the analog baseband output, an integrated harmonic-rejection PA, and a phase-locked loop (PLL).

5.4.1 Complex-Tap RF Feed Forward Canceler

The two RF FFCs used on this chip are implemented as 5-tap true-time delay analog FIR filters with complex coefficient values (Fig.5.9) as described in the aforementioned section to achieve a deeper SI cancellation over a broader bandwidth. The inputs to the FFCs are

connected to the PA output which has an R_{opt} of about 6.25 Ω transformed by a matching network. The PA output (primary coil of the balun shown in Fig.5.9) has a smaller voltage swing as compared to the secondary coil, improving the canceler's input-referred linearity. A capacitive divider first attenuates the PA output signal at the FFC input and then a Type-II RC passive PPF [77] generates differential signals with quadrature phases that are then passed through a passive delay line. The delay line was implemented as an RC-CR APF with a maximum delay of each stage of 68 ps. A Class-AB push-pull buffer is placed between each delay stage to prevent the loading of the previous stage which helps to increase the delay line bandwidth and linearity. Signals with different delays are complex-weighted by 7-bit digitally-controlled Cartesian G_m stages which set the value of the filter coefficients. A regulated cascode is used in the G_m stages to improve the canceler's output impedance and the linearity. The canceler's linearity is further enhanced by independently tuning the gate voltage of M_1 and M_3 using 5-bit I-DACs (Fig.5.9), where current tuning was found to be superior to calibrating the gate voltage to compensate for devices variations. The added biasing and auxiliary circuits have negligible impact on the overall power consumption (<1.5 mW) and noise, since they operate in the subthreshold region. The outputs of each G_m stage are summed in current domain before being injected as a cancellation current at the RX input. The canceler presents a high-input ($R_{in} \approx 2.2k\Omega$) and output impedance ($1k\Omega < R_{out}$) to minimize the effect of loading the PA output and reduce the impact on LNA/RX S_{11}.

The total delay spread of the proposed RF complex 5-tap FIR filter is about 0.28 ns. In practice, when the SI delay with relatively high power (Fig.2.2a) exceeds the delay spread of the RF canceler, the complex-tap FIR filter behaves similarly to a vector modulator [19, 51]. Fig.5.12 shows the simulated SI cancellation of one RF canceler with a 120 MHz modulated signal. While the achievable SI cancellation decreases as the SI delay spread increases, the cancellation does not drop suddenly after an SI delay of 0.28 ns. Instead, it follows a more gradual roll-off. The canceler, with a total delay spread of 0.28 ns, still provides about 10 dB of cancellation when the SI delay spread exceeds 3 ns. Methods to increase the delay spread of the RF canceler will be presented in the next chapter.

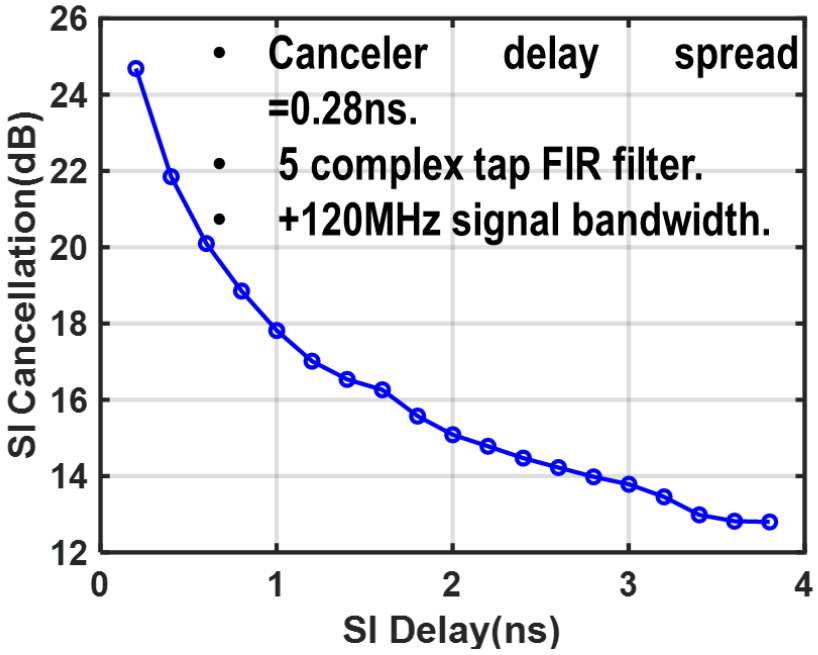


Figure 5.12: Simulated SI cancellation of the complex tap filter (Fig.5.9) versus SI delay spread using the behavioral-level model from Fig.5.6a.

The one-stage passive PPF used in the complex-tap FIR filter (Fig.5.9) contributes a non-negligible IQ phase error dependence on PVT variations [78]. Fig.5.13a shows the simulated IQ phase error of the one-stage PPF versus frequency, where a phase error of more than 25° can be observed over PVT variations. Fig.5.13b is an illustration showing one normalized 3-bit (n=3) Cartesian G_m stage with a phase error θ of 25° to cancel the SI leakage. When the θ increases, each constellation point of the canceler rotates, and the region defined by all the constellation points changes from a square to a diamond shape, as shown in Fig.5.13b. A method similar to [51] is utilized to analyze the impact of the phase error on SI cancellation. The cancellation range of the complex one-tap filter is determined by the radius (r_{max}) of the largest circle (the red circle in Fig.5.13b) within the diamond region defined by the

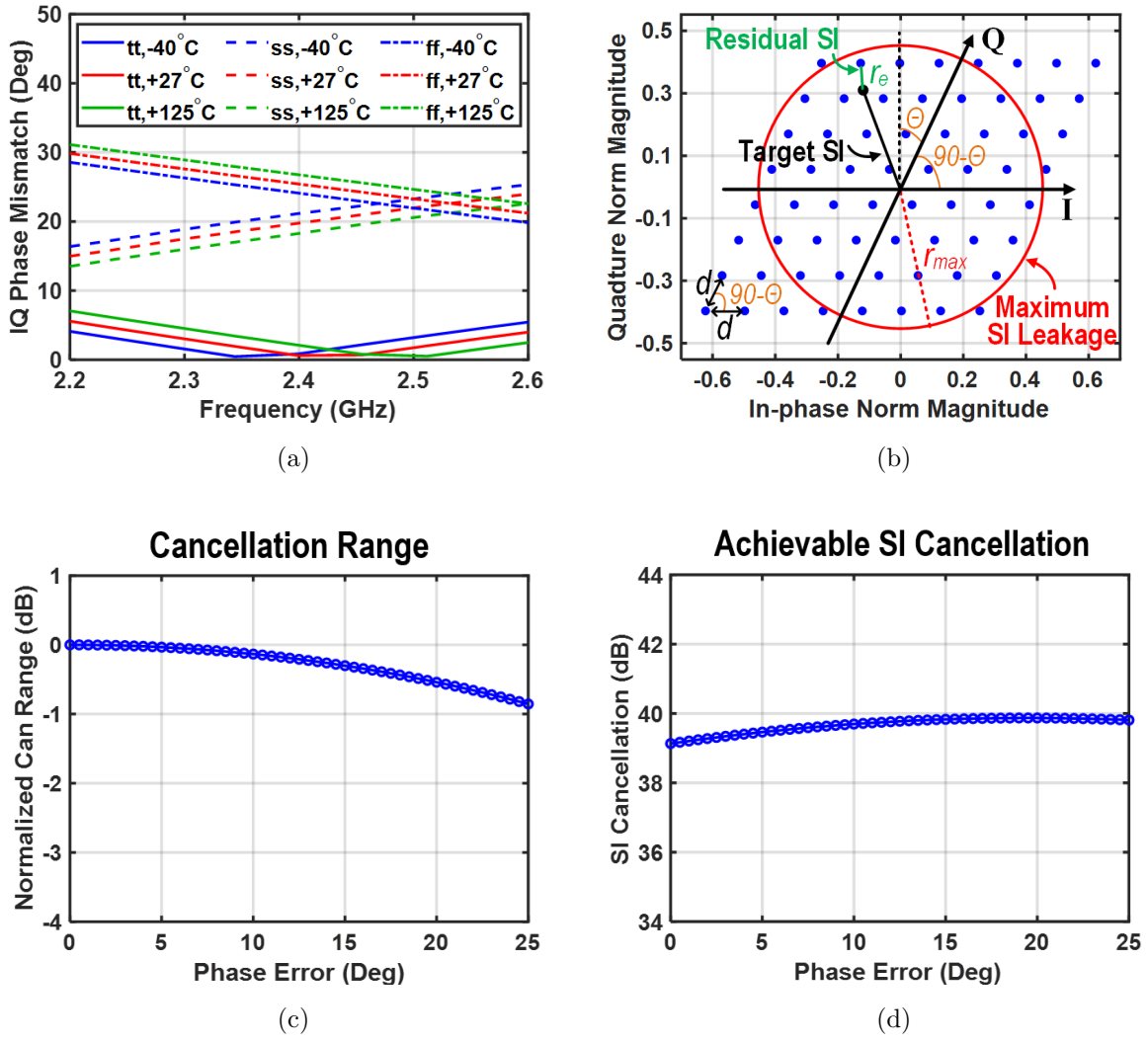


Figure 5.13: (a) Simulated phase error of a one-stage passive PPF in Fig.5.9 over PVT variations. (b) An illustration showing the use of a 3-bit Cartesian G_m stage to perform SI cancellation. (c) Normalized cancellation range and (d) achievable SI cancellation at one frequency point as a function of the phase error of a 7-bit Cartesian G_m stage.

constellation points, which can be calculated as:

$$r_{max} = 2^n d \cdot cos((90-\theta)/2) \cdot sin((90-\theta)/2) \tag{5.7}$$

where $0°<\theta<90°$ is assumed, and d represents the spacing between neighbouring constellation points along the I/Q axis (shown in Fig.5.13b). When performing SI cancellation, the closest constellation point to the target SI is chosen, and some residual SI (the green vector in Fig.5.13b) remains. The maximum residual SI occurs when the target SI is right at the center of three constellation points and its amplitude (r_e) can be calculated as:

$$r_e = d \cdot \frac{sin(\theta/2)}{sin(\theta)} \tag{5.8}$$

Then, the achievable SI cancellation of the n-bit Cartesian G_m stage with phase error θ at one frequency is:

$$SIC(dB) = 20 \cdot log_{10}(r_{max}/r_e) \tag{5.9}$$

Fig.5.13c and Fig.5.13d show the impact of the phase error θ on the normalized cancellation range ($\frac{r_{max}(\theta)}{r_{max}(0)}$) and the achievable SI cancellation, respectively, for a 7-bit Cartesian G_m stage which is used to implement the FFC (Fig.5.9) in this design. The cancellation range decreases by less than 1 dB with a phase error of 25° (Fig.5.13c). This can be tuned out by reducing the attenuation of the tunable attenuator at the FFC input (Fig.5.9), but it would degrade the canceler linearity. The achievable SI cancellation improves slightly when the phase error increases, as the residual SI amplitude (r_e) also decreases with the reduced cancellation range. Further behavioral level simulations were performed with the complex 5-tap filter using the simulation diagram in Fig.5.6a and the SI cancellation for a 120 MHz modulated signal varies by less than 1.5 dB, when increasing the phase error from 0-30°, as shown in Fig.5.14.

5.4.2 On-Chip Tuned Z_{Bal} for the Electrical-Balanced Duplexer

Fig.5.15a shows the detailed implementation of the Z_{Bal} in the EBD which consists of one fixed polysilicon resistor, one inductor, and three identical tunable capacitor banks. A

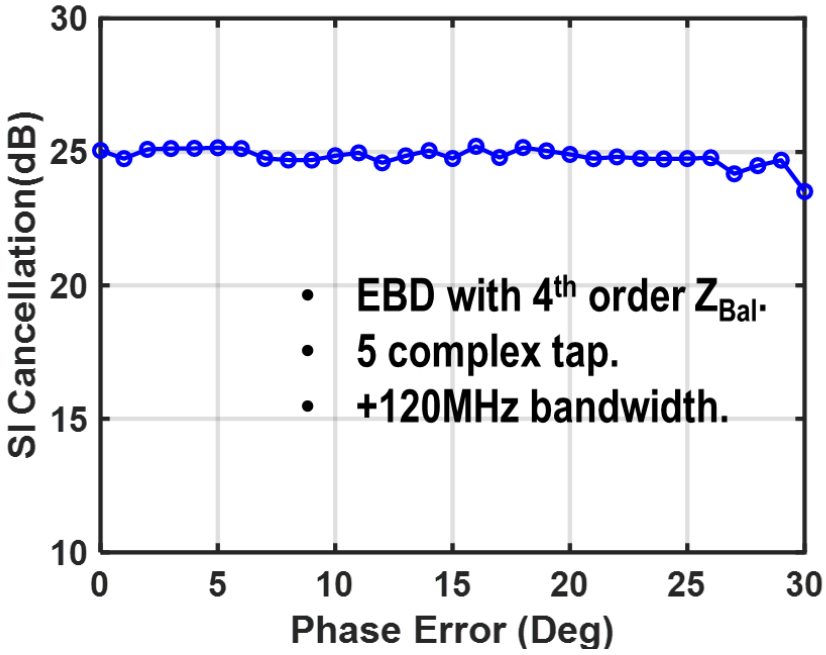
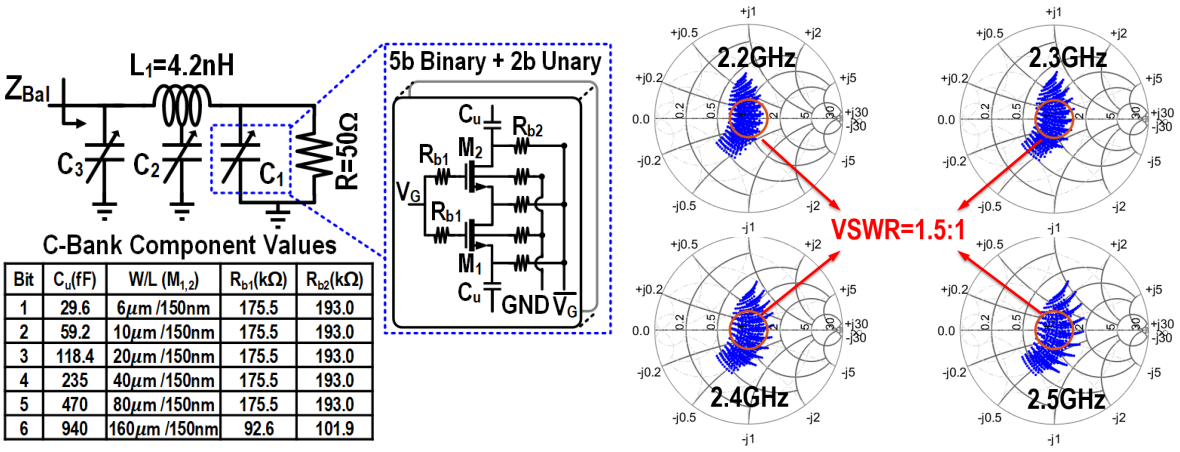


Figure 5.14: Simulated SI cancellation of the complex tap filter versus phase error using the behavioral-level model from Fig.5.6a.

fixed 50Ω resistor with an area occupying 80 $\mu m \times 60\ \mu m$ is used to avoid potential electro-migration issues [46] and linearity degradation of the EBD [79] when the input signal power is high. The integrated inductor has a DC inductance of 4.2 nH with a quality factor of 14 at 2.4 GHz. A tunable capacitor bank is placed between the center tap of the inductor and ground, which effectively realizes a 4^{th} order Z_{Bal} while minimizing the area compared to the work in [73]. The tunable capacitor bank consists of 7-bit switched capacitor cells shown in Fig.5.15a, where the five least significant bits (LSB) are binary coded and the two most significant bits (MSB) are thermometer coded. Each switched capacitor cell includes two unit Metal-Oxide-Metal (MOM) capacitor and two stacked thick-oxide NMOS transistors in order to sustain the large voltage swing of the TX output signal. The segmented coded switched-capacitor cells and the sizing parameters shown in Fig.5.15a ensure the capacitance increases monotonically as the code increases. Each capacitor bank has a tuning range of



Bit	C_u(fF)	W/L ($M_{1,2}$)	R_{b1}(kΩ)	R_{b2}(kΩ)
1	29.6	6μm /150nm	175.5	193.0
2	59.2	10μm /150nm	175.5	193.0
3	118.4	20μm /150nm	175.5	193.0
4	235	40μm /150nm	175.5	193.0
5	470	80μm /150nm	175.5	193.0
6	940	160μm /150nm	92.6	101.9

(a) (b)

Figure 5.15: (a) Transistor-level implementation of the Z_{Bal}. (b) Simulated VSWR of the Z_{Bal} after parasitic extraction.

0.3-2 pF, limited by the parasitic capacitance of the off switches (C_{OFF}) [46, 47]. The simulated impedance tuning range of the Z_{Bal} for a 9×9×9 coarse tuning between 2.2-2.5 GHz is shown in Fig.5.15b and a VSWR of 1.5 is achieved. Fig.5.16a-5.16d show the simulated Z_{Bal} impedance tuning range across different processes (tt, ss, ff) and temperatures (-40, 27, 125 ℃) within the frequency range of 2.2-2.5 GHz. The parasitic extraction simulation results indicate that the VSWR of the 4th order Z_{Bal} ranges from 1.2 to 1.8 across all PVT corners, which eliminates the need for additional PVT mitigation circuits.

A 24 pF MOM capacitor shorts the center tap of the EBD's secondary coil to ground (Fig.5.18), minimizing the TX-to-RX SI common-mode leakage. This capacitor occupies a minimal area of 0.0064 mm^2, which is much smaller than the differential EBD [74] used to enhance the common-mode rejection. Due to the symmetric layout of the EBD in this design, the proposed C_{CT} has minimal impact on the amplitude and phase imbalance of the differential signal at the receiver input. Simulations were performed using the Lorentz Solution PeakView EM simulation tool to analyze these effects, accounting for all metal

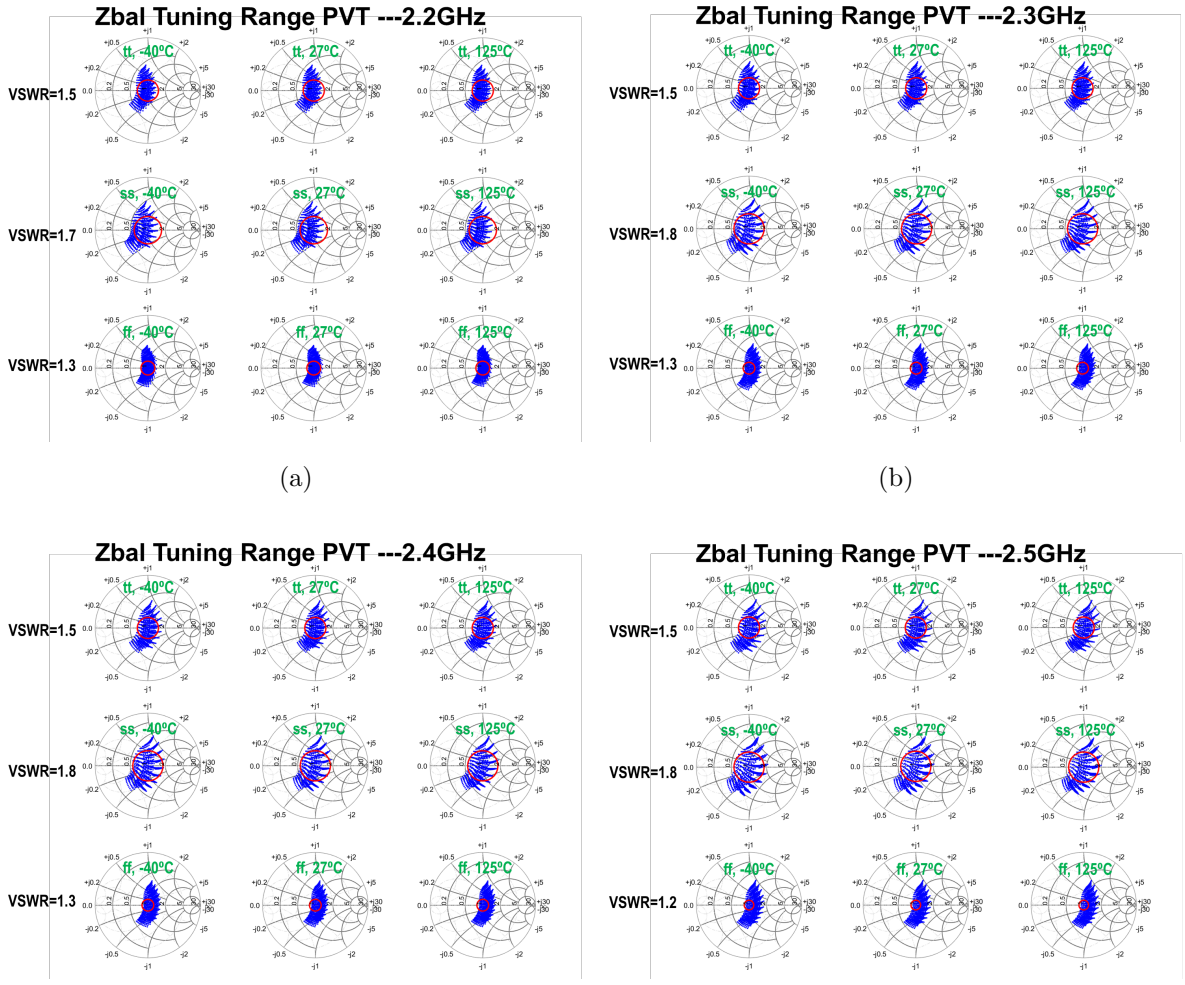
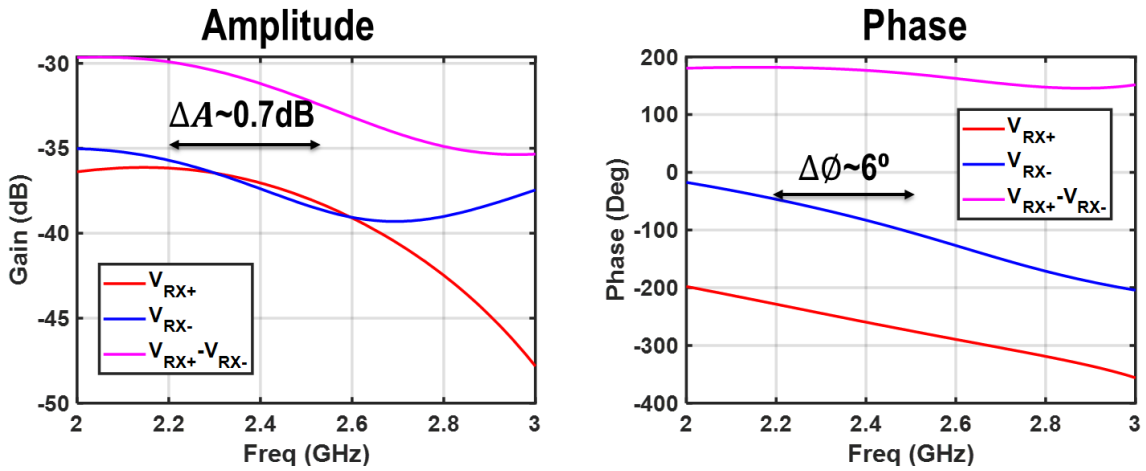


Figure 5.16: Simulated VSWR of the Z_{Bal} after parasitic extraction across different PVT corners between 2.2-2.5 GHz.



(a) (b)

Figure 5.17: Simulated (a) amplitude and (b) phase imbalance of the EBD with C_{CT}.

interconnects to the differential receiver input and the connection to C_{CT}. The simulation results show the amplitude imbalance of the differential signal is less than 0.7 dB (Fig.5.17a), and the phase imbalance remains below 6 degrees (Fig.5.17b) within the frequency range of 2.2-2.5 GHz.

5.4.3 Power Amplifier

The FD AFE chip integrates a harmonic-rejection PA. The input signal from an external signal generator to the PA is first amplified by a pre-driver stage (Fig.5.18). The signal passing through three parallel phase shifters have phase differences of 0°, 45°, 90° which are then combined by the switch-capacitor PA main stage at the PA output [80], with gain ratios of about 1, $\sqrt{2}$, and 1. As illustrated in Fig.5.18, this gain and phase configuration effectively suppresses the possibility of producing distortion from the PA's 3rd and 5th order harmonics inter-modulating as they pass through the FFC, resulting in counter 3rd-order inter-modulation (CIM_3 [81]) that falls in the RX signal band. Each phase shifter contains

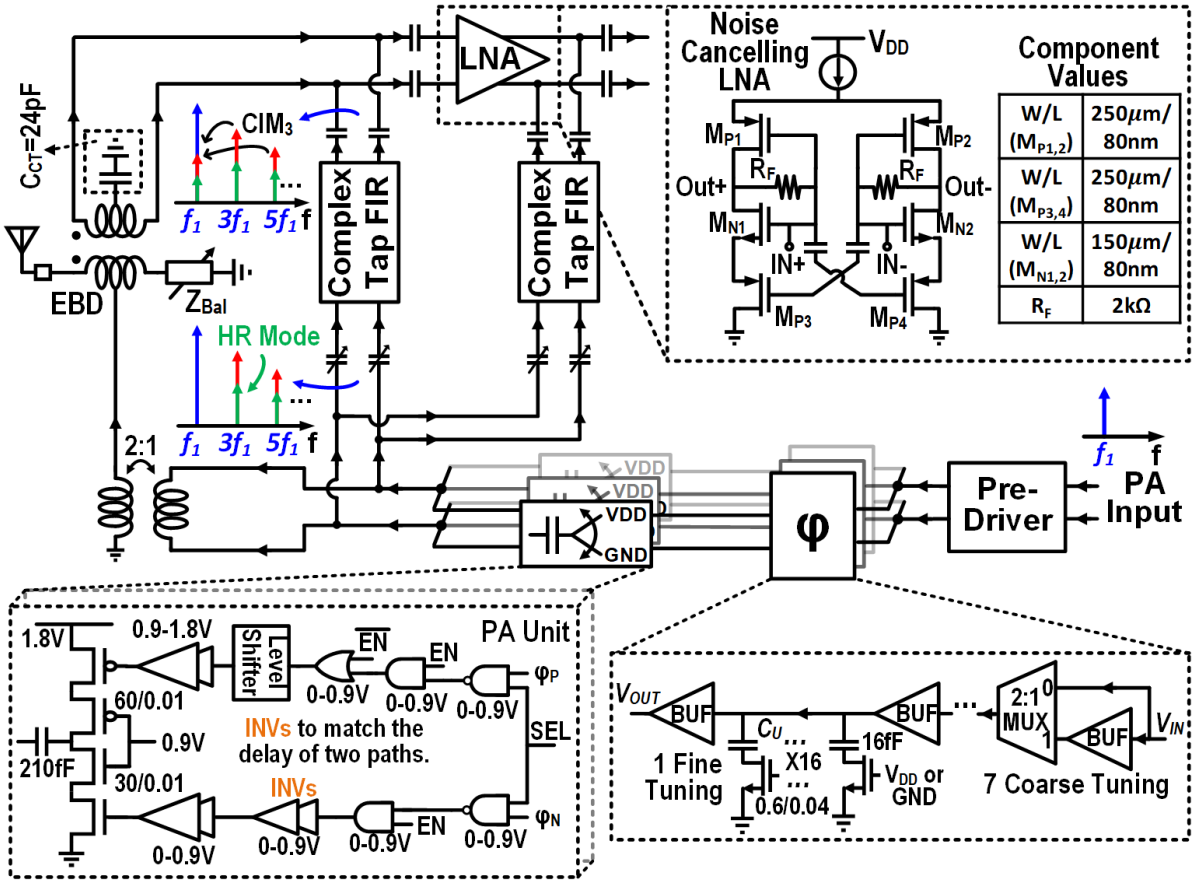


Figure 5.18: The harmonic-rejection PA and the resistive feedback cross-coupled LNA schematics.

seven coarse and one fine-tuning stage based on an inverter delay (Fig.5.18), which covers a phase tuning range from 0° to 90° for all PVT corners. The post-parasitic extracted simulated phase resolution of the phase shifter is less than 1.5°. The PA main stage consists of 15 thermometer-coded PA units (Fig.5.18) for the 0° and 90° paths, and 22 units are used for the 45° path to control the gain ratios coarsely. Moreover, each path includes additional 3 parallel thermometer-coded PA cells for fine-tuning the gain ratios (not shown in Fig.5.18).

5.4.4 Receiver

The LNA is implemented as a current-reuse G_m stage driving a passive current-mode down-conversion mixer. The resistive feedback cross-coupled LNA (shown in Fig.5.18) produces a broadband impedance match and noise cancellation of $M_{N1,2}$ and $M_{P3,4}$, as well as provides further rejection of any residual common-mode SI leakage [82], which again, improves the RX linearity. Both the main receiver path and the mixed-signal cancellation path contain a passive quadrature down-conversion mixer, followed by an inverter based trans-impedance amplifier (TIA) with variable gain, and a 50 Ω output buffer (Fig.5.11). The mixer is driven by a quadrature 25% duty cycle square wave LOs which are generated from an integrated integer-N Type-II PLL and a clock divider [83].

5.5 Chip and System Measurement Results

The FD transceiver chip was fabricated in Taiwan Semiconductor Manufacturing Company's (TSMC) 10-metal layer 40nm CMOS process technology and occupies 3.2 mm^2 while operating off a 0.9 V, 1.1 V, and 1.8 V power supply, as shown in Fig.5.19. A standalone canceler and a receiver test structure were placed on the top side of the die (Fig.5.19). Two versions of the test board with different chip-on-board packaging were utilized for various testing modes of the transceiver chip. On the first test board, the EBD's antenna and input port use probe pads, while all other pads on the chip are wire-bonded, which allows for measurements of the EBD TX-to-ANT insertion loss, the EBD TX-to-ANT IIP_3, and the maximum SI suppression of the cancellation system, etc. On the second version of the test board, the EBD's input pad is left open which only imposes the minimal capacitive loading (≈20 fF) to the PA output. All other pads, including the EBD's antenna port, are wire-bonded in order to measure the transceiver's system performance. Different modes of testing which include the short- and long-delay spread SI suppression, and commonly accepted metrics for RF testing for both the TX and RX signal paths were performed with the transceiver chip using the measurement setup shown in Fig.5.20. A Tektronix AWG7000A arbitrary

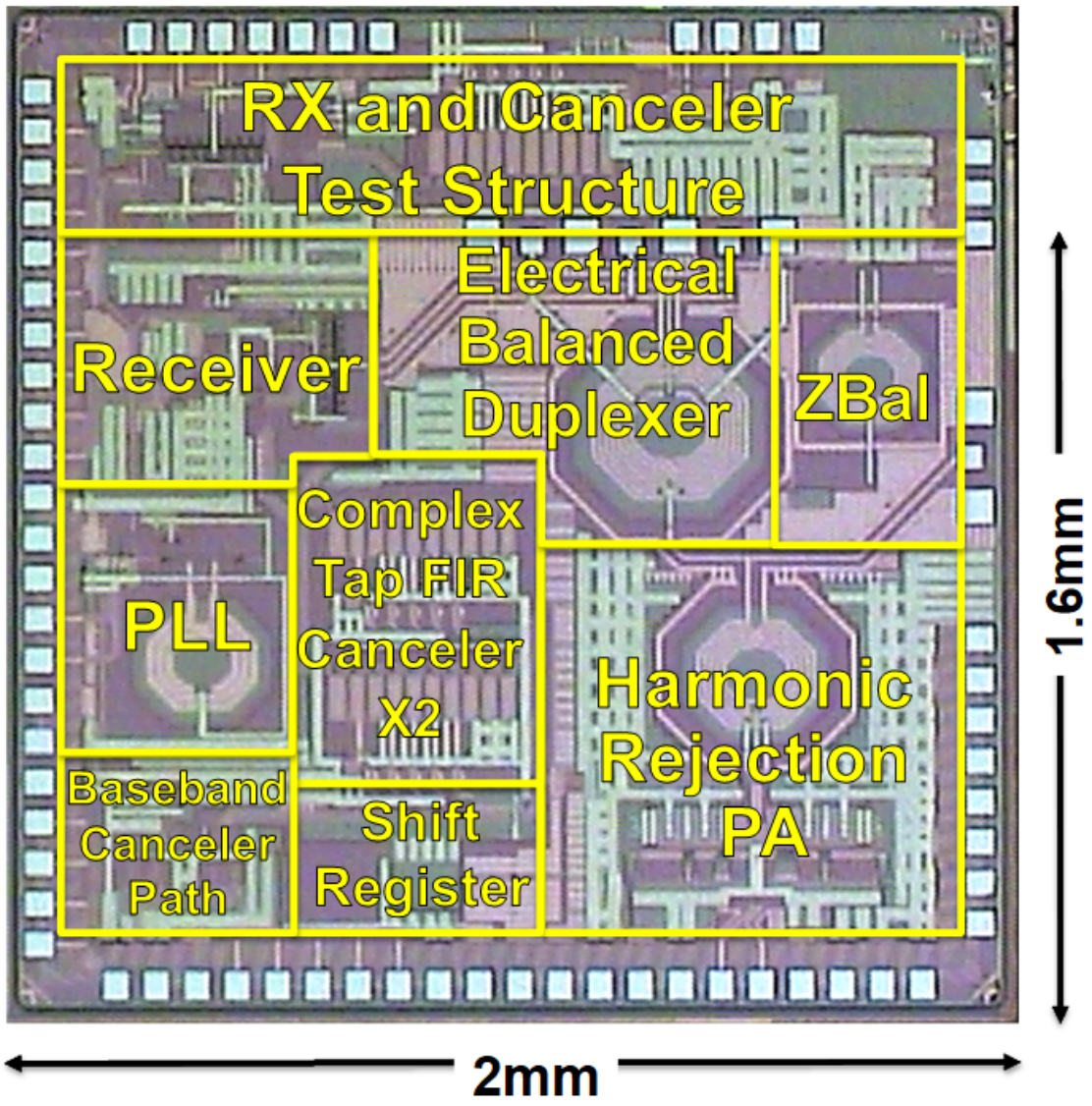


Figure 5.19: Die photograph of the FD transceiver AFE.

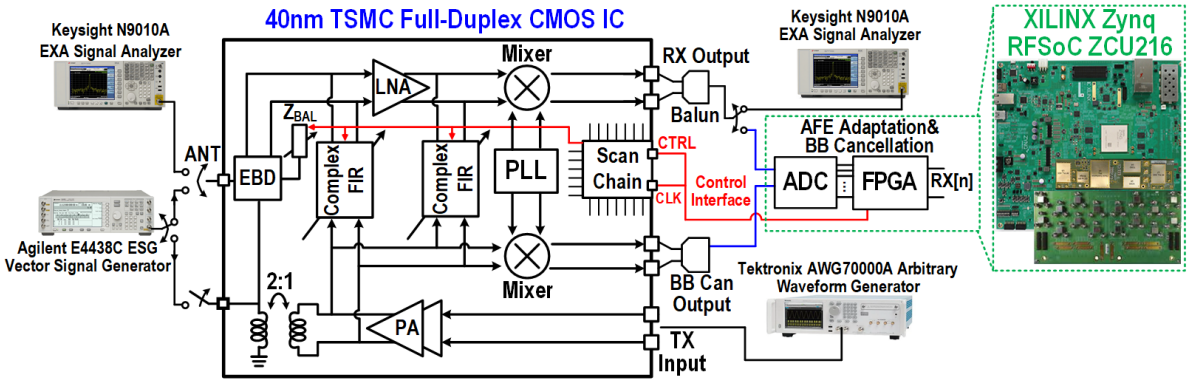


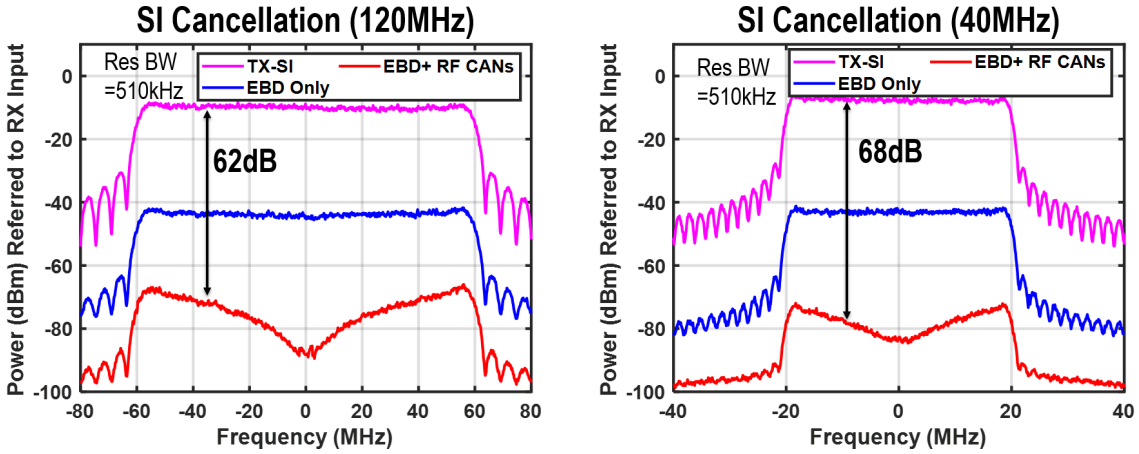
Figure 5.20: Measurement setup of the FD transceiver IC interfacing with the Xilinx RFSoC evaluation kit for different testings.

waveform generator or an Agilent E4438C vector signal generator provides an input signal to the PA, EBD or antenna input ports. A Keysight N9010A EXA signal analyzer was used to measure the TX RF output or RX baseband output signal. A Xilinx ZCU216 RFSoC evaluation kit completes the calibration loop to tune the RF cancelers, and the long-delay spread mixed-signal baseband SI cancellation path.

5.5.1 Integrated RF SI Suppression Measurements

While performing integrated RF SI suppression measurements, the EBD's Z_{Bal} network was first tuned to achieve a broadband SI rejection with minimal amplitude and group delay variation. A modulated signal with a specific bandwidth was applied to the PA input, with both RF cancelers turned off. The SI signal coupled through the EBD and then down-converted to baseband was measured using a spectrum analyzer at the receiver analog baseband output. The received SI spectrum was then analyzed, and the procedure was repeated to find the optimum Z_{Bal} setting for minimized SI power and amplitude variation within the bandwidth.

A Xilinx ZCU216 RFSoC evaluation kit including 14-bit/250MSPS ADCs emulating the digital back-end was programmed to realize a calibration function for the RF cancellation



(a) (b)

Figure 5.21: Measured SI spectrum after the suppression of the EBD and two RF cancelers referenced to RX input for (a) 120 MHz and (b) 40 MHz QPSK-modulated signal.

path (Fig.5.20). The calibration was first applied to the canceler prior to the LNA, then the post-LNA canceler was tuned for maximum suppression. A "pseudo-blind" search algorithm was utilized to find the optimum code setting for five complex filter taps from the MSB to the LSB sequentially, to minimize the residual SI power at the RX baseband. The algorithm focuses on the two MSBs of all filter taps using a blind search algorithm. After the first two MSBs converge to a maximum cancellation, the MSB (of the two) is stored in memory, while the calibration algorithm then repeats the process focusing on the next two MSBs (or MSB-1 and MSB-2), again converging on maximum cancellation. The process repeats iteratively until the LSB is calibrated for maximum SI cancellation. The convergence time in this calibration algorithm can be broken down into two parts: 1) the time to measure the average residual SI power ($\sim$7 s), and 2) the time to update the filter tap values ($\sim$120 s). The speed of the first phase of calibration is limited by the complexity of the modulation method, while the second phase is limited by the clock frequency and the length of the scan-chain. While this calibration method is sufficient for the testing, significant improvements in

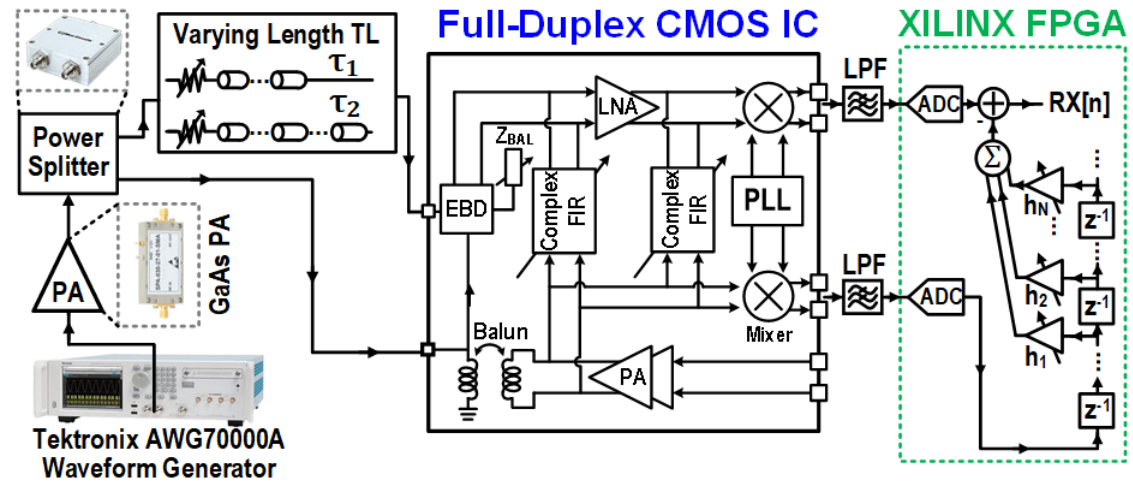
convergence time are needed for practical solutions used in the field. In this implementation, the integrated scan-chain serves as bottleneck to the convergence time because of the slow interface that exists between the Xilinx RFSoC and the scan-chain on the chip (shown in Fig.5.20). If all the digital functions for calibration and cancellation were integrated on chip with the transceiver, the digital bus to the AFE would have significantly less capacitance, then the convergence time can be significantly reduced.

A Xilinx ZCU216 RFSoC evaluation kit including 14-bit/250 MSPS ADCs emulating the digital back-end was programmed to realize a calibration function for the RF cancellation path (Fig.5.20). The calibration was first applied to the canceler prior to the LNA, then the post-LNA canceler was tuned for maximum suppression. A "pseudo-blind" search algorithm was utilized to find the optimum code setting for five complex filter taps from the MSB to the LSB sequentially, to minimize the residual SI power at the RX baseband. The algorithm focuses on the two MSBs of all filter taps using a blind search algorithm. After the first two MSBs converge to a maximum cancellation, the MSB (of the two) is stored in memory, while the calibration algorithm then repeats the process focusing on the next two MSBs (or MSB-1 and MSB-2), again converging on maximum cancellation. The process repeats iteratively until the LSB is calibrated for maximum SI cancellation. The convergence time in this calibration algorithm can be broken down into two parts: 1) the time to measure the average residual SI power ($\sim$7 s), and 2) the time to update the filter tap values ($\sim$120 s). The speed of the first phase of calibration is limited by the complexity of the modulation method, while the second phase is limited by the clock frequency and the length of the scan-chain. While this calibration method is sufficient for the testing, significant improvements in convergence time are needed for practical solutions used in the field. In this implementation, the integrated scan-chain serves as bottleneck to the convergence time because of the slow interface that exists between the Xilinx RFSoC and the scan-chain on the chip (shown in Fig.5.20). If all the digital functions for calibration and cancellation were integrated on chip with the transceiver, the digital bus to the AFE would have significantly less capacitance, then the convergence time can be significantly reduced.

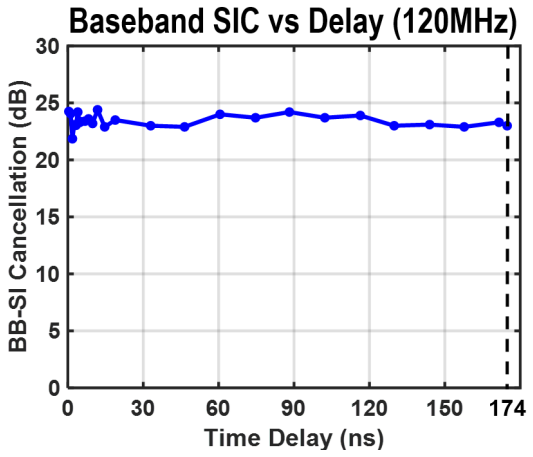
The measured short-delay spread SI suppression of the EBD and FFCs are shown in Fig.5.21a and Fig.5.21b, when the EBD antenna port is terminated into a load with a VSWR of 1.15:1. The TX-SI in Fig.5.21a and Fig.5.21b are measured directly at the EBD antenna port with an output power of 13 dBm, while the residual SI after the EBD and two FFCs is measured at the RX analog baseband output, then referenced to the RX input. For a signal bandwidth of 120 MHz, the total SI suppression is 62 dB, with 34 dB attributed to the EBD, 17 dB from the pre-LNA FFC, and 11 dB of cancellation from the post-LNA FFC. For a signal bandwidth of 40 MHz, the total SI suppression is 68 dB, with 35 dB coming from the EBD, 21 dB from the pre-LNA FFC, and the remaining 12 dB from the post-LNA FFC. Since the coherence bandwidth of the residual SI decreases after each cancellation [6] injection point, the number of taps of the post-LNA FFC should be increased relative to the pre-LNA FFC.

5.5.2 Long-Delay Spread SI Cancellation Measurements

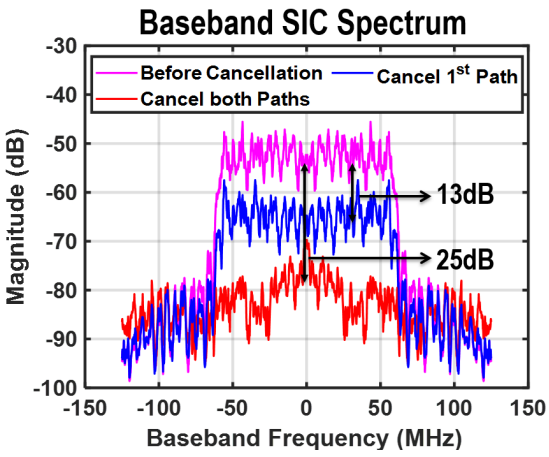
To demonstrate the ability of the mixed-signal baseband canceler to suppress long-delay spread SI, transmission lines with variable lengths were employed (Fig.5.22a). An external PA, or the on-chip PA, was used to apply the long-delay spread SI signal to the RX input. As shown in Fig.5.22a, a test signal from the external PA output is applied to a power splitter. One power splitter output is connected to the EBD TX input to generate a reference signal for the differential mixed-signal baseband cancellation path, while the other output is connected to a transmission line with varying length to model the effect of long-delay spread SI. At the analog baseband, both the receiver and the mixed-signal canceler outputs are taken off-chip and fed into 14-bit/250 MSPS ADCs on the Xilinx RFSoC evaluation kit, after which eight-tap digital FIR filters, adapted using an LMS algorithm with 60 flip-flops ($\sim$240 ns canceler delay spread), are used to match the time-of-flight for the long-delay spread SI. Each tap (h_1 to h_n) of the filter has a resolution of 16 bits with a real-tap coefficient, which are selected to strike a balance between the canceler performance, FPGA resource utilization, and clock frequency. Using transmission lines of varying length, the



(a)



(b)



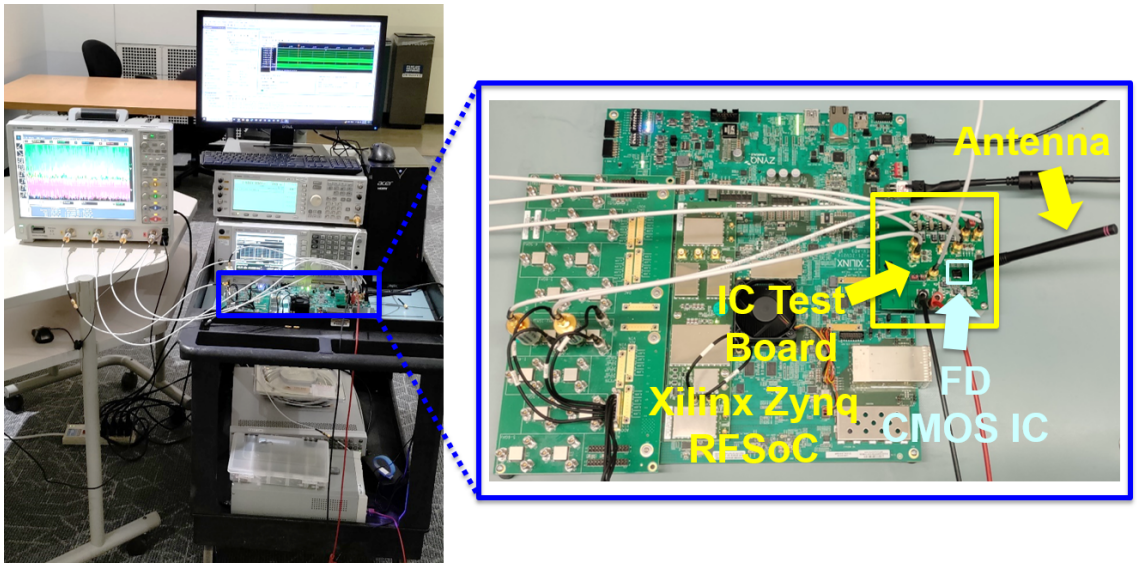
(c)

Figure 5.22: (a) Long-delay spread SI cancellation measurement setup. (b) Measured SI cancellation of the mixed-signal baseband canceler versus delay spread. (c) Measured baseband SI cancellation of two simultaneous reflections with different delay spreads ($\tau_1 \approx 8ns$, $\tau_2 \approx 174ns$).

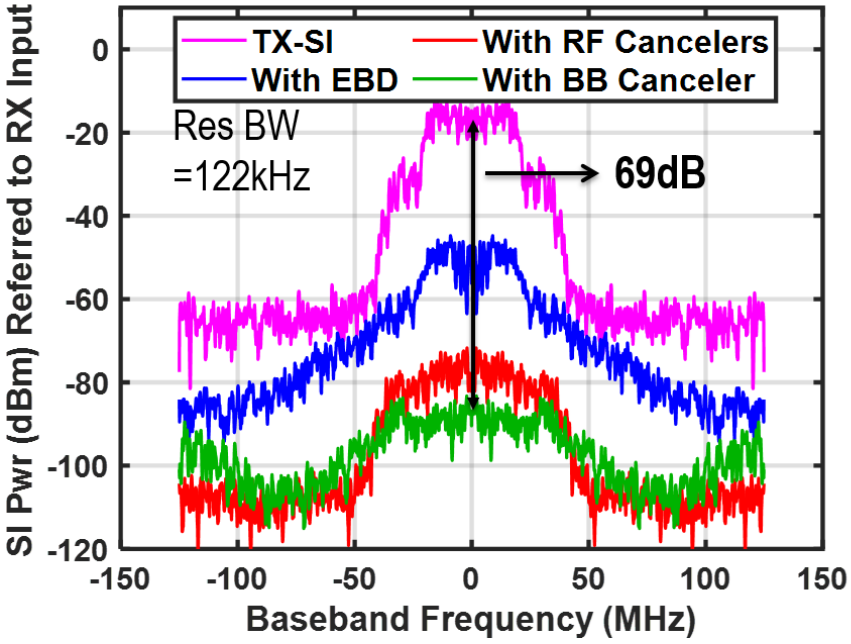
SI delay was varied between 0.4 ns to 174 ns and the suppression from the mixed-signal baseband cancellation path was measured. 23-25 dB cancellation can be observed for a 120 MHz-modulated signal in Fig.5.22b. Additional measurements were made with multiple SI reflection paths, synthesized using two transmission lines of varying length, but running in parallel (Fig.5.22a). The spectrums of the multi-path reflection signal at the digital baseband both before and after cancellation are shown in Fig.5.22c. When the SI consists of two different delay paths ($\tau_1 \approx 8ns$, $\tau_2 \approx 174ns$), the baseband canceler provides 25 dB of cancellation when all eight taps are configured to match both the SI delay spread and amplitude. The digital FIR filter converges within 10,000 digital samples which is less than 40 μs. The estimated area and power consumption of the digital portion of the baseband cancelers (excluding the ADCs) based on Synopsys Design Compiler synthesis results are 0.2 mm^2 and 23 mW.

5.5.3 SI Suppression Measurements with an Antenna

To measure the performance of the canceler network with an antenna and a physical wireless channel, SI suppression measurements were performed in variety of environments including an office, a hallway, and an atrium, as shown in Fig.5.23a. For the purposes of comparison, these measurements were taken at the identical locations as the SI profile versus time shown in Fig.2.2a. A commercial 2.4 GHz dipole antenna (Linx Technologies ANT-2.4-CW-HWR-SMA) is connected to the antenna port of the EBD which is wire-bonded to the test board. Fig.5.23b shows the measured SI spectrum referred to the RX input after each canceler path in an office environment. For a 40 MHz QPSK-modulated signal, the total SI suppression provided by the cancellation system is 69 dB, with 32 dB attributed to the EBD, 27 dB from the RF cancelers, and 10 dB cancellation from the mixed-signal baseband canceler. Moreover, the measured total SI suppression consistently exceeds 67 dB, while the RF SI suppression is above 56 dB in all tested environments. The RF SI suppression experienced some degradation (approximately 10 dB) when compared to the measured SI suppression with a 50Ω resistor, which is primarily due to two factors: the larger VSWR of the antenna



(a)



(b)

Figure 5.23: (a) SI suppression measurement setup using a commercial antenna. (b) Measured SI spectrum referred to RX input after each canceler path for a 40 MHz modulated signal.

(ranging between 1.5 and 2) and the wirebond inductance of the antenna pad. These two issues could be addressed in the future by incorporating a more accurate antenna impedance model in the simulation. The SI cancellation provided by the baseband canceler can be improved by increasing the number of filter taps and improving their resolution in future work.

5.5.4 Transceiver Evaluation of Common RF Metrics

To measure the ability of the FD transceiver to handle broadband interference and have sufficient linearity to accommodate high-power multi-carrier signals, the IIP_3 was calibrated and measured by using a stand-alone canceler integrated test sub-system on the chip's top side (Fig.5.19). The process of calibrating the canceler's linearity begins with two tones of equal amplitude from a signal generator that are applied to the canceler input. The IM_3 at the canceler output is then measured using a spectrum analyzer. A binary search algorithm is employed to find the optimum setting of the I-DACs to maximize the canceler's linearity performance. The canceler input-referred IP_3 (referred to R_{opt} of the PA) is +42 dBm which is 6 dB higher post calibration (Fig.5.24a). The measured IIP_3 enhancement is smaller than the simulated IIP_3 enhancement (+10 dB shown in Fig.5.10b) post calibration. This is attributed to the fact that all the I-DACs used to tune the G_m stages' linearity share a common control bus. Thus, random device mismatch between the various G_m stages cannot be individually tuned out. This error has been corrected in a future version of this chip by providing independent tuning control (I-DACs) for each individual G_m stage. The measured EBD TX-to-ANT IIP_3 is +55 dBm, as shown in Fig.5.24b. Since the EBD's differential receiver outputs are connected to the LNA on chip, simulations with parasitic extractions were performed on the EBD TX-to-RX IIP_3 with different Z_{Bal} code settings, considering the on and off states of the switches. Fig.5.24c shows that the EBD TX-to-RX IIP_3 is greater than 49 dBm, which is 7 dB higher than the measured IIP_3 of the RF canceler (Fig.5.24a). This suggests that the nonlinear distortion generated by the SI suppression circuitry at the RX/LNA input is dominated by the RF canceler prior to the LNA. Future work can further

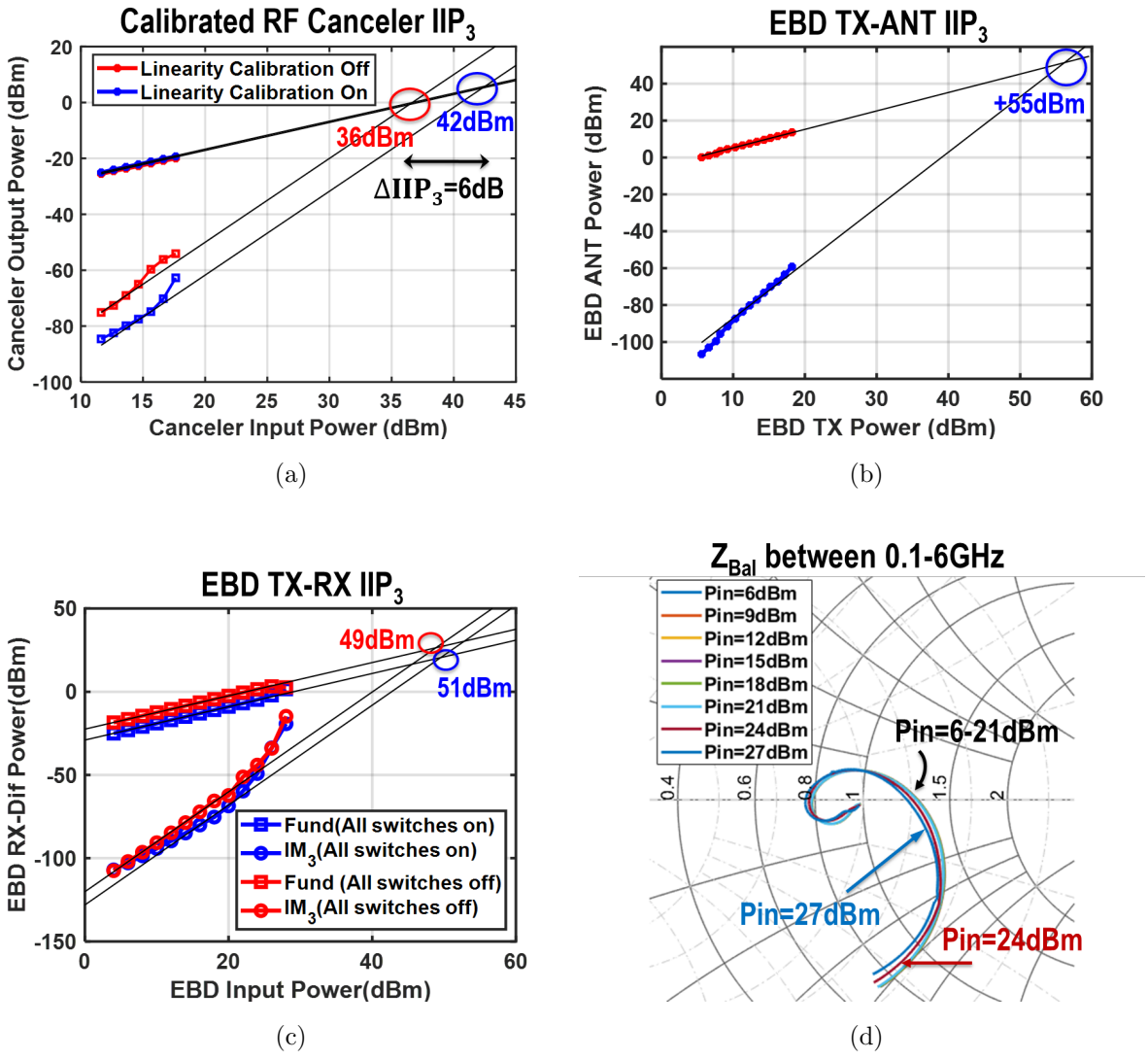
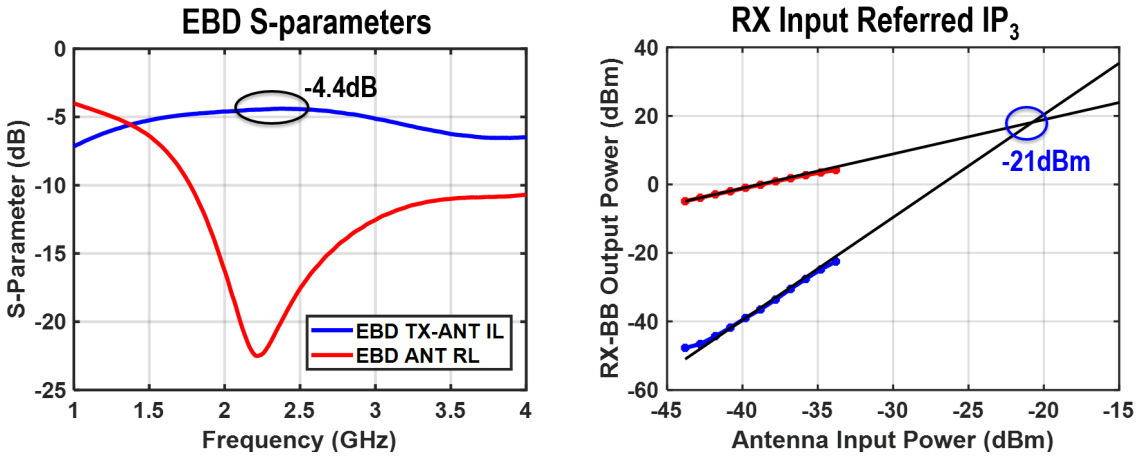


Figure 5.24: (a) Measured canceler IIP_3 before and after linearity calibration. (b) Measured EBD TX-to-ANT IIP_3. (c) Parasitic-extracted simulated EBD TX-to-RX IIP_3 for different Z_{Bal} switch settings. (d) Parasitic-extracted simulated impedance of Z_{Bal} at different input power levels.

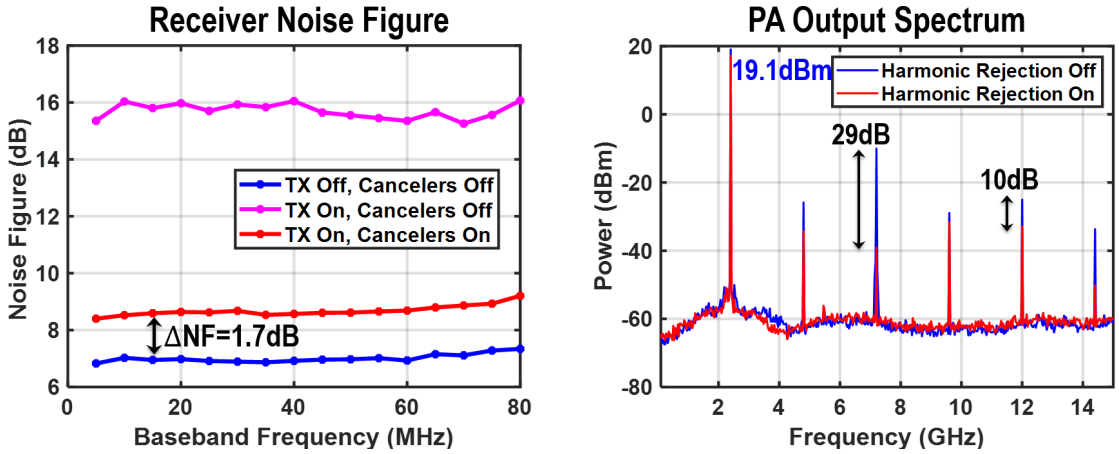


(a) (b)

Figure 5.25: (a) Measured EBD antenna return loss and TX-to-ANT insertion loss. (b) Measured RX IIP_3 with a maximum gain of 40 dB.

enhance the linearity of the RF FFC by incorporating noise cancellation techniques [25] or utilizing process technologies capable of supporting higher voltage swings. To further investigate the Z_{Bal}'s power handling ability, the impedance of Z_{Bal} across the 0.1–6 GHz frequency range was simulated under various input power levels while keeping the same Z_{Bal} code setting. Fig.5.24d shows that for input powers to the Z_{Bal} below 21 dBm, the impedance of the Z_{Bal} remains nearly identical on the Smith chart. This demonstrates that the Z_{Bal} can operate effectively at typical high TX power levels exceeding 24 dBm by assuming a minimum TX insertion loss of 3 dB in a balanced EBD.

Using the same Z_{Bal} setting that was used to measure the EBD SI attenuation in Fig.5.21a and 5.21b, the EBD antenna port S_{11} was measured to be less than -15 dB between 2.0-2.6 GHz (Fig.5.25a). The measured EBD transmitter-to-antenna insertion loss is -4.4 dB. The receiver has a maximum measured gain of 40 dB and a single-side-band 3 dB bandwidth of 85 MHz. The measured receiver in-band IIP_3 at the maximum gain setting is -21 dBm (Fig.5.25b). This is limited by the 50Ω baseband output buffer on this chip. The entire



(a) (b)

Figure 5.26: (a) Measured RX NF and NF degradation when cancelers are turned on. (b) Measured harmonic rejection PA spectrum at PA output.

receiver consumes 25 mW from a 0.9/1.8 V power supply. Fig.5.26a shows the measured receiver double-side-band NF versus baseband frequency at the maximum receiver gain. When both the PA and the cancelers are turned off, the measured NF is 6.8 dB, where 3.8 dB comes from the EBD ANT-to-RX insertion loss based on simulations. When both the transmitter and the cancelers are turned on, the NF degradation is +1.7 dB, where 1.4 dB comes from the canceler prior to the LNA and 0.3 dB comes from the canceler after the LNA. The PLL has a measured locking range from 4.3 to 5.0 GHz while consuming 15 mW (including LO dividers) from a 0.9 V supply and a measured phase noise of -116 dBc/Hz at a 1 MHz frequency offset.

Fig.5.26b shows the measured output spectrums of the PA when a CW signal is applied to the PA input. The PA has a maximum measured TX output power of +19.1 dBm after de-embedding the EBD transmitter-to-antenna insertion loss of 4.4 dB. The PA consumes 295 mW (including PA pre-drivers and phase shifting stages) with a maximum PAE of 27%. When the PA operates in the harmonic-rejection mode, the measured 3^{rd} and 5^{th} order

harmonic suppression are 29 dB and 10 dB, respectively. The transmitted output power decreases by 1.8 dB in the harmonic-rejection mode.

Table.I provides a comparison of this FD AFE with prior art on FD radios. The FD transceiver in this work achieves a broader measured SI cancellation bandwidth and longer delay spread as compared to prior art. The post-calibration canceler IIP_3 is enhanced by 6 dB which is also greater than prior art. The higher receiver NF in this design compared to [20,23,24,27,69] is primarily due to the insertion loss of the EBD used in the integrated FD air interface. However, when de-embedding the simulated EBD ANT-to-RX insertion loss of 3.8 dB from the measured NF of 6.8 dB, the NF of the remaining receiver is comparable or better than other prior art listed in Table.5.1.

5.6 Conclusion

This chapter demonstrates a 2.4 GHz FD radio transceiver with multiple self-interference cancellation paths in the receiver chain. The mixed-signal baseband canceler achieves +23 dB cancellation over 120 MHz bandwidth for the delay between 0.4-174 ns. The integrated EBD with a tuned impedance matching network and two complex-tap FIR filters provide +62 dB cancellation over 120 MHz bandwidth for delay spread between 0-280 ps. To the best of our knowledge, this transceiver chip provides the longest delay-spread cancellation across wider cancellation bandwidth as compared to prior art. In addition, a series of techniques to enhance the cancellation bandwidth and canceler linearity are demonstrated in this work.

Table 5.1: Performance Summary and Comparison Table with Prior FD Publications

	ISSCC [24]	**JSSC [20]**	**ISSCC [21]**	**JSSC [69]**	**RFIC [23]**	**JSSC [27]**	**This Work**
Architecture	Switched capacitor RF & analog BB FIR with stacked capacitor	RF & Analog BB FIR filter	Double-RF adaptive FIR	Code-domain IAD N-path	Switched capacitor RF & analog BB FIR	Active nested G_m nested VM	Integrated EBD & two complex RF FIR & mixed signal BB canceler
Technology	CMOS 65nm	CMOS 40nm	CMOS 40nm	GF 45nm SOI	CMOS 65nm	CMOS 65nm	CMOS 40nm
Frequency (GHz)	0.1-1	1.7-2.2	1.6-1.9	0.4-1.1	0.1-1	0.9	2.1-2.5
Integrated SIC (dB) / BW(MHz)	42 / 40	50 / 42	65 / 80 70 / 40	49.5 / 13	32 / 20 16 / 40	70 / 0.8 52 / 20	62 / 120 68 / 40
Baseband SIC (dB) / BW(MHz)	12 / 40	18 / 40	NA	NA	16 / 20	NA	23 / 120
Canceler Delay Spread(ns)	RF: 7.75 BB: 85	RF: 0.26 BB: 130	RF: 0.2	>5	RF: 1.1 BB: 75	88[d]	RF: 0.28 BB: 240
RF Canceler IIP_3 (dBm)	NA	36	40	NA	NA	23	42
Canceler Power (mW)	118.4 (RF) 14.4 (BB)[a]	3.5 (RF) 8 (BB)	14.3	<40	25.5 (RF) 6.5 (BB)	44.4	35 (RF) 26 (BB)[f]
Canceler Area (mm^2)	1.6 (RF) 1.8 (BB)[b]	0.025 (RF) 0.26 (BB)	0.12	NA	1.1 (RF) 1.7 (BB)[b]	0.6[b]	0.2 (RF) 0.29 (BB)[f]
IB RX IIP_3(dBm)	-14 (Gain of 24dB)	-5	NA	+23.1	-18.7 (Gain of 27dB)	NA	-21 (Gain of 40dB)
RX P_{1dB}(dBm)	-25 (Gain of 24dB)	-15	NA	+12.1	-27 (Gain of 27dB)	NA	-31 (Gain of 40dB)
RX NF (dB)	3.7	4	8.1	2.6-5.6	5.3	4.4[e]	6.8 (3.8 from EBD)
SIC NF Degradation (dB)	0.8 (LP) / 2.8 (HP)[e]	1.55	1.6 (Two RF Cancelers)	0.8-3.55	1.9	1.75	1.7 (Two RF Cancelers)
RX Power (mW)	34	32.4[g]	NA	18	31	NA	40[g]
Active Area (mm^2)	7.2	3.5	4	1.12	5.15	1.2	3.2

[a] The canceler power is calculated from the power per tap reported in [24]. [b] The canceler area estimated from the chip micrograph. [c] NF degradation of 0.8dB and 2.8dB are measured with P_{TX}=+7dBm and +15dBm, respectively. [d] The reference signal for cancellation is delayed at the analog baseband and then up-converted to RF carrier frequency to cancel the SI at RX input. [e] The NF of an off-chip receiver. [f] The baseband canceler power and area include the measured on-chip analog portion of the canceler and the estimated digital portion of the canceler on FPGA. The ADCs are not integrated on this chip, therefore their area and power are not reported. [g] The RX power includes the power consumption of the PLL and LO buffers.

Chapter 6

A HIGHLY TUNABLE RF SELF-INTERFERENCE CANCELER WITH MACHINE-LEARNING ACCELERATED ADAPTATION FOR FULL-DUPLEX RADIO APPLICATIONS

The FD radio front-end presented in Chapter 5 integrates four independent SI suppression paths, achieving broadband and deep cancellation for both short- and long-delay spread SI from various interference reflection paths. However, adapting a single RF canceler requires over 120 seconds, making it challenging to mitigate SI in dynamic wireless environments. This chapter addresses this limitation by introducing a 2.4 GHz RF SI canceler chip with extensive tuning capabilities, leveraging a machine-learning-augmented algorithm to accelerate adaptation [84]. The proposed design enhances SI cancellation depth, canceler linearity, and convergence speed. The prototype chip, fabricated using a 40 nm CMOS process, features improved tuning capabilities in filter coefficients, delay spread, and linearity. A custom-designed neural network (NN) is implemented on an FPGA within a Xilinx RFSoC evaluation board to accelerate the canceler chip's adaptation process. The RF canceler, realized as a 6-tap complex finite impulse response (FIR) filter with programmable delay spread, achieves 32 dB SI cancellation over a 40 MHz bandwidth in a real wireless channel and an input-referred third-order intercept point (IIP_3) of +38 dBm. The NN computes an initial canceler setting, followed by a dithered linear search algorithm, achieving a convergence time of less than 10.5 ms. The SI canceler chip demonstrates a maximum group delay of 2 ns, an output noise density of -184 dBV/$\sqrt{\text{Hz}}$, and an S_{11} of -10 dB across 2.3 - 2.8 GHz. The RF SI canceler occupies an active area of approximately 1.8 mm^2 and consumes 39 mW.

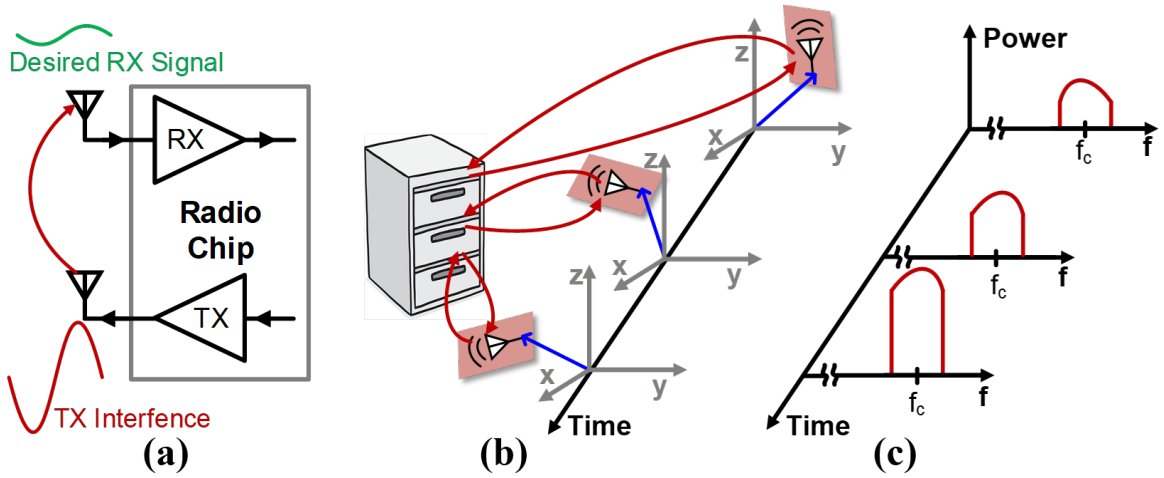


Figure 6.1: (a) Self-interference generated from a radio's own transmitter impacting its receiver. An illustration of (b) radio movements and (c) the resulting dynamic SI frequency response in real-world environments.

6.1 Introduction

The demand for wireless connectivity has increased significantly in recent decades and is expected to grow five- to tenfold in the coming decade [1,39]. This trend drives research toward enhancing mobile transceiver data rates while reducing latency to support emerging applications such as autonomous vehicles and edge computing, in addition to existing standards like Wi-Fi, cellular, and Bluetooth. In-band full-duplex (FD) radios improves wireless network capacity by enabling simultaneous transmission and reception on the same frequency. However, self-interference (SI) from the transmitter (TX) is a major challenge, as it can saturate the receiver (RX) front-end and degrade sensitivity, particularly with high-output power signals (Fig. 6.1a).

Despite decades of research on integrated SI cancelers [19–22,24,27,29,30,50,55,69,85–87], significant challenges remain. First, the dynamic nature of SI, caused by the movement of the radio transceiver and surrounding objects (Fig.6.1b), requires SI cancelers with wide

tuning ranges and numerous parameters to address variations in amplitudes, phase, and delay spreads of the SI frequency response (Fig.6.1c). Analog true-time delayed finite impulse response (FIR) filters have been utilized as feedforward cancelers (FFC) to suppress SI leakage at the receiver input [5, 20, 21, 24], preventing receiver from saturation. However, these filters lack independent phase control, limiting their cancellation bandwidth and depth [18, 26]. While designs such as [18, 65] address this limitation by using complex filter tap coefficients with independent phase tuning, their limited delay spread tuning range makes it challenging to cancel SI with longer path delays at the receiver input. To improve the filter tap delay tuning range, additional tuning capabilities have been introduced in [27,29,55] using tunable resistor and capacitor banks. However, the number of filter taps in these designs is limited, ultimately constraining the achievable SI cancellation bandwidth and depth [88].

Secondly, the varying SI frequency response in wireless environments necessitates a rapid adaptation of all canceler tuning parameters to minimize latency in FD radios. RF FFCs implemented with discrete components have demonstrated fast adaptation using the least mean square (LMS) algorithm (Fig.6.2a) [54, 56]. However, extracting the filter state information required by the LMS algorithm typically demands high-speed and power-hungry mixed-signal circuits. While the analog LMS loop in [55] eliminates this requirement, distortion and noise from the adaptation loop can degrade the canceler's performance. Additionally, analog control requires a dedicated I/O pad for each parameter, which is typically less programmable than digital control. In [18, 89], the canceler adaptation is based solely on the residual SI signal (Fig. 6.2b), simplifying the implementation of the adaptation loop. However, these methods typically require more iterations to converge compared to the LMS algorithm [90]. The approach in [24, 27] pre-measures the canceler's frequency responses and stores the corresponding settings in a look-up table (LUT), which is then used to optimize SI cancellation and accelerate the adaptation (Fig.6.2c). However, as the number of tuning parameters increases, the pre-measurement time becomes significant, adding overhead to the overall adaptation process. By leveraging the linear properties of FIR filters, the method in [57] computes weight coefficients in a single iteration using linear algebra, based

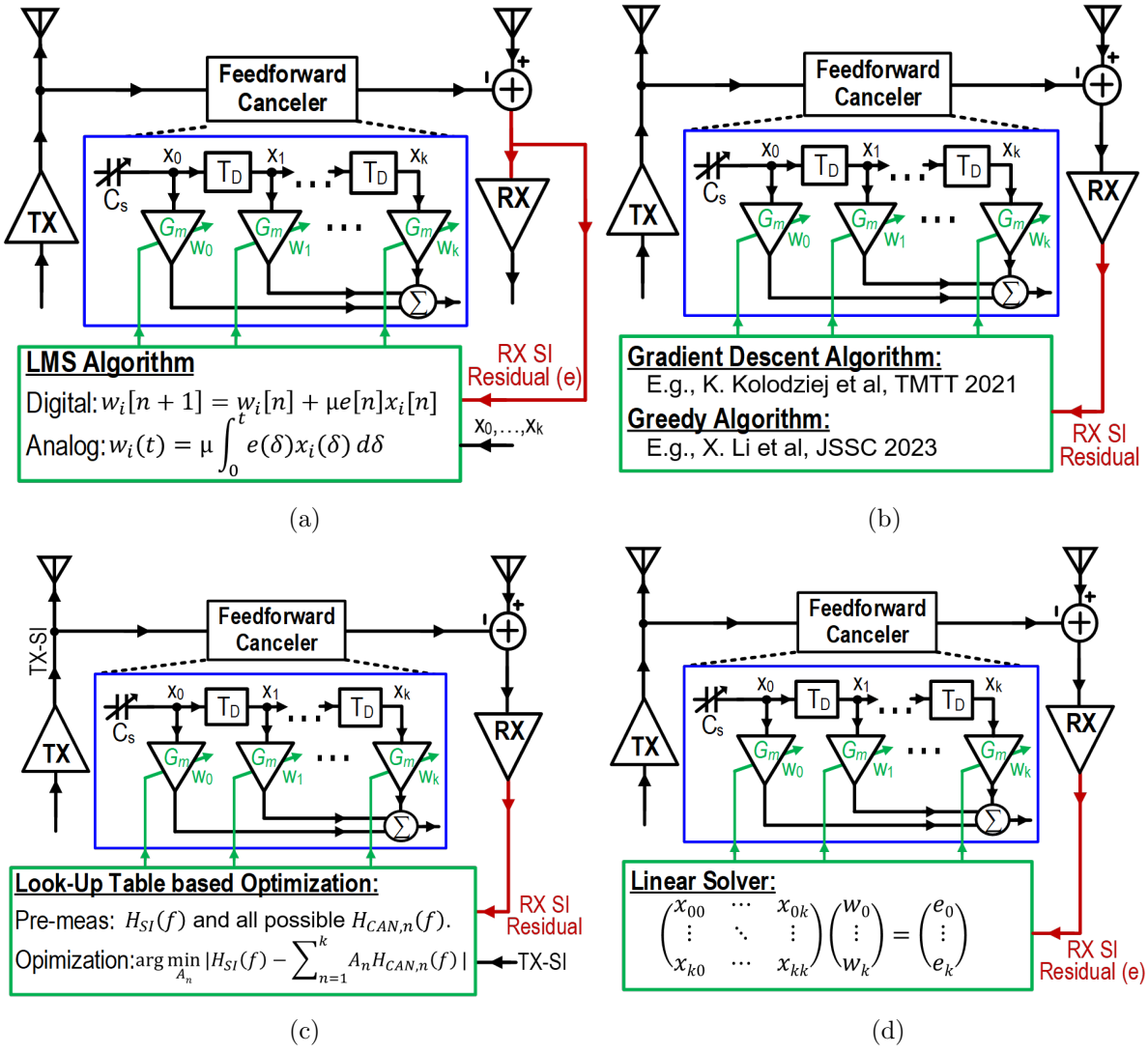


Figure 6.2: Prior optimization algorithms used for adapting RF SI cancelers include: (a) analog or digital least mean square algorithms, (b) gradient descent or greedy algorithms, (c) frequency-domain optimization using a look-up table, and (d) linear algebra solvers.

on pre-calibrated filter state information x_{ij} and residual SI signal e_i (Fig.6.2d). However, the nonlinear relationship between amplitude, phase, and control codes in integrated cancelers can significantly degrade the accuracy of the computed solution, thereby limiting the achievable cancellation performance. Moreover, as SI cancelers require wider tuning ranges for future FD radios, the number of tuning parameters will continue to grow, exponentially expanding the canceler's tuning space and further increasing the convergence time of these algorithms.

This chapter provides an expanded description of the 2.4 GHz RF SI canceler prototype chip initially presented in [84]. To the best of our knowledge, this is the first implementation of an ML algorithm to adapt an RF canceler chip at the transistor level in a FD radio. The key contributions of this work include:

- Implementation of a 2.4 GHz RF SI canceler chip for FD radios with extensive tuning capabilities, including filter amplitude, phase, delay spread, and linearity. The enhanced tuning range allows the canceler to effectively address variations in the SI frequency response in dynamic wireless environments. The canceler is designed as a discrete add-on for integration with transceiver chips from different manufacturers.

- Development of an ML-augmented algorithm, implemented at the register transfer level (RTL) on an FPGA, to accelerate the canceler's adaptation process. The algorithm achieves a total measured convergence time of about 10 ms.

- Comprehensive SI cancellation measurement of the integrated canceler chip in real-world wireless channels across various environments.

The remainder chapter is organized as follows: Section 6.2 describes the proposed ML-augmented SI canceler architecture. Section 6.3 presents the detailed implementation of the RF canceler chip, followed by the design and implementation of the ML algorithms in Section 6.4. Measurement results are given in Section 6.5, and conclusions are provided in Section 6.6.

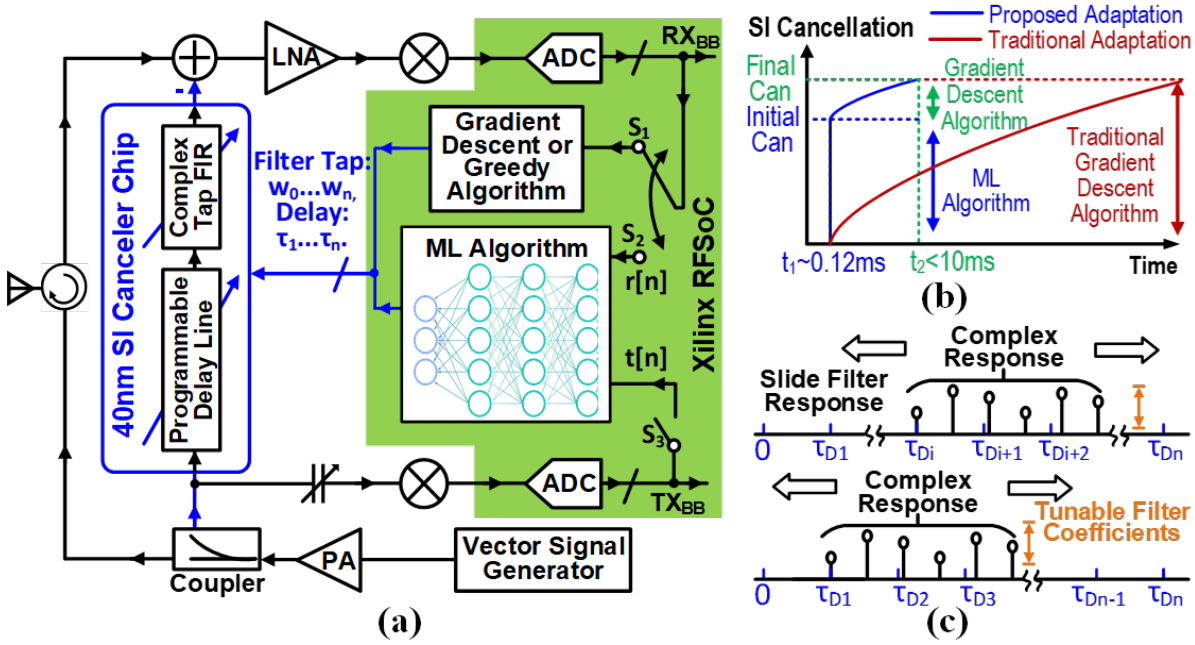


Figure 6.3: (a) Architecture diagram of the RF SI canceler chip adapted using a machine-learning-augmented algorithm on a Xilinx RFSoC. (b) Convergence time of canceler adaptation with the ML-augmented algorithm. (c) Illustration of adjusting the delay spread of the programmable delay line to mitigate SI over a wide delay range.

6.2 Transceiver Architecture with ML-Augmented Canceler Adaptation

Fig.6.3a shows the proposed highly tunable RF SI canceler chip with a machine-learning (ML) augmented adaptation algorithm within a 2.4 GHz FD radio transceiver. A circulator at the radio antenna-air interface provides initial SI attenuation. Additional SI cancellation is performed by the RF canceler chip, placed between the power amplifier (PA) output and the receiver low-noise amplifier (LNA) input. Suppressing SI at the radio RX/LNA input prevents RX saturation and relaxes the linearity requirements for the LNA and subsequent RX chain components. The proposed RF SI canceler chip consists of a programmable delay line (PDL) followed by a 6-tap complex FIR filter with linearity-enhanced transconductance

stages. The canceler chip provides independent tuning capabilities for key parameters including amplitude, phase, delay spread, and linearity of each filter tap. Each parameter is designed with a wide tuning range to improve both SI cancellation depth and bandwidth. All tuning parameters of each filter tap are digitally controlled by the radio's digital back-end (DBE), implemented on a Xilinx RFSoC, where the ML-augmented algorithm is co-designed with the canceler chip to adapt the tuning parameters. While Fig.6.3a shows the adaptation loop for a single RF canceler path, this represents the adaptation for an entire RF canceler network, which may include multiple canceler paths at various points in the RX chain [18, 20, 21, 24, 29].

The proposed adaptation system, shown in Fig.6.3, places the SI canceler chip within a loop that includes both an ML algorithm for rapid coarse adaptation and a gradient descent algorithm for fine-tuning. The ML algorithm computes an initial coarse solution in approximately 0.12 ms, followed by gradient descent refinement, which converges typically within 10 ms (Fig.6.3b). Both the residual SI at the receiver ADC output (r[n]), and the digital version of the down-converted TX reference signal (t[n]) serve as inputs to the ML algorithm, implemented as a custom-designed neural network (NN). This allows the NN to learn the relationship between various SI leakage responses from the radio antenna-air interface and the corresponding canceler settings. The training data set is obtained by optimizing the canceler chip under various conditions using traditional optimization algorithms, such as the pseudo-blind search algorithm described in [18]. The down-converted TX reference signal t[n] effectively captures the nonlinearity and distortion of the PA in the TX path. The proposed ML-augmented algorithm significantly reduces the number of iterations required by traditional gradient descent [89] or pseudo-blind search algorithms [18], as shown in Fig.6.3b, thereby reducing the convergence time and latency in FD systems. Expanded descriptions of the RF canceler chip and the ML-augmented algorithm are given in the following sections.

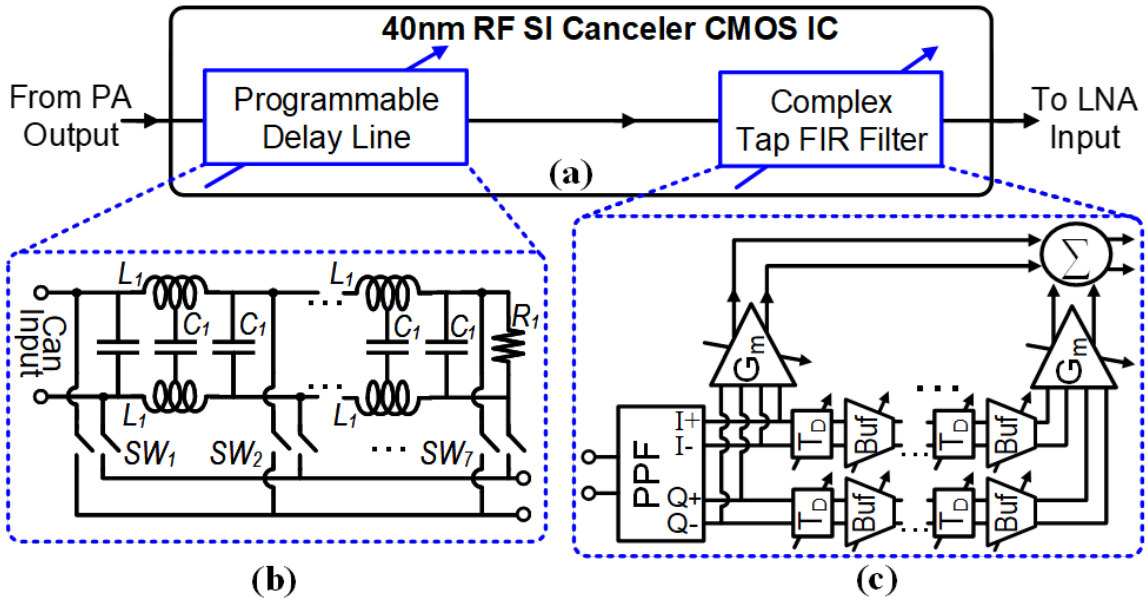


Figure 6.4: (a) Block diagram of the RF SI canceler chip, including (b) a programmable delay-spread LC delay line and (c) a complex-tap FIR filter.

6.3 Highly Tunable Integrated SI Canceler

The SI canceler chip is implemented as a 6-tap FIR filter with complex coefficients and programmable delay spread, as shown in Fig.6.4a. The use of complex filter coefficients allow for independent control of gain and phase for each filter tap, enhancing both the SI cancellation depth and bandwidth [18, 26]. The programmable delay line (PDL) in the canceler can shift the complex filter's impulse response in the time domain, as shown in Fig.6.3c, which provides an additional degree of freedom to address SI with varying delay spreads from the antenna-air interface. This distinguishes this work from previous designs in [18, 20, 21, 24]. Additionally, the linearity of each filter tap can be independently tuned to achieve the highest canceler linearity performance. The chip also provides the option to configure the number of filter taps and switch between real and complex filter coefficients, further enhancing its tunability.

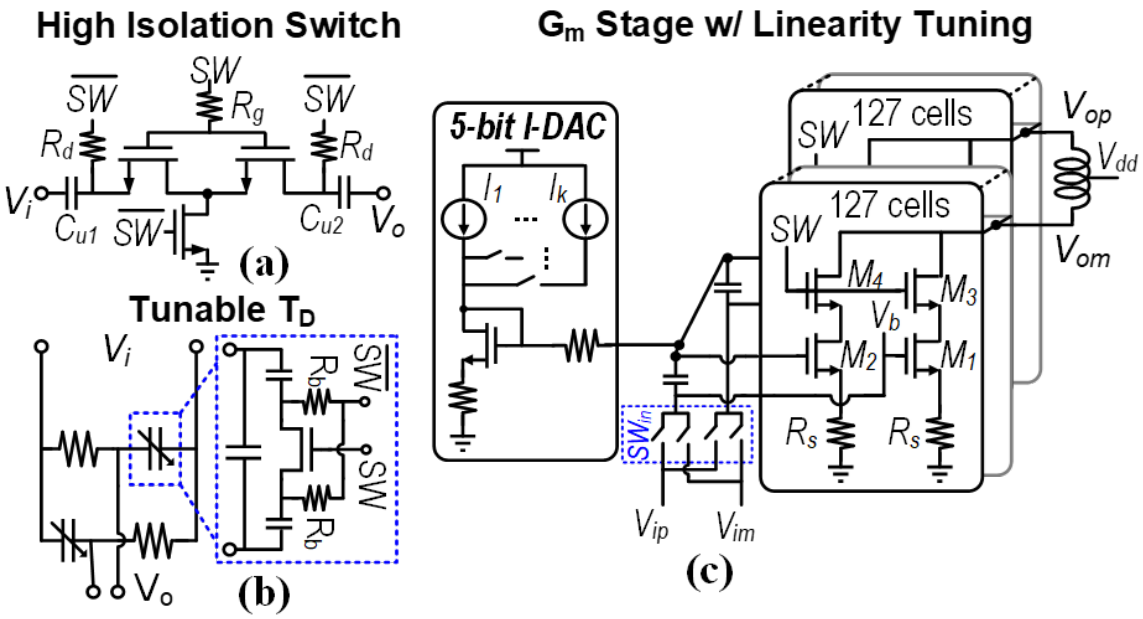
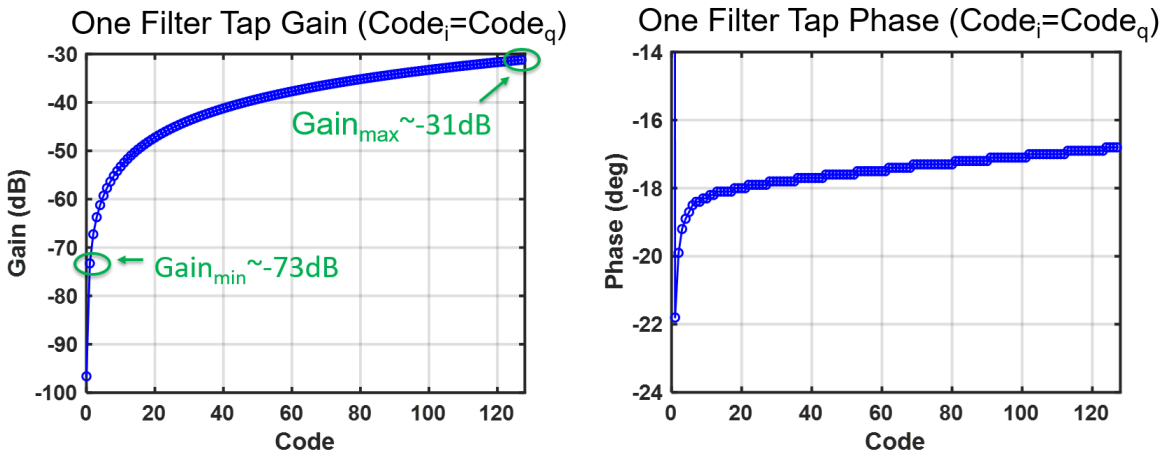


Figure 6.5: Transistor-level implementation of (a) the high-linearity and isolation switch within the LC delay line, (b) the tunable delay cell, and (c) the trans-conductance G_m stage within the complex-tap FIR filter.

Fig.6.4b and c show the detailed circuit implementations of the 2.4 GHz canceler chip, including the delay line and the FIR filter, respectively. An integrated balun (not shown in Fig.6.4) provides impedance matching and converts the PA output to differential signals, which are then passed through a 6-stage LC delay line. The output of each LC stage can be switched to allow signals with different delay spreads to be directly coupled to the input of the subsequent complex FIR filter. By controlling the switches in Fig.6.4b (with one switch turned on at a time), a tunable delay spread ranging from zero to approximately 760 ps can be achieved from the LC delay line. Each switch in the PDL utilizes a T-type configuration (shown in Fig.6.5a), which enhances the switch's isolation and minimizes coupling between signals passing through different LC stages. Capacitors C_{u1} and C_{u2} are sized differently across the various switches ($SW_{1,\,2,\,\ldots}$), which compensates for the different attenuation of



(a) (b)

Figure 6.6: Simulated (a) amplitude and (b) phase of a single complex filter tap versus control code after parasitic extraction.

signals with various delay spreads. R_g and R_d in Fig.6.5a are DC-biasing resistors which reduce the signal-dependent switch resistance, thereby enhancing the linearity of the switch. A capacitor placed between the center tap of each inductor within the LC delay line (shown in Fig.6.4b) splits the unit inductor into two, effectively doubling the cutoff frequency ($\frac{2}{\sqrt{LC}}$) of the LC delay line [91], which reduces the number of inductors required and saves silicon area. To prevent unwanted signal reflections after signals traverse the various LC stages, the LC delay line is terminated with a 100Ω poly resistor that matches the characteristic impedance at the end of the delay line.

The output of the switch array connects to the input of the complex FIR filter, which uses a poly-phase filter (PPF) as the first stage (Fig.6.4c). With an input impedance greater than 2 kΩ, the FIR filter minimizes loading effects on the preceding LC delay line. Each delay stage in the FIR filter provides a switchable delay between 50 ps and 70 ps, achieved by varying the capacitors via the switch shown in Fig.6.5b. The maximum delay spread of the complex-tap FIR filter is approximately 350 ps. Each complex filter tap includes an 8-bit

digitally-controlled trans-conductance (G_m) stage with source-degenerated resistors, allowing for independent tuning of both amplitude and phase, as shown in Fig.6.5c. Integrated I-DACs within each filter tap adjust the gate voltage of the auxiliary device M_2 to cancel the 3^{rd} order nonlinearity of M_1, thereby improving the linearity of the G_m stage [18]. This independent tuning of linearity across each G_m stage compensates for random transistor mismatches, enhancing both the linearity of individual G_m stages and the overall canceler. The filter tap coefficients for amplitude and phase are controlled by switching the cascode devices (M_3 and M_4) in both the I and Q paths. This method minimizes direct signal coupling from the input to output through the gate-drain capacitors of M_1 and M_2 in Fig.6.5c, thereby effectively enhancing the tuning range and resolution of each filter tap. The simulated amplitude and phase response of a single complex filter tap after parasitic extraction, is shown in Fig.6.6a and 6.6b when adjusting the G_m stage control codes in both I and Q paths. Each complex tap achieves an amplitude tuning range of about 42 dB, with phase variation of less than 5 degrees when adjusting the amplitude. Additionally, the proposed G_m stage supports both positive and negative amplitudes through the switch SW_{in} in Fig.6.5c, effectively enabling a full 360-degree phase tuning range for each filter tap.

The outputs of each G_m stage are shorted together and loaded with a differential inductor (Fig.6.5c) at the canceler output, which can sustain a larger voltage swing compared to previous designs [18, 20, 21, 24, 27], thereby further enhancing the canceler's linearity. The canceler's output presents a differential impedance of about 1 kΩ at 2.4 GHz, allowing the injection of cancellation current at the receiver/LNA input, as shown in Fig.6.4a. Additionally, this design integrates six dedicated shift registers on-chip for each complex filter tap to control the weight coefficients, which significantly reduces the time needed to update the filter tap value from the FPGA DBE during canceler adaptation. A separate longer shift register is used for all other canceler tuning parameters, including delay spread and current bias, which typically require less frequent configuration than the filter tap values.

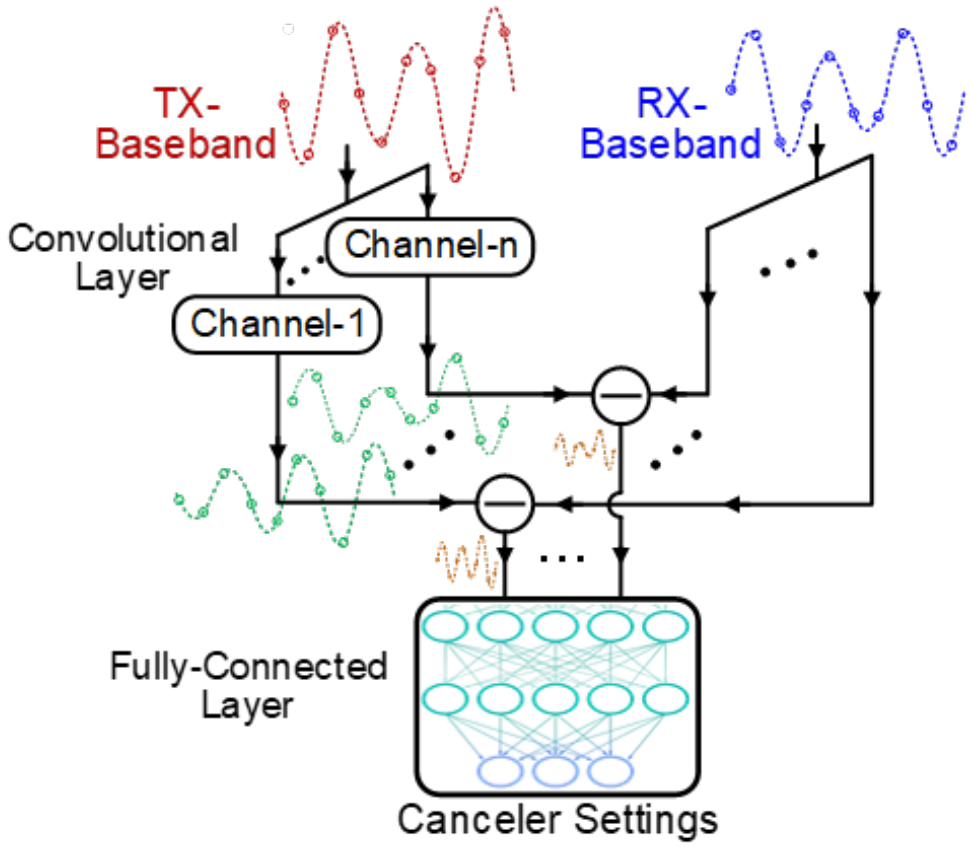


Figure 6.7: Conceptual diagram illustrating the use of convolutional and fully-connected layers to convert TX and RX baseband signals into optimized canceler settings.

6.4 Machine Learning-Augmented Adaptation Algorithm

This section provides a detailed discussion of the proposed ML algorithm, focusing on the custom-designed neural network architecture, training strategy, and its register-transfer level (RTL) implementation.

6.4.1 Neural Network Architecture

ML algorithms using neural networks (NNs) are widely applied in wireless communication and sensing systems due to their ability to learn complex relationships between input data

and desired outcomes without requiring explicit rule-based programming. This allows ML algorithms to optimize model parameters automatically, enabling effective generalization to new data. Leveraging these advantages, various ML-based methods have been explored for SI cancellation in FD systems [70]. For example, deep neural network (DNN)-based methods have been used to mitigate SI at the DBE of radio transceivers These methods effectively suppress nonlinear SI components while requiring fewer hardware resources compared to conventional cancellation techniques [36]. However, most existing ML-based SI cancellation approaches operate exclusively at the DBE, limiting their ability to address SI at the RF front end. Although prior studies [92, 93] have explored combining NNs with RF canceler adaptation, neither the canceler nor its adaptation have yet been implemented at the transistor-level. The proposed design bridges this gap by designing a NN-augmented adaptation loop on an FPGA for an integrated RF SI canceler.

Fig.6.7 shows the custom-designed NN architecture to facilitate RF canceler adaptation. A key observation in FD transceivers is that the SI signal at the RX input can be modeled as the transmitted signal convolved with various channel impulse responses across different environments [26]. This process is analogous to the convolution operation using multiple kernels in a convolutional neural network (CNN). Leveraging this property, the proposed NN architecture incorporates a convolutional layer, as shown in Fig.6.7. The digitized TX baseband signal t[n], is convolved with multiple kernels, each representing a specific channel impulse response. The resulting RX baseband predictions are then compared to the actual measured RX baseband ADC output r[n], generating error signals. These error signals effectively capture SI channel responses in different environments, independent of the TX and RX baseband signal. The error signals are subsequently down-sampled and condensed before being converted into optimized RF canceler settings through fully connected (FC) layers, as shown in Fig.6.7.

After training on a sufficient amount of representative data (discussed in the next section), the NN can ideally configure the canceler to an optimal or near-optimal setting in a single iteration, which will significantly reduce convergence time. This method eliminates

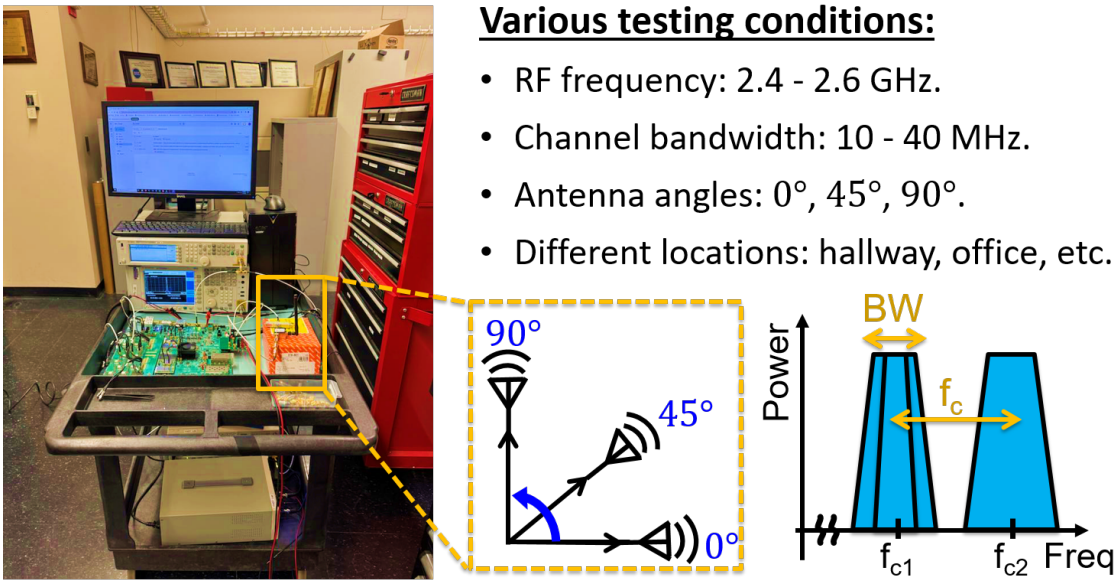


Figure 6.8: Testing setup and conditions for training data collections, including the carrier frequency and bandwidth of the SI signal, antenna angles, and radio positions.

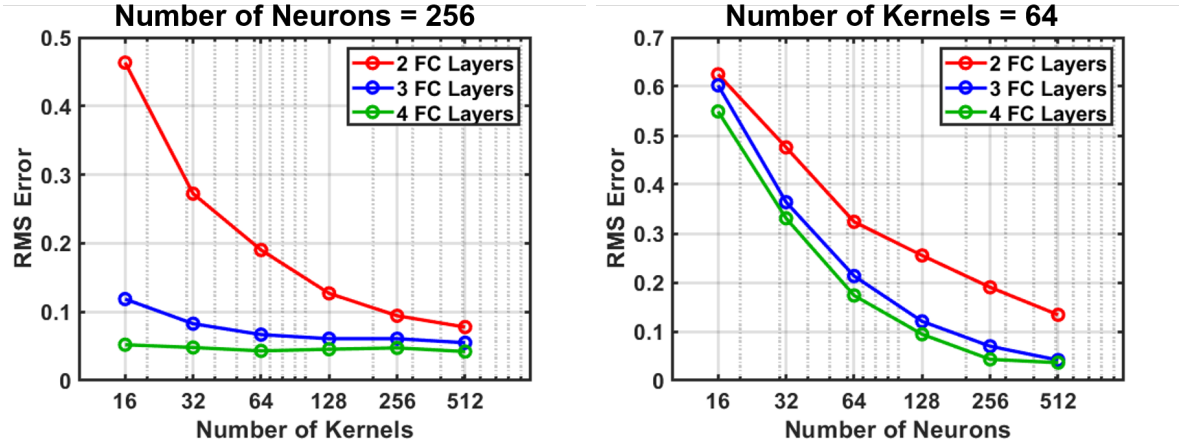
the need to pre-measure all possible canceler settings, as required in [24, 27], thereby enhancing scalability as the number and resolution of tuning parameters increase in future designs. Additionally, incorporating a convolutional layer helps effectively reduce the parameter count and training time [94], thereby saving both hardware resource utilization and power consumption. Compared to the NN architecture in [92] that relies solely on FC layers, the proposed NN directly uses the time-domain data for adaptation, reduce its dependence on FC layers, and the total number of FC layers. The detailed training process and NN design parameters are discussed in the next section.

6.4.2 Neural Network Training

The training dataset for this design is collected using a radio transceiver built upon discrete RF components, operating with the RF canceler chip described in Section 6.3. Testings are conducted across various indoor wireless environments, such as offices and hallways. The

dataset includes variations in carrier frequency, signal bandwidth, and antenna position, as shown in Fig.6.8. With a sufficiently diverse set of measured data, the trained NN can effectively capture the canceler's behavior under voltage and temperature variations. For each data point, canceler settings optimized using traditional algorithms, such as the pseudo-blind search algorithm [18], serve as the ground truth for NN training. The measured input samples t[n] and r[n] (Fig.6.3), along with their corresponding ground-truth canceler settings, are utilized to train the NN in Matlab. The Adam optimization algorithm is employed to compute all NN parameters, including kernel values in the convolutional layer, and weights and biases in FC layers, as shown in Fig.6.7. The training process begins with an initial learning rate of 0.0002, which decays by a factor of 0.95 every 20 epochs to ensure smooth convergence. A batch size of 128 is used with training running for up to 1000 epochs. Model validation is performed every 500 iterations using a test dataset comprising 20% of the total samples within the dataset. The CNN architecture consists of a single convolutional layer with 64 kernels of size 1×16, followed by a global average pooling layer and two FC layers, each consisting of multiple neurons with a ReLU activation function. Batch normalization is applied at the input of each ReLU activation to accelerate training, and a dropout layer with a dropout ratio of 0.5 is used to prevent overfitting. The measured dataset includes over 57,000 samples, with 80% allocated for training and the remaining 20% reserved for validation.

The training accuracy of the proposed NN is influenced by various factors within the NN architecture, including the number of kernels, the number of FC layers, and the number of neurons in each FC layer. To compare different NN configurations, training is performed by varying these parameters, and the normalized validation root mean square (RMS) error is used to assess training accuracy. Fig.6.9a shows the simulated normalized RMS error as the number of kernels and FC layers (ranging from 2 to 4) is varied, with 256 neurons in each FC layer. Since the number of kernels corresponds to the number of different characteristic impulse responses used to model real wireless channel information, the RMS error decreases, and training prediction accuracy improves as the number of kernels increases. Additionally, it



(a) (b)

Figure 6.9: Normalized validation RMS errors of the proposed neural network by varying (a) the number of kernels and (b) the number of neurons with different FC layers.

is observed that when the number of FC layers is larger than two, the reduction in RMS error begins to diminish when the number of neurons exceeds 64. Fig.6.9b shows the simulated normalized RMS error as a function of neuron count with 64 kernels. Increasing the number of neurons in the FC layer helps reduce the RMS error and improves NN prediction accuracy by utilizing more parameters to characterize the input-output relationship. However, this also results in higher hardware resource utilization, increased power consumption, and longer training times.

Due to the trade-off between accuracy and hardware resources, the NN described in Fig.6.7, with 64 kernels, 3 FC layers (including the output layer), and 200 neurons per FC layer, is utilized in this design. This design choice achieves a normalized RMS error of approximately 0.08, corresponding to less than 9 LSB for the 8-bit weight coefficients used in the canceler chip. Fig.6.10 shows a detailed breakdown of the NN's layer functions. The NN takes 128 digital samples from both the TX reference path t[n] and the receiver path r[n] ADCs at a time (as shown in Fig.6.3). The convolved t[n] with 64 kernels are subtracted from

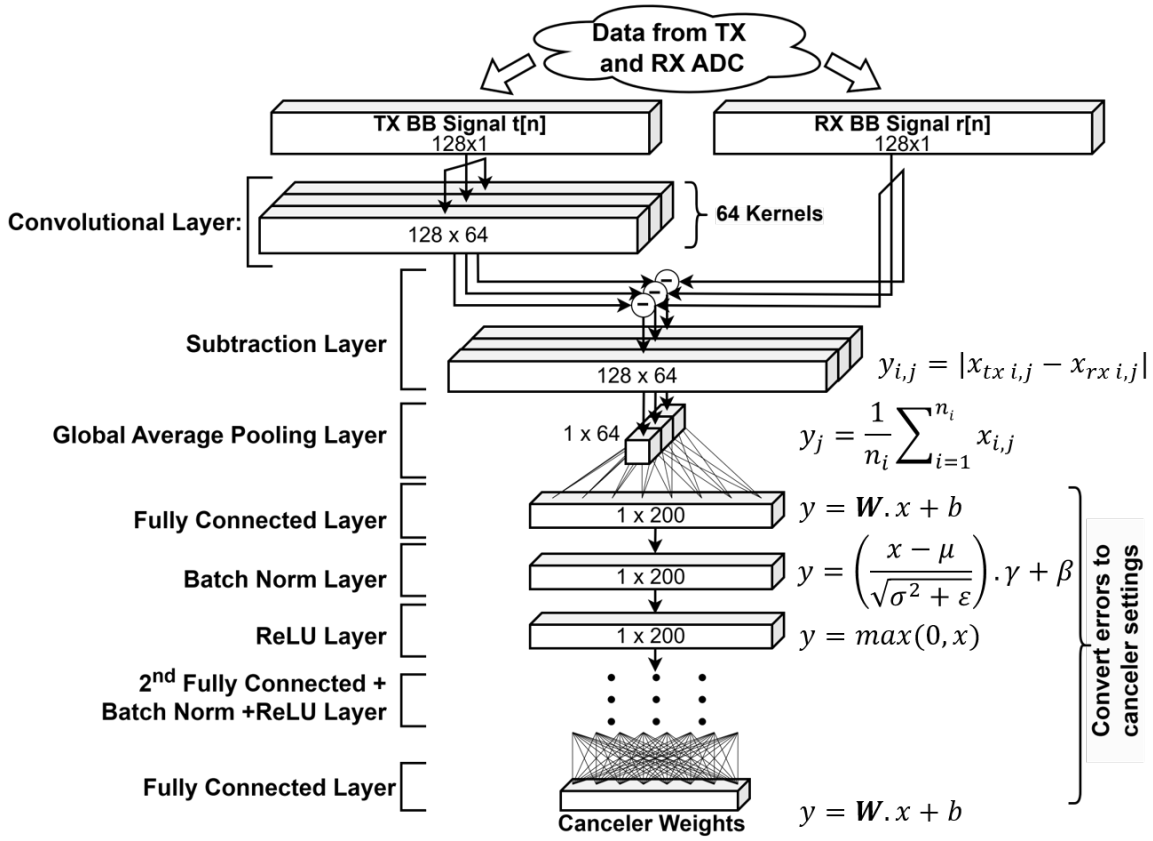


Figure 6.10: Detailed layer implementations of the proposed NN for adapting the SI canceler chip, including convolutional, pooling, and fully connected layers.

r[n] to calculate their absolute difference, producing an error map. This is then down-sampled by a pooling layer, which averages its elements. The output of the pooling layer shows the performance of using multiple kernels to model the SI leakage frequency response. Finally, a standard deep NN, consisting FC layers (for matrix multiplication and addition), a batch normalization layer (for input normalization), and a ReLU layer (for nonlinear activation), converts the averaged error into optimized canceler settings.

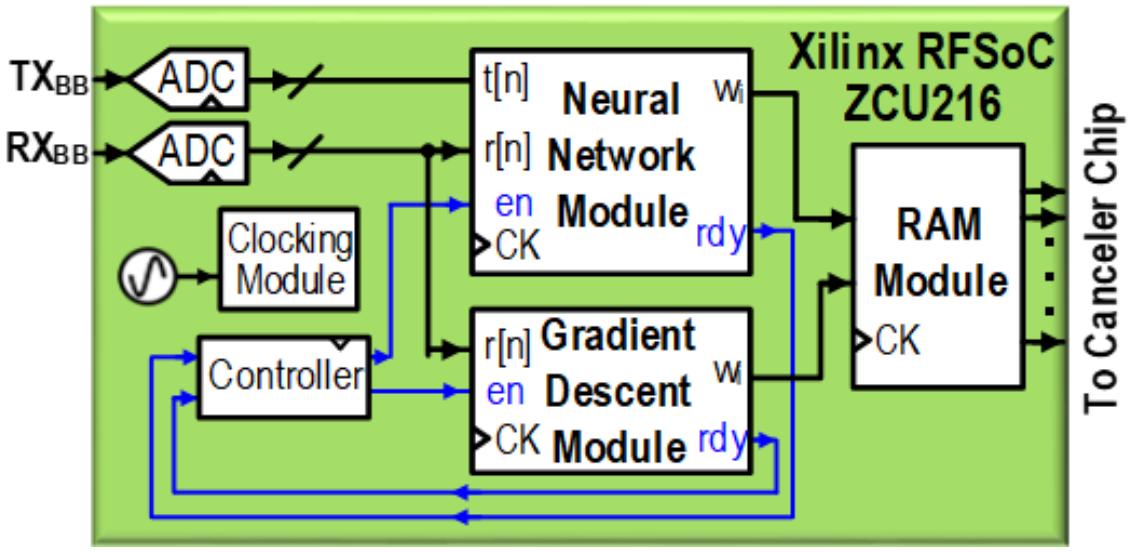


Figure 6.11: Block diagram of the ML-augmented adaptation algorithm implemented on the Xilinx ZCU216 RFSoC.

6.4.3 Algorithm Hardware Implementation

The proposed ML-augmented algorithm is implemented as RTL modules and integrated with ADC modules on a Xilinx ZCU216 SoC. Fig.6.11 shows the block diagram of the implementation with key modules and their interfaces. The ADCs digitize the baseband outputs from both the TX reference path and receiver path into 14-bit signals, which are then processed by the NN module to generate the initial canceler settings. These settings also serve as starting points for the gradient descent module, which further fine-tunes the canceler parameters. The RAM module in Fig.6.11 stores the canceler settings computed by both the NN and gradient descent modules, converts them into a serialized output, and finally send them to the canceler chip. The clocking module generates multiple clock signals at different frequencies to meet the timing requirements of various system components.

Fig.6.12 shows the RTL implementation of key layers within the NN. A computation node that performs $y = \Sigma w_i x_i + b_i$ serves as the fundamental building block for various NN layers. Here, y and x_i represent the output and input data, respectively, while w_i and b are the node's

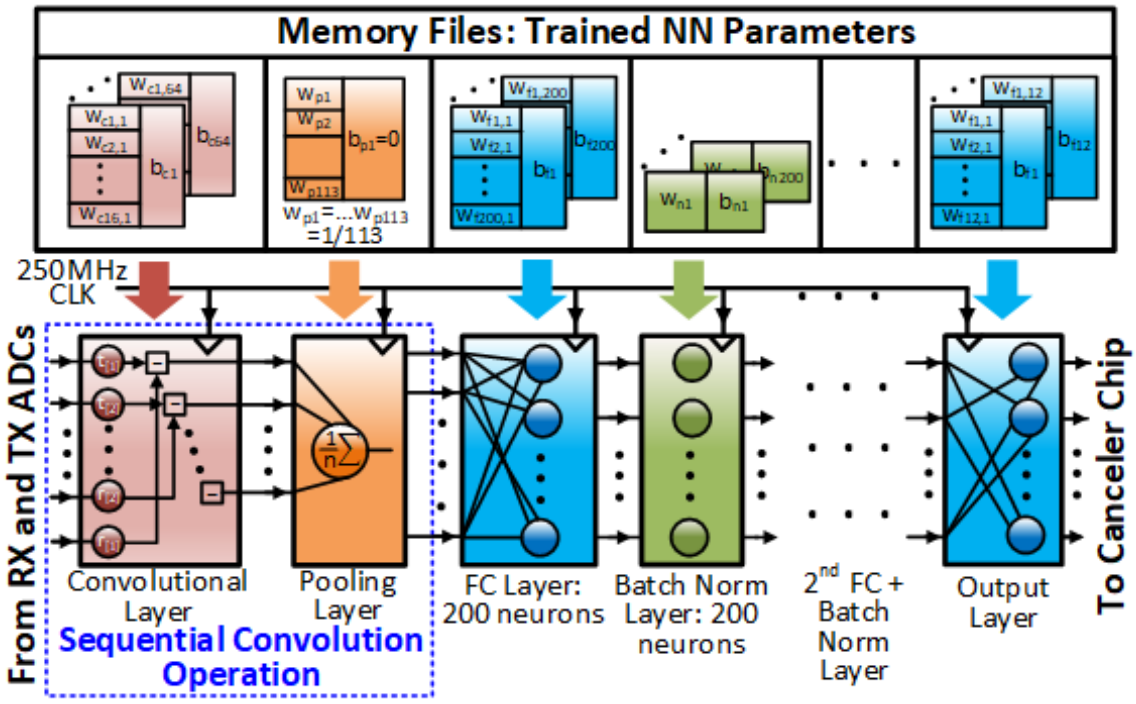
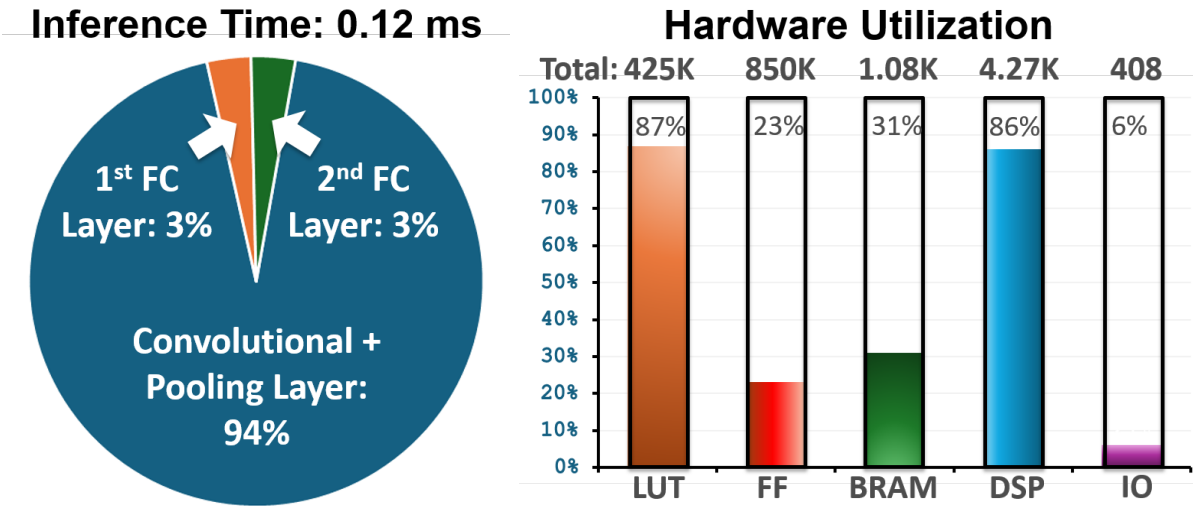


Figure 6.12: RTL implementation of key neural network layers on FPGA.

trained weights and biases stored in memory files as shown in Fig.6.12. The convolutional layer applies a kernel of length 16 to t[n], performing an inner product calculation at each position as it slides across the input data t[n]. The resulting convolved outputs, which have a data length of 113, are then subtracted from r[n]. The pooling layer is implemented by assigning equal weights ($w_{pi} = \frac{1}{113}$ for kernel length of 16) to all input elements and setting the bias (b_{p1}) to zero. To reduce resource utilization, convolution and pooling operations are executed sequentially for each of the 64 kernels, with results stored in a serial-in parallel-out shift register. The fully connected layer performs standard multiplication and addition operations for each input using the trained parameters ($w_{fi,j}$ and b_{fi}) stored in the memory files. The batch normalization layer applies a normalization function (Fig.6.10) using w_n and b_n, while the ReLU activation function (also shown in Fig.6.10) is merged into this stage. Once all operations are completed, the NN module asserts the "rdy" signal high (Fig.6.11).



(a) (b)

Figure 6.13: (a) Inference time (computation latency) and (b) Inference time (computation latency) and (b) hardware utilization of the NN on the FPGA, including lookup tables (LUTs), flip-flops (FFs), block RAM (BRAM), digital signal processing (DSP) units, and input/output (IO) pins.

The RAM module in Fig.6.11 then retrieves the NN output and sends them to the canceler chip. All data paths in the NN use a 32-bit resolution, with 4 bits allocated to the integer part and 28 bits to the decimal part, ensuring accurate calculations with minimal rounding errors.

Post-synthesis simulation in Vivado shows that the proposed NN, operating at a clock frequency of 250 MHz, achieves an overall inference time of approximately 0.12 ms. As shown in Fig.6.13a, 94% of this time is consumed by the sequential convolution operations of multiple kernels in the convolutional layer. The inference time can be reduced by parallelizing the convolution operations, albeit at the cost of increased resource utilization. Fig.6.13b shows the hardware utilization of the NN algorithm on the FPGA. Due to the extensive multiplication and addition operations within the NN, the implementation predominantly

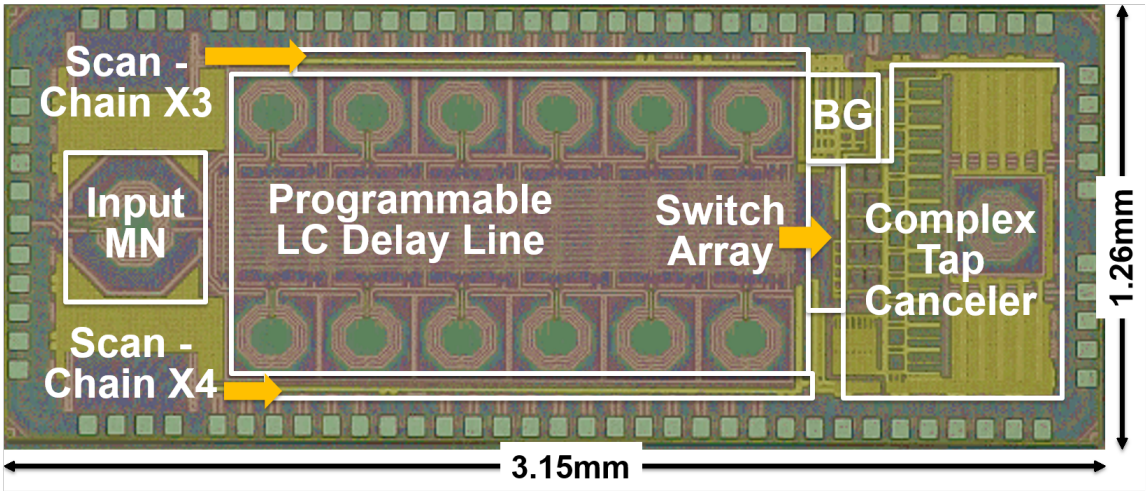


Figure 6.14: Die photograph of the RF SI canceler CMOS chip.

utilizes lookup tables (LUTs) and digital signal processing (DSP) units. While the NN's prediction accuracy can be improved by increasing the number of FC layers and neurons (shown in Fig.6.9a and 6.9b), it will require additional hardware resources. The total power consumption of the NN in FPGA is about 211 mW, with 51% attributed to logic operations (e.g., matrix addition and multiplication) and 47% to data transitions. Implementing the NN algorithm using application-specific integrated circuits (ASICs) could significantly further reduce inference time and power consumption, as matrix operations within the NN can be extensively optimized using custom-designed on-chip blocks.

6.5 Chip and System Measurement Results

The RF SI canceler chip, fabricated using a TSMC's 40 nm CMOS process, occupies a total area of 4 mm^2 and operates with 1.0 V and 1.8 V supply voltages. The active area of the core canceler circuit, including the PDL and the complex tap filter, is about 1.8 mm^2, as shown in Fig.6.14. The ML-augmented adaptation loop including both the NN and gradient descent optimization algorithms is implemented on the FPGA of the Xilinx ZCU216 RFSoC, which emulates the DBE of the FD transceiver. The DBE computes the canceler settings

Algorithm 1 Algorithm for Adapting the Canceler

Input: Multiple independent dither sequences δ_i and a convergence factor μ.

Result: Minimize power of r[n] ($e^2[n]$) aiming at $e^2[n] < e^2_{th}$.

Initialize canceler settings using NN-computed results $w_i[0]$.

1: **while** $e^2[n] > e^2_{th}$ **do**

2: Apply dither sequences: $w'_i[n+1] = w_i[n] + \delta_i[n]$.

3: Measure residual SI power $(e'[n+1])^2$

4: Update canceler settings: $w_i[n+1] = w_i[n] - \mu\delta_i[n]\{(e'[n+1])^2 - (e[n])^2\}$.

5: Measure residual SI power again $(e[n+1])^2$.

6: **end while**

and sends them to each filter tap via six on-chip shift registers operating at a 25 MHz clock rate. This clock rate is primarily limited by the speed of the level shifters on the test board, which can be significantly improved by integrating the level shifters on the same chip.

6.5.1 Canceler Adaptation Performance

In the canceler adaptation loop, ADCs on the RFSoC, operating at a 250 MSPS sampling rate, convert the reference TX and RX baseband signals into the digital domain. A modified dithered linear search (DLS) algorithm, shown in Algorithm 1, uses the initial canceler settings provided by the NN to further optimize SI cancellation. This algorithm operates as a gradient descent optimizer, calculating the gradient at each iteration by simultaneously applying multiple dither sequences $\delta_i[n]$ to the previous weight values $w_i[n]$. Each dither sequence $\delta_i[n]$ is a 16-bit Hadamard sequence with values of either +1 LSB or -1 LSB. The DLS algorithm in this design leverages the power difference of the residual SI before and after applying $\delta_i[n]$ to calculate the gradient, which enhances algorithm's stability compared to [90]. In addition, Algorithm 1 in this design requires less processing and computation per iteration, reducing both algorithm execution time and resource consumption compared to [24, 87]. Beyond adapting the canceler weight values, the modified DLS algorithm can

Canceler Convergence Iteration

	Iteration (PBS)	Iteration (NN + PBS)	Iteration (Gradient Descent)	Iteration (NN + Gradient Descent)
Initial Can	NA	1	NA	1
Final Can	~ 1.2e8	~ 28e3	~ 30e3 – 100e3	~ 2e3 – 5e3

(a)

Canceler Convergence Time

	Time (PBS)	Time (NN + PBS)	Time (Gradient Descent)	Time (NN + Gradient Descent)
Initial Can	NA	0.12ms	NA	0.12ms
Final Can	~ 250s	~ 60ms	~ 62ms – 208ms	~ 4.3ms – 10.5ms

(b)

Figure 6.15: (a) Number of iterations and (b) convergence time of SI cancellation using pseudo-blind search, gradient descent (Algorithm 1), and NN-augmented adaptation algorithms.

be applied to adjust other cancellation-related tuning parameters [95], such as delay spread and bias current. This extends its capabilities beyond previous optimization algorithms that focus on weight coefficients [54–56]. However, since these additional parameters share a single long shifter register in this design, the convergence time of the canceler is limited by the time needed to update these settings.

The proposed ML-augmented adaptation algorithm significantly accelerates the canceler's convergence compared to traditional optimization algorithms. Fig.6.15a compares the number of iterations required for convergence using different approaches. For a six-tap complex FIR filter, the post-trained NN determines the initial canceler settings in a single iteration. The canceler adaptation process then typically completes in 2,000 to 5,000 iterations using the gradient descent method in Algorithm 1 and 28,000 iterations with the pseudo-blind search (PBS) method. This corresponds to a reduction of about 10 times in iterations compared to Algorithm 1 and more than 1000 times compared to the PBS method [18], when both are initialized from an all-zero filter state.

Fig.6.15b shows the measured canceler convergence time when tested with a QPSK-modulated signal. The NN's computation time is approximately 0.12 ms at a clock frequency

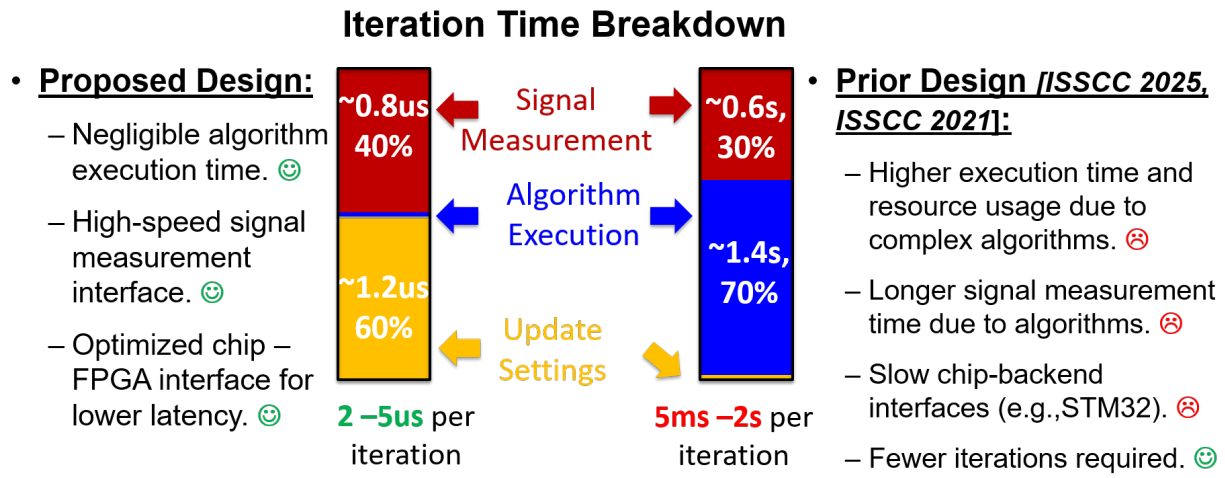


Figure 6.16: Comparison of iteration time breakdown between the proposed adaptation algorithm (Algorithm 1 or PBS method) and prior SI canceler adaptation methods [24, 87].

of 250 MHz. Each iteration of both the gradient descent method (Algorithm 1) and the PBS method consists of two main components: measuring the residual SI power (accounting for approximately 60% of the iteration time) and updating the on-chip canceler settings from the FPGA DBE (approximately 40%). The time required for both components is minimized by optimizing the chip-FPGA interface design, including high-speed data converters and the FPGA mezzanine card plus (FMCP) connector on the Xilinx RFSoC board. Since the algorithm execution time per iteration (Fig.6.15a) is completed within a single clock cycle, it is negligible compared to these two main components, as shown on the left side of Fig.6.16. In contrast, the iteration time in prior works such as [24, 57, 87], is dominated by computationally intensive algorithms like Bayesian optimization [87] and the signal measurement times required by these algorithms, as shown on the right side of Fig.6.16. For example, in [87], signal measurements and algorithm execution account for approximately 30% and 70% of the total iteration time, respectively, with each iteration taking about 2 seconds and a total convergence time of approximately 800 seconds. In comparison, the proposed NN-assisted algorithm achieves final SI cancellation in 4.3-10.5 ms using Algorithm 1 and approximately

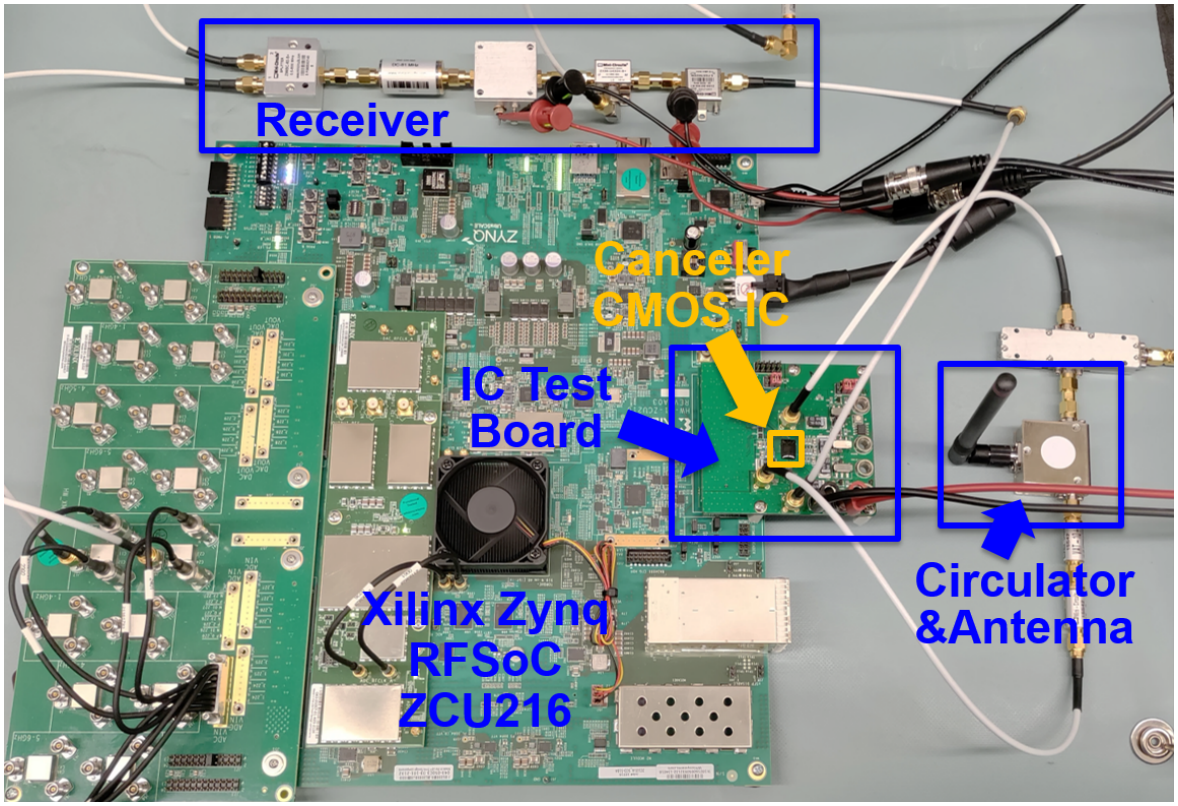
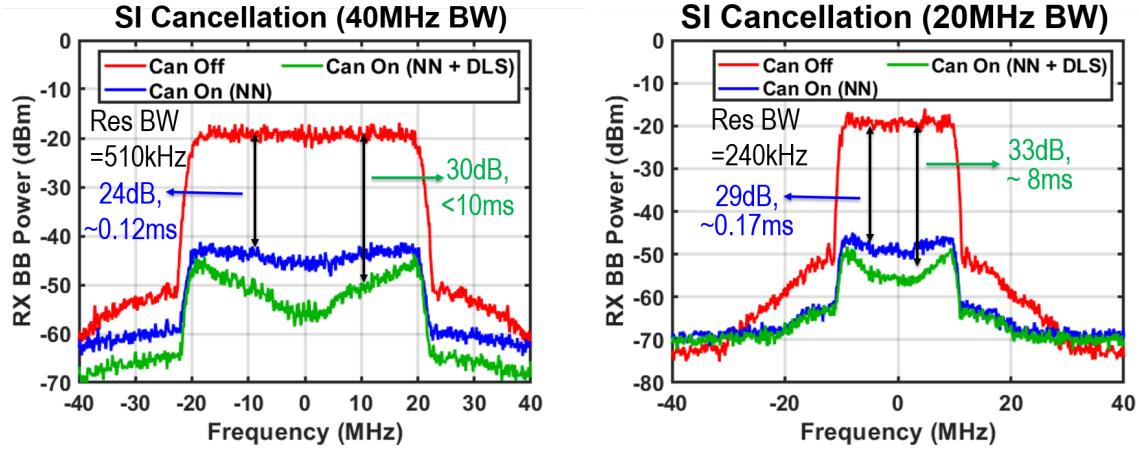


Figure 6.17: Test setup of the RF canceler chip interfacing with a circulator terminated with an antenna and a Xilinx RFSoC running ML-augmented algorithms for optimizing SI cancellation.

60 ms with the PBS method [18], as shown in Fig.6.15b. Implementing the NN-augmented algorithm as an ASIC on the same die as the SI canceler and transceiver can further reduce the convergence time by leveraging higher-speed clocks and dedicated digital control buses.

6.5.2 SI Cancellation Measurement

To evaluate the SI canceler chip's performance in a real wireless environment, SI cancellation measurements were performed in various indoor environments, including an office and a hallway. The test setup, shown in Fig.6.17, includes an Agilent E4438C vector signal generator to provide input signals to a discrete PA. Initial SI attenuation at the radio air interface

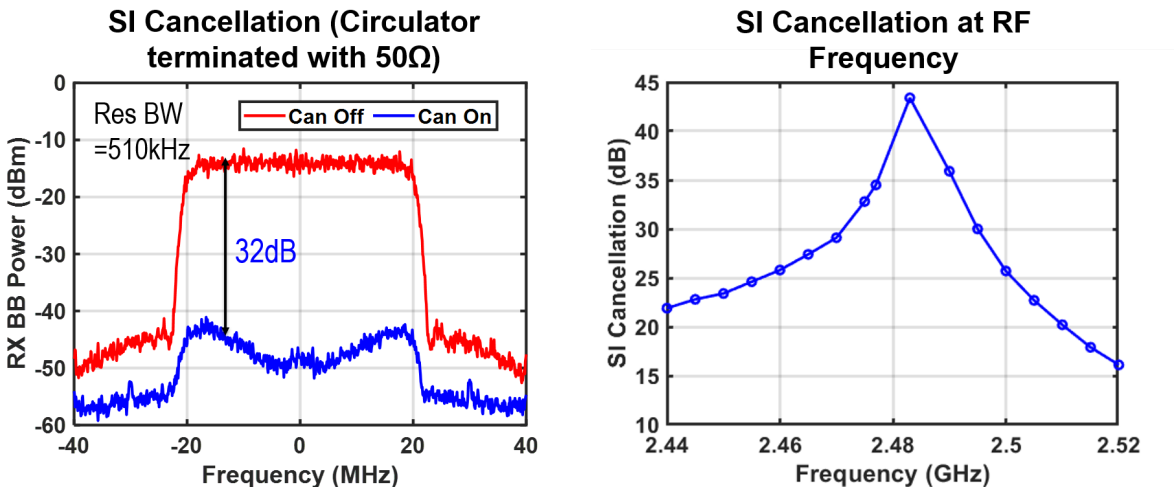


(a) (b)

Figure 6.18: Measured SI spectrum at the receiver analog baseband output after SI cancellation using the NN-augmented algorithm for (a) 40 MHz and (b) 20 MHz modulated signals.

is achieved using a MECA Electronics CS-2.500 RF circulator, which is terminated with a Linx Technologies ANT-2.4-CW-HWR-SMA dipole antenna. The receiver chain consists of commercially available RF components including an LNA, mixer, baseband amplifier, and low-pass filters. Fig.6.18a and 6.18b show the measured SI spectrum at the receiver ADC input before and after SI cancellation in the office environment. The canceler input signal power is about +6 dBm, which corresponds to a PA output power of +18 dBm when the PA output is connected to a directional coupler with a 12 dB coupling factor (as specified by our contractor). For a 40 MHz / 20 MHz QPSK-modulated signal, the ML-augmented algorithm provides an initial average SI cancellation of 25 dB / 30 dB across the bandwidth in approximately 0.12 ms, which is followed by gradient descent adaptation using Algorithm.1. Ultimately, the canceler achieves 29 dB / 33 dB of SI cancellation across the 40 MHz / 20 MHz bandwidth, typically in less than 10 ms.

SI cancellation was further measured with the circulator's antenna port terminated with a 50 Ω resistor to characterize the system's maximum cancellation capability. Under this



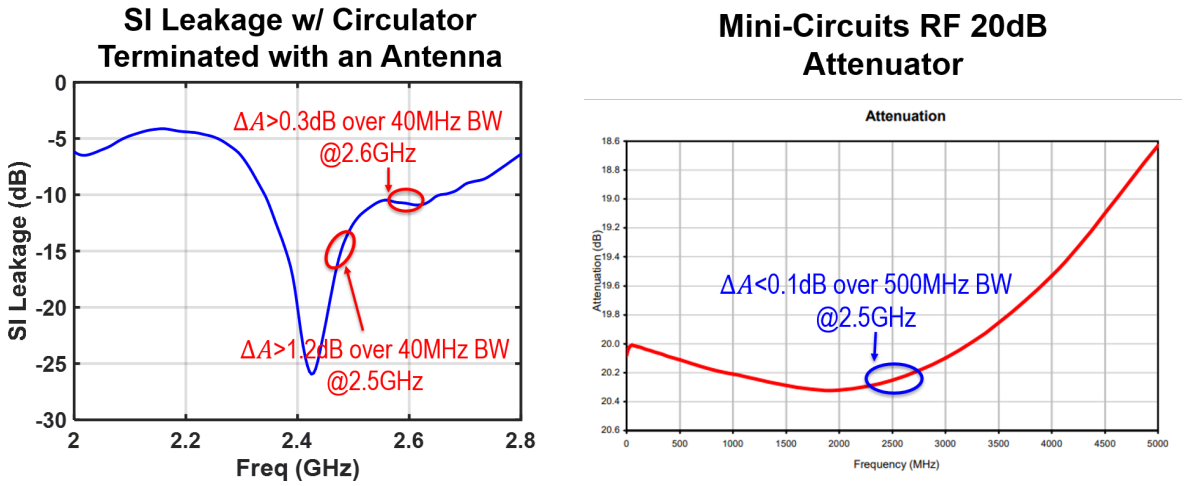
(a) (b)

Figure 6.19: (a) Measured SI spectrum at the receiver's analog baseband output before and after cancellation, with the circulator's antenna port terminated with a 50 Ω load. (b) Measured SI cancellation at the RF carrier frequency using the same canceler setting.

setup, the circulator path provides an initial SI attenuation of about 34 dB. Fig.6.19a shows the measured SI spectrum at the receiver ADC input for a 40 MHz modulated signal, where the canceler achieves an average cancellation of 32 dB across the bandwidth. Fig.6.19b shows the measured SI cancellation referred to the RF carrier frequency for a single-tone input, using the same canceler settings, with a maximum SI cancellation of approximately 43 dB.

6.5.3 Post-Cancellation SI Spectrum Discussion

As shown in Fig.6.18a and Fig.6.19a, the residual SI spectrum after cancellation shows a notch-shaped profile: higher cancellation is achieved near the center of the frequency band, while lower cancellation is observed at the band edges. This behavior is caused by two factors: the frequency response flatness of the SI leakage (as discussed in Chapter 3) and the delay mismatch between the canceler and the SI leakage path. To investigate these effects,



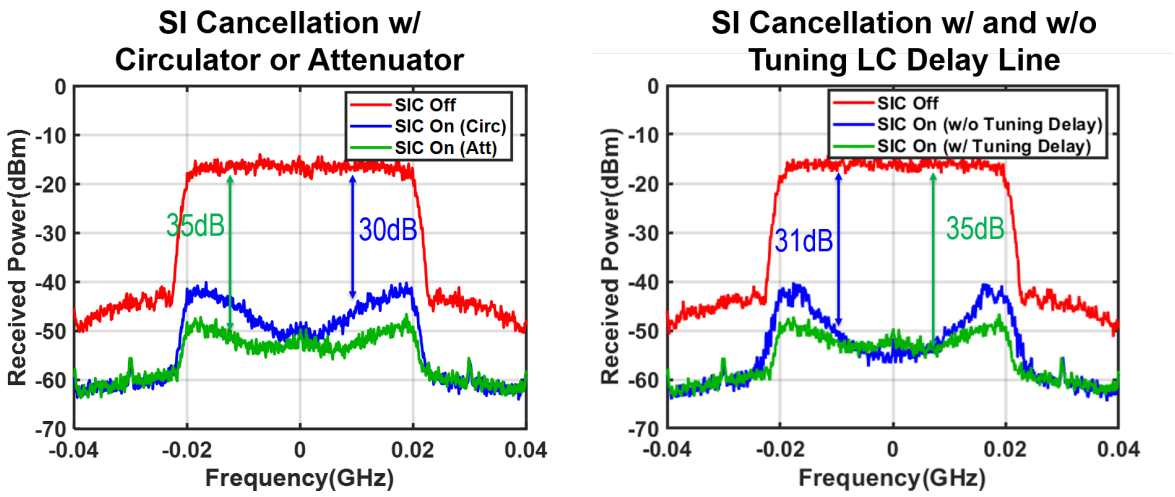
(a) (b)

Figure 6.20: (a) Measured SI leakage amplitude response when circulator is terminated with a dipole antenna. (b) Amplitude response of a Mini-Circuits RF attenuator [96] used to mimic the frequency response of SI leakage.

a series of measurements were conducted.

First, two different frequency responses were used to model the antenna-air-interface SI leakage, and their corresponding cancellation was compared using the same canceler chip developed in this work. Fig.6.20a shows the measured SI leakage amplitude response of the circulator (described in Section 6.5.2) when its antenna port is terminated with a dipole antenna. At the center frequency of about 2.5 GHz, the amplitude variation is approximately 1.2 dB across a 40 MHz bandwidth. In contrast, when the SI leakage is emulated using a Mini-Circuits RF attenuator [96], the amplitude variation is less than 0.1 dB across a 500 MHz bandwidth centered at 2.5 GHz, showing a significantly flatter frequency response.

The corresponding measured residual SI spectrum after cancellation for the two SI leakage models are shown in Fig.6.21a. In these measurements, the average attenuation level of the SI leakage modeled by the RF attenuator (Fig.6.20b) is adjusted to match that of the

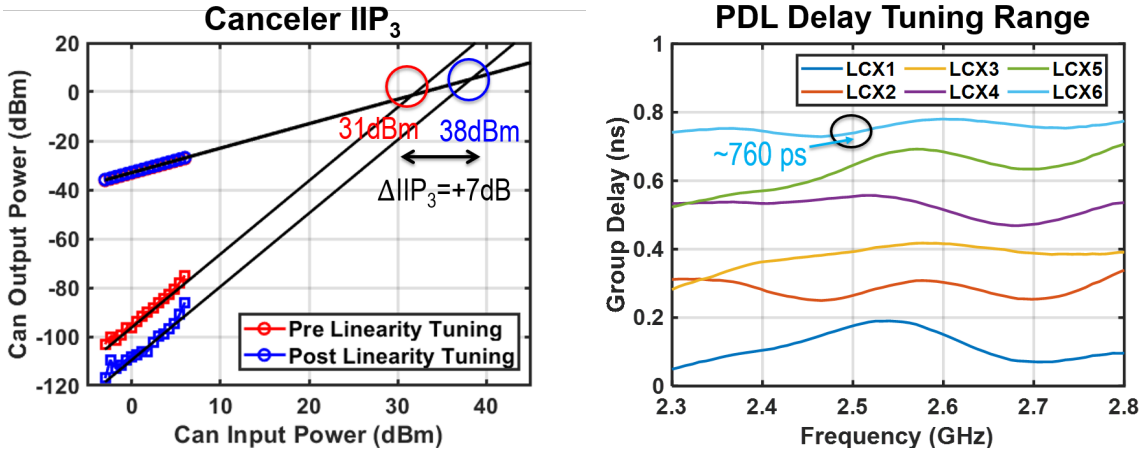


(a) (b)

Figure 6.21: (a) Measured residual SI spectrum at the receiver's analog baseband output for the two SI leakage profiles shown in Fig.6.20a and 6.20b. (b) Measured residual SI spectrum with and without tuning the LC delay line, when the SI leakage is modeled using RF attenuators.

circulator-antenna setup (Fig.6.20a). For both cases, the delay spread of the LC delay line and the complex tap filter coefficients are optimized to maximize cancellation. As shown in Fig.6.21a, an average cancellation of about 35 dB is achieved across a 40 MHz bandwidth when using the RF attenuator-based model, which is 5 dB higher than the cancellation obtained with the circulator-antenna model. This improvement is attributed to the flatter frequency response of the RF attenuator, as shown in Fig. 6.20b. To improve cancellation depth over wider bandwidths in future FD radio designs, the circulator's frequency response can be flattened using an impedance tuner or a higher-order matching network [48], thereby improving spectrum flatness of the residual SI..

Second, the shape of the post-cancellation SI spectrum is also influenced by the delay matching between the canceler and SI leakage path. Measurements were performed to com-



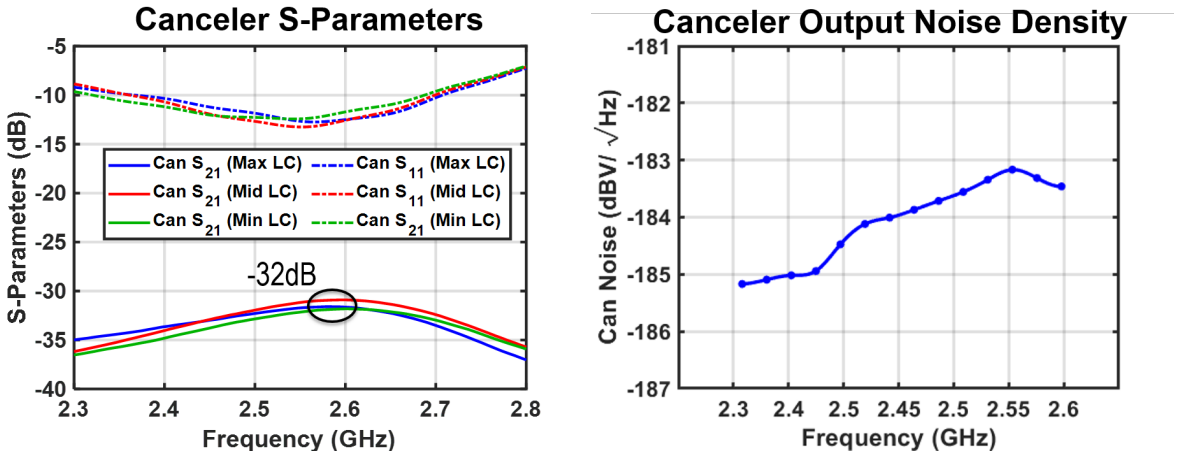
(a) (b)

Figure 6.22: (a) Measured canceler IIP_3 referenced to a 50 Ω input impedance, before and after linearity tuning. (b) Measured delay spread of the programmable delay line after passing across various LC stages.

pare cancellation performance with and without tuning the delay spread of the canceler, as shown in Fig.6.21b. The delay tuning is achieved by adjusting the delay spread of the LC delay line, as described in Section 6.3 in this design. As shown in Fig.6.21b, co-optimizing the delay spread and canceler filter tap coefficients improves the average cancellation from 31 dB to 35 dB over a 40 MHz bandwidth. Therefore, techniques to further enhance both the delay spread coverage and resolution are required to improve SI cancellation in future canceler designs.

6.5.4 SI Canceler RF Metrics

To measure the SI canceler chip's performance under high-power multi-carrier signals, its linearity was optimized, and the input third-order intercept point (IIP_3) of the canceler was measured using a two-tone test, as shown in Fig.6.22a. Two equal-amplitude signal tones spaced 10 MHz apart were applied to the canceler input. After calibration using independent



(a) (b)

Figure 6.23: (a) Measured canceler input return loss (S_{11}) and gain (S_{21}) with various PDL switch settings. (b) Measured canceler output noise density.

current DACs for each filter tap (Section 6.3), the canceler achieves a maximum IIP_3 of +38 dBm (referenced to a 50 Ω input impedance) at an input power level of +6 dBm. This represents an improvement of approximately 7 dB compared to the canceler without linearity tuning and a 5 dB enhancement over the design in [18] when referenced to the same input impedance. Fig6.22b shows the measured delay tuning range of the LC delay line across various switch settings. The PDL provides an adjustable delay spread ranging from 0 to 760 ps at 2.5 GHz. The total measured maximum delay spread of the canceler chip, including the group delay contributions from the input and output matching network and the 6-tap FIR filter, is about 2 ns.

The measured input return loss (S_{11}) of the canceler is better than -10 dB across 2.4-2.7 GHz for various switch settings, as shown in Fig.6.23a. The canceler achieves a nominal gain of approximately -32 dB with different PDL configurations when the first filter tap is enabled. The measured output noise density of the canceler is about -184 dBV/$\sqrt{Hz}$ at 2.45 GHz (Fig.6.23b), which results in a receiver noise figure (NF) degradation of about 1.8 dB

when assuming an initial receiver NF of 6 dB.

Table.6.1 compares the proposed SI canceler chip with previous integrated and on-board RF canceler solutions. The proposed design demonstrates enhanced linearity over prior integrated implementations and achieves state-of-the-art SI cancellation performance. The ML-augmented canceler adaptation algorithms significantly accelerate convergence time compared to previous integrated, digitally tunable RF cancelers. Additionally, the design supports a greater number of tuning parameters with higher resolution than most prior solutions. Integrating the radio DBE with the canceler and AFE on a single chip is expected to further reduce convergence time by leveraging higher clock speeds.

6.6 Conclusion

This chapter demonstrates a highly tunable RF SI canceler chip operating with an ML-augmented adaptation algorithm. By combining a custom-designed neural network with a gradient descent algorithm, the adaptation convergence time is improved compared to previous integrated, digitally controlled cancelers. The canceler achieves an IIP_3 of +38 dBm and provides 30 dB of SI cancellation over a 40 MHz bandwidth in wireless environments, representing state-of-the-art performance. To the best of our knowledge, this work is the first implementation of an ML-augmented algorithm deployed at the RTL level to adapt an integrated RF SI canceler for FD radio systems.

Table 6.1: Performance Comparison Table with Prior Integrated or Discrete RF SI Cancelers

	This Work	**JSSC [18]**	**ISSSC [24]**	**JSSC [27]**	**JSSC [55]**	**TMTT [89]**	**OJSC [92]**	**TMTT [57]**
Adaptation Algorithm	ML-Augmented Gradient Descent	Pseudo-Blind Search	Frequency Domain Optimization w/ a LUT[d]	Frequency Domain Optimization w/ a LUT[d]	Analog Least Mean Square	Gradient Descent	Deep Neural Network	Linear Solver w/ a LUT[d]
Digital-Control Capability?	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes
Technology	CMOS 40nm	CMOS 40nm	CMOS 65nm	CMOS 65nm	CMOS 65nm	PCB	PCB	PCB
Frequency (GHz)	2.4 - 2.7	2.1 - 2.5	0.1 - 1.0	0.9	0.5 - 2.5	2.4 - 2.5	2.5	6.7
RF SIC (dB) / BW (MHz)	32 / 40	33 / 40, 28 / 120[b]	30 / 40	52 / 20	29 / 20	30 / 30	40 / 20	22 / 400
Weight Tuning Parameters	12	10	16	6	2	8	4	8
Weight Resolution (bit)	8	7	6	>13	N.A.	12	N.R.	12
Convergence Iteration	2000 - 5000	$\sim$ 6.3e8	3	N.A.	N.A.	$\sim$ 500	6-20	1
Convergence Time (ms)	4.3 - 10.5	127e3	15[e]	N.A.	1e-3	0.5[h]	5.9e-3[h]	$\sim$ 3
RF Canceler Delay (ns)	2	0.28	7.75	80[f]	3[g]	6	$\sim$ 1[g]	6
Canceler IIP_3 (dBm)	38	42[c]	N.R.	23	N.R.	N.R.	N.R.	N.R.
Canceler Power (mW)	39	35	118.4	44.4	16 - 52	N.R.	N.R.	N.R.
RF SIC NF Degradation (dB)	1.8[a]	1.7	0.8 - 2.8	1.75	1.2	N.R.	N.R.	1.5 - 6.5
Active Chip Area (mm^2)	1.8	0.2	1.6	0.63	0.4	N.A.	N.A.	N.A.

[a] NF degradation calculated by assuming an RX NF of 6 dB. [b] SI cancellation achieved by two RF cancelers. [c] Canceler IIP_3 referred to an R_{Opt} of about 6Ω for the PA. [d] The algorithms in [24, 27] require pre-measurement of the canceler's frequency response under various settings. [e] Algorithm optimization time required in Matlab, excluding communication time between the algorithms and the canceler chip. [f] The canceler reference signal is delayed at the analog baseband, then up-converted to RF frequency to cancel SI at the RX input. [g] Canceler delay estimated from the group delay at the antenna-air interface. [h] Time required for collecting digital samples, excluding algorithm processing time and the time needed to update the canceler circuits. N.A.: Not applicable. N.R.: Not reported.

Chapter 7

CONCLUSION AND FUTURE WORK

The increased demand for higher data rates and lower latency in future 5G and 6G communications, along with emerging wireless applications, necessitates more efficient utilization of the RF spectrum between 1-6 GHz. This dissertation proposed methods to address key challenges in implementing practical in-band FD radio systems focusing on two main aspects: 1) Utilizing a divide-and-conquer approach to mitigate multi-path SI reflections within an FD transceiver front-end. 2) Leveraging AI algorithms to assist the adaptation of a highly tunable RF SI canceler chip.

7.1 Dissertation Summary

The dissertation first presents a theoretical analysis of analog FIR filter design considerations for SI cancellation in FD radios. Two FD ICs, based on these design guidelines, have been designed, fabricated, and tested in various environments to demonstrate their SI mitigation capabilities.

The first prototype chip, discussed in Chapter 5, implements an FD transceiver front-end featuring four SI cancellation paths to mitigate both short- and long-delay sprea SI across a wide bandwidth. Measurements results demonstrate 62 dB SI cancellation for delay spreads up to 0.28 ns and 23 dB cancellation for delay spreads up to 174 ns, across a 120 MHz bandwidth. Additionally, by incorporating linearity enhancement techniques within the canceler's filter taps, the RF SI canceler achieves a measured IIP_3 of +42 dBm. However, two major limitations remain: 1) The SI cancellation adaptation process relies on a traditional pseudo-blind search algorithm, which takes over 120 seconds, which does not meet the low-latency requirements of future communication systems. 2) The RF canceler has insufficient

tuning capabilities, such as delay spread, which could limit its effectiveness and adaptability in dynamic wireless environments.

To address these challenges, the second prototype chip, as described in Chapter 6, introduces a highly tunable RF SI canceler with AI-augmented adaptation algorithms. Designed as a plug-in for 2.4 GHz transceivers, this canceler IC supports SI cancellation for FD operation by independently tuning key parameters such as filter tap gain, phase, delay spread, and linearity. Measurements show that the canceler achieves 32 dB SI cancellation across a 40 MHz bandwidth in real-world wireless testing, with notable improvements in linearity and delay spread of approximately 5X and 7X, respectively. Additionally, an AI-augmented algorithms, implemented on a Xilinx RFSoC, enables rapid optimization of the canceler's settings within 10 millisecond, significantly reducing convergence time compared to traditional method. This work successfully demonstrates an RF SI canceler chip with enhanced tunability, deeper SI suppression, and significantly faster adaptation, making it a promising solution for practical FD radio systems in next-generation wireless networks.

7.2 Future Research Directions

The proposed FD transceiver front-end with ML-augmented SI cancellation adaptation presented in this dissertation achieves deep cancellation across a wide bandwidth while significantly accelerating the adaptation process. The next step is to develop a highly programmable single-radio solution capable of handling both self-interference and broadband interference while optimizing cost and power consumption. Beyond wireless radios, the techniques presented in this dissertation could also be extended to mitigate interference in quantum computing systems, particularly in the qubit readout process, which could contribute to potential advancements in in quantum computing technology by improving the fidelity and stability of qubit measurements.

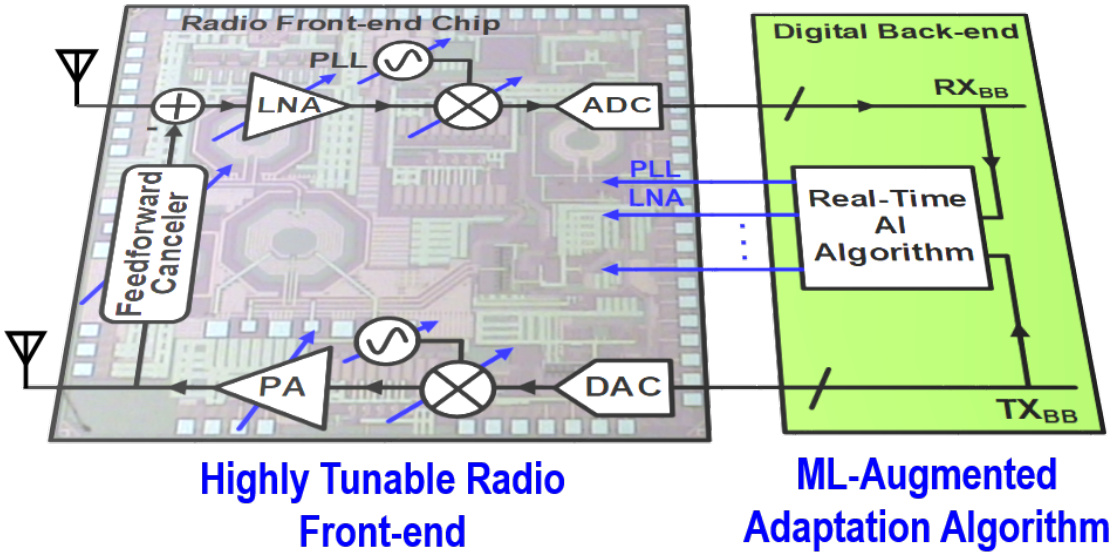


Figure 7.1: A highly tunable radio chip front-end adapted by ML algorithms implemented using ASICs for optimizing various radio performance metrics.

7.2.1 Highly Programmable Radio Systems with an Integrated Back-end

Chapter 6 presents integrated techniques to enhance the tunability of SI mitigation circuits in FD radios. However, future radio systems may require even higher tunability across multiple performance metrics including noise figure, linearity, bandwidth, and operation frequency to support various wireless standards. In addition to mitigating SI from the radio's own transmitter, radio systems must also handle broadband interference, which includes both in-band and out-of-band components from other users. A single-chip radio solution that supports multiple wireless standards is desirable to develop a cost- and area-efficient radio system.

The ML-augmented adaptation algorithm proposed in Chapter 6 can be further extended to optimize the large tuning vector space of the forementioned radio chip for optimal performance in dynamic environments, as shown in Fig.7.1. While implementing ML algorithms on an FPGA (Chapter 6) provides reconfigurability for testing, it is not optimized in terms of

clock speed, power efficiency, and hardware resources. For instance, the maximum clock frequency of the NN implemented on the FPGA in Chapter 6 is 250 MHz, with a computation time of approximately 0.1 ms. However, using modern CMOS sub-5nm FinFET technology could easily achieve a clock frequency of 1 GHz [97]. Additionally, using ASICs with dense on-chip memory would further enhance computation efficiency while significantly reducing power consumption as compared to FPGA-based implementations. The ultimate goal of the project is to integrate the radio's digital back-end with the highly tunable radio front-end chip to develop a single, fully adaptive radio system for various wireless applications. If successful, this could contribute to the development of single-chip or single-package solutions, seamlessly integrating with existing wireless devices such as smartphones, laptops, and IoT devices, thereby supporting emerging applications for future wireless communications.

7.2.2 Integrated Qubit Readout Circuits for Quantum Computing

A quantum computer typically consists of an array of Qubits and a controller that controls and reads out the states of qubits [98]. Many research efforts [9, 10, 15, 99, 100] have focused on implementing the controller using CMOS technology operating at cryogenic temperature (cryo-CMOS) due to its compactness and scalability. However, discrete ferrite circulators or Hall effect circulators [101] have been widely used in both superconducting qubits [102] and spin qubits [103] during the readout process to isolate the qubit reflection signal from the desired readout signal, which remains a major obstacle for achieving a fully integrated qubit processor. This challenge is similar to mitigate self-interference in in-band FD radio systems. Therefore, the integrated interference mitigation techniques developed in this dissertation could also be applied to mitigate readout signal coupling in a quantum controller, as shown in Fig.7.2. For example, an integrated electrical balanced duplexer (EBD) using pure passive components with wide bandwidth, low noise, and low power consumption at cryogenic temperature, could serve as an effective integrated circulator for the qubit readout circuit front-end, providing isolation on various TX-RX coupling, as shown in Fig.7.2. Moreover, additional interference mitigation can be applied later in the qubit readout chain

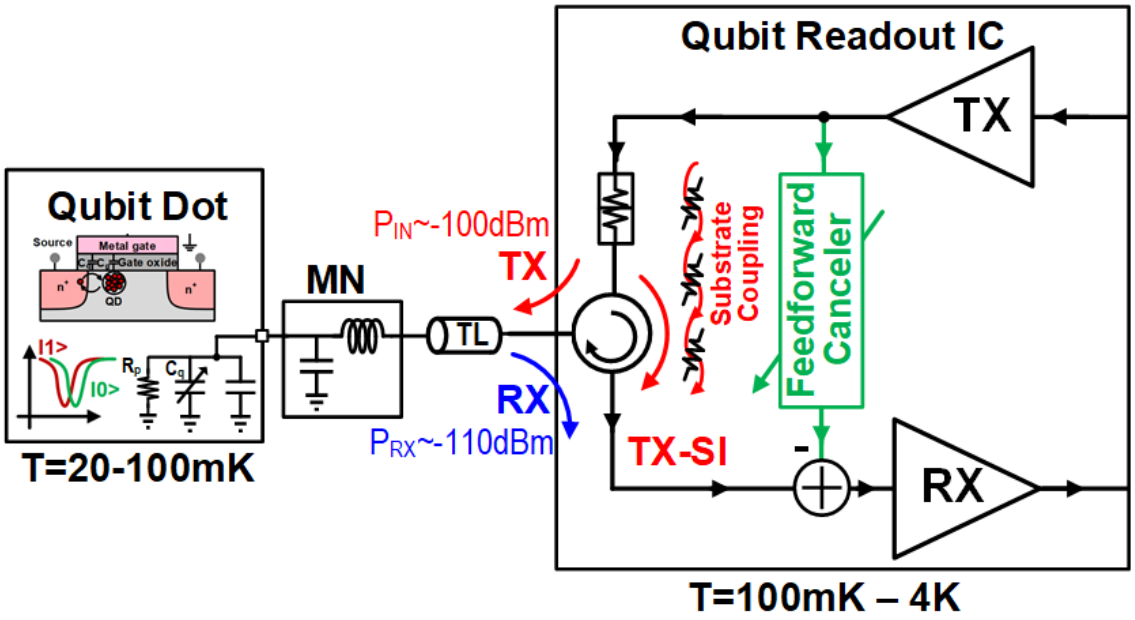


Figure 7.2: Possible qubit state readout interface using an integrated circulator and feedforward canceler in a quantum controller.

(Fig.7.2), depending on the specifications of different types of qubits. This idea can be further explored in future research to facilitate the development of a fully-integrated CMOS quantum processor.

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