CMOS Short Pulse Generator IC Development

Jabir Mohammad Patel

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Committee:

Debasis Dawn

Massimiliano Laddomada

Orlando Baiocchi

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Abstract

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Jabir Mohammad Patel

Chair of the Supervisory Committee:

Debasis Dawn

School of Engineering & Technology

The objective of this project is to design, simulate, and characterize a Novel CMOS-based short pulse generator (SPG) that can generate a sub-nano second pulse width and capable of repetition while consuming less power. The CMOS Short Pulse Generator will be based on the Marx Generator topology but will use a combination of CMOS switches for fast switching to generate periodic short pulses. The specific objective of this project is to introduce innovative circuit architecture to achieve periodic pulses with fast rise times and short durations of sub-nanosecond while consuming less power compared to the existing state-of-the-art pulse generators. This research will aim to design and layout a fully integrated CMOS short pulse generator IC for fabrication and test a prototype built on breadboard and fabricated on PCB to validate the proof-of-concept. This research will contribute to advancing the state-of-the-art in pulse generator technology, with potential applications in various fields.

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DEDICATION

I dedicate this thesis to my parents, wife and two beautiful kids who have been my constant source of love, support, and inspiration throughout my academic journey. Their unwavering belief in me, their encouragement, and their sacrifices have made this accomplishment possible.

I also dedicate this thesis to Dr. Debasis Dawn and Dr. Massimiliano Laddomada whose passion, dedication, and perseverance have inspired me to pursue my goals with diligence and commitment.

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Chapter 1. INTRODUCTION

In today's fast-paced world, there is an increasing demand for high-speed electronics that can perform complex operations quickly and efficiently. One important component of these electronics is a short pulse generator that can produce very narrow pulses with durations in the sub-nanosecond range. Such pulses are critical in applications ranging from ultrafast signal processing to high-speed communication systems and medical devices.

The design and development of short pulse generators is a challenging task that requires a deep understanding of circuit design, semiconductor physics, and high-frequency electronics. In recent years, several research efforts have focused on the development of short pulse generators based on different topologies and technologies, including avalanche transistors, tunnel diodes, and pulse-forming networks.

In this thesis, we present a novel CMOS-based short pulse generator capable of producing periodic sub-nanosecond pulses with fast rise times and low power consumption. Our approach is based on the Marx generator topology, which has been widely used in high-voltage applications but has not been extensively explored in the context of sub-nanosecond pulse generation. We use a combination of CMOS switches for fast switching to generate periodic short pulses, and introduce simple yet innovative circuit architecture to achieve fast rise times and short durations while consuming less power compared to the existing state-of-the-art pulse generators.

The main objective of this thesis is to design, simulate, and characterize the proposed CMOS-based short pulse generator, and to validate the proof-of-concept through prototyping on various platforms including breadboard and PCB, as well as fabricating a fully integrated sub-nano second short pulse generator IC. We will also present the results of our simulation and characterization studies, and compare our generator's performance with existing pulse generators. Our work aims to provide a new and efficient solution for generating sub-nanosecond pulses, which has potential applications in a wide range of fields, from high-speed communication to biomedical imaging and diagnostics.

1.1 BACKGROUND AND MOTIVATION

Short pulse generators have become increasingly important in various fields, such as high-speed communication, biomedical imaging and diagnostics, and scientific research. These pulse generators are designed to produce ultrafast electrical pulses that are less than one nanosecond in duration. With their unique properties, sub-nanosecond pulses have numerous applications, including high-speed communication and data transmission, time-resolved spectroscopy, and laser-based material processing.

Despite the significant progress in pulse generation technology, existing pulse generators are still limited in terms of their pulse width, rise time, and high peaks. This limitation has led to a growing demand for new and efficient solutions that can produce shorter pulses with higher repetition rates and voltage. Additionally, the existing pulse generators are often bulky, expensive, and require complex setup and operation procedures, making them unsuitable for many applications, particularly those requiring portability and simplicity.

The need for high-voltage pulse generators in biological applications has been well established. For instance, in electroporation, a method used for gene delivery and cell transformation, high-voltage pulses are applied to cells to create temporary pores in their membranes, allowing DNA or other molecules to enter. In addition, high-voltage pulses have been used in electrosurgery for the removal of tissue and in neurostimulation for the treatment of various neurological disorders. The study by Achour et al. [1] (2019) proposed a compact and low-cost high-voltage pulse generator design for biological applications. The generator's performance was evaluated in terms of output voltage, pulse duration, and rise time, and the results showed that it could generate high-voltage pulses with sub-microsecond rise times and pulse durations in the range of tens of microseconds. The authors demonstrated the feasibility of using their generator for electroporation and electrochemotherapy in vitro, which suggests that this design could be a promising solution for various biological applications that require high-voltage pulses.

The motivation of this thesis is to design and develop a new, efficient, and portable sub-nanosecond pulse generator that can overcome some of the limitations of existing pulse generators. The proposed pulse generator will be based on a compact and robust design that can produce ultrafast electrical pulses with high repetition rates and minimal jitter. The pulse generator will also be designed to be easily operated and integrated into existing systems, making it an ideal solution for a wide range of applications.

Overall, this thesis aims to contribute to the development of pulse generation technology by providing a new and efficient solution for generating short sub-nanosecond pulses. By addressing the current limitations of existing pulse generators, the proposed pulse generator has the potential to enable new applications in high-speed communication, biomedical imaging, and scientific research.

1.2 RESEARCH OBJECTIVES

The research objectives of this study aim to explore the design, development, and evaluation of short sub-nanosecond pulse generators. Specifically, the research will focus on:

1. Analyzing the current state-of-the-art pulse generators and identifying their limitations in terms of pulse width and efficiency.
2. Designing and developing a new pulse generator that can produce short sub-nanosecond pulses with high efficiency.
3. Evaluating the performance of the new pulse generator and comparing it with existing state-of-the-art pulse generators.
4. Investigating the potential applications of the new pulse generator in various fields, including high-speed communication, biomedical imaging and diagnostics, and other related areas.
5. Providing recommendations for further improvement and future research directions based on the results of the study.
6. Overall, the research objectives of this study aim to contribute to the advancement of pulse generator technology and enable the development of new applications that require short sub-nanosecond pulse generation.

1.3 RESEARCH METHODOLOGY

The proposed research will employ a mixed-methods approach to achieve the research objectives. The methodology will include both experimental and simulation studies. The experimental study will involve the design and implementation of breadboard and printed circuit board (PCB) circuits for sub-nanosecond pulse generation using the Cadence design tool. The breadboard circuits will be used for initial testing and validation, while the PCB circuits will be used for final testing and verification.

The simulation study will involve the use of Cadence tools for the design and simulation of sub-nanosecond pulse generator Integrated Circuit (IC). The simulations will be used to optimize the design and evaluate the performance of the proposed circuit. The simulations will also be used to investigate the effect of various circuit parameters on the pulse width and amplitude.

Overall, the research methodology will include a combination of experimental and simulation studies, as well as data analysis, to achieve the research objectives. The experimental studies will provide validation and verification of the simulation results, while the simulation studies will allow for the optimization of the circuit design before implementation.

1.4 ORGANIZATION OF THE THESIS

The thesis is structured into seven chapters, each addressing specific aspects of the research.

Chapter 1 introduces the thesis by providing a background of the research problem, stating the motivation for the research, outlining the research objectives, describing the research methodology, and presenting the organization of the thesis.

Chapter 2 reviews the literature on short pulse generators, starting with an overview of their applications, followed by the integration of CMOS technology in their design, and a discussion of the design considerations. The chapter then examines existing short pulse generators and their limitations, concluding with a summary of the literature review.

Chapter 3 presents the design of the short pulse generator, covering the architecture, CMOS switching circuit design, Marx generator topology and its integration with CMOS switching, design optimization for short pulse width, design challenges, and solutions.

Chapter 4 describes the simulation setup and results of the short pulse generator, as well as comparing its performance with existing pulse generators.

Chapter 5 focuses on the prototyping phase, which includes the breadboard prototype testing and results, the PCB prototype design and testing, and the results of the PCB prototype.

Chapter 6 describes the layout process of the short pulse generator IC, including design rules, constraints, fabrication, and packaging.

Finally, Chapter 7 concludes the thesis by summarizing the contributions of the research, drawing conclusions and implications for future research, and presenting the limitations and recommendations for future work.

Chapter 2. LITERATURE REVIEW

2.1 OVERVIEW OF SHORT PULSE GENERATORS

Short pulse generators are electronic devices that generate short-duration, high-voltage pulses of electrical energy. These generators are used in various fields such as medicine, physics, and engineering for a range of applications including high-power microwave generation, pulsed power research, and biological experiments. Short pulse generators typically utilize pulse-forming networks (PFNs) to convert a DC power source into short pulses and current. PFNs consist of a series of capacitors and inductors that are charged and discharged rapidly, resulting in a high-voltage pulse. The pulse width, amplitude, and repetition rate of the generated pulses depend on the design of the PFN and the charging and discharging circuits.

The performance of short pulse generators is often characterized by the rise time, fall time, pulse width, peak voltage, and pulse repetition frequency. Rise time and fall time refer to the time required for the pulse to reach its maximum and minimum voltage, respectively. Pulse width refers to the duration of the pulse, while peak voltage refers to the maximum voltage reached by the pulse. Pulse repetition frequency refers to the number of pulses generated per second.

Several types of short pulse generators exist, including the Blumlein generator, Marx generator, and pulse transformer-based generators. Blumlein generators use a transmission line structure to generate high-power pulses with fast rise times. Marx generators consist of a series of capacitors and spark gaps arranged in a ladder-like structure and can produce very high peak voltages with fast rise times. Pulse transformer-based generators use a high-voltage transformer to generate short pulses with a fast rise time.

Overall, short pulse generators are crucial tools in various fields that require high-voltage, short-duration pulses of electrical energy. The design and optimization of short pulse generators are essential for achieving desired performance characteristics for specific applications.

2.2 INTEGRATION OF CMOS TECHNOLOGY IN SHORT PULSE GENERATOR

Short pulse generators (PGs) have gained increasing attention in the field of high-speed communications due to their simplicity in circuit design, low power consumption, and high frequency pulse capabilities compared to continuous wave systems [2-6]. In recent years, several techniques have been explored to generate ultra-short pulses, including the use of logic gates [8-10] and under-damping state of R-L-C circuits [6, 11]. Among these techniques, CMOS technology has shown great potential for implementing short pulse generators.

One promising approach for CMOS-based short pulse generators is the use of shaping-differential and phase detect circuits. Tang et al. [6] proposed a design and measurement of ultra-short pulse generators based on shaping-differential and phase detect circuits, using TSMC MS/RF 0.13-μm CMOS process. They demonstrated that by using a differential circuit, a narrower pulse width can be achieved compared to conventional design. The measurements were in good agreement with simulations, indicating the potential of CMOS technology in producing ultra-short pulses.

Another application of CMOS technology in short pulse generators is the use of slot bow-tie antennas integrated on-chip [5]. Assefzadeh and Babakhani proposed an 8-psec 13 dBm peak EIRP digital-to-impulse radiator with an on-chip slot bow-tie antenna in silicon. Their design achieved a high level of integration by using CMOS technology and a slot bow-tie antenna. They demonstrated the potential of CMOS technology in producing short pulse generators with high radiation efficiency.

Moreover, CMOS technology has been used for generating ultra-wide band (UWB) pulses. Bachelet et al. [9] presented a fully integrated CMOS UWB pulse generator using a 0.18-μm CMOS process. Their design achieved a pulse repetition rate of 50 MHz and a pulse width of 125 ps. The UWB pulses were generated using a differential pulse generator and a resonant peaking network. They demonstrated the potential of CMOS technology in producing UWB pulses for communication applications.

In summary, CMOS technology has shown great potential for implementing short pulse generators due to its high level of integration, low power consumption, and compatibility with high-frequency circuits. These results demonstrate the potential for future developments in CMOS technology to advance short pulse generator designs for a variety of applications.

2.3 DESIGN CONSIDERATIONS FOR SHORT PULSE GENERATORS

When designing short pulse generators (PGs), there are several important considerations to take into account to ensure their proper operation and performance. Some key design considerations for short PGs include:

Pulse width: The pulse width is one of the most critical parameters for short PGs, as it determines the information-carrying capacity of the pulse. To achieve shorter pulse widths, designers can employ techniques such as shaping-differential circuits, which can generate narrower pulse widths compared to conventional designs, as demonstrated by Tang et al. (2017).

Rise and fall times: The rise and fall times of the pulse waveform are also important parameters to consider when designing short PGs. Fast rise and fall times are desirable for achieving high data rates, but they can also introduce signal distortion and noise, which can degrade the performance of the PG. Therefore, designers must balance the trade-off between pulse width, rise and fall times, and signal quality.

Frequency range: The frequency range of the PG is another important consideration, as it determines the maximum data rate that can be achieved. For example, Roderick et al. (2006) demonstrated an ultra-wideband beamforming system that operates at frequencies up to 10 GHz. The frequency range of the PG can be extended by using advanced CMOS processes with higher cutoff frequencies, as demonstrated by Kubota et al. (2014) in their 10 GHz center-frequency Gaussian pulse generator using 65-nm logic CMOS.

Power consumption: The power consumption of the PG is an important design consideration, particularly in battery-powered applications. Techniques such as pulse shaping and power gating can be employed to reduce power consumption without sacrificing performance.

Integration with other components: In many applications, the PG must be integrated with other components such as antennas, receivers, and transmitters. Therefore, designers must ensure that the PG is compatible with these components and that the interfaces between them are properly designed to minimize signal loss and noise.

Noise and interference: Short PGs are susceptible to noise and interference from various sources, including power supply noise, substrate noise, and electromagnetic interference. Designers must employ techniques such as shielding, filtering, and grounding to minimize these effects and ensure reliable operation of the PG.

In conclusion, the design of short PGs requires careful consideration of several key parameters, including pulse width, rise and fall times, frequency range, power consumption, integration with other components, and noise and interference. By carefully optimizing these parameters, designers can achieve high-performance short PGs that meet the requirements of a wide range of applications.

2.4 EXISTING SHORT PULSE GENERATORS AND THEIR LIMITATIONS

Existing short pulse generators have been designed for various applications, such as ultra-wideband communication, radar systems, and medical imaging. However, these generators are often limited in terms of pulse duration, amplitude, and noise level.

One limitation of existing short pulse generators is the pulse duration. Many generators can produce pulses with durations in the range of picoseconds to nanoseconds. However, shorter pulse durations are often required for high-speed applications, such as optical communication and radar systems. To achieve even shorter pulse durations, advanced techniques, such as mode-locked lasers and pulse compression techniques, have been developed.

Another limitation is the amplitude of the generated pulse. High-power pulses are often required for many applications, such as radar and medical imaging. However, achieving high power levels can be challenging due to various constraints, such as the limited output voltage swing of CMOS transistors.

Furthermore, noise is a critical factor that limits the performance of short pulse generators. Noise can be introduced by various components, such as voltage references, amplifiers, and switches. Minimizing noise levels requires careful design and optimization of the generator's components.

In summary, existing short pulse generators have limitations in terms of pulse duration, amplitude, and noise level. Addressing these limitations requires careful consideration of the design, choice of materials, and integration of advanced techniques.

2.5 SUMMARY OF LITERATURE REVIEW

The literature review in Chapter 2 provides an overview of short pulse generators and their applications in various fields such as medicine, physics, and engineering. The chapter highlights the importance of pulse-forming networks (PFNs) in short pulse generator designs and their characteristics such as rise time, fall time, pulse width, peak voltage, and pulse repetition frequency. Several types of short pulse generators are discussed, including the Blumlein generator, Marx generator, and pulse transformer-based generators.

The integration of CMOS technology in short pulse generator design is also explored. The potential of CMOS technology in producing ultra-short pulses and generating ultra-wide band (UWB) pulses is highlighted. The chapter also outlines important design considerations for short pulse generators, including pulse width, rise and fall times, and frequency range.

Chapter 3. SHORT PULSE GENERATOR DESIGN

3.1 SHORT PULSE GENERATOR ARCHITECTURE

A short pulse generator is a device that produces electrical pulses with very short durations, typically on the order of picoseconds or femtoseconds. These generators are used in a variety of applications, including high-speed communication systems, ultrafast spectroscopy, and laser pulse generation.

There are several different architectures used in the design of short pulse generators, each with its own advantages and disadvantages. One common architecture is the pulse-forming network (PFN), which consists of a series of capacitors and switches that are charged up and then discharged in a controlled manner to produce the desired pulse shape. PFN-based generators can be compact and efficient, but they may require precise timing and control to achieve the desired pulse characteristics.

Another architecture is the voltage-controlled oscillator (VCO), which uses a resonant circuit to produce a sinusoidal waveform that can be shaped into a pulse through the use of nonlinear elements such as diodes or transistors. VCO-based generators can be very fast and precise, but they may require careful tuning to achieve the desired frequency and amplitude.

A third architecture is the mode-locked laser, which uses a feedback loop to generate a train of ultrafast pulses with durations on the order of femtoseconds. Mode-locked lasers can be extremely precise and stable, making them ideal for applications such as optical communications and ultrafast spectroscopy.

Finally, Marx generator is a type of high voltage pulse generator architecture that is commonly used for creating short duration, high voltage pulses. It is composed of multiple capacitors and spark gap switches arranged in a ladder-like configuration, known as a Marx bank. When a high voltage source is discharged into the first capacitor in the Marx bank, the capacitor charges up to the voltage of the source. When the voltage across the capacitor reaches a critical level, it discharges through the first spark gap switch into the next capacitor. This process repeats through each stage of the Marx bank, resulting in an additive voltage pulse across the output. The resulting pulse is typically high voltage, short duration, and fast rising. Marx generators are often used in applications such as pulsed power systems, high energy physics experiments, and electromagnetic pulse (EMP) testing.

Overall, the choice of short pulse generator architecture depends on the specific requirements of the application, such as pulse duration, repetition rate, and output power. By carefully selecting the appropriate architecture and optimizing the design, it is possible to create short pulse generators that meet a wide range of performance requirements.

3.2 MARX GENERATOR TOPOLOGY AND ITS INTEGRATION WITH CMOS SWITCHING

Erwin Otto Marx introduced the Marx generator in 1924 as an electrical circuit designed to produce a high-voltage pulse from a low-voltage DC supply. These generators find application in high-energy physics experiments, where they are used to simulate the effects of lightning on aviation equipment and power-line gear. The Z Machine at Sandia National Laboratories employs a set of 36 Marx generators to generate X-rays [12].

The circuit generates a high voltage pulse by charging n capacitors (C) in parallel to a voltage V_{CC} through resistors (R_C). While charging, the spark gaps (S_G) act as open circuits since they have a breakdown voltage greater than V_{CC}. The last spark gap isolates the generator's output from the load, preventing the capacitors from discharging prematurely. Figure 3. 1 shows the schematic of a typical Marx generator.

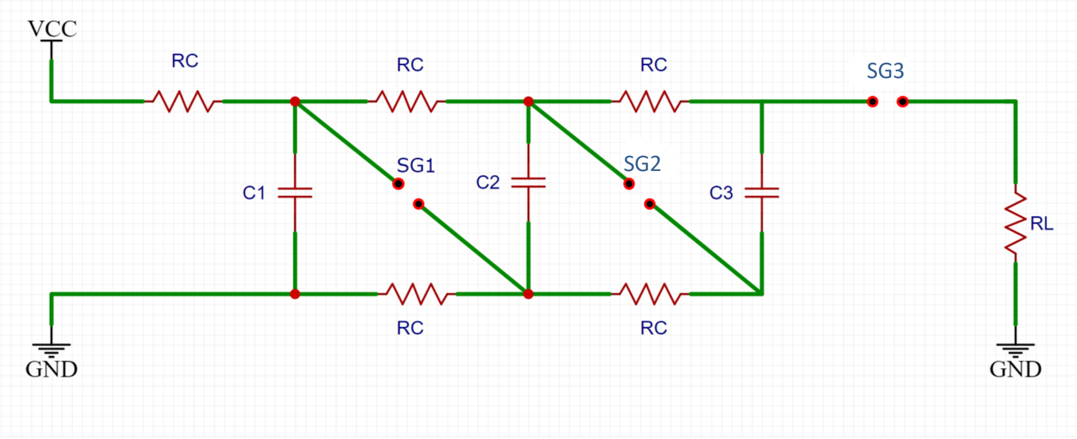


Figure 3. 1 The Schematic of a Typical Marx Generator with Spark Gaps.

To create the high-voltage pulse, the first spark gap is triggered, causing it to break down and short-circuit the gap, which connects the first two capacitors in series and applies a voltage of about 2VC across the second spark gap. As a result, the second gap breaks down and adds the third capacitor to the "stack", and the process continues until all the gaps have been sequentially broken down. This process is known as "erection."

The last gap connects the output of the series "stack" of capacitors to the load. In theory, the output voltage will be $N * V_{CC}$, which is the number of capacitors multiplied by the charging voltage. However, in practice, the output voltage is usually lower. None of the charging resistors (R_C) are subjected to more than the charging voltage, even when the capacitors have been erected. The output is a brief pulse since the charge available is limited to the charge on the capacitors, which discharge through the load. When the spark gaps stop conducting, the low-voltage supply begins charging the capacitors again [13].

Marx generators are modules commonly used in pulsed power systems that generate high-voltage and high-power electrical pulses from low-voltage and low-power supplies. They work by charging capacitors in parallel and then discharging them in series, which effectively increases the output voltage to $N * V_{CC}$, where N is the number of capacitors, and V_{CC} is the charging voltage.

To overcome the voltage and power limitations of CMOS technologies, there is interest in developing on-chip Marx generators, which have not yet been reported. This development could enable truly portable lab-on-chip systems that require high-voltage and high-power electrical pulses not available with standard CMOS devices and circuits, such as pulsed field electrophoresis that requires a field intensity of 1-10 kV/m across a ~10-100 µm microfluidic channel. Voltages of 10 V to 100 V, which are much lower than the required high-voltages, need to be integrated and connected to prevent losses. The on-chip Marx generator circuits can achieve high-power electrical pulses, but their implementation is challenging [13].

The circuit illustrated in Figure 3. 2 is an on-chip Marx generator that functions in the same manner as a conventional Marx generator. However, instead of using traditional spark gaps (S_G) as switches, high-speed CMOS switches are utilized.

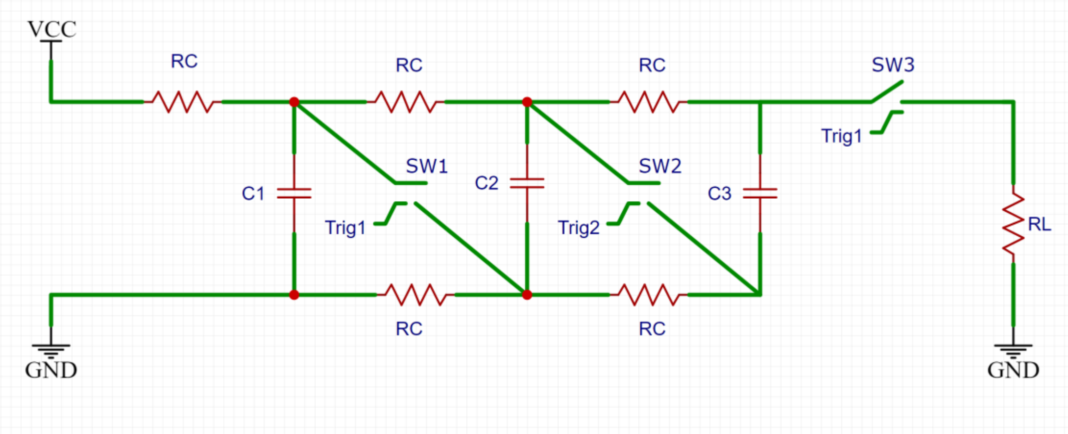


Figure 3. 2 The Schematic of the 3-Stage Marx Generator with Highspeed CMOS Switches.

3.3 The Proposed On-Chip Short Pulse Generator

In this section, we present a novel on-chip Short Pulse Generator that utilizes a combination of high-speed MOSFET switches both for charging and discharge phase. Stage resistance (R_C) has been replaced with series of highspeed MOSFET switches reducing voltage loss due to current path observed by capacitors during discharge mode. Our circuit consists of 7 highspeed MOSFETs as switches (S_W), 2 Stage Capacitors (C) and a load resistor (R_L) for measurement purposes. Gates of all switches are driven by 2 controlled Pulse Width Modulation (PWM) sources. To prevent current path during discharge mode, SW1, SW3, SW4, and SW6 are triggered 180° out of phase from SW2, SW5, and SW7 resulting in a direct and more efficient discharge path of the capacitors. The generator is capable of producing a periodic sub-nanosecond short pulse, making it highly useful for various applications. This new design is a significant improvement over conventional topologies [13] due to its simplicity, reducing voltage loss due to current path observed by capacitors during discharge mode. Figure 3. 3 shows the schematic of the proposed on-chip Short Pulse Generator.

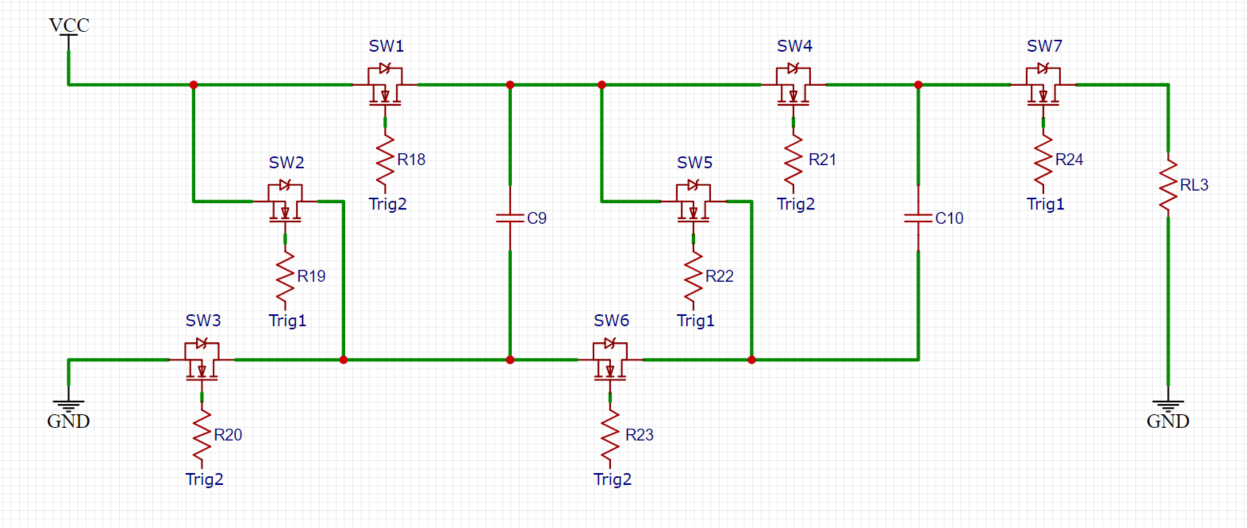
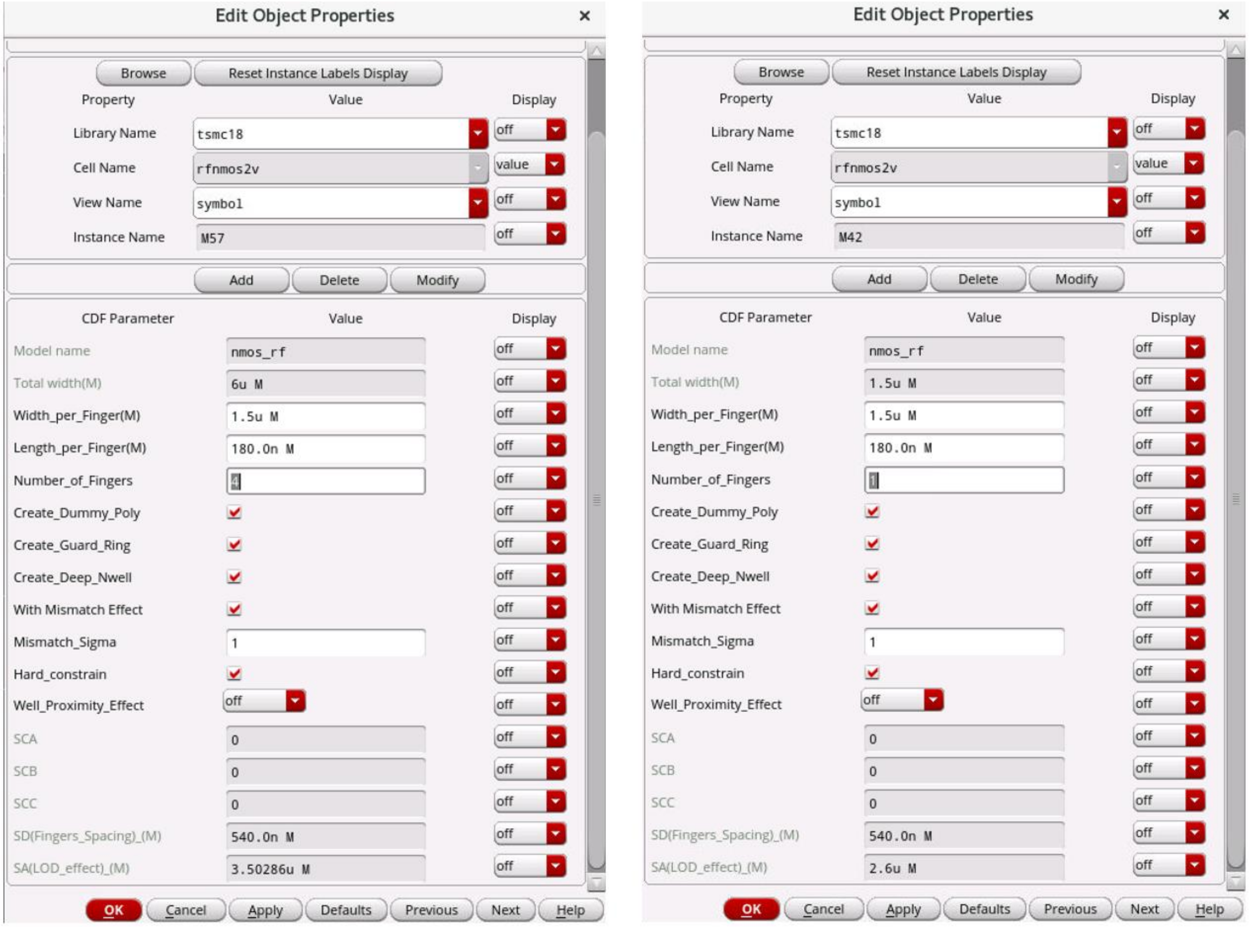


Figure 3. 3 The Schematic of the Proposed On-Chip Short Pulse Generator.

3.4 DESIGN CHALLENGES AND THEIR SOLUTIONS

The decision to eliminate stage resistors from the short pulse generator design was not without its challenges. On one hand, stage resistors can lead to voltage drops during both the charging and discharging phases, which can ultimately limit the output voltage and energy of the generator. However, the absence of resistors makes it difficult to control the current path during the discharge phase, resulting in increased voltage loss due to inductive effects.

To overcome these challenges, the proposed design employs high-speed MOSFETs as switches for charge and discharge phase. Relying solely on MOSFETs as the switches for the charge and discharge phases comes with its own set of challenges, such as the possibility of increased power dissipation due to the high on-resistance of the MOSFETs. To address these challenges, careful consideration was given to the selection of the MOSFETs used in the design, with an emphasis on minimizing their on-resistance by precisely setting the length and width. The relationship between the resistance of the channel and its width-to-length ratio is inverse; a decrease in the channel length results in lower resistance, allowing for increased current flow. The MOSFETs provide low on-resistance, minimizing the voltage drop during the discharge phase. In addition, the use of MOSFETs enables precise control of the current path, allowing for a more efficient direct discharge of the capacitors.



(a)

Property	Value	Display
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Cell Name	rfnmos2v	value
View Name	symbol	off
Instance Name	M57	off

CDF Parameter	Value	Display
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Width_per_Finger(M)	1.5u M	off
Length_per_Finger(M)	180.0n M	off
Number_of_Fingers	4	off
Create_Dummy_Poly	☑	off
Create_Guard_Ring	☑	off
Create_Deep_Nwell	☑	off
With Mismatch Effect	☑	off
Mismatch_Sigma	1	off
Hard_constrain	☑	off
Well_Proximity_Effect	off	off
SCA	0	off
SCB	0	off
SCC	0	off
SD(Fingers_Spacing)_(M)	540.0n M	off
SA(LOD_effect)_(M)	3.50286u M	off

(b)

Property	Value	Display
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Cell Name	rfnmos2v	value
View Name	symbol	off
Instance Name	M42	off

CDF Parameter	Value	Display
Model name	nmos_rf	off
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Width_per_Finger(M)	1.5u M	off
Length_per_Finger(M)	180.0n M	off
Number_of_Fingers	1	off
Create_Dummy_Poly	☑	off
Create_Guard_Ring	☑	off
Create_Deep_Nwell	☑	off
With Mismatch Effect	☑	off
Mismatch_Sigma	1	off
Hard_constrain	☑	off
Well_Proximity_Effect	off	off
SCA	0	off
SCB	0	off
SCC	0	off
SD(Fingers_Spacing)_(M)	540.0n M	off
SA(LOD_effect)_(M)	2.6u M	off

Figure 3. 4 MOSFET Properties for Different Switches - (a) SW1, SW3, SW4, SW6 and (b) SW2, SW5, SW7.

The choice of MOSFET width and length dimensions, set at 1.5µm as the minimum, plays a critical role in determining their performance characteristics, balancing on-resistance and gate capacitance trade-offs. To optimize the design, the number of fingers was adjusted. SW2, SW5, and SW7 were precisely configured with four fingers to increase the effective channel width, reducing on-resistance and enabling better current handling for efficient capacitor discharge and higher output voltage. Conversely, SW1, SW3, SW4, and SW6 had one finger to maintain lower on-resistance and minimize gate capacitance for effective capacitor charging. This configuration aimed to maximize output voltage while considering the trade-offs, ensuring optimal MOSFET performance and desired circuit functionality. Figure 3. 4 provides a detailed object properties view of the switches used in the design, offering a more technical insights into their specifications.

The Short Pulse Generator during its charging phase is modeled in the schematic presented in Figure 3. 5, while the direct discharge path observed during the discharge phase is illustrated in Figure 3. 6.

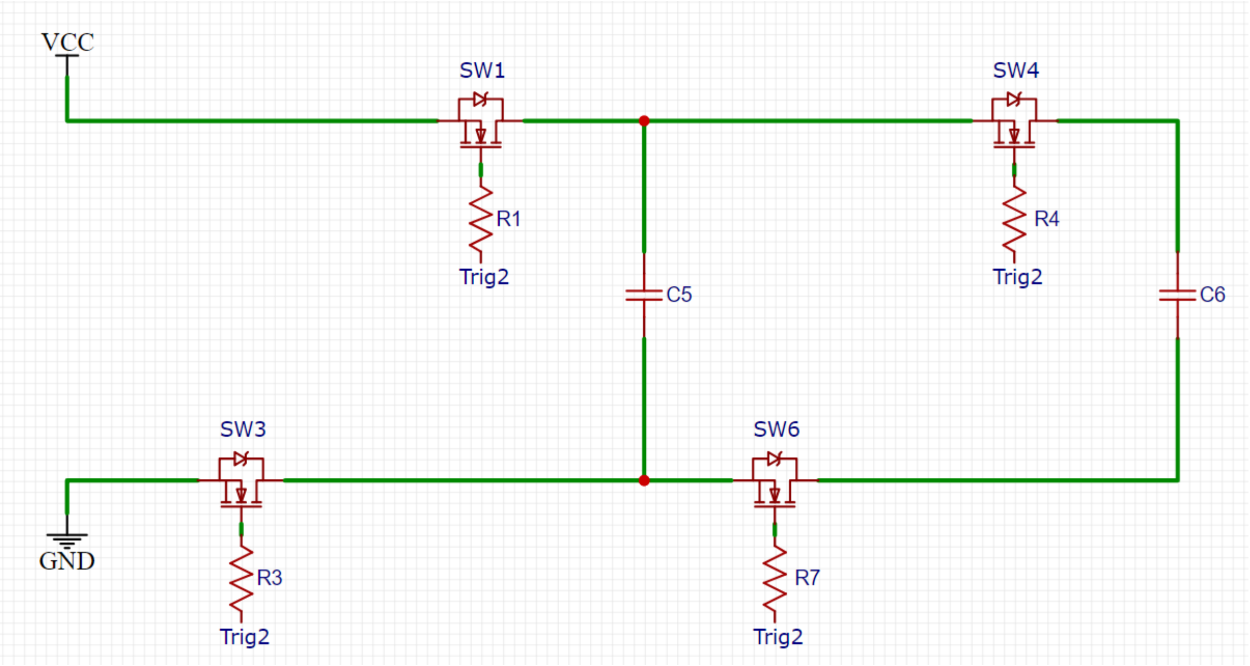


Figure 3. 5 Equivalent Circuit Model of Short Pulse Generator During Charging phase.

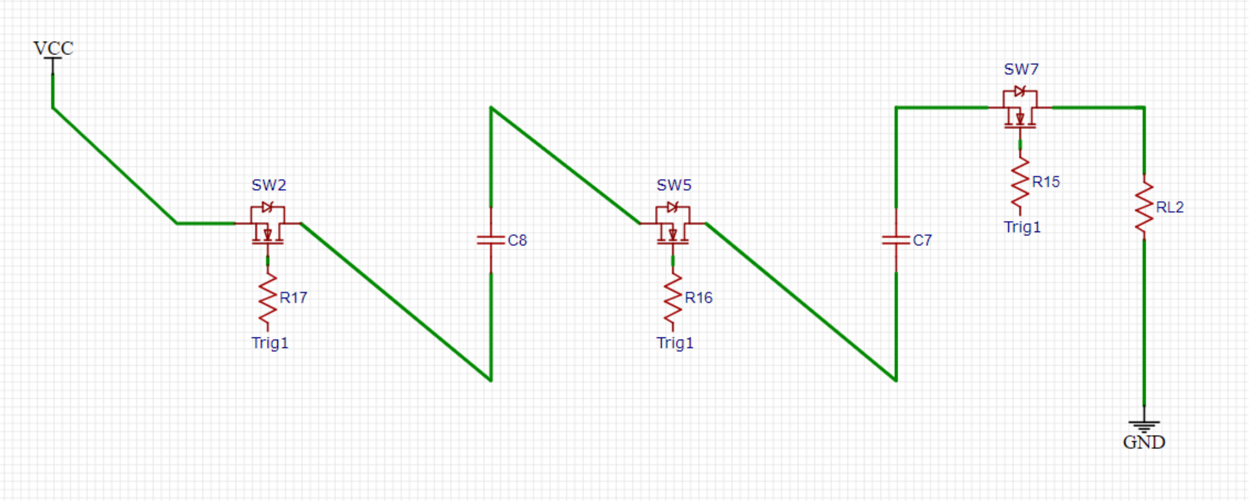


Figure 3. 6 Equivalent Circuit Model of Short Pulse Generator During Discharging phase.

To achieve a short pulse width, the design uses a combination of PWM sources to control the gates of the MOSFETs. The PWM sources trigger the MOSFETs in a 180° out-of-phase sequence, enabling a more efficient and direct discharge path for the capacitors. During the charging phase of the Short Pulse Generator, SW2, SW5 and SW7 are in the off state while SW1, SW3, SW4, and SW6 are in the on state allowing capacitors to charge to V_{CC}. Conversely, in the discharge phase, the PWM sequence is reversed, causing SW2, SW5, and SW7 to turn on while SW1, SW3, SW4, and SW6 switch off, creating an open circuit and enabling a more direct discharge path.

The R_C time constant is a measure of how long it takes for a capacitor to charge or discharge through a resistor in a circuit. In the case of the Short Pulse Generator that uses MOSFETs and capacitors, there are no resistors in the circuit. Therefore, the time constant of the circuit is determined solely by the capacitance of the capacitors and the equivalent series resistance (ESR) of the MOSFETs. The ESR of the MOSFETs is a measure of the resistance encountered by the current flowing through the MOSFETs and the parasitic elements in the

MOSFETs themselves. In general, MOSFETs have a much lower ESR than resistors, which means that the time constant of the Short Pulse Generator circuit is much smaller than that of a conventional RC circuit. This results in faster charging and discharging times, which is important for generating short pulses with high repetition rates.

The addition of a resistor at the gate of a MOSFET serves as a protective measure for the gate. The resistor acts as a current limiting device, preventing excessive current flow into the gate during the charging phase of the circuit. Without this resistor, the gate can become damaged or destroyed due to the high current flow, leading to circuit malfunction or failure. Additionally, the gate resistor helps to slow down the switching speed of the MOSFET, reducing the likelihood of ringing or oscillation in the circuit. Overall, the inclusion of a gate resistor enhances the reliability and stability of the MOSFET-based circuit design.

In summary, one of the challenges faced in the design of the Short Pulse Generator was to minimize voltage drops during the charge and discharge phase of the capacitors. Conventionally, this is achieved using stage resistors (R_C), but this results in voltage loss and reduced efficiency. To overcome this challenge, we used a combination of MOSFETs as high-speed switches and capacitors for charge and discharge phases of the circuit. This approach eliminated the need for stage resistors and reduced voltage drops, resulting in higher efficiency and a shorter pulse duration. However, there were challenges in optimizing the circuit to ensure that the MOSFETs had sufficient on-resistance to compensate for the lack of resistors and to maintain a stable output voltage. By carefully selecting the MOSFETs and implementing a suitable PWM strategy, we were able to overcome these challenges and achieve the desired performance of the Short Pulse Generator. In the following chapter, we will look at the simulation results of the proposed design.

Chapter 4. CADENCE SIMULATION AND RESULTS

4.1 SIMULATION SETUP AND RESULTS

The simulation setup was conducted using Cadence software and 180-nm TSMC RF CMOS technology to evaluate the performance of the proposed on-chip Short Pulse Generator. The input voltage (V_{CC}) was set to 2V to maintain V_{CC} < VDS of the selected MOSFETS, and the amplitude of the PWMs were set 5V with a period of 1ns, corresponding to a frequency of 1GHz. To achieve the desired 180° out of phase operation, trigger at the gates of SW1, SW3, SW4, and SW6 or PWM_2 as shown in Figure 4. 1 was configured to have a delay time of 500ps, which is half of the period. The rise and fall time of both PWM_1 and PWM_2 was set to 1ps respectively to ensure accurate and fast switching of the MOSFETs. Figure 4. 2 shows the object properties of both PWM sources in cadence. The simulation results were analyzed to evaluate the effectiveness of the proposed design in generating short pulses with sub-nanosecond durations.

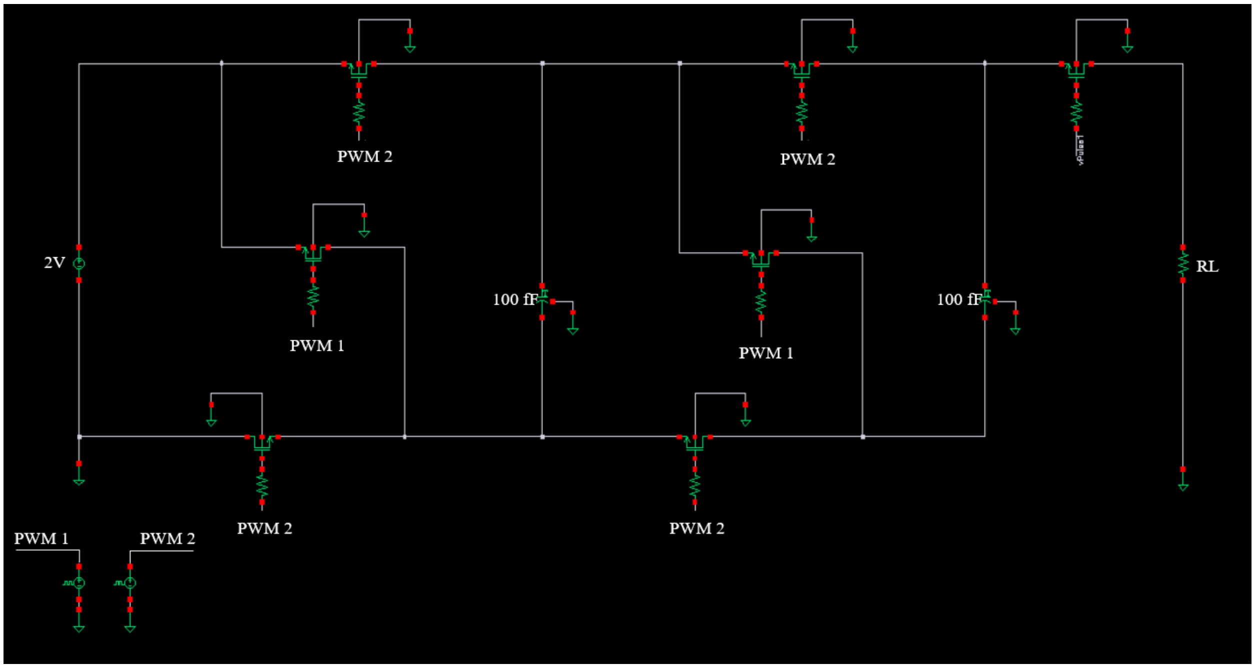


Figure 4. 1 Schematic of the Proposed Short Pulse Generator in Cadence.

Figure 4. 3 presents the transient analysis settings pane in which we can observe the 10ns stop time to insure 10 cycles of periodic output pulse.

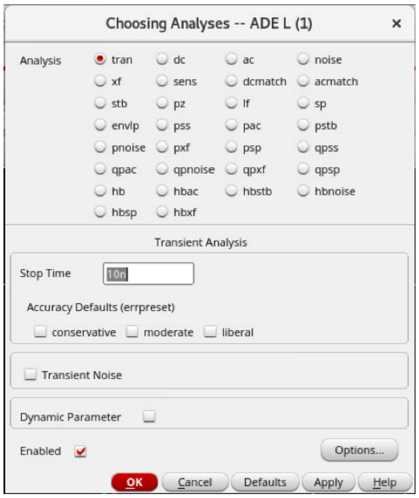
(a)

CDF Parameter	Value	Display
Frequency name for 1/period		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage		off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	0 V	off
Voltage 2	5 V	off
Period	1n s	off
Delay time	500.0p s	off
Rise time	1p s	off
Fall time	1p s	off
Pulse width	500.0p s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge	linear	off

(b)

CDF Parameter	Value	Display
Frequency name for 1/period		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage		off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	0 V	off
Voltage 2	5 V	off
Period	1n s	off
Delay time		off
Rise time	1p s	off
Fall time	1p s	off
Pulse width	500.0p s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge	linear	off

Figure 4. 2 Cadence Object Properties of $PWM_{1\ (a)}$ and $PWM_{2\ (b)}$ respectively.



Choosing Analyses -- ADE L (1)

Analysis
● tran ○ dc ○ ac ○ noise
○ xf ○ sens ○ dcmatch ○ acmatch
○ stb ○ pz ○ lf ○ sp
○ envlp ○ pss ○ pac ○ pstb
○ pnoise ○ pxf ○ psp ○ qpss
○ qpac ○ qpnoise ○ qpxf ○ qpsp
○ hb ○ hbac ○ hbstb ○ hbnoise
○ hbsp ○ hbxf

Transient Analysis

Stop Time 10n

Accuracy Defaults (errpreset)
☐ conservative ☐ moderate ☐ liberal

☐ Transient Noise

Dynamic Parameter ☐

Enabled ☑

Figure 4. 3 Cadence Transient Analysis Setup for simulation.

The selected load values were based on industry standards commonly used for various measurement scenarios. The load values considered were 100 Ohm, 1-2K Ohm, 10k Ohm, and 100K Ohm. The 100 Ohm load is typically employed for testing analog circuits, sensors, and low-power applications, while the 1-2K Ohm range is commonly used for testing digital circuits, microcontrollers, and logic gates. The 10k Ohm load is suitable for testing op-amp circuits, filters, and other analog circuits, and the 100K Ohm load is often utilized for testing high-impedance circuits like amplifiers and sensor interfaces. In the Cadence software, a comprehensive set of load values as shown in **Error! Reference source not found.**, were e mployed to evaluate the output pulse characteristics, such as duration, shape, and peak voltage.

Load R	**Peak Voltage**
100 Ω	574.072 mV
1k Ω	2.563 V
2k Ω	3.148 V
5k Ω	3.654 V
10k Ω	3.872 V
49.9k Ω	4.090 V
100k Ω	4.124 V

Table 4. 1 Load Resistor Value Selection for Output Pulse Measurements – Cadence

This extensive range of load values allowed for a detailed analysis of the pulse behavior under different load conditions, enabling the identification of the optimal load value for this specific application. Figure 4. 4 presents the simulated output waveform of the short pulse under various load resistor conditions. The waveform illustrates the response of the circuit when different load resistor values are applied. By analyzing the waveform, we can observe how the load resistor affects important characteristics of the short pulse, such as its shape, duration, and peak voltage. This comprehensive analysis provides valuable insights into the behavior of the circuit under different load conditions and aids in the selection of an appropriate load resistor for optimal performance.

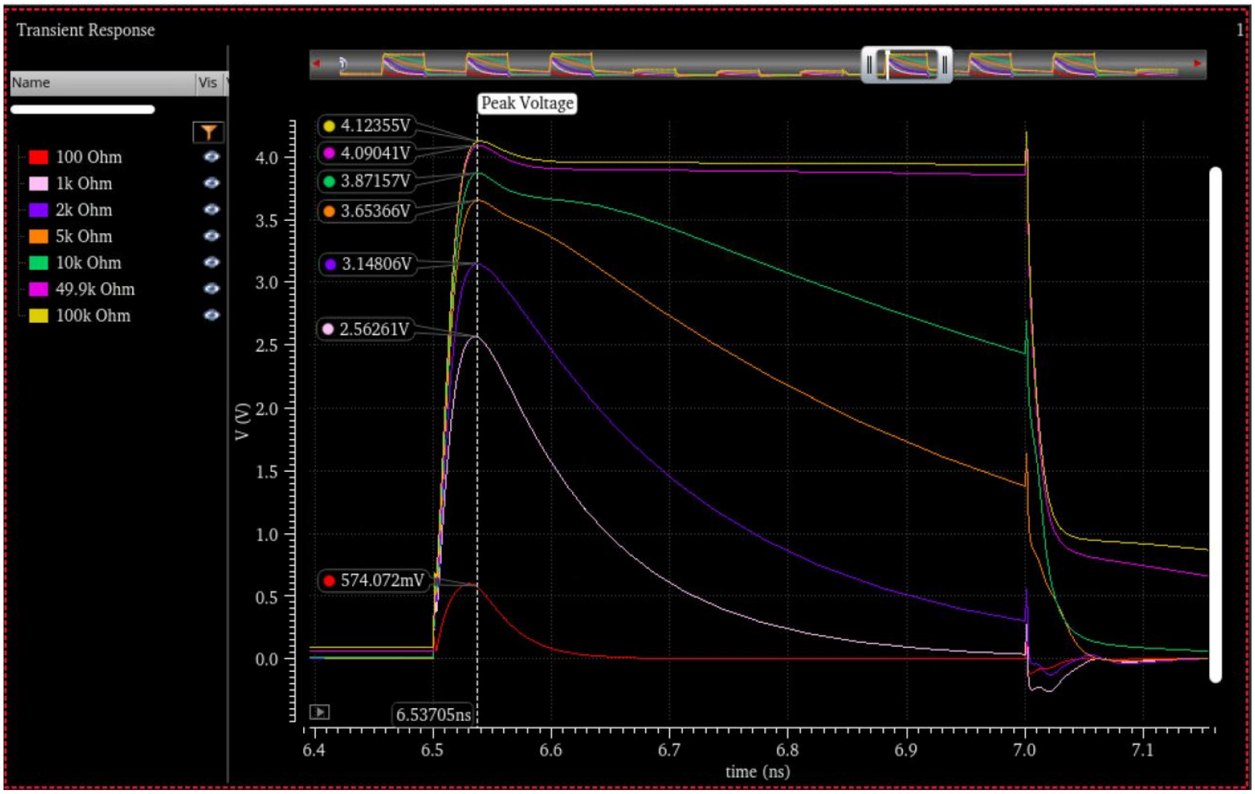


Figure 4. 4 Comparison of Output Pulse Waveforms for Various Load Resistors

The results, as shown in the table above, indicate that the peak voltage of the output pulse increases with higher load resistor values. However, it is crucial to note that as the load resistance increases beyond a certain point, the pulse characteristics start to deviate from the desired waveform. With higher load resistors, there is an observed deformation of the pulse shape and an increase in pulse duration. This distortion suggests that the load resistor value significantly impacts the pulse generation process. To achieve optimal performance, it is essential to select a load resistor that balances the desired peak voltage with maintaining the integrity of the pulse shape and duration.

Based on the results in Figure 4. 4 and the provided table, a load resistor value of 2k Ω stands out as the ideal choice for further analysis. It offers a favorable combination of sufficient peak voltage (3.148V) and a pulse waveform that remains relatively close to the desired shape and duration. Further analysis and experimentation can be conducted using this optimal load resistor value to evaluate the pulse generator's performance in more detail.

The simulation results showed that the proposed Short Pulse Generator circuit was able to generate a periodic sub-nano second pulse with duration of 488.72ps and voltage amplitude of 3.148V from and input of 2V DC supply. The output waveform of the simulation is presented in Figure 4. 5. The pulse width was calculated by taking the 10% of the rise time and 90% of the fall time as demonstrated in the waveform presented in Figure 4. 6.

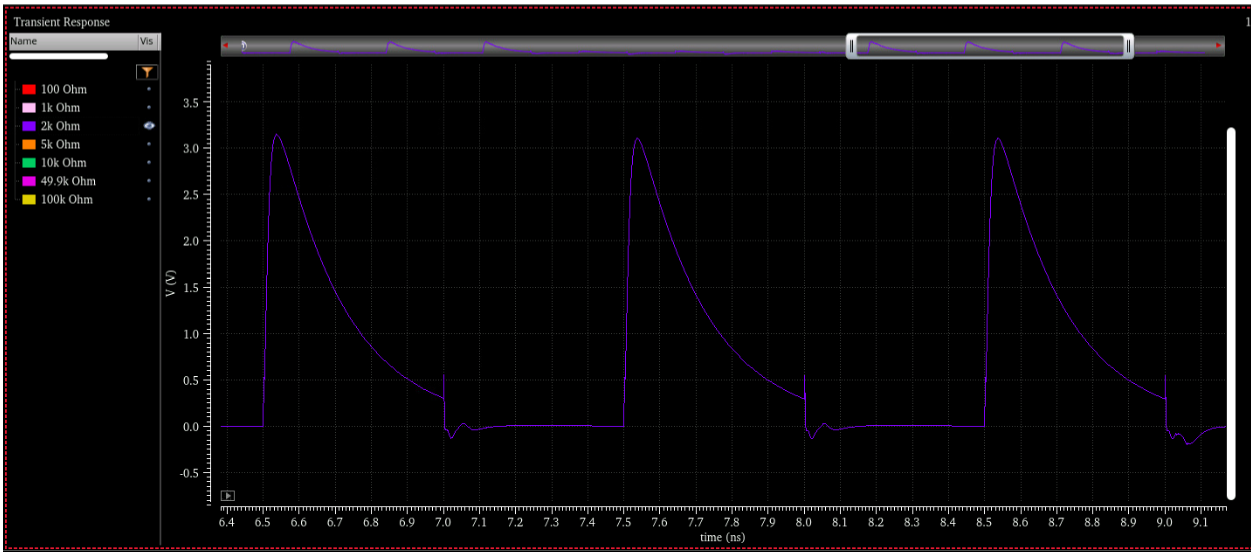


Figure 4. 5 Output Waveform of the Short Pulse Generator from Cadence.

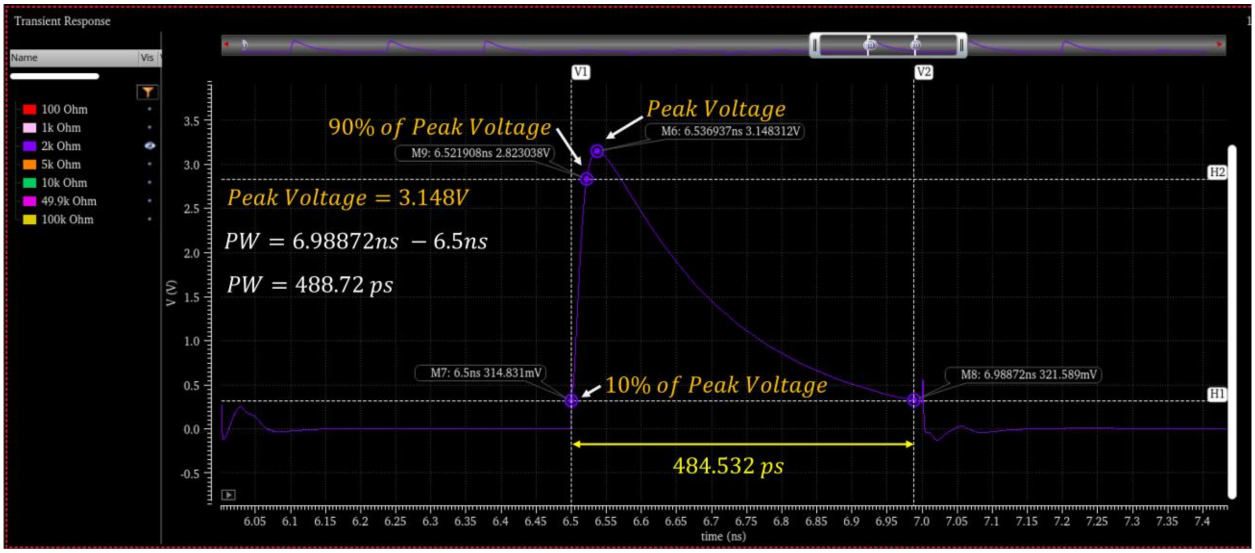


Figure 4. 6 Sub-nano Second Pulse Duration Response Time Analysis.

The generated pulse demonstrated the effectiveness of the proposed Short Pulse Generator circuit, as it was able to generate a high-speed periodic sub-nano second pulse with a short duration of less than half of a nano second with the integration of MOSFETs as highspeed switches. The results obtained from the simulation indicate that the proposed circuit has the potential to be used in various applications that require high-speed, short-duration pulses. Further improvements can be made by optimizing the circuit parameters to achieve better performance in terms of pulse amplitude, even shorter duration period, and repetition rate as much higher operating frequencies.

4.2 PERFORMANCE EVALUATION OF THE SHORT PULSE GENERATOR

The proposed circuit consists of 2 stage capacitors, hence 2 stage system. With V_{CC} of 2V, the theoretical output should have been 4 volts based on $N * V_{CC}$ where N is the number of capacitors. Although the proposed Short Pulse Generator was designed to generate a pulse with amplitude equal to N times the input voltage ($N * V_{CC}$), the simulation results showed a peak pulse voltage of 3.148V. There could be several reasons for this discrepancy between the expected and observed output amplitude.

One possible reason could be the limitations of the 180nm technology used for designing and simulating the circuit. The parasitic capacitances and resistances in the MOSFETs and interconnects may have resulted in voltage drops and reduced the output voltage. Additionally, the rise and fall times of the PWM signals could have affected the charging and discharging of the capacitors, leading to non-ideal switching behavior and reduced efficiency.

Another possible reason why the output pulse amplitude did not reach the desired level of $N * V_{CC}$ could be attributed to the MOSFET's breakdown voltage limitation. MOSFETs have a maximum breakdown voltage, and if this limit is exceeded, the device will stop functioning, and there is a risk of permanent damage to the MOSFET. To overcome this limitation, stacked MOSFETs can be used as switches since the breakdown voltage of a single MOSFET is limited [13]. In this approach, multiple MOSFETs are stacked together in a series to increase the total voltage handling capacity. By doing this, the breakdown voltage limit can be exceeded while still maintaining the device's safe operating parameters. This technique is commonly used in high-power applications, where a single MOSFET cannot handle the voltage or current requirements. Additionally, stacking MOSFETs may also result in an increased on-resistance and decreased efficiency, so the trade-offs between breakdown voltage and performance should be carefully considered in the design process. However, this method also increases the complexity of the circuit design, and careful consideration must be taken to ensure proper operation and reliability.

Overall, while the observed output voltage of the Short Pulse Generator did not meet the expected amplitude, the results provide valuable insights into the challenges and limitations of on-chip pulse generators using MOSFET switches. The output voltage of the Short Pulse

Generator was measured to be 3V with a DC supply of 2V. This result demonstrates the potential of the proposed design in generating output pulses with amplitudes greater than the input voltage, up to a maximum of $N * V_{CC}$ in addition to sub-nano second pulse width and repetition. This suggests that with appropriate adjustments to the design and implementation, higher output voltages could be achieved. However, further research and experimentation would be necessary to optimize the design and overcome the limitations discussed earlier. Further optimization of the design and choice of components could potentially improve the performance of the circuit in future iterations.

Chapter 5. PROTOTYPING

5.1 BREADBOARD PROTOTYPE TESTING AND RESULTS

The proposed design of the Short Pulse Generator was implemented on a breadboard circuit for experimental validation. The breadboard circuit allowed for easy prototyping and testing of the design concept before moving on to more advanced fabrication processes. The breadboard circuit consisted of the key components required for the operation of the Short Pulse Generator. The circuit utilized the IRFZ44N MOSFET as high-speed switches, known for their robustness and performance. The IRFZ44N MOSFET offers a voltage rating of 55V, a continuous drain current of 49A, and a low on-resistance (R_{DS} (on)) of 17mΩ, making it an ideal choice for high-power applications. These specifications ensured that the MOSFET could handle the required voltage and current levels effectively. The breadboard circuit configuration is depicted in Figure 5. 1, providing a visual representation of the arrangement and interconnection of the various components.

Overall, the combination of these components on the breadboard formed the foundation of the Short Pulse Generator, enabling the desired pulse generation functionality to be achieved. Initially, an Arduino microcontroller was utilized to generate the required pulse width modulation (PWM) signals for the experiment. However, to further enhance the control and precision of the PWM generation process as well as to eliminate the need of an external function generator, an analog circuit driven by a NE555 timer was subsequently introduced as a replacement. The integration of the NE555 timer, along with a transistor network, facilitated the generation of two complementary PWM signals with the desired phase separation while making it more suitable for PCB application as we will see in section 5.2. A combination of potentiometers were employed to finely adjust the duty cycle and frequency of the PWM signals, allowing for precise customization. This modification significantly improved the accuracy and versatility of the PWM setup, ultimately optimizing the performance and functionality of the short pulse generator. The waveform of meticulously calibrated pulse width modulation (PWM) signals is depicted in Figure 5. 2.

Finally, a load resistor was included in the circuit to simulate a real-world application and to measure the output pulse characteristics. It allowed for the observation and analysis of the generated pulses, including their duration and amplitude.

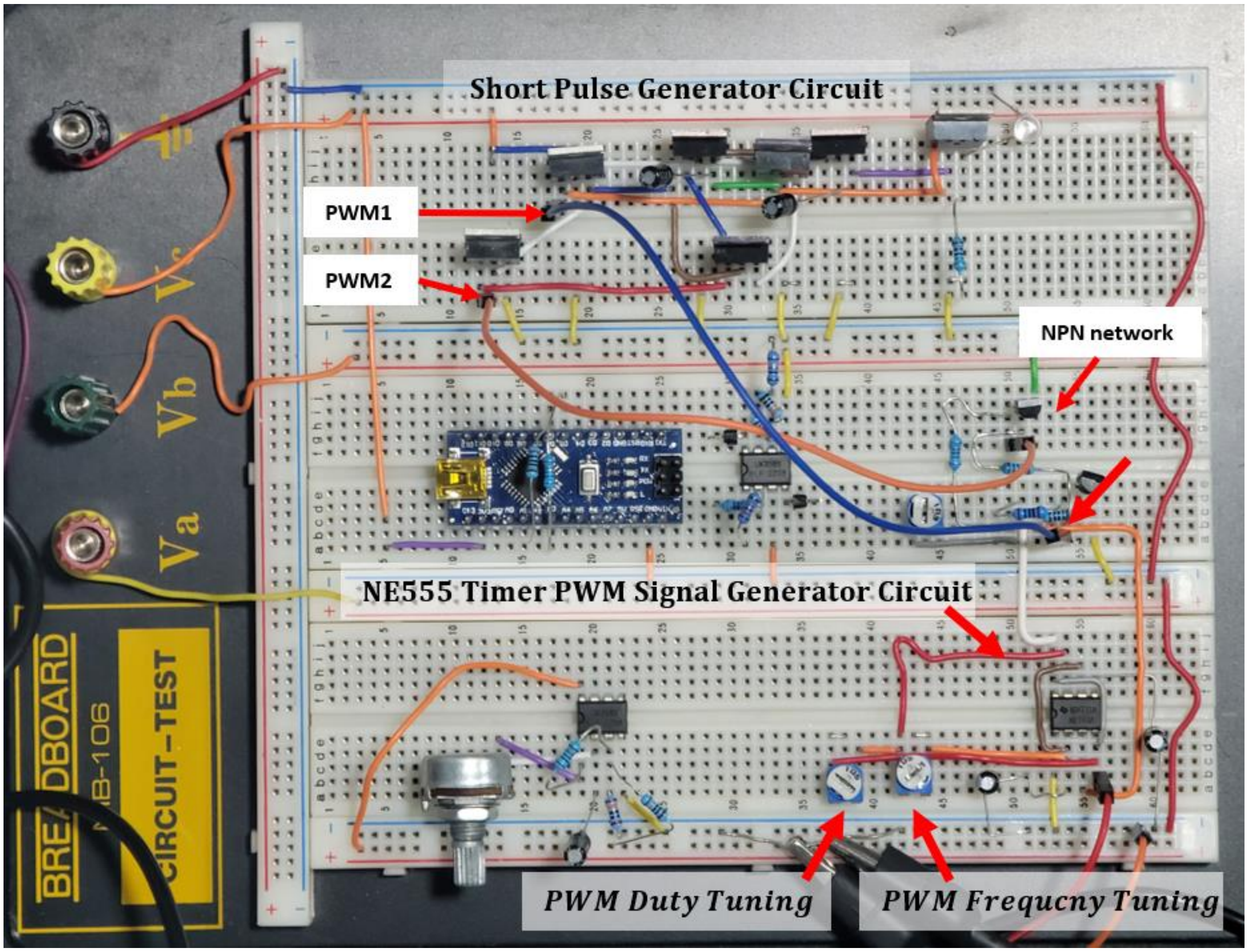


Figure 5. 1 Breadboard Circuit Configuration of the Short Pulse Generator.

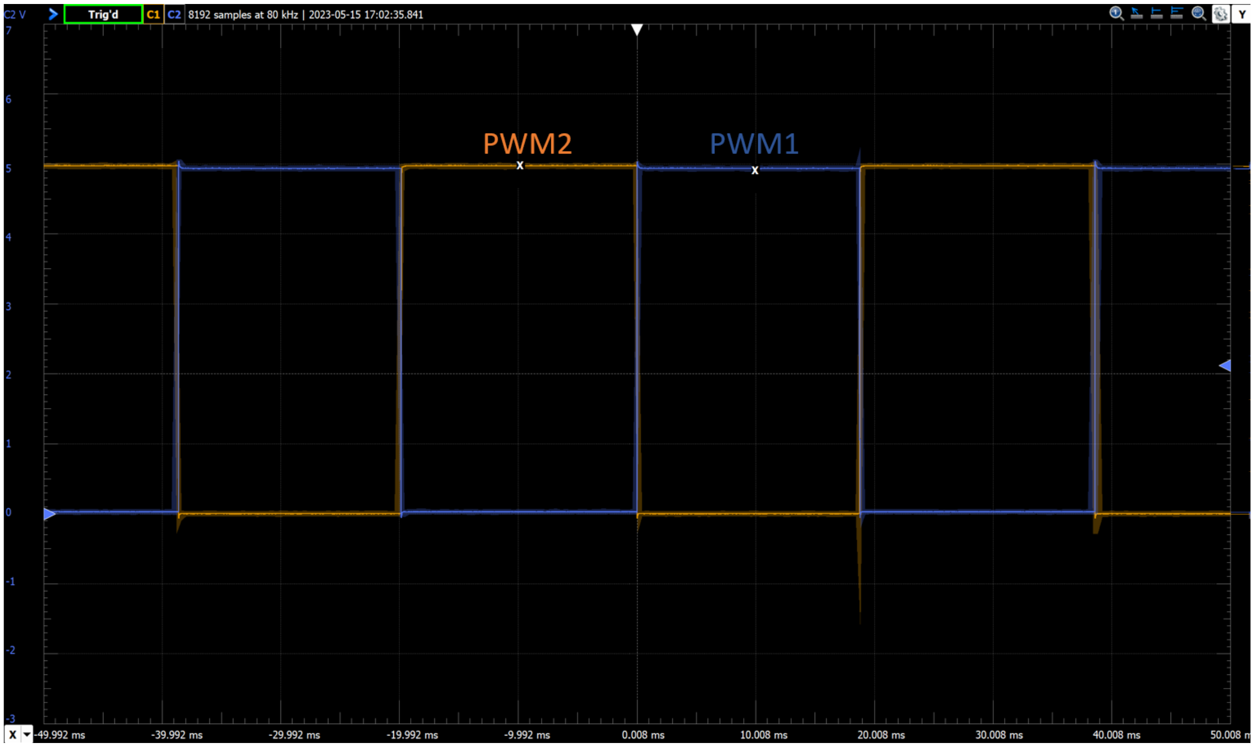


Figure 5. 2 Waveform of the PWM Signals generated by 555 Timer in Conjunction with Transistor Network (PWM tuned to 50% duty cycle) - Breadboard Prototype.

Throughout the construction of the breadboard circuit, attention was given to ensuring proper connections, component placement, and electrical insulation. The circuit was powered using a suitable 2V DC power supply, providing the necessary voltage levels for the operation of the components and measured using an onboard Oscilloscope integrated into the Analog Discovery 2 device. An additional 5V was also supplied to the input pin of the 555 timer IC using the available on-board power supply integrated into the Analog Discovery 2.

The breadboard circuit provided a practical platform for testing and validating the proposed design. It allowed for the verification of the circuit's functionality, pulse generation capabilities, and performance characteristics. The experimental results obtained from the breadboard circuit served as a foundation for further refinement and optimization of the design before progressing to more complex implementations. Figure 5. 3 showcases the arrangement and configuration employed for the measurements in the experimental setup.

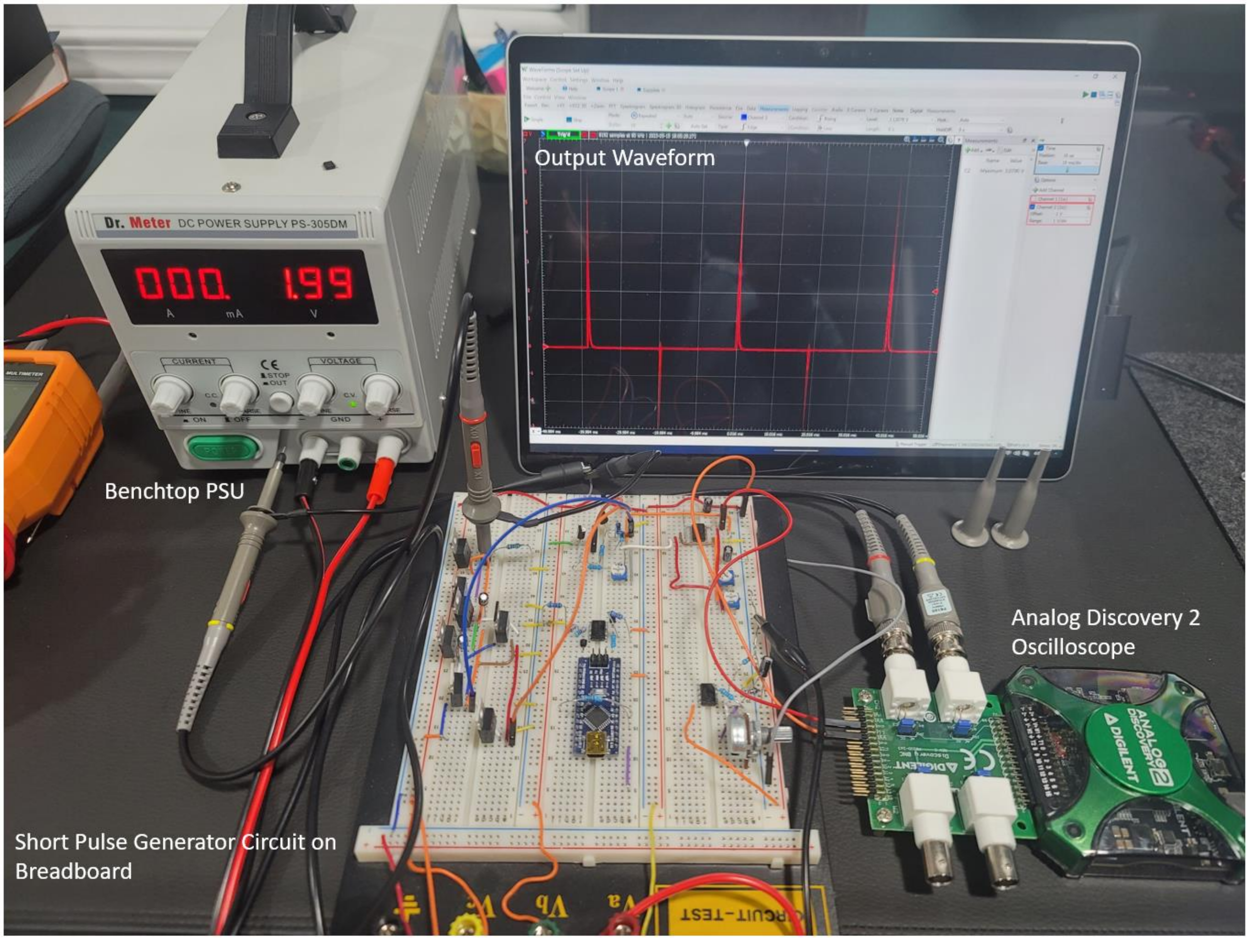
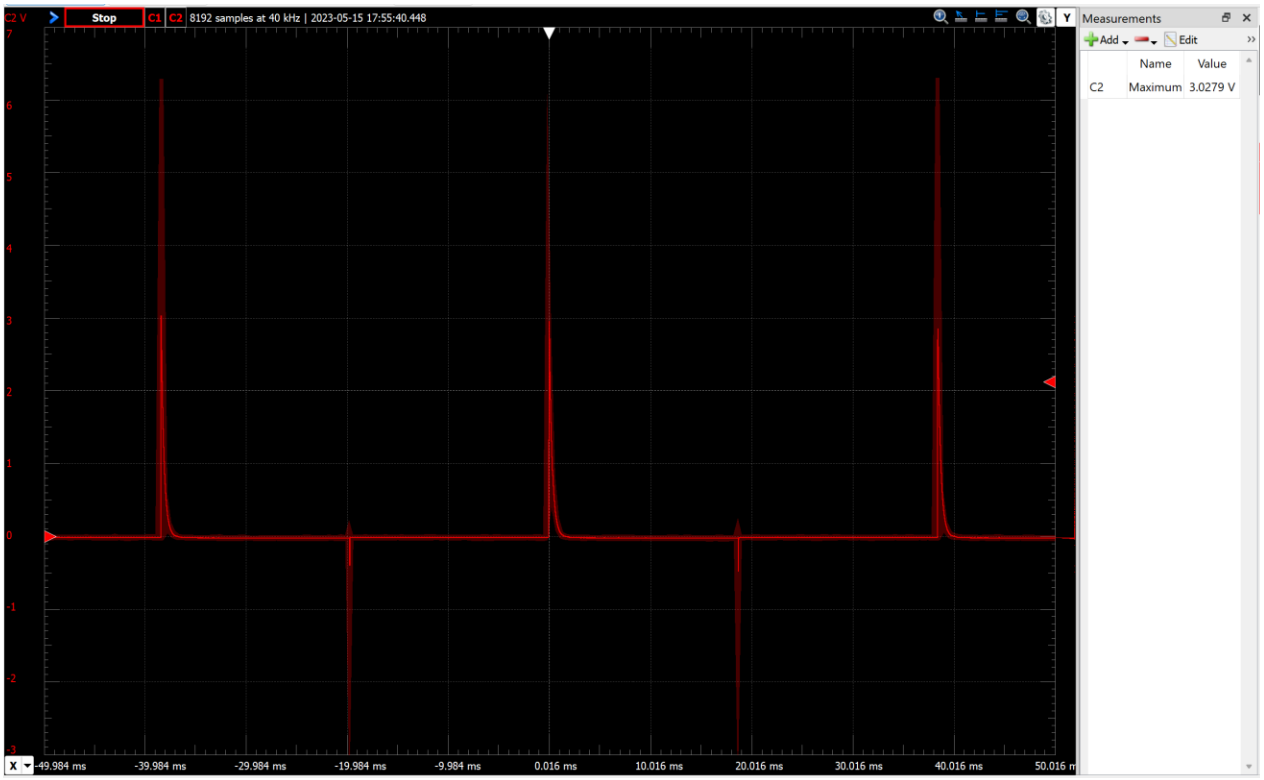


Figure 5. 3 Measurement Configuration and Setup of the Breadboard Circuit.

The breadboard circuit, optimized for practical breadboard applications, was successfully tested to validate the performance of the proposed short pulse generator. The measured peak voltage of the output pulse was found to be 3.0279V as shown in Figure 5. 4, which closely aligns with the peak voltage of 3.016V obtained in the Cadence simulation. This strong correlation between the simulated and measured results confirms the accuracy and reliability of the design. The optimized circuit demonstrated its capability to generate the desired repeated short pulses with consistent output voltage, further reinforcing the effectiveness and feasibility of the proposed design for practical applications.



	Name	Value
C2	Maximum	3.0279 V

Figure 5. 4 Output Waveform of the Short Pulse Generated by the Optimized Breadboard Circuit.

In the following section, the focus shifts towards the integration of the short pulse generator from the breadboard prototype to a more practical implementation on a printed circuit board (PCB). This chapter aims to explore the challenges and considerations involved in translating the optimized design onto a PCB platform. The PCB integration offers numerous advantages, including compactness, durability, and ease of manufacturing. By transitioning from the breadboard to a PCB, the short pulse generator can be further refined and prepared for real-world applications. The chapter delves into the design considerations, layout optimization, and performance evaluation of the PCB-integrated short pulse generator, providing valuable insights into the practical implementation of this novel circuit.

5.2 PCB PROTOTYPE DESIGN AND TESTING

In this section, the focus is on the prototyping of the short pulse generator circuit on a printed circuit board (PCB). The design process involved the use of the EasyEDA schematic capture tool, which facilitated the creation of an organized and structured schematic representation of the circuit. The schematic served as a blueprint for the layout design, ensuring the proper placement and interconnection of components.

During the PCB layout stage, careful consideration was given to component selection. While there were similarities between the SMD components used in the PCB prototype and the through hole components used in the breadboard circuit, certain factors, such as package size and performance considerations, influenced the specific component choices for the PCB prototype. The selection aimed to strike a balance between performance, availability, and ease of assembly. Figure 5. 5 presents the schematic representation of the short pulse generator circuit designed in EasyEDA schematic capture tool.

The schematic of the short pulse generator circuit showcases the modular nature of the design, with distinct blocks of circuits dedicated to specific operations. Notably, the inclusion of a buck converter circuit stands out, as it plays a crucial role in supplying a stable 2V DC voltage to the short pulse generator network. This buck converter circuit efficiently steps down the input DC voltage of 5V to the desired voltage level required for the operation of the short pulse generator. In addition to the buck converter circuit, the schematic incorporates a transistor network responsible for generating the phase-shifted PWM signals as mentioned in section 5.1. the output signal produced by the 555 timer IC can sometimes fall below 5V, leading to inconsistent performance. To address this issue, pull-up resistors were incorporated into the design. These resistors effectively elevate the signal voltage to a stable 5V level, ensuring that the PWM signals are consistently scaled within the desired voltage range. This modification prevents the voltage across the drain-to-source (VDS) of the MOSFETs from falling below the gate-to-source voltage (VGS). Maintaining a sufficient VDS voltage above the VGS threshold is crucial for proper MOSFET operation and avoids potential performance issues or undesired behavior. The inclusion of pull-up resistors in the design effectively addresses this concern and guarantees a stable and reliable supply of PWM signals to the MOSFET gates, ensuring optimal performance and preventing any potential complications due to insufficient voltage levels.

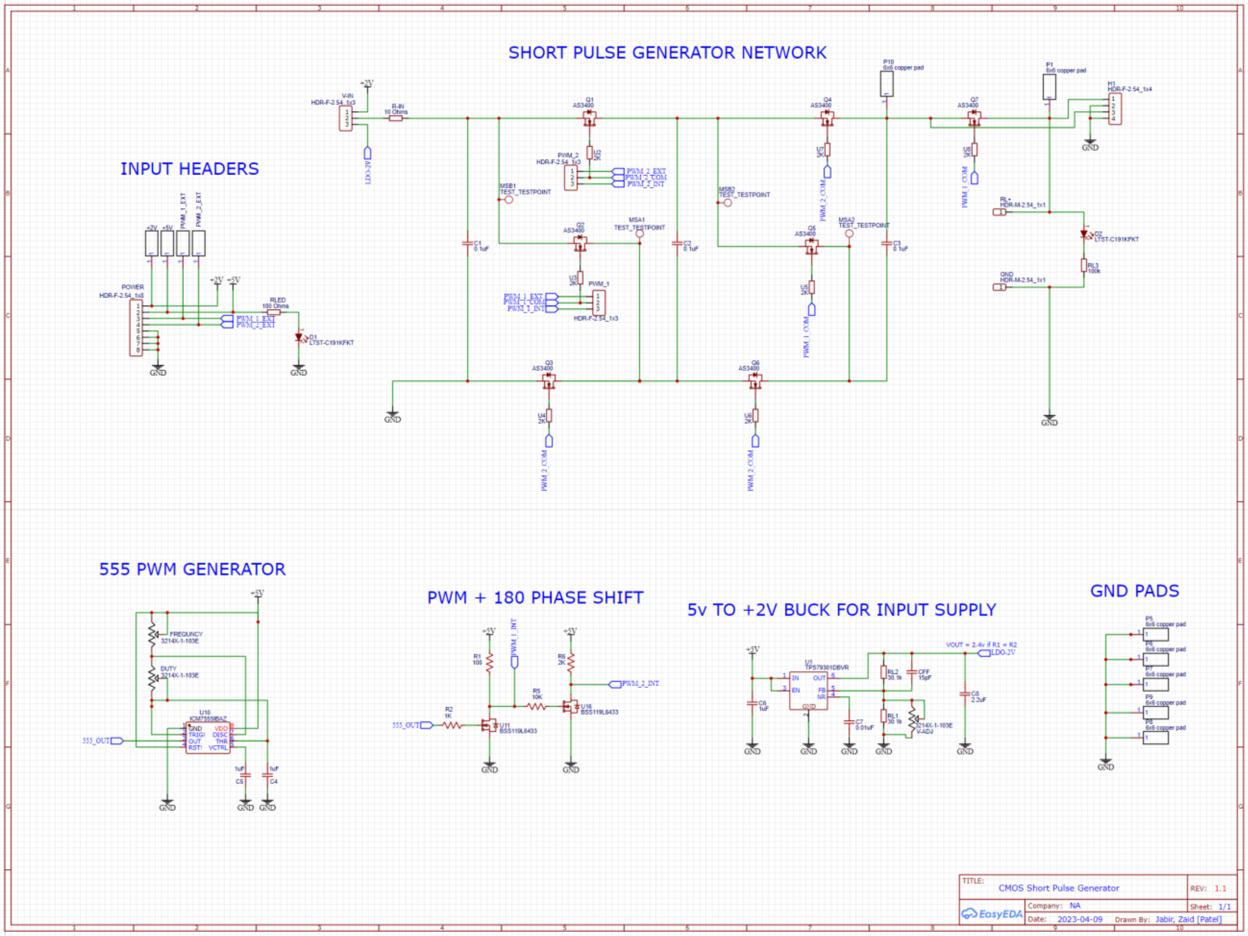


Figure 5. 5 Schematic of Short Pulse Generator Designed in EasyEDA Schematic Capture tool.

To gain a comprehensive understanding of the circuit configuration proposed for the PCB design, Figure 5. 6 presents a detailed block diagram. This diagram provides a visual representation of the various circuit blocks and their interconnections. By examining the block diagram, one can discern the distinct functional units and their relationships, aiding in the comprehension of the overall circuit design.

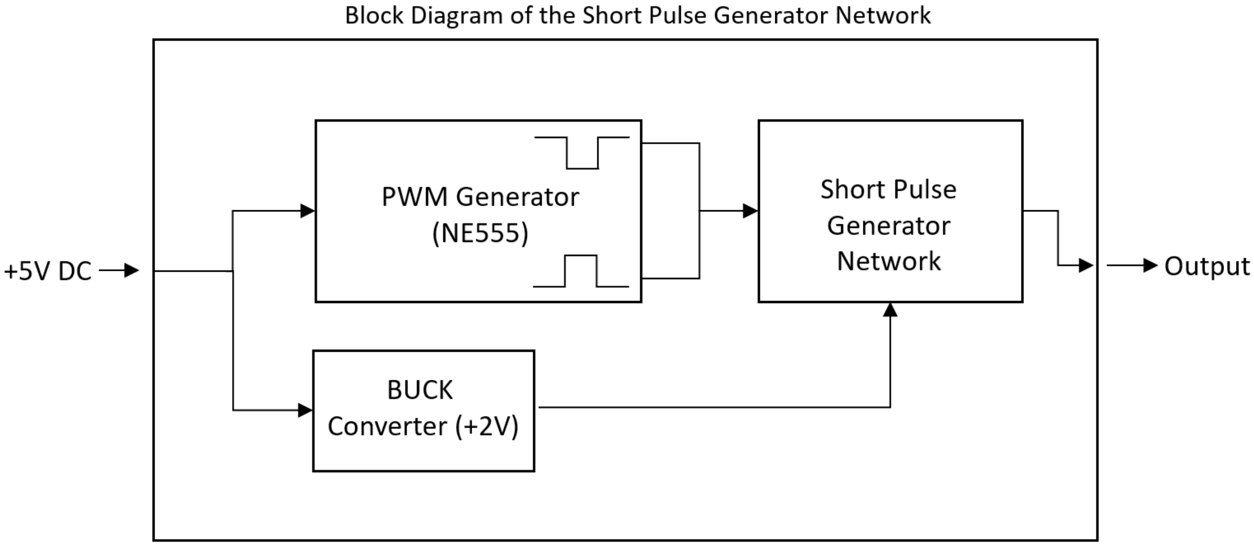
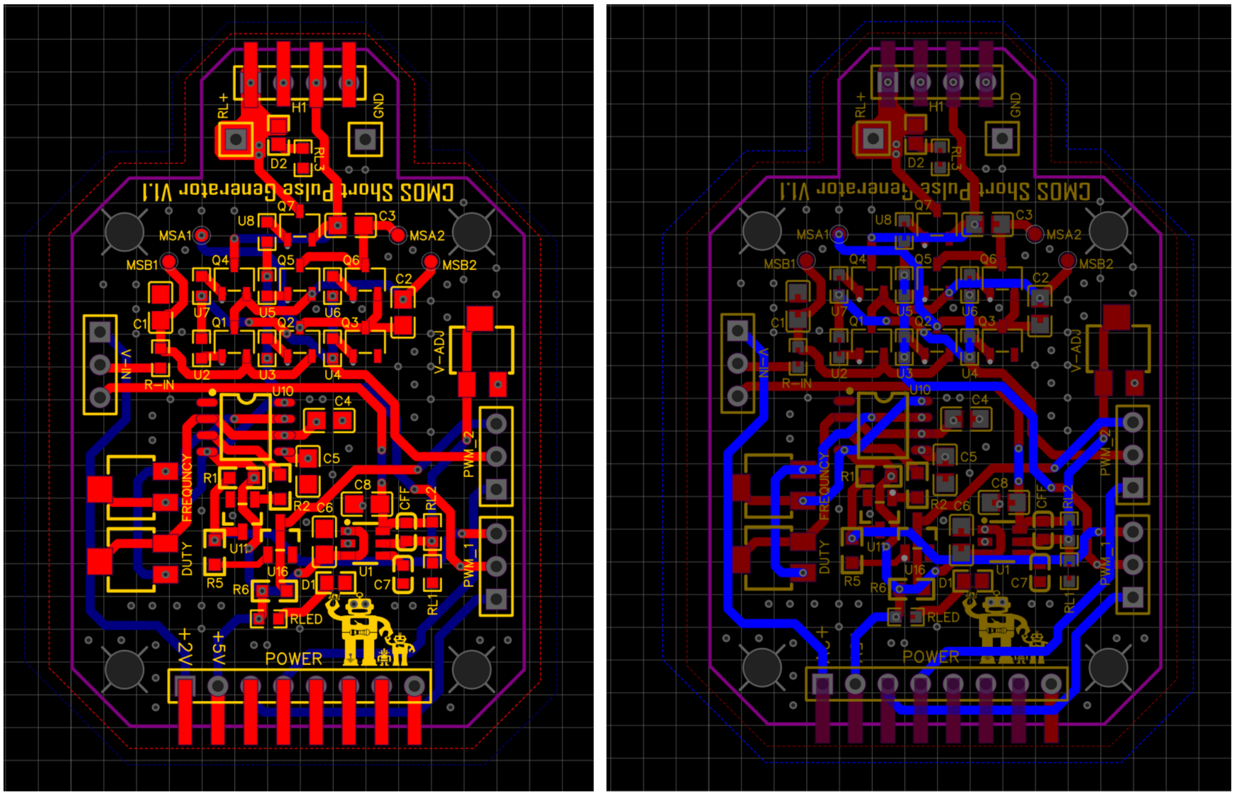


Figure 5. 6 Block Diagram of the Reduced Circuit Proposed for PCB Integration.

To streamline the power supply requirements, a buck converter IC was employed to reduce the need for separate DC supplies to power the 555 timer IC and the input of the Short Pulse Generator. This buck converter circuit efficiently converts the available 5V input to a stable 2V output, effectively minimizing the supply requirement to a single 5V input. To enhance the flexibility and tunability of the circuit, a potentiometer was incorporated in parallel to one of the resistors in the resistor divider to provide an adjustable output capability for future adjustments. By introducing a potentiometer into the design, the output of the circuit can be fine-tuned and customized according to specific requirements. By integrating the buck converter into the circuit, the complexity and number of power sources are significantly reduced, simplifying the overall system design and enhancing its practicality for various applications. This consolidation of power supply enables a more compact and efficient implementation of the circuit, providing a practical solution for powering the 555 timer IC and the Short Pulse Generator without the need for multiple power sources.

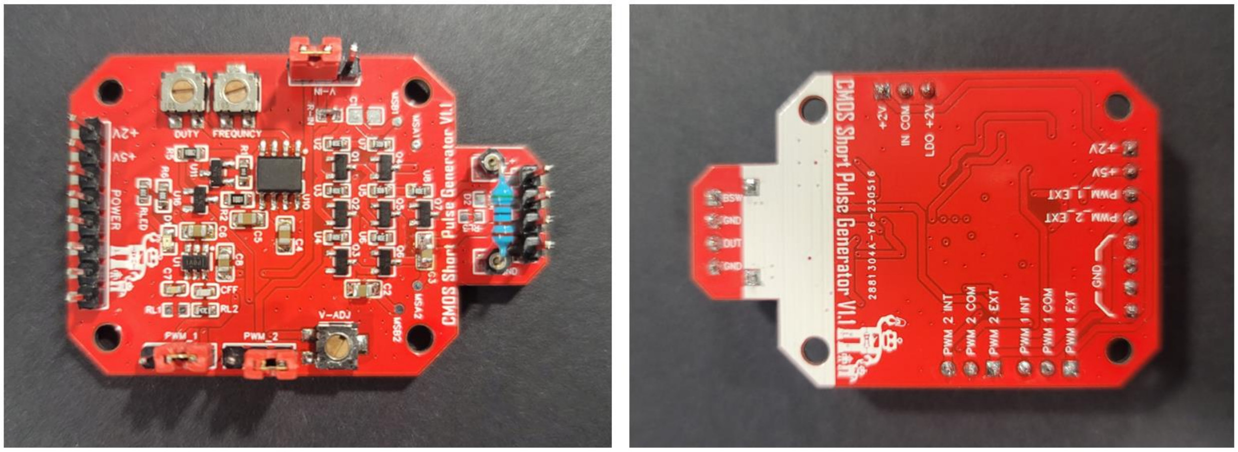
The layout design of the PCB prototype was meticulously executed to achieve multiple objectives, including optimizing signal integrity, minimizing noise, ensuring proper power distribution, and achieving a compact design. Careful consideration was given to the placement of components to minimize signal interference and maintain appropriate spacing. The layout design aimed to maximize the utilization of board space while maintaining clear signal paths and efficient power delivery. Figure 5. 7 illustrates the result of this comprehensive layout design approach, highlighting the strategic component placement and the overall compactness and routing of the PCB prototype.



(a) (b)

Figure 5. 7 PCB Layout of the Short Pulse Generator Circuit, Including Top (a) and Bottom (b) Layers.

Once the layout design was completed, the PCB prototype was fabricated using industry-standard techniques. Attention was given to the quality of fabrication, ensuring accurate reproduction of the layout design. Following fabrication, the prototype underwent thorough testing and validation to verify its functionality and performance. Figure 5. 8 showcases the fabricated PCB of the short pulse generator circuit, providing a visual representation of the physical implementation of the design. Figure 5. 9 shows the layout representation highlighting the various circuit blocks and their placement on the PCB. The labeled blocks indicate the specific components and their interconnections, allowing for a visual understanding of the physical arrangement of the circuit on the board.



(a)

(b)

Figure 5. 8 Completed PCB Prototype of the Short Pulse Generator Circuit, Including Top (a) and Bottom (b) Layers.

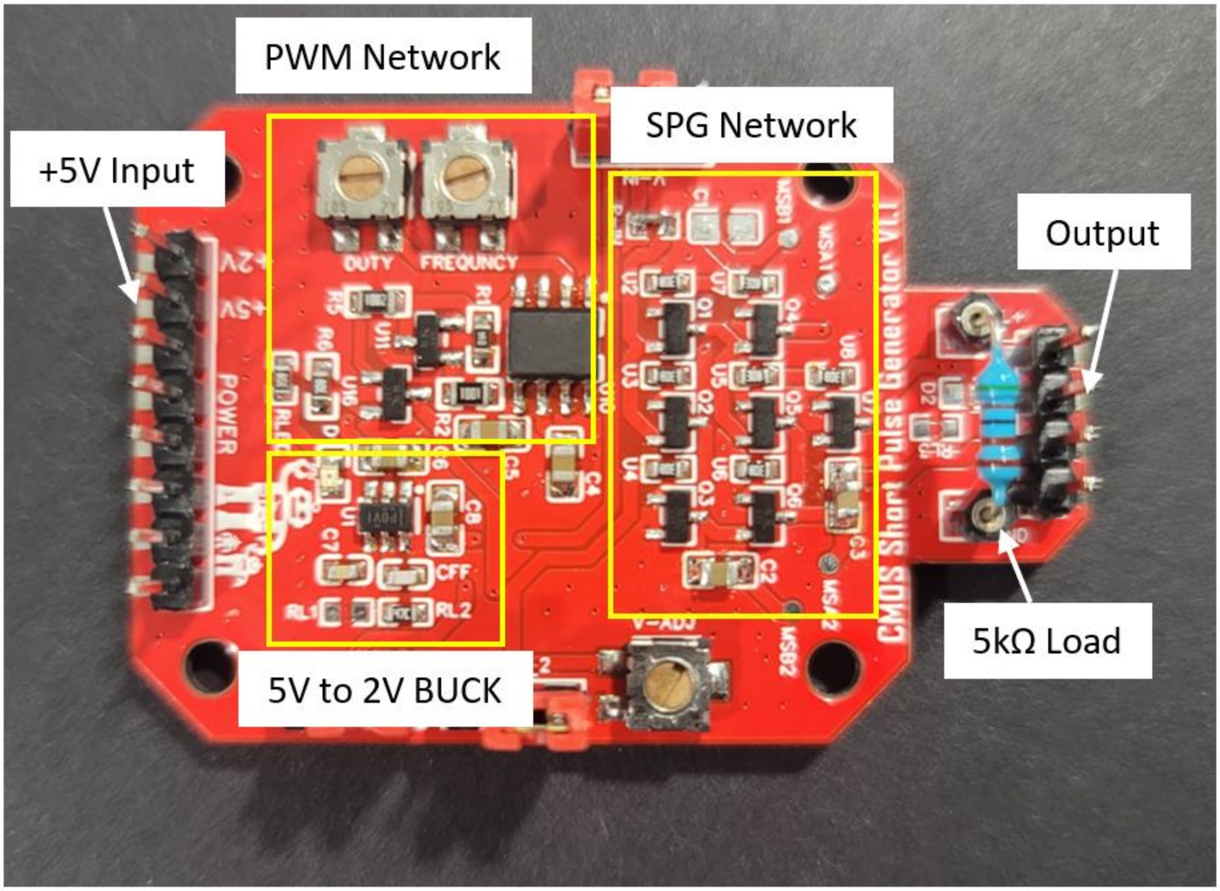


Figure 5. 9 PCB layout showcasing the arrangement of circuit components.

The PCB prototyping phase served as a critical step in the development process, transitioning the circuit from a conceptual design to a physical implementation. It offered advantages such as compactness, durability, and the potential for mass production. The next chapter will focus on the evaluation and analysis of the PCB-integrated short pulse generator, shedding light on its performance, reliability, and suitability for real-world applications.

5.3 PCB PROTOTYPE RESULTS

The fabricated PCB of the Short Pulse Generator was subjected to thorough testing to assess its performance and validate its functionality. The PCB testing setup, as depicted in **Error! Reference source not found.**, involved the utilization of a single 5V DC input provided b y an external power supply unit (PSU). On the PCB board, a dedicated buck converter circuit than converts the 5V input voltage

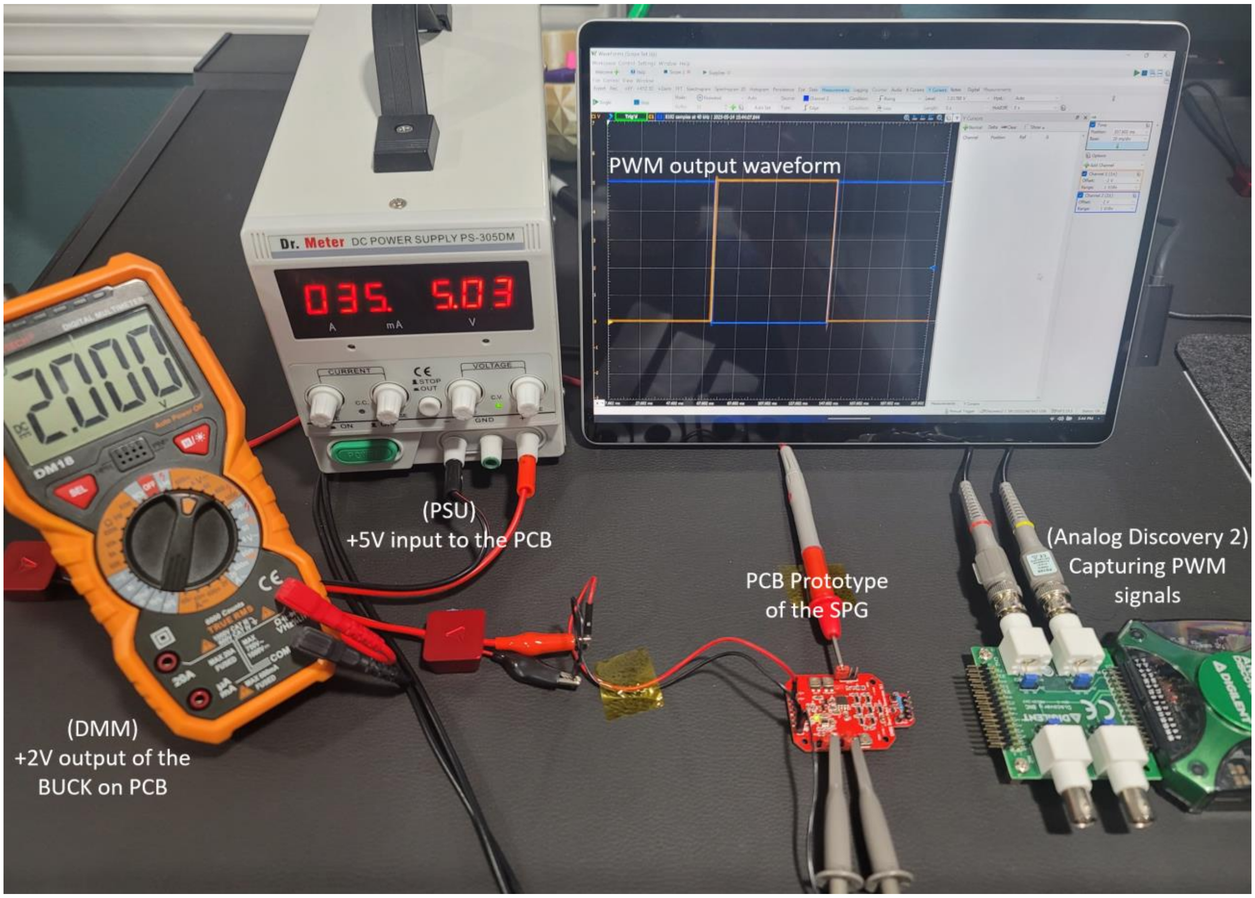
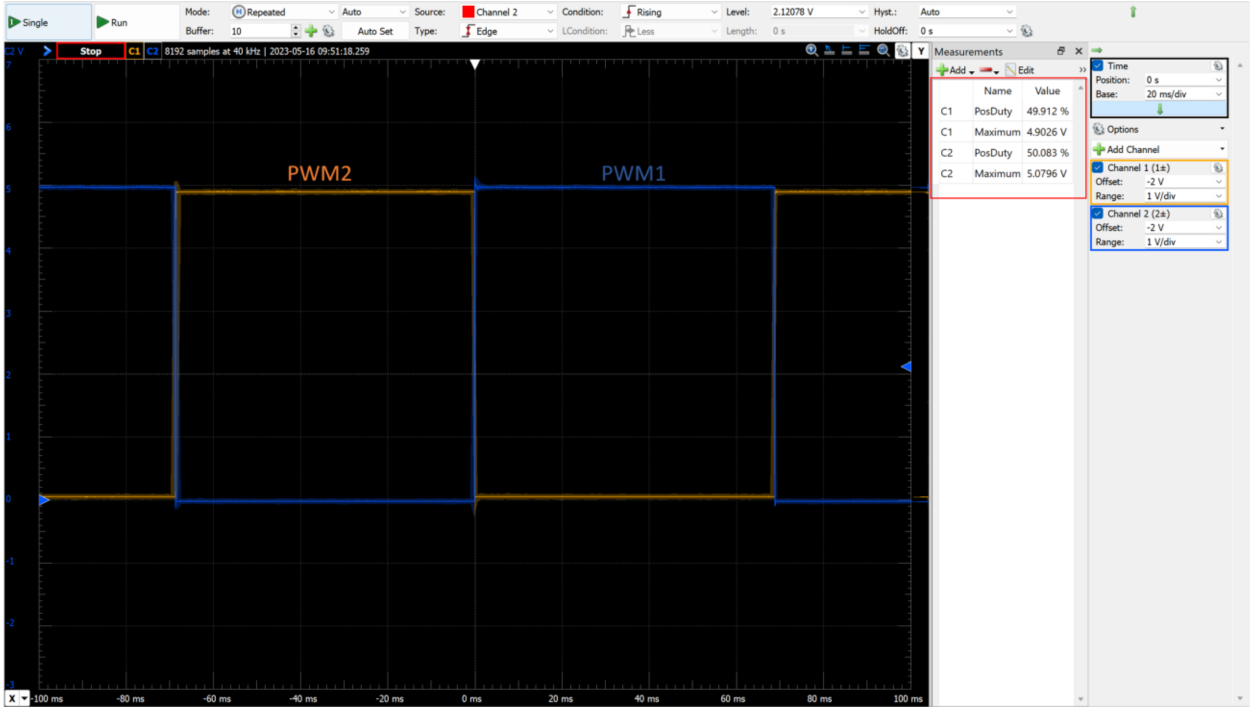


Figure 5. 10 PWM Measurement Configuration and Setup of the PCB Prototype.

to the desired 2V DC voltage level. The buck converter circuit efficiently reduced the voltage and ensured a stable and regulated 2V DC supply for the Short Pulse Generator circuit. This onboard buck converter eliminated the need for an additional power supply, simplifying the setup and enhancing the overall efficiency and functionality of the testing process. The functionality of the buck converter circuit was validated by measuring the output using a multimeter, positioned on to the left in **Error! Reference source not found.**. The PWM1 and PWM2 signals were carefully adjusted to achieve a duty cycle of approximately 50%, as observed in **Error! Reference source not found.**.



Mode: Repeated
Auto
Buffer: 10
Auto Set
Source: Channel 2
Type: Edge
Condition: Rising
LCondition: Less
Level: 2.12078 V
Length: 0 s
Hyst.: Auto
HoldOff: 0 s

8192 samples at 40 kHz | 2023-05-16 09:51:18.259

Measurements

	Name	Value
C1	PosDuty	49.912 %
C1	Maximum	4.9026 V
C2	PosDuty	50.083 %
C2	Maximum	5.0796 V

Time
Position: 0 s
Base: 20 ms/div

Channel 1 (1±)
Offset: -2 V
Range: 1 V/div

Channel 2 (2±)
Offset: -2 V
Range: 1 V/div

Figure 5. 11 Waveform of the PWM Signals generated by 555 Timer in Conjunction with Transistor Network (PWM tuned to 50% duty cycle) - PCB Prototype.

To ensure the consistency and reliability of the Short Pulse Generator circuit, the same approach was followed for selecting the load resistor during the PCB testing phase. The values used in the Cadence simulation were applied to the physical PCB circuit. **Error! Reference source not found.** illustrates the relationship between different load resistor values and the corresponding peak output voltage of the Short Pulse Generator PCB circuit.

Load R	Peak Voltage
100 Ω	1.593 V
1k Ω	2.900 V
2k Ω	3.015 V
5k Ω	2.891 V
10k Ω	2.932 V
49.9k Ω	3.002 V
100k Ω	2.988 V

Table 5. 1 Load Resistor Value Selection for Output Pulse Measurements – PCB

The objective was to evaluate the behavior of the output pulse waveform with different load resistors in a real-world scenario. The results, as depicted in Figure 5. 12, revealed a similar trend to the Cadence simulation. That is when the load resistance increased beyond a certain threshold, the pulse waveform began to exhibit distortions and longer durations. Based on the observed results, it was evident that the load resistor of 2k Ω offered the optimal balance between achieving the desired peak voltage and maintaining the integrity and shape of the output pulse waveform. Therefore, this value was chosen as the preferred load resistor for the PCB implementation, ensuring the best performance and functionality of the Short Pulse Generator circuit in practical applications.

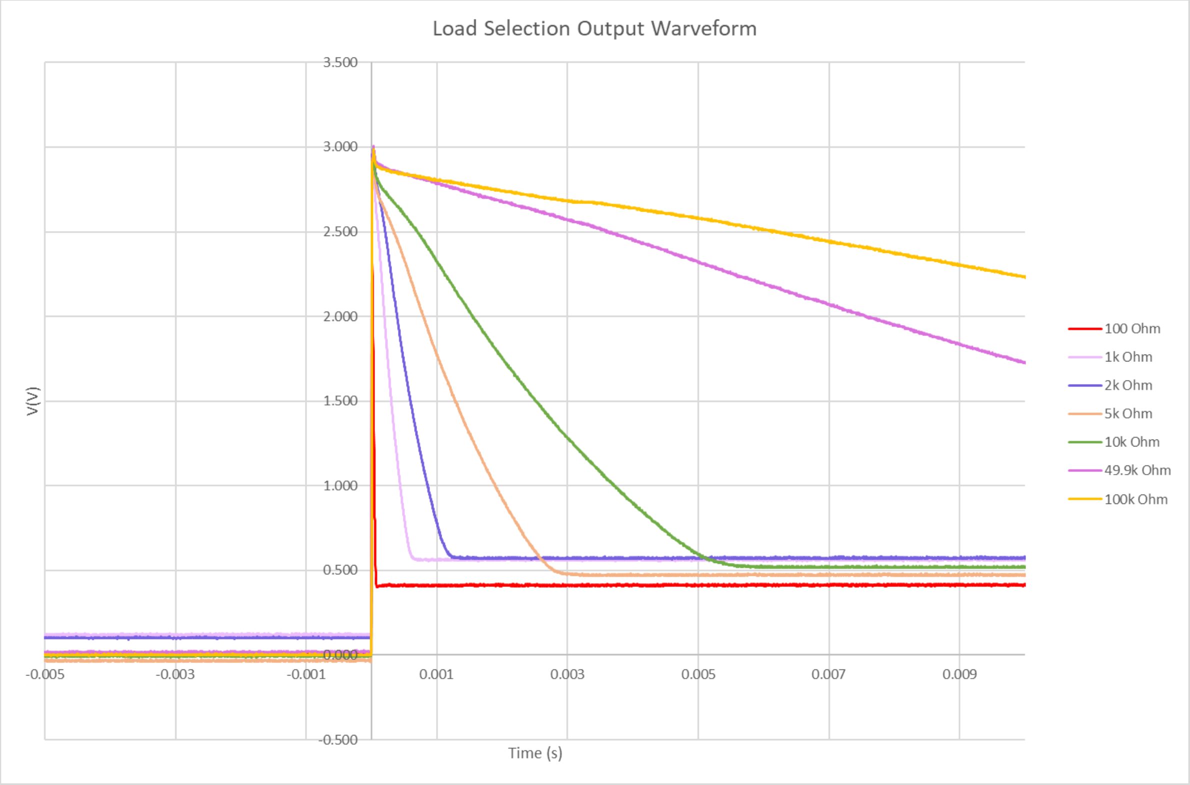


Figure 5. 12 Comparison of Output Pulse Waveforms with Various Load Resistors tested on PCB Prototype

Figure 5. 13 illustrates the test setup used to measure the output of the PCB prototype, while Figure 5. 14 presents the resulting output waveform measured across a 2kΩ load resistor.

The waveform captured in Figure 5. 14 provides visual confirmation of the successful generation of the desired short pulses, serving as empirical evidence of the PCB's accurate translation of the designed circuit. The clear and distinct short pulses observed in the waveform validate the functionality and effective operation of the PCB prototype, affirming its ability to maintain signal integrity and generate the intended waveform.

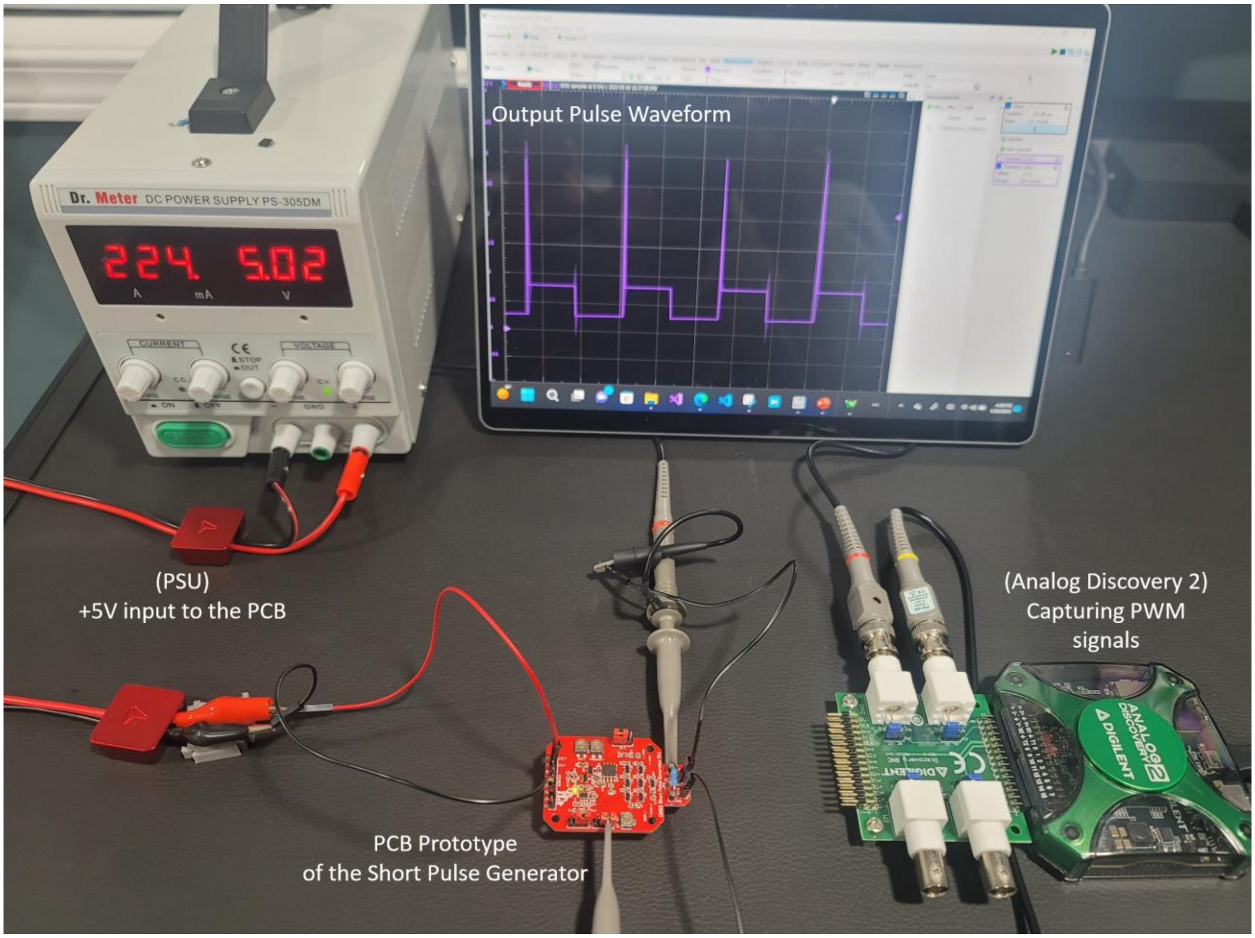
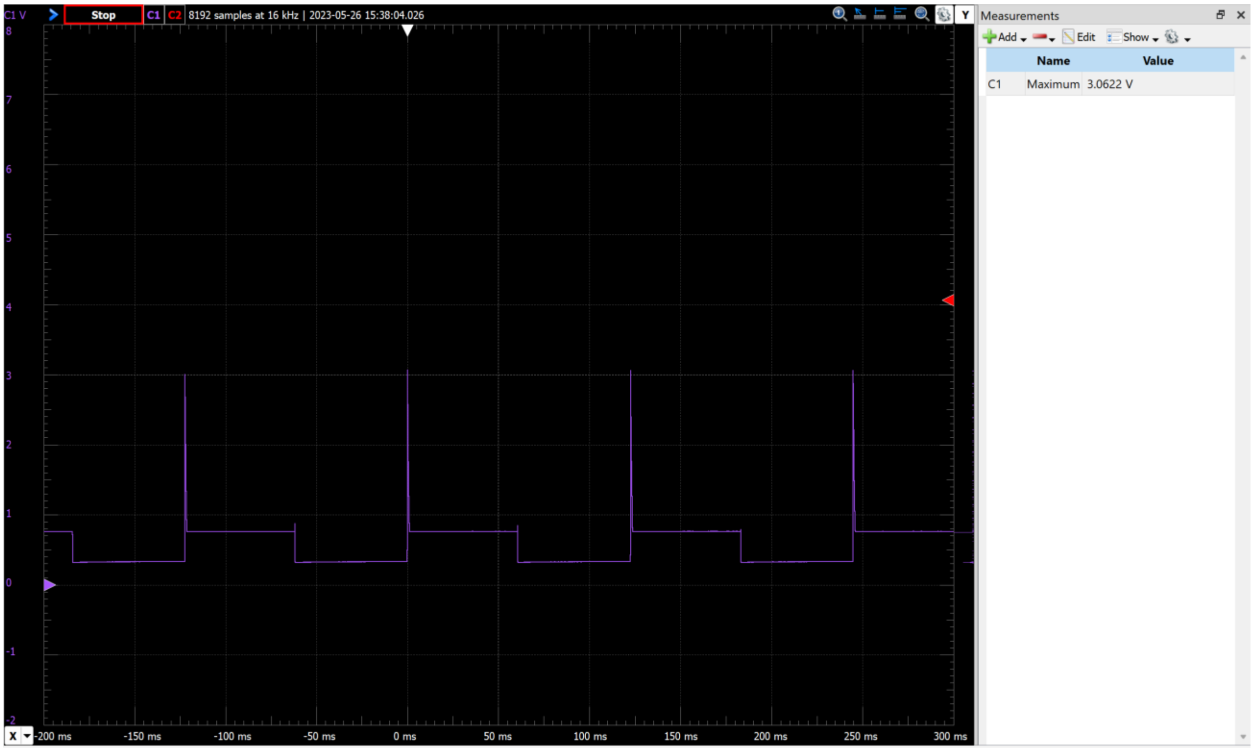


Figure 5. 13 Output Measurement Configuration and Setup of the PCB Prototype.

The measured results obtained from testing the PCB prototype were compared to both the simulation results and the measurements taken from the breadboard setup. This comparison allowed for a comprehensive evaluation of the PCB's performance. The output waveform exhibited a peak voltage of 3 V as showcased in Figure 5. 14, which closely matched the design specifications observed in both the original Cadence simulation and the breadboard implementation. During the testing phase, a discrepancy was observed between the output wave shape obtained from the PCB setup and previous test results from breadboard measurements and the simulated results in Cadence. For instance, we can observe the notable DC offset in Figure 5. 14. Several factors could contribute to this mismatch. Firstly, component tolerances and manufacturing variations can introduce slight variations in the circuit's behavior, impacting the output voltage. Additionally, parasitic capacitances, resistances, and inductances present in the PCB layout can affect the circuit's performance and introduce additional impedance. Furthermore, signal reflections, noise coupling, and improper grounding can contribute to the observed deviation in the output voltage. Lastly, one of the most suspected reasons to why we see such distortion could be due to capacitors exhibiting leakage current. Capacitors, even when fully discharged, may exhibit a small amount of leakage current. This leakage current can

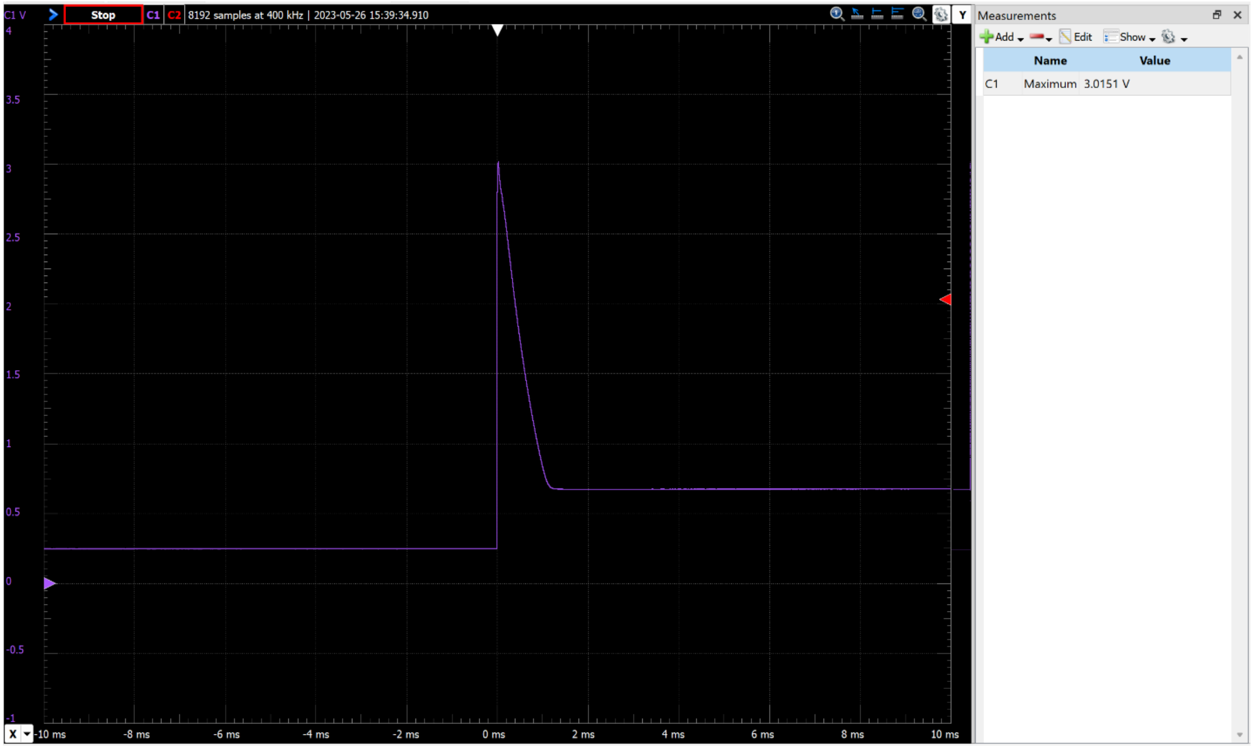


	Name	Value
C1	Maximum	3.0622 V

Figure 5. 14 Output Waveform of the Short Pulse Generated by the PCB Circuit.

cause a gradual discharge over time, preventing the capacitor from reaching a complete zero voltage.

Despite the observed deviation in the output peak voltage, it is noteworthy that the pulse duration and the basic shape of the pulse remained consistent with the expected results. This indicates that the circuit successfully generated the desired periodic short pulses, fulfilling its intended functionality. Further analysis and optimization can be performed to address the output voltage deviation and improve the overall performance of the circuit.



	Name	Value
C1	Maximum	3.0151 V

Figure 5. 15 Zoomed-in View of a Single Output Pulse Across 2k Ω Load Resistor on PCB Prototype

The consistent alignment between the simulation results from Cadence and the measurements obtained from the fabricated PCB as well as the breadboard implementation of the Short Pulse Generator affirms the effectiveness and reliability of the short pulse generator as a physical device. These results validate the accuracy of the design process and serve as strong evidence in support of the proof of concept for the proposed circuit. The successful translation of the circuit design from the simulation environment to the physical PCB further reinforces the feasibility and functionality of the short pulse generator concept.

Overall, the measured results highlight the excellent performance of the PCB prototype and provide confidence in the circuit's potential for practical applications. The successful generation of the desired waveform, the close alignment with the design specifications, and the reliability of the output signal affirm the suitability and effectiveness of the short pulse generator for various electronic applications. The successful testing of the PCB confirms its ability to generate the desired output waveform with stability and reliability. These results validate the effectiveness of the design and provide confidence in the functionality of the integrated circuit. The PCB's performance lays the foundation for further integration and application-specific optimizations in the next phase of development.

In conclusion, the successful implementation of the short pulse generator on the PCB represents a significant milestone in the project. The circuit design, optimization, and thorough testing have demonstrated the feasibility and functionality of the proposed design. With the achievement of generating the desired short pulses with consistent amplitude and duration, the PCB prototype has proven its capability to fulfill the intended purpose. Building upon this achievement, the next chapter will delve into the crucial process of performing IC layout of the short pulse generator using Cadence software. This phase will enable the integration of the circuit into a more compact and integrated form, paving the way for enhanced performance and wider applications.

Chapter 6. LAYOUT AND FABRICATION OF SPG IC

6.1 OVERVIEW OF THE LAYOUT PROCESS

The layout process plays a crucial role in the successful implementation of an integrated circuit (IC) development. In this chapter, we focus on the layout and potential fabrication of the Short Pulse Generator (SPG) IC. The layout phase involves the precise placement and routing of the circuit components on the IC substrate, ensuring optimal performance, signal integrity, and manufacturability.

For the IC layout of the SPG, it's important to note that certain circuit blocks, such as the PWM generation and buck converter circuits observed in previous designs, will not be implemented within the IC. Instead, the IC will solely consist of the Short Pulse Generator itself, with available pins provided for interconnecting with external circuits and other ICs.

Using Cadence and the TSMC 180nm technology, we will design the layout of the SPG IC, ensuring proper placement and interconnection of the circuit components. We will take into consideration the design rules and constraints specific to the 180nm technology, such as minimum feature size, spacing, and layer assignments, to ensure a manufacturable and reliable layout. During the layout process, special attention will be given to the placement of the SPG components, their interconnections, and the routing of signals. Design considerations such as minimizing parasitic capacitance and inductance, optimizing power distribution, and ensuring proper signal isolation will be taken into account to achieve the desired performance of the SPG IC.

By focusing solely on the SPG circuit and providing external pins for connectivity, the IC design offers flexibility and modularity, allowing it to be seamlessly integrated into larger systems and circuits. The layout phase will pave the way for the subsequent fabrication and packaging stages, bringing us closer to a fully functional and standalone Short Pulse Generator IC.

6.2 DESIGN RULES AND CONSTRAINTS

During the layout phase, meticulous attention is given to the design rules and constraints that govern the fabrication process of the integrated circuit (IC). These design rules define the minimum feature sizes, spacing, and other critical parameters that ensure the IC's functionality, performance, and reliability. By adhering to these rules, we can mitigate potential issues such as short circuits, cross-talk, and manufacturing defects.

The minimum feature sizes dictate the smallest dimensions that can be reliably patterned during the fabrication process. These include dimensions such as the width and spacing of metal and polysilicon lines, the size of contact and via holes, and the dimensions of transistor gates and diffusion regions. By following these guidelines, we can ensure that the IC's components are fabricated with precision and consistency.

Spacing rules determine the minimum distance that must be maintained between adjacent features to prevent interference or unintended electrical coupling. These rules account for factors like signal isolation, power distribution, and capacitance control. By adhering to proper spacing guidelines, we can minimize the risk of cross-talk, where signals from neighboring components interfere with each other, and ensure optimal signal integrity throughout the IC.

In addition to feature sizes and spacing, other constraints related to layer assignments, metal stack-up, and the use of specialized components must also be considered. Layer assignments determine the arrangement of different circuit elements on different layers of the IC, allowing for efficient interconnections. Metal stack-up specifies the sequence and properties of metal layers used for interconnecting components and routing signals. Specialized components, such as high-voltage devices or low-noise analog components, may require specific design considerations to ensure their proper functionality and performance.

By meticulously adhering to these design rules and constraints, we can optimize the layout for manufacturability, reliability, and performance. The layout phase plays a crucial role in translating the circuit design into a physical implementation that meets the desired specifications. Through careful consideration of these design rules, we can create an IC layout that maximizes functionality, minimizes potential issues, and ensures the robust operation of the Short Pulse Generator (SPG) IC.

6.3 SHORT PULSE GENERATOR IC LAYOUT AND DESIGN RULE CHECK

The integrated circuit (IC) layout for the Short Pulse Generator (SPG) is displayed in Figure 6. 1. The layout design incorporates several components and interconnections that have been carefully placed to optimize signal integrity, minimize noise, and ensure efficient power distribution. The placement of each component is precisely aligned with the design requirements, and the routing of the metal and polysilicon traces is strategically planned to minimize signal interference. Notably, the layout design also incorporates size considerations, specifically for cost control purposes. As a result, the SPG IC achieves a compact size of only 0.68 mm by 0.68 mm, demonstrating the successful balance between performance and cost-effectiveness. The compact and well-organized layout exemplifies the attention to detail and adherence to best practices in IC design, ensuring reliable and robust performance of the SPG IC.

The layout process for the Short Pulse Generator (SPG) IC followed a systematic approach to ensure accuracy and minimize errors. Each component was brought into the layout individually, allowing for careful placement and alignment. A reference area of 1mm by 1mm was designated, and components were arranged within this area to provide sufficient spacing between each other. This spacing allowed for the routing of thick traces to ensure proper power distribution and minimize signal interference. By following this step-by-step approach, the layout design achieved optimal component positioning and trace routing, contributing to the overall performance and reliability of the SPG IC.

During the layout process, special attention was given to the placement of test pads for post-tapeout testing. The test pads were strategically positioned to closely resemble the original circuit configuration, allowing for easy access and accurate measurements during testing. The left side of the IC was designated for the input power delivery to the SPG input terminals, ensuring efficient power supply to the circuit. The right side was allocated for the output pulse, facilitating convenient probing and analysis of the generated pulses. The top and bottom portions of the layout were dedicated to the PWM signals, providing clear visual indication of the signal flow within the design. This thoughtful arrangement of the test pads enables streamlined testing and enhances the understanding of the circuit's functionality and performance.

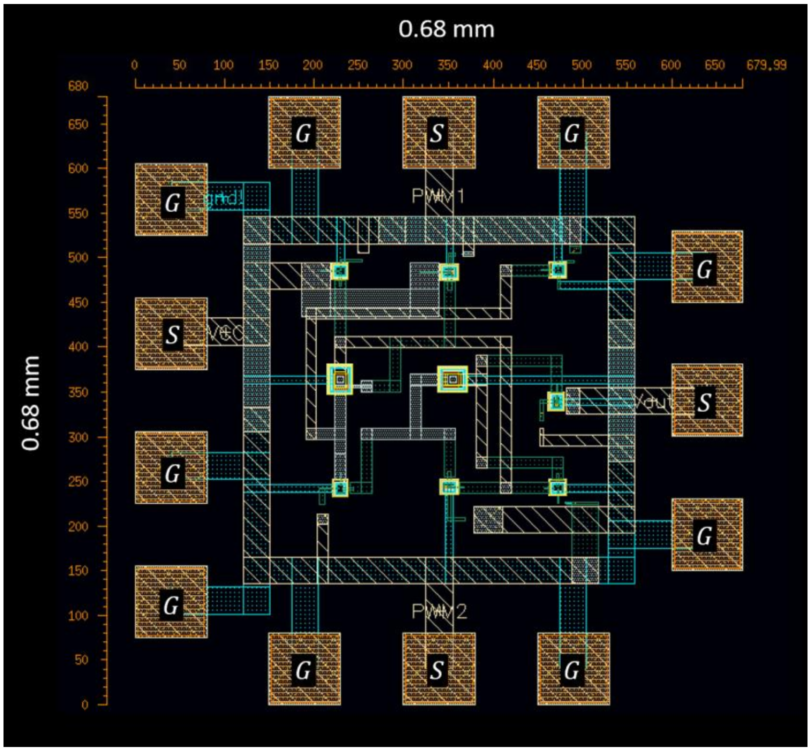


Figure 6. 1 Cadence IC Layout of the Finalized Short Pulse Generator Circuit.

To facilitate the testing of the IC, specific test pad configurations were chosen based on the nature of the signals and the available testing probes. On the left side of the IC, where the DC supply is connected, a test pad configuration of GSGG (Ground, Signal, Ground, Ground) was selected. This configuration aligns with a DC probe's 4 contact pins, allowing for accurate DC testing. The Signal pad in this configuration corresponds to the DC input pad, enabling direct measurement of the input voltage. For the PWM signal inputs located at the top and bottom of the IC respectively as well as the output pulse located on the right side of the IC, a test pad configuration of GSG (Ground, Signal, Ground) was adopted. This configuration matches an RF test probe's 3 contact pins, which are specifically designed for RF signal testing. By using this configuration, the output pulse and PWM signals can be easily probed and analyzed for their waveform characteristics and performance. Figure 6. 2 illustrates the high-frequency probe tip configurations that correspond to the chosen test pad configurations mentioned earlier. These probe tip configurations are designed specifically for high-frequency signal testing and analysis.

On the right side of Figure 6. 2, the probe tip configuration showcases the GSG (Ground, Signal, Ground, Ground) configuration. This configuration aligns with the test pad layout for the DC supply input, allowing for precise measurement and analysis of the DC signal.

On the left side of Figure 6. 2, the probe tip configuration exhibits the GSG (Ground, Signal, Ground) configuration. This configuration matches the test pad layout for the output pulse and PWM signals, enabling accurate probing and examination of the high-frequency signals of 1GHz.

The chosen test pad configuration depicted in Figure 6. 1 holds significant importance due to the expensive nature of high-frequency probes and the potential additional costs associated with customizing them for specific applications. Figure 6. 3 showcases the actual images of high-frequency probes commonly used in real-world applications. These images provide a visual representation of the probes used for RF signal testing and DC testing, as described earlier.

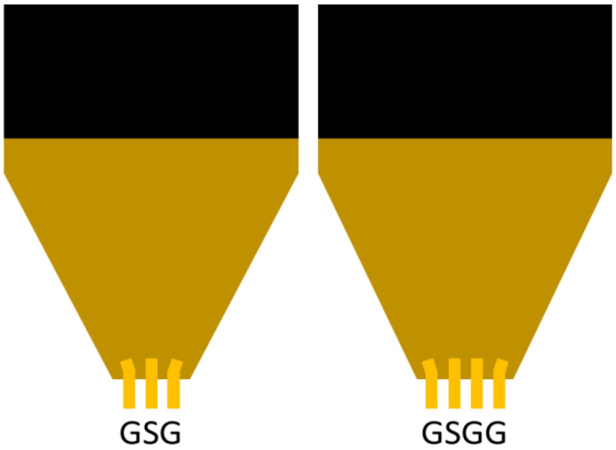


Figure 6. 2 Diagram of the High Frequency Probe Tip Configurations.

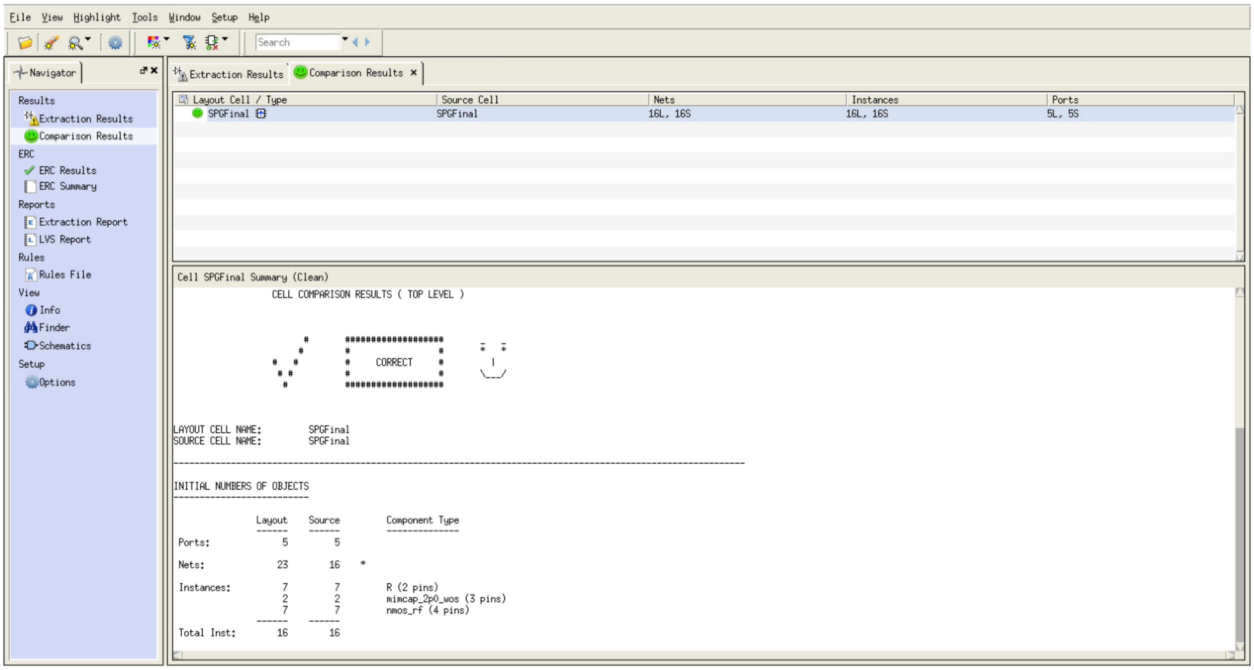
The proper alignment between the test pad configurations and the high-frequency probe tip configurations ensures reliable and efficient testing of the IC's signals all while minimizing the need for costly customizations of high frequency RF test probes. This thoughtful pad configuration ensures compatibility with existing high-frequency probes, reducing both expenses and potential delays in the testing and characterization process. By employing the appropriate probe tip configuration for each test pad, precise measurements and analysis can be performed, leading to a comprehensive understanding of the IC's performance in high-frequency applications.

Figure 6. 3 Examples of High Frequency Test Probes Commonly used in RF Application.

Once the layout was completed, a Layout vs. Schematic (LVS) rule check and Design Rule Check (DRC) were performed was performed. The LVS rule check involved comparing the physical layout of the IC with its corresponding schematic to verify their consistency and correctness. It ensured that the connections and geometries on the layout matched the intended design captured in the schematic. Similarly, the DRC check examined the layout against a set of predefined design rules to identify any violations or errors in the layout. By successfully passing the LVS and DRC checks, we confirmed the accuracy and validity of the layout implementation, ensuring that the physical layout accurately represented the desired circuit functionality while adhering to the specified design rules.

Figure 6. 4 confirms the successful Layout vs. Schematic (LVS) rule check, ensuring accurate representation of the IC layout.   Figure 6. 5 showcases the Design Rule Check (DRC), demonstrating compliance with design rules. These results instill confidence in the accuracy and

reliability of the IC layout, facilitating the next fabrication steps.

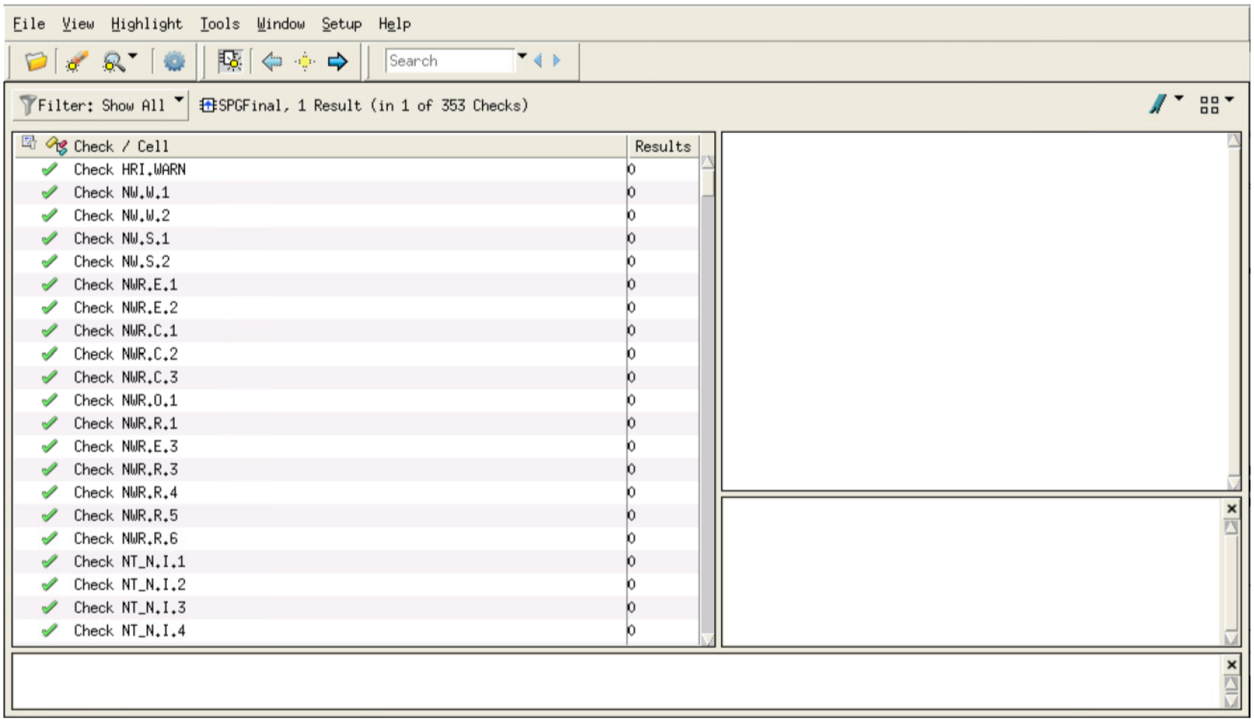


Layout Cell / Type	Source Cell	Nets	Instances	Ports
SPGFinal	SPGFinal	16L, 16S	16L, 16S	5L, 5S

Cell SPGFinal Summary (Clean)

```
                CELL COMPARISON RESULTS ( TOP LEVEL )


                   #      ###################      _   _
                  #       #                 #      *   *
              #  #        #     CORRECT     #        |
               # #        #                 #      \___/
                #         ###################


LAYOUT CELL NAME:         SPGFinal
SOURCE CELL NAME:         SPGFinal

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:              23        16    *

 Instances:          7         7         R (2 pins)
                     2         2         mimcap_2p0_wos (3 pins)
                     7         7         nmos_rf (4 pins)
                ------    ------
 Total Inst:        16        16
```

Figure 6. 4 Results of the Calibre Layout vs. Schematic (LVS) Rule Check.



Check / Cell	Results
✓ Check HRI.WARN	0
✓ Check NW.W.1	0
✓ Check NW.W.2	0
✓ Check NW.S.1	0
✓ Check NW.S.2	0
✓ Check NWR.E.1	0
✓ Check NWR.E.2	0
✓ Check NWR.C.1	0
✓ Check NWR.C.2	0
✓ Check NWR.C.3	0
✓ Check NWR.O.1	0
✓ Check NWR.R.1	0
✓ Check NWR.E.3	0
✓ Check NWR.R.3	0
✓ Check NWR.R.4	0
✓ Check NWR.R.5	0
✓ Check NWR.R.6	0
✓ Check NT_N.I.1	0
✓ Check NT_N.I.2	0
✓ Check NT_N.I.3	0
✓ Check NT_N.I.4	0

Figure 6. 5 Results of the Calibre Design Rule Check (DRC).

The layout phase of the Short Pulse Generator (SPG) IC has been successfully completed, signifying a significant milestone in the design process. With meticulous attention to detail, the components have been precisely placed and routed to optimize signal integrity, minimize noise, and ensure efficient power distribution. The layout design adheres to design rules, constraints, and considerations specific to the SPG IC.

The completion of the layout phase signifies the readiness of the SPG IC for the next stages, which may include fabrication, testing, and validation. The layout serves as a blueprint for the physical realization of the SPG IC, and its accuracy and fidelity play a crucial role in determining the IC's performance and functionality.

The successful completion of the layout phase paves the way for subsequent steps in the IC development process, such as fabrication, where the physical IC is manufactured based on the layout design. These subsequent stages involve techniques such as photolithography, etching, deposition, and interconnection to bring the IC to life. Additionally, packaging methods are employed to ensure the IC's reliability, compatibility, and protection.

While the specific details regarding fabrication steps and subsequent processes may not be covered in this thesis, it is important to acknowledge that the completion of the layout phase signifies an essential progress towards the realization of the Short Pulse Generator IC.

Chapter 7. CONCLUSION AND FUTURE WORK

7.1 SUMMARY OF CONTRIBUTIONS

The project's contributions are summarized as follows:

Design of a 1GHz Short Pulse Generator: The project involved the design of a Short Pulse Generator operating at 1GHz using 180nm CMOS TSMC technology. The design focused on achieving precise pulse generation with a desired amplitude and frequency.

Successful Simulation and Periodic Pulse Generation: Through extensive simulation, the Short Pulse Generator design was validated, and periodic pulses were achieved. The simulation results demonstrated the feasibility of the design and its ability to generate pulses with the desired characteristics.

Minimal Component Design: The Short Pulse Generator design was optimized to utilize minimal components while maintaining the desired functionality. This approach not only simplified the circuit but also reduced cost and complexity.

Breadboard Implementation and Alignment: To validate the design's proof of concept, a breadboard circuit was implemented. The breadboard circuit successfully generated pulses that aligned with the simulation results, verifying the functionality and performance of the design.

Fabrication of PCB Prototype: A PCB prototype was fabricated to further validate the Short Pulse Generator design. The fabricated PCB exhibited performance consistent with both the cadence simulation and the breadboard implementation, confirming the design's effectiveness and reliability.

The Short Pulse Generator design achieved the desired operating frequency of 1GHz using the 180nm CMOS TSMC technology. Through thorough simulation and testing, the design demonstrated its capability to generate periodic short pulses with high precision and accuracy. The successful implementation of the design showcases its feasibility and effectiveness in meeting the project objectives. The utilization of the specific CMOS technology highlights its compatibility with modern fabrication processes and its potential for integration into vast IoT devices. The contributions of this project lay the foundation for further advancements in short pulse generation technology and its applications in various fields. The design achieved periodic pulse generation with a little over 3 volts amplitude. The implementation of the design on a breadboard and the fabrication of a PCB prototype further validated the design's performance and alignment with the simulation. These contributions demonstrate the feasibility and practicality of the Short Pulse Generator concept for various applications.

7.2 CONCLUSIONS AND IMPLICATIONS FOR FUTURE RESEARCH

In conclusion, the design and implementation of the Short Pulse Generator have been successfully accomplished, yielding promising results. The project demonstrated the feasibility of generating periodic short pulses at a frequency of 1GHz using the TSMC 180nm CMOS technology. The design was thoroughly tested and validated through simulation, breadboard prototyping, and PCB fabrication, with consistent alignment between the results. The compact and efficient design of the Short Pulse Generator, along with its minimal component requirements, further contribute to its practicality and potential for integration into various electronic systems.

The successful development of the Short Pulse Generator opens up avenues for further research and exploration. Future studies could focus on enhancing the performance of the generator by optimizing the design for even higher frequencies or investigating alternative technologies to achieve shorter pulse durations with high output voltage. Additionally, exploring the potential applications of the Short Pulse Generator in fields such as telecommunications, signal processing, and high-speed data transmission could lead to new advancements and innovative solutions.

Furthermore, the integration of the Short Pulse Generator with other circuitry or systems could be an area of future research. Investigating the compatibility and interaction of the generator with different components, such as microcontrollers or communication interfaces, would expand its usability and broaden its potential applications.

In conclusion, the successful design and implementation of the Short Pulse Generator lay a solid foundation for future research and development in the field of pulse generation. The project's outcomes contribute to the advancement of pulse generation technology and hold implications for various industries and applications.

7.3 LIMITATION AND RECOMMENDATIONS FOR FUTURE WORK

One limitation of the proposed design is the lower-than-expected output voltage. In an ideal scenario, the Short Pulse Generator should have operated similarly to a Marx generator, where the output voltage is $N * V_{CC}$, where N is the number of capacitors in circuit. With two capacitors representing two stages in the design, the anticipated output voltage should have been 4V, considering the input voltage of 2V. Instead of the anticipated 4V output voltage, the circuit was able to achieve an output voltage of just over 3V for the sub-nanosecond pulses. Although it did not fully align with the principle of the Marx generator, this voltage level still showed promising results within the limitations of the CMOS technology and other potential factors involved in the design.

For future work, addressing the limitations and further enhancing the output voltage is recommended. Exploring alternative circuit topologies, incorporating additional stages or capacitors, and optimizing the design parameters could potentially improve the output voltage performance. Additionally, investigating advanced CMOS technologies with higher voltage handling capabilities or considering alternative technologies altogether might offer new possibilities for achieving the desired output voltage levels.

Furthermore, it is crucial to conduct a thorough analysis of the circuit's performance under different operating conditions and further understand the factors that limit the output voltage. This analysis can guide the refinement of the design and identify opportunities for improvement.

For future work recommendations, it is advisable to integrate a comparator circuit into the proposed design to facilitate high-frequency applications and simplify the integration of the Short Pulse Generator (SPG) into various systems. This comparator circuit would serve the purpose of receiving an input signal from the Voltage Controlled Oscillator (VCO) and transforming it into Pulse Width Modulation (PWM) signals. By incorporating the comparator circuitry, the Short Pulse Generator would no longer rely on external PWM sources, reducing the complexity of the overall system. This would result in easier integration and improved portability of the SPG, making it more versatile for different applications. Furthermore, the addition of the comparator circuit would enable precise and customizable modulation of the output pulses, allowing for fine-tuning of the pulse characteristics to meet specific requirements of high-frequency applications.

In summary, while the proposed Short Pulse Generator design did not fully achieve the anticipated output voltage, it exhibited promising results and laid the foundation for future research. Addressing the limitations, exploring alternative approaches, and conducting in-depth investigations will pave the way for advancements in pulse generation technology and enable the realization of higher output voltage levels in future iterations of the circuit.

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