Circuit Techniques for Optimized Recording of Neural Signals

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Abstract

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Bidirectional Brain Computer Interfaces (BBCIs) are an emerging technology that will provide increased quality of life for patients with various neurological disorders, and will likely someday enhance the human-computer interaction among healthy human populations. The bidirectional nature of these systems mean that many hundreds to thousands of sense and stimulation electrodes must exist simultaneously in human tissue. This complex system creates a number of engineering challenges that are explored in this work, which discusses techniques for accurately and completely recording sensed information from the brain. In this dissertation two primary efforts are discussed that utilize the character of biological signals to build optimal, robust, and efficient systems for recording data from the brain. Data-driven specifications are described for a particular type of neural signal, electrocorticography, which is recorded from electrodes on the brain surface. Based on this work, a novel mixed-signal feedback architecture is exploited to create a robust and efficient neural recording platform, including time-domain multiplexing to reduce the silicon area required

for each electrode recording site, and stimulation artifact suppression, to maintain the integrity of the recorded data in the presence of bidirectional communication with the tissue. Measurement results will demonstrate the utility of these data-driven specifications and the success of this new architecture.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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Chapter 1

INTRODUCTION

The interface between the brain and electronic hardware is often called a Bidirectional Brain Computer Interface (BBCI). BBCIs are systems capable of recording and stimulating brain activity, allowing computers to transmit and receive data to and from tissue simultaneously. These systems have the potential to enable a host of new medical treatments that will benefit patients suffering from a variety of neurological disorders in the short-term. In the longer term, BBCIs will enable dramatically enhanced user-interfaces for human-computer interaction.

There are a number of extant technical challenges to full implementation of BBCI based treatments. Ideally, these systems will be implanted and completely wireless, will be robust to artifacts from full-duplex communication with the brain, will acquire data from tissue in a power and area efficient fashion across thousands of electrodes, and will operate robustly and autonomously for a number of years [1]. Presently, the state-of-the-art is to use rack-mounted instruments in a laboratory setting, including those produced by Tucker Davis Technologies and Blackrock Microsystems. More recently, off-the-shelf implementations that are too large for full implantation, such as the Neurochip, have been demonstrated.

This dissertation explores the implementation of BBCI-compatible recording electronics. Several techniques for improved recording performance are discussed, including techniques for miti-

gating the offset and electrode drift present in the neural tissue, recording the large dynamic range of neural data, suppressing artifacts generated by stimulation, and significantly reducing the per-channel area footprint of recording electronics by time-division multiplexing (TDM). Two separate systems are presented: The first demonstrates a technique for the acquisition of Electrocorticography (ECoG) that delta-encodes the signal input using an analog technique. This work additionally discusses data-driven specifications for ECoG recording systems. The second system is a TDM mixed-signal feedback chip with common-mode and differential-mode artifact suppression that significantly reduces the per-channel area requirements of recording while providing a robust interface with the tissue. Both advance the state-of-the-art in BBCI recording systems.

This work is primarily focused on ECoG recording, because is the primary focus of this work because it is the most promising tissue interface for BBCI [50]. However, many of the observations are applicable to the recording of other biopotentials such as single-neuron acquisition, EEG, and EMG. The mixed-signal technique discussed Chapter 4 is a platform that will operate with both single-neuron recording and ECoG.

Chapter 2 provides an overview of the fundamentals of BBCI signal acquisition and discusses the current state-of-the-art. An overview of electrocorticography is given for context, and important contributions over the past 15 years to recording electronics are discussed in detail. Additionally, a brief review of the existing work on artifact suppression is given.

Chapter 3 discusses an equalization technique that is implemented using an analog delta-encoding technique. It also describes a data-driven approach to determining performance specification for ECoG recording.

Chapter 4 expands on the ideas proposed in Chapter 3 by taking the analog technique for delta-encoding and converting it into a Nyquist-rate mixed-signal feedback system. This improvement enables the use of TDM for significant improvements in area efficiency over the state-of-the-art by storing the mixed-signal feedback data in a register. Additionally, mixed-signal feedback enables the suppression of common-mode and differential-mode artifacts before amplification, which eases the linearity requirements of the amplifier and makes possible the acquisition of biopotentials in the presence of an artifact for integrated circuit (i.e. low supply voltage) approaches to neural signal recording.

Chapter 5 summarizes the contributions of this work and discuss several future improvements to this platform that could be included in future iterations.

Chapter 2

INTEGRATED CIRCUITS FOR THE ACQUISITION OF CORTICAL BIOPOTENTIALS

The development of circuits to observe brain activity has a long history of scholarship that provides important context for the demonstrated systems. Additionally, a basic understanding of the behavior of particular biopotential signals is useful when digesting this work. While the techniques introduced in here are applicable to different types of signals, electrocorticography (ECoG) is the primary test vehicle, so this mode of signal acquisition will be the focus.

In this chapter, a basic history and important technical details of ECoG are discussed, followed by discussions of the state-of-the-art for both ECoG recording platforms (which are sparse in the literature), and a more general discussion of neural recording platforms. Finally, the literature and current state of artifact suppression technology is briefly described.

2.1 Interfacing Electronics with the Brain

While neural activity is often measured by directly observing individual neurons, there is significant information contained in the local field potential (LFP), which is the sum of a large number of neural activities aggregated into slowly moving extracellular potential changes. LFPs can be recorded in different ways. The most invasive technique employs penetrating electrodes, which pierce the pial surface of the cortex and provide the highest spatial resolution. Electroencephalogra-

phy (EEG) relies on measurements from outside the skull on the surface of the skin, and is the least invasive. EEG does not require surgery, but has significantly lower spatial resolution and signal amplitude. ECoG represents an advantageous middle ground between these two extremes. ECoG requires surgery but does not involve the extensive brain trauma and subsequent tissue response produced by penetrating electrodes; the technique can still capture important neural information with the high spatial and temporal resolution critical for BCI research. [33].

However, ECoG instrumentation both in the lab and in the clinic has some critical drawbacks for BCI research. The recording equipment is rack mounted with long tethers connected to the subjects. This measurement setup is problematic because it makes it difficult for the subject to behave naturally, induces motion artifacts, and limits recording times; additionally, long-term transdermal connections commonly cause chronic infection. As a result of these requirements, there is a need for high-density wireless ECoG recording sensor systems. Accordingly, there has been significant research effort into this problem in recent years [12, 17, 39, 48, 65, 66].

2.2 Introduction to Electrocorticography

ECoG has been a powerful tool for studying the function of the brain since the 1950s. It was developed by neurosurgeons Wilder Penfield and Herbert Jasper, who used electrical recordings from the surface of the brain to help locate sources of epileptic seizures and deliver electrical stimulation to map cortical function. This allowed surgeons to minimize the area of resection for epilepsy treatment [43]. In current practice, ECoG arrays are applied as a strip or grid of metal electrode pads (see Figure 2.1). ECoG arrays are used extensively in rodents and non-human

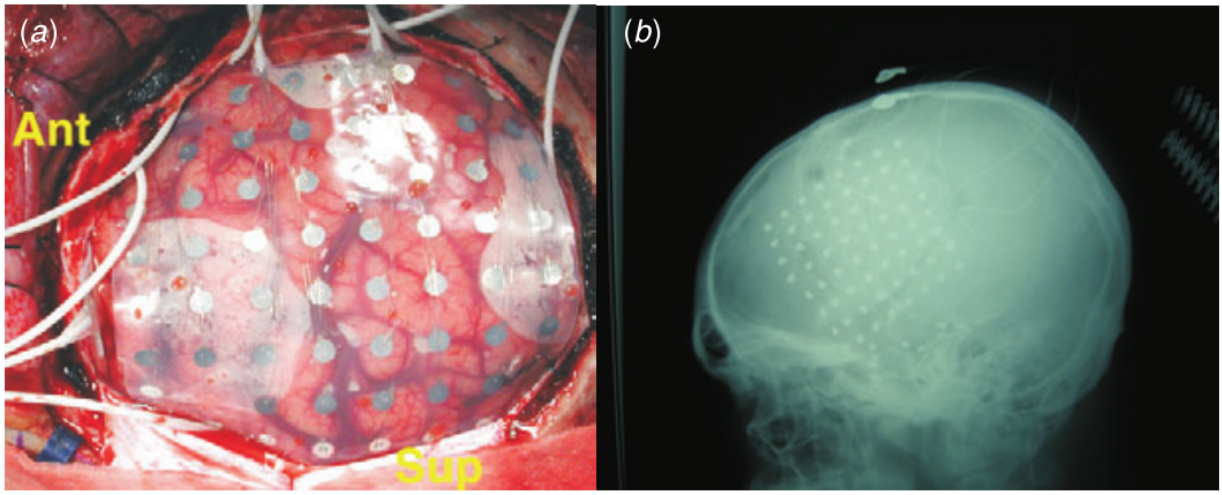


Figure 2.1: An ECoG electrode grid implanted in human subject [26]. (a) shows a photograph of the implanted array. (b) is an x-ray of the patient's skull.

primates; in humans it has demonstrated utility in neurophysiology and BCI research [49].

2.2.1 The Nature of ECoG Signals

Electrical activity recorded from the surface of the brain reflects a complex summation of activity from the neural tissue below the electrode. The spatial and temporal organization of neurons underneath a contact both contribute to the acquired signal. Modeling work [28] and non-human primate research [13, 40] conclude that much of the ECoG signal comes from the underlying, axially oriented pyramidal cell dipoles. Between 100-10,000 cells as far as 0.5 mm away contribute to the signal acquired by an electrode [3, 41]. Additional modeling shows that the primary contribution to a distant LFP comes not only from the intrinsic synaptic potentials of a population of cells but also the phase synchrony of these potentials.

A number of oscillatory components within specific frequency ranges (bands) have been described in electrocorticography. These bands reflect anatomical and functional characteristics of cortical and subcortical networks and their interactions, and they are correlated with a variety of cognitive processes and behaviors. Starting with the lowest frequency, researchers have distinguished the following bands: δ (1-4 Hz), ϑ (4-8 Hz), α (8-13 Hz), β (15-30 Hz), γ (30-60 Hz), and high-γ ($>$60 Hz). These rhythms have been tied to cortical activity during language production and understanding [8, 9], vision [21], movement [34], and movement planning [10], among others.

Figure 3.1 shows the time and frequency domain behavior of ECoG recorded from a quietly sitting macaque monkey. Its amplitude clearly shows a characteristic attenuation as a function of frequency. There is typically an increase in power spectral density (PSD) in the beta band (the 'β-bump'), and a rapid attenuation at higher frequencies, including γ and high-γ. The β band is thought to arise from the near-synchronous oscillatory firing of widespread populations of neurons, and higher frequency bands are more directly related to spatially-localized multi-unit cortical activity [11, 34].

2.2.2 Utility of ECoG in BCI and Neuroscience

High-fidelity ECoG recordings have been used for a wide range of clinical applications and investigations of basic research principles. ECoG has been validated as both as a tool for investigating new phenomena in the brain as well as a viable control platform for a variety of output technologies. ECoG signals have been recorded, decoded, and/or volitionally modulated to control cursors on computer screens [50], move robotic arms for paralyzed patients [64], and decode individual

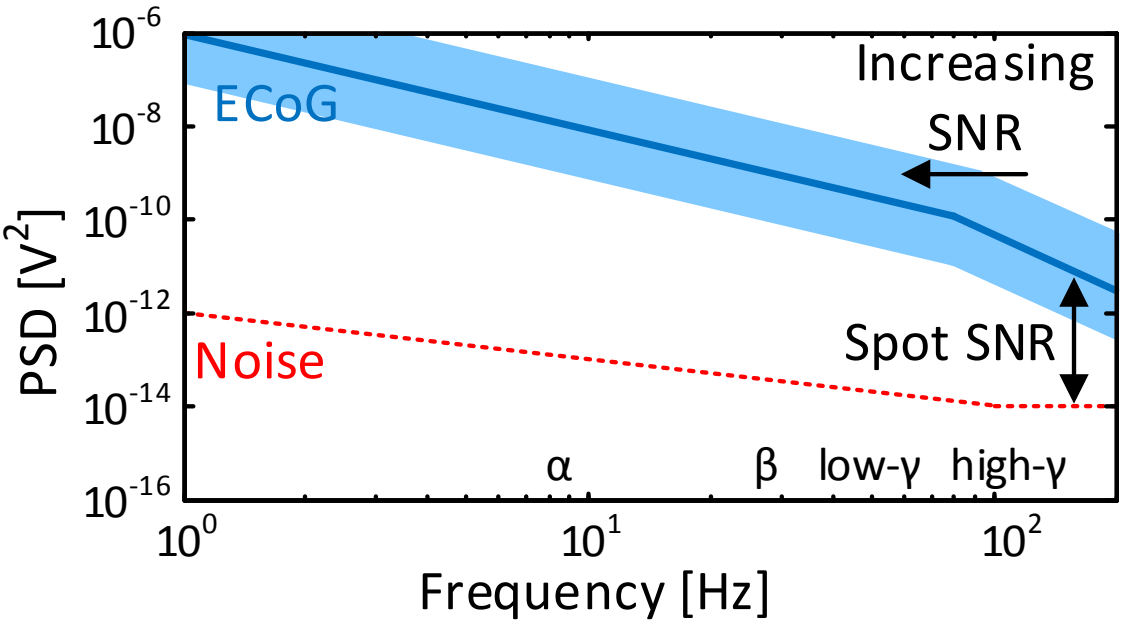


Figure 2.2: Typical PSD of ECoG and representative noise PSD of a low-noise amplifier.

finger movements [25]. For the treatment of epilepsy, ECoG activity can be used to detect pre-ictal activity and deliver electrical stimulation to preempt and stop intractable seizures [57]. In most of these applications, high-frequency components of ECoG (γ and high-γ), have consistently provided the most relevant features. These small and highly-localized signals are the most difficult to record using current technology.

2.2.3 Future Needs for Brain Computer Interfaces

Long-term recording of ECoG has been validated with a variety of clinical uses; however, one of the primary concerns with current technology is the longevity of wired systems. Electrode design and encapsulation techniques have been developed that minimize the risk of infection around implanted wires. New electrode materials and geometries have been shown to take advantage of

the body's natural healing and defense responses to ensure that implanted systems are stable long term without signal degradation [51]. The development of power-efficient electronics for scalable, high-density, and wireless ECoG recording remains an open technical challenge.

2.3 Biopotential Recording

The literature on integrated ECoG recording arrays is limited when compared to integrated single neuron recording systems, so both will be presented here. Many of the advancements for neural recording systems, especially as they apply to the acquisition of local field potentials, are directly applicable to ECoG recording.

2.3.1 Recording Requirements

As scientists realized the potential for stable implantation that is critical for BBCI [49], ECoG has received more attention from the engineering community. The driving force behind this attention is the development of fully implantable ECoG arrays.

As the desire for higher spatial resolution for BBCI applications increases, severe area constraints have become an important engineering problem. Additionally, power consumption remains an important metric, especially as the number of channels increases, but in BBCI systems this constraint is less severe due to the much larger power requirements of stimulation. A primary driver of area usage and design difficulties is the large DC offset and electrode drift present in the electrode-tissue interface, which can be hundreds of millivolts in certain circumstances. Additionally, the signal spectrum is colored, which creates a large dynamic range ($\approx$ 80dB) that must be recorded.

Noise performance is critical at the bottom end of this dynamic range, as signals, particularly for ECoG, can be as small as 1μV. Finally, in BBCI systems, another important criteria is that the system can simultaneously stimulate and record; this requires mitigation of artifacts created by the stimulator, which are analogous to transmitter interference in a transceiver.

Common-mode rejection ratio (CMRR) is also an important consideration for biopotential amplifiers. Interfering signals in the body, power mains noise (50-60Hz), and other low frequency interferers can obfuscate the small, low frequency signals of interest, but a good CMRR in concert with carefully balanced inputs can mitigate these problems. Power supply rejection ratio (PSRR) is also significant, particularly for wireless solutions, as on-chip regulation typically has 10s of microvolts of residual noise.

The primary driving Figure of Merit (FOM) for biopotential amplifiers has for decades been the Noise Efficiency Factor (NEF) [56]:

$$\mathrm{NEF} = \mathrm{V_{rms,in}}\sqrt{\frac{2\mathrm{I_{tot}}}{\pi \mathrm{V_t} \cdot 4\mathrm{kT} \cdot \mathrm{BW}}} \tag{2.1}$$

where $\mathrm{V_{rms,in}}$ is the input referred RMS noise voltage, $\mathrm{I_{tot}}$ is the total current dissipated in the circuit, $\mathrm{V_t}$ is the thermal voltage, k is Boltzmann's Constant, T is temperature, and BW is the bandwidth of the amplifier. This equation is fundamentally related to how efficiently an amplifier uses bias current to improve noise performance, and is 1 for a single-ended bipolar transistor without flicker noise. However, in more recent years as amplifier systems have become more complex, this expression continues to be used and incorporates non-physical relationships including those introduced by data converters. This typically does not completely decouple the FOM from

its physical significance, because in well designed systems the data converter power consumption and contribution to noise is usually quite small.

More recently, a secondary expression has gained some acceptance where the power consumption, rather than current consumption, is considered. This is called the Power Efficiency Factor (PEF) [38]:

$$\mathrm{PEF} = \mathrm{NEF}^2 \mathrm{V_{DD}} \tag{2.2}$$

where $\mathrm{V_{DD}}$ is the power supply of the amplifier. In many cases, this power supply is linearly regulated from a higher supply voltage, so care must be taken when considering which metric is more applicable for a given implementation.

2.3.2 Existing ECoG and Neural Recording Amplifiers

Integrated circuits have been used to assist in the acquisition of neural signals since Wise introduced the integrated buffer amplifier in to neural probe shanks in 1971 [61]. More recent important early work toward integrating instrumentation amplifiers for cortical biopotential acquisition is demonstrated in [20]. This work is designed for penetrating electrodes to capture single-neuron spike activity as well as local field potentials (LFPs). The authors AC-couple the amplifier inputs to suppress DC offset and utilize pseudoresistors to create a low-frequency high-pass corner ($<$1Hz) (Figure 2.3). The primary drawback is that pseudoresistance is highly process dependent, but this is a amplifier topology that is still in frequent use today.

An early example of ECoG-specific CMOS-compatible work is shown in Figure 2.4 [12]. In

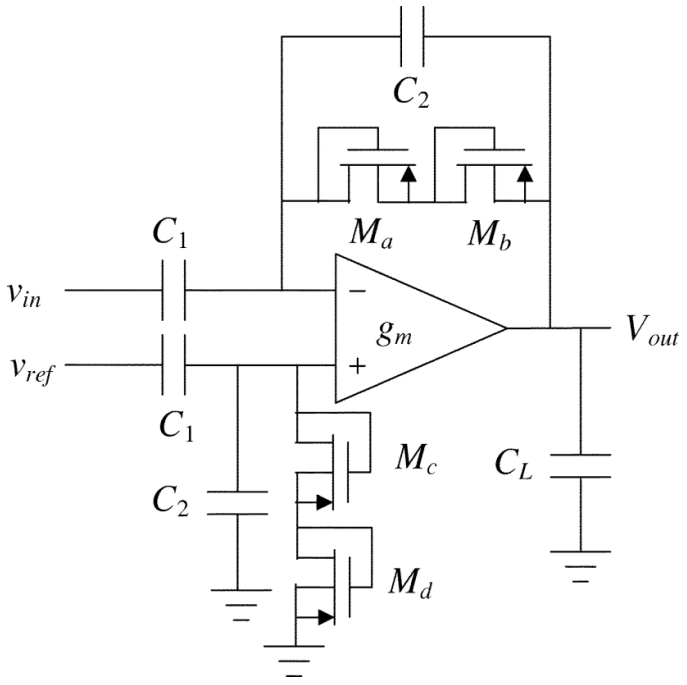


Figure 2.3: AC-coupled instrumentation amplifier for biopotential acquisition using pseudoresistors to set a low-frequency high-pass corner [20].

this work, chopper stabilization [14] is used to eliminate low-frequency flicker noise and other correlated interferers including low-frequency drift of the electrode potential. It also has beneficial effects for the CMRR. Chopper stabilization is a commonly used technique for both non-invasive and invasive biopotential recording [60, 62, 65]. This technique is now commonly used in ECoG amplifiers.

Additional improvements to NEF are achieved using current reuse, or inverter-based topologies (Figure 2.5), where both NMOS and PMOS transistors are used as gain devices [23]. These topologies eliminate load devices in favor of a complementary pair of active devices, so that all devices contributing significant noise to the amplifier are also contributing gain. These amplifiers

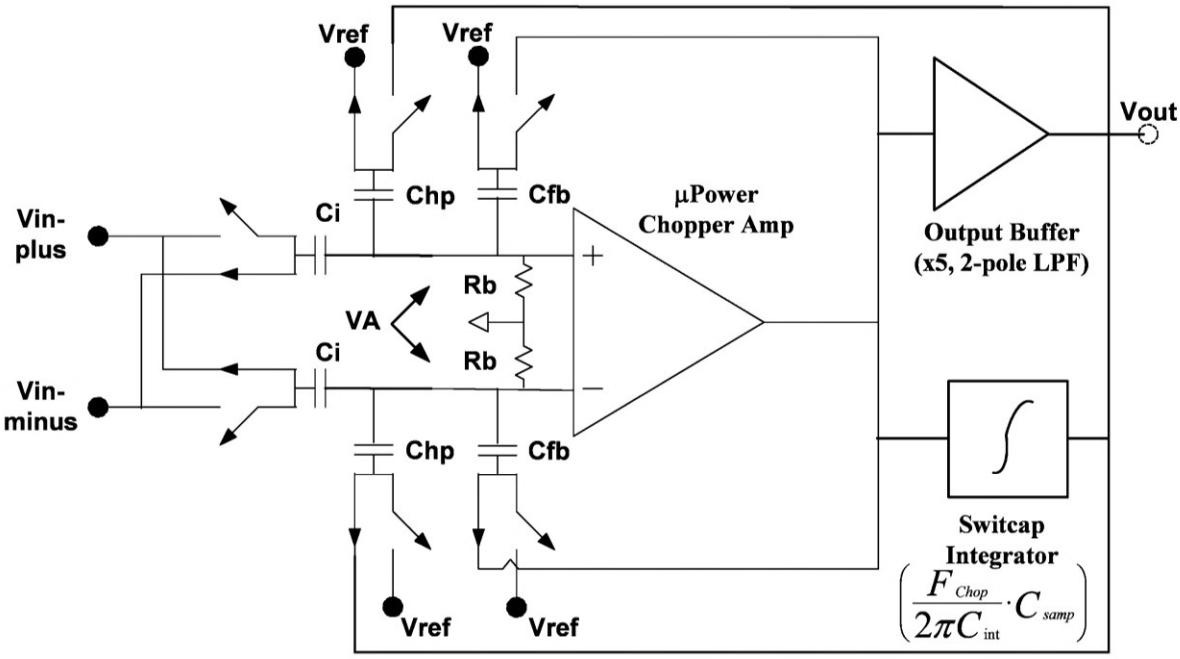


Figure 2.4: Chopper stabilized LFP/ECoG recording amplifier. [12].

are frequently also operated in an open-loop configuration, to further improve noise performance.

Mixed-signal feedback can also be implemented to suppress offset and increase the amplifier dynamic range, as is demonstrated in [39]. In this implementation, an oversampled DAC feeds back the output of a digital IIR low-pass filter, giving the overall system a high-pass response and suppressing the DC offset. Similar work was done by the same authors in [38] to separate LFPs from spikes and deal with dynamic range issues introduced by these signals.

2.4 Artifact Suppression

Another important area of work in high-fidelity biopotential acquisition, especially for BBCI, is the development of artifact suppression techniques. Large stimulation voltages ($>$10V) are required

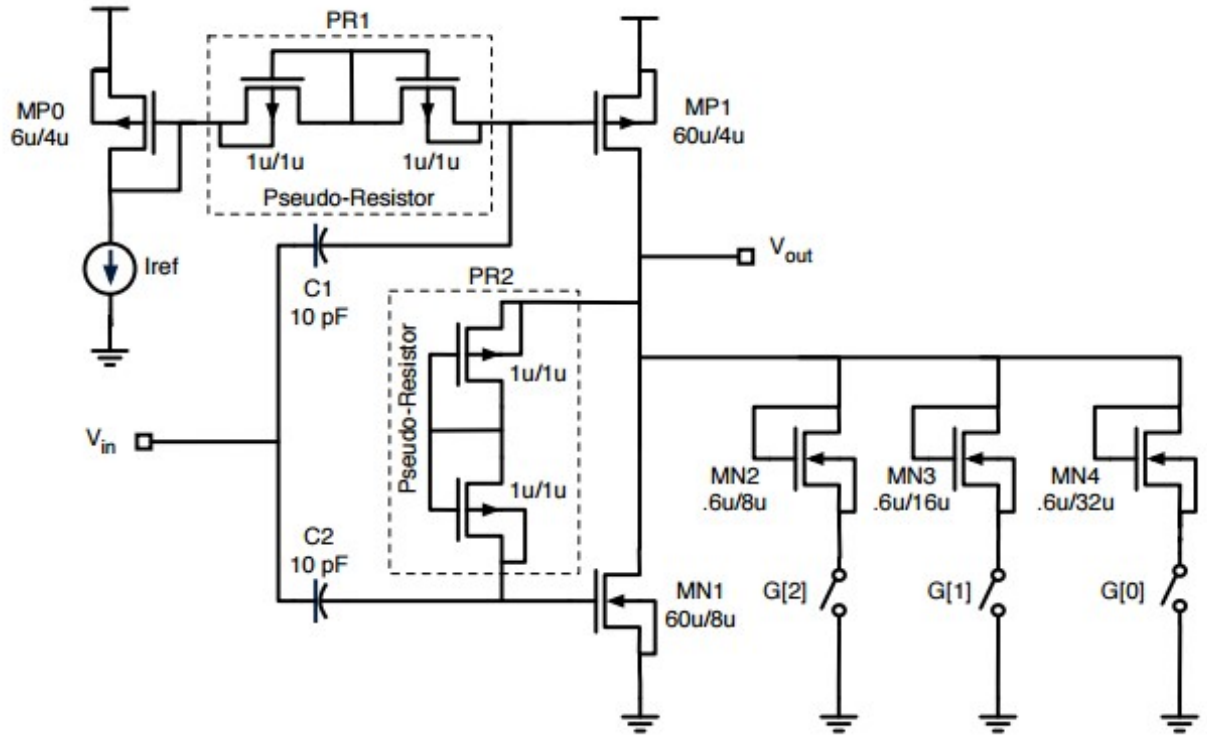


Figure 2.5: Open loop current-reuse amplifier implemented to optimize noise performance. This amplifier is also single-ended, which further improves noise performance while losing the advantages of differential operation. [23].

due to the high-impedance nature of existing electrode technology. These stimulation voltages, once through the electrode tissue interface, propagate easily through the low-impedance of the body. Combined with the required sensitivity of biopotential amplifiers, these signals can completely saturate an amplifier rendering the recorded signal unusable, particularly in CMOS implementations.

Conventional rack-mounted recording platforms typically have significantly more dynamic range, which allowed for artifact suppression using post-processing techniques such as template

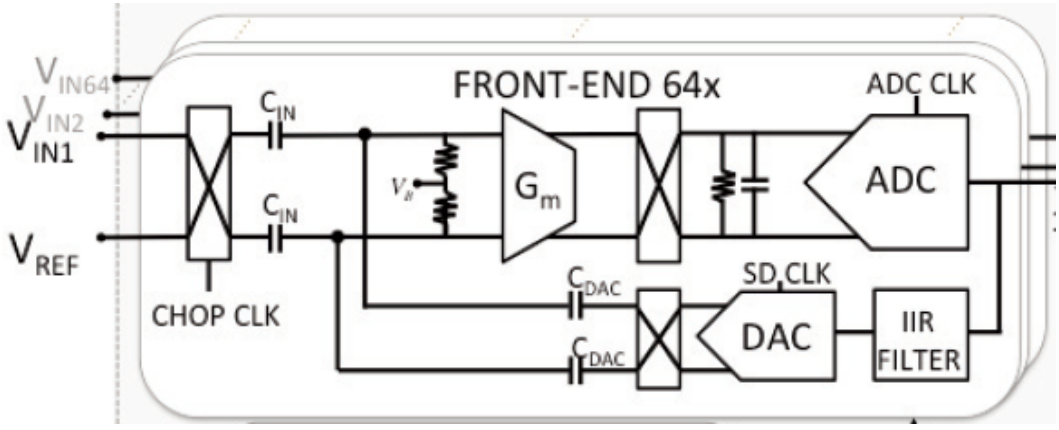


Figure 2.6: ECoG amplifier with mixed-signal feedback using an oversampled TDC-based ADC and oversampled DAC [39].

subtraction [22, 27]. However, CMOS implementations have much lower dynamic range capabilities due to limitations from supply voltages, so alternative methods must be used.

Many existing CMOS implementations of bidirectional systems use simple methods such as blanking [2] the input signal during an artifact to avoid saturating the amplifier inputs. Blanking is particularly useful in closed-loop feedback amplifiers, where these amplifiers can settle with time constants >1 second. However, in BBCI use-cases, stimulation pulses will be frequent and come from a number of stimulating electrodes at different latencies. As a result, blanking the electronics for every stimulation artifact is not possible. Instead, future systems must actively suppress stimulation artifacts so that the fidelity of the underlying neural signal is preserved.

Some early efforts focus on increasing the dynamic range of CMOS amplifiers. In one example, [4], the authors increase the dynamic range of the amplifier to 20mV. An additional technique [24] demonstrates using a time-to-digital conversion technique (TDC) to make use of the large dynamic range available in the time domain. However, time-domain electronics are highly nonlinear, so

considerable effort is expended mitigating this nonlinearity in this approach.

The most promising approach is the use of front-end suppression techniques. A very early example of this is shown in [31], where the authors suppress the differential artifacts using a DAC at the amplifier inputs. This is a very promising technique that we were also working on when this paper was published. A schematic of the system is shown in Figure 2.7.

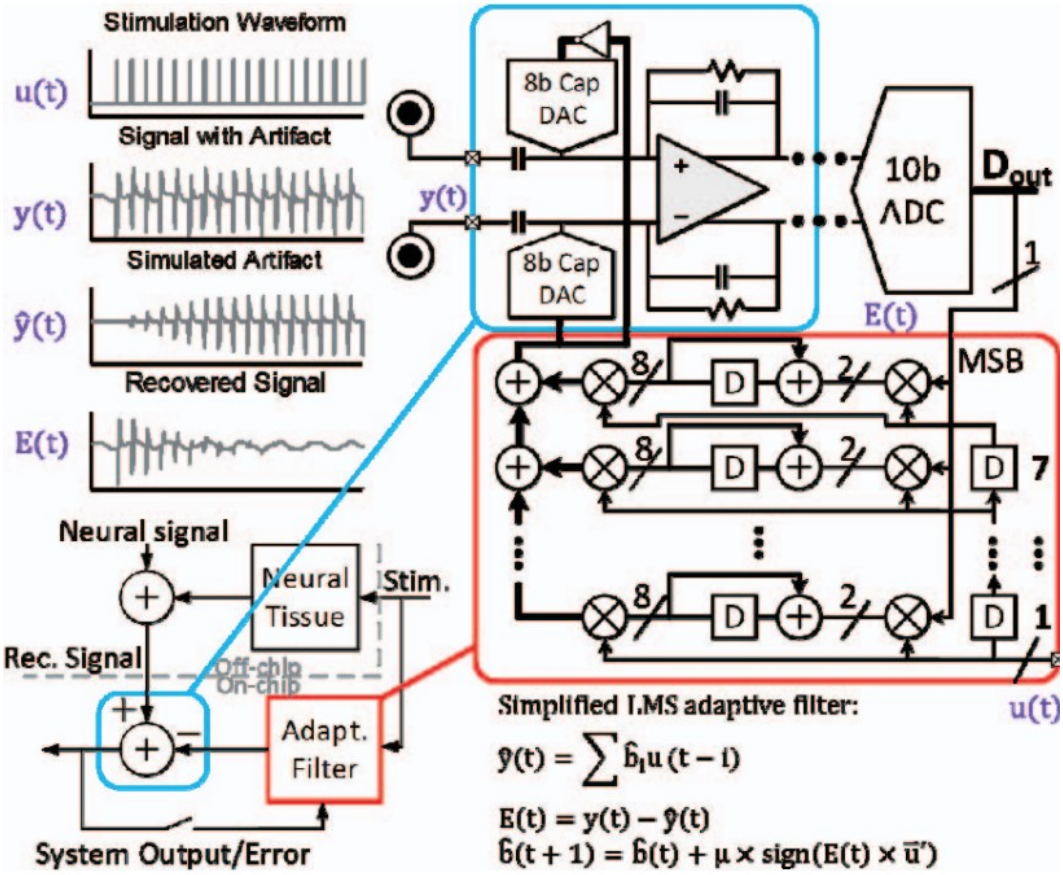


Figure 2.7: Concept and schematic of front-end differential artifact suppression using a DAC at the amplifier inputs. [31].

Chapter 3

EXPLOITING ELECTROCORTICOGRAPHIC SPECTRAL CHARACTERISTICS FOR OPTIMIZED SIGNAL CHAIN DESIGN

3.1 Introduction

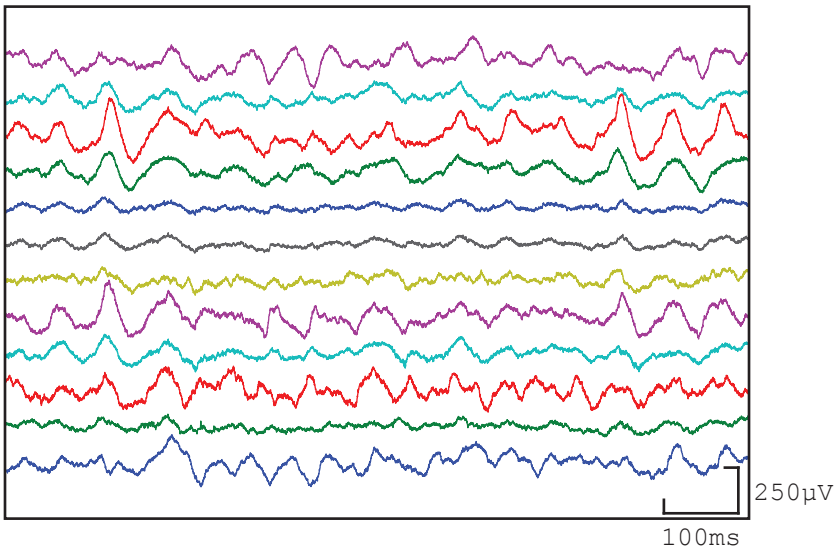
Most existing recording systems are designed to be agnostic to unique ECoG signal characteristics, primarily, the inversely proportional relationship between signal power and frequency. In this chapter we discuss two ways to exploit the spectral characteristics of ECoG. The first is a new target for ECoG amplifier noise specifications based on the unique spectral characteristics and use cases for ECoG data. This reduces power consumption and system complexity by more accurately reflecting the requirements of ECoG recording. The second is to differentiate the input ECoG signal before digitization in order to reduce the dynamic range requirements of the ADC. We demonstrate a prototype utilizing these approaches with prerecorded and real-time in-vivo recordings.

Section 3.2 discusses some properties of ECoG that can be exploited for optimal front-end design. Section 3.3 describes the prototype developed to test these ideas, and Section 3.4 describes the prototype test results. Section 3.5 shows the prototype recording in-vivo, and finally Section 3.6 draws conclusions from this work.

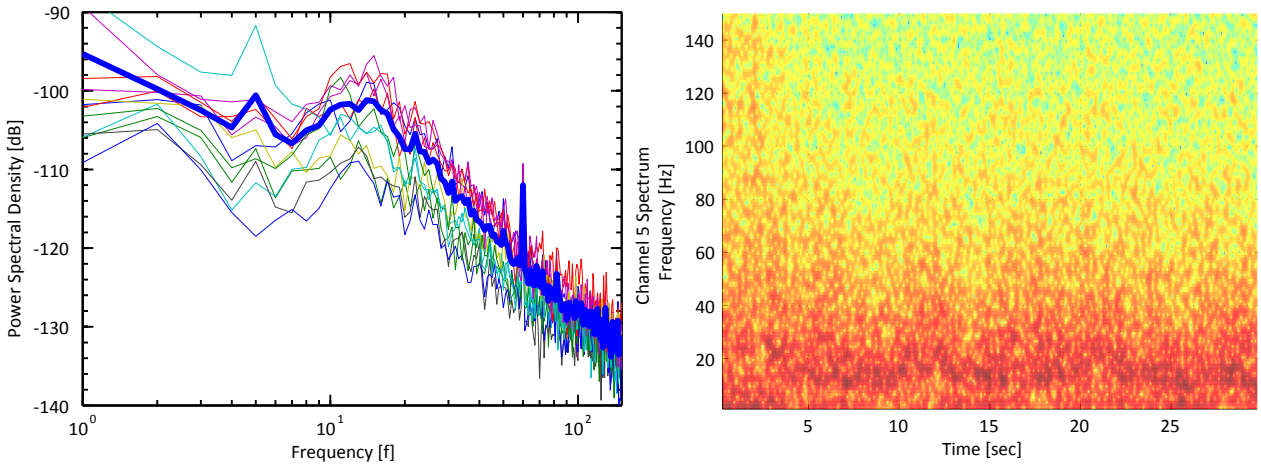
3.2 Exploiting the ECoG PSD for Efficient Design

The unique frequency characteristics of ECoG and the reliance on the PSD for analysis allow for more efficient design than is possible with a conventional analog front end (AFE). As seen in Figure 3.1 and described in Figure 2.2, the ECoG power spectrum does not have consistent amplitude throughout the range of frequencies. Instead, it attenuates with frequency. It has been proposed that the power spectrum decays approximately with $1/f^2$ below 80 Hz and at $1/f^4$ above [32]. We will show that an understanding of this frequency coloring in the signal spectrum has important implications that drive design decision.

We can improve circuit performance without loss in signal fidelity by taking advantage of the ECoG PSD. First, it is reasonable to neglect 1/f noise under certain conditions that will be discussed in the next section. Second, the use of an integrated noise specification typically results in overdesign. We propose an alternate spot noise target. This will reduce the amplifier power requirements by easing the amplifier noise requirements. Finally, we will show that utilizing an analog-to-digital converter (ADC) in the conventional sense is inefficient, as the quantization noise has a mostly constant PSD across frequency. A very high-resolution ADC is required to digitize the full signal range, but this can be reduced by addressing the differences between the ECoG PSD and the PSD of the ADC quantization noise. These optimizations, made possible by examining the ECoG PSD, can offer significant power savings and circuit complexity reduction over conventional methods.



(a)



(b) (c)

Figure 3.1: Characteristics of recorded ECoG from an awake macaque monkey. (a) One second of ECoG data. (b) PSD of 30 seconds of ECoG data. The bold line corresponds to the PSD mean of 12 channels. (c) Spectrogram corresponding to one channel of (b).

3.2.1 Determining Requirements for SNR

The ECoG data in Figure 3.1 shows a strong frequency dependence, as discussed in Chapter 2. These spectral characteristics drive analysis of ECoG signals into the frequency domain, or into sub-banded time domain slices for each of the identified ECoG bands. Consequently, a more suitable approach for determining ECoG noise requirements is to use a bandwidth appropriate to the analysis, instead of the noise integrated over the entire ECoG spectrum. In the case of spectrograms, as in Figure 3.1c, this is typically on the order of a 1 Hz bandwidth. For time domain analysis, the uppermost band (high-γ) has the smallest amplitude, and will drive noise requirements in the time-domain context.

Consider the model described in [32] and shown in Figure 2.2. As more signal is integrated below the maximum frequency of interest, the SNR will always increase because the ratio of signal to noise increases as frequency decreases. As a result, the worst case noise requirements are at the maximum in-band frequency. Integrating the noise through the high-γ band will still be a less stringent requirement than achieving adequate SNR to properly record the highest frequency bin of the spectrogram. As a result, the spot noise at this frequency should drive the noise specifications beyond those required for time-domain analysis.

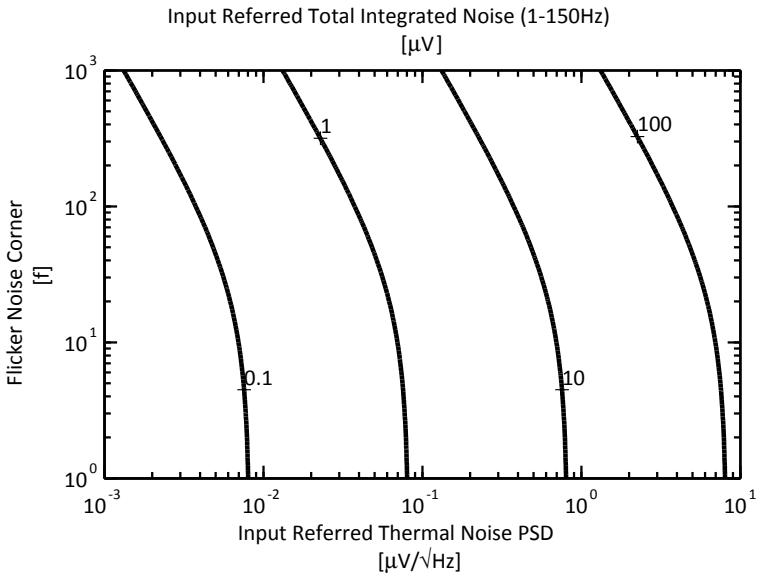
Figure 3.2 compares the traditional integrated noise metric (from 1-150 Hz) with the spot noise metric (at 150 Hz). This analysis can be generalized to other maximum frequency choices. The contour plots show the dependence of input-referred total integrated noise and spot noise, respectively, on the input-referred thermal noise and noise corner. It is clear in Figure 3.2a that for integrated noise, flicker noise has a significant impact. However, in Figure 3.2b, flicker noise remains

insignificant to approximately a 100 Hz noise corner. An integrated noise specification forces the design to account for flicker noise that may not affect performance for this application.

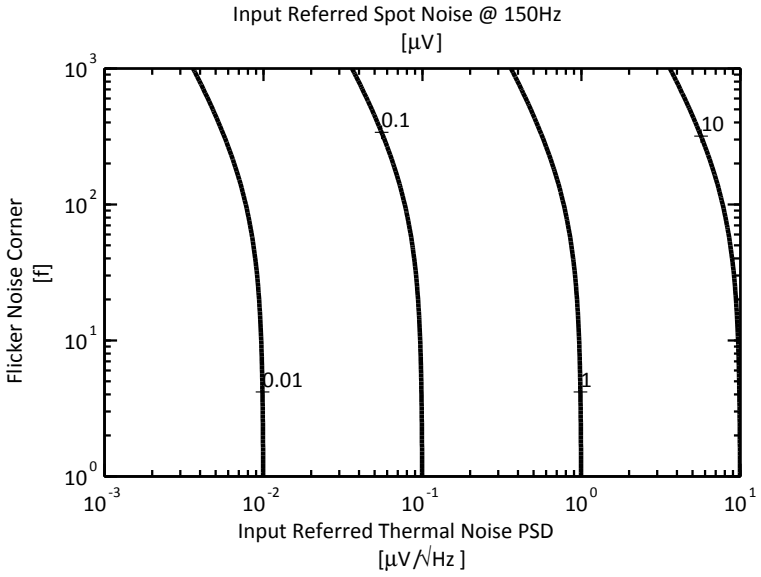
Secondly, compare the required input referred thermal noise for a 1 μV integrated noise target with a 100 nV/$\sqrt{\text{Hz}}$ spot noise target. A 1 μV integrated noise target requires approximately 85 nV/$\sqrt{\text{Hz}}$ of thermal noise PSD, assuming ideal elimination of flicker noise. The 100 nV$\sqrt{\text{Hz}}$ spot noise target requires 100 nV$\sqrt{\text{Hz}}$ thermal noise floor. A 15% reduction in noise results in a 27% reduction in power because of the quadratic relationship between noise and bias current. More importantly, ECoG research is beginning to look at higher bandwidths (e.g. 500 Hz-1 kHz) [39], and at 500 Hz the required thermal noise floor is 45 nV/$\sqrt{\text{Hz}}$. Because ECoG amplifiers are noise limited, a spot noise specification of 100 nV$\sqrt{\text{Hz}}$ could result in a four-fold decrease in power consumption. Whether the use of spot noise results in significant power savings or not, the spot noise metric is more closely coupled to the actual noise requirements for this use case than a broadband integrated noise specification, and will result in a better understanding of the system requirements.

To assess whether targeting a spot noise of 100 nV$\sqrt{\text{Hz}}$ is sufficient to accurately record real data and view it in the time domain, consider Figure 3.3. In this figure the SNR of the average PSD shown in Figure 3.1b versus the designed amplifier noise specifications is shown. Note that the scale of the amplitudes in Figure 3.1b are considerably smaller than those seen in other work (e.g. [32]), so this represents a fairly conservative analysis. It also suggests that the spot noise target should be conservatively designed to accomodate a variety of recording scenarios, which is why we have chosen 100 nV$\sqrt{\text{Hz}}$.

Figure 3.3a shows that the SNR is quite high for a 100 nV$\sqrt{\text{Hz}}$ thermal noise floor with a

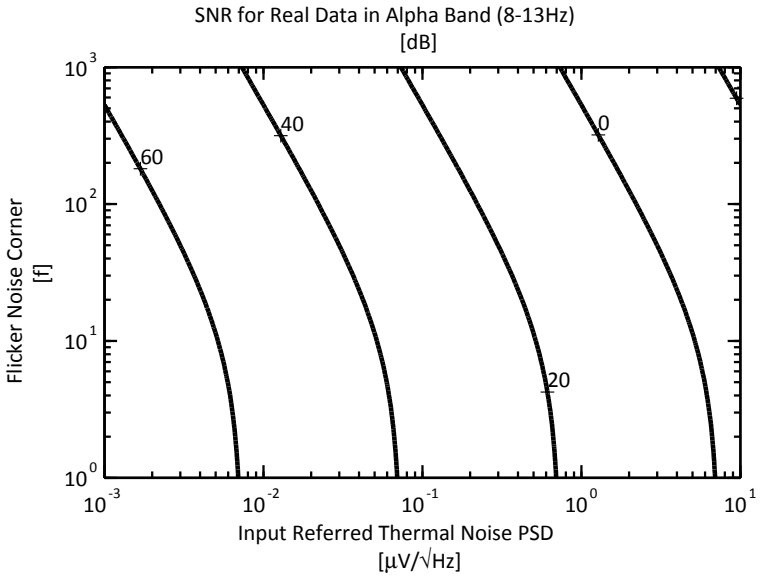


(a) Integrated noise plotted against both thermal and flicker noise

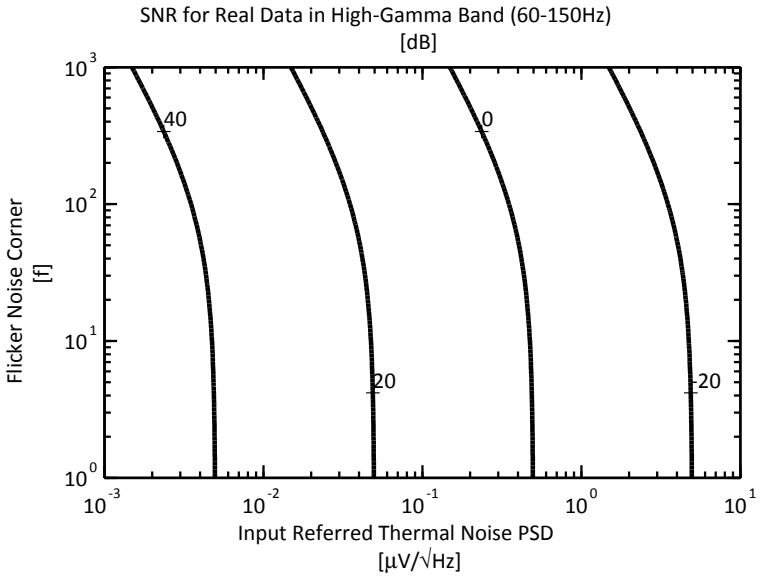


(b) Spot noise plotted against both thermal and flicker noise

Figure 3.2: Contour plots comparing the difference in required noise performance when utilizing a total integrated noise target from 1-150 Hz versus targeting the spot noise at 150 Hz.



(a) SNR in the α band of prerecorded data from Figure 3.1b



(b) SNR in the high-γ band of prerecorded data from Figure 3.1b

Figure 3.3: SNR for a designed level of noise performance in the α and high-γ bands. The contour plots clearly show that the SNR is quite high in the α band for any choice that achieves good SNR in the high-γ band. The plots also show that the SNR in the high-γ band is relatively insensitive to the noise corner as long as that noise corner is not significantly higher than the band itself.

100 Hz noise corner. There is considerable dependence on the flicker noise, but the SNR is still sufficient (> 30 dB). Figure 3.3b shows that even these relatively small signals still have more than 10 dB of SNR under the designed conditions. As a point of reference, the mean PSD of Figure 3.1b at 150 Hz is 260 nV/$\sqrt{\text{Hz}}$ RMS, giving a spot SNR of 8.3 dB at 150 Hz.

Given this new spot noise target, the traditional noise efficiency factor (NEF) expression [56] must be altered slightly. The resulting expression is shown in Equation 3.1.

$$\text{Spot NEF} = V_{n,spot}\sqrt{\frac{2I_{tot}}{\pi \cdot V_T \cdot 4kT}} \tag{3.1}$$

The results of this analysis are twofold. First, there is no need to try to suppress 1/f noise if the maximum-frequency SNR is sufficient. Second, overall noise requirements for the amplifier can be relaxed to reduce amplifier power consumption. In this paper we show a prototype that validates both of these assumptions.

3.2.2 Optimizing ADC Resolution Requirements

With ECoG PSD characterized by $1/f^2$ and $1/f^4$ attenuation with frequency, the SNR at the maximum frequency is much smaller than the total SNR required across frequencies. This leads to inflated ADC requirements to accommodate the entire signal dynamic range simultaneously. A highly calibrated variable-gain amplifier (VGA) can somewhat mitigate these requirements by ensuring that the entire ADC range is used for a given channel (eliminating the variable amplitude from electrode to electrode). A VGA combined with a tunable high-pass filter can also be used, but in this case the entire ECoG spectrum is not simultaneously available; this significantly decreases

the utility for BCI.

The full dynamic range of the ADC can be utilized at all frequencies by reshaping the waveform into a signal with a more consistent amplitude across the frequency spectrum. One simple way to equalize the signal spectrum is to perform differentiation. This, to first-order, makes the resulting spectrum white because the signal is primarily proportional to $1/f^2$. After differentiation and digitization, the signal can be recovered with low overhead using a digital integrator. Accordingly, the primary component of signal amplitude variation, the variation across frequency, is dramatically reduced by equalizing this spectrum before digitization. Differentiation of a signal decreases the amplitude of the signal by an additional 20 dB for each decade of frequency range. Over the range from 1-150 Hz, this reduces the low frequency content by 43dB with respect to the high-frequency signal. The high-frequency signal is more than 43dB below the low-frequency signal before differentiation, so this ideally results in a 43 dB reduction in dynamic range, which corresponds to more than 6 bits of ADC resolution.

The idea of preemphasizing parts of the ECoG spectrum is not new. In [37] the authors create a pre-emphasis at high-γ signal frequencies. This technique has a particular corner frequency that must be precisely calibrated for proper reconstruction. In another case, [66], the authors sub-band the data at different frequencies before digitization, which also reduces the total signal dynamic range but precludes native viewing the entire ECoG band. In [7], the authors describe a ”folding” technique, where the signal is reset to a default DC value when it increases beyond a threshold. This technique requires significant post-processing to recover the original signal, but can reduce the ADC resolution requirement.

In [59] the authors show the efficacy of implementing a high-pass corner at 100 Hz using discrete devices, and proves that highly reliable reconstruction is possible. This technique is also utilized in [63] for a penetrating electrode recording system using a switch capacitor filter to implement the high-pass corner. By performing this operation in the first stage, the authors reduce the size of the required input capacitors by relaxing the high-pass corner requirements of the system. This can significantly reduce the chip area of an amplifier channel, as these amplifiers are typically limited by the size of the AC coupling capacitors at their input. However, when the spectrum shaping is implemented in the first stage, the amplifier's flicker noise becomes the dominant contributor to SNR degradation at low frequencies.

3.2.3 Proposed Signal Chain

One way of implementing this analog-differentiator, digital-integrator scheme is shown in Figure 3.4. It utilizes the Low-Noise Amplifier (LNA) then VGA neural amplifier scheme first proposed in [20] and widely used since, but replaces the VGA with an analog high-pass filter with a corner above the maximum frequency desired, which serves as a differentiator. By placing the spectrum shaping circuit in the second stage, we reduce the noise requirements of the first stage and can apply the ideas presented in Section 3.2.1. After the ADC, data is recovered by a digital accumulator, recovering a very accurate version of the original signal with relaxed ADC requirements and without the need for VGA calibration.

To understand how quantization affects the overall SNR of the system when it is shaped as described in Figure 3.4, consider Figure 3.5. This figure shows the output-referred SNR of the

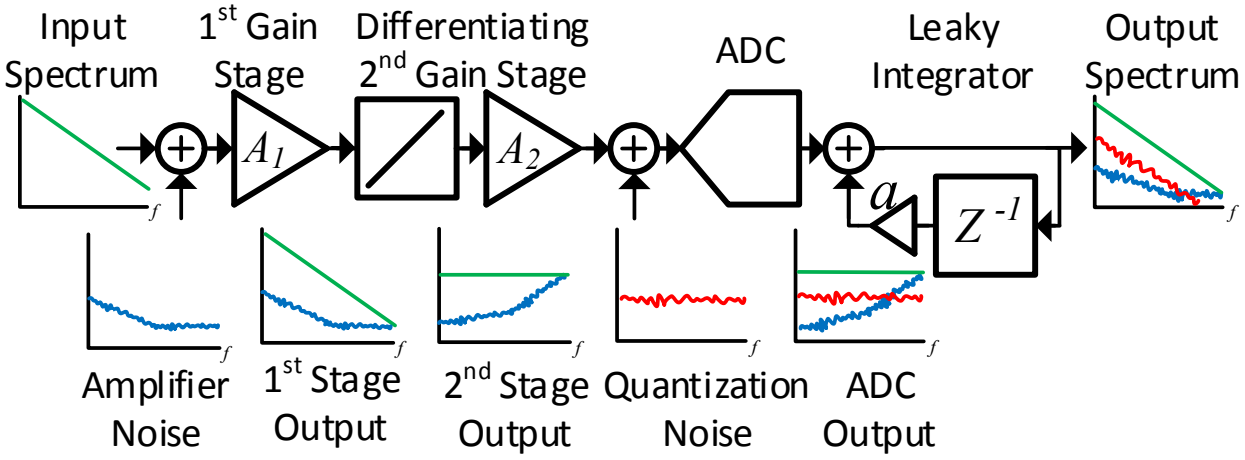


Figure 3.4: Conceptual block diagram of signal chain.

average PSD in Figure 3.1b versus frequency for electrical and quantization noise over several different quantization levels. ECoG signals satisfy all of Bennett's Criteria [45], and therefore the quantization noise can be considered to be random, which results in the familiar quantization noise PSD $V^2 = V_{LSB}^2/12f_s$. This is analyzed along with thermal noise to produce Figure 3.5, which shows that for $N < 7$, the system begins to significantly degrade the signal. The most significant degradation occurs at low frequency. The precise quantization level needed will depend on the spectral content of the channel. This data has a much smaller amplitude than the model in [32] and weakens at low frequency, as can be seen in Figure 3.1b, with relatively low power in the δ and ϑ bands. Thus, the SNR is lower at very low frequencies while our model would have predicted a constant SNR. As previously stated, this suggests that there is considerable variability in ECoG signals, and design should be conservative.

Using this technique, we have eliminated the need for a VGA and have reduced the required

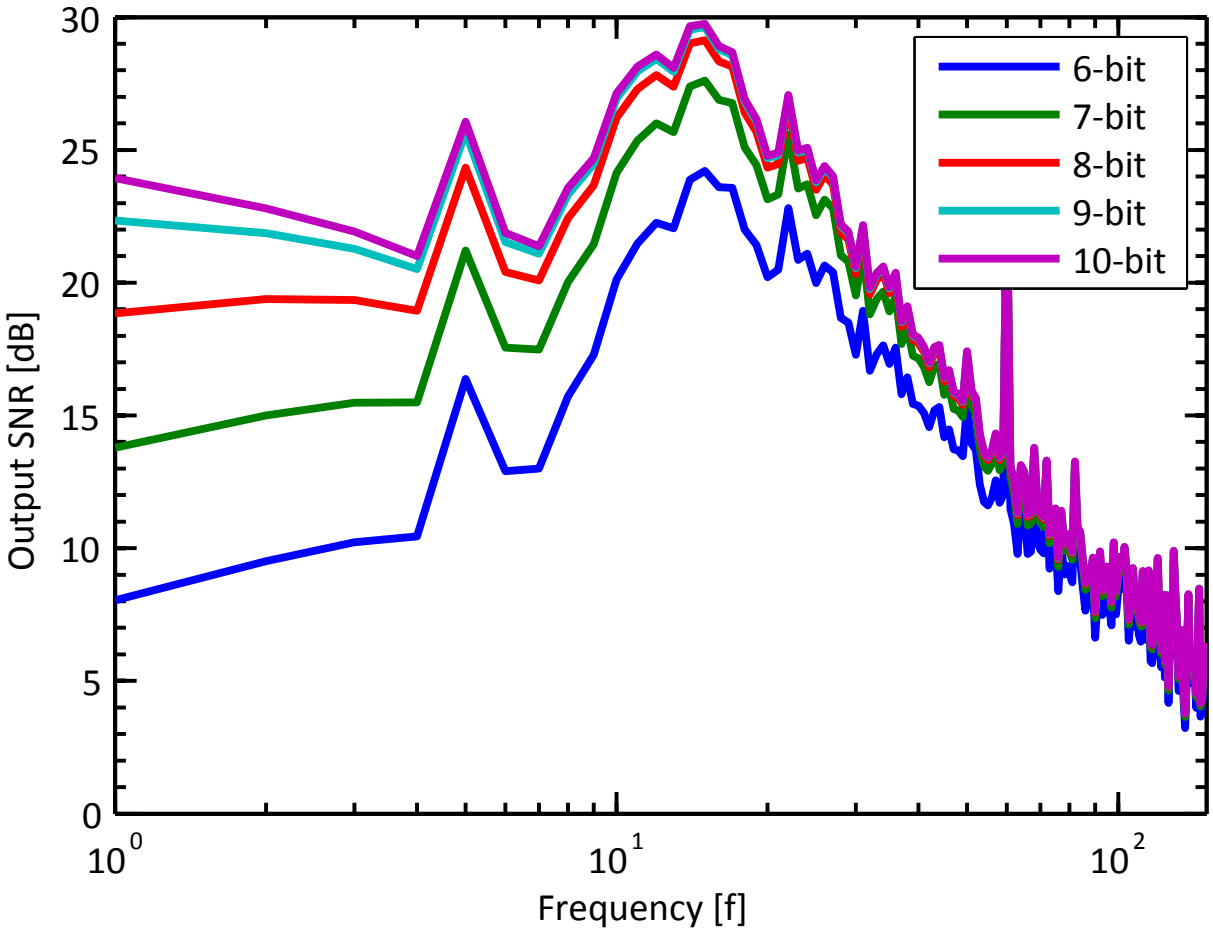


Figure 3.5: Plot of output referred SNR versus both physical and quantization noise for the average PSD shown in Figure 3.1b. The quantization noise was calculated using V_{ref} = 1 V and f_s = 500 Hz. At N = 6, the signal begins to degrade significantly.

ADC resolution. Eliminating the VGA still yields significant ADC resolution savings because the VGA addresses variability in signal amplitude between channels and across time, while the differentiator addresses the variability in signal amplitude from low-to-high frequencies.

Elimination of the VGA is critical for large-scale ECoG systems, because individually tuning hundreds of amplifier channels is an intractable problem. While this system does not directly address the channel to channel variation of the signal that makes a VGA necessary, it does reduce the dynamic range of an individual channel. This makes the need for precisely controlled dynamic range less important, which allows for a greater tolerance in second stage gain. This allows designers to remove the VGA without having to significantly overdesign dynamic range. Our implementation, as shown conceptually in Figure 3.4 does not have a VGA.

Automatic gain control (AGC) is an alternative method for eliminating individual VGA tuning [42, 47], but it requires complicated digital control schemes that consume additional power. Converting a gain stage into a differentiating stage does not nominally consume any additional power. In reality, implementing both an AGC scheme and this differentiation scheme would minimize the required ADC resolution. These schemes are complimentary if the resulting reduction in ADC power from the AGC scheme is larger than the power consumed by the AGC scheme itself.

3.3 Prototype Amplifier Design

Figure 3.6 shows the constructed front-end block diagram. The first amplifier stage is an LNA that uses capacitive feedback to AC couple the signal with pseudoresistors to create a high-pass corner below 1 Hz. C_1 and C_2 were sized to produce 40 dB of gain in the pass band. The amplifier

was compensated to produce a low-pass pole at 250 Hz to ease the antialiasing filter requirements, making the overall stage have a bandpass response.

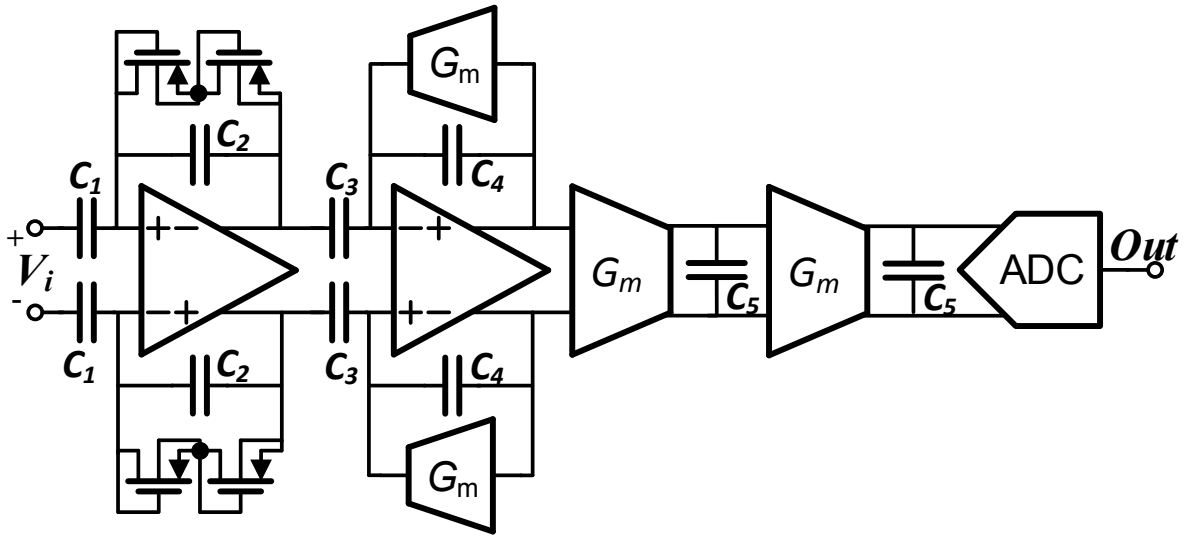


Figure 3.6: Block diagram of prototype ECoG signal chain with off-chip ADC. C_1 = 20 pF, C_2 = 200 fF, C_3 = 10 pF, C_4 = 100 fF, C_5 = 400 fF. All are metal-insulator-metal (MIM) capacitors with a density of 2 fF/μm^2.

The second stage performs the differentation of the input signal. The stage is similar to the first, but instead of pseudoresistors it utilizes G_m cells to create a high-pass corner at 200 Hz. This filter serves as a differentiator for all signals in the passband of the first stage. Once again, the stage is compensated to place a pole at 250 Hz to ease antialiasing requirements.

After amplification and conditioning the signal is additionally antialiased in two successive G_mC filters and is then ready to be digitized with an ADC.

The transistor-level schematic of the first- and second-stage operational amplifiers is shown in Figure 3.7. The topology is identical for both stages, but they differ in bias conditions and transistor geometry because of their different performance requirements. The topology utilizes tail current

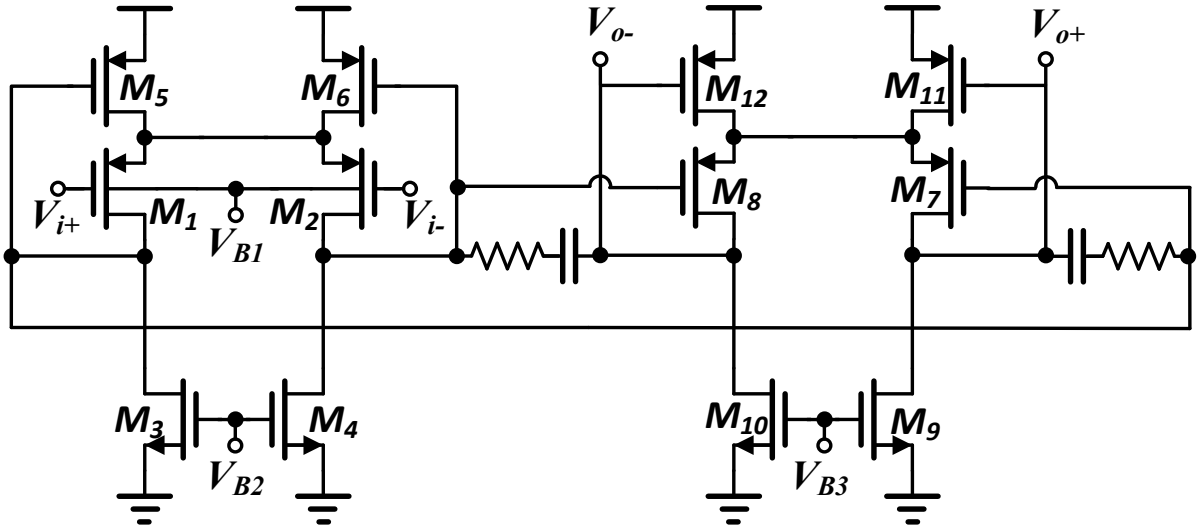


Figure 3.7: Opamp topology for both amplifier stages.

source-based common-mode feedback for both stages, making both the first and second stage of the op-amp self-biased and fully differential. While less linear than resistive sensing of the common-mode, this scheme is practically realizable for ultra-low-power amplifiers and does not require an external common-mode feedback voltage. Additionally, using this self-biased scheme, there is no additional current consumed for the comparison of common-mode voltage. The amplifier operates from a supply voltage of 1 V, but all devices are 2.5 V I/O devices to reduce gate leakage for these large and low-bias-current devices.

In the first stage, the bias current and device geometry are increased in the M_1, M_2 legs for improved 1/f and thermal noise performance. This stage has a forward biased bulk voltage V_{B1} to reduce the required V_{ov} of these devices. The amplifiers are compensated for stability using standard lead compensation.

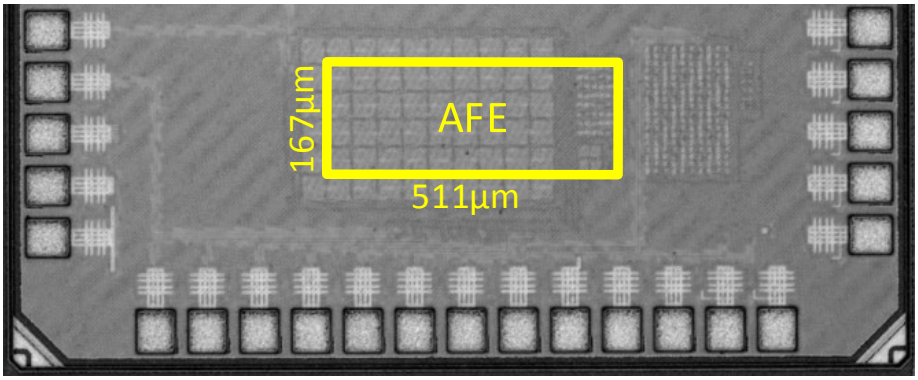
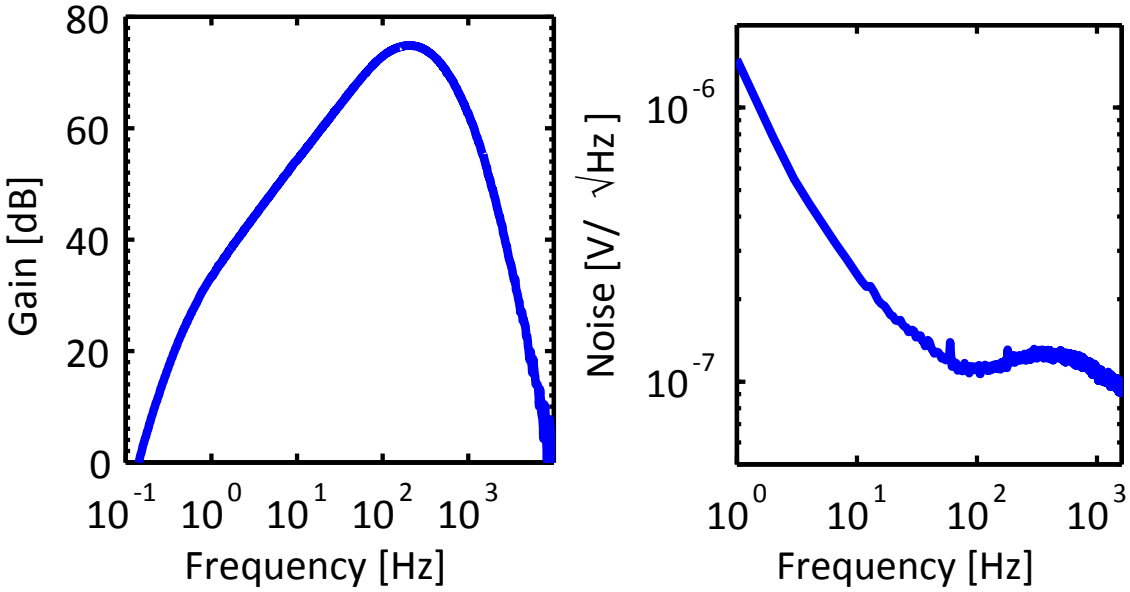
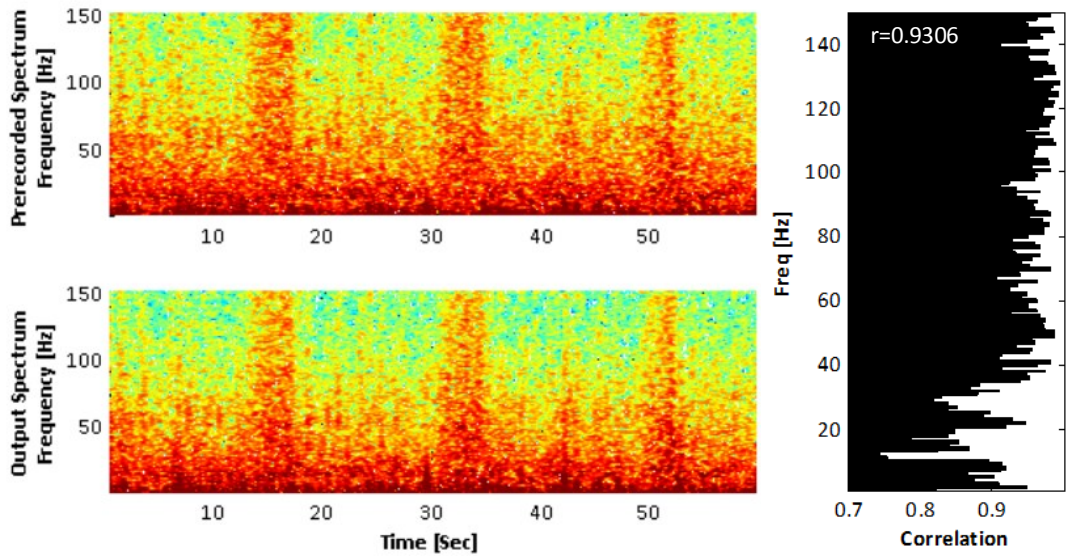


Figure 3.8: Fabricated die photo.

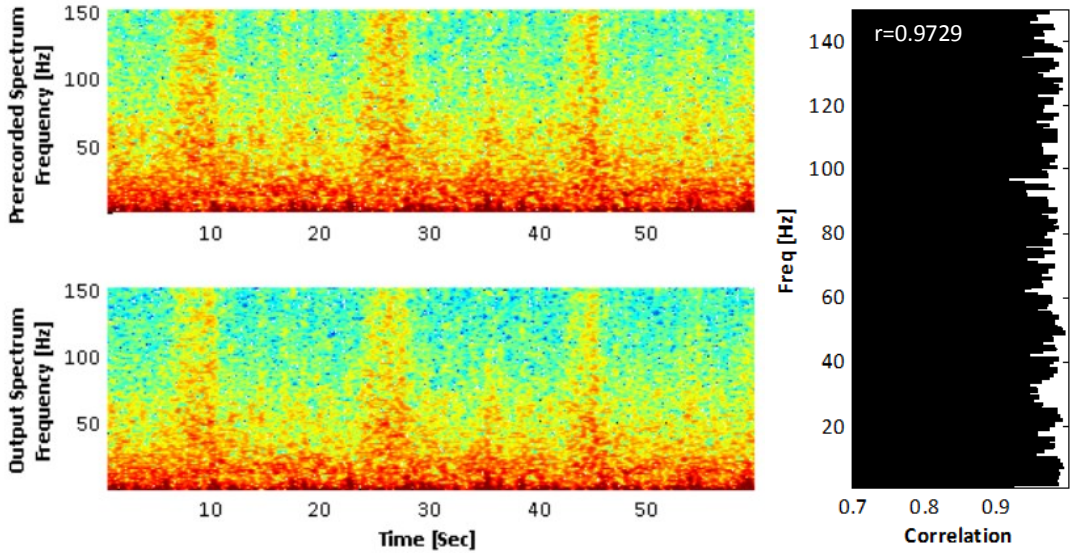


(a) (b)

Figure 3.9: Measured AFE magnitude response and input-referred noise PSD.



(a)



(b)

Figure 3.10: Comparison of prerecorded data to same data after processing with AFE. (a) represents data in original form, while (b) represents data from the same channel with doubled signal power that verifies the low-frequency saturation hypothesis.

Table 3.1: Performance comparison of prototype with other ECoG AFEs

	JSSC'07 [12]	JSSC'08 [65]	TCAS'11 [66]	ESSCIRC'13 [17]	ISSCC'14 [39]	This Work
Power per channel (μW)	2	6.9	3.2	36.3[3]	2.3[3]	1.08
Spot Noise[1] ($nV/\sqrt{Hz}$)	100	55	80	—	58	112
Spot NEF[1]	3.88	3.21	5.56	—	4.83	4.52
Spot PEF[1,2]	27.10	30.91	37.10	—	11.66	20.43
CMRR (dB)	100	120	80	87	—	82
PSRR (dB)	—	—	60	90	—	68
AFE Bandwidth (Hz)	0.005-180	0.5-100	0.4-200	—	1-500	0.5-150
ADC Resolution	—	11-bit[4]	8-bit[5]	16-bit[6]	15-bit	7-bit[7]
Area (mm^2/ch)	0.8	0.45	0.4[8]	—	0.025	0.085
VGA	Yes	Yes	Yes	No	No	No
Supply Voltage (V)	1.8	3	1.2	3.3	0.5	1
Technology	0.8 μm	0.5 μm	130 nm	0.6 μm	65 nm	65 nm

[1] At 150 Hz, [65] is at 100 Hz [2] $(NEF)^2 \cdot V_{DD}$ [38] [3] Includes bias circuits [4] EEG amplifier
[5] Sub-bands signal to reduce resolution [6] Direct digital conversion from multiplexed array [7] Based on analysis in Section 3.4 [8] Requires off-chip filter

3.4 Prototype Measurement Results

The prototype discussed in Section 3.3 was fabricated in a 1p9m 65 nm CMOS process. A die photo of the resulting IC is shown in Figure 3.8. While the chip was fabricated with an ADC on-chip, we bypassed this ADC for the purposes of this paper in order to better understand the ADC requirements. A single ECoG amplifier channel is on the chip with dimensions of 511 μm by 167 μm.

The resulting transfer function and noise performance for the fabricated chip are shown in Figure 3.9. The amplifier has a 40 dB/decade high-pass filter for low frequencies that decreases to 20 dB/decade high-pass at 0.5 Hz. This 20 dB/decade high-pass behavior corresponds to integration in the signal band of interest. Above the maximum frequency of 150 Hz several poles from the amplifier compensation and antialias filtering orchestrate an 80 dB/decade rolloff. The input referred noise plot in Figure 3.9b shows that 1/f noise is present, as expected, and that the system achieves a noise floor of 112 nV/$\sqrt{\text{Hz}}$ at 150 Hz, the designed maximum frequency of interest. This measurement is close to the designed target of 100 nV/$\sqrt{\text{Hz}}$ discussed previously.

3.4.1 Signal Fidelity Testing

A first comparison of prerecorded ECoG data with the same data run through this prototype system is shown in Figure 3.10a. This figure shows good fidelity ($r > 0.9$) throughout the frequency range except at the lower end of the spectrum. The discrepancy is due to saturation in the first amplifier stage for large, low-frequency signal content. This is especially prevalent during large motion artifact events, which is not a primary concern as this is work toward a future fully-implanted

system, which will not be subject to the same large scale motion artifacts. These motion artifacts are a part of the prerecorded data, and are due to the test setup used to record the data on an awake and moving macaque monkey.

Figure 3.10a primarily shows that this particular prototype does not have sufficient dynamic range to accommodate a signal as large as the prerecorded data used without some saturation. In simulation, the 1% total harmonic distortion (THD) of the front-end is 4 mV peak-to-peak, which is typically sufficient for ECoG applications. However, this dataset has spikes as large as 8 mV peak-to-peak.

By reducing the PSD of the same channel's signal by a factor of 2 before it is input to the amplifier, as seen in Figure 3.10b (with a slight time shift), we see that the correlation issues at low frequencies disappear, and we end up with a very high overall correlation rate of r = 0.9729. There is no strong frequency component to the correlation. This result supports the hypothesis that saturation is the root cause of the poorly correlated low-frequency signal, and suggests that the gain of the LNA stage should be lower in order to accomodate signals larger than 4 mV peak-to-peak. This would increase the power required for the first stage.

3.4.2 Required ADC Resolution

Figure 3.11 shows how the correlation between the prerecorded spectra in Figures 3.10a and 3.10b is affected by the number of bits used for digitization. This experiment was conducted via post-processing in Matlab using various quantization levels assuming a 1 V referenced ADC. In all cases the data were sampled at 1 kS/s. For the original waveform, correlation is highly consistent down

to 6-bits; below 6 bits there is deterioration of the signal quality.

In the scaled waveform shown in Figure 3.10b, correlation is degraded somewhat earlier, below 7-bits of resolution. This is expected for a direct scaling of the original signal. 7-bit ADC resolution is still sufficient to achieve high fidelity (r = 0.97) to the prerecorded data.

3.4.3 Comparison to State-of-the-Art

Table 3.1 shows the results of this prototype compared to other ECoG recording designs. This system achieves the lowest power per channel of the listed amplifiers. This is not primarily due to more efficient amplifier design, as the spot-NEF and spot-PEF figures show. Instead, we have reduced the power requirements by targeting an appropriate noise specification as discussed in Section 3.2.

Most of the other specifications are comparable to other state-of-the-art works, but note that this system is capable of being digitized by a 7-bit ADC. This is significantly lower than any other system with the exception of [66], which sub-bands the data and does not allow for simultaneous recording of full-spectrum ECoG. Note that most other systems without a VGA require substantially higher ADC resolution. Our system outperforms all listed systems at full signal reconstruction.

3.5 In-Vivo Measurement Results

In addition to the prerecorded data used in Section 3.4, the prototype AFE was also tested in-vivo on a non-human primate to verify that the system is capable of recording electrophysiological

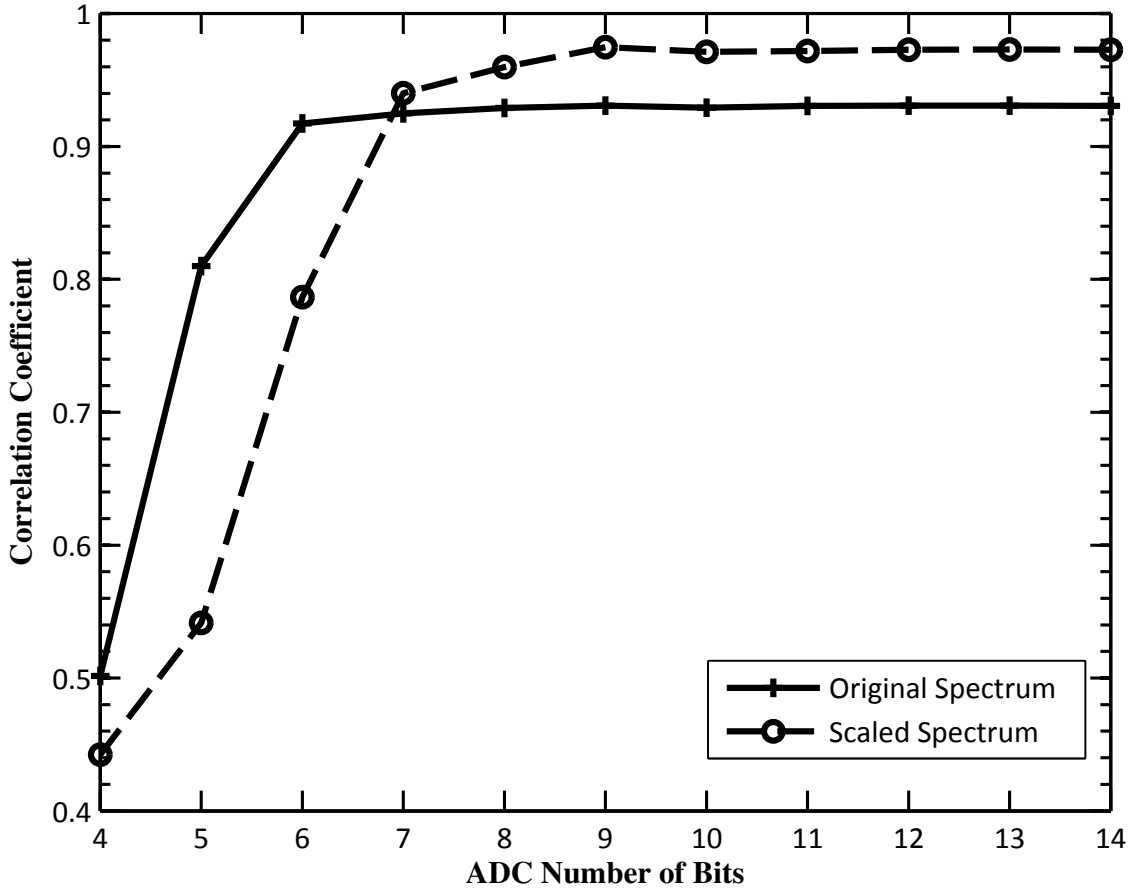
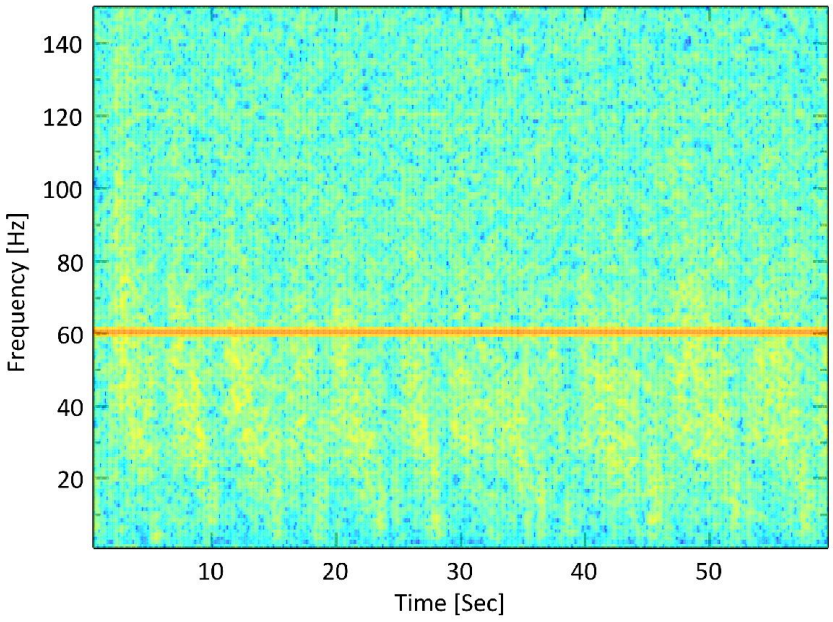
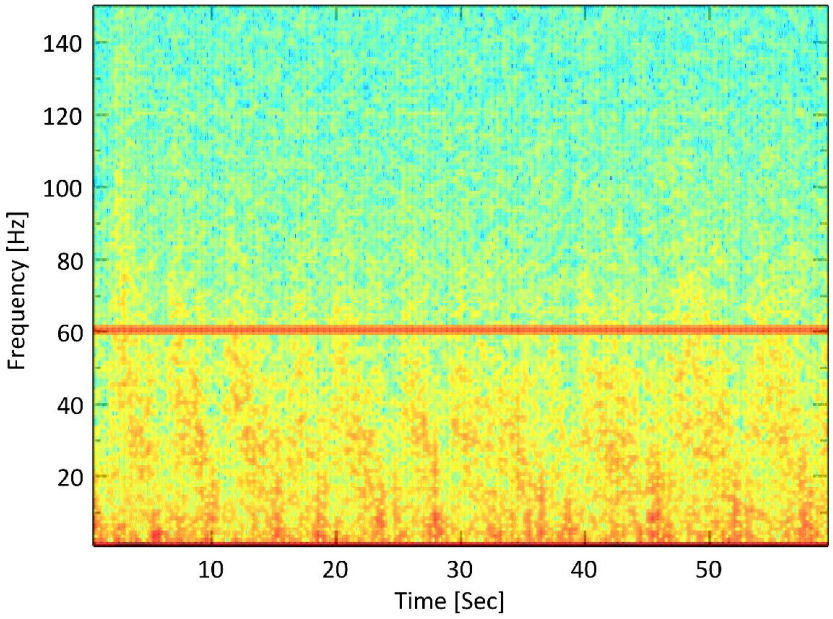


Figure 3.11: Change in correlation with ADC resolution for the prerecorded ECoG data in Figure 3.10a and Figure 3.10b.

data in a normal preparation. A sedated macaque monkey with previously implanted 250um platinum/iridium rod electrodes placed over primary motor cortex was connected to the prototype amplifier using approximately 12 inches of unshielded wire. The positive amplifier terminal was connected to a surface electrode and the negative terminal was connected to the ground screw located in the animal's skull. Sixty seconds of data were recorded through the amplifiers and output to an external ADC. The resulting spectrograms and PSD, both before and after integration, are

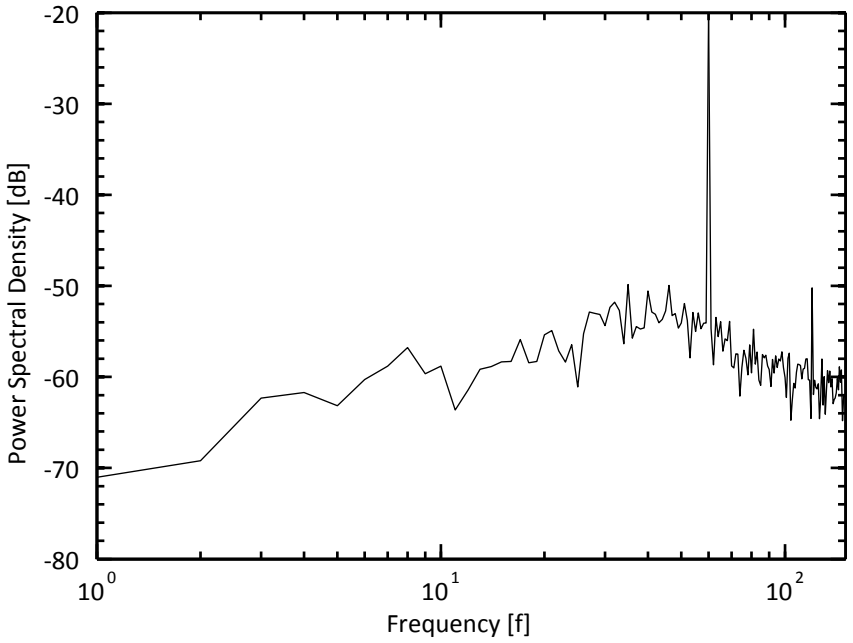


(a) Spectrogram of amplifier output before integration

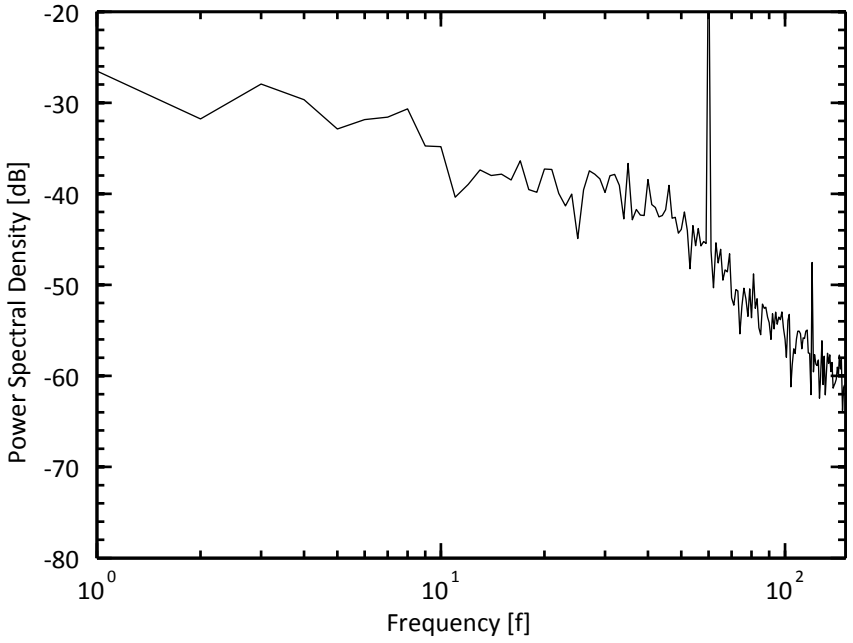


(b) Spectrogram of amplifier output after integration

Figure 3.12: Spectrogram at amplifier output of 60 s of in-vivo recording of a sedated macaque monkey using the prototype chip before and after integration.



(a) Before integration



(b) After integration

Figure 3.13: PSD of output spectrograms presented in Figure 3.12. This figure shows a characteristic neural signature in (b)

shown in the Figures 3.12 and 3.13, respectively.

As can be seen from the figure, the AFE successfully records in-vivo neural data. The signal power shows a characteristic decay with frequency (once recovered with integration). There is a significant 60 Hz peak on the amplifier output caused by the unshielded inputs, but this interference does not saturate the amplifier. Additionally, there is a second harmonic at 120 Hz, approximately 30dB below the first harmonic. This is caused by differences between the active and reference electrode wire lengths, which differentially couple 60 Hz and its harmonics to the amplifier input. Both the 60 Hz and 120 Hz harmonics are due to conditions imposed by the test environment available for this experiment. As shown in Figure 3.10, the system has sufficient CMRR and PSRR to reject 60 Hz in situations where the input leads are well matched.

Before integration, the signal has approximately 18 dB of dynamic range. After integration, the recovered signal has 35 dB of dynamic range, so in this particular case the ADC dynamic range required is approximately half of that required for a normal AFE.

3.6 Conclusion

In this paper we have discussed techniques for AFE design specific to electrocorticography. Amplifier efficiency can be improved by properly accounting for performance as it relates specifically to the signal of interest. We have shown that it is possible to decrease the required ADC resolution to 7-bits while simultaneously eliminating the need for a VGA. We have also shown that the noise performance requirements of ECoG are much less aggressive than are typically implemented on neural interface recording AFEs, which led to power savings in this prototype, and can potentially

yield significant additional savings if these findings are utilized more aggressively and over larger frequency ranges. Our differentiation technique has been successfully implemented for ECoG, and could have utility for other biopotentials that have similar underlying PSD characteristics. Reducing the power budget for recording channels is highly desirable, especially for high-density wireless recording, so these improvements will assist in enabling future wireless high-density ECoG recording systems.

Chapter 4

A SCALABLE, HIGHLY-MULTIPLEXED DELTA-ENCODED DIGITAL FEEDBACK ECOG RECORDING AMPLIFIER WITH COMMON AND DIFFERENTIAL-MODE ARTIFACT SUPPRESSION

4.1 Introduction

Chronic BBCI applications face several key engineering challenges. The desire for high electrode density and large spatial coverage will result in thousands of electrodes [1], with a goal of single-neuron interfaces. BBCIs require closed-loop neuromodulation, which generates large stimulation artifacts that obfuscate important signals during and shortly after stimulation. Power density requirements due to tissue heating remain restrictive, particularly in monolithic solutions. Additionally, a single-chip solution with efficient operation for both electrocorticography (ECoG) ($<$500Hz signals) and single neuron recording ($<$8kHz signals) is highly desirable.

In this chapter we demonstrate a channel, process, and frequency scalable recording system in standard 65nm CMOS. Figure 4.1 shows a high-level block diagram of the implemented system. There are several contributions to the state of the art described in this work. Highly multiplexed recording channels achieve a tenfold increase in recording channel density. Channel offset and signal dynamic range are robustly handled with a delta-encoding feedback loop that combines low-precision data converters to achieve high-precision recording. Real-time common-mode and differential-mode artifact suppression at the amplifier inputs is also demonstrated. The system

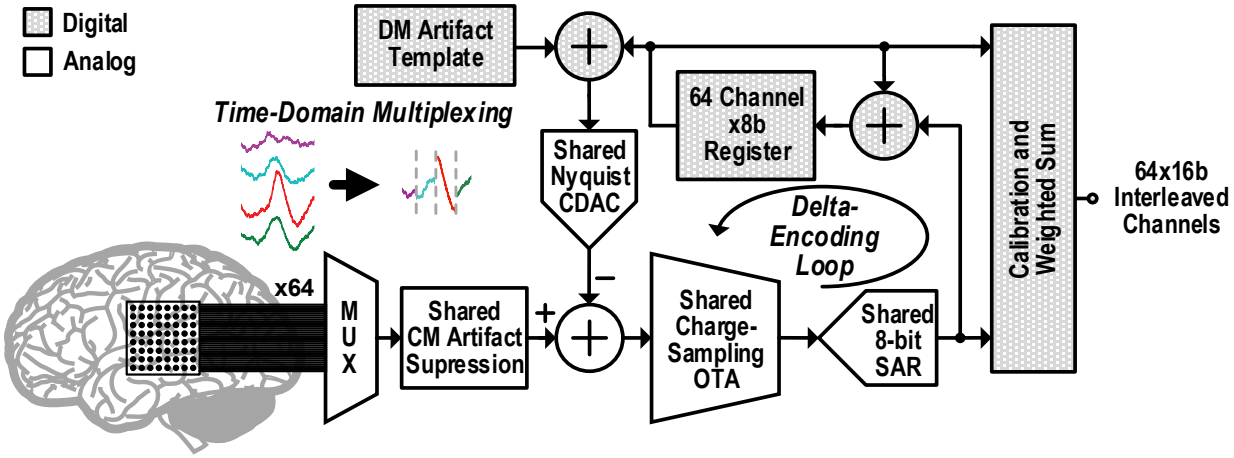


Figure 4.1: Functional block diagram of the highly-multiplexed, digitally-delta-encoded ECoG signal chain with common mode and differential mode artifact suppression.

scales efficiently in frequency and channel-count, making it useful for a variety of biopotential acquisition applications.

In Section 4.2 we discuss the overall architecture and analysis that led to the implemented prototype. Section 4.3 describes the details of the fabricated prototype. The results of prototype measurement, both on the bench and in-vivo are presented in Section 4.4. Finally, we discuss conclusions and potential next steps of this work in Section 4.5.

4.2 Artifact-Suppressing Multiplexed Digital-Feedback Architecture

As discussed in previous chapters, the PSD of ECoG and other biopotentials is colored with approximately $1/f^2$ [32]. This PSD shows that adjacent samples have very similar amplitude and strongly suggests performing signal acquisition by delta encoding, the measurement of the differences between samples. A digital delta-encoding scheme enables several other enhancements

including multiplexed amplifier operation, artifact suppression at the amplifier inputs, scalable sampling frequency, and the use of simple and robust blocks for acquisition. All of these are achieved without first-order impact on the noise performance of the amplifier.

4.2.1 Delta Encoding

We have previously shown in [54, 55] that analog delta encoding can be used to reduce ADC requirements at the amplifier output. Here we encode the signal in a similar way using digital feedback, as shown in Figure 4.2. In contrast with existing digital feedback schemes that require high-precision oversampling converters [39], the proposed architecture uses delta-encoding to track differences between successive samples at Nyquist rate. This significantly reduces the ADC dynamic range requirement for signals containing low-amplitude, high-frequency and high-amplitude, low-frequency content.

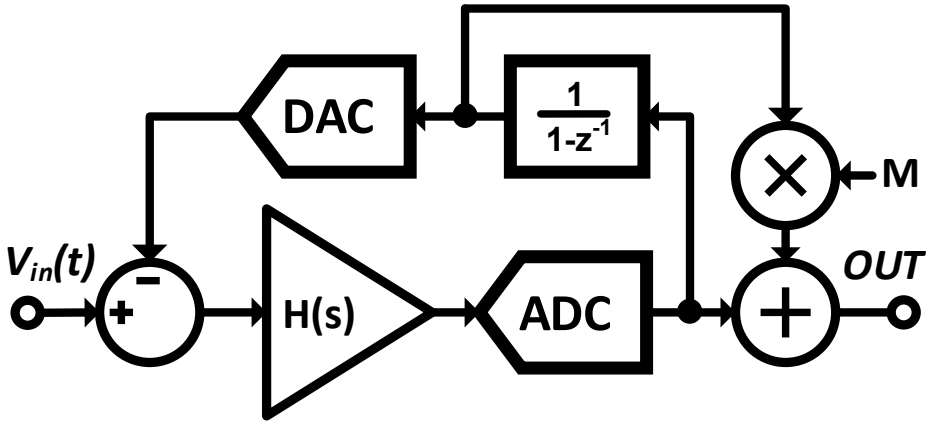


Figure 4.2: Delta encoding using an accumulating digital feedback loop. The aggregate count in the accumulator tracks the coarse voltage level that is fed back to the DAC, while the ADC output is the delta between the accumulated value and input voltage. Summing the ADC residue with the DAC interpolates the coarsely quantized DAC output to reconstruct the full signal waveform.

The input signal is passed through a gain stage H(s) and then digitized at moderate resolution (8 bits). The ADC code is input to a digital accumulator that tracks the large-scale variation of the signal based on the incremental differences between values. This accumulation is fed back to the input to complete the delta-encoding operation.

A full-scale feedback DAC would require oversampling. Instead, the accumulator operates on a truncated version of the ADC output and stores only 8 bits translating to an 8-bit DAC at the input. This makes implementation of the feedback DAC at Nyquist possible. The signal can still be reconstructed by adding the accumulator output weighted by the gain factor M to the ADC residue output. Thus, the ADC acts as an interpolator for the delta-encoder, allowing high-resolution data acquisition with moderate-resolution converters. In realistic systems, M will be calibrated to compensate for DAC transfer function nonidealities which are amplified at the ADC input.

4.2.2 Multiplexing for Channel Area Reduction

This digital feedback architecture makes it possible to multiplex the feedback networks for many channels using compact memory storage. Multiplexing the entire signal chain allows for recording channel density approximately 10x the state of the art. The accumulated residue in Figure 4.2 is stored on a channel-wise basis and then recalled periodically. In this implementation, the system can be multiplexed between 1 and 64 channels.

To achieve a large number of multiplexed channels, the amplifier must have a wide bandwidth so that settling is possible between adjacent independent channels. This directly contradicts the need for a low-pass response to eliminate noise aliasing from higher frequencies at the amplifier

inputs. To avoid this problem, we use charge sampling to create a sinc envelope filter on the input signal and input noise, while leaving the amplifier noise of a single stage amplifier in terms of kT/C. As described in [36], the noise power due to sources before the charge integration stage is linearly proportional to the sampling interval, which is nominally reduced by a factor of N for N independent channels. Therefore, we can say that multiplexing increases noise voltage due to sources before the input of the amplifier by $\sqrt{\mathrm{N}}$. This demonstrates the need to avoid additional gain stages before the integrating amplifier so that only biological and electrode noise is amplified by this factor. This penalty is reasonable for many electrode configurations where electrode noise does not limit signal acquisition [15, 52].

Crosstalk between adjacent samples should also be considered for multiplexed channels. As demonstrated in Figure 4.3, the value of the previous channel can considerably influence the current channel, especially when charge sampling, because the signal is not allowed to settle. To avoid this problem, we autozero each node in the circuit with high-precision settling between samples.

4.2.3 Noise Analysis

Two general paradigms exist for sampling of signals, as illustrated in Figure 4.4a. The conventional method of sampling requires a sampling time constant small enough to settle to several time constants within the allotted sampling window. Charge sampling, as discussed above, relies on a precise sampling period and therefore does not require settling for multiple time constants. Multiple time constant sampling substantially increases the required amplifier bandwidth, increasing power consumption and amplifier noise.

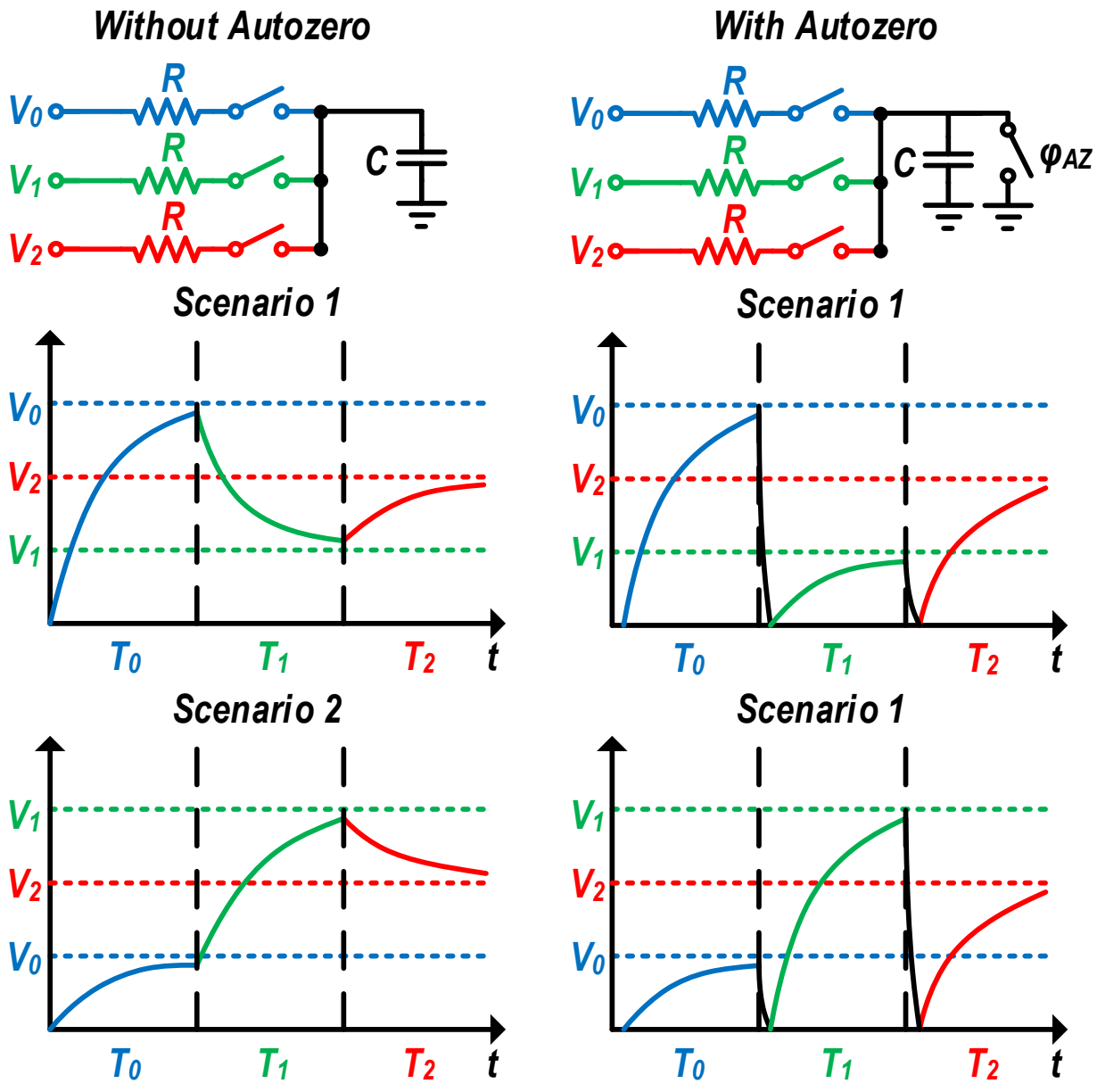
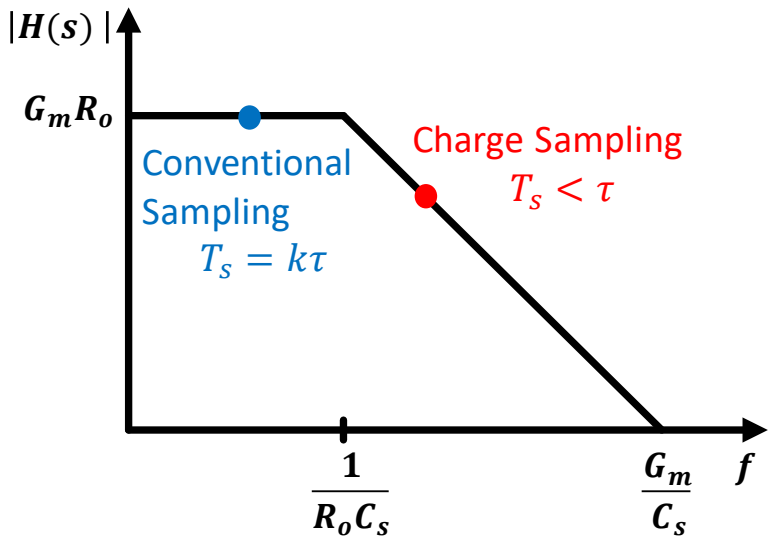
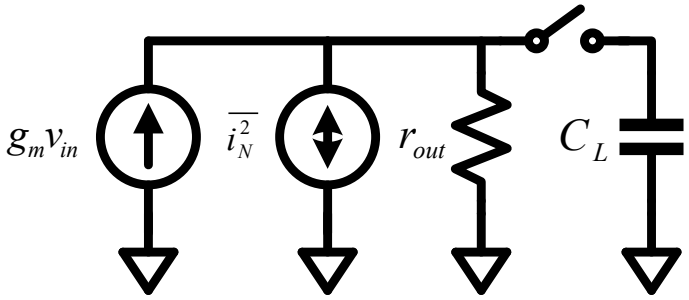


Figure 4.3: Exaggerated comparison of multiplexed inputs with and without autozeroing. Without autozero, correlation exists between adjacent channels leading to significant crosstalk.



(a)



(b)

Figure 4.4: (a) qualitatively demonstrates the meaning of charge sampling with respect to conventional sampling. (b) is the noise model for a OTA-based sampling stage.

To find the optimal operating region on this curve, we need to determine the most efficient time constant for the system. To do this, we analyze the input-referred noise of the system in the presence of transient settling. First, we know that the noise generated by a transconductance amplifier, as modeled in Figure 4.4b, is given by $\overline{i_N^2} = 4kT\alpha G_m$, where α captures topological, sizing, and process constraints on transconductor noise performance. From this expression, we can derive the output noise voltage from one sampling operation as:

$$\overline{v_{N-out}^2} = \overline{i_N^2} R_o^2 f_{noise} = \alpha G_m R_o \frac{kT}{C} \tag{4.1}$$

The gain of the circuit, including transient effects, is given by $A = G_m R_o \left[1 - e^{-\frac{T_S}{R_o C_s}}\right]$, where T_s is the sampling interval bounded by the sampling rate. Given this, we can derive the input referred noise as:

$$\overline{v_{N-in}^2} = \frac{\overline{v_{N-out}^2}}{A^2} = \frac{\alpha kT}{C_s G_m R_o \left[1 - e^{-\frac{T_S}{R_o C_s}}\right]} \tag{4.2}$$

From this we can easily derive the input-referred noise voltage as:

$$\overline{v_{N-in}} = \sqrt{\frac{\alpha kT}{G_m}} \frac{1}{\sqrt{\tau}\left[1 - e^{-\frac{T_S}{R_o C_s}}\right]} \tag{4.3}$$

This expression shows the expected inverse proportionality between noise voltage and $\sqrt{G_m}$. It also shows that T_s should be as large as the the sampling frequency allows. More importantly, it describes the optimal relationship between the sampling interval and the time constant, which is plotted in Figure 4.5. The optimal τ is coupled to the sampling interval at $\tau \approx 0.8T_S$. Since

there is one pole, the amplifier has optimal noise performance with a sampling interval just above the 3dB bandwidth. However, the 3dB bandwidth is highly dependent on the process-sensitive output impedance of the amplifier. Also, the sinc transfer function necessary for filtering electrode noise at the input to the amplifier requires operating past the 3dB bandwidth. Overall, this suggests operating near the 3dB bandwidth but in the integrating region of the curve.

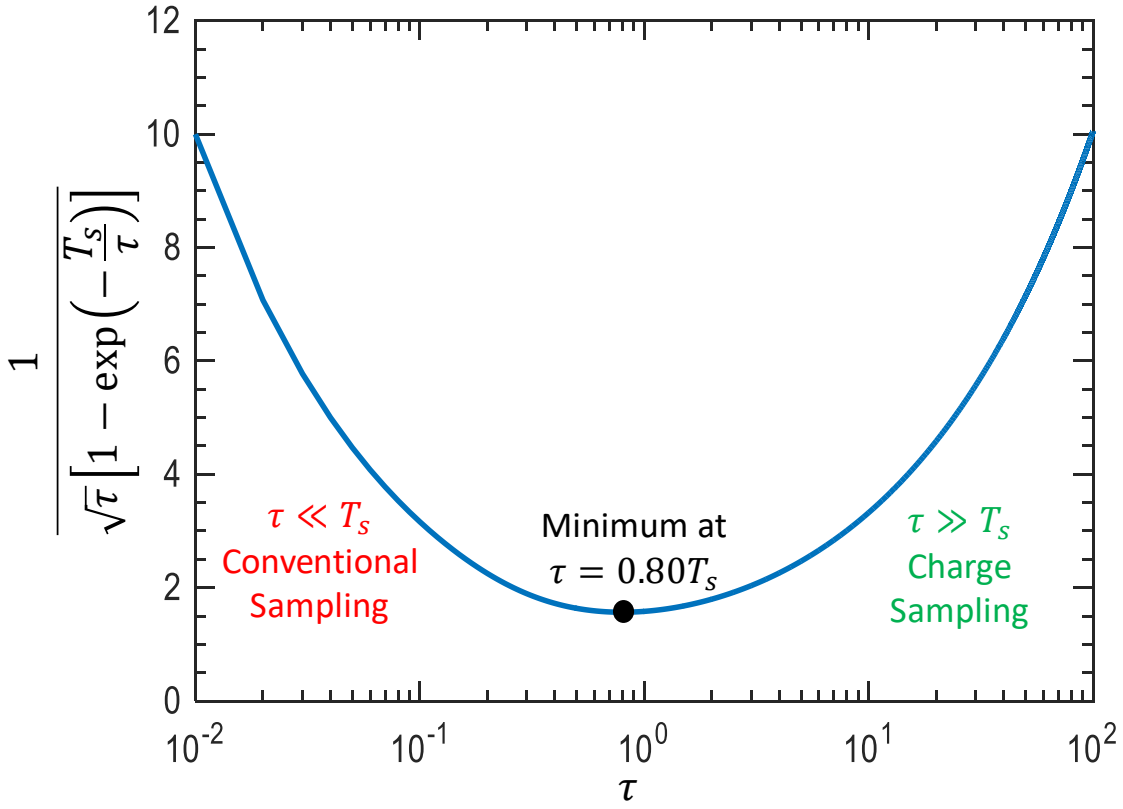


Figure 4.5: Equation 4.3 has a minimum at $\tau \approx 0.80T_s$.

A digital calibration is required for the transconductance and capacitive variability. This is optimally implemented by either adjusting the transconductance, or more easily, the load capacitance. A secondary fine tuning can take place using the integration period, but it is clear from the

expression that there is a noise penalty for using this adjustment. The penalty for adjusting G_m or C is proportional to the square-root, while adjusting T_s affects the input referred noise linearly.

In the charge sampling regime, the expression in Equation (4.3) simplifies by taking the linear part of the series expansion of the exponential term to Equation (4.4), where we assume weak inversion operation with $G_m = 25I_D$ and $\omega = 1/\tau$.

$$\overline{v_{N-in}} = \frac{1}{T_s}\sqrt{\frac{\tau \cdot \alpha kT}{G_m}} = \frac{1}{T_s}\sqrt{\frac{\alpha kT}{25I_D\omega}} \tag{4.4}$$

From this definition of input noise, we consider the case where we have N channels operating in time-division multiplexed portions of the total sampling period ($T_s = T_{s-1ch}/N$). In equation (4.3), we showed that τ (and therefore ω) should be fixed to a given proportion of the sampling interval, so this means that $\omega = N\omega_{1ch}$.

It is easily shown that the gain due to charge sampling is given by $v_{out}/v_{in} = G_mT_s/C_s$, so if we assume C_s is minimized and fixed for optimal noise performance, $G_m = NG_{m-1ch}$. These two terms substituted into Equation (4.4) under the square-root cancel with the linear change in N due to multiplexing. The result demonstrates that multiplexing has no nominal impact on noise performance under the chosen operating conditions.

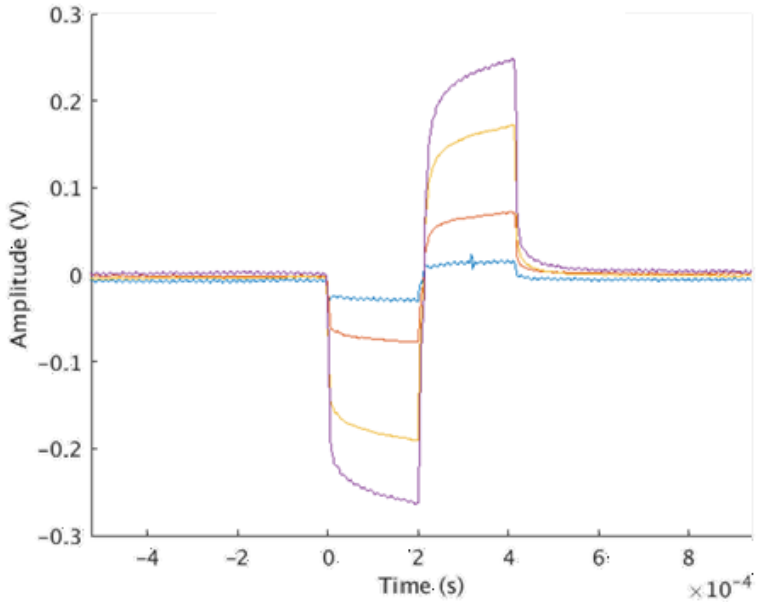
4.2.4 Artifact Suppression

Common- and differential-mode artifacts (Figure 4.6) create problems for biopotential acquisition in BBCIs because the required stimulation voltages are much larger than the recorded signals. Neuroscientists are interested in neural behavior that occurs shortly after stimulation [30]. As a

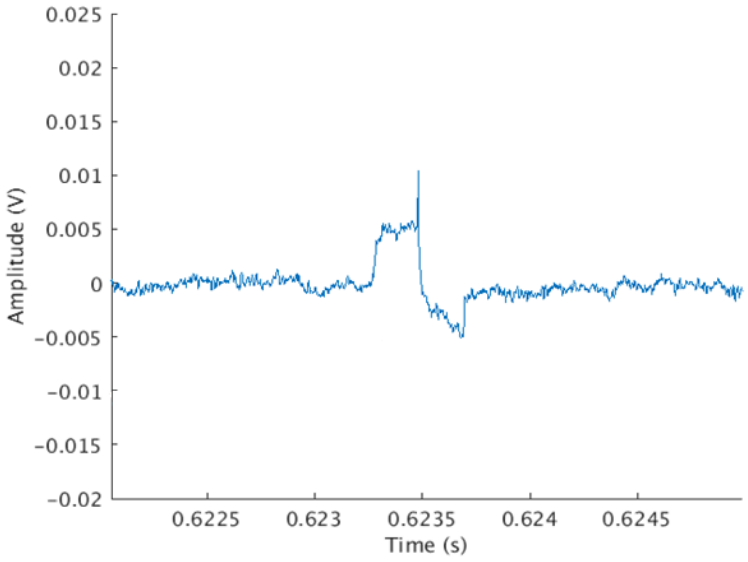
result, techniques that suppress common and differential-mode artifacts are desirable.

In this mixed-signal feedback implementation, the feedback DAC can be leveraged to enable differential stimulation artifact suppression at the amplifier inputs. Existing template subtraction methods [22, 27] can be implemented at the amplifier inputs to significantly reduce the dynamic range requirements of the signal chain. Adaptive methods are also possible. The efficacy of differential suppression techniques is limited by the DAC dynamic range. Very large artifacts would require a large DAC range. Additionally, DAC quantization limits the precision of artifact suppression. However, provided that the DAC can suppress artifacts into the linear range of the amplifier, further suppression is possible using post-processing techniques.

Large common-mode (CM) artifacts on the order of 100s of mV are often overlooked but can also degrade performance, particularly with the noise-efficient open-loop amplifiers employed in modern neural recording. We propose a passive, switched-capacitor technique shown in Figure 4.7 for CM artifact suppression (CMS) to stabilize the amplifier operating point and preserve differential gain. During pre-sampling, the CM signal is extracted by a switched-capacitor network and subtracted from the input signal, canceling it before amplification. This is a four-stage process. First the network is autozeroed to eliminate crosstalk from the previously sampled channel. Next, the input signal is sampled across the input capacitor C_{IN} with the bottom plate grounded. The differential mode signal is then cleared by connecting the differential inputs. At this point, the common mode voltage is stored across C_{IN}, and the bottom plate of C_{IN} is connected to the amplifier without showing the common mode offset. At this point, the signal can be resampled and the common mode voltage will not move the capacitor bottom plate (the amplifier input).



(a)



(b)

Figure 4.6: Common-mode (a) and differential-mode (b) artifacts for an H-bridge type stimulator. The amplitude and shape of both artifacts can vary considerably with the stimulation current and electrode.

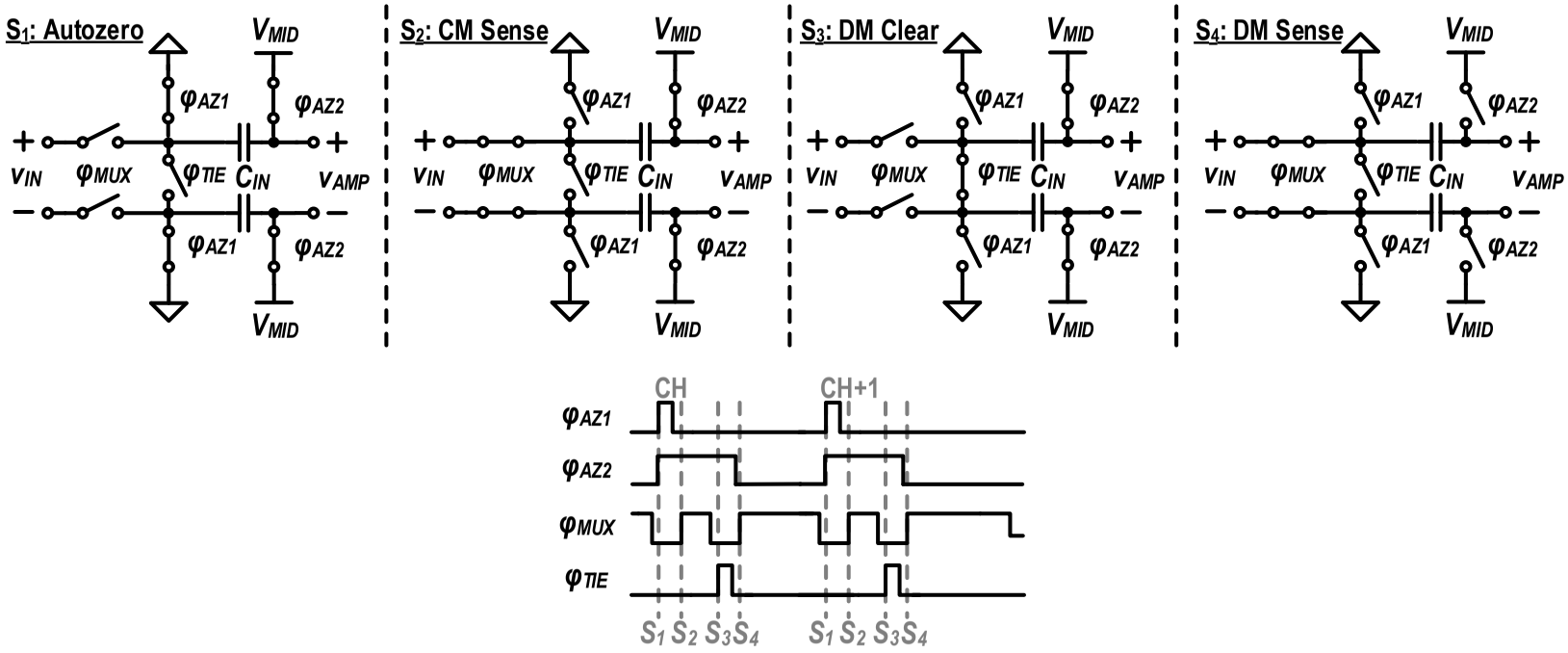


Figure 4.7: Operation and timing of the common-mode suppression (CMS) system. The common-mode voltage is double sampled onto the input capacitors in a four-step cycle.

There are two primary drawbacks to using this technique to eliminate common-mode offset. First, this technique introduces kT/C noise when the autozero switch φ_{AZ2} is opened. The magnitude of this noise is proportional to the series combination of C_{IN} and the electrode capacitance in parallel with the amplifier input capacitance. We will design C_{IN} such that we can reasonably approximate it as the total capacitance at this node. For C_{IN} = 50pF, this adds 9.1μV of integrated noise at the amplifier inputs, which corresponds to about 2 LSBs at the system output. This is undesirable but superior to blanking the channel.

The second issue is that the input impedance of the amplifier is considerably lower when sampling the common-mode voltage onto a large capacitor. The electrode interface must charge up this capacitor, which is substantially larger than the amplifier input capacitance. The effect is that the switched-capacitor input resistance is $\approx$10x lower, which will increase the high-pass corner between the electrode capacitance and the equivalent input resistance. For some electrodes, this will cause the high-pass corner to move into the signal band of interest. However, this effect is predicable, and because the SNR of the signal is high at low frequencies, the passband can be recovered using digital post-processing techniques.

The CMS scheme is also limited by the sampling rate of the system. This means that high-frequency transitions in the CM artifact are not sufficiently sampled for the technique to be effective. However, these transitions can be timed appropriately so that they occur while sampling on channels without useful information, which are common in implanted systems. The worst-case situation is when the entire CM artifact is a ramp function. If the slope of this ramp is steep enough, this technique will not be able to eliminate CM artifacts completely, but it will still allow operation

closer to the desired CM voltage than otherwise.

4.2.5 Frequency Scalability

One additional benefit of charge sampling is that the system scales efficiently with frequency. The gain of the amplifier in the charge-sampling regime is given by $A_v = G_m T_s/C_s$, so as T_s changes due to higher or lower sampling frequencies, the gain can be held constant without modifying the G_m. This allows for scaling of the system without modifying the transistor-level design of the amplifier. Coupled with the ability to select the number of channels, the system can be scaled in frequency with only a square-root impact on noise efficiency for decreasing T_s, as can be seen from Equation 4.4.

4.3 Detailed System Implementation

Details of the overall system are shown in Figure 4.8. Charge sampling in the amplifier eliminates the added power requirements of 7τ settling due to context switching between channels. Sample precision is determined by clock jitter, which is easily controlled at target sampling rates. A return-to-zero scheme at the inputs is implemented to eliminate crosstalk between channels (-92dB) and provide a uniform DC-coupled switched-capacitor input resistance. Use of a single amplifier for recording an array of channels allows for correlated double-sampling using a dummy channel to reduce flicker noise if required by the application.

Voltage-subtraction is enabled through digital storage for each channel with an 8-bit feedback DAC. Delta-encoding allows an 8-bit Nyquist-rate ADC to provide the dynamic range required for

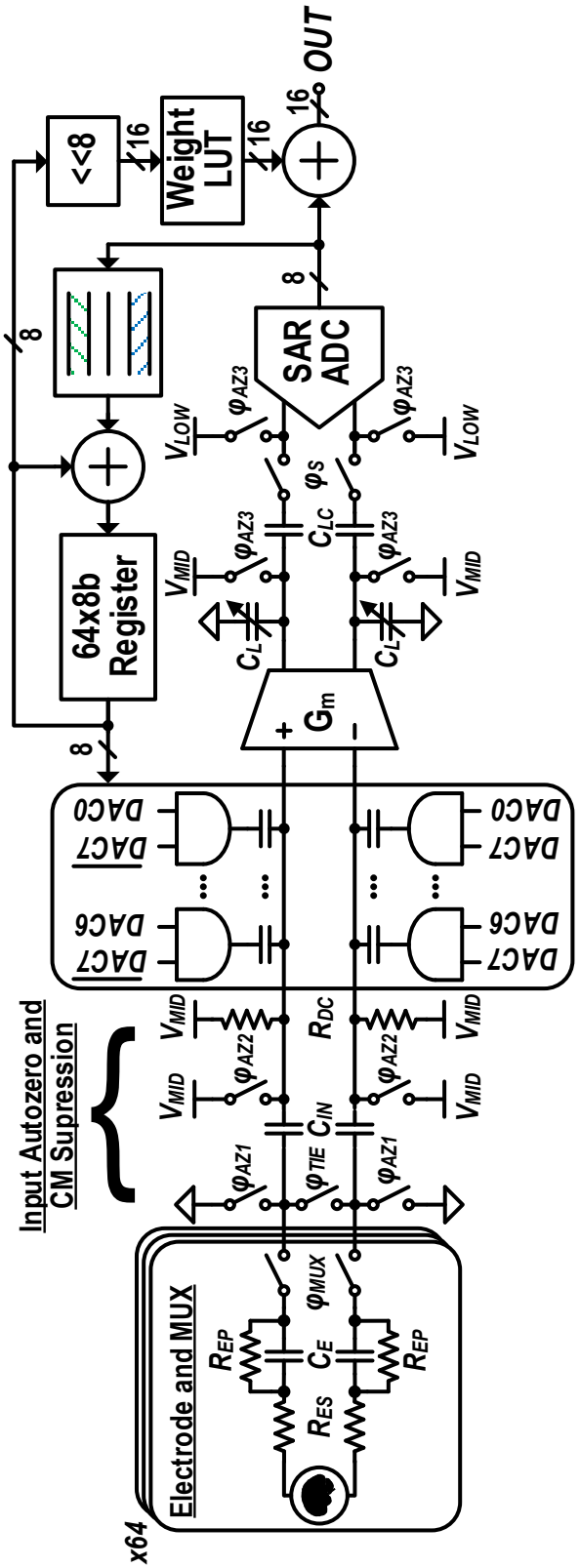


Figure 4.8: Detailed schematic of the analog front end, including delta-encoded feedback loop with 8-bit DAC and 8-bit ADC, CMS system, autozero scheme, and interpolation.

ECoG signal acquisition. The signal can be reproduced by adding the stored signal state to the ADC output (the digitized delta-encoder residue). A one-time calibration is sufficient to handle systematic DAC nonlinearity.

The amplifier output is AC coupled to a SAR ADC operating at 0.5V. The sampling-frequency-dependent input resistance (10-100MΩ) forms a high-pass corner with the series electrode capacitance (C_E) that is $<$1Hz for most electrodes and sampling rates. In rare situations where the high-pass corner is $>$1Hz, digital filtering can be effectively used to equalize the signal, exploiting the high SNR at low frequencies.

4.3.1 Timing

The timing of the system in normal operating mode is shown in Figure 4.9. After completing the sample from the previous channel, the input MUX is disabled and the DAC is returned to zero-state. This is done to ensure that the amplifier inputs start in a known state with similar impedances for every channel. Next, the autozero switches are activated, bringing both the input and output to a known state. In the nominal operating mode, the DAC top-plate is not autozeroed, but uses a large pseudoresistor to set the bias. This avoids kT/C noise at the amplifier inputs due to this switch, because this switch has no low-impedance path to ground.

After the input autozero is completed, it is disabled and the sampling switch at the input to the ADC is enabled. The system is still not sampling, because the output autozero is still active. The DAC is then enabled slightly before the MUX. This ensures that the DAC sees a uniform impedance. Next, the autozero switch at the output is disabled, which allows the OTA to begin

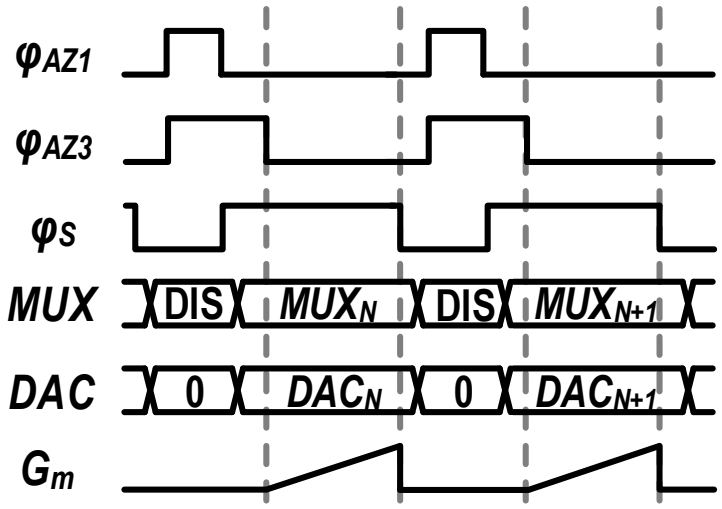


Figure 4.9: Autozero and sampling operation timing for 4.8.

integrating charge at the output. When the sampling window is completed, the sampling switch opens and the whole process begins again on the next channel.

4.3.2 OTA Stage

A schematic for the operational transconductance amplifier (OTA) is shown in Figure 4.10. The current-reuse amplifier topology leverages the high voltage supply needs of a stimulator on a monolithically integrated chip to operate at 2.5V. This allows a large amplifier device stack using thick-oxide devices, which improves noise efficiency and CMRR without gate-leakage concerns. This is particularly true because there is a level conversion to a 0.5V supply at the ADC input.

The two sets of input pairs are sized deep in weak inversion with very large areas to mitigate flicker noise. The cascode devices are sized in moderate inversion to maximize gain while minimizing the effects of their capacitance. The input CM voltage to the PMOS and NMOS devices

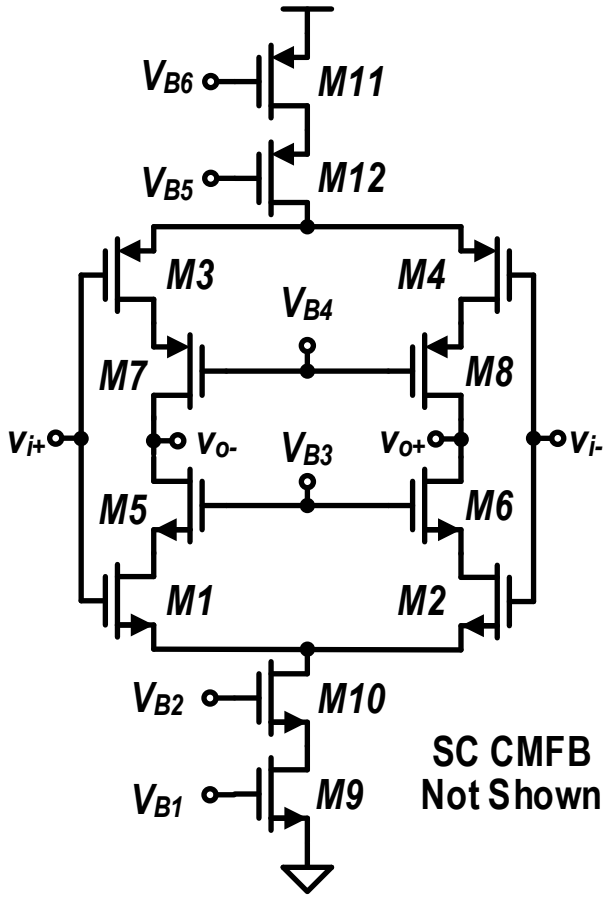


Figure 4.10: Transistor level implementation of the charge-sampling OTA.

is at mid-rail, so the tail devices are cascoded with the available headroom to improve CMRR and PSRR.

4.3.3 ADC Implementation

The ADC at the output of the amplifier serves as the sampling switch and a portion of the load capacitance for the charge-sampling amplifier. It is implemented as a top-plate sampling, monotonic-switching SAR ADC [29] with asynchronous logic timing [18]. In this fully differential implemen-

tation, a 7-bit DAC combined with an initial sign measurement creates an 8-bit output. The unit capacitor is implemented using a Metal-Oxide-Metal (MOM) capacitor structure with a unit size of 7.7fF. The large unit capacitor was implemented for robustness, because the power consumption of the ADC is negligible compared to the power consumed by the OTA. The entire ADC is powered with a 0.5V supply, which is primarily implemented to reduce the dynamic range requirements of the OTA and the LSB size of the converter, but also improves efficiency.

4.3.4 DAC Implementation

The DAC was also implemented using a monotonic switching structure similar to the ADC. 10fF unit capacitors are binary weighted over 7 bits with an additional bit from the sign of the operation. These unit capacitor values divide with the 50pF input capacitors and parasitic capacitance from the amplifier inputs to create nominal DAC step sizes of 500μV when driven with a 2.5V reference, which is half of the input-referred range of the OTA-ADC combination. Variations in the common-mode voltage due to the monotonic switching nature are partially mitigated by inverting the switching direction of the MSB [5]. The residual variation in the common-mode range does not affect the linearity of the system output with a THD specification of 0.1%.

4.4 Results

This system prototype was fabricated in a 1p9m 65nm CMOS process. The die photo is shown in Figure 4.11. The chip has been tested both on the bench for performance measurements and in-vivo to verify functionality in living tissue.

4.4.1 Bench Measurements

For measurements on the bench, a Platinum-Iridium microwire is emulated with R_{ES} = 7.5kΩ, C_E = 820pF, and R_{EP} = 5GΩ [15]. A Stanford Research Systems DS360 signal generator is used for high-resolution sinusoidal signal generation at low frequencies, and a Terasic DE1-SOC FPGA board is used to acquire the digital output signals.

Figure 4.12 demonstrates a measured signal recording of a nearly full-scale 35mVrms sinusoid applied at the inputs. This figure displays the interpolation of the accumulated output voltage that drives the DAC with the ADC output residue to form a complete high-resolution waveform.

The noise performance of the system sampling with both 2kS/s (ECoG) and 20kS/s (Single-neuron) rates is given in Figure 4.13. The use of correlated double sampling (CDS) is also demonstrated for ECoG recording to demonstrate that flicker noise can be mitigated if necessary with the expected 3dB increase in the thermal noise floor.

Figure 4.14 shows the INL and DNL of the system before and after calibration. Before calibration, the INL of the system varies considerably because the 8-bit DAC linearity is not sufficient after amplification with respect the ADC output. Calibration demonstrates that this can be corrected. Slight variation in the gain due to CM-DM conversion at the amplifier inputs causes the slope of the ADC interpolation vary, causing some additional INL issues. This increases the INL to < 3 LSB. DNL is always limited by thermal noise from the amplifier and is therefore $> \pm 0.5$ LSB with or without calibration, This demonstrates appropriate design, since the amplifier dominates power consumption and should be the limiting noise contributor.

Bench measurements of the CMS system are shown in Figure 4.15a. Without the CMS system,

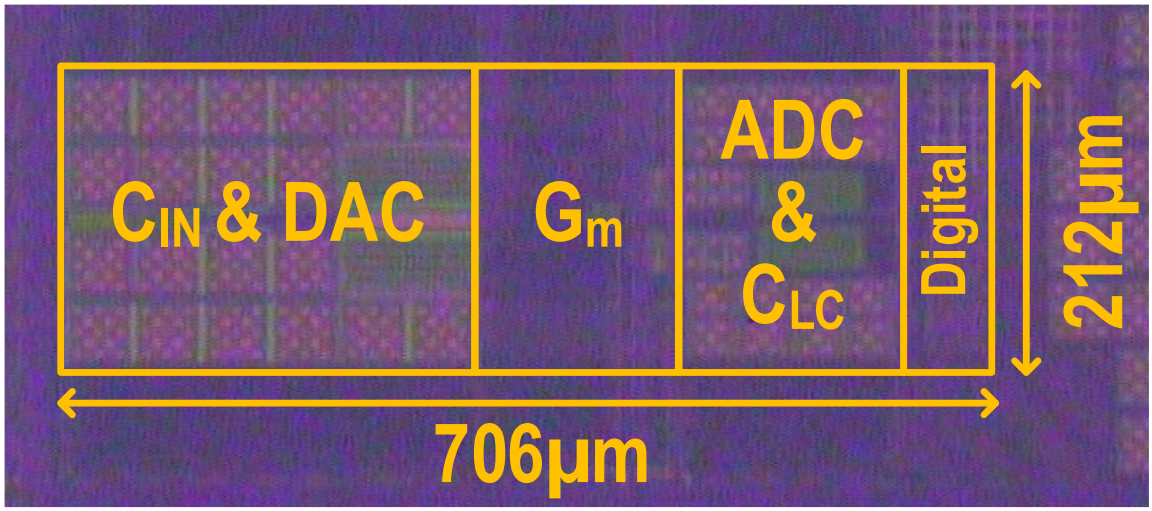


Figure 4.11: Photomicrograph of the implemented prototype.

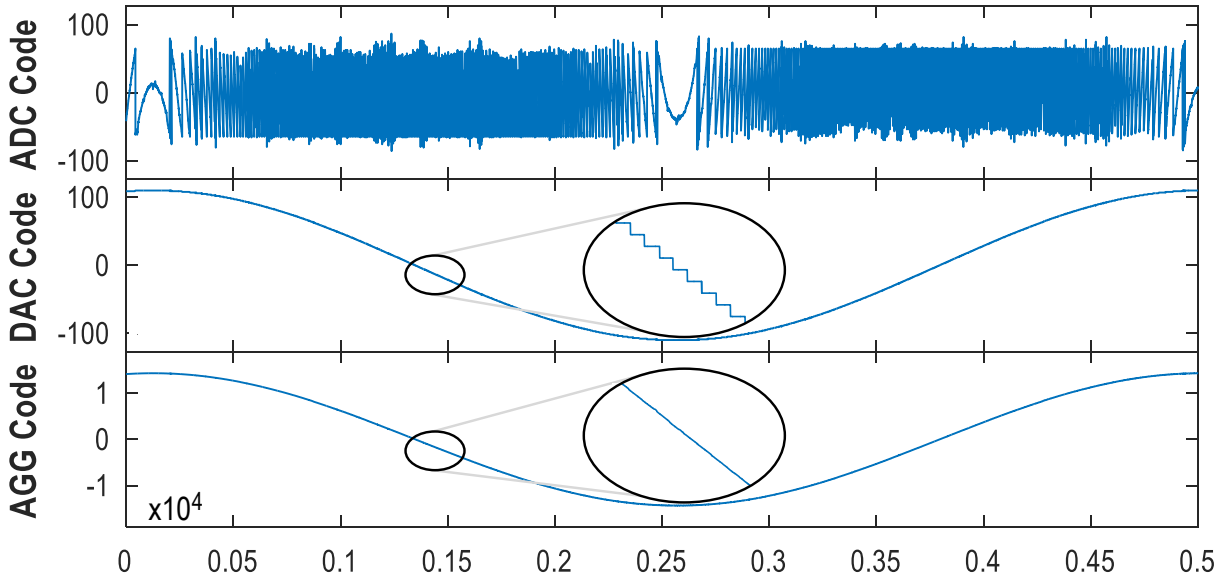
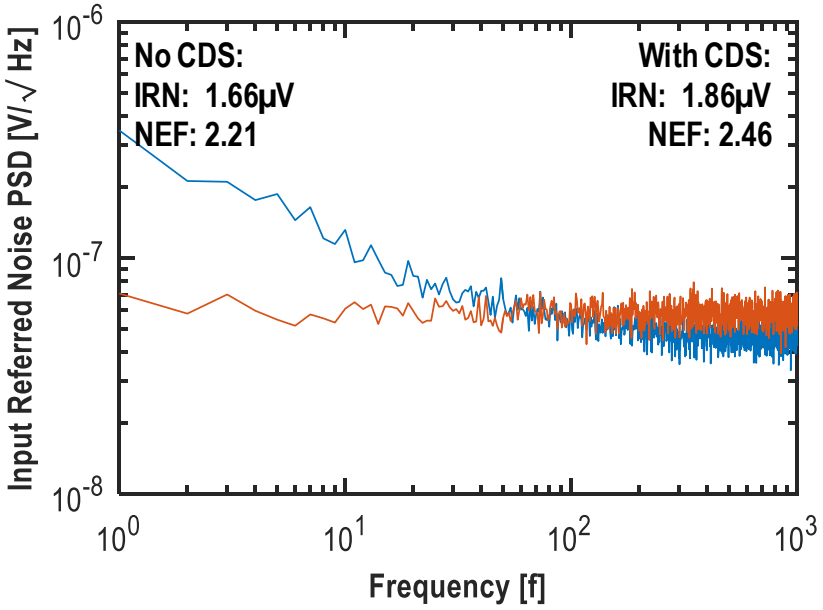
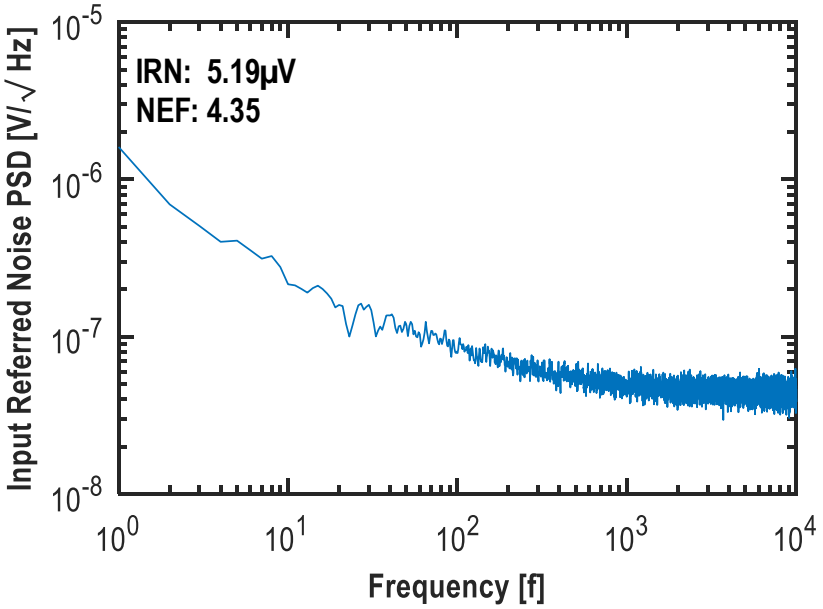


Figure 4.12: Demonstration of the ADC+DAC aggregation for a 2Hz, 35mV rms sinusoidal input. The ADC residue interpolates the coarsely quantized DAC signal to create a 14-bit aggregated output.



(a)



(b)

Figure 4.13: Input-referred noise measurements for (a) ECoG and (b) single neuron recording configurations. Correlated-double sampling (CDS) operation is also shown in (a).

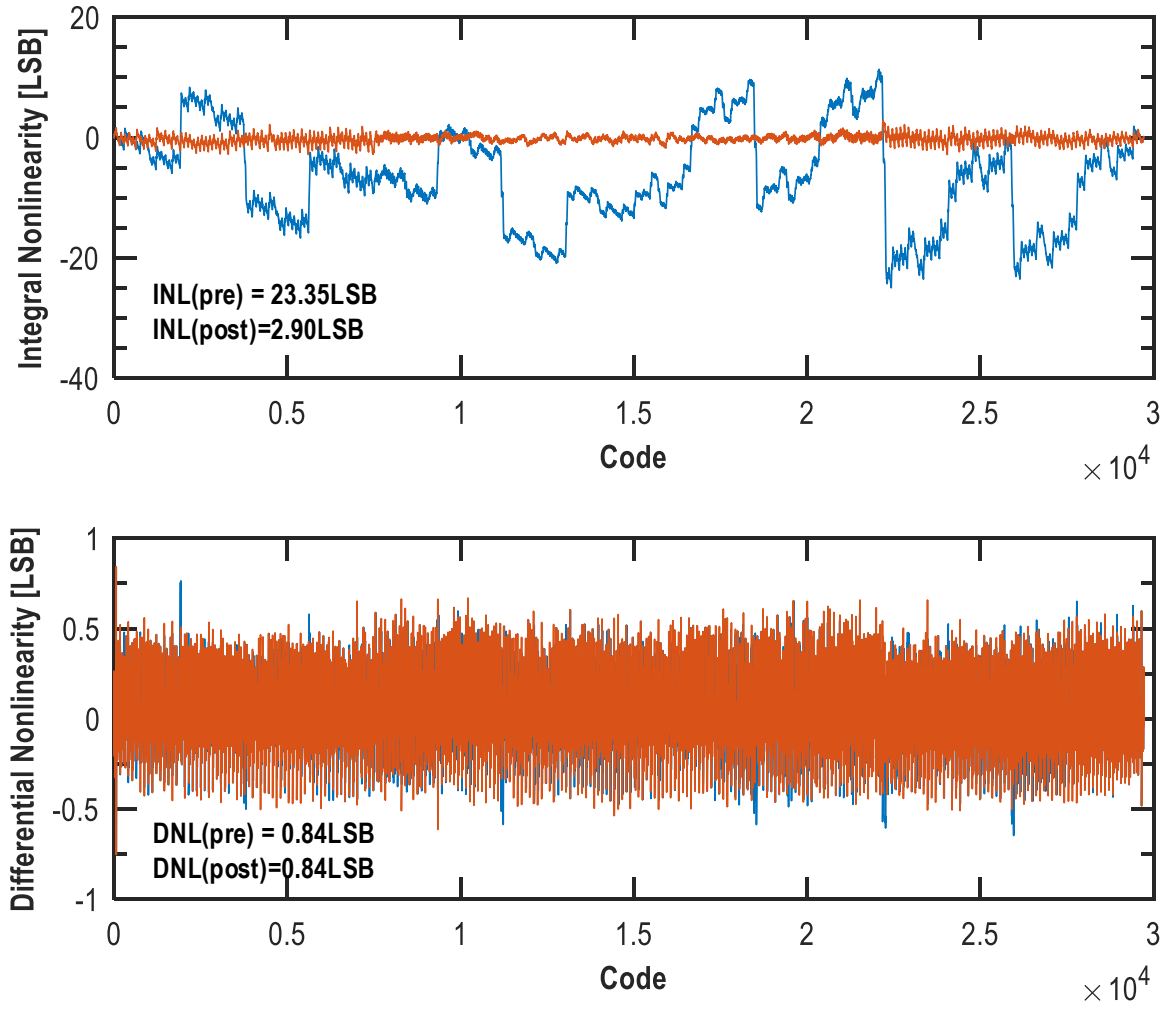


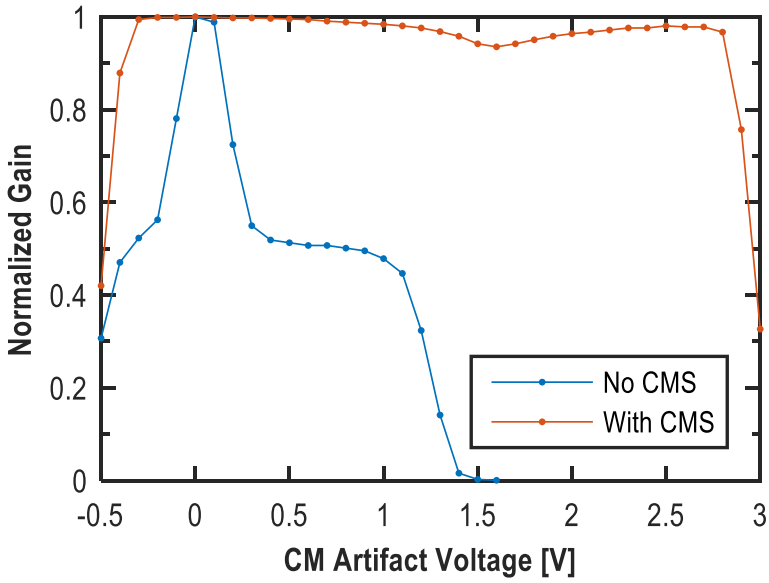
Figure 4.14: INL and DNL measurements of the prototype both before and after calibration obtained using the histogram method over 16777216 samples. The DNL is dominated by the noise floor of the amplifier, while the INL shows 2.90LSB linearity after calibration.

even small common-mode artifacts can substantially modulate the gain of the amplifier, which creates a nonlinear intermodulation product with the common-mode artifact and potentially sets the operating point of the amplifier in a highly nonlinear region. When CMS is turned on the gain remains very consistent until the complementary transmission-gate based switches of the multiplexer begin to enter the accumulation region. There is a 6% degradation of the gain near mid-range due to the complementary switches employed at the MUX input. The linearity of these switches is sufficient for recording purposes, but is degraded over large voltage swings. This could easily be corrected by bootstrapping the MUX switches, which could also be leveraged for increased voltage range.

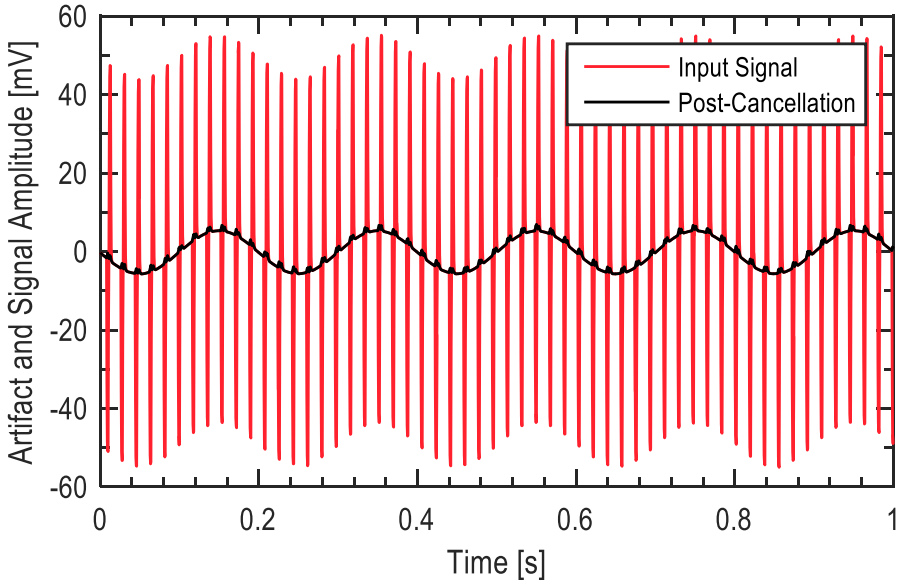
The differential-mode suppression scheme is demonstrated in Figure 4.15b. We use an H-bridge stimulator [44] in combination with our signal generator to create a test signal with an artifact. A 5Hz, 10mV sinusoid with a $\pm$54mV biphasic differential stimulation artifact is input to the system and suppressed at the amplifier inputs, demonstrating 46dB of artifact suppression before the amplifier inputs. This number is limited by the step size of the input DAC, but further post-processing suppression is possible because 46dB of suppression brings the artifact into the linear range of the signal chain.

4.4.2 In-vivo Measurements

In-vivo measurements were made on a pigtail macaque during two separate sessions. Figure 4.16 demonstrates operation on 3 channels simultaneously using time division multiplexing. Both the time domain and frequency domain are shown for clarity. The signal from all three channels shows



(a)



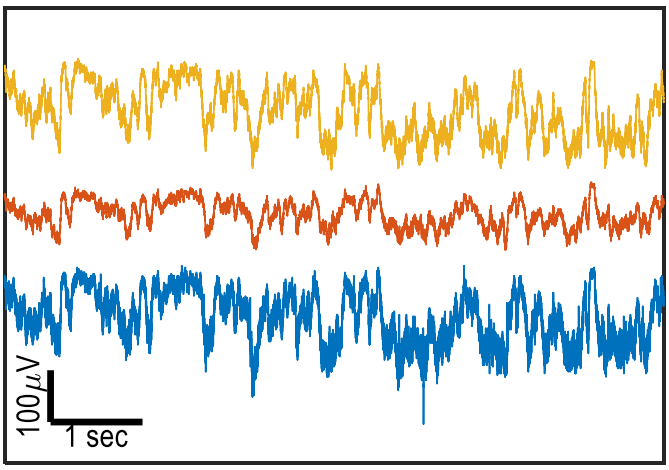
(b)

Figure 4.15: In-Vivo recordings in the presence of artifacts for common-mode (a) and differential-mode (b). (a) shows the voltage at the input to the amplifier with and without common-mode suppression. (b) shows the reconstructed output waveform with and without front-end suppression. (b) shows a 10mV sinusoidal 5Hz signal with a $\pm$54mV biphasic stimulation artifact before and after front-end suppression.

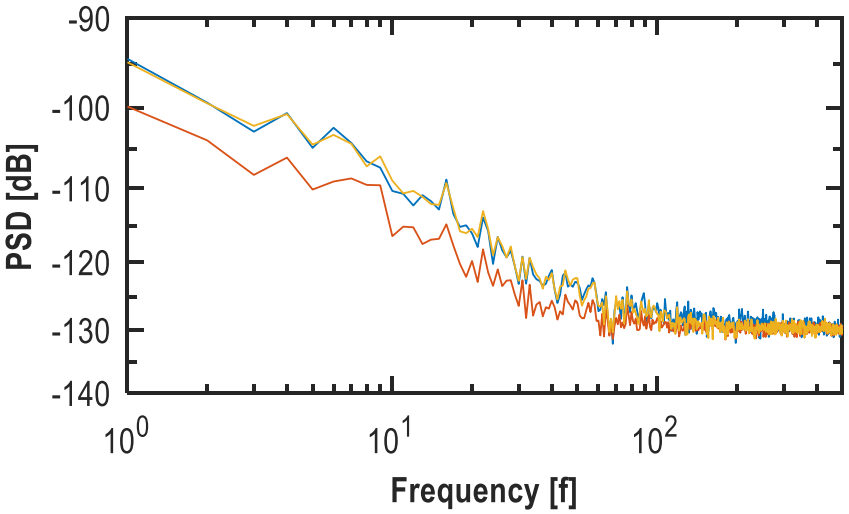
the characteristic colored behavior with frequency. The noise floor of the system is clearly visible at -130dB, demonstrating the limited and acceptable additional noise acquired from aliasing of the electrode series resistor.

A second set of measurements were taken on the same animal at a later date as shown in Figure 4.17. In this case we were able to demonstrate 16 simultaneous acquisitions for more than 2 minutes of acquisition time. Part (a) shows the full 2 minute acquisition, which clearly demonstrates the platform's ability to adapt to electrodes that are drifting in amplitude over several millivolts. Part (b) shows a 1 second subset of the original 2 minutes of data with correlated periodic waveforms on several channels.

In Figure 4.18, the common-mode and differential-mode suppression schemes are demonstrated in-vivo. Figure 4.18a shows the common mode suppression scheme across 3/64 channels. The buffered common-mode voltage at the amplifier inputs is measured using an oscilloscope with and without the suppression scheme enabled. In the case where the scheme is disabled, large common-mode variation is seen due to sampling of stimulus artifacts on the 3/64 channels that are connected. When the scheme is enabled, the common-mode voltage is stabilized and is always within 10mV of the nominal common-mode input voltage. Figure 4.18b shows the behavior of the differential-mode suppression system. While the suppression capability is limited by the coarseness of the input DAC, as discussed in Section 4.3 above, we demonstrate that the amplifier does not saturate when our suppression scheme is enabled. This allows for linear post-processing of the signal after digitization.

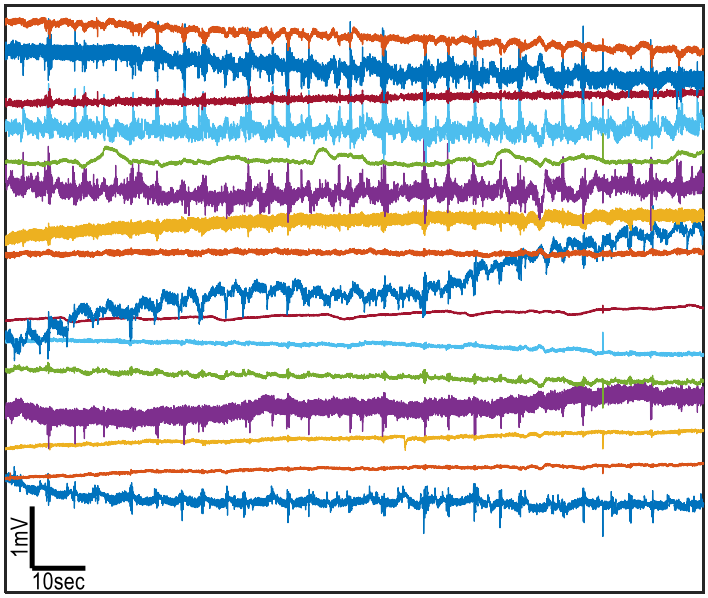


(a)

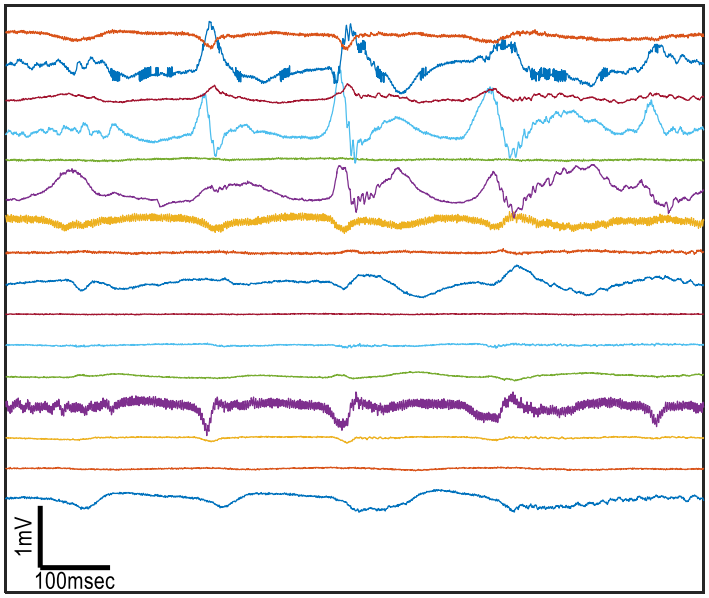


(b)

Figure 4.16: Simultaneously acquired multiplexed in-vivo measurements from the motor cortex of a sedated pigtail macaque on a single front end. Results in time (a) and frequency (b) domain on 3/64 channels.

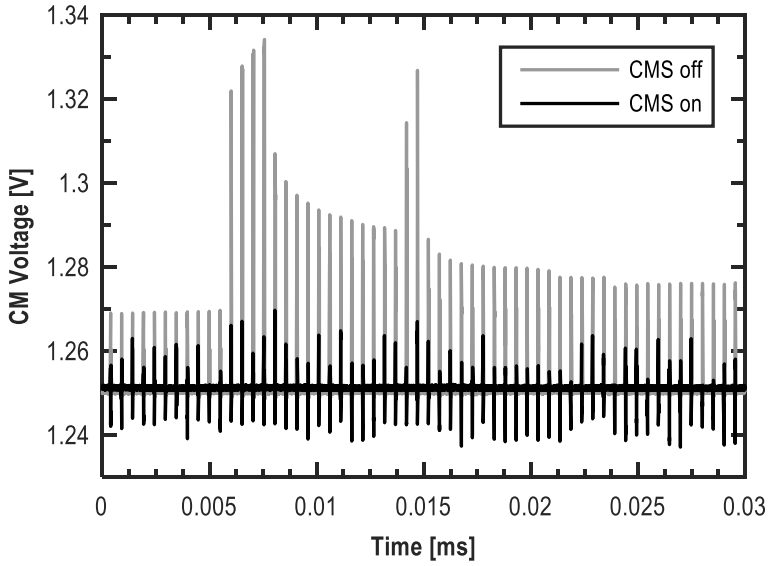


(a)

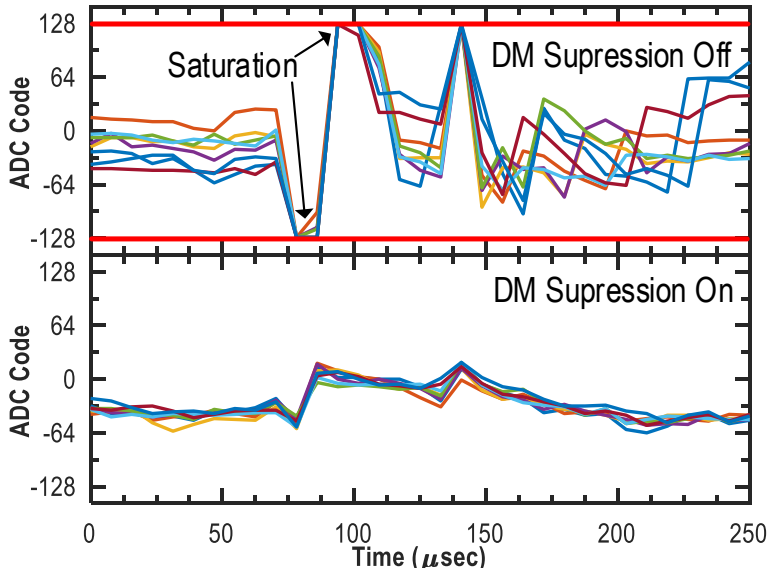


(b)

Figure 4.17: Sixteen channels of simultaneously acquired multiplexed in-vivo measurements from the motor cortex of a sedated pigtail macaque on a single front end. (a) shows more than 2 minutes of signal acquisition time while (b) demonstrates a 1 second subset of this data.



(a)



(b)

Figure 4.18: In-Vivo recordings in the presence of artifacts for common-mode (a) and differential-mode (b). (a) shows the voltage at the input to the amplifier with and without common-mode suppression. (b) shows the reconstructed output waveform with and without front-end suppression.

4.4.3 Comparison to State-of-the-Art

Table 4.1 compares the results from this chip to other recent works representing the state-of-the-art in cortical biopotential acquisition for both ECoG and single-neuron use cases. It demonstrates that the work performs comparably to the literature along all metrics and scales well with frequency without a major performance impact. Our primary contributions include the CMS scheme for common mode artifacts and full signal-chain multiplexing which improves the channel density by a factor of $>$10x. We also demonstrate excellent crosstalk performance because of the autozero scheme and the lack of parasitic paths between channels past the multiplexer inputs, which are next to the individual pads.

4.5 Conclusion

We have demonstrated a delta-encoded digital feedback biopotential amplifier with both CM and DM artifact suppression capabilities. The delta-encoding architecture enables a large dynamic range using low-resolution data converters and enables high-density multiplexing to reduce area. Measurements show frequency scalability from 2kHz to 20kHz to allow flexible usage for different biopotential applications. The resulting prototype performance is comparable to the state of the art with up to a 10x reduction in area per channel in the 64 channel configuration.

Table 4.1: Performance comparison of prototype with other biopotential amplifiers

	ISSCC'14 [39]	JSSC'16 [31]	JSSC'14 [6]	ESSCIRC'16 [46]	This Work ECoG	This Work Neural
Technology	65 nm	0.18 µm	0.18 µm	0.13 µm	65 nm	
Supply Voltage (V)	0.5	0.5, 1	1.8	1.2, 1.8	0.5, 2.5	
DM Artifact Suppression	—	Yes[1]	—	—	Yes[2]	
CM Artifact Suppression	—	—	—	—	Yes[3]	
Multiplexing	—	—	ADC	Shank	Complete	
Number of Channels	64	8	8	768	64	16
Channel Area (mm^2/ch)	0.025	0.17	N/A	0.12[4]	0.0023	0.0092
Power per channel (µW)	2.3	0.33	56.7	3	2.98	11.9
Input Referred Noise (μV_{rms})	1.2	3.05	5.2[5]	12.4[5]	1.66	5.19
Noise Efficiency Factor	4.76	1.63	1.77[5]	8.5[5]	2.21	4.35
AFE Bandwidth (Hz)	1-500	1-2k	0.1-700	0.5-8k	1-1k[6]	1-10k[6]
CMRR (dB)	88	—	—	—	76	
PSRR (dB)	67	—	—	—	82	
Peak-to-Peak Range (mV)	100	—	—	—	110	
Crosstalk (dB)	-85	—	—	-63	-92	

[1] Least-mean squares algorithm operating on a DAC at the amplifier inputs.

[2] Serial chip input to DAC at amplifier inputs. [3] Switched-capacitor offset correction scheme. [4] Full Probe.

[5] Amplifier Only. [6] DC coupled to electrode

Chapter 5

CONCLUSIONS

Several techniques for biopotential acquisition that are particularly suited for cortical signal recording have been demonstrated throughout this work. These approaches address several of the important outstanding needs for recording in BBCI applications and do not impact conventional performance metrics when compared with the state-of-the-art.

Minimizing the channel area by using time-domain multiplexing through the entire signal chain eliminates an active-area bottleneck for high-density recording applications critical to BBCI. This is made possible by offset suppression through Nyquist-rate delta encoding using a mixed-signal feedback topology. Earlier work on this topic demonstrated analog delta-encoding to mitigate the large dynamic range of biopotential signals. Artifact suppression, both common-mode and differential-mode, addresses another critical need for full-duplex communication with neural tissue in BBCI applications, especially when the number of stimulation sites increases for truly bidirectional systems.

Future directions for this work should particularly focus on the low-noise amplifier inputs. Improving the DC input impedance by using a servo loop would reduce concerns about electrode impedance affecting the high-pass corner at the inputs in DC coupled configurations, but would also increase the DC offset sensitivity of the amplifier. Increased DAC dynamic range is possible

to correct for this offset sensitivity, especially with a DC servo loop, as the input impedance can be decoupled from the input capacitance.

The addition of active common-mode suppression methods at the input would also be beneficial to eliminate the kT/C noise capture observed using the passive common-mode suppression technique. This could be achieved using either the existing input DAC revised with a fully-differential switching structure and a significantly larger range coverage (made possible with the addition of a DC servo loop). Alternatively, active electronics could be used to suppress the common-mode and differential-mode signals together, with additional power consumption. Ideally, either technique would make use of digital techniques to adaptively suppress the artifact at the inputs.

While a current reuse topology is optimal for noise efficiency, other amplifier topologies would improve immunity to common-mode variations at the amplifier inputs at the cost of increased power consumption. Amplifier efficiency is not as important in BBCI systems with many active stimulators, because the power injected into the tissue for stimulation will be orders of magnitude larger than amplifier power consumption.

In general, Amdahl's law suggests that the direction for biopotential acquisition in BBCI implementations should, to a reasonable degree, trend away from absolutely minimizing power in the recording channel and toward minimizing area and implementing features to improve robust and reliable recording performance.

The demonstrated techniques present a basic framework for very high density recording platforms to enable novel experiments and true full-duplex BBCI platforms with the spatial density and coverage required for the application and future neuroscience needs. Integrating this system

with a CMOS compatible stimulation platform [44] and wireless power and data transmission will allow for the high channel counts in very small form factors necessary for BBCI.

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Appendix A

OPERATIONAL DETAILS OF THE ECOG4 AMPLIFIER

This appendix details operation of the *ECOG4* platform for future use, including I/O and scan configuration settings.

A.1 Chip I/O

Analog Supply Pins

AVSS_ESD ESD ground supply. Also supplies ground for test buffer amplifiers and bandgap reference.

AVDD_ESD ESD power supply. Also supplies power for the test buffer amplifiers and bandgap reference. Nominally 2.5V.[1]

AVSS Analog core ground supply.

AVDD Analog core power supply. Operates at 2.5V.

Analog Reference Pins

VREF125 1.25V analog reference.

RESBIAS Bias for input resistor tuning. Can be used to reduce input impedance when the electrode impedance is low to reduce the residual DC offset.

VREFP ADC 0.5V reference.

VREFM ADC ground reference.

VREF025 0.25V reference for ADC.

VBGR Bandgap reference output voltage. Loaded nominally with a 10 μF capacitor.

Analog I/O

BUFF_FT_IN Input to test version of the analog output buffers.

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[1] There is an unknown issue with the bandgap reference that requires a higher supply voltage. 2.85V mitigates the issue.

BUFF_FT_OUT Output to test ersion of the analog output buffers.

SARIP Buffered positive SAR input node (before sampling switches).

SARIM Buffered negative SAR input node (before sampling switches).

GMOP OTA positive output (before level conversion).

GMOM OTA negative output (before level conversion).

DACOP Positive top plate of DAC; also the OTA positive input node.

DACOM Negative top plate of DAC; also the OTA negative input node.

VIP<16:0> Positive electrode input channels. Channels 15-0 are individual channels, while channel 16 is for inputs 63-16. This node could be multiplexed using an external MUX.

VIM<16:0> Negative electrode input channels. Channels 15-0 are individual channels, while channel 16 is for inputs 63-16. This node could be multiplexed using an external MUX.

Digital Supply Pins

ROVDD Digital supply for the on-chip ring oscillator VDD. Should be tuned so that the *SERIAL_CLK* node is at 13.56MHz, nominally.

DVDD 0.5V digital supply for the digital core.

DVDD_1V_REC 1V digital supply for interconnect on the chip.

DVDD_SCAN 1V scan digital supply.

DVSS Shared digital ground.

DVDD_1V 1V pad VDD for the core side of the pads.

DVSS_1V 1V pad ground pin for the core side of the pads.

DVDD_25V 2.5V dirty VDD for powering the pad drivers.

DVSS_25V 2.5V dirty ground for powering the pad drivers.

Digital I/O

RESET Global chip reset. Also zeros all analog switches.

SERIAL_EN Indicator to latch serial output data.

SERIAL_CLK 13.56 MHz clock coming from the on-chip tunable ring oscillator. Operates as the serial clock.

SERIAL_IN Serial input data for driving the input DAC. Useful for testing artifact suppression schemes. Also contains an enable bit for the

SERIAL_OUT Serial output data from chip, including Channel, ADC output and accumulator output (DAC input).

SCAN_PHI First phase scan clock.

SCAN_PHI_B Second phase scan clock.

SCAN_UPDATE Scan update.

SCAN_CAPTURE Scan capture.

SCAN_IN Scan input.

SCAN_OUT Scan output.

A.2 Scan Control

This chip is primarily controlled by a large scan register using the *Processing Systems Lab* scan IP.

This section will detail configuration paramters and optimal configurations for certain use cases.

A.2.1 Description of Scan Configuration Parameters

dac_delay 2-bit tunable delay for the DAC completion signal inside of the 8-bit SAR ADC block. This was implemented for robustness, but generally can be set to 0. Increasing the value will slow down SAR conversion.

az_delay 2-bit tunable delay for the autozero control signal coming from the analog clocks block. Increasing this value ensures adequate settling time after enabling the MUX inputs. Operation has been demonstrated with this value set to 0, but full performance has not been evaluated under these conditions.

ctune 5-bit thermometrically coded load capacitance tuning parameter. This determines the amount of load capacitance at the OTA output in 1pF increments. Tuning this value is the most noise-optimal way of changing the gain of the amplifier, though there is not sufficient range in the current implementation for all desired use cases.

train_mode Disable accumulation feedback when high. Useful for debug.

calib_mode When high, enables calibration mode, which completely disables DAC feedback. In combination with **calib_dac**, this allows explicit input DAC values to be applied to the chip through scan. Primarily useful for debug and testing.

calib_dac 8-bit 2's complement value to apply to the input DAC when **calib_mode** is enabled.

ch_start 6-bit value that in combination with ch_stop determines which channels are cycled during multiplexed operation. Setting ch_start = ch_stop will disable multiplexed operation.

ch_stop see ch_start.

threshold_pos 8-bit 2's complement value that determines which ADC code triggers an increment in the DAC code on the positive side.

threshold_neg 8-bit 2's complement value that determines which ADC code triggers a decrement in the DAC code on the negative side.

artifact_en Killswitch toggle when low for any artifact functionality, common-mode or differential-mode. This must be set to '1' for artifact suppression.

mux_en_cycles 10-bit unsigned value that determines how many cycles to wait for to enable the MUX after the end of the previous sample.[2]

mux_en_int_start 10-bit unsigned value that determines which cycle to start the intermediate MUX enable that samples the common-mode signal in CMS mode.

mux_en_int_stop 10-bit unsigned value that determines which cycle to stop the intermediate MUX enable that samples the common-mode signal in CMS mode.

az_mux_start 10-bit unsigned value that determines which cycle to start autozeroing the MUX in nominal sampling mode.

az_mux_stop 10-bit unsigned value that determines which cycle to stop autozeroing the MUX in nominal sampling mode.

az_mux_cmc_start 10-bit unsigned value that determines which cycle to start autozeroing the MUX in CMS sampling mode.

az_mux_cmc_stop 10-bit unsigned value that determines which cycle to stop autozeroing the MUX in CMS sampling mode.

az_dac_start 10-bit unsigned value that determines which cycle to start autozeroing the DAC in CMS sampling mode. Note that the DAC is not autozeroed unless CMS mode is enabled.

az_dac_stop 10-bit unsigned value that determines which cycle to stop autozeroing the DAC in CMS sampling mode. Note that the DAC is not autozeroed unless CMS mode is enabled.

tie_en_start 10-bit unsigned value that determines which cycle to connect the inputs together in CMS sampling mode.

---

[2]Scan parameters between **mux_en_cycles** and **dac_disable_stop** operate on a separate clock domain with a high-frequency on chip ring-oscillator. This should be corrected in a future revision.

tie_en_stop 10-bit unsigned value that determines which cycle to disconnect the inputs in CMS sampling mode.

dac_disable_start 10-bit unsigned value that determines which cycle the DAC should be disabled in all modes.

dac_disable_stop 10-bit unsigned value that determines which cycle the DAC should be enabled in all modes.

duty_cycle_threshold 10-bit unsigned integer that determines the number of 13.56MHz clock cycles to leave the sampling switch at the ADC input on.[3]

period_threshold 10-bit unsigned integer that determines the number of 13.56MHz clock cycles that make a full sampling period on a per-channel basis.

ss_slowdown_factor 2-bit division ratio for serializer.[4]

ss_offset_delay 2-bit delay for serializer.

A.2.2 Preferred ECoG Operational Scan Configuration

```
input [1:0] dac_delay = 2
input [1:0] az_delay = 3
input [4:0] ctune = 31
input train_mode = 0
input calib_mode = 0
input [7:0] calib_dac = 0
input [5:0] ch_start = 0
input [5:0] ch_stop = 63
input [7:0] threshold_pos = 64
input [7:0] threshold_neg = 192
input artifact_en = 0
input [9:0] mux_en_cycles = 50
input [9:0] mux_en_int_start = 11
input [9:0] mux_en_int_stop = 45
input [9:0] az_mux_start = 1
input [9:0] az_mux_stop = 49
```

[3]Note that this is a different clock domain from the preceding scan codes.

[4]An error in the input serializer requires both **ss_slowdown_factor** and **ss_offset_delay** to be 0 to use the input serializer.

```
input [9:0] az_mux_cmc_start = 1
input [9:0] az_mux_cmc_stop = 10
input [9:0] az_dac_start = 1
input [9:0] az_dac_stop = 49
input [9:0] tie_en_start = 46
input [9:0] tie_en_stop = 48
input [9:0] dac_disable_start = 2
input [9:0] dac_disable_stop = 46
input [9:0] duty_cycle_threshold = 90
input [9:0] period_threshold = 106
input [1:0] ss_slowdown_factor = 0
input [1:0] ss_offset_delay = 0
```

A.2.3 Preferred Single Neuron Operational Scan Configuration

```
input [1:0] dac_delay = 2
input [1:0] az_delay = 3
input [4:0] ctune = 0
input train_mode = 0
input calib_mode = 1
input [7:0] calib_dac = 0
input [5:0] ch_start = 0
input [5:0] ch_stop = 15
input [7:0] threshold_pos = 64
input [7:0] threshold_neg = 192
input artifact_en = 0
input [9:0] mux_en_cycles = 50
input [9:0] mux_en_int_start = 11
input [9:0] mux_en_int_stop = 45
input [9:0] az_mux_start = 2
input [9:0] az_mux_stop = 48
input [9:0] az_mux_cmc_start = 2
input [9:0] az_mux_cmc_stop = 48
input [9:0] az_dac_start = 1
input [9:0] az_dac_stop = 49
input [9:0] tie_en_start = 46
input [9:0] tie_en_stop = 48
input [9:0] dac_disable_start = 4
input [9:0] dac_disable_stop = 46
input [9:0] duty_cycle_threshold = 29
input [9:0] period_threshold = 42
```

```
input [1:0] ss_slowdown_factor = 0
input [1:0] ss_offset_delay = 0
```