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Design Techniques for Pin-Efficient Multi-Level Wireline Transceivers

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Abstract

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The demand for higher bandwidth links in high performance computing systems, particularly with the advent of chiplet-based and multi-chip module (MCM) architectures, has raised the critical challenge of interconnect bottlenecks. The finite number of available physical I/O pins limits system-level bandwidth, thereby requiring innovative pin-efficient transceiver solutions. This dissertation presents a comprehensive exploration of novel multi-level signaling methods and advanced circuit techniques aimed at designing high-speed wireline transceivers that overcome these limitations. A 12-bit 8-wire 8-level permutation coding scheme is first introduced for parallel wireline transceivers. This scheme achieves a 150% pin efficiency, significantly reducing the required baud rate for a given data rate, which in turn mitigates inter-symbol interference (ISI). Furthermore, its inherent design suppresses simultaneous switching noise (SSN), electromagnetic interference (EMI), and common-mode noise (CMN). Secondly, a novel non-uniformly quantized successive approximation register analog-to-digital converter (SAR ADC) with code-dependent weights (NUSA-CDW) is proposed for wireline receivers. This ADC architecture offers flexibility in realizing non-linear transfer functions to improve bit-error-rate (BER) compared to conventional SAR ADCs. Thirdly, Chord-PAM4 (CPAM4) signaling is presented as a pin-efficient and noise-resilient multi-level scheme for parallel links. CPAM4 increases pin efficiency by 50% compared to conventional differential PAM4 signaling when Chord-PAM4 signals are correlated over 4 wires (CPAM4-6). It

enhances pin efficiency by leveraging both amplitude and spatial domain coding, projecting binary input data onto multi-level signals while maintaining robustness against CMN, SSN, and ISI. Finally, a configurable UCle/LPDDR4X combo-PHY transceiver is designed and implemented in 28nm CMOS technology. This transceiver supports NRZ, PAM4, and the proposed CPAM4 signaling, providing a universal communication solution for die-to-die links that accommodates both data computing and memory access standards. The transceiver in CPAM4-6 mode provides 150% pin efficiency and 1.19pJ/b energy efficiency at 21Gb/s data rate.

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DEDICATION

to my family

Chapter 1

INTRODUCTION

The trajectory of high-performance computing systems over the past decades has been marked by a series of architectural transitions, each driven by the need to overcome the limitations of technology scaling. System designs have evolved from monolithic single-core processors to multicore systems, and more recently, to chiplet-based and multichip module (MCM) architectures. Figure 1 shows the HPC microprocessor trend over 50 years [1]. While these transitions have enabled continued performance scaling, they have also exacerbated the challenge of interconnect bottlenecks. The number of available physical I/O pins often becomes a limiting factor to system-level bandwidth, motivating the need for pin-efficient transceiver solutions.

Advanced signaling techniques such as pulse amplitude modulation (PAM) [5, 6], chord signaling [3, 7, 8], and permutation codes [9, 10, 2] provide a pathway toward enhancing pin efficiency and signal integrity. These methods are particularly well-suited for emerging heterogeneous integration platforms, including 2.5D interposers and 3D-stacked chiplets, where pin density and power integrity issues are especially pronounced [7]. Traditional binary signaling scheme, non-return-to-zero (NRZ), require one pin per bit per unit interval (UI). PAM signaling such as Four-level PAM (PAM4) has become popular as the data rate continue to grow for their ability to increase the pin efficiency by 2x and relax the link Nyquist rate [5]. However, these multi-level schemes are more sensitive to noise and inter-symbol interference (ISI), and they impose stringent linearity requirements on both transmitter and receiver front-end circuits. As a result, high-speed transceiver designs must incorporate advanced equalization techniques, including continuous-time linear equalizers (CTLEs), decision feedback equalizers (DFEs), and high-speed ADC-based receivers, to maintain signal integrity

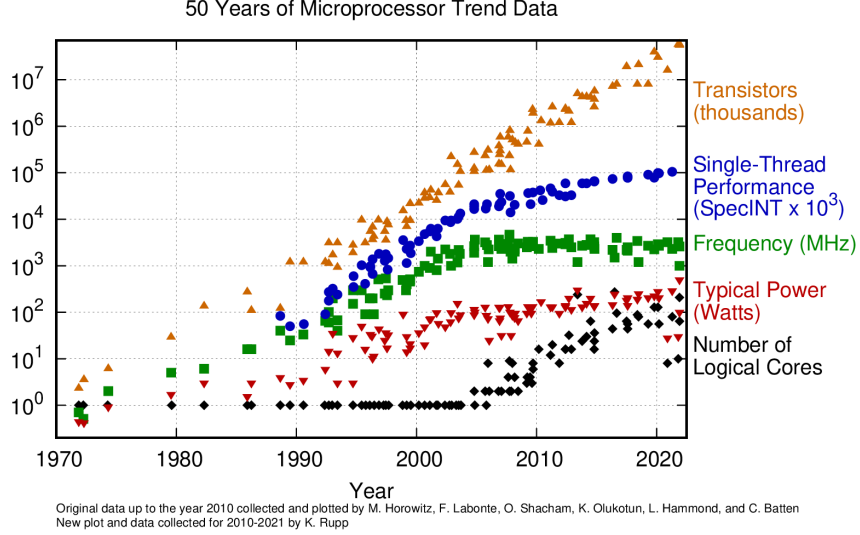


Figure 1.1: 50 yeas of microprocessor trend [1].

and recover data reliably. Moreover, as system designs adopt more complex packaging technologies, including 2.5D interposers, chiplets, and high-bandwidth memory (HBM) stacks, the power integrity and signal integrity challenges become more pronounced. Simultaneous switching noise (SSN), power delivery fluctuations, and electromagnetic coupling pose severe limitations on signaling reliability, especially in high-density I/O environments.

To address these challenges, this thesis explores pin-efficient multi-level signaling methods and circuit-level techniques for designing multi-level wireline transceivers. A 12-bit 8-wire 8-level permutation coding is proposed to improve pin efficiency with 8 levels of signal. To enable utilization of various equalization techniques for multi-level signaling, a non-uniformly quantized SAR ADC with code-dependent weights is designed for multi-level wireline receivers. A pin-efficient Chord-PAM4 signaling is proposed to improve pin efficiency while maintaining noise resilience. A UCIE/LPDDR4X combo-PHY leveraging Chord-PAM4 is designed to provide a universal communication solution for die-to-die links supporting both data computing and memory access. Fig. 1.2 illustates an example of a chiplet-based system,

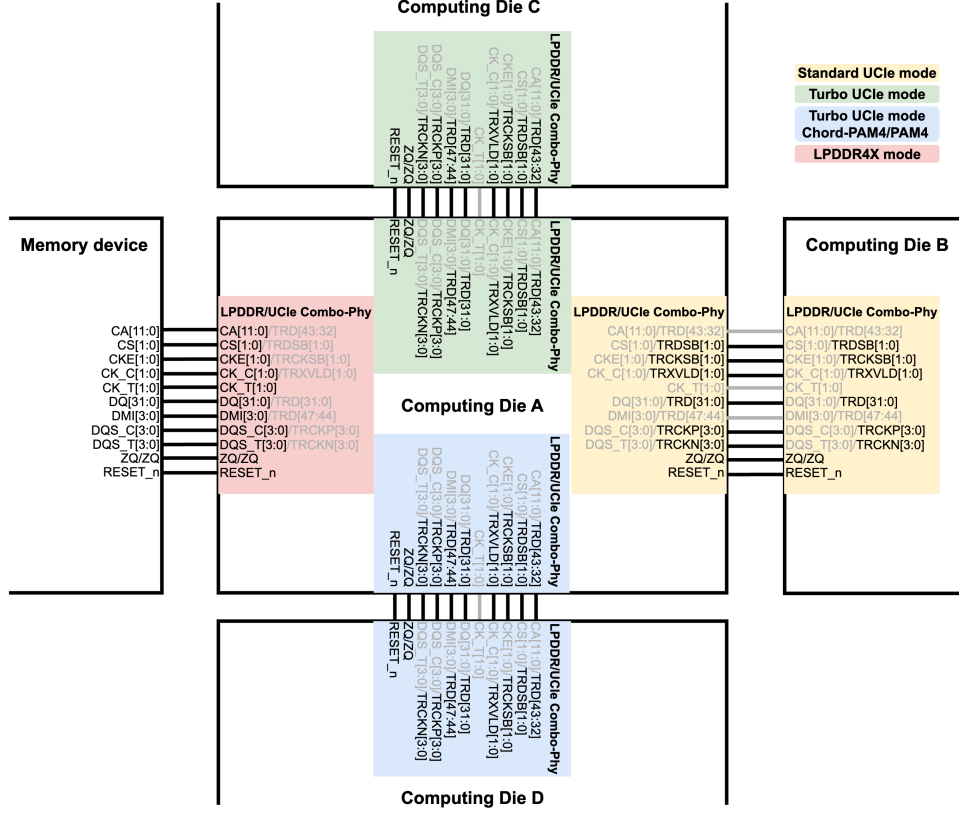


Figure 1.2: A chiplet-based system with the proposed UCIe/LPDDR4X combo-PHY.

where the integrated high-speed links can be configured either in the standard LPDDR4X mode to interface with DDR memory dies, or the UCIe mode to interface with computing dies. To fully utilize the pins required for LPDDR4X, the UCIe PHY is extended from its standard 16 lane mode to a 48 lane turbo mode. When A communicates with DDR, it works in the LPDDR4X mode. When communicate with B and C-D, it operates in the 16-lane standard mode and the 48-lane turbo mode. In the turbo mode, throughput is further increased with Chord-PAM4/PAM4.

The remainder of this thesis is organized as follows. Chapter 2 provides a comprehensive background on signaling methods, pin efficiency, signal integrity, and wireline transceiver circuits. Chapter 3 introduces pin-efficient 12-bit 8-wire 8-level permutation coding. Chap-

ter 4 presents non-uniformly quantized SAR ADC with code-dependent weights for wireline receivers. Chapter 5 proposes pin-efficient noise-resilient Chord-PAM4 signaling. Chapter 6 implements a configurable Chord-PAM4/PAM4/NRZ Transceiver combining and enhancing UCle/LPDDR4X standards.

Chapter 2

BACKGROUND

2.1 Pin Efficiency

In recent high-performance computing (HPC) and system-on-chip (SoC) architectures, the demand for high-bandwidth, low-latency communication between processors, memory, and accelerators continues to escalate. On-board and on-package interconnects form the backbone of such communication. However, the number of I/O pins available on a chip or package is a limited and costly resource. *Pin efficiency*, defined as the ratio of the number of bits transmitted per I/O pin per unit interval (UI), has therefore emerged as a critical figure of merit in wireline transceiver design [11, 2, 12, 7]. Pin efficiency (η) quantifies how effectively a wireline transceiver utilizes its available physical I/O pins to transmit information. It is commonly expressed as

$$\eta = \frac{\text{Total Data Throughput per UI}}{\text{Number of I/O Pins}} \times 100\% \quad (2.1)$$

Traditional single-ended non-return-to-zero (NRZ) signaling schemes transmits 1 bit per pin and has a pin efficiency of 100%. As data rates have approached physical channel limitations, driven by increased parasitic loading, signal integrity issues, and power constraints, engineers have explored multi-level modulation schemes such as pulse amplitude modulation (PAM) to enhance data throughput without increasing I/O pins [13]. This trend is evident in high-speed interfaces such as 400G Ethernet and GDDR6, which exploit multi-level signaling to alleviate I/O bottlenecks while maintaining manageable power and area overheads [14]. For example, 4-level PAM (PAM4) signaling doubles the bit-per-symbol rate relative to NRZ (2 bits per symbol), thus improving pin efficiency:

$$\eta_{\text{PAM-4}} = \frac{\log_2 4}{1} = 200\% \quad (2.2)$$

High pin efficiency of PAM signaling is achieved by sacrificing signal-to-noise ratio (SNR). For differential PAM-4 signaling, the pin efficiency is

$$\eta_{\text{PAM-4}} = \frac{\log_2 4}{2} = 100\% \quad (2.3)$$

as it transmits data over a pair of transmission lines to suppress common-mode noise.

For a desired data throughput, high pin efficiency system has low symbol rate as the symbol rate is expressed as

$$f_s = \frac{f_b}{\eta} \quad (2.4)$$

resulting in low insertion loss and Gaussian noise [5, 15].

2.2 *Signal Integrity*

Signal integrity (SI) refers to the quality of an electrical signal that propagate from transmitter to receiver through wireline channels [15, 16, 17, 18]. It is important to analyze and mitigate signal impairment such as distortion, jitter, and noise to ensure it remains reliable and accurate enough to be correctly interpreted by the receiving end. As high-speed wireline transceivers push toward 56 Gb/s, 112 Gb/s, and beyond using PAM4 or other state-of-art multi-level modulation, maintaining signal integrity across lossy and bandwidth-limited channels becomes a major bottleneck. With reduced eye height and increased levels per symbol, multi-level systems are inherently more sensitive to signal impairments. To ensure reliable data recovery and low bit error rates (BER), careful management of signal integrity impairments such as inter-symbol interference (ISI), thermal noise, and simultaneous switching noise (SSN) is essential across the entire communication channels [17, 6, 19].

ISI is smearing of signals to subsequent signals due to limited bandwidth of the transmission lines. This is particularly severe in high-speed systems where the signal bandwidth approaches the Nyquist frequency of the channel, and the channel exhibits frequency-dependent attenuation due to skin effect, dielectric loss, and reflections from impedance discontinuities. The problem becomes more acute with N-level signaling, where the minimum eye height is

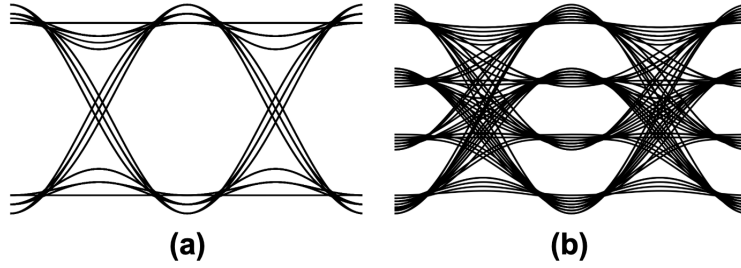


Figure 2.1: Eye diagrams with ISI: (a) NRZ signaling and (b) PAM4 signaling.

approximately $1/N$ that of an NRZ signal operating at the same peak-to-peak swing, making the receiver much more vulnerable to ISI-induced closure. Fig. 2.1 depicts eye diagrams with ISI of NRZ and PAM4. ISI manifests as vertical eye degradation and horizontal timing uncertainty, which significantly impacts timing margins. It is typically modeled as a convolution of the transmitted symbols with the impulse response of the channel, leading to deterministic amplitude and phase distortion. To mitigate ISI, transceivers employ a combination of analog and digital equalization techniques. Transmitter-side equalizers such as finite impulse response (FIR) filters pre-compensate for anticipated channel loss by boosting high-frequency components [20, 21]. On the receiver side, continuous-time linear equalizers (CTLE) [22, 23] provide frequency-dependent gain to amplify attenuated spectral components, while decision feedback equalizers (DFE) and feed-forward equalizers (FFE) in the digital domain attempt to cancel post-cursor and precursor ISI based on previous symbol decisions [24]. Adaptive algorithms can be used to calibrate equalizer coefficients to track changes in the channel due to voltage, temperature, or aging effects [23].

Noise in high-speed wireline systems originates from a variety of sources and is typically classified as either random or deterministic. Random noise, such as thermal noise and shot noise, and is generally modeled as additive white Gaussian noise (AWGN). Deterministic noise, on the other hand, includes crosstalk from neighboring lanes, reflections, duty-cycle distortion, quantization noise in ADCs, and deterministic jitter components like periodic jitter and data-dependent jitter. In multi-level transceivers, the small voltage margin between

adjacent levels means that even modest amounts of noise can cause symbol errors, especially when compounded with ISI. Noise tolerance is typically assessed through eye opening analysis, SNR calculations, and BER simulations. For systems targeting extremely low BERs (e.g., 10^{-12}), forward error correction (FEC) schemes are commonly employed to absorb errors induced by noise [25]. However, FEC latency and coding overhead impose constraints on system design and protocol compatibility. It is important to balance the trade-offs between noise margin, power consumption, and latency to meet specification requirements.

SSN arises when multiple drivers switch concurrently and inject large transient currents into the shared power delivery network (PDN). These currents flow through parasitic inductance and resistance in the power and ground paths, generating voltage fluctuations that can couple into sensitive nodes and degrade signal integrity. SSN is particularly challenging in high-density I/O systems, such as those used in high-bandwidth memory (HBM) and chiplet-based architectures [26, 27, 28]. As more lanes operate simultaneously at high speed, the aggregate current variation di/dt increases significantly, exacerbating the SSN impact on both data and clock channels. In multi-level signaling systems, where voltage margins are small and timing windows narrow, SSN can easily cause eye closure. The problem is further amplified by simultaneous activity across multiple dies, packages, and sockets, especially in vertically stacked or 2.5D/3D integrated systems. Several mitigation strategies have been developed to reduce SSN, including careful floorplanning to minimize simultaneous transitions, decoupling capacitor placement to stabilize PDN impedance, staggered launch techniques to desynchronize aggressor channels, and coding schemes such as 8B10B or Gray coding to limit the number of transitions per clock cycle [29, 30]. In transceivers with adaptive biasing or power gating, dynamic SSN suppression techniques may also be employed to reduce the magnitude of transient events [31].

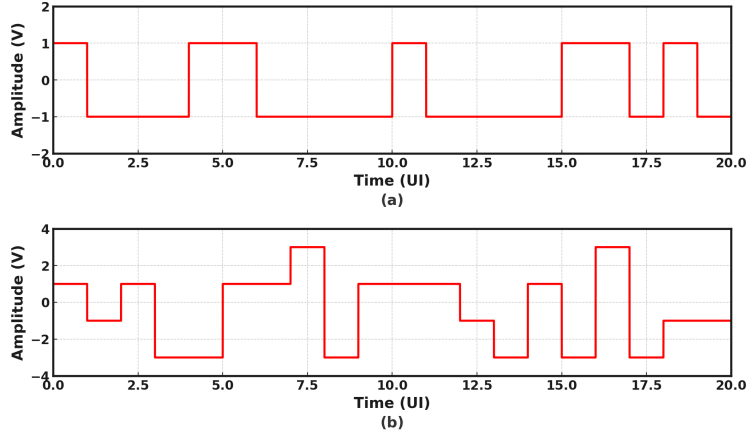


Figure 2.2: Signal waveforms of (a) NRZ signaling and (b) PAM4 signaling.

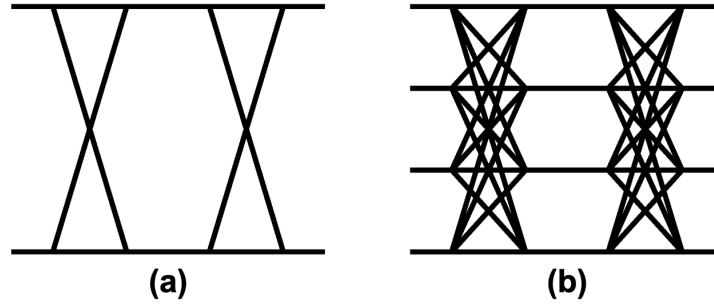


Figure 2.3: Eye diagrams of (a) NRZ signaling and (b) PAM4 signaling.

2.3 Line code

2.3.1 PAM

PAM has emerged as a significant signaling scheme in recent high-speed wireline links, particularly as data rates scale beyond 28 Gb/s [5, 32, 33, 6, 34, 35, 36]. Traditional NRZ (or PAM2) signaling encodes 1 bit per symbol, requiring a doubling of the symbol rate to increase the data rate. This leads to significant challenges in equalization and power consumption due to the increased Nyquist frequency. PAM4, on the other hand, encodes 2 bits per symbol by employing four amplitude levels, thereby doubling pin efficiency and the throughput for

the same symbol rate. Fig. 2.2 and Fig. 2.3 depicts the waveforms and eye diagrams of NRZ and PAM4 signaling. This effectively reduces the Nyquist frequency by half and alleviates channel bandwidth requirements. For instance, in a backplane channel designed for 28 Gb/s NRZ, operating at 56 Gb/s NRZ would require a Nyquist frequency of 28 GHz, where insertion loss can exceed 60 dB [5]. Such loss is well beyond the equalization capability of most transceivers. PAM4 signaling, however, confines the Nyquist frequency to 14 GHz at 56 Gb/s, resulting in a more manageable 31 dB loss. The adoption of PAM4 comes with several design challenges. The reduced vertical eye opening due to the compressed signal swing between adjacent levels increases the system's susceptibility to thermal noise, jitter, and ISI [37]. Transmitter linearity becomes critical, as level mismatches can further degrade the eye diagram [36]. To address this, metrics such as Ratio of Level Mismatch (RLM) are specified in standards to quantify acceptable deviations in level spacing. In the transmitter presented in [5], auxiliary current sources and cascode compensation are used to preserve amplitude linearity while maintaining power efficiency. At the receiver, the need to resolve four distinct voltage levels has driven the development of ADC-based architectures [5, 38]. These receivers typically include analog front-ends with continuous-time linear equalizers (CTLE) and automatic gain control (AGC), followed by high-speed time-interleaved ADCs and digital signal processing (DSP). The DSP performs feed-forward and decision-feedback equalization to mitigate ISI. For low-loss channels, fewer ADC bits and lower power are sufficient, while for high-loss environments, additional resolution and digital equalization can be engaged. Despite the increased complexity, PAM4 remains a key enabler for bandwidth-efficient and pin-limited interconnects. Its adoption has been solidified in standards such as OIF-CEI-56G [39], and its evolution continues with more advanced signaling schemes such as PAM8 [40, 41]. As pin efficiency becomes an increasingly important metric in multi-die and chiplet systems, PAM signaling provides a scalable path forward for high-throughput wireline transceivers.

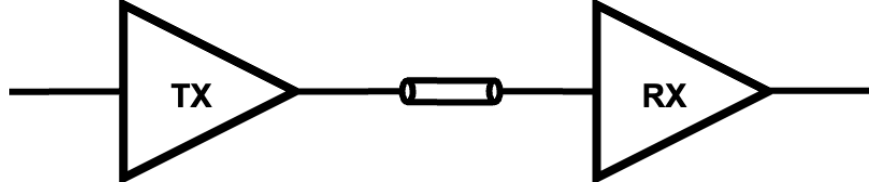


Figure 2.4: Single-ended communication system.

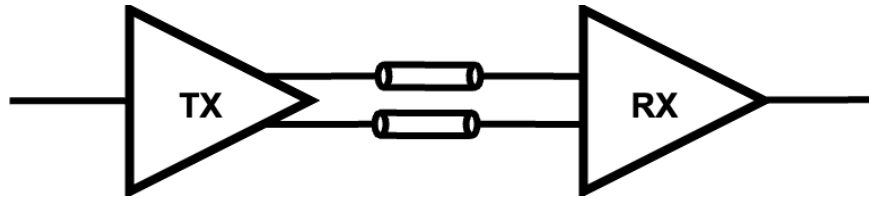


Figure 2.5: Differential communication system.

2.3.2 Single-ended and Differential Signaling

In single-ended signaling, each signal is referenced to a common ground. A voltage level on a single conductor represents the data, while the return current flows through the ground plane or return path. Fig. 2.4 illustrates a single-ended communication system. This scheme is simple and cost-efficient, making it common in low-to-moderate speed systems such as general-purpose I/O, parallel buses, and legacy DRAM interfaces. It also has higher pin efficiency and throughput than differential signaling as discussed in Section 1.1. However, as signaling frequencies increase, the shared return path can lead to severe issues related to SSN, common-mode noise and crosstalk between adjacent signal lines [42]. Because return currents follow the path of least impedance, any discontinuity or impedance mismatch in the ground path can degrade the signal quality due to increased loop area and common-mode noise injection [15].

Conversely, differential signaling transmits information using a pair of conductors with equal and opposite signals. Fig. 2.5 illustrates a single-ended communication system. The receiver senses the voltage difference between the positive and negative transmission lines,

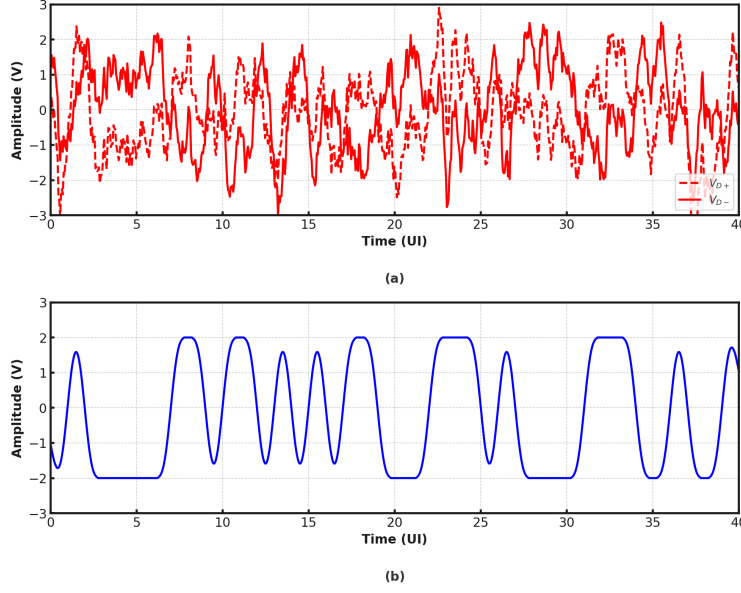


Figure 2.6: Differential signal waveforms with common-mode noise: (a) single-ended waveforms and (b) differential waveform.

which cancels out any noise that is common to both. Fig. 2.6 illustrates differential signal waveforms with common-mode noise. Fig. 2.6(a) shows the single-ended waveforms v_{D+} and v_{D-} , which can not be recovered correctly due to large common-mode noise. Fig. 2.6(b) shows the differential waveform. As can be seen, the common-mode noise is canceled in the differential waveform

$$\begin{aligned}
 v_{\text{Diff}} &= (v_{D+} + v_{\text{noise}}) - (v_{D-} + v_{\text{noise}}) \\
 &= v_{D+} - v_{D-}
 \end{aligned}$$

This property, known as common-mode noise rejection, makes differential signaling highly robust against power supply noise, electromagnetic interference (EMI), and SSN. Because the current flows in a closed loop between the two conductors, differential signaling naturally reduces loop area and radiated emissions, making it ideal for high-speed, high-density interconnects such as PCIe, SATA, USB, and HBM interfaces [43]. Differential signaling also supports smaller voltage swings (typically 200–800 mV peak-to-peak) and higher signaling

rates compared to single-ended I/O. These benefits come at the cost of increased routing complexity, power consumption, and layout constraints. Differential pairs must be tightly matched in length and spacing to preserve signal symmetry and minimize timing skew. Impedance control is also more stringent; typical differential impedance is designed to $100\ \Omega$ for differential termination, compared to $50\ \Omega$ for single-ended lines. One critical distinction between the two modes is their behavior under switching events. In single-ended systems, large numbers of simultaneously switching drivers can induce substantial voltage fluctuations on the shared ground and power planes, manifesting as SSN. In differential systems, because return currents are confined within the differential pair, the impact of switching noise is significantly attenuated. This makes differential signaling especially suitable for multi-gigabit links, where timing margins and jitter sensitivity are tight. Mode conversion is another challenge that differential signaling encounters [15]. Imperfections in differential trace routing, such as length mismatch or asymmetry, can cause a portion of the differential signal to convert into common-mode noise and vice versa. This not only increases susceptibility to interference but can also result in signal degradation and EMI violations. Proper layout practices, such as symmetric via design, careful return path continuity, and guard traces, are essential to minimize these effects.

2.3.3 *Permutation Coding*

Permutation coding has emerged as a promising approach to improve pin efficiency in high-speed parallel wireline transceivers [11, 2, 10, 9, 44]. It builds upon multi-level and multi-wire signaling techniques by leveraging the combinatorial properties of permutations to encode data with high efficiency, while simultaneously offering resilience to reference voltage noise and SSN.

The basic idea of permutation coding is to map groups of input bits to a specific permutation of a multi-level vector, known as the base code. Each permutation of the base code represents a unique symbol that can be transmitted across multiple wires in parallel. Fig. 2.7 shows an example waveform of four-level permutation coding over four wires (4B4W4L) [2].

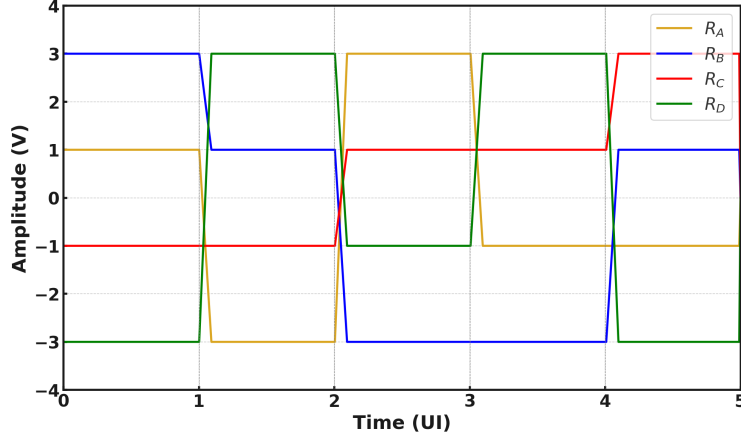


Figure 2.7: Permutation coding with four-level signals over four wires (4B4W4L).

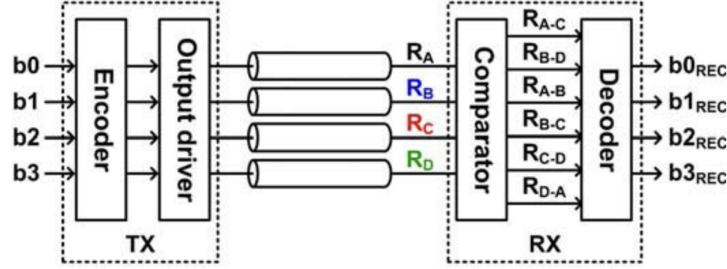


Figure 2.8: Transceiver architecture of 4B4W4L permutation coding [2].

In contrast to PAM signaling, where symbols are mapped to discrete amplitude levels and are sensitive to both ISI and reference voltage noise, permutation coding achieves relative encoding across wires. Since decoding relies solely on comparing the relative magnitudes of signals across wires rather than absolute levels, the receiver is inherently immune to common-mode disturbances and reference drift. This feature enables receivers without reference voltage. Fig. 2.8 shows 4B4W4L permutation coding transceiver architecture.

By carefully selecting the base code and the allowable permutations, permutation coding enables a larger number of unique symbols compared to conventional NRZ or PAM schemes,

thereby increasing pin efficiency. For example, a base code can be represented as a vector:

$$\text{Base Code: } B = [0, 1, 1, 2]$$

This base code yields a total of

$$C_{\max} = \frac{4!}{1! \cdot 2! \cdot 1!} = 12$$

unique permutations. The underlying base code typically contains multiple repeated elements, each representing a discrete signal level. The total number of distinct permutations available from a base code B with repeated elements is given by:

$$C_{\max} = \frac{n!}{m_1! \cdot m_2! \cdots m_k!}$$

where n is the total number of elements, k is the number of distinct amplitude levels, and m_i is the multiplicity of each level. The achievable pin efficiency is then determined by:

$$\eta_{\text{pin}} = \frac{\log_2 C_{\max}}{n} \cdot 100\%$$

For example, a 4-wire 3-level permutation coding scheme has been shown to achieve 75% pin efficiency while maintaining DC balance and low EMI [10]. Furthermore, permutation codes naturally balance wire activity by spreading energy uniformly across symbols.

Another important benefit of permutation coding lies in its support for symbol correlation. By correlating sequences of encoded symbols, additional redundancy can be exploited to enforce a minimum transition density—essential for reliable clock and data recovery (CDR) in embedded-clock systems. For instance, Lin et al. reported a 4-wire, 3-level permutation coding scheme that increased transition density from 75% (found in PRBS patterns) to 85.6% through symbol-level correlation, all without reducing throughput or bit efficiency [10]. This structured increase in transition events enables robust CDR without the need for dedicated clock lines, making permutation coding suitable for clock-embedded signaling architectures.

While permutation coding offers substantial advantages, it also introduces tradeoffs. The relative encoding reduces noise margin due to smaller signal level spacing, and the increased

complexity of permutation-based encoding and decoding may demand higher circuit overhead. Nonetheless, the lower required baud rate for a given data rate mitigates channel loss, and the robustness to noise and SSN often outweighs these drawbacks in bandwidth-constrained environments.

2.3.4 Chord Signaling

Chord signaling (CS) has emerged as a promising alternative to conventional signaling approaches by distributing information spatially across multiple wires using orthogonal transformations [3, 7, 8]. Chord signaling can be viewed as a generalization of differential signaling. While differential signaling encodes one bit across a two-wire pair (yielding 50% pin efficiency), chord signaling encodes n bits over $n + 1$ wires using orthogonal basis vectors, most commonly derived from the Walsh-Hadamard matrix. This spatial coding scheme ensures that each bit is reconstructed at the receiver using a linear combination of wire voltages, leveraging the orthogonality of the transformation to isolate each bit from the others. Fig. 2.9 shows an example of chord signaling, ensembled NRZ (ENRZ) signaling [3]. The transmitter in ENRZ communication system performs a orthogonal transformation: it takes three digital input bits, maps them into an $n + 1$ -dimensional analog signal vector using a Hadamard transform, and drives the result onto $n + 1$ physical wires. On the receiver side, the inverse Hadamard transform recovers the individual bits by projecting the received multi-wire vector back into the original bit space. This avoids the need for complex equalizers or high-resolution ADCs.

The pin efficiency of chord signaling is given by

$$\eta_{\text{CS}} = \frac{n}{n + 1} \times 100\% \quad (2.5)$$

The pin efficiency of ENRZ and CNRZ-5 are 75% and 83%, higher than 50% pin efficiency compared to conventional differential NRZ signaling. Another key advantage of chord signaling is its low sensitivity to ISI despite transmitting multi-level signals over channels [7]. In conventional PAM signaling, the signal-dependent ISI exacerbates as the number of lev-

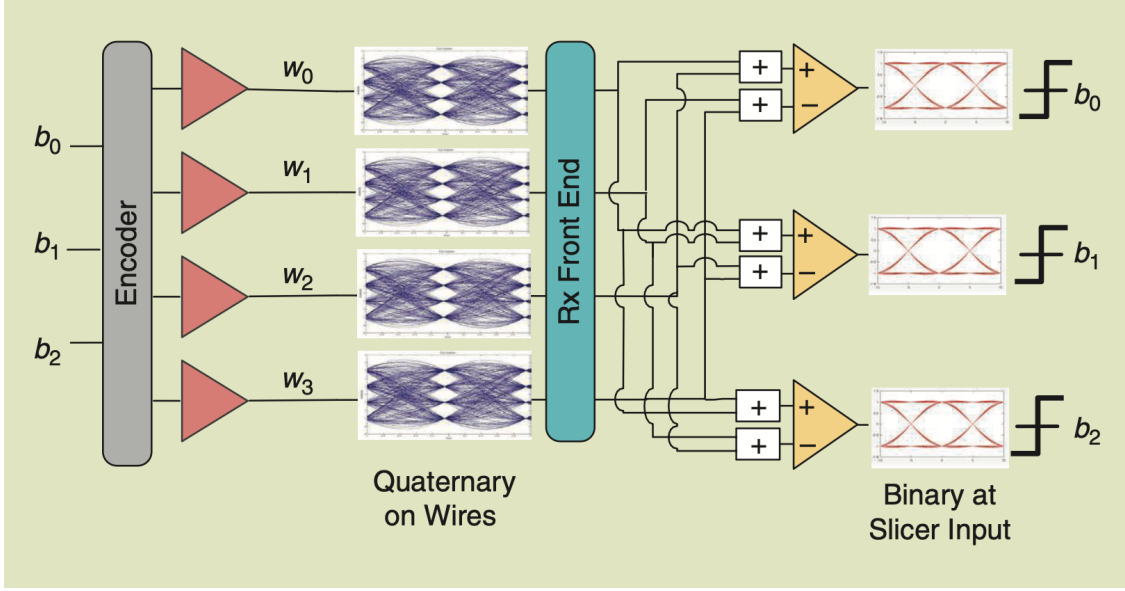


Figure 2.9: ENRZ transceiver architecture [3].

els increase and limits the scalability of bit rates. In contrast, chord signaling decodes the multi-level signals into NRZ signals before entering slicers, yielding an ISI ratio of 1.0. This property enables robust operation even in the presence of modest channel dispersion, greatly reducing the need for power-hungry adaptive equalization. Chord signaling also provides enhanced resilience to common-mode noise and crosstalk. Since the transmitted vector is balanced and often zero-sum, much like in differential signaling, the system inherently suppresses common-mode noise. In terms of energy efficiency, chord signaling compares favorably to PAM-based solutions. For example, ENRZ, a 3-bit 4-wire implementation, and CNRZ-5 (correlated NRZ), a 5-bit 6-wire variant, demonstrate data rates of up to 20 Gb/s per wire with excellent energy and area efficiency [3, 7]. Despite its many advantages, chord signaling does pose implementation challenges. The most significant challenge is sensitivity to inter-wire skew. Since decoding depends on matched arrival times across all wires, skew must be controlled within a small fraction of the unit interval. However, skew compensation circuits, either at the transmitter (e.g., calibrated delay buffers) or receiver (e.g., programmable phase

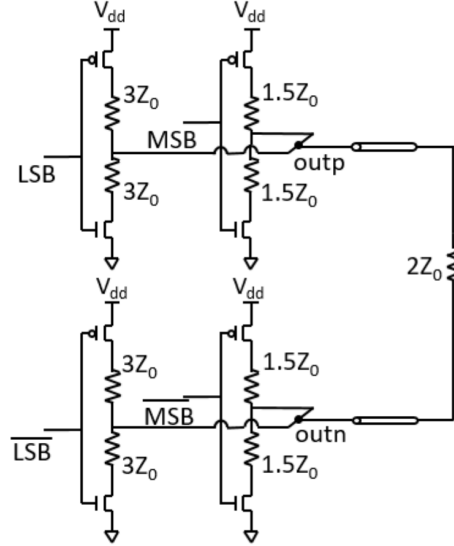


Figure 2.10: PAM4 SST driver schematic [4].

interpolators), can mitigate this issue without significant overhead.

2.4 Multi-level Transceivers

The growing demand for bandwidth in high-performance computing and communication systems has driven the adoption of multi-level signaling schemes such as PAM and CS. These schemes improve bandwidth efficiency without a proportional increase in channel count or clock rate, but they also present new challenges in transmitter and receiver design. This section introduces the architecture and circuit-level considerations for such high-speed multi-level transceivers.

At the transmitter side, voltage-mode SST drivers are widely used in multi-level wireline links due to their superior linearity and energy efficiency compared to current-mode logic (CML) drivers [4]. SST drivers achieve impedance matching by placing resistors in series with the signal path, simplifying integration and reducing power consumption. Fig. 2.10 illustrates SST driver schematic for PAM4 transmitter. The driver consists of two binary-

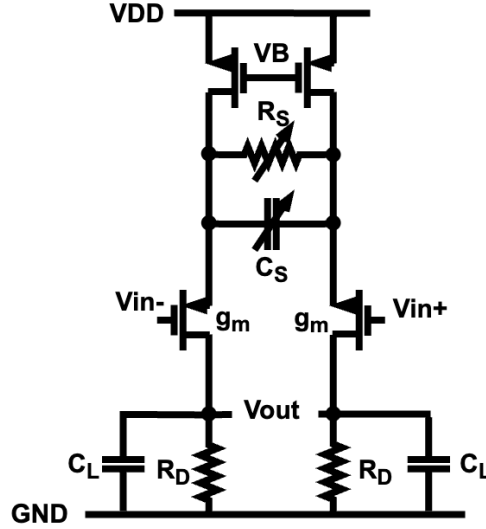


Figure 2.11: Fully differential active CTLE schematic.

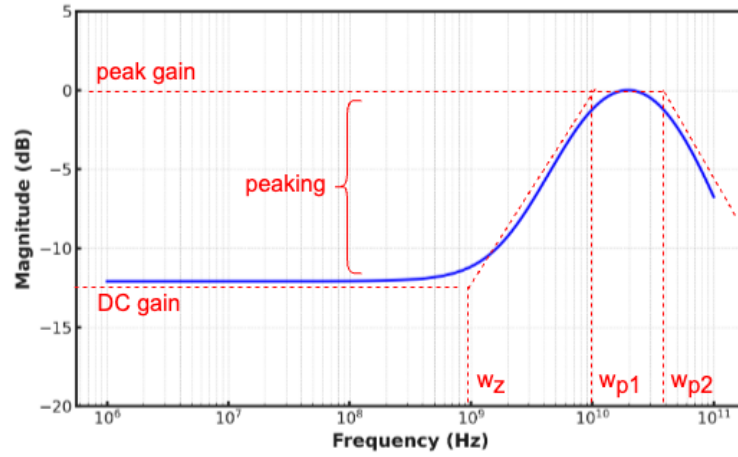


Figure 2.12: Fully differential active CTLE frequency response.

weighted slices connected in parallel. Each slice is controlled by MSB and LSB of a PAM4 signal.

To combat high-frequency loss and ISI in electrical channels, multi-level receivers typically incorporate a CTLE as the analog front-end block [5, 6, 33, 38]. The CTLE is a programmable

analog filter that provides peaking gain to compensate for channel-induced high-frequency attenuation [15]. A well-tuned CTLE can significantly increase eye opening before slicing, enabling robust operation over a wide range of channel conditions without excessive analog complexity. Fig. 2.11 shows a widely used fully differential active CTLE schematic [45]. Unlike passive CTLEs that rely solely on resistive-capacitive (RC) networks, active CTLEs introduce transconductance and tunable impedance elements to provide additional gain and control over the peaking response. As illustrated in Fig. 2.11, it consists of a differential pair with resistive and capacitive source degeneration and load resistors. The transfer function of the CTLE can be expressed as:

$$H(s) = \frac{g_m}{C_p} \cdot \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + \frac{g_m R_S}{2}}{R_S C_S}\right) \left(s + \frac{1}{R_D C_p}\right)} \quad (2.6)$$

This structure introduces a zero at $\omega_z = \frac{1}{R_S C_S}$, and two poles at $\omega_{p1} = \frac{1 + \frac{g_m R_S}{2}}{R_S C_S}$ and $\omega_{p2} = \frac{1}{R_D C_p}$. The zero boosts high-frequency gain, while the poles define the bandwidth and peaking behavior of the CTLE. The DC gain and ideal peak gain are given respectively by:

$$\text{DC gain} = \frac{g_m R_D}{1 + \frac{g_m R_S}{2}} \quad (2.7)$$

$$\text{Ideal peak gain} = g_m R_D \quad (2.8)$$

Thus, the ideal peaking factor, defined as the ratio of peak gain to DC gain, is:

$$\text{Ideal Peaking} = \frac{\omega_{p1}}{\omega_z} = 1 + \frac{g_m R_S}{2} \quad (2.9)$$

Increasing R_S reduces ω_z and boosts the peaking and equalization strength. Increasing C_S reduces both ω_z and ω_{p1} and adjust the shape of frequency response.

Following the CTLE, advanced receiver architectures leverage high-speed ADCs to digitize the incoming signal for further equalization in the digital domain [5, 38]. The ADC digitizes the signal equalized by CTLE at the symbol rate, enabling flexible digital signal processing (DSP) for equalization and error correction. ADC-based architectures allow for

sophisticated adaptive equalization strategies (e.g., DFE and FFE) and integration with DSP-based CDR schemes. They also eliminate the analog slicer, enhancing scalability to higher modulation levels. Despite their flexibility, ADC-based receivers face power and linearity challenges, especially at higher sampling rates and resolutions. Efficient interleaving, low-noise front-ends, and clock calibration techniques are critical to enable energy-efficient implementations. Recent works such as Im *et al.* [32] have shown that ADC-based PAM4 receivers can achieve 112 Gb/s throughput with low BER using a 36-way interleaved SAR ADC and inverter-based front-end amplifiers.

Chapter 3

PIN-EFFICIENT 12-BIT 8-WIRE 8-LEVEL PERMUTATION CODING FOR PARALLEL WIRELINE TRANSCEIVERS

3.1 Introduction

As CMOS process technology improves, the on-chip operation frequency increases rapidly, which naturally leads to the demand of increasing I/O data rates. While CMOS technology scales as Moore's law, printed circuit board (PCB) technology does not scale at the same rate. The increasing gap between CMOS technology and PCB technology limits the number of chip I/O pins [46]. The contradiction between I/O pin density and bandwidth therefore urgently calls for pin-efficient signaling for wireline transceivers. Many recent researches focus on improving the data rate and pin efficiency at the same time.

Pin efficiency is defined as the ratio of the bits of data transferred at each clock cycle and the number of pins used to transfer the data. The pin efficiency of NRZ signaling is 50% since it transmits one bit of data over two wires. Single-ended signaling uses one wire to transmit one bit of data, achieving 100% pin efficiency. However, it suffers from common-mode noise and requires accurate reference voltage shared by each link. Due to high frequency noise coupled from input data, it is hard to maintain an accurate and stable reference voltage. The four-level pulse-amplitude modulation (PAM4) then doubles the pin efficiency to 100%, since each symbol contains two bits of data. However, PAM4 signaling suffers from SSN on power supply and ground of the output driver at the transmitter side, which is caused by the rapid input-dependent transitions at the output of the transmitter [46, 47, 48]. This simultaneous switching noise becomes even worse as the link density increases such as in memory interface. Permutation coding [47, 46, 49, 50, 48] reported recently can improve pin efficiency to 75%-100%. It also eliminates EMI since the total output current of the

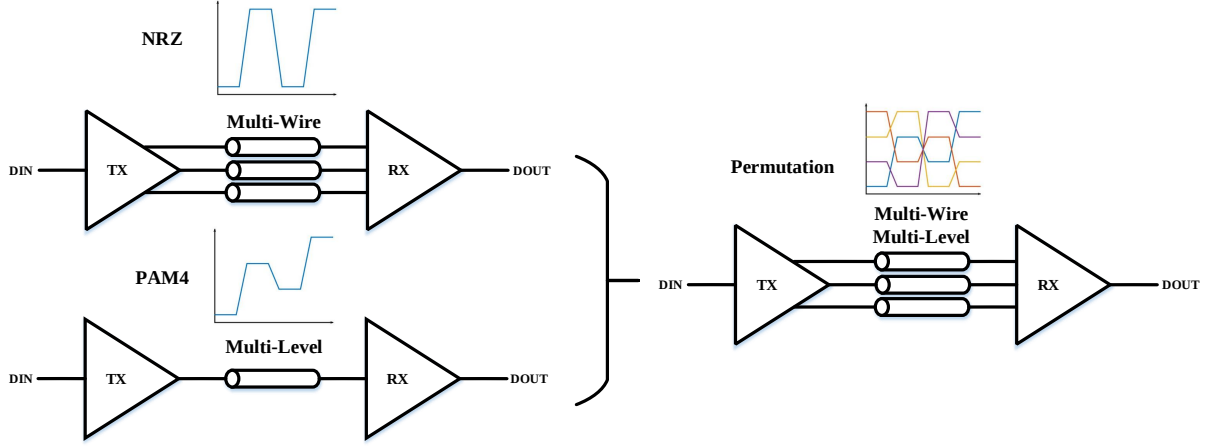


Figure 3.1: NRZ, PAM4 and permutation coding.

transmitter driver is constant [48].

To achieve higher data rate by increasing pin efficiency, we designed a 12-bit 8-wire 8-level permutation coding [12]. The proposed coding scheme achieves pin efficiency of 150%, 3x of NRZ signaling. With the same data rate, it can reduce the baud rate to 1/3 of conventional NRZ signaling, which results in decreased ISI. Thus it compensates for reduced noise margin due to 8-level signaling in each wire. The 12B8W8L-PC also saves 80% of energy in terms of signaling compared to NRZ. When transmitting 12-bit data, 12B8W8L-PC consumes 32 units of energy by sending 8-level symbols through 8 wires. NRZ signaling consumes 168 units of energy by sending binary symbols through 24 wires when the output voltage range is the same as 12B8W8L-PC. In addition, the encoding and decoding logics of the proposed coding are simple and consume much less energy than signaling. Besides, the 12B8W8L-PC intrinsically eliminates SSN, EMI and common-mode noise. A wireline transceiver adopting the proposed coding scheme is designed in a 65nm CMOS process. FR4 microstrip lines and on-chip silicon striplines are designed and simulated in electromagnetic tools. The transceiver operates at 6Gb/s/pin data rate and consumes 0.79pJ/b energy efficiency over the above transmission lines.

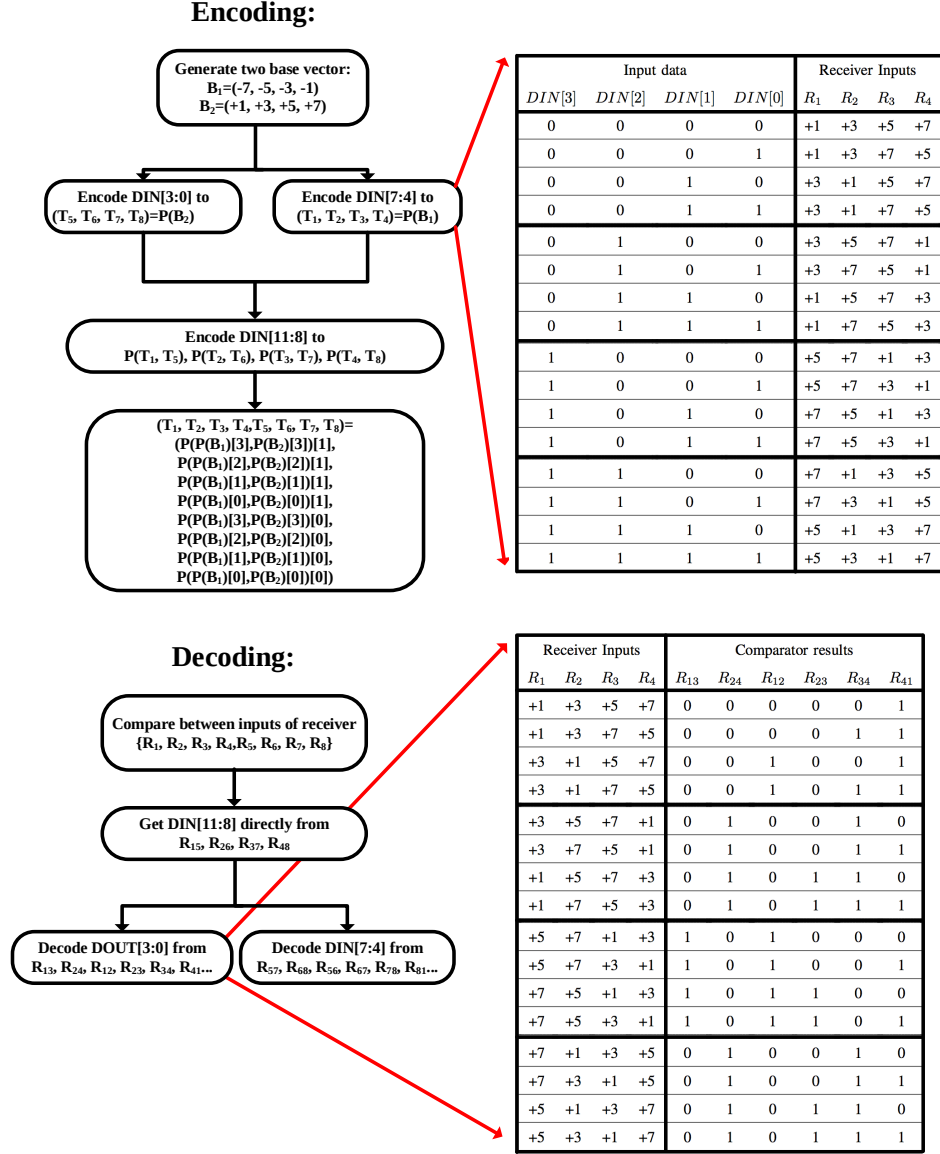


Figure 3.2: Encoding and decoding process of the proposed coding scheme.

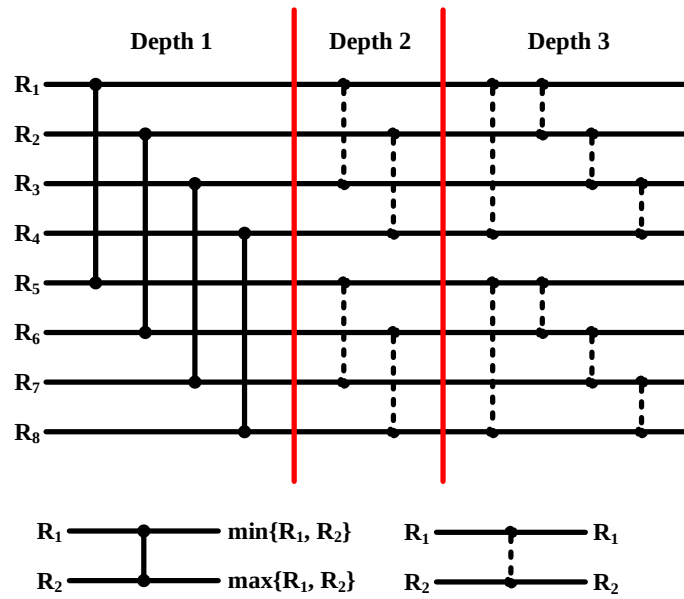


Figure 3.3: Sorting network of decoding process.

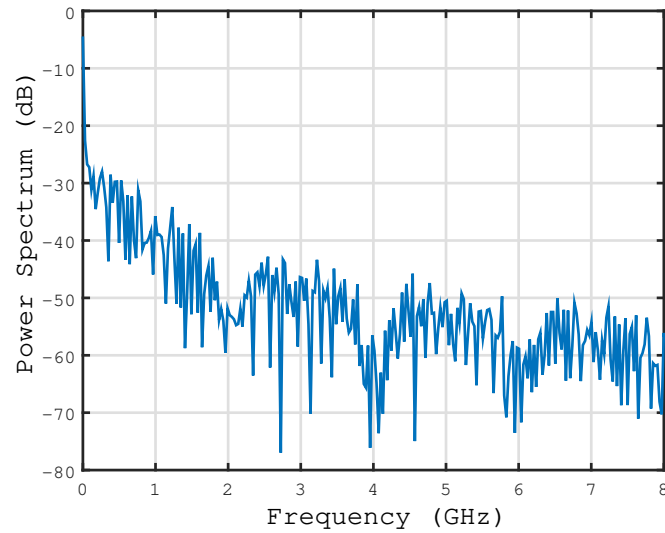


Figure 3.4: 6Gb/s/pin Proposed 12B8W8L permutation coding.

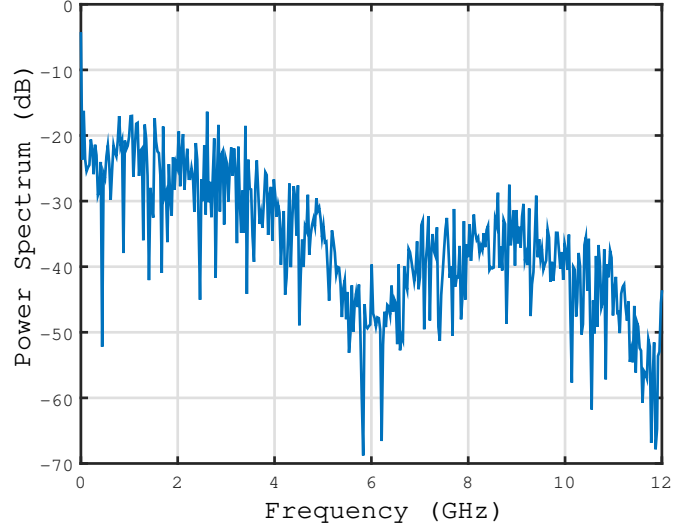


Figure 3.5: Power spectrums of 6Gb/s/pin NRZ signaling.

3.2 12-Bit 8-Wire 8-Level Permutation Coding

3.2.1 Permutation Codes

To start with, a brief review of permutation coding is provided. Permutation coding in wireline communication is used in most of the multi-wire-multi-level link systems reported recently. In Fig. 3.1, a multi-wire (MW) link system, a multi-level (ML) link system and a multi-wire-multi-level (MWML) link system are illustrated. S_1 shows a MW link system using NRZ signaling where each pair of wires are independently transmitted. S_2 is a ML link system that is promising when data rate is high. A MWML system is illustrated in S_3 where permutation coding are used. Different from MW systems, the input data are jointly coded. It transmits multi-level symbols in each wire to map input data to a unique sequence

of a base code. The base code B is defined as

$$\begin{aligned}
 B = & (d_{11}, d_{12}, \dots, d_{1m_1}, \\
 & d_{21}, d_{22}, \dots, d_{2m_1}, \\
 & \dots \\
 & d_{k1}, d_{k2}, \dots, d_{km_k})
 \end{aligned} \tag{3.1}$$

where d_{ij} is an element of the base code, and

$$\begin{aligned}
 d_{i1} &= d_{i2} = \dots = d_{im_i}, \quad i = 1, 2, \dots, k \\
 d_{11} &\neq d_{21} \neq \dots \neq d_{k1}
 \end{aligned} \tag{3.2}$$

representing B has k distinct elements d_{i1} and each of them repeated m_i times. The total number of elements in the base code is

$$n = m_1 + m_2 + \dots + m_k \tag{3.3}$$

3.2.2 Proposed 12B8W8L-PC

In the proposed 12B8W8L-PC, twelve bits of input data are transmitted across eight pins using 8-level signaling. The base code $\mathbf{B}_1$ is

$$B_1 = (-7, -5, -3, -1, +1, +3, +5, +7) \tag{3.4}$$

and $m_1 = \dots = m_7 = 1$, $n = k = 8$. The maximum number of codewords is

$$C_{max} = \frac{n!}{m_1!m_2!\dots m_k!} = 40320 \tag{3.5}$$

while only 4096 permutation codes are chosen to simplify the encoder and the decoder logic, *i.e.* $C = 4096$.

The encoding process is composed of three steps. Each step deals with four bits of input data. The 12-bit input data and the output vector of the encoder are denoted as $DIN[11:0]$ and $P_t(B)$, respectively. The expression of $P(B)$ is

$$P_t(B) = (T_1, T_2, T_3, T_4, T_5, T_6, T_7, T_8) \tag{3.6}$$

The encoding process is as follows:

1. Four bits of input data $DIN[3:0]$ are encoded to (T_1, T_2, T_3, T_4) . (T_1, T_2, T_3, T_4) is the permutation code of the base code $(+1, +3, +5, +7)$. Mapping rules are illustrated in Fig. 3.2.
2. Another four bits of input data $DIN[7:4]$ are encoded to (T_5, T_6, T_7, T_8) by permuting the base code $(-7, -5, -3, -1)$. Mapping rules are the same as the first step.
3. Last four bits of input data $DIN[11 : 8]$ are encoded by interchanging each element from (T_1, T_2, T_3, T_4) with corresponding element from (T_5, T_6, T_7, T_8) . For example, assume $(T_1, T_2, T_3, T_4) = (+1, +3, +5, +7)$ and $(T_5, T_6, T_7, T_8) = (-7, -5, -3, -1)$. If $DIN[11]$ is zero, then no interchanging between T_1 and T_5 happens. So the encoded data $P_t(B) = (+1, +3, +5, +7, -7, -5, -3, -1)$. If $DIN[11]$ is one, then we interchange the value of T_1 with T_5 . So the encoded data are $(-7, +3, +5, +7, +1, -5, -3, -1)$.

The encoding logic of T_1 is as follows:

$$\begin{aligned}
 A[7] &= \overline{DIN[11]} \cdot \overline{DIN[3]} \cdot \overline{DIN[2]} \oplus \overline{DIN[1]} \\
 A[6] &= \overline{DIN[11]} \cdot \overline{DIN[3]} \cdot \overline{DIN[2]} \otimes \overline{DIN[1]} \\
 A[5] &= \overline{DIN[11]} \cdot \overline{DIN[3]} \cdot \overline{DIN[2]} \oplus \overline{DIN[1]} \\
 A[4] &= \overline{DIN[11]} \cdot \overline{DIN[3]} \cdot \overline{DIN[2]} \otimes \overline{DIN[1]} \\
 A[3] &= \overline{DIN[11]} \cdot \overline{DIN[7]} \cdot \overline{DIN[6]} \oplus \overline{DIN[5]} \\
 A[2] &= \overline{DIN[11]} \cdot \overline{DIN[7]} \cdot \overline{DIN[6]} \otimes \overline{DIN[5]} \\
 A[1] &= \overline{DIN[11]} \cdot \overline{DIN[7]} \cdot \overline{DIN[6]} \oplus \overline{DIN[5]} \\
 A[0] &= \overline{DIN[11]} \cdot \overline{DIN[7]} \cdot \overline{DIN[6]} \otimes \overline{DIN[5]}
 \end{aligned} \tag{3.7}$$

where $A[7:0]$ are control signals generating T_1 .

Decoding is realized by comparing 8-level input signals followed by relatively simple decoding logic. Similar to encoding scheme, decoding process is composed of three steps.

Each step recovers four bits of transmitted data. The signals received at the receiver side are denoted as $P_r(B)$, whose expression is

$$P_r(B) = (R_1, R_2, R_3, R_4, R_5, R_6, R_7, R_8) \quad (3.8)$$

The decoding process is as follows:

1. $DOUT[11:8]$ are recovered directly from comparison results $R_{15}, R_{26}, R_{37}, R_{48}$. Here R_{15} is the comparison result of R_1 and R_5 .
2. $DOUT[3:0]$ are decoded from comparator results listed in Fig. 3.2. The decoding logic of $DOUT[3]$ is

$$\begin{aligned} DOUT[3] = & R_{13} \cdot \overline{DOUT[11]} \cdot \overline{DOUT[9]} \\ & + R_{17} \cdot \overline{DOUT[11]} \cdot DOUT[9] \\ & + R_{53} \cdot DOUT[11] \cdot \overline{DOUT[9]} + \\ & + R_{37} \cdot DOUT[11] \cdot DOUT[9] \end{aligned} \quad (3.9)$$

3. Decoding of $DOUT[7:4]$ is similar to $DOUT[3:0]$. The decoding logic of $DOUT[7]$ is

$$\begin{aligned} DOUT[7] = & R_{57} \cdot \overline{DOUT[11]} \cdot \overline{DOUT[9]} \\ & + R_{53} \cdot \overline{DOUT[11]} \cdot DOUT[9] \\ & + R_{17} \cdot DOUT[11] \cdot \overline{DOUT[9]} \\ & + R_{13} \cdot DOUT[11] \cdot DOUT[9] \end{aligned} \quad (3.10)$$

This decoding technique requires 28 comparators in total. To reduce the number of comparators, an alternative three-stage decoding algorithm is introduced below.

An alternative decoding algorithm is based on Batcher's odd-even mergesort as illustrated in Fig. 3.3. In this sorting network, each solid vertical line connecting two signals represents a compare-and-swap unit, while each dotted vertical line represents a comparator. If a pair

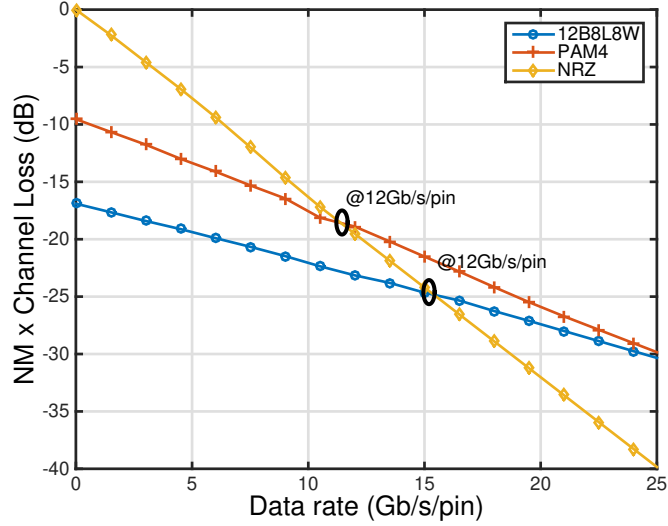


Figure 3.6: NM x Channel loss of NRZ, PAM4 and 12B8W8L signaling on 9-inch FR4 link.

of wires are connected by a solid vertical line, the compare-and-swap unit first compare the values and swap them if the bottom wire's value is smaller than the top wire's value. In the first stage of the decoding algorithm, $DOUT[11:8]$ are decoded directly from R_{15} , R_{26} , R_{37} , and R_{48} , respectively. In second stage, $DOUT[7:6]$ and $DOUT[3:2]$ are decoded directly from R_{57} , R_{68} , R_{13} , and R_{24} , respectively. In third stage, $DOUT[5:4]$ and $DOUT[1:0]$ are decoded based on R_{56} , R_{78} , R_{12} , and R_{34} . The decoding logic of $DOUT[1]$ is

$$\begin{aligned}
 DOUT[1] = & R_{12} \cdot \overline{DOUT[3]} \cdot \overline{DOUT[2]} \\
 & + \overline{R_{34}} \cdot \overline{DOUT[3]} \cdot DOUT[2] \\
 & + \overline{R_{12}} \cdot DOUT[3] \cdot \overline{DOUT[2]} \\
 & + R_{34} \cdot DOUT[3] \cdot DOUT[2]
 \end{aligned} \tag{3.11}$$

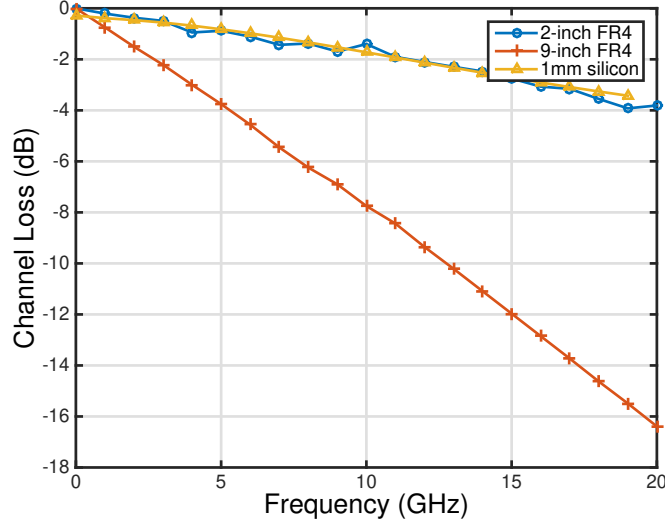


Figure 3.7: Channel loss of FR4 microstrip and on-chip stripline links.

3.2.3 Analysis of 12B8W8L-PC

In this section, we will calculate important characteristics of 12B8W8L-PC and compare it with other signaling. Pin efficiency can be calculated by

$$\eta = \frac{\log_2 C}{n} \cdot 100\% \quad (3.12)$$

where C is the number of codewords and n is the length of each codeword. The maximum pin efficiency of the 8-wire 8-level permutation coding scheme is $\eta_{max} = 191\%$. Since the proposed coding has 4096 codewords, its pin efficiency is $\eta = 150\%$. Because the permutation coding transmits multi-level symbols, it actually transmits more information than NRZ signaling. Therefore, the permutation coding can improve the pin efficiency.

The baud rate is defined as how many symbols are transmitted at each second. Thus baud rate is limited by the bandwidth of the link.

$$R_{Bd} \leq BW \quad (3.13)$$

Table 3.1: Comparison of NRZ, PAM-4, and Permutation Coding

Signaling	NRZ	PAM-4	PC (k, n=4)	PC (n=k)
Number of parallel links	4	4	4	n
Capacity	16	256	24	$n!$
Data Rate@baud rate= R_{Bd}	$0.5R_{Bd}$	R_{Bd}	$1.15R_{Bd}$	$\frac{\log_2(n!) \cdot R_{Bd}}{n}$
Pin Efficiency	50%	100%	115%	$\frac{\log_2(n!)}{n}$
Noise Margin@output range=1	1	0.33	0.33	$\frac{1}{n-1}$
Pin Efficiency/Noise Margin	0.5	3	3.44	$\frac{(n-1) \cdot \log_2(n!)}{n}$
Simultaneous Switching Noise	No	Yes	No	No
Reference voltage	No	Yes	No	No

The data rate, i.e. bit rate of each link is

$$R_b = R_{Bd} \cdot \eta \quad (3.14)$$

The data rate of the proposed coding is

$$R_b = 1.5R_{Bd} \quad (3.15)$$

For NRZ signaling, since the pin efficiency is 50%, the maximum data rate is half of the bandwidth of the link. However, since the permutation coding can achieve a better pin efficiency, it can push the maximum data rate further than NRZ signaling. Fig. 3.4 shows the power spectrum of the proposed coding scheme with a data rate of 6Gb/s/pin. The majority of the signal power is in 2GHz since the baud rate is 2GBd. Fig. 3.5 shows the

power spectrum of NRZ with a data rate of 6Gb/s/pin. The majority of the signal power is in 6GHz since the baud rate is 6Gb/s.

Since a permutation coding carries multi-level signals, it tends to shrink noise margin. Here we define noise margin as the distance between adjacent signal levels

$$NM = 20\log \frac{\max\{d_{ij}\} - \min\{d_{ij}\}}{k - 1} \quad (3.16)$$

where k denotes the number of distinct values in the base code. From Eq. (16) we can see that in order to achieve the same noise margin as NRZ signaling, multi-level signaling should increase the output range. The noise margin of 12B8W8L-PC is

$$NM = 20\log \frac{V(+7) - V(-7)}{7} \quad (3.17)$$

where $V(+7)$ and $V(-7)$ are the maximum and minimum voltages of 12B8W8L-PC. When the output range $V(+7) - V(-7)$ is the same as NRZ signaling, the noise margin of the proposed permutation coding is only 1/7 of the NRZ signaling, which would degrade its SNR. However, when the data rate is the same, the proposed coding scheme only requires 1/3 baud rate of the NRZ signaling. Therefore it suffers from smaller channel loss. When the channel loss is large enough, it will compensate for the noise margin. Fig. 3.6 illustrates different trends of $NoiseMargin \times ChannelLoss$ of NRZ, PAM4 and proposed 12B8W8L coding. The channel loss of the 9-inch FR4 link used here is shown in Fig. 3.7. According to the figures, when the data rate is less than 7Gb/s/pin, NRZ signaling achieves best figure of merit. However, as the data rate increases, the PAM4 and the 12B8W8L coding exceeds the NRZ signaling. The proposed coding scheme has the best performance in terms of $NoiseMargin \times ChannelLoss$ when the data rate is higher than 16Gb/s/pin.

Table. 3.1 compares the property of 4-wire NRZ, 4-wire PAM-4, 4-wire 4-level permutation coding and n-wire n-level permutation coding. Data rate shows that when transmitting the same amount of symbols at each clock cycle, how many bits of input data are actually transmitted. The noise margin is calculated with $\max\{d_{ij}\} - \min\{d_{ij}\} = 1$. As can be seen from the table, the permutation coding has a relatively higher data rate, higher pin efficiency but smaller noise margin. In other words, the permutation coding makes a tradeoff

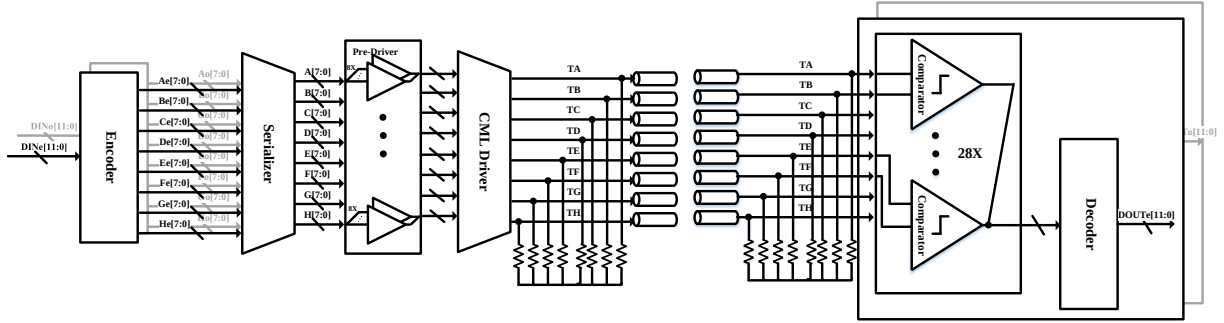


Figure 3.8: Circuit architecture of the proposed transceiver circuit.

between noise margin and pin efficiency. If the permutation coding and NRZ signaling have the same data rate, the permutation coding needs lower baud rate than NRZ signaling. As a result, the channel loss of permutation coding is smaller and compensates for the loss of noise margin. The beauty of permutation coding schemes is that for each code in $P(B)$, the sum of all the elements is constant. Therefore, it distributes the energy evenly among each code. As a result, the variation of the driving current becomes theoretically zero, eliminating the $L(di/dt)$ switching noise. The decoding of permutation coding is realized by comparing between elements of each code and sort the order of the code. This means that the receiver only cares about the relative values of each elements instead of the absolute values. Thus, the receiver is immune to common mode noise and a single-ended implementation becomes a promising option. Besides, unlike PAM signaling, the receiver of $P(B)$ does not require any reference voltage since it compares between elements. Therefore it eliminates signal degradation due to reference voltage noise.

3.3 Circuit Implementation

A transceiver circuit is designed in a 65nm CMOS process to demonstrate the proposed encoding scheme. The block diagrams of the transmitter and receiver circuits are shown in Fig. 3.8. To relax the timing constraints and achieve high data rate, a half rate architecture

with two clock phases is adopted. As can be seen in Fig. 3.8, the transmitter consists of an encoder, a 2-to-1 multiplexer, pre-drivers, and a pull-up pull-down current-mode logic driver. First, the input data feeds into the encoder to generate 8×8 control signals for the current-mode logic driver. Next, a 2-to-1 multiplexer serializes two sets of control signals for current-mode logic driver and doubles the data rate. The full rate control signals then flow through pre-drivers and switches the current-mode driver to generate eight-level voltages. Termination is done both at the transmitter and the receiver. Fig. 3.8 depicts the block diagram of the receiver. The input signals of the receiver flow into two sets of twenty-eight comparators. Four bits of recovered data are obtained directly from the comparison results, while the other 8 bits are obtained from the following decoder. The output DC eye-opening is $50mV$ and the output range of the current-mode logic driver is $350mV$.

The output driver at the transmitter side is shown in Fig. 3.9. It consists of four current paths and each path contains two current sources to generate two output voltages. Each current source is connected to eight switches so that it can be connected to any link among eight links. According to the input signals, each current sources will be connected to only one link and generate a specific permutation of output voltages. Four current paths generate eight levels of output voltage, dissipating 50% less current compared to pull-down drivers. The common mode node voltage remains at a constant voltage value if the current sum of eight current sources is zero. Mismatch between pull-up and pull-down driving strength will result in shifting of common mode voltage. If the driving strength of the pull-up network is stronger than the pull-down network, then the common mode voltage will shift toward V_{DD} so that the pull-up current is reduced to match the sum of pull-down current. Therefore, it is important to match the currents of two current sources. A four-bit binary calibration is applied to each current source to match the currents. Besides, cascode current source is used to maintain the common mode voltage at a constant level. The termination resistor R_T and the current I are chosen as 50Ω and $1mA$ respectively.

A capacitive pre-emphasis equalizer is adopted to reduce inter-symbol interference. Since it has a DC gain of one no amplifier is required. Compared to time-discrete de-emphasis

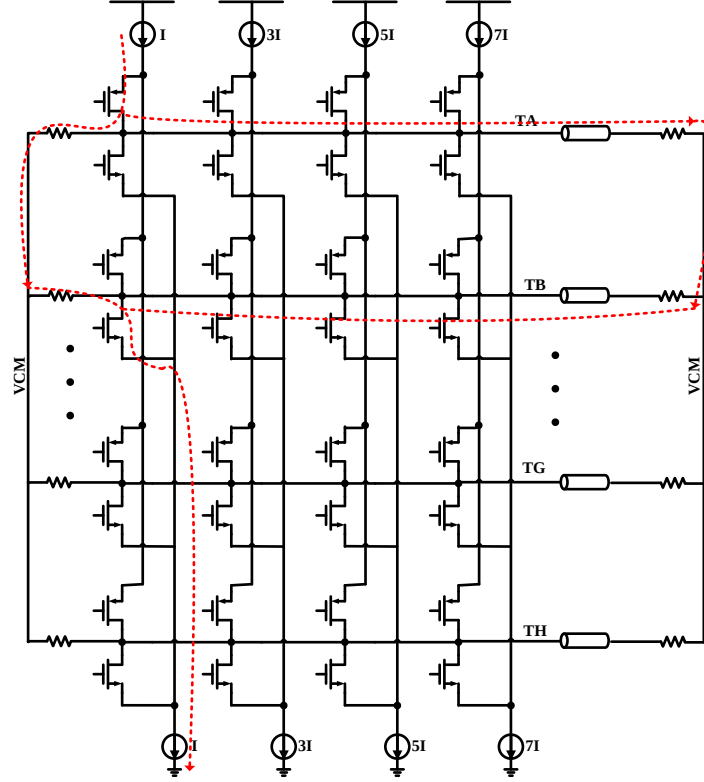


Figure 3.9: Circuit diagram of current-mode logic driver.

scheme, it does not require high speed flip-flops as delay units. The pre-emphasis equalizer has a coefficient generator and a voltage-mode equalizer. The voltage-mode equalizer consists of seven identical high-pass filters and each filter is formed by an inverter connected in series with a capacitor. The coefficient generator controls how many voltage-mode equalizers are enabled. The pre-emphasis equalizer is connected in parallel with the output driver. During each transition, the equalizer will provide current that proportional to the difference of the output voltages between consecutive two clock cycles. In order to get efficient equalization,

the entire delay of the equalizer, including the coefficient generator and the voltage-mode equalizer, should match the delay of the pre-driver and the current-mode logic driver. To get an adjustable equalizer strength, a 4-bit thermometer code is used to control it.

Twenty-eight comparators are used for receiver to compare different input voltages transmitted from the link. In order to reduce the kick-back noise, a dynamic comparator without tail current source is adopted for this work. The offset calibration is done by 3-bit binary code with a resolution of 5mV. The output of the comparator is saved in a SR latch to synchronize with the following pipelined digital circuit.

True single-phase clock(TSPC) flip flop is adopted for pipelined encoder and decoder. The TSPC flip flop is composed of three stages. The first stage is a pre-charge stage. This stage is transparent when clock is low, which means that the node X is updated with the value of D only when clock is low. The second stage is a latch stage. This stage stores the value of node X at the rising edge of clock signal. When clock is low, node Y is pre-charged to VDD. Then, when the rising edge of clock signal comes, node Y will be updated to GND if node X is high. When clock is high, no matter what the value of X is, the value at Y can not be modified. The third stage is another pre-charge stage. Different from the first stage, it is transparent when clock is high. This stage propagates node Y only when the clock signal is high.

3.4 Post-Layout Simulation Result

To test the transceiver circuit, two 12-bit pseudo-random binary sequence(PRBS-12) generators are implemented to produce input data for the transceiver. Four-inch FR4 links with channel loss shown in Fig. 3.7 are used during simulation. The bit error rate (BER) was measured at the receiver by comparing decoded input data with the outputs from pseudo-random binary sequence generators. At 2GHz clock frequency with 10 ps RMS random jitter, the proposed transceiver achieves 8×6 Gb/s/pin data rate with 10^{-4} BER. The eye diagram is shown in Fig. 3.10. The baud rate is 4GBd and the smallest eye opening is 70 ps and 37 mV horizontally and vertically. The eye-diagram is asymmetric because of different

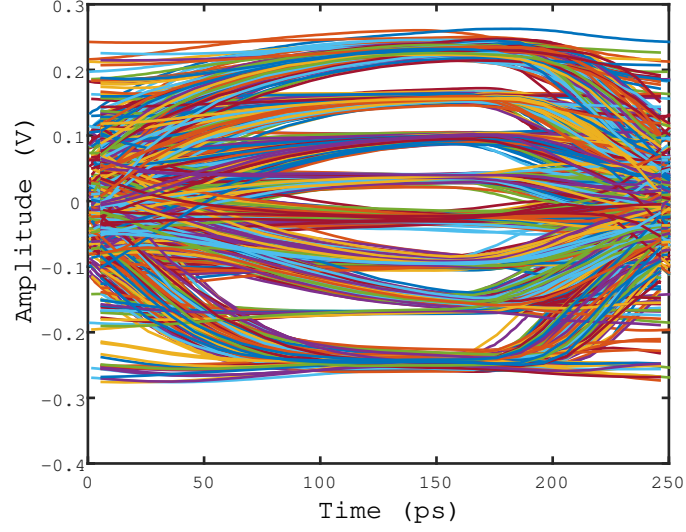


Figure 3.10: Eye-diagram of the proposed transceiver circuit with random jitter of 10ps rms.

Table 3.2: Performance Summary

Reference	[48] JSSC 2016	[50] ISSCC 2016	This work
Coding scheme	4B4W4L	5B6W4L	12B8W8L
Technology	65 nm	28 nm	65 nm
Power supply	1.2V	1V/1.5V	1.2V
Channel	2" FR4	5-24 mm MCM	4" FR4
Pin efficiency	100%	83%	150%
Data rate	8 Gb/s/pin	20.83 Gb/s/pin	6 Gb/s/pin
Energy efficiency	2.39 pJ/b	0.94 pJ/b	0.99 pJ/b

parasitic capacitance on each data path. In pre-layout simulation, eyes are almost identical. The energy efficiency is 0.99 pJ/bit. A summary of performance is listed in Table. 3.2

Chapter 4

NON-UNIFORMLY QUANTIZED SAR ADCS WITH CODE-DEPENDENT WEIGHTS FOR WIRELINE RECEIVERS

4.1 Introduction

High insertion loss channels and multi-level signaling boost the demands for ADC-based I/O link transceivers. The ADCs in wireline receivers receive input signals with non-uniform distribution mainly due to ISI and noise from the wireline channels. It naturally calls for design of non-uniformly quantized ADCs. The role of the ADCs in turn evolves from signal type conversion to signal type conversion and equalization of ISI.

Previous research on non-uniformly quantized ADCs are based on flash ADCs since it is straight forward to control the threshold voltages. A non-uniform flash ADC is introduced to optimize power consumption of receivers [51]. A 3-bit [52] and a 1-to-6-bit [38] non-uniform flash ADCs are proposed to minimize BER. The 3-bit non-uniform flash ADC adjust the threshold voltages by controlling the reference voltages of comparators. The 1-to-6-bit non-uniform flash ADC shuts down the comparators inputting unwanted threshold voltages. However, SAR ADCs are widely used for mid-resolution (4-8 bits) applications including transceivers [5] and usually outperform flash ADCs. Therefore, we propose to the very first design non-uniform SAR ADCs for transceivers.

One simple approach to design NUSAs is to control the transfer function by using non-binary weighted CDAC. To distinguish it from NUSA-CDWs, we name it as non-uniform SAR ADC with code-independent weights (NUSA-CIW). However, such NUSA-CIW generate a limited amount of transfer functions. An N -bit NUSA-CIW has $N - 1$ switching capacitors and $2^N - 2$ non-zero threshold voltages. Each threshold voltage is a linear func-

tion of $N - 1$ capacitor weights as shown in Eq. (4.1)

$$VT_i = \sum_{j=0}^{N-2} k_j \frac{C_j}{C_{tot}} \quad i = 1, 2, \dots, 2^N - 2 \quad (4.1)$$

where VT_i is the threshold voltage of NUSA, C_j/C_{tot} is the capacitor weight and k_j is the coefficient of each capacitor weight. There are $2^N - 2$ linear equations and $N - 1$ variables, which is naturally an ill-defined problem. When $2^N - 2 > N - 1$, there is a high chance that there is no solution for the equations. Therefore many transfer functions cannot be realized by this naive NUSA. The percentage of the transfer functions that can be realized by this NUSA further reduces when the resolution of the ADC increases. Fig. 4.1 shows an example of a 5-bit NUSA-CIW. In this example, the NUSA-CIW cannot generate the target transfer function due to the above reasons.

This chapter proposes a configurable NUSA-CDW that realizes non-linear transfer functions. The NUSA-CDWs acquire flexibility for transfer functions by allowing different capacitor weights for different digital output codes. There are three main advantages of NUSA-CDWs. NUSA-CDWs improve BER when used in ADC-based receivers compared to conventional SAR ADCs. NUSA-CDWs are less power-hungry than non-uniform flash ADCs for mid-to-high resolutions since they are based on SAR ADC architecture. NUSA-CDWs achieve a much wider range of transfer functions than NUSA-CIW. This chapter also derives the statistical BER of the receivers with NUSA-CDWs and the BER lower bound of the receivers with NUSA-CIW to theoretically prove BER improvement of NUSA-CDWs. A 5-bit NUSA-CDW circuit using 65nm CMOS technology is designed and simulated to verify the proposed architecture.

4.2 NUSA with Code-Dependent Weight

In this section, we introduce a SAR ADC architecture that achieves non-uniform transfer function. The reason why NUSA-CIW does not work lies in the switching algorithm of SAR ADC. SAR ADC uses a binary searching method. Therefore, the threshold voltages of a SAR ADC are correlated. Fig. 4.2 shows threshold voltages of a 4-bit SAR ADC. At the

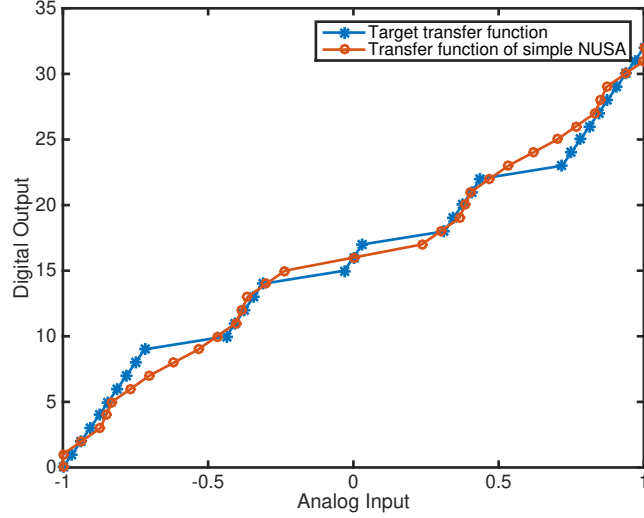


Figure 4.1: Transfer function of a 5-bit simple NUSA, i.e. NUSA-CIW.

third conversion step, C_1 is either switched up or switched down based on the comparison result of VI and corresponding VT_i (one of VT_{14} , VT_{10} , VT_6 , and VT_2). As a result, all the threshold voltages from the fourth conversion step are dictated by C_1 . In other words, the threshold voltage steps at the fourth conversion step are C_1 . This property extremely limits flexibility of the transfer function.

To overcome such intrinsic property of SAR ADCs and generate non-uniform transfer functions, we introduce a NUSA with code-dependent weight. At each conversion step, a NUSA-CDW not only dictates how to switch the capacitor arrays but also dictates the weight of the switching capacitor based on the comparison result. This allows distinct threshold steps and removes correlation between threshold voltages. Fig. 4.3 shows threshold voltages of a 4-bit NUSA-CDW. We define a threshold voltage path as a set of threshold voltages traversed to output a digital code and a path code is the corresponding output digital code. For example, Fig. 4.3 shows a path with path code 111x

$$Path^{(111x)} = \{VT_8, VT_{12}, VT_{14}, VT_{15}\} \quad (4.2)$$

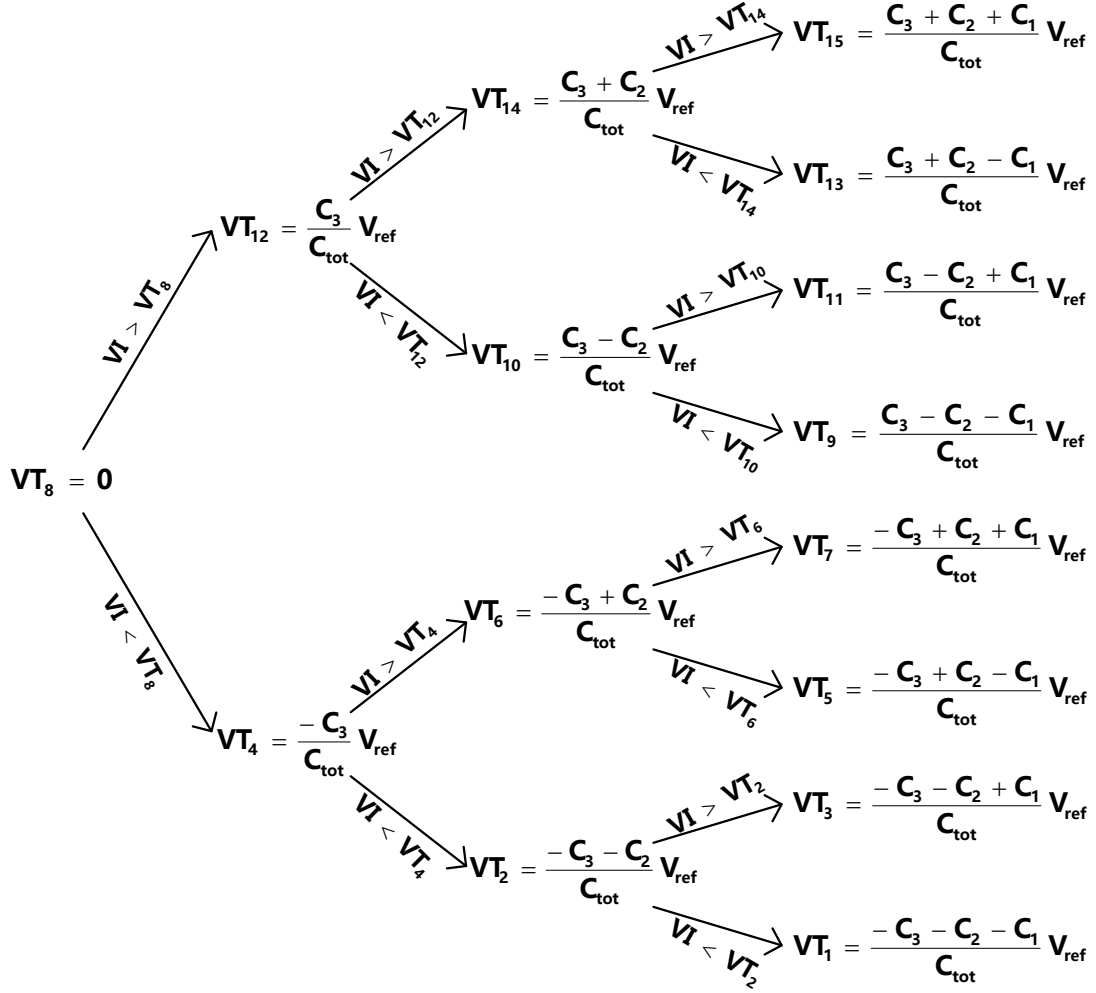


Figure 4.2: Threshold voltage trees of 4-bit ADCs: NUSA-CIW.

where 111x represents that the path code is either 1111 or 1110. An N-bit NUSA-CDW has 2^{N-1} threshold voltage paths. Each path has a set of independent capacitor weights. Therefore there are 2^{N-1} sets of capacitor weights. For example, the capacitor weight set

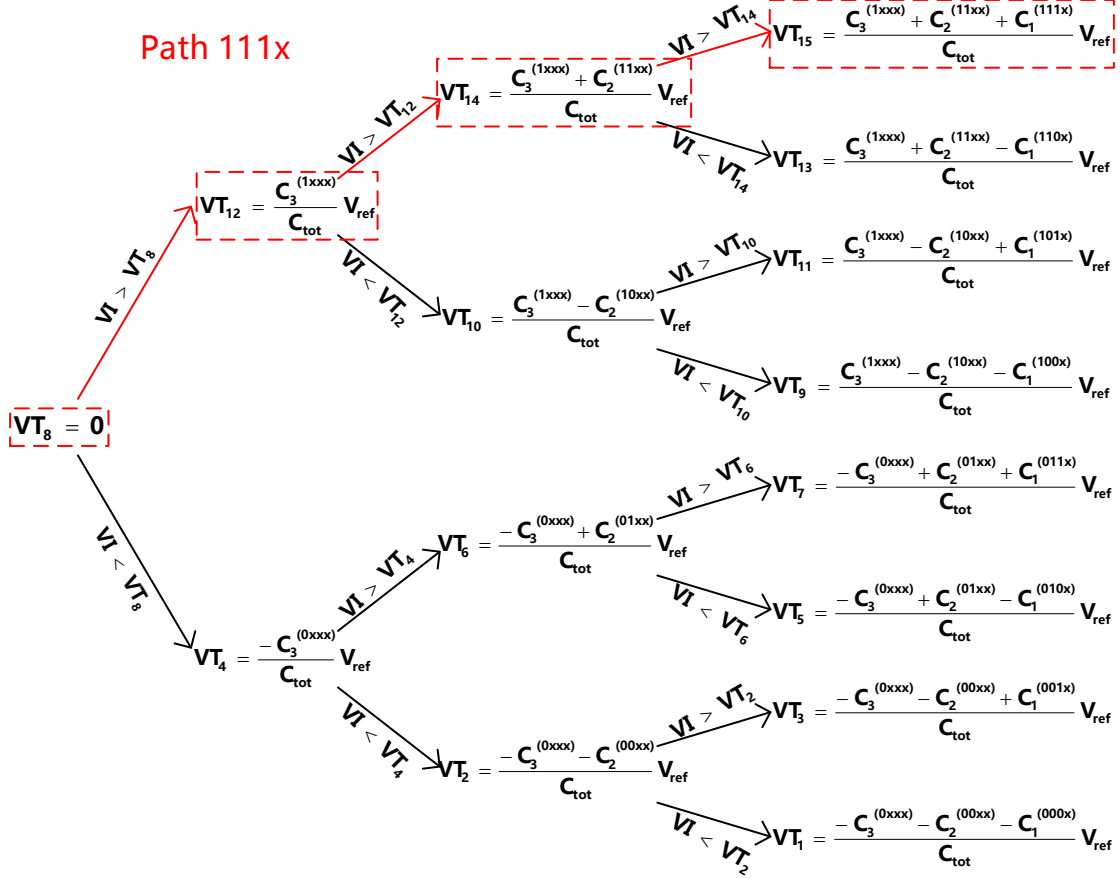


Figure 4.3: Threshold voltage trees of 4-bit ADCs: NUSA-CDW.

$CW^{(111x)}$ of $Path^{(111x)}$ is

$$CW^{(111x)} = \left\{ \frac{C_3^{(1xxx)}}{C_{tot}}, \frac{C_2^{(11xx)}}{C_{tot}}, \frac{C_1^{(111x)}}{C_{tot}}, \frac{C_0^{(111x)}}{C_{tot}} \right\} \quad (4.3)$$

where $C_3^{(1xxx)}/C_{tot}$ is the capacitor weight of C_3 . The path code of C_3 is 1xxx since all of these 16 paths traverse VT_{12} and thus they share the same capacitor weight of C_3 . In other words, there are two capacitor weights of C_3 . There are 2^{N-j} independent capacitor weights for each C_j and $2^N - 2$ total capacitor weights for an N-bit NUSA-CDW.

The expression of threshold voltages of an N-bit NUSA-CDW becomes

$$VT_i = \sum_{j=0}^{N-2} (i \bmod 2^{N-1-j}) (2D_{N-1-j} - 1) \frac{C_{N-1-j}^{(p)}}{C_{tot}} V_{ref} \quad (4.4)$$

where $i = 1, 2, \dots, 2^N - 1$ denotes the index of the threshold voltages, D_{N-1-j} denotes the $N - 1 - j$ -th bit from LSB, $(C_{N-1-j}/C_{tot})^{(p)}$ is the capacitor weight of C_{N-1-j} at the path p , p denotes the path code, and V_{ref} denotes the reference voltage. In Eq. (4.4), there are $2^N - 2$ non-zero equations and $2^N - 2$ variables. Thus a NUSA-CDW can realize a wide range of transfer functions. Since each path has its own capacitor weight set, a NUSA-CDW is a combination of 2^{N-1} NUSA-CIW. Fig. 4.4 shows the transfer function of a 3-bit NUSA-CDW and four 3-bit NUSA-CIW. The capacitor weights of each NUSA-CIW are identical to each path of the NUSA-CDW. In other words, the equivalent transfer function of each path. The transfer function of the NUSA-CDW aligns with the transfer function of each NUSA-CIW when the digital output equals the path code. When the capacitor weight sets of all the paths are identical, a NUSA-CDW degenerates to a NUSA-CIW.

4.3 Analysis of NUSA-CDW

Non-uniform ADCs can be used in wireline transceivers to improve the BER of the receivers [52]. In this section, we derive the minimum BER improvement ratio of the receivers using the NUSA-CDW compared with those using the NUSA-CIW.

We utilize a statistical BER-optimal algorithm [52] to obtain the transfer function of NUSA-CDW that provides the minimum BER. The channel is modeled as a discrete-time linear time-invariant(LTI) system $h[n]$ with additive white Gaussian noise $\eta[n]$. The length of $h[n]$ is L and the standard deviation of $\eta[n]$ is σ_n . The receiver is composed of a NUSA and a maximum likelihood detector.

Since the NUSA-CDW can perfectly fit the threshold voltages generated by the BER-optimal algorithm, the BER of the NUSA-CDW is the same as the BER-optimal formula-

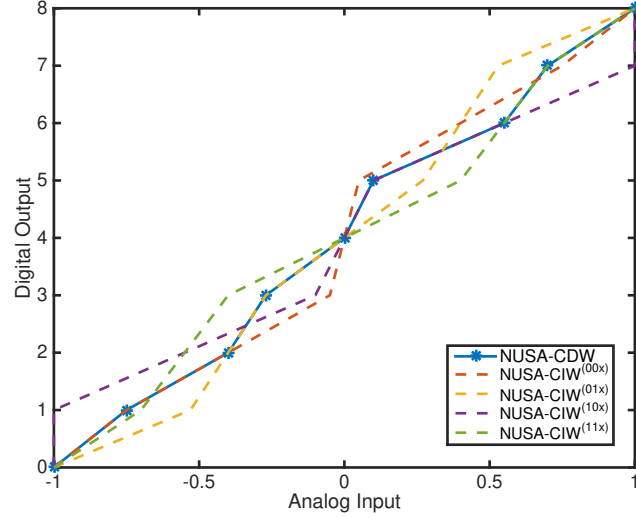


Figure 4.4: Transfer functions of a 3-bit NUSA-CDW and 3-bit NUSA-CIW. The capacitor weights of each NUSA-CIW is identical to each path of the NUSA-CDW.

tion [52] as shown in Equation (4.5)

$$P_{e,CDW} = \sum_{k=1}^{2^N-1} P_{e,CDW,k} = \sum_{k=1}^{2^N-1} \frac{Q\left(\frac{d_k}{\sigma_n}\right)}{2^{L-1}} \quad (4.5)$$

where $P_{e,CDW,k}$ is the BER from k th threshold voltage, $Q(\cdot)$ is the Q-function and d_k is the minimum distance of the k th threshold voltage VT_k to the nearest noise-free channel output.

On the contrary, the NUSA-CIW may not be able to fit the BER-optimal transfer function. When the NUSA-CIW cannot fit the target transfer function perfectly, the BER of the NUSA-CIW is

$$P_{e,CIW} = \sum_{k=1}^{2^N-1} P_{e,CIW,k} = \sum_{k=1}^{2^N-1} \frac{Q\left(\frac{d_k - \Delta VT_k}{\sigma_n}\right)}{2^{L-1}} \quad (4.6)$$

where ΔVT_k is the difference between the threshold voltage of NUSA-CIW $\hat{VT}_k$ and the target threshold voltage VT_k . The total threshold voltage error is $\Delta VT_{tot} = \sum_{k=1}^{2^N-1} \Delta VT_k$.

In this section, we use the total threshold voltage error, ΔVT_{tot} , to characterize the performance of NUSA-CIW. In order to obtain the minimum BER improvement ratio of

Algorithm 1 NUSA-CIW optimization algorithm

```

1: Sort  $\{d_k\}$  with descending order
2:  $\Delta VT_{remain} = \Delta VT_{tot}$ 
3: for  $k \in \{1, 2, \dots, 2^N - 1\}$  do
4:   if  $\Delta VT_{remain} \geq k(d_k - d_{k+1})$  then
5:     for  $i \in \{1, 2, \dots, k\}$  do
6:        $\Delta VT_{i-} = d_k - d_{k+1}$ 
7:        $\Delta VT_{remain-} = k(d_k - d_{k+1})$ 
8:     end for
9:   else
10:    for  $i \in \{1, 2, \dots, k\}$  do
11:       $\Delta VT_{i-} = \Delta VT_{remain} / k$ 
12:    end for
13:    Break
14:  end if
15: end for

```

NUSA-CDW compared with NUSA-CIW, we introduce an Algorithm 1 that can achieve the lower bound of BER given ΔVT_{tot} . We will prove the optimality of Algorithm 1 latter.

The algorithm first sorts $\{d_k\}$ with a descending order so that $Q(d_1/\sigma_n)$ contributes the least to the total BER. The basic idea of the algorithm is to progressively reduce larger threshold voltages to a smaller threshold in a descending order. If the total threshold voltage error is large enough, all $2^N - 1$ thresholds will become the same in the end.

Now we prove that Algorithm 1 is able to produce the lower bound of BER for NUSA-CIW when given a fixed total error ΔVT_{tot} through mathematical induction. First, consider the base step of mathematical induction when the total error ΔVT_{tot} needs to be allocated to ΔVT_1 and ΔVT_2 to achieve minimum $Q((d_1 - \Delta VT_1)/\sigma_n) + Q((d_2 - \Delta VT_2)/\sigma_n)$. We assume d_k is in descending order. If $\Delta VT_{tot} \geq d_1 - d_2$,

$$2Q\left(\frac{d_1 + d_2 - \Delta VT_{tot}}{2\sigma_n}\right) \leq Q\left(\frac{d_1 - \Delta VT_1}{\sigma_n}\right) + Q\left(\frac{d_2 - \Delta VT_2}{\sigma_n}\right) \quad (4.7)$$

where ΔVT_1 and ΔVT_2 are any possible combinations that satisfy $\Delta VT_1 + \Delta VT_2 = \Delta VT_{tot}$. Equation (4.7) is derived from Jensen's inequality. It holds because $Q(x)$ is a convex function when $x \geq 0$. If $\Delta VT_{tot} < d_1 - d_2$,

$$\begin{aligned} Q\left(\frac{d_1 - \Delta VT_{tot}}{\sigma_n}\right) + Q\left(\frac{d_2}{\sigma_n}\right) &< Q\left(\frac{d_1}{\sigma_n}\right) + Q\left(\frac{d_2}{\sigma_n}\right) + \frac{\delta Q\left(\frac{d_1 - \Delta VT_{tot}}{\sigma_n}\right)}{\delta VT} \Delta VT_{tot} \\ &\leq Q\left(\frac{d_1}{\sigma_n}\right) + \frac{\delta Q\left(\frac{d_1 - \Delta VT_1}{\sigma_n}\right)}{\delta VT} \Delta VT_1 + Q\left(\frac{d_2}{\sigma_n}\right) + \frac{\delta Q\left(\frac{d_2}{\sigma_n}\right)}{\delta VT} \Delta VT_2 \\ &\leq Q\left(\frac{d_1 - \Delta VT_1}{\sigma_n}\right) + Q\left(\frac{d_2 - \Delta VT_2}{\sigma_n}\right) \end{aligned} \quad (4.8)$$

where ΔVT_1 and ΔVT_2 are any combinations satisfying $\Delta VT_1 + \Delta VT_2 = \Delta VT_{tot}$. Equation (4.8) satisfies because $\delta Q(x)/\delta x$ is monotonically descending when $x > 0$.

Next, we prove the inductive step, i.e. if Algorithm (4.8) is the lower bound BER for $k \in \{1, 2, \dots, n\}$, then then it is the lower bound BER for $k \in \{1, 2, \dots, n + 1\}$. Similar to the base step, if $\Delta VT_{tot} > \sum_{k=1}^{k=n-1} d_n - d_k$, based on Jensen's inequality and the convex property of $Q(x)$ when $x > 0$, we can prove that $d_k - \Delta VT_k = (\sum_{k=1}^{k=n+1} d_k - \Delta VT_{tot})/n$

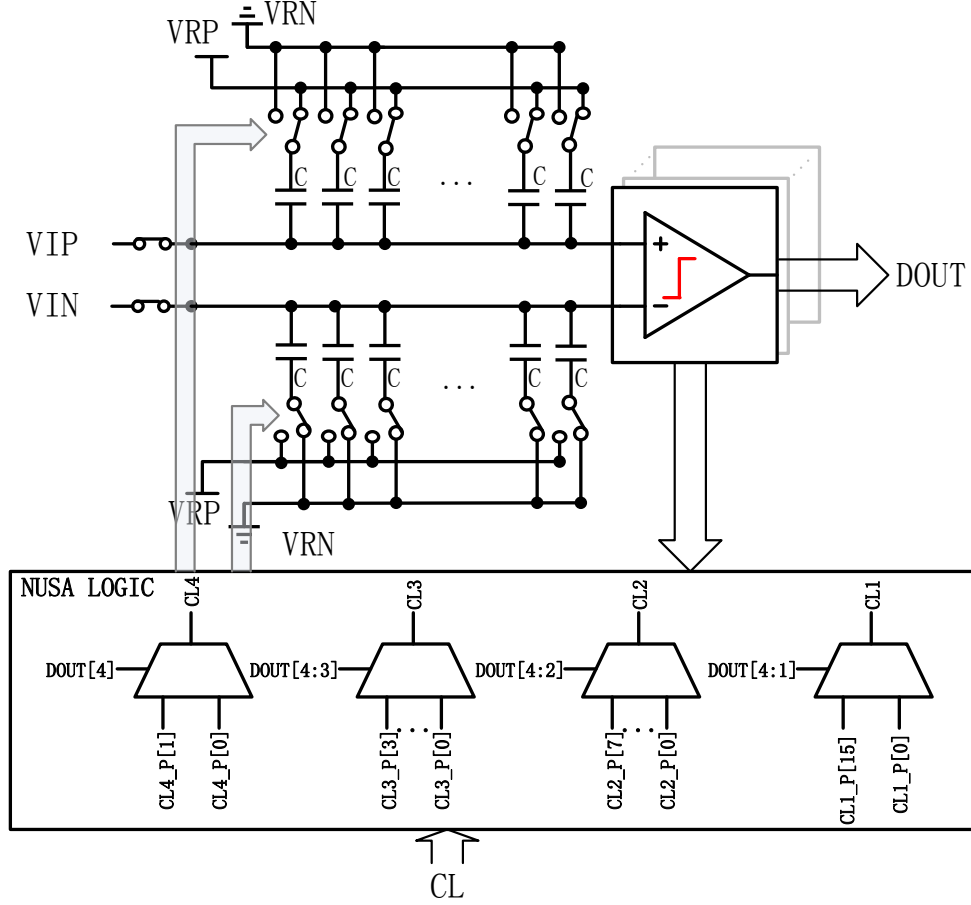


Figure 4.5: Circuit diagram of a 5-bit NUSA-CDW.

provides the minimum BER. If $\Delta VT_{tot} < \sum_{k=1}^{k=n-1} d_n - d_k$, because of the monotonically descending slope of $Q(\cdot)$, all of ΔVT_{tot} should be allocated to $VT_k, k \in \{1, 2, \dots, n\}$, which is a solved sub-problem. Therefore, given a total threshold error ΔVT_k , the lower bound of $P_{e,CIW}$ in Eq. (4.6) is obtained by allocating threshold errors with Algorithm 1.

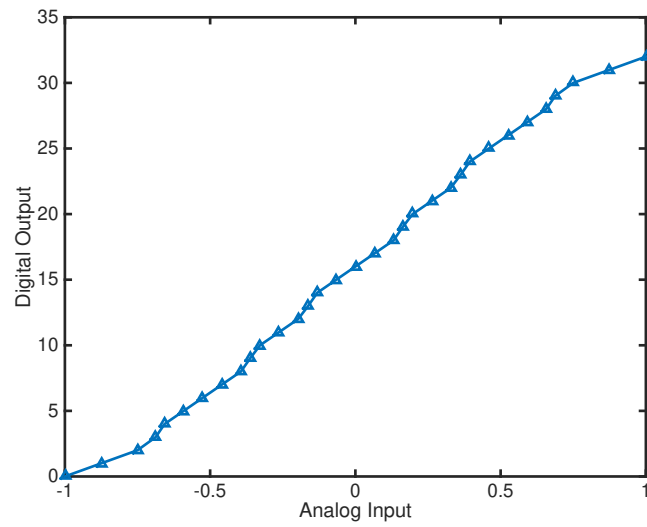


Figure 4.6: Transfer function of the 5-bit NUSA-CDW circuit.

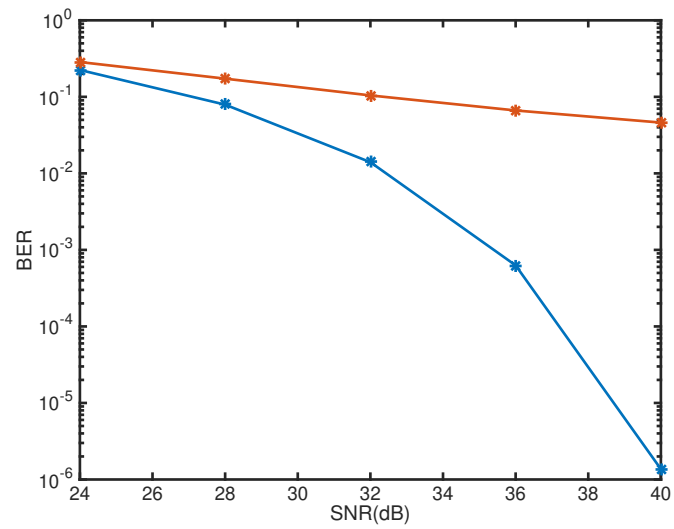


Figure 4.7: BER vs. SNR of the 5-bit NUSA-CDW circuit and an ideal 5-bit uniform ADC.

4.4 Circuit implementation

A configurable 5-bit NUSA-CDW circuit is implemented in 65nm technology. The NUSA-CDW circuit is composed of sample-and-hold circuit, a differential capacitive DAC, 5 comparators, and the NUSA digital logic as illustrated in Fig. 4.5. We use a bootstrapped switch to implement the sample-and-hold block. The CDAC consists of binary weighted capacitors. It employs set-and-down switching to improve the speed of the ADC yet maintain a constant common-mode voltage [53]. We adopt one comparator for each conversion step to get rid of the SAR logic and save feedback delay [54]. The NUSA logic mainly composed of multiplexers to select capacitor weights. The inputs of the NUSA logic are 16 sets of the control signals for the capacitive DAC. Each set of the control signals corresponds to one threshold voltage. The transfer function can be easily configured by modifying the control signals. The NUSA-CDW circuit works as follows. First, we configure the control signals based on the desired transfer function. Then we start to run the ADC circuit. The sample-and-hold circuit captures the input analog signal to the top plate of the capacitive DAC. The first comparator compares the output of the capacitive DAC and generates the first bit of the digital output. Based on this comparison result, the NUSA logic selects one set of the control signals. The selected control signals then switches the capacitor arrays to obtain a new threshold voltage for next conversion step. After five conversion steps, the NUSA-CDW circuit outputs a 5-bit digital code.

Table 4.1 shows the simulation results of the 5-bit NUSA-CDW circuit. The 5-bit NUSA-CDW circuit is simulated at 512MS/s sampling rate. The full-scale input range of the ADC is $1.8 \text{ V } V_{pp,diff}$ and the power supply is 1.2 V. We first configured it as a uniform ADC. SNDR and ENOB of the ADC circuit are 30.88dB and 4.83 bits at 244MS/s input frequency. Then we configured it with a non-uniform ADC. The transfer function of the NUSA-CDW circuit is plotted in Fig. 4.6. The power consumption is $600.59 \mu\text{W}$ and the figure of merit is 36.6 fJ/conv. We also simulated the NUSA-CDW circuit within a wireline transceiver. The channel response of $h[n] = [0.0788, 0.2627, 0.1576, 0.1051, 0.0525, 0.002]$. The NUSA-CDW

Table 4.1: Performance Summary

Architecture	NUSA-CDW	Non-uniform flash
Technology	65 nm	90 nm
Resolution	5 b	3 b
Supply voltage	1.2 V	1.2 V
Sampling frequency	512 MS/s	4 GS/s
Differential input range	1.8 V	0.1 V
SNDR@near F_{Nyquist}	30.88 dB	
ENOB	4.83 bits	1.4 bits
Power consumption	600.59 μW	
FoM	36.6 fJ/conv	1.42 pJ/conv

circuit is configured to generate transfer function shown in Fig. 4.6. BERs of the receiver using the NUSA-CDW circuit at various SNRs are depicted in Fig. 4.7. When SNR of the channel is 40 dB, the NUSA-CDW improves BER from 4.6e-2 to 1.3e-6 compared to the conventional SAR ADC. BER enhancement of the NUSA-CDW increases with SNR.

Chapter 5

CHORD-PAM4: A PIN-EFFICIENT NOISE-RESILIENT SIGNALING FOR PARALLEL LINKS

5.1 Introduction

The chiplet-based architecture is rapidly advancing for high-performance computing and artificial-intelligence (AI)-infused edging computing. It can improve yields, reduce the cost, and allow each die to be fabricated in different technologies. Chiplet-based architecture tends to have ultra-short reach inter-chip links and therefore has low channel attenuation. However, as more chips are inter-connected to integrate an immense system, more noise such as SSN and common-mode noise (CMN) would be induced to the links. Therefore, it is significant to balance between noise and ISI to build high communication capacity transceivers for ultra-short reach links [7]. Developing signaling methods that are inherently less sensitive to ISI and therefore require less equalization overhead is essential for relaxing design tradeoffs and opening the door to the implementation of data transceivers with much higher data transfer rates. In addition, innovation of chiplet-based architecture requires configurable low-power high-speed high-bandwidth die-to-die links supporting both data computing and memory access.

There are various signaling methods for high speed links that have been studied. Differential non-return-to-zero (NRZ) has good signal-to-noise ratio (SNR) but low pin efficiency. Signal-ended PAM4 signaling has high pin efficiency but suffers from noise. Multi-wire multi-level permutation signaling [2, 11, 10, 9, 44] encodes input data into the sequence of levels across wires. It has a high pin-efficiency and is robust to SSN. Chord signaling [7, 3, 8] is a multi-wire multi-level signaling method that achieves high pin efficiency to enhance overall data rate without compromising CMN, SSN, ISI sensitivity and crosstalk. Different from

pulse amplitude modulation (PAM) signaling, which uses amplitude domain modulation, chord signaling leverages not only amplitude domain modulation but also spatial domain coding to enhance transmission efficiency.

Chord signaling performs orthogonal transformation to redistribute N bits of binary data over $(N + 1)$ wires (CNRZ-N) such that the orthogonal transformation enforces

$$\sum_{i=0}^N \frac{w_i}{N + 1} = V_{\text{CM}} \quad (5.1)$$

to suppress CMN, SSN and crosstalk. In Eq. 5.1, w_i denotes the signal level transmitted over the i -th wire, N denotes the number of bits of data transmitted, and V_{CM} denotes the common-mode voltage at the output of the transmitter. The transmitted signals w_i are multi-level signals, whereas the decoded signals (after inverse orthogonal transformation) at the input of slicers remain two-level signals. The two-level signals after decoding result in low ISI sensitivity.

This chapter proposes Chord signaling for PAM4 signals, i.e. Chord-PAM4, to enhance pin efficiency and noise resilience. Chord-PAM4 signaling over four wires, CPAM4-6, increases pin efficiency to 150%, translating into 6 bits transmitted over four wires. Also, this chapter thoroughly analyzes Chord-PAM4's pin efficiency, SSN, SNR and ISI sensitivity. The proposed signaling is verified by a prototype configurable combo-PHY transceiver that supports in a 28nm technology.

5.2 Chord-PAM4 signaling

The proposed Chord-PAM4 (CPAM4) signaling is a family of signaling methods, denoted as CPAM4-N, that transmit N bits of binary data across $N/2 + 1$ wires by linear transformation such that it meets

$$\sum_{i=0}^{\frac{N}{2}+1} \frac{w_i}{\frac{N}{2} + 1} = V_{\text{CM}} \quad (5.2)$$

CPAM4-6 signaling is a specific member of the CPAM4 family. For illustrative purposes, we will use CPAM4-6 as an example to introduce the CPAM4 signaling concept.

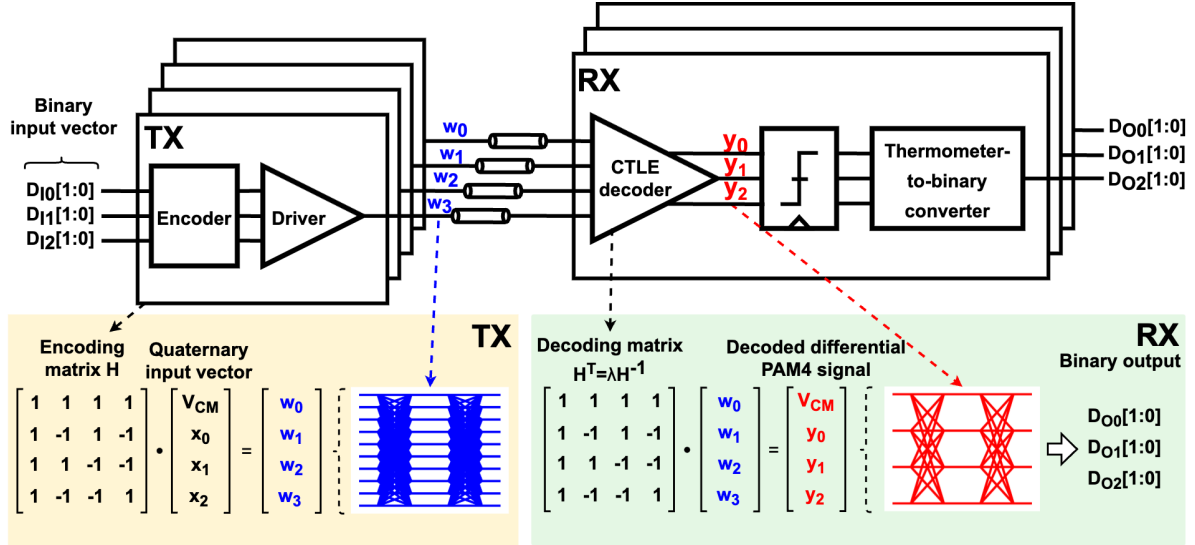


Figure 5.1: Illustration of proposed CPAM4-6 signaling and its link architecture.

Fig. 5.1 illustrates the overall link architecture of CPAM4-6 signaling. In this scheme, six bits of binary input data, $D_{I0}[1:0]$ through $D_{I2}[1:0]$, are transmitted across four wires. All six bits of input data are connected to each of the four transmitters to perform CPAM4-6 encoding. Each wire is connected to a respective transmitter, which outputs the encoded signal w_i for transmission. The transmitted signals w_0 through w_3 propagate through their respective wires and are fed to all three receivers. Each receiver independently decodes received signals and outputs two bits of binary data.

The transmitter is composed of a CPAM4 encoder and an output driver to generate w_0 through w_3 . Three 2-bit binary input data $D_{I0}[1:0]$ through $D_{I2}[1:0]$ are first converted into a quaternary input vector $\mathbf{x}$. This vector is then correlated by performing a linear transformation with an encoding matrix $\mathbf{H}$

$$\mathbf{H} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \quad (5.3)$$

$\mathbf{H}$ is a Walsh–Hadamard matrix, which offers several advantages as will be discussed later. A constant value V_{CM} is inserted in $\mathbf{x}$ to match the vector length for the transformation. Each element x_i of the quaternary input vector can take one of the PAM4 levels from $\{-1, -1/3, +1/3, +1\}$. This linear transformation encodes the quaternary input vector into a 10-level signal vector $\mathbf{w}$ with four signals, which are then redistributed across four wires. $\mathbf{w}$ is given by

$$\mathbf{w} = \mathbf{H}\mathbf{x} = \begin{bmatrix} V_{\text{CM}} + x_0 + x_1 + x_2 \\ V_{\text{CM}} - x_0 + x_1 - x_2 \\ V_{\text{CM}} + x_0 - x_1 - x_2 \\ V_{\text{CM}} - x_0 - x_1 + x_2 \end{bmatrix} \quad (5.4)$$

where $w_i \in \{0, 1/9, 2/9, \dots, 8/9, 1\}$. CPAM4 signaling achieves high pin efficiency because it projects binary input data onto multi-level signals, thereby expanding the available codeword space. Furthermore, the inclusion of an extra wire ensures Eq. 5.2 to inherit resilience to CMN, SSN, and crosstalk.

The receiver consists of a continuous-time linear equalization (CTLE) decoder, a slicer and a thermometer-to-binary-code (TM2B) converter. The CTLE decoder performs an inverse linear transformation on the received signals $\mathbf{w}$ to retrieve the PAM4 signals $\mathbf{y}$, which correspond to quaternary input data $\mathbf{x}$.

$$\mathbf{y} = \mathbf{H}^T \mathbf{w} = \begin{bmatrix} w_0 + w_1 + w_2 + w_3 \\ (w_0 - w_1) + (w_2 - w_3) \\ (w_0 - w_2) + (w_1 - w_3) \\ (w_0 - w_1) + (w_3 - w_2) \end{bmatrix} \quad (5.5)$$

Since each column of $\mathbf{H}$ is mutually orthogonal, $\mathbf{H}^{-1} = \lambda \mathbf{H}^T$. Equation 5.5 shows that the decoding process is fully differential, which inherently eliminates CMN. Following decoding, the slicer compares the recovered PAM4 signals with three reference voltages to generate the thermometer output data. Subsequently, the TM2B converter converts the thermometer data into the final binary output data $D_{00}[1:0]$ through $D_{02}[1:0]$.

A Walsh–Hadamard matrix is chosen as the CPAM4-6 encoding matrix due to the following design-friendly properties:

1. The sum of each column, except the 0th column, is zero. Hence, the sum of the transmitted signals across four wires remains constant. This leads to a stable supply current, which significantly reduces SSN and EMI [7].
2. $\mathbf{H}^{-1} = \mathbf{H}^T$. Combined with the first property, this ensures that each row of the decoding matrix sums to zero. This characteristic effectively eliminates CMN because the decoding process is fully differential.
3. The value of each matrix entry h_{ij} is either 1 or -1. This simplifies the encoding process as it eliminates the need for complex multiplications, thereby reducing encoding overhead. Furthermore, due to the property $\mathbf{H}^{-1} = \mathbf{H}^T$, data can be decoded by multiplying with the same low-overhead matrix.
4. The sums of each row are equivalent for all rows. The sums of each row are equivalent for all rows. This property allows for identical designs of the transmitter drivers across all lanes, which leads to improved matching and performance consistency among the lanes.

CPAM4-6 signaling also shares similar properties with differential PAM4 signaling: both methods introduce one extra wire to enhance noise performance. In fact, when $N = 2$, CPAM4-2 is equivalent to differential PAM4 signaling. In other words, CPAM4 can be considered as a generalized form of differential PAM4. This also explains CPAM4’s inherent resistance to noise and crosstalk.

Table 5.1: Code space of CPAM4 and m W4L permutation signaling.

Number of wires m	CPAM4 code space $C_{\text{CPAM4-}N}$	m W4L permutation code space $C_{m\text{W}p\text{L},\text{max}}$
2	4	2
3	16	6
4	64	24
5	256	60
6	1024	180
7	4096	630
8	16384	2520

5.3 Analysis of Chord-PAM4 Signaling

5.3.1 Pin Efficiency

Pin efficiency is a critical figure of merit for parallel links that refers to the efficiency of I/O pin utilization [11, 2, 10, 44, 7]. A pin-efficient link enhances overall data transfer throughput. For instance, a single-ended non-return-to-zero (NRZ) link transmits 1 bit per pin per symbol, meaning the pin efficiency is 100%. In contrast, a differential NRZ link has 50% pin efficiency because it requires two pins to transmit 1 bit. When the signal bandwidth is the same, the data rate of a differential link drops to half that of a single-ended link due to low pin efficiency.

The pin efficiency of CPAM4- N is given by

$$\eta_{\text{CPAM4-}N} = \frac{N}{\frac{N}{2} + 1} \quad (5.6)$$

The pin efficiency of CPAM4 is improved by 2x compared to CNRZ with the same number of wires. CPAM4-6 has 150% pin efficiency, achieving 50% higher pin efficiency compared to differential PAM4 signaling. The pin efficiency of CPAM4 increases with the number of

wires. The theoretical limit of their pin efficiency is

$$\eta_{\text{CPAM4-}N} < \lim_{N \rightarrow \infty} \eta_{\text{CPAM4-}N} = 200\% \quad (5.7)$$

The high pin efficiency of CPAM4 eases the requirement for signal bandwidth. When the desired data bit rate is f_b , the symbol rate of CPAM4-N $f_{s, \text{CPAM4-}N}$ is

$$f_{s, \text{CPAM4-}N} = \frac{f_b}{\eta_{\text{CPAM4-}N}} \quad (5.8)$$

The symbol rate of CPAM4-6 is 2/3 that of differential PAM4. Consequently, CPAM4-6 experiences lower channel loss and Gaussian noise.

Another category of pin-efficient signaling methods is multi-wire multi-level permutation signaling [2, 11, 10, 9, 44]. This method encodes data into the sequence of levels across wires, rather than independently encoding data into each wire's level. The pin efficiency of an m -wire p -level ($m\text{WpL}$) permutation signaling method is given by

$$\eta_{m\text{WpL}} \leq \frac{\lfloor \log_2 C_{m\text{WpL}} \rfloor}{m} = \frac{\lfloor \log_2 \frac{m!}{\prod_{i=1}^p q_i!} \rfloor}{m} \quad (5.9)$$

where $C_{m\text{WpL}}$ denotes the total number of possible permutation codewords and q_i denotes the number of times level i is repeated in the codeword. The pin efficiency is maximized when $\max(q_i)$ is minimized, which corresponds to the largest possible $C_{m\text{WpL}}$. This maximum pin efficiency, denoted as $\eta_{m\text{WpL}, \max}$, is expressed as

$$\eta_{m\text{WpL}, \max} = \frac{\lfloor \log_2 C_{m\text{WpL}, \max} \rfloor}{m}$$

where $C_{m\text{WpL}, \max}$ is calculated as

$$C_{m\text{WpL}, \max} = \frac{m!}{\left\lceil \frac{m}{p} \right\rceil!^{m \bmod p} \left(\left\lceil \frac{m}{p} \right\rceil - 1 \right)!^{p - (m \bmod p)}} \quad (5.10)$$

As can be seen, the pin efficiency of permutation signaling is limited by the number of possible codewords, i.e., its code space. Due to permutation characteristics, the code space is a factorial of the number of wires.

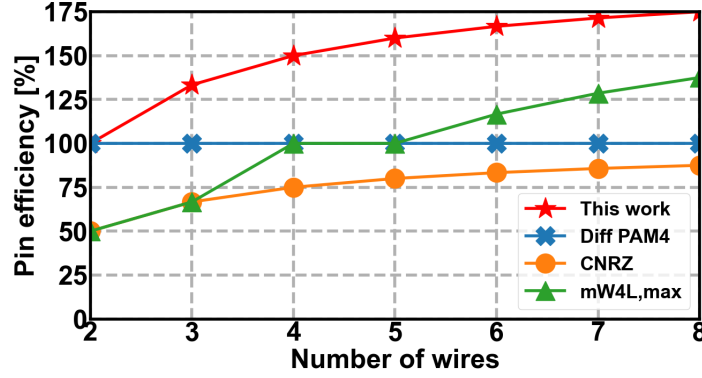


Figure 5.2: Pin efficiency of various signaling methods.

To demonstrate that CPAM4 has higher pin efficiency, the code space of CPAM4 is also derived. CPAM4 has two sets of code spaces $C_{\mathbf{w}}$ and $C_{\mathbf{y}}$ for $\mathbf{w}$ and $\mathbf{y}$. Since there is no restriction on the number of levels for $\mathbf{w}$, $C_{\mathbf{w}}$ can theoretically be considered infinite. Therefore, the overall code space of CPAM4 $C_{\text{CPAM4-}N}$ is limited by $C_{\mathbf{y}}$. As $\mathbf{y}$ are PAM4 signals, $C_{\text{CPAM4-}N}$ and $\eta_{\text{CPAM4-}N}$ are given by

$$C_{\text{CPAM4-}N} = C_{\mathbf{y}} = 4^{m-1} \quad (5.11)$$

$$\eta_{\text{CPAM4-}N} = \frac{\lfloor \log_2 C_{\text{CPAM4-}N} \rfloor}{m} = \frac{2(m-1)}{m} \quad (5.12)$$

As shown in Table 5.1, CPAM4 exhibits a larger code space than m W4L permutation signaling; consequently, it achieves higher pin efficiency with the same number of wires.

Fig. 5.2 plots the pin efficiency of different signaling methods versus the number of wires m . The pin efficiency of CPAM4 increases from 100% to 175% as the number of wires increases from 2 to 8. When $m = 2$, the pin efficiencies of CPAM4 and differential PAM4 are the same, consistent with CPAM4 being a generalized form of differential PAM4 signaling. As m increases, the pin efficiency of CPAM4 significantly outperforms differential PAM4 without sacrificing noise resilience. When $m = 4$, CPAM4-6 achieves 150% pin efficiency, which is 1.5x that of differential PAM4 signaling. Compared to CNRZ signaling, the pin

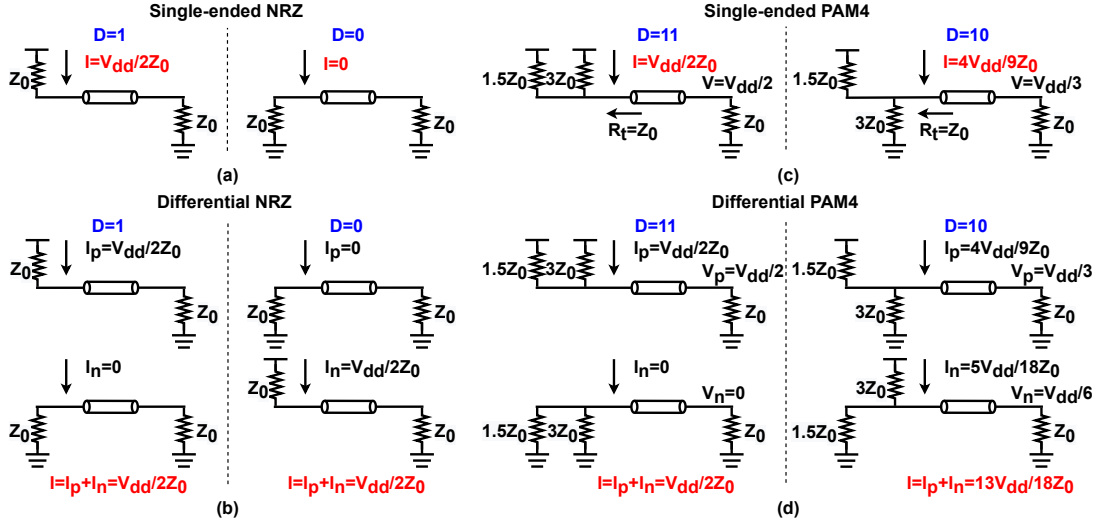


Figure 5.3: Equivalent circuits of voltage-mode output drivers for current variation and SSN analysis. The depicted signaling methods are: (a) single-ended NRZ, (b) differential NRZ, (c) single-ended PAM4, and (d) differential PAM4. Differential NRZ signaling eliminates total current variation, whereas differential PAM4 still exhibits current variation.

efficiency of CPAM4 is approximately 2x higher. The $mW4L$ permutation signaling also exhibits a rising trend. However, for the same m , its pin efficiency remains lower than that of CPAM4 signaling, as previously demonstrated.

5.3.2 SSN

Simultaneous switching of multiple output drivers results in SSN, which manifests as a voltage fluctuation, V_{SSN} , on the power supply. V_{SSN} can be calculated by

$$V_{SSN} = L \frac{di}{dt} \quad (5.13)$$

where L represents the inductance between the device power supply and the system power supply, which is mainly contributed by the board and package traces, and i is the total current drawn by the output drivers from the power supply. SSN is influenced by the signaling

method, as the signaling method determines the total current of the output driver [9, 11, 44, 2, 7]. To illustrate the influence of signaling methods on current variation, Fig. 5.3 compares the current profiles for single-ended versus differential, and NRZ versus PAM4 signaling.

Figs. 5.3(a) and (b) show the equivalent circuits of voltage-mode output drivers for single-ended NRZ and differential NRZ, respectively. For single-ended NRZ, the output driver current I drops from $V_{dd}/2Z_0$ to 0 as the input data transitions from $D = 1$ to $D = 0$, where Z_0 denotes transmission line's characteristic impedance. For differential NRZ, although the currents for each output driver I_p and I_n still change with the input data, the total current from the two output drivers remains constant. Consequently, differential NRZ eliminates SSN. Figures 5.3(c) and (d) depict the equivalent circuits for single-ended PAM4 and differential PAM4, respectively. The PAM4 output driver comprises two branches corresponding to the most significant bit (MSB) and the least significant bit (LSB) of the input data to generate four levels of signal. To match the termination impedance R_t with the characteristic impedance Z_0 , the output driver resistors are scaled to $1.5Z_0$ for the MSB branch and $3Z_0$ for the LSB branch. In contrast to NRZ, the total currents for both differential and single-ended PAM4 fluctuate when input data change from $D = 11$ to $D = 10$. The total currents I of differential PAM4 for $D = 11$ and $D = 00$ are equal to the sum of I of single-ended PAM4 for $D = 11$ and $D = 00$. Similarly, I of differential PAM4 for $D = 10$ and $D = 01$ are equal to the sum of I of single-ended PAM4 for $D = 10$ and $D = 01$. As a result, while differential PAM4 mitigates current variation and SSN, it does not fully eliminate them.

CPAM4 signaling inherently reduces the output driver's current variation due to the constant sum of its output signals, as shown in Eq. 5.2. For derivation and comparison of the current variation between CPAM4 and differential PAM4, both are assumed to employ source series termination (SST) drivers [55, 4], a common architecture in multi-level signaling transmitters. Fig. 5.3 depicts the schematic of an SST output driver. It consists of $p - 1$ slices connected in parallel to generate a p -level output signal. The resistance of each driver slice is given by

$$R_s = (p - 1)R_t \quad (5.14)$$

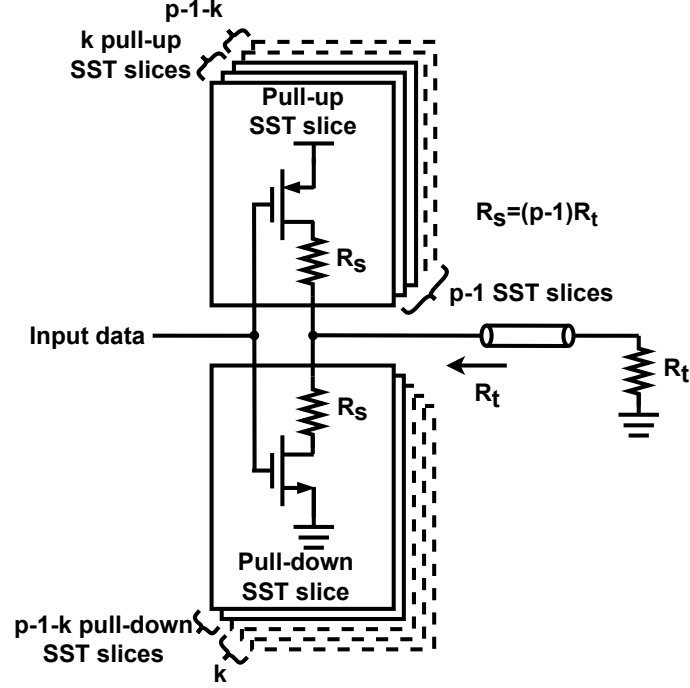


Figure 5.4: Schematic of the SST output driver with $(p - 1)$ slices to generate p levels of the output signal.

where R_t is the desired termination resistance. When the transmitter generates an output signal w , the number of slices pulling up is determined by

$$k = \frac{2(p-1)w}{V_{dd}} \quad (5.15)$$

The total resistance and the corresponding current of each transmitter are expressed as

$$R_{tot} = \frac{R_s}{k} + \frac{\frac{R_s}{p-1-k} R_t}{\frac{R_s}{p-1-k} + R_t} = \frac{R_t}{2 \left(\frac{w}{V_{dd}} - \left(\frac{w}{V_{dd}} \right)^2 \right)} \quad (5.16)$$

$$I = \frac{V_{dd}}{R_{tot}} = \left(\frac{w}{V_{dd}} - \left(\frac{w}{V_{dd}} \right)^2 \right) \frac{2V_{dd}}{R_t} \quad (5.17)$$

The total current across the four channels is the sum of their individual currents

$$I_{\text{tot, CPAM4-6}} = \sum_{i=0}^3 I_i = \frac{2V_{\text{dd}}}{R_t} \sum_{i=0}^3 \left(\frac{w_i}{V_{\text{dd}}} - \left(\frac{w_i}{V_{\text{dd}}} \right)^2 \right) \quad (5.18)$$

The output signal vector $\mathbf{w}$ is expressed as

$$\mathbf{w} = a_{\text{TX}} \mathbf{H} \mathbf{x}, \quad a_{\text{TX}} = \frac{1}{12} \quad (5.19)$$

where a_{TX} is the scaling coefficient to obtain the output signal values $\mathbf{w}$. Inserting Eq. 5.19 into Eq. 5.18, $I_{\text{tot, CPAM4-6}}$ is derived as

$$I_{\text{tot, CPAM4-6}} = -\frac{(x_0^2 + x_1^2 + x_2^2)}{18R_t V_{\text{dd}}} - \frac{V_{\text{CM}}^2}{18R_t V_{\text{dd}}} + \frac{2V_{\text{CM}}}{3R_t} \quad (5.20)$$

Considering that CPAM4-6 transmits 6-bit data per unit interval, the current per bit of input data for CPAM4-6 is

$$I_{\text{bit, CPAM4-6}} = -\frac{(x_0^2 + x_1^2 + x_2^2)}{108R_t V_{\text{dd}}} - \frac{V_{\text{CM}}^2}{108R_t V_{\text{dd}}} + \frac{V_{\text{CM}}}{9R_t} \quad (5.21)$$

To derive the output driver current variation for differential PAM4, it can be modeled as CPAM4-2, i.e., a member of CPAM4 family that transmits 2-bit data across two wires. The output signals are then given by

$$\begin{bmatrix} w_0 \\ w_1 \end{bmatrix} = a_{\text{TX}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} V_{\text{CM}} \\ x_0 \end{bmatrix}, \quad a_{\text{TX}} = \frac{1}{4} \quad (5.22)$$

To transmit 6-bit data, differential PAM4 requires six channels. The total current of differential PAM4 across six channels is expressed as

$$I_{\text{tot, Diff-PAM4}} = -\frac{(x_0^2 + x_1^2 + x_2^2)}{4R_t V_{\text{dd}}} - \frac{3V_{\text{CM}}^2}{4R_t V_{\text{dd}}} + \frac{3V_{\text{CM}}}{R_t} \quad (5.23)$$

The current per bit of input data for differential PAM4 is

$$I_{\text{bit, Diff-PAM4}} = -\frac{(x_0^2 + x_1^2 + x_2^2)}{24R_t V_{\text{dd}}} - \frac{V_{\text{CM}}^2}{8R_t V_{\text{dd}}} + \frac{V_{\text{CM}}}{2R_t} \quad (5.24)$$

Eq. 5.21 and Eq. 5.24 reveal that the non-constant data-dependent term in $I_{\text{bit, CPAM4-6}}$ has the same functional dependence on input data but with a smaller coefficient than that in

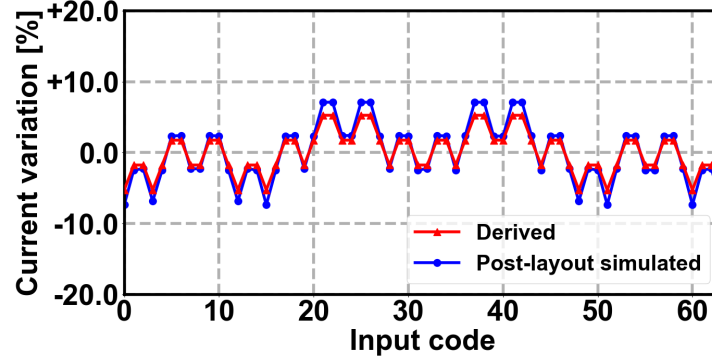


Figure 5.5: Comparison of the derived and post-layout simulated total output driver current variation per bit $\Delta I_{\text{bit, CPAM4-6}}$ for CPAM4-6 signaling, plotted against 6-bit input data.

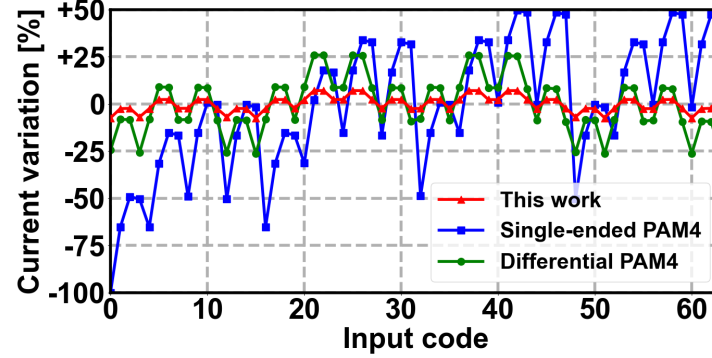


Figure 5.6: Post-layout simulated total output driver current variation per bit ΔI_{bit} versus 6-bit input data for CPAM4-6, single-ended PAM4, and differential PAM4 transmitters.

$I_{\text{bit, Diff-PAM4}}$. Consequently, the current variation for CPAM4-6 $\Delta I_{\text{bit, CPAM4-6}}$ is lower than that for differential PAM4 $\Delta I_{\text{bit, Diff-PAM4}}$.

Fig. 5.5 presents a validation of the theoretical derivation for CPAM4-6. It demonstrates that the derived $\Delta I_{\text{bit, CPAM4-6}}$ closely matches the post-layout simulated results across different input data. Theoretically, the maximum variation and standard deviation of the total

output driver current are 5.26% and 3.04%, respectively. Fig. 5.6 compares the post-layout simulated ΔI_{bit} among CPAM4-6, single-ended PAM4 and differential PAM4. This plot demonstrates that CPAM4-6 significantly enhances current stability compared to both single-ended PAM4 and differential PAM4, consistently across all input data codes. Specifically, the current variation of CPAM4-6 remains within 7.36% with a 4.11% standard deviation, while the current variations of differential and single-ended PAM4 fluctuate by up to 26.9% (with a 14.9% standard deviation) and 100% (with a 34.6% standard deviation), respectively.

5.3.3 CMN

CPAM4 signaling is inherently robust to CMN. $\mathbf{w}$ and $\mathbf{y}$ are susceptible to CMN. To demonstrate CMN rejection of CPAM4, we take CPAM4-6 as an example and CMN is injected to $\mathbf{w}$ and $\mathbf{y}$. The signals received at the receiver front end with CMN are

$$\mathbf{r} = \mathbf{w} + n_{\text{CM},\mathbf{w}} \quad (5.25)$$

Then after propagating through the decoder, $\mathbf{y}'$ is

$$\mathbf{y}' = \mathbf{H}^T \mathbf{r} = \mathbf{H}^T \mathbf{w} + \mathbf{H}^T \mathbf{n}_{\text{CM},\mathbf{w}} \quad (5.26)$$

Because $(\mathbf{H}^T \mathbf{n}_{\text{CM},\mathbf{w}})_i = 0$ for $i = 1, 2, 3$, the output of decoder is

$$\mathbf{y}' = \begin{bmatrix} V_{\text{CM}} + 4n_{\text{CM},\mathbf{w}} \\ y_0 \\ y_1 \\ y_2 \end{bmatrix} \quad (5.27)$$

It shows that the decoded signals y_i are free from $n_{\text{CM},\mathbf{w}}$. Hence, CMN injected at $\mathbf{w}$ is rejected by the decoder. Next, CMN $n_{\text{CM},\mathbf{y}}$ is injected to $\mathbf{y}'$. Because $\mathbf{y}'$ is differential signal, $n_{\text{CM},\mathbf{y}}$ is rejected by the slicer.

5.3.4 SNR

To analyze the effective noise from channels, assume that each wire is subject to independent and identically distributed (i.i.d.) Gaussian noise with a root mean square (RMS) power

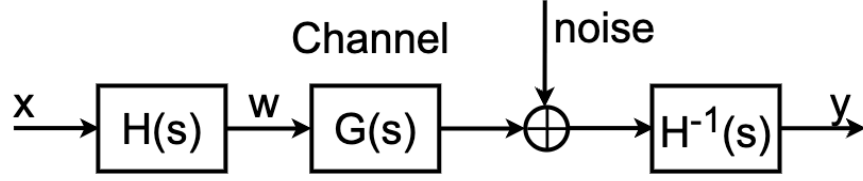


Figure 5.7: Link system block diagram.

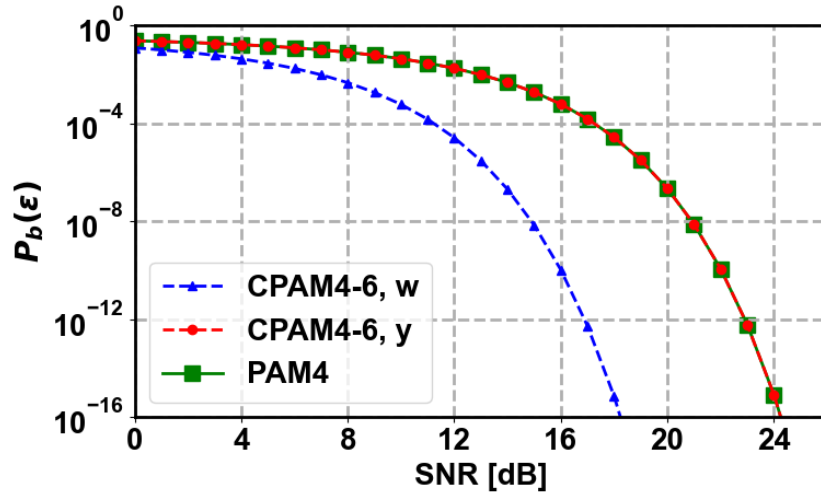


Figure 5.8: Probability of bit error as a function of SNR for CPAM4-6 and PAM4.

spectral density of N_0 . The link transfer function block diagram is illustrated in Fig. 5.7.

The SNR for $\mathbf{w}$ and $\mathbf{y}$ at the data rate f_b is

$$\text{SNR}_{\mathbf{w}} = \frac{d_{\mathbf{w}}}{\sqrt{f_N N_0}} = \frac{d_{\mathbf{w}}}{\sqrt{\frac{f_b}{2\eta_{\text{CPAM4-6}}} N_0}} \quad (5.28)$$

$$\text{SNR}_{\mathbf{y}} = \frac{d_{\mathbf{y}}}{\sqrt{\sum_{i=0}^N (h_{ij}^T)^2 \frac{f_b}{2\eta_{\text{CPAM4-6}}} N_0}} \quad (5.29)$$

where $d_{\mathbf{w}}$ and $d_{\mathbf{y}}$ are the minimum distance between the levels of $\mathbf{w}$ and $\mathbf{y}$, and f_N is the bandwidth of noise and is equal to Nyquist frequency of CPAM4-6 signals. From Eq. 5.28

and Eq. 5.29, we can get the SNR ratio of $\mathbf{y}$ and $\mathbf{w}$

$$\alpha = \frac{\text{SNR}_{\mathbf{y}}}{\text{SNR}_{\mathbf{w}}} \quad (5.30)$$

From Eq. 5.30 and probability of bit error formula [56, 57], probability of bit error for CPAM4-6 $P_b(\varepsilon)$ as a function of $\text{SNR}_{\mathbf{w}}$ is

$$P_b(\varepsilon) \approx \frac{P_s(\varepsilon)}{\log_2(p_{\mathbf{y}})} = \frac{2(p_{\mathbf{y}} - 1)}{p_{\mathbf{y}} \log_2(p_{\mathbf{y}})} Q\left(\frac{\alpha \text{SNR}_{\mathbf{w}}}{2}\right) \quad (5.31)$$

where $P_s(\varepsilon)$ is probability of symbol error and $p_{\mathbf{y}}$ is the number of levels of $\mathbf{y}$. Fig. 5.8 plots $P_b(\varepsilon)$ versus SNR for CPAM4-6 and PAM4. As shown in the figure, to achieve the desired BER, $\mathbf{w}$ requires a lower SNR than PAM4. Thus, although CPAM4-6 has low SNR penalty due to multi-level signals transmitted over channels, the requirement for SNR is relaxed at the same time. When SNR of $\mathbf{y}$ is the same as that of PAM4, they achieve the same BER.

Fig. 5.9 shows normalized SNR with $V_{\text{FS}}/\sigma_n = 1$ as a function of $\sigma_{\text{CMN}}/\sigma_n$ when the total noise $\sqrt{\sigma_n^2 + \sigma_{\text{CMN}}^2}$ is constant, where $\sigma_n = \sqrt{f_b N_0}$ and σ_{CMN} is RMS of CMN and V_{FS} is the peak-peak amplitude of signal. SNR of differential PAM4 is given by

$$\text{SNR}_{\text{Diff-PAM4}} = \frac{d_{\text{Diff-PAM4}}}{\sqrt{\frac{f_b}{\eta_{\text{DIFF-PAM4}}} N_0}} \quad (5.32)$$

The SNR of single-ended PAM4 is

$$\text{SNR}_{\text{SE-PAM4}} = \frac{d_{\text{SE-PAM4}}}{\sqrt{\frac{f_b}{2\eta_{\text{SE-PAM4}}} N_0 + \sigma_{\text{CMN}}^2}} \quad (5.33)$$

Eq. 5.29 and Eq. 5.32 show that CPAM4-6 has -4.77 dB penalty in SNR compared to differential PAM4. CPAM4-6 shows better SNR than single-ended PAM4 due to its CMN resilience except for when $\sigma_{\text{CMN}}/\sigma_n < 1$.

5.3.5 ISI Sensitivity

The ISI sensitivity of a signaling method generally increases with the number of signal levels. CPAM4 transmits a higher number of levels $p_{\mathbf{w}} \geq 4$ through the channels, where these levels

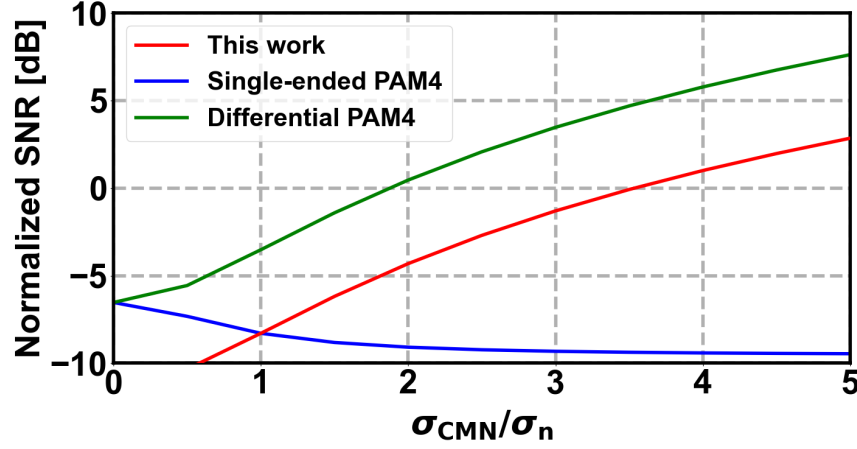


Figure 5.9: Normalized SNR versus $\sigma_{\text{CMN}}/\sigma_n$.

are directly distorted by ISI. This might initially suggest a high sensitivity to ISI. However, CPAM4 exhibits the same ISI sensitivity as PAM4 because these levels are reduced to four at the slicers after decoding. This section will prove that ISI sensitivity is determined by the number of levels at the slicer p_y , rather than the number of levels transmitted over the channel p_w .

The transmitted signal $\mathbf{w}(\mathbf{t})$ is given by

$$\mathbf{w}(\mathbf{t}) = \mathbf{H} \cdot \mathbf{x}(\mathbf{t}) \quad (5.34)$$

where $\mathbf{x}(\mathbf{t})$ is the quaternary input signal. After passing through a channel with an impulse response $g(t)$, the received signal $\mathbf{r}(\mathbf{t})$ is calculated by the convolution

$$\mathbf{r}(\mathbf{t}) = g(t) \otimes \mathbf{w}(\mathbf{t}) \quad (5.35)$$

The received signal on the i -th wire is

$$r_i(t) = \int_{-\infty}^{\infty} \sum_{j=0}^3 h_{ij} x_j(\tau) g(t - \tau) d\tau \quad (5.36)$$

The output signal of the decoder $\mathbf{y}(\mathbf{t})$ is obtained by applying the inverse transformation:

$$\mathbf{y}(\mathbf{t}) = \mathbf{H}^{-1} \cdot \mathbf{r}(\mathbf{t}) \quad (5.37)$$

The i -th element of $\mathbf{y}(\mathbf{t})$ is given by

$$y_i(t) = \sum_{k=0}^3 h_{ik}^{-1} \int_{-\infty}^{\infty} \sum_{j=0}^3 h_{kj} x_j(\tau) g(t - \tau) d\tau \quad (5.38)$$

Since the decoding matrix is the inverse of $\mathbf{H}$, the expression for $y_i(t)$ simplifies to

$$y_i(t) = \int_{-\infty}^{\infty} x_i(\tau) g(t - \tau) d\tau \quad (5.39)$$

Defining T as the clock period and $y_i(t)$ can be written as

$$\begin{aligned} y_i(t) &= \sum_{n=-\infty}^{\infty} x_i(nT) g(t - nT) \\ &= x_i(0) g(t) \left(1 + \sum_{n=-\infty}^{-1} \frac{x_i(nT)}{x_i(0)} \frac{g(t - nT)}{g(t)} \right. \\ &\quad \left. + \sum_{n=1}^{\infty} \frac{x_i(nT)}{x_i(0)} \frac{g(t - nT)}{g(t)} \right) \end{aligned} \quad (5.40)$$

As evident from the above equation, the decoded signal is independent of the transmitted signal $\mathbf{w}(\mathbf{t})$ or the encoding matrix $\mathbf{H}$. Therefore, the ISI sensitivity of CPAM4 is not determined by $p_{\mathbf{w}}$. In Eq. (5.40), the term $\frac{x_i(nT)}{x_i(0)} \frac{g(t-nT)}{g(t)}$ represents the ISI-related fading factor, where $x_i(nT)/x_i(0)$ quantifies the contribution to ISI originating from the signaling method itself [7]. In the worst-case scenario, $x_i(nT)/x_i(0)$ can be as large as three, which is equivalent to the case for PAM4 signaling. Thus, CPAM4 has the same ISI sensitivity as PAM4 signaling.

Chapter 6

A CONFIGURABLE PIN-EFFICIENT NOISE-RESILIENT CHORD-PAM4/PAM4/NRZ TRANSCEIVER COMBINING AND ENHANCING UCIE/LPDDR4X STANDARDS

6.1 Introduction

Chiplet-based architecture is rapidly advancing for high-performance computing and AI-infused edging computing. Its innovation requires configurable low-power high-speed high-bandwidth die-to-die links supporting both data computing and memory access. This work presents the first reported transceiver, fabricated and tested in 28nm CMOS, that can be configured to support both UCIE [1] and LPDDR4X [2] standards. Fig. 1 illustrates an example of a system-on-chiplets (SoC), where the integrated high-speed links can be configured either in the standard LPDDR4X mode to interface with DDR memory dies, or the UCIE mode to interface with computing dies. To fully utilize the pins required for LPDDR4X, the UCIE PHY is extended from its standard 16 lane mode to a 48 lane turbo mode. In addition to NRZ signaling, the turbo-UCIE mode supports PAM4 signaling and Chord-PAM4 (CPAM4) signaling introduced in previous chapter. PAM4 signaling doubles the bandwidth of NRZ at reduced signal-to-noise ratio (SNR), while CPAM4 further achieves 50% higher pin efficiency over differential PAM4 with little SNR degradation. Further, CPAM4, as a form of generalized dynamically differential signaling, is inherently resilient to common-mode noise (CMN), has low simultaneously switching noise (SSN) and electromagnetic interference (EMI).

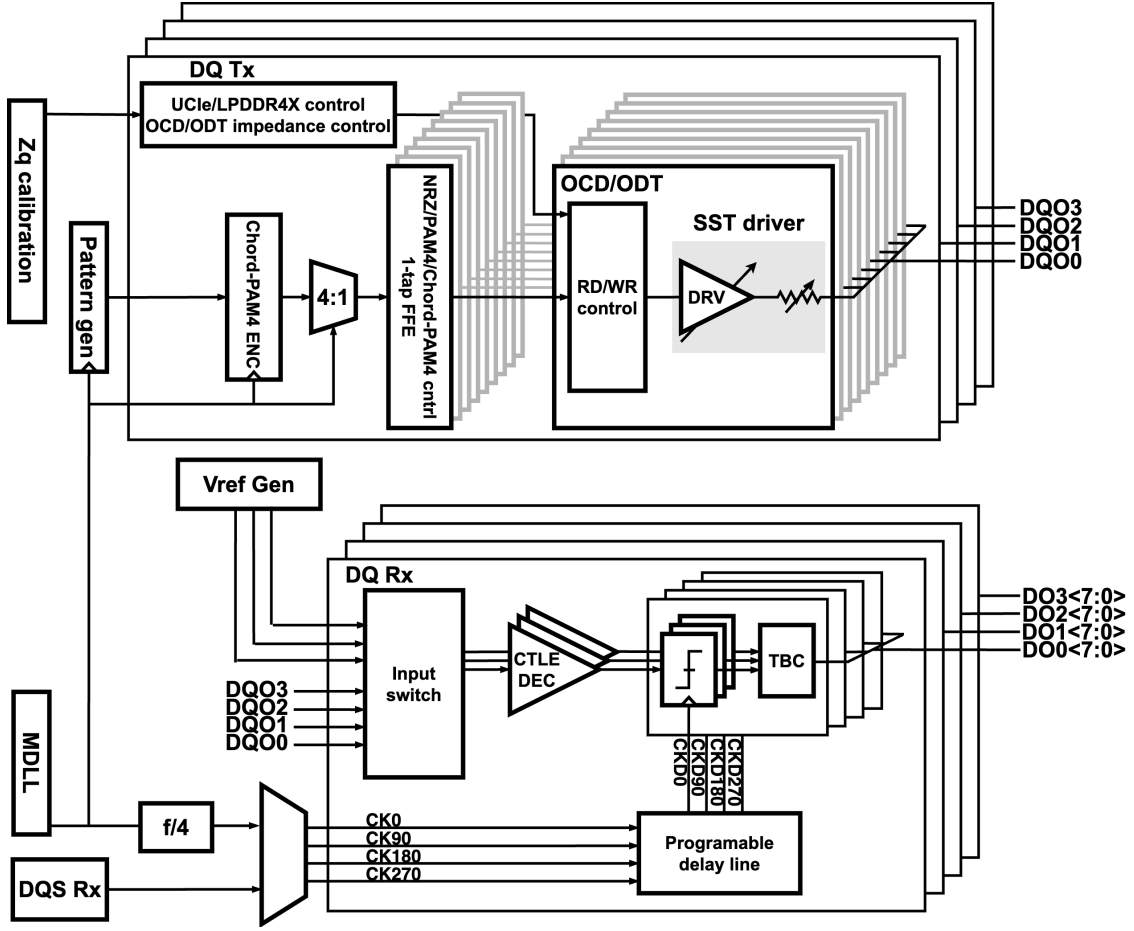


Figure 6.1: Combo-PHY transceiver architecture.

6.2 Circuit Implementation

6.2.1 Architecture

Figure 6.1 illustrates the architecture of the configurable bidirectional UCIe/LPDDR4X combo-PHY transceiver, which features the proposed CPAM4-6 signaling. This combo-PHY transceiver can be configured to support both UCIe [58] and LPDDR4X standards. In UCIe mode, it supports multiple signaling schemes: NRZ, PAM4, and CPAM4-6. Table 6.1 summarizes the mode specifications of this transceiver, where V_s denotes the transmitter's

Table 6.1: Combo-PHY transceiver Mode Specifications

Mode	LPDDR4X	UCIe		
Signaling	NRZ	NRZ	PAM4	CPAM4
Signal levels at the TX output (V_s)	0, 1	0, 1	1/8, 3/8, 5/8, 7/8	0, 1/9, 2/9, ..., 9/9
Signal levels at the RX output (V_s)	0, 1	0, 1	1/8, 3/8, 5/8, 7/8	-6/9, -2/9, +2/9, +6/9
TX Termination impedance (Ω)	40-240	30	30	30
RX Termination impedance (Ω)	40-240	50	50	50
# of driver slices enabled	1-6	8	8	9
Reference voltages (V_s)	0.5	0.5	2/8, 4/8, 6/8	-4/9, 0, +4/9

output swing. This versatile multi-mode configuration allows the transceiver to adapt to various performance requirements and channel conditions, ranging from traditional binary signaling to high-bandwidth multi-level modulation schemes. Figure 6.2 depicts an example of a system-on-chiplets (SoC), where the integrated high-speed links can be configured either in the standard LPDDR4X mode to interface with memory devices, or in the UCIe mode to interface with computing dies. To fully utilize the pins typically required for LPDDR4X, the UCIe PHY is extended from its standard 16-lane mode to a 48-lane turbo mode. Beyond standard NRZ signaling, to further enhance throughput, the turbo-UCIe mode supports the

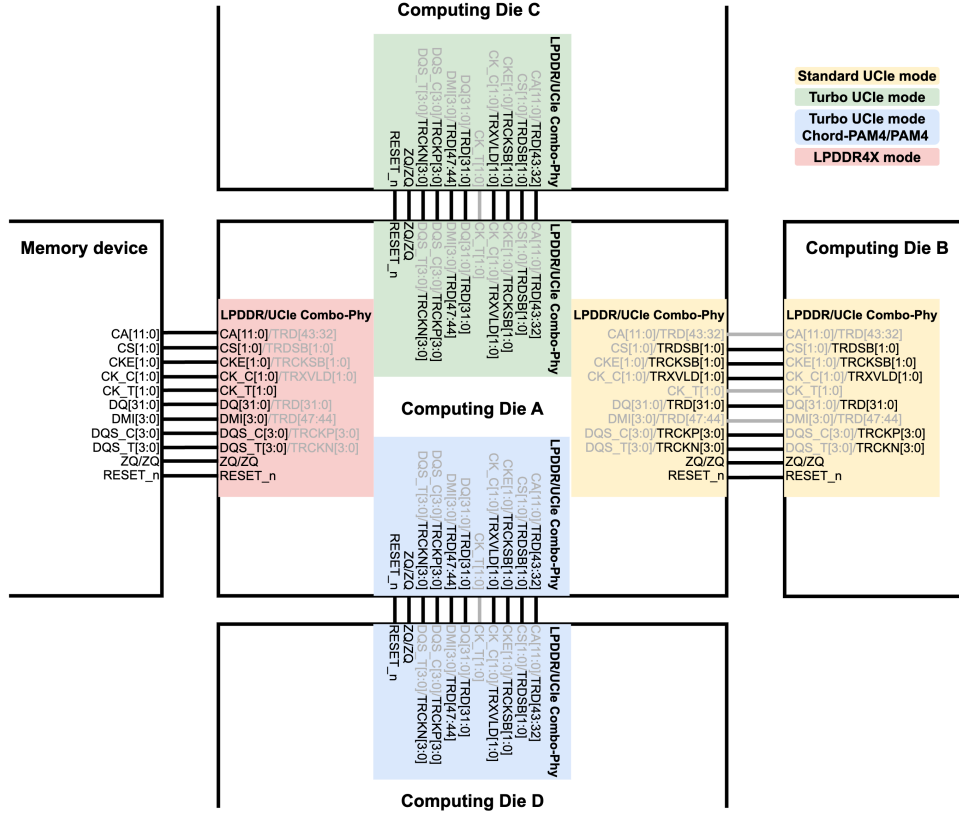


Figure 6.2: A chiplet-based system with the proposed UCle/LPDDR4X combo-PHY. When A communicates with a memory device, it works in the LPDDR4X mode. When communicate with B, C and D, it operates in the 16-lane standard mode and the 48-lane turbo mode. In the turbo mode, throughput is further increased with CPAM4-6/PAM4.

PAM4 signaling and the novel CPAM4 signaling introduced in this paper.

The transceiver is composed of four data lanes (DQ TXs and DQ RXs) and a differential pair of clock forward lanes (DQS TXs and DQS RXs). The transceiver adopts a quarter-rate architecture. In the DQ TX, a digital CPAM4-6 encoder first encodes binary input data. This approach is chosen over an analog encoder to minimize area and parasitics. The encoded CPAM4-6 data, along with the input data for NRZ/PAM4, are then serialized via the 4:1 multiplexers (MUXs). The four-phase clock for the 4:1 MUXs are generated by an on-chip

on-chip multiplying delay-locked loop (MDLL). A dedicated signaling mode control block selects the appropriate data lines to feed into each driver slice. A total of nine slices of the source-series termination (SST) driver operate as an off-chip driver (OCD) in write mode or on-die termination (ODT) in read mode. In the DQ RX, a CTLE-based CPAM4-6 decoder simultaneously decodes 10-level signals and performs equalization. An input switch controls the signaling mode by selecting corresponding input for the CTLE decoder. In NRZ/PAM4 modes, the CTLE decoder degrades to a conventional CTLE. Finally, four sets of slicers and TM2B decoders, triggered by quarter-rate clocks, recover binary output data.

The key component enabling the proposed transceiver to support both UCIE and LPDDR4X standards is the SST driver. Based on the Read/Write control block configuration, it operates in two modes to enable bidirectional functionality: as an off-chip driver (OCD) in DQ TX or as on-die termination (ODT) in DQ RX. The SST driver incorporates a tunable resistor slice that adapts to different termination requirements across different standards. For LPDDR4X compatibility, it maintains equal termination resistance values for both OCD and ODT modes, ensuring a consistent output swing of $0.5V_{DD}$. In this mode, one to six SST driver slices can be enabled to provide termination resistance ranging from 40Ω to 240Ω , in compliance with the LPDDR4X standard. In contrast, when supporting the UCIE standard, the driver employs fixed termination values: 50Ω for ODT and 30Ω for OCD. This configuration delivers an output swing exceeding 400 mV. In both UCIE NRZ and PAM4 modes, five driver slices are enabled for ODT and eight driver slices for OCD. In CPAM4 mode, ODT maintains five enabled driver slices, while OCD utilizes all nine available driver slices.

6.2.2 Transmitter

Figure 6.3 illustrates the CPAM4-6 encoder, which is implemented with two different topologies to perform linear transformation. As an illustrative example, the encoder is assumed to calculate $w_1 = -x_0 + x_1 - x_2$, which corresponds to the second row of the linear transformation matrix $\mathbf{H}$.

In Fig. 6.3(a), an analog encoder, originally designed for CNRZ-5 in [7], is redesigned to

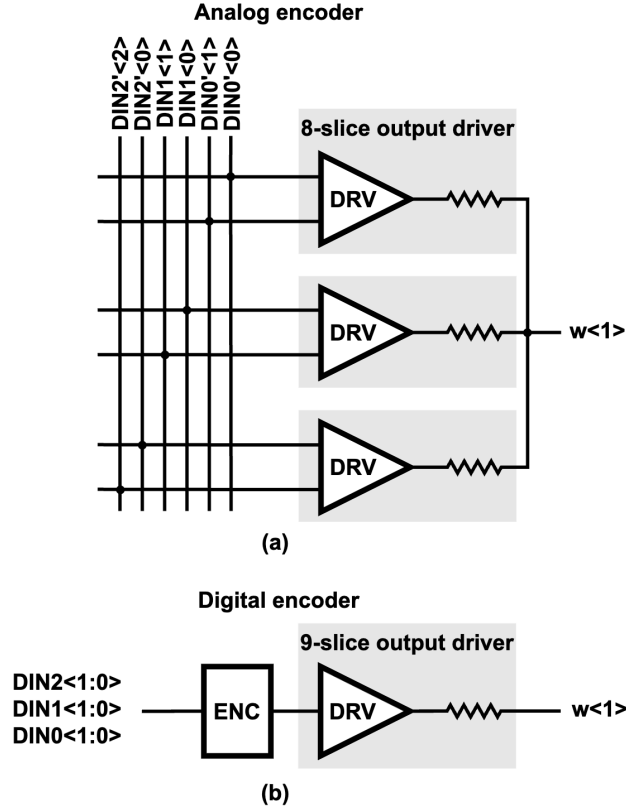


Figure 6.3: CPAM4-6 encoder topology: (a) analog encoder; (b) digital encoder.

perform CPAM4-6 encoding. Each 2-bit input data is connected to n_j voltage-mode PAM4 output drivers, where n_j corresponds to the weight of the input data, i.e., $|h_{1j}|$. In this particular case, all h_{1j} coefficients are either $+1$ or -1 ; therefore, each $D_{Ij}[1:0]$ connects to one PAM4 output driver. Negative weights are realized by performing a two's complement operation on $D_{Ij}[1:0]$. In this figure, $D'_{I2}[1:0]$ and $D'_{I0}[1:0]$ denote the two's complement of $D_{I2}[1:0]$ and $D_{I0}[1:0]$, respectively. The outputs of drivers are all connected in parallel to w_1 , enabling the summation of the weighted inputs. These output drivers are impedance-scaled such that their parallel connection achieves the desired termination impedance. The

**Proposed digital encoder reduces
the number of SST driver slices from 32 to 9.**

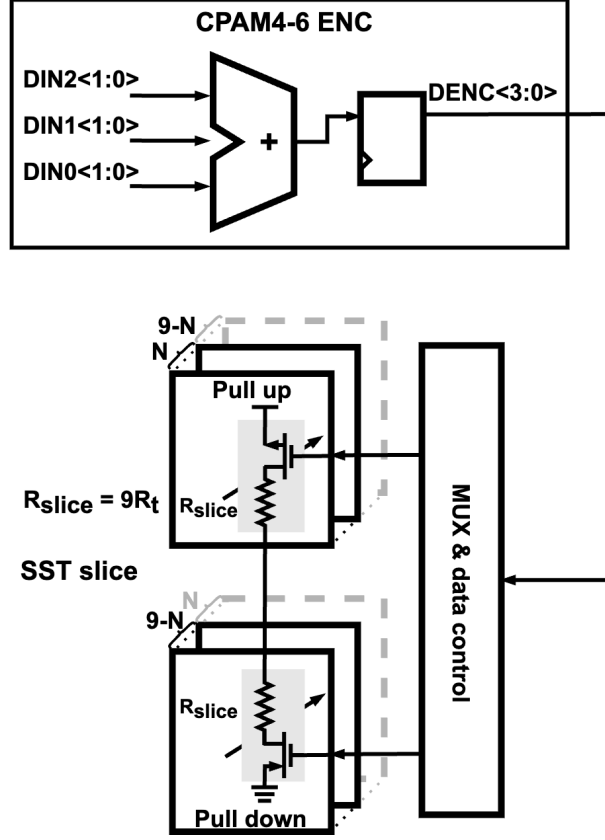


Figure 6.4: Schematic of the CPAM4-6 encoding circuit.

scaling factor K_i for each output w_i is given by

$$K_i = \sum_{j=1}^{N/2} |h_{ij}| \quad (6.1)$$

where $N/2$ denotes the number of $D_{Ij}[1:0]$ inputs and its value is $N/2 = 3$ for CPAM4-6. The total impedance used increases by a factor of K_i^2 compared to that of a PAM4 driver, which leads to high overhead in terms of silicon area and parasitic capacitance. For instance, the impedance increase is 64x for CNRZ-5 [7] and 9x for CPAM4-6, when compared to conventional PAM4 drivers. While it is theoretically possible to reduce this overhead by

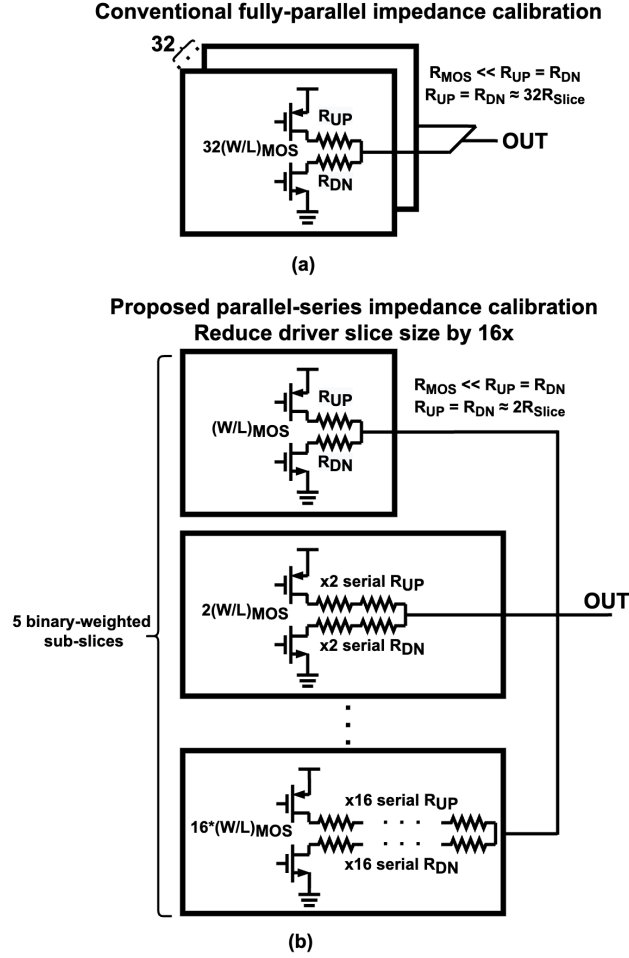


Figure 6.5: Impedance tuning for an SST output driver slice: (a) fully parallel impedance calibration; (b) proposed parallel-series impedance calibration.

minimizing $\sum_{j=1}^{N/2} |h_{ij}|$ during the encoding matrix design, the CPAM4-6 example demonstrates that this approach is not effective even with optimization. Another drawback of this design is that the values of K_i are not necessarily identical for each i . This discrepancy results in different numbers of parallel drivers for each channel, which introduces mismatch and consequently aggravates skew between channels. This issue is particularly critical because chord signaling is inherently vulnerable to skew, as it directly translates into jitter after decoding.

To circumvent the challenges encountered by the analog CPAM4-6 encoder, a digital CPAM4-6 encoder is proposed, as depicted in Fig. 6.3(b). In contrast to the analog CPAM4-6 encoder, this digital CPAM4-6 encoder divides the encoding process into two distinct steps: linear transformation and signal generation, rather than performing it in a single step. In the linear transformation step, the 2-bit input data $D_{I0}[1 : 0]$ through $D_{I2}[1 : 0]$ are fed into a separate digital encoder to perform the linear transformation. Subsequently, in the signal generation step, a PAM10 output driver generates the corresponding analog signal w . The primary advantage of this digital encoder topology is that the output driver is fully decoupled from the linear transformation process. Consequently, the output driver degenerates to a normal, single output driver, which significantly reduces the encoding overhead. Specifically, the overhead of the output driver is effectively reduced from an 8x increase (as seen in the analog approach) to only 27% compared to a conventional PAM4 driver. The digital encoder not only minimizes area overhead but also significantly decreases parasitic capacitance on the high-speed signal paths, thereby alleviating the need for additional resources for equalization. Furthermore, this overhead is independent of the encoding matrix $\mathbf{H}$. Hence, unlike the analog topology, the overhead does not increase as $\sum_{j=1}^{N/2} |h_{ij}|$ increases. Moreover, since all channels now utilize a single output driver, no additional skew is introduced between channels. The digital logic of the digital encoder is designed to be as simple and compact as possible in order to further minimize any extra overhead. Figure 6.4 shows the schematic of the digital encoder. The linear transformation is essentially implemented by an adder. A retimer is employed following the adder to account for any skew among its outputs. Then, a single-stage logic block generates control signals for the output drivers.

The output driver of the proposed TX is an SST output driver [55]. It comprises nine slices connected in parallel to generate 10-level signal in CPAM4 mode. The output impedance of the output driver can deviate from the nominal termination impedance due to process variations. To account for this, the output impedance is designed tunable with 5-bit control signals, allowing the output impedance to meet the impedance resolution specified by LPDDR4X and UCIe standards. Figure 6.5(a) illustrates a conventional parallel impedance

calibration for an output driver slice [55]. In this approach, the sub-slice impedance (R_{UP} and R_{DN}) is scaled to 32x of the original slice impedance R_{slice} and duplicated 32 times. This scaling ensures that the effective impedance of each individual R_{slice} remains unchanged. The most significant bit (MSB) of the control signal connects to the inputs of 16 sub-slices, while the least significant bit (LSB) connects to a single sub-slice. This topology results in a total impedance that is 32^2 times larger than that of a driver slice without impedance calibration (i.e., sum of 32 R_{UP} and R_{DN}). This significant increase leads to an enormous area and parasitic overhead. If this approach were adopted in a CPAM4 output driver, there would be a total of 9×32 sub-slices connected in parallel. The total impedance utilized would be $R_{drv} = (9 \times 32)^2 R_t = 82944 R_t$, where R_t is the nominal termination impedance. The overhead is further exacerbated by the multi-slice structure of the CPAM4 driver.

To mitigate the impedance calibration overhead of the output driver, a parallel-serial tunable slice is introduced for the output driver. Figure 6.5(b) shows the schematic of the proposed driver slice. It comprises five sub-slices, each connected to one bit of the control signal. The MSB of the control signal connects to the top sub-slice, which contains one R_{UP} and one R_{DN} . The LSB of the control signal connects to the bottom sub-slice, which consists of 16 serial R_{UP} and R_{DN} . In contrast to the conventional topology shown in Fig. 6.5(a), the binary-weighted sub-slice impedance in this proposed design is achieved by resistors connected in serial. When the total impedance of the proposed slice is also R_{slice} , the individual R_{UP} and R_{DN} values are equal to $2R_{slice}$. This value is notably only 1/16 of the corresponding R_{UP} and R_{DN} values used in a fully parallel slice. The total impedance utilized in this proposed slice is 64x of a driver slice without impedance calibration. This design effectively suppresses calibration overhead by 16x compared to conventional fully parallel slices.

6.2.3 Receiver

In the receiver, the CPAM4-6 decoder is integrated within the CTLE circuit. Figure 6.6 depicts the CTLE decoder circuit in the CPAM4-6 mode of this combo-PHY. The decoder

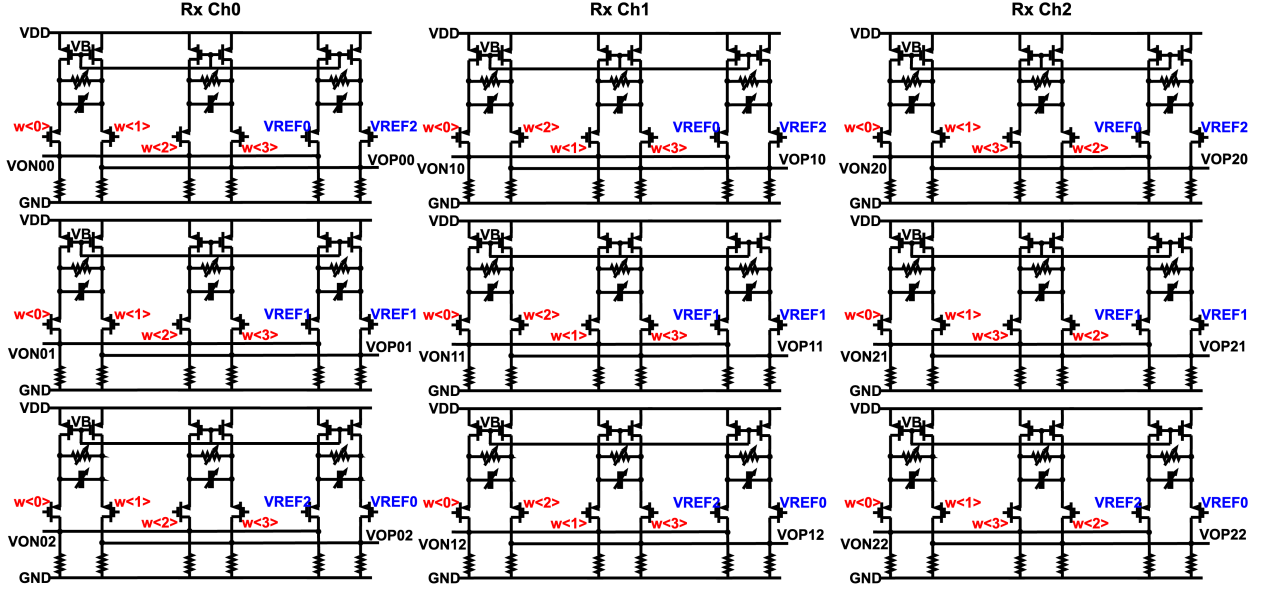


Figure 6.6: Schematic of the CTLE decoder circuit in CPAM4-6 mode.

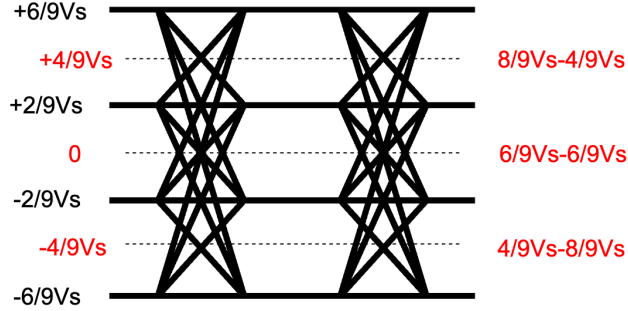


Figure 6.7: CPAM4-6 eye diagram after decoding with differential reference voltages.

essentially performs three primary operations: subtraction, addition, and multiplication. The subtraction is performed by leveraging the differential pairs of the CTLE. The outputs of two CTLEs are then connected to perform addition. Finally, multiplication is implemented by duplicating the corresponding CTLE circuit. For instance, as shown in Fig. 6.6, the CTLE circuit of RX Channel 0 (CH0) calculates $y_0 = (w_0 - w_1) + (w_2 - w_3)$ by connecting the outputs of two CTLEs. A third CTLE, with a pair of reference voltages as inputs, is

also connected to the outputs to compare the results with the differential reference voltages. For instance, in the first row of the schematic in Fig. 6.6, the CTLE decoder calculates $(w_0 - w_1) + (w_2 - w_3) - (V_{\text{REF2}} - V_{\text{REF0}})$ and then feeds the differential output pair to a comparator to compare $(w_0 - w_1) + (w_2 - w_3)$ with $(V_{\text{REF2}} - V_{\text{REF0}})$. The outputs of the CTLE decoder in RX CH0 are

$$\text{VOP}_{00} - \text{VON}_{00} = (w_0 - w_1) + (w_2 - w_3) - (V_{\text{REF2}} - V_{\text{REF0}}) \quad (6.2)$$

$$\text{VOP}_{01} - \text{VON}_{01} = (w_0 - w_1) + (w_2 - w_3) - (V_{\text{REF1}} - V_{\text{REF1}}) \quad (6.3)$$

$$\text{VOP}_{02} - \text{VON}_{02} = (w_0 - w_1) + (w_2 - w_3) - (V_{\text{REF0}} - V_{\text{REF2}}) \quad (6.4)$$

This CTLE decoder with three input pairs ensures that the PAM4 signals are decoded and compared to differential reference voltages. Because the CTLE decoder uses differential reference voltages, it suppresses CMN originating not only from signals but also from reference voltages.

Figure 6.7 illustrates the eye diagram after decoding, i.e., the eye diagram of signals $\mathbf{y}$ as calculated by Eq. 5.5. Here, V_s denotes the voltage swing of the signals before decoding. The signal levels after decoding are $\{-6/9V_s, -2/9V_s, +2/9V_s, +6/9V_s\}$, whereas the signal levels before decoding are $\{0, 1/9V_s, 2/9V_s, \dots, V_s\}$. The reference voltages $\{-4/9V_s, 0, +4/9V_s\}$ are implemented using differential pairs $\{8/9V_s - 4/9V_s, 6/9V_s - 6/9V_s, 4/9V_s - 8/9V_s\}$.

In NRZ and PAM4 modes, the CTLE decoder functions as a conventional CTLE. In NRZ mode, one out of the three CTLE decoder is enabled. All of its input pairs are connected to w_i and V_{REF1} . In PAM4 mode, all CTLE decoders are enabled. For each CTLE decoder, all input pairs are shorted and connected to w_i and V_{REF0} , w_i and V_{REF1} , and w_i and V_{REF2} , respectively.

6.3 Measurement Results

The proposed transceiver was realized using a 28nm CMOS technology. The layout was automatically generated by a template-driven generator, utilizing a standard digital place-and-route (P&R) flow. The die and package photographs are shown in Fig. 6.8. The silicon

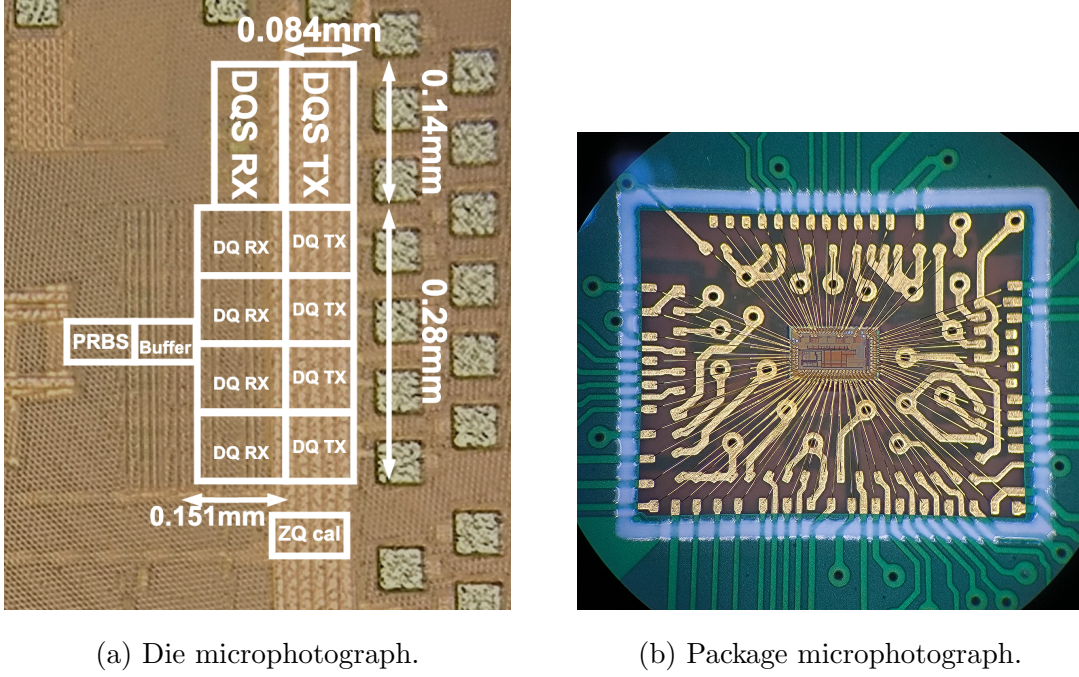


Figure 6.8: Prototype combo-PHY photos.

area occupied by the transceiver is 0.016mm^2 per lane. Performance measurements were conducted with 20mm channels under different supply voltages: 0.6V for DDR NRZ mode and 0.8V for UCIE NRZ, PAM4 and CPAM4 mode. A Tektronix MSO06 oscilloscope equipped with passive probes were employed for TX eye measurements. RX data are captured by oscilloscope and transfer to computer(PC) for BER analysis. The measurement stations are shown in Fig. 6.9.

Fig. 6.10 presents the measured eye diagrams in various modes using PRBS15 pattern. Fig. 6.10 (a) and (b) illustrate the eye diagrams for CPAM4 mode with a data rate of 5.25 Gbps/pin at the end of 20 mm channel. Fig. 6.10(a) shows the measured 10-signal-level TX output (w_0) eye diagram. Due to the presence of noise and channel loss, the TX output eye is closed. However, Fig. 6.10(b) reveals the decoded PAM4 signal (qo_0) eye diagram can still be successfully recovered without the need for equalization. Nevertheless, the measured jitter of the decoded PAM4 eye diagram is higher than anticipated, primarily attributing to

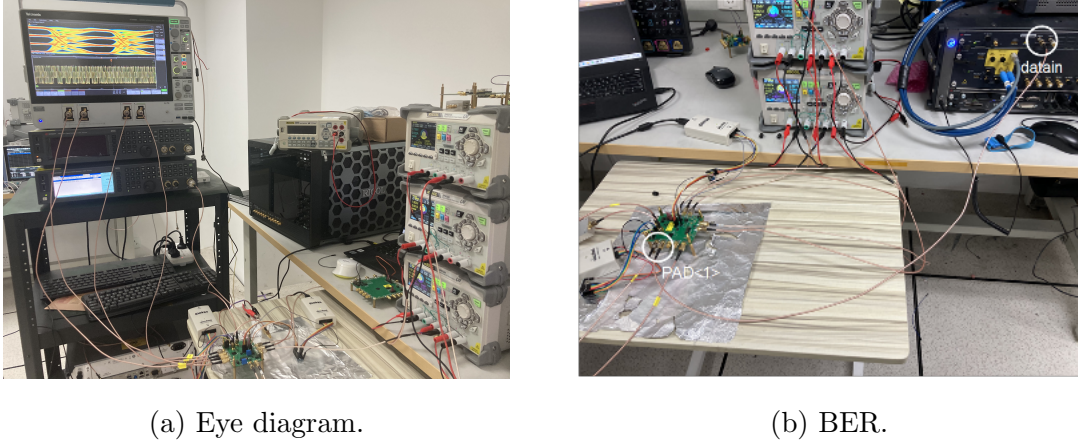


Figure 6.9: Measurement stations.

the lane skew introduced by probe cables during measurement. Fig. 6.10 (c) depicts the eye diagram for UCIE NRZ mode at a data rate of 4.6 Gb/s/pin. The measured eye diagram comfortably meet the 40 mV eye diagram mask requirement specified by the UCIE standard [58]. Fig. 6.10(d) shows the eye diagram for PAM4 signaling at a data rate of 7 Gb/s/pin. The proposed transceiver achieves higher data rate in PAM4 mode compared to UCIE NRZ but with reduced eye opening due to the signal complexity.

Fig. 6.11 illustrates measured total current variation of 4-wire CPAM4-6 transmitters and 3-wire PAM4 transmitters. The trend of current variation matches the derived result in Fig. 5.5. The current variation in CPAM4-6 mode remains within 6.77% with a 3.74% standard deviation, while in PAM4 mode it fluctuate by up to 63.4% with a 23.5% standard deviation. This result demonstrates that CPAM4-6 effectively alleviates output driver current fluctuation and suppresses SSN.

Fig. 6.12 shows measured CPAM4-6 eye diagrams with ± 100 mV power supply noise. The eye diagram is measured at 2.1Gb/s/pin. When the power supply noise is injected, the pre-decode eye diagram is closed. After decoding, the eye diagram is effectively recovered with only 4 mV to 20 mV eye height attenuation. This power supply noise rejection is

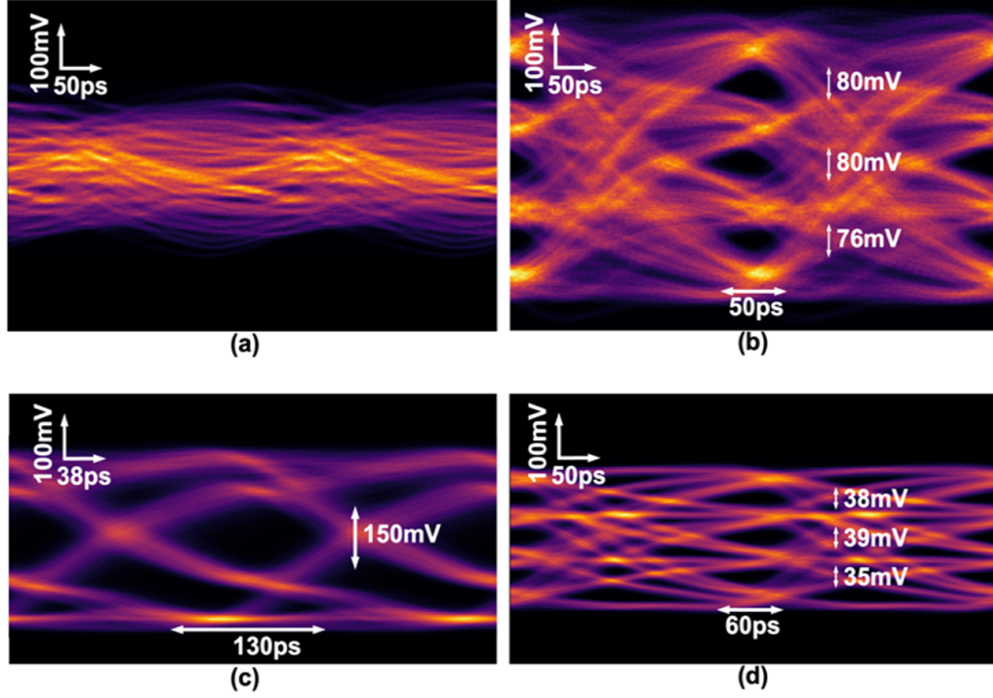


Figure 6.10: TX eye diagram in different modes (a) CPAM4 before decoding, corresponding to TX output (w_0) (b) CPAM4 after decoding, corresponding to CTLE DEC output (q_0) (c) UCIE NRZ (d) PAM4

because the majority of power supply noise is in common mode as four channels of CPAM4-6 transceivers share a power distribution network. As discussed in Section III, CPAM4-6 rejects CMN after decoding due to inherently differential decoder.

Fig. 6.13 shows measurement results of the VREF generator. The blue curve depicts measured VREF1 voltages with the internal bandgap output VBG, whereas the red curve depicts measured VREF1 voltages with VBG from an external voltage source. The external VBG voltage is 550mV, which is equal to the nominal internal VBG voltage. Ideally, the red curve and blue curve should be identical given the external VBG voltage is equal to the internal VBG voltage. However, VREF1 with external VBG is higher than VREF1 with internal VBG. This is mainly because the internal VBG voltage is lower than expected

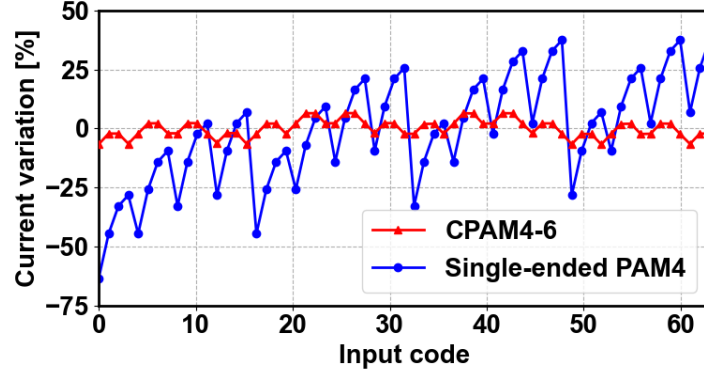


Figure 6.11: Measured total current variation versus 6-bit input data of 4-channel CPAM4-6 and 3-wire single-ended PAM4 transmitters.

due to malfunction in start up circuit in the bandgap circuit. The ranges of VREF1 are $[113mV, 338mV]$ and $[157mV, 576mV]$ with internal VBG and external VBG, respectively. The higher boundary meets the requirement, whereas the lower boundary is higher than expected. The measured VREF1s are linearly approximated by

$$\begin{aligned}\widehat{VREF1}_{in} &= 1.06 * code + 67.06 \\ \widehat{VREF1}_{ex} &= 1.88 * code + 96.55\end{aligned}\tag{6.5}$$

The step of VREF1 with external VBG is 1.88mV which is close to the simulation result, while step of VREF1 with internal VBG is lower than expected, mainly because of low internal VBG voltage. When the control code is lower than 50, VREF1 deviates from its linear approximation, which also causes the lower boundary of VREF1 to be not as low as expected. This is because the opamp does not operating in the saturation region when the control code is small. It may lead to higher BER especially when the eye height of the eye diagram is small. Fig. 6.14 illustrates measured delay of the DQS delay line versus the control codes. The DQS delay line is configured by 8-bit control codes. The DQS delay line consists of a coarse delay line and a fine delay line. The purpose of this coarse-fine design is

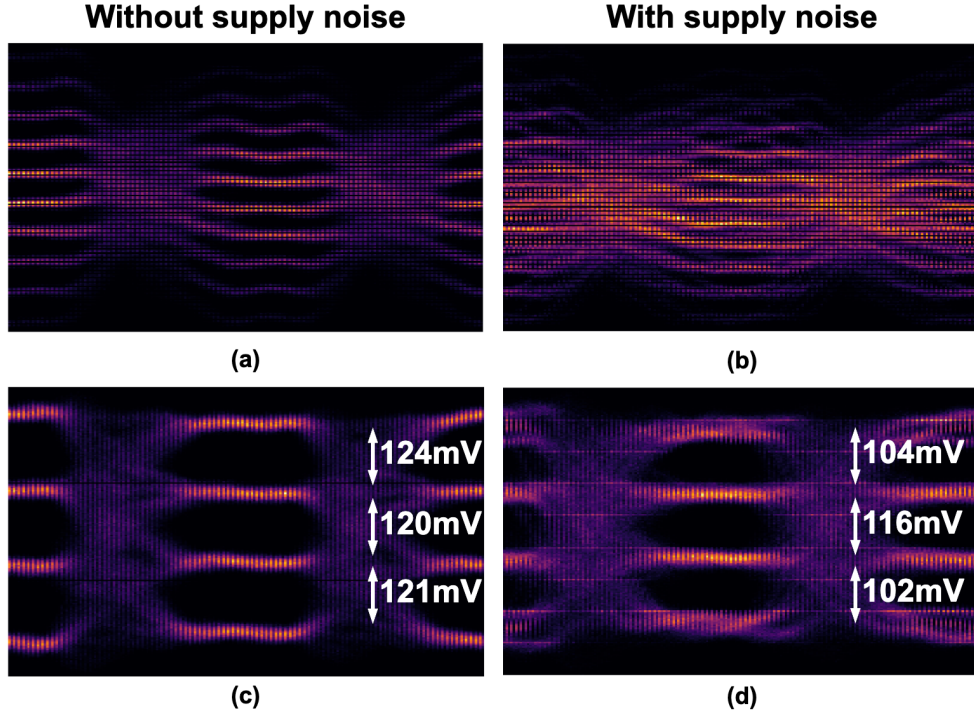


Figure 6.12: Measured eye diagrams for CPAM4-6 with ± 100 mV power supply noise: pre-decode eye (a) without power supply noise and (b) with power supply noise; decoded eye (c) without power supply noise and (d) with power supply noise.

to cover a wide range of delay while maintaining high resolution to meet the specification. Three bits of control codes take charge of the coarse delay line, while five bits of control codes control the fine delay line.

Table 6.2 summarizes the comparison between the proposed transceiver using CPAM4 and prior works. The results demonstrate that the proposed CPAM4 signaling achieves the highest pin efficiency among multi-level and multi-wire signaling schemes. The transceiver achieves energy efficiencies of 0.557 pJ/b, 1.128 pJ/b, 0.768 pJ/b, and 1.161 pJ/b, in DDR NRZ, UCIE NRZ, PAM4 and CPAM4 mode, respectively. The measured bit error rate (BER) in UCIE NRZ, PAM4, and CPAM4 mode is below $1e-9$, $1e-6$, and $1e-8$, respectively. Due to

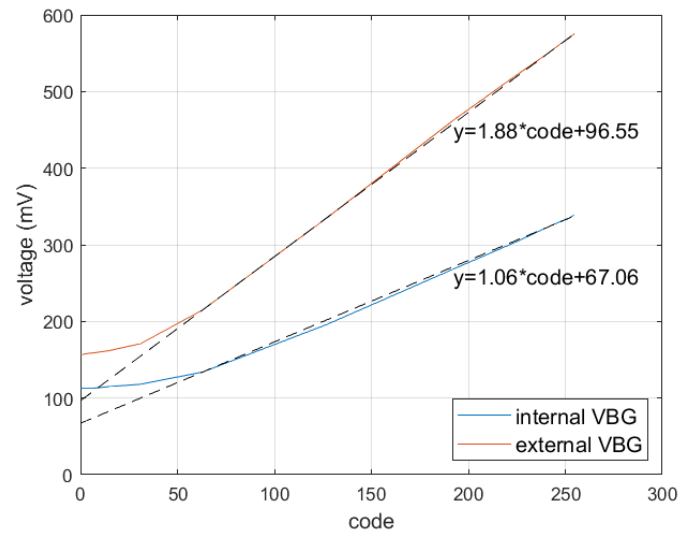


Figure 6.13: Measured VREF voltage VS control code.

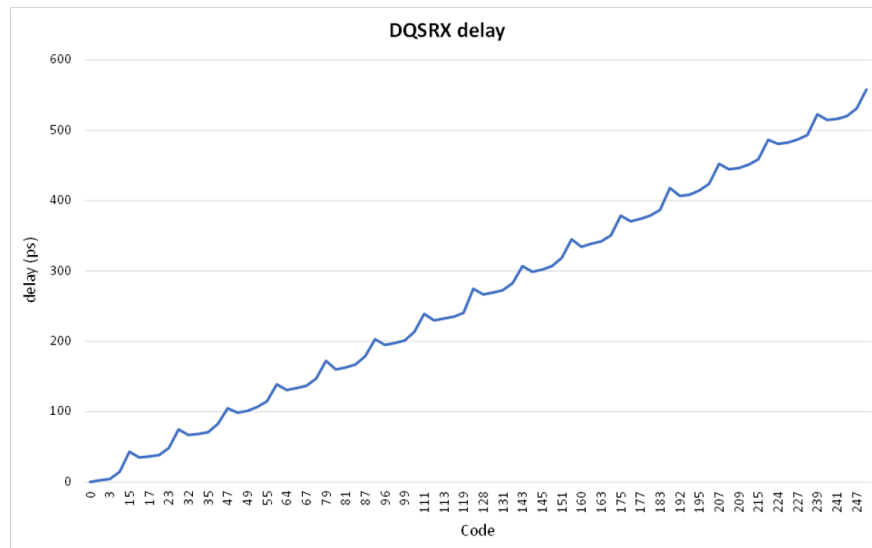


Figure 6.14: Measured DQS delay VS control code.

Table 6.2: Comparison table of the proposed transceiver using CPAM4 signaling between prior works

Reference	JSSC 2016	JSSC 2020	IEEE Access 2022	This work
Signaling	4B4W4L	CNRZ-5	CNRZ-7	CPAM4
Pin efficiency	100%	83.3%	85.7%	150%
ISI ratio	3	1	1	3
Technology	65nm CMOS	16nm FinFET	28nm CMOS	28nm CMOS
Supply (V)	1.2	1.1	N/A	0.8
Channel	30mm FR4	2” FR4	50mm die-to-die	20mm FR4
Driver type	CML	SST	SST	SST
Equalization type	Capacitive pre-amphasis	CTLE	CTLE	CTLE
Data rate (Gb/s/pin)	8	20.83	35	5.25
Energy efficiency (pJ/b)	2.39	1.02	1.1	1.19
Core area (mm^2)	0.52	0.63	0.66	0.066

the limitations of the testing equipment, the maximum testable frequency is approximately 4.6 GHz.

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