# CMOS RF Energy Harvester IC Development

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## Abstract

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This thesis details the design, simulation, and optimization of a Radio Frequency Energy Harvester (RF-EH) utilizing a 180nm Complementary Metal-Oxide Semiconductor (CMOS) process. The device operates at 2.4 GHz ISM band, converting ambient RF energy into DC (Direct Current) power, ideal for low-energy wireless devices. Key features include a rectifier circuit, a 180-degree phase shifter, and a charge pump voltage multiplier. With an input power of 0 dBm, the system achieves an 18.11% efficiency, using a 70kΩ load and five CP stages. The efficiency peaks at 32.11% at 10 dBm input. This foundational work paves the way for future research targeting enhanced efficiency and optimizing circuit design for practical applications.

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# DEDICATION

This thesis is dedicated to my incredible parents, who have been the unwavering pillars of support throughout my educational journey. Their continuous encouragement and firm belief in my capabilities have served as my driving force, particularly in times of challenges and uncertainties.

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I am immensely grateful to each of you for believing in me and for your significant roles in shaping my path. It is with great pride and humility that I present this thesis in honor of your collective faith and support.

# Chapter 1. INTRODUCTION

This thesis discusses designing and analyzing a Radio Frequency Energy Harvester (RF-EH) implemented in TSMC (Taiwan Semiconductor Manufacturing Company) 180nm technology. The motivation for this research stems from the increasing demand for energy-efficient, sustainable solutions to power the vast network of wireless devices that form the backbone of our digital world. As the Internet of Things (IoT) expands, the need for remote, low-maintenance power sources becomes more critical.

RF-EHs offer a promising solution, with the capability to convert ambient RF energy, prevalent in our environments due to extensive wireless communication, into usable DC (Direct Current) power. This study focuses on enhancing the efficiency of RF-EHs operating at 2.4 GHz, a commonly used frequency band in wireless communications.

The 2.4GHz frequency band is particularly interesting in the context of RF Energy Harvesting due to its widespread use and potential for energy collection. This band, part of the Industrial, Scientific, and Medical (ISM) radio bands, is globally available and unlicensed, meaning it can be freely used without requiring regulatory permissions.

Most notably, the 2.4GHz band is home to several prevalent wireless technologies, including Wi-Fi (IEEE 802.11b/g/n), Bluetooth, and ZigBee, which are extensively used in the current Internet of Things (IoT) paradigm. As a result, the environment is rich with 2.4GHz RF signals, providing a copious source of ambient energy for harvesting.

The ISM bands were initially reserved for using RF electromagnetic fields for industrial, scientific, and medical purposes other than telecommunications. However, due to the relative lack

of telecommunications traffic within these bands, ISM bands are now heavily used for unlicensed communications applications, including Wi-Fi and Bluetooth devices.

Moreover, harvesting energy from the 2.4GHz band makes practical sense due to the ubiquity of the signals in both residential and industrial areas. RF Energy Harvesting systems designed to tap into this frequency band can leverage the pervasive wireless infrastructure, essentially transforming the 'waste' RF signals into a usable energy source, contributing to the efficiency and sustainability of wireless communication networks.

Therefore, the utilization of the 2.4GHz ISM band for RF Energy Harvesting provides an opportunity to recycle the abundant ambient energy, making the technology an attractive solution for powering future low-power devices and sensors in the expanding IoT ecosystem.

The thesis starts with a review of the basic principles of RF energy harvesting and an overview of the state-of-the-art technologies and techniques in this field. This helps establish the context for the proposed design and the need to improve existing methodologies.

Following this, the design and optimization of a RF-EH is presented. The RF-EH comprises a charge pump rectifier and a 180-degree phase shifter for maximum power transfer. Careful attention has been given to the choice of input power to meet the Federal Communications Commission's (FCC) regulations regarding Effective Isotopically Radiated Power (EIRP) and the availability of standard antennas.

The design process has been validated using Cadence Virtuoso for circuit layout and simulation. Issues concerning the physical layout, Design Rule Check (DRC), and Layout Versus Schematic (LVS) are also discussed, ensuring the design is ready for fabrication.

Finally, the thesis concludes with an assessment of the project's outcomes, along with directions for future research. This includes reflections on the study's contributions, the applicability of the design, and suggestions for enhancing the RF-EH's efficiency further.

By presenting a comprehensive exploration of the design and optimization of RF-EH, this thesis contributes to ongoing efforts toward creating sustainable, energy-efficient solutions for powering our digital future.

## 1.1 Background and Motivation

A novel CMOS RF Energy Harvester was introduced in [1] Figure 1, which presents a fully integrated single-chip solution in 130nm CMOS technology designed to harvest energy from RF signals and achieve higher RF-to-DC conversion efficiency compared to previous studies. RF-EH employs the Dickson Charge Pump (CP) principle [2], known for its high multiplying efficiency and current driving technique, making it ideal for implementation on a fully integrated chip. The first prototype of the RF-EH design described in [1] was built and tested in [3].

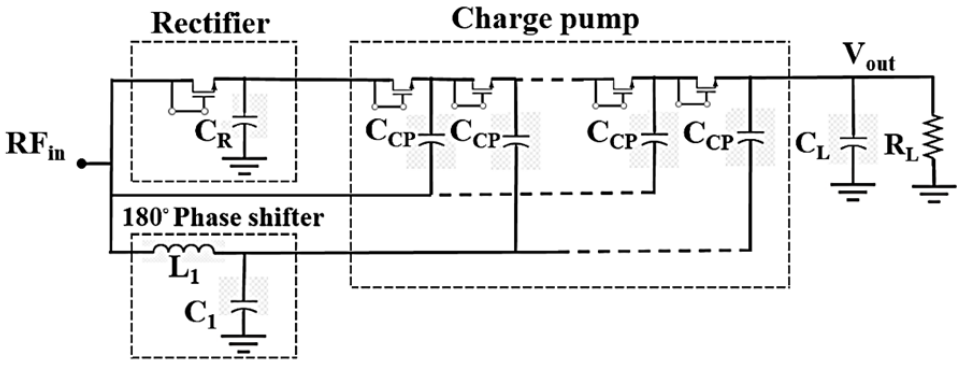


Figure 1 Circuit Diagram of the proposed Single-Band Energy Harvester [1].

## 1.2 Research Objectives and Approaches

The proposed research aims to address the need for energy-harvesting solutions for low-power wireless devices. By developing a high-performance CMOS RF energy harvester, this thesis seeks to demonstrate the feasibility of using ambient RF energy sources to power low-power devices. The results of this research will be helpful in future energy harvesting studies and contribute to developing sustainable energy solutions. The main objectives of this thesis are:

1. To design a high-performance CMOS RF energy harvester for low-power applications.
2. To optimize the circuit design to maximize efficiency and output power.
3. To simulate the circuit under various conditions to verify performance and identify potential issues.
4. To implement the circuit layout and prepare it for fabrication (tape-out).

To achieve the objectives mentioned, the proposed methodology for this thesis involves the following steps:

1. Identify and optimize components for each network; Impedance Matching Networks, rectifier, Dickson Charge Pumps, and 180-degree phase shifter.
2. Design, optimize, and simulate the circuit using the TSMC 180nm design package embedded in Cadence. The design will involve selecting component values, size, and connections to achieve the desired circuit behavior.
3. The optimization step will involve refining the circuit design to meet specific performance criteria, such as minimizing power consumption and maximizing output

power. Simulations will be run to test the circuit's performance under various conditions and verify that the circuit meets the required specifications.

Implement the circuit layout using the Cadence Virtuoso layout tool and prepare for fabrication. The circuit layout will involve arranging the components to optimize the physical space available and minimize interference between components. Once the layout is finalized, it will be prepared for tape-out, which involves preparing the design files for fabrication at a commercial process foundry such as TSMC.

## 1.3 Contribution of the Thesis

The primary contribution of this thesis is the development of a CMOS RF energy harvester IC for use in wireless sensor networks. By designing, simulating, and laying out the circuit using TSMC 180nm technology, we have demonstrated the feasibility of using CMOS technology for efficient energy harvesting in the 2.4GHz range. The thesis also contributes to the body of knowledge on RF energy harvesting by presenting a comprehensive literature review of the field and discussing the design and performance of the proposed harvester IC.

Furthermore, this thesis contributes to the practical application of RF energy harvesting by building upon previous proof of concept studies. By demonstrating the efficacy of the harvester IC design through experimental evaluation and comparison with existing designs, this thesis provides a foundation for future research and development in this field.

## 1.4 Organization of the Thesis

The thesis is organized into five main chapters, each focusing on a different aspect of the RF energy harvester IC design and evaluation. Chapter 1 provides an introduction to the research questions and objectives, a review of the relevant literature, and an overview of the thesis

organization. Chapter 2 presents a comprehensive literature review of RF energy harvesting, including existing CMOS designs and related proof of concept studies.

Chapter 3 describes the design and simulation of the proposed harvester IC, including the rectifier and voltage multiplier circuits, and presents a power output analysis. Chapter 4 details the layout and fabrication process of the harvester IC using TSMC 180nm technology.

Finally, Chapter 5 provides a summary of the thesis, discusses the contributions of the work, and outlines directions for future research. Overall, this organization provides a logical progression from literature review to design and simulation, layout, fabrication, and finally, evaluation and summary of the proposed harvester IC design.

# Chapter 2. LITERATURE REVIEW

The rapid growth of wireless technologies has given rise to a proliferation of low-power devices, such as sensors and Internet of Things (IoT) devices, which require reliable and sustainable power sources. RF energy harvesting (EH) has emerged as a promising solution to address this challenge, as RF electromagnetic energy is widely available. The wireless RF energy harvester utilizes a wireless antenna to capture RF energy and convert it into DC voltage. The availability of 66 μW of RF energy for the GSM and ISM bands has been demonstrated in [4]. However, there are known challenges in receiving antennas in specific geographic locations, for example, distance from the antenna and buildings in dense cities that can affect the received power levels at the antenna. A standard energy harvesting (EH) block consists of several key components, including an RF antenna, matching network, rectifier, Charge Pump, and charge storage devices. The RF signal is received by the antenna, converted to DC by the rectifier, amplified by the Charge Pump, and then stored in a battery or delivered directly to the load. The increasing demand for implantable biomedical devices and remote sensors has led to a growing interest in the ability to harvest RF electromagnetic energy from the environment. These devices are limited by their finite battery life. However, the potential solution to this challenge is supported by several studies that have demonstrated the potential of RF-EH for various applications [5]-[9]. The performance of RF-EH systems is reviewed in [10]-[16], considering the input power level, DC load, and fabrication process.

## 2.1 Overview of RF Energy Harvesting

RF energy harvesting is a promising technology that has gained substantial traction in recent years, predominantly for powering low-power electronic devices in applications such as wireless

sensor networks and the Internet of Things (IoT). This technology capitalizes on ambient radio frequency signals in the environment, converting them into usable electrical energy. The process of RF energy harvesting hinges on the principle of rectification, where an antenna captures RF signals, and a rectifier circuit transforms the alternating current (AC) signal into direct current (DC) power. The harvested energy can either be stored in a battery or directly utilized to power small-scale electronic devices.

A significant advantage of RF energy harvesting is its potential for continuous or even perpetual operation, eliminating the need for battery replacement. This technology offers a more sustainable and eco-friendlier alternative by harnessing energy from existing RF sources such as Wi-Fi networks, cellular towers, and other wireless communication systems. Furthermore, RF energy harvesting facilitates the deployment of self-sustaining wireless sensor networks in remote or hard-to-reach locations where battery replacement is impractical or costly.

Despite its advantages, RF energy harvesting presents several challenges, including limited power availability from RF sources, efficiency constraints of rectifier circuits, and the need for precise antenna design and impedance matching. Developing efficient and optimized RF energy harvesting circuits and systems is crucial to address these challenges, enabling maximum power extraction and enhancing overall system performance.

This thesis will explore designing and developing a CMOS RF energy harvester IC for the 2.4GHz frequency range, leveraging TSMC 180nm technology. By tackling these challenges and leveraging the benefits of CMOS technology, this research seeks to contribute to the field of RF energy harvesting, pushing the boundaries of efficient and reliable power generation for wireless sensor networks and IoT devices.

## 2.2 CMOS Technology for RF Energy Harvesting

Complementary Metal-Oxide-Semiconductor (CMOS) technology is increasingly favored in the field of RF energy harvesting, primarily due to its compatibility with integrated circuit (IC) fabrication processes and its potential for low power consumption. CMOS technology presents several benefits, including cost-effectiveness, high integration density, and the potential for system-on-chip (SoC) implementation, making it an attractive choice for RF energy harvesting circuit design.

In RF energy harvesting systems employing CMOS technology, the rectifier circuit plays a pivotal role, converting the AC signal from the antenna into DC power. Various CMOS rectifier topologies, such as the voltage doubler, Dickson charge pump, and full-wave bridge rectifiers, have been proposed and explored to efficiently rectify the RF signal and minimize power losses, thereby maximizing the harvested energy.

Furthermore, CMOS technology facilitates the integration of additional components within the RF energy harvester IC, including impedance-matching networks, power management circuits, and energy storage elements. This integration reduces overall footprint, cost, and power consumption, while simultaneously enhancing system performance and efficiency. CMOS technology also enables the implementation of advanced power management techniques, such as duty cycle control and adaptive impedance matching, further boosting the energy harvesting process.

This thesis will focus on designing and developing a CMOS RF energy harvester IC using the TSMC 180nm process by adopting CMOS technology. The integration of CMOS-based rectifier circuits, impedance-matching networks, and other essential components on a single chip promises efficient energy harvesting within the 2.4GHz frequency range. This research

contributes to the advancement of RF energy harvesting systems, fostering the development of compact, low-power, and cost-effective solutions for powering wireless sensor networks and IoT devices.

## 2.3 Related Work on RF Energy Harvesting Proof of Concept

The RF energy harvesting field has seen tremendous development over the past years. Numerous studies have been conducted in this field to build prototypes and produce promising results. This section delves into the most significant breakthroughs made, using a 1 MHz frequency for the initial proof of concept and a 900 MHz frequency for the subsequent PCB design.

### 2.3.1 *Proof of concept using 1MHz frequency*

Our preliminary proof of concept focused on utilizing a 1 MHz frequency. This frequency was chosen due to its widespread use in several RF devices, allowing for potentially significant ambient energy sources. Moreover, 1 MHz falls within the frequency range that can be effectively converted to DC power through energy-harvesting circuits.

During this phase, the key aim was to verify the feasibility of the RF energy harvesting concept. We built a simple setup consisting of an RF energy harvester circuit connected to a low-power device. The testing was conducted under controlled conditions, with a fixed RF source emitting at 1 MHz. Figure 2. 1 shows the block diagram of 1MHz RF-EH proof of concept.

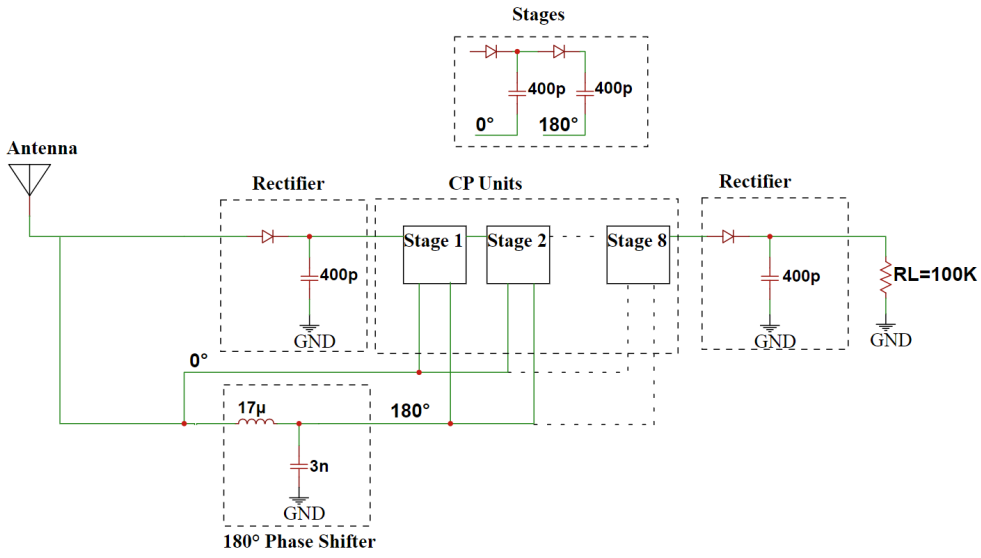


Figure 2. 1 1MHz RF-EH Proof of concept block diagram

The results were promising, as the harvester efficiently collected and converted the RF energy. The low-power device attached to the harvester remained operational throughout the testing period, solely powered by the harvested energy.

We selected the commonly used 1N34A Schottky diode to simulate and construct the circuit on a breadboard. Thanks to its low forward voltage drop and fast switching capability, the diode's characteristics made it ideal for our proof of concept.

To calculate the 180-degree phase shifter, we employed the following equation:

$$\omega^2 L_1 C_1 = 2.0 \quad (1.1)$$

We then selected readily available values from our lab for the inductor ($L_1$) and capacitor ($C_1$). Based on this equation, we chose $L_1 = 17\mu H$ and $C_1 = 3nF$.

Figures 2. 2 and 2. 3 below illustrate the input and output voltages, respectively, clearly representing the circuit's performance.

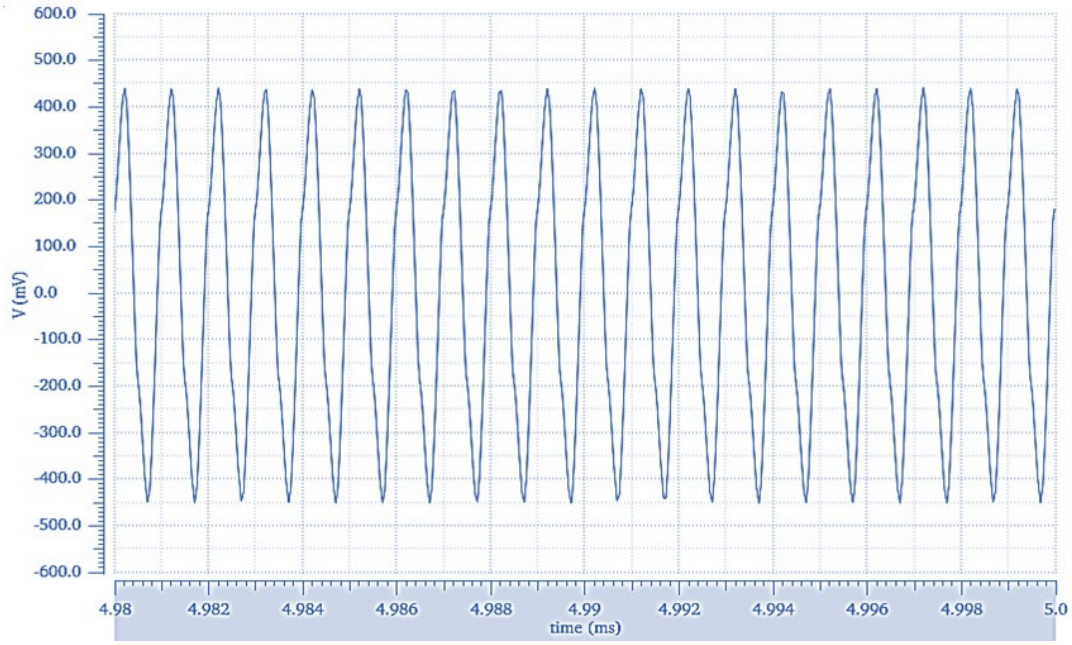


Figure 2. 2 1 MHz input 0dBm

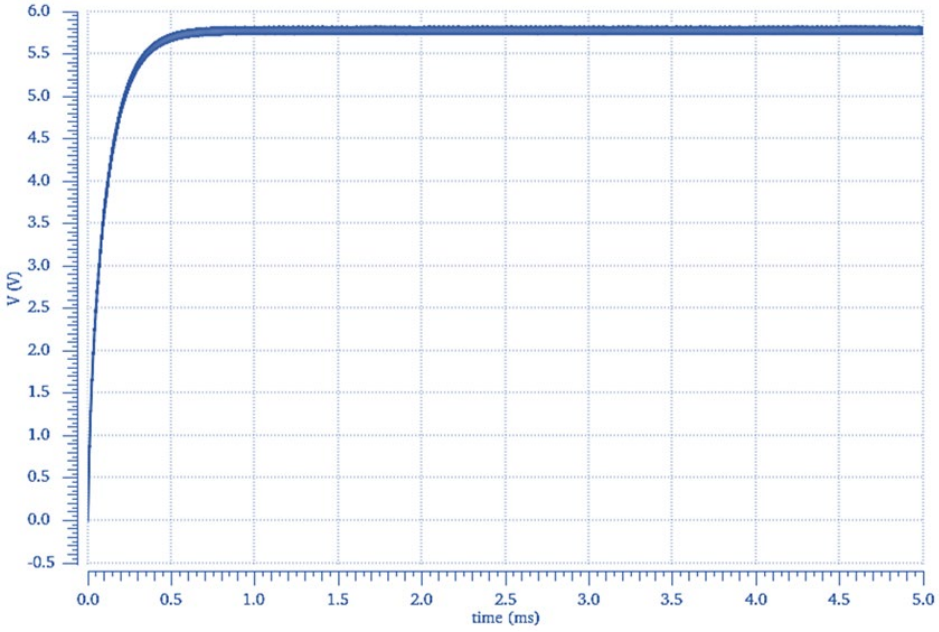


Figure 2. 3 1MHz RF-EH DC output across 100KΩ resistor.

We then calculated the input and output power to derive the system's efficiency. This measurement enabled us to evaluate how effectively our energy harvesting system converted the RF energy at 1 MHz into usable DC power.

The table below documents several design tests we performed on this 1 MHz EH system, noting the varying efficiencies with different configuration parameters.

Table 2. 1 CP Units Optimization of 1MHz EH system

| # of CP | $V_{rms}$ | $I_{rms}$(A) | $V_{dc}$ (V) | $I_{dc}$ (A) | $P_{in}$ (W) | $P_{out}$ (W) | Ƞ (%) |
|---|---|---|---|---|---|---|---|
| 5 | 3.098E-01 | 5.29E-03 | 3.467 | 4.953E-05 | 1.64E-03 | 1.717E-04 | 10.49 |
| 8 | 2.960E-01 | 4.29E-03 | 4.8 | 6.900E-05 | 1.27E-03 | 3.312E-04 | 26.06 |

As indicated in the table, optimizing the values and stages of the charge pump (CP) significantly affects the system's efficiency. Notably, we optimized our 1 MHz EH system with eight stages of the CP, resulting in a substantial efficiency increase to a threshold of 26.06%. However, it is essential to note that while these eight stages provided the optimum results, adding more than eight CP stages led to decreased efficiency, and fewer than eight stages also resulted in less efficiency.

This observation points to an important design consideration, suggesting a balance in the number of CP stages for optimal energy conversion efficiency. The exact number may vary depending on the specific characteristics of the RF source and the circuit components. Still, our results suggest that around eight stages could serve as a good starting point for 1 MHz RF energy harvesting systems.

After successfully performing measurements and calculations in our simulation environment and obtaining the maximum efficiency, our next step was to validate the simulation results in a

real-world scenario. To accomplish this, we sought to implement our design in a prototype device and conduct necessary measurements without relying solely on idealized conditions as assumed in Cadence simulations.

We, therefore, implemented the 1 MHz EH system on a breadboard, optimizing the prototype's components based on their availability in the market. It's worth noting that the values of the components used for the 1 MHz prototype are not exact, but they are close to those used in the Cadence simulations, allowing for some tolerance. This approach allowed us to maintain the integrity of our design while adapting to the realities of available components.

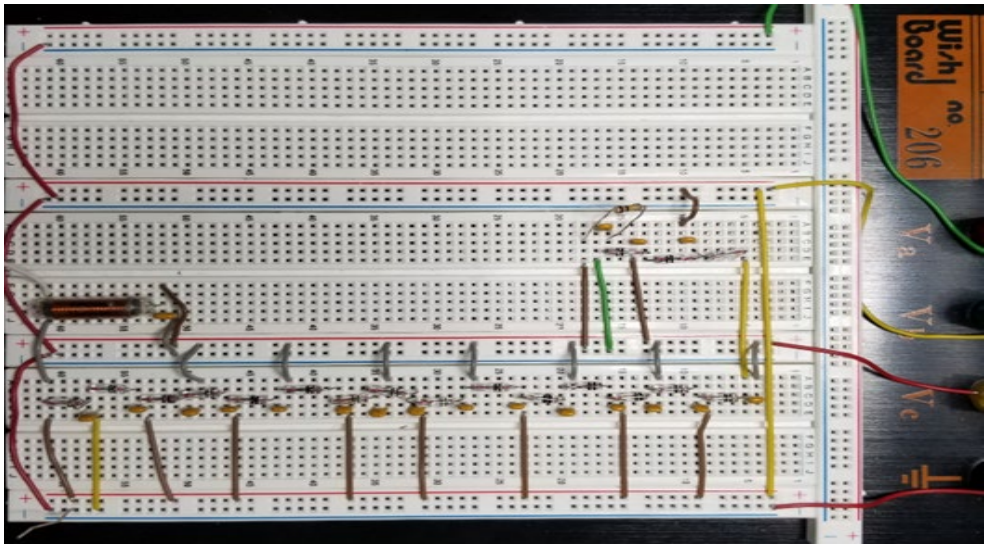


Figure 2. 4 1 MHz prototype assembled on the Breadboard

Creating a physical prototype allowed us to verify our simulations' results and explore the nuances of RF energy harvesting under practical conditions. This hands-on testing allowed us to see the effects of non-ideal components and other real-world factors that may not be captured in our initial simulations, providing a complete understanding of our 1 MHz energy harvesting system.

The energy harvesting (EH) prototype was tested using a 1MHz RF input signal. This signal was sourced directly from a function generator, set to a voltage swing of 1Vpp, to align with the input power we anticipated based on our simulations and the power present in the ambient environment.

Measurements were taken using an oscilloscope, as illustrated in Figure 2. 5 below. This figure shows the input AC signal (blue) compared to the output DC voltage (green). Additionally, measurements were taken to calculate the efficiency of our system, and these results are shown in the following table.

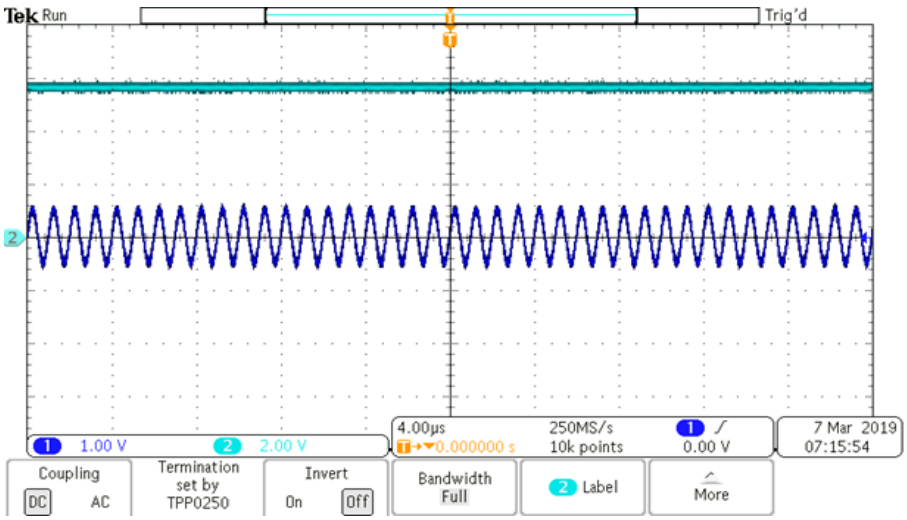


Figure 2. 5 RF input (blue) Vs. DC output (green) measured on Oscilloscope

As Figure 2. 5 illustrates, the calculated power of the 1MHz EH system was found to be 1.59mW, with an output voltage of 4.4V and a conversion efficiency of 7.35%.

When comparing these results with those of our Cadence simulation, we observed a significant drop in efficiency - a decrease of 73%. This can be attributed primarily to the shift from an ideal to a nonideal environment and the varying tolerances of our components. There

was also additional resistance in our prototype that should have been considered in our simulation, which could contribute to this discrepancy.

These real-world challenges underscore the importance of considering practical constraints and potential variations when moving from simulation to actual implementation. Despite these hurdles, the proof of concept demonstrated the feasibility and potential of the RF energy harvesting system.

### 2.3.2 *PCB design for 900MHz frequency*

Based on the successful preliminary results with the 1 MHz frequency, we shifted our focus to a more relevant and widely used frequency band, the 900 MHz. This frequency falls under the ISM band, globally available for Industrial, Scientific, and Medical (ISM) applications without a license. Hence, it presents a practical frequency for real-world RF energy harvesting scenarios.

We designed a Printed Circuit Board (PCB) that houses an RF energy harvester circuit optimized for the 900 MHz frequency. This PCB was created to develop a more compact, efficient, and practical version of our proof of concept. Figure 2. 6 shows the 900MHz RF-EH block diagram.

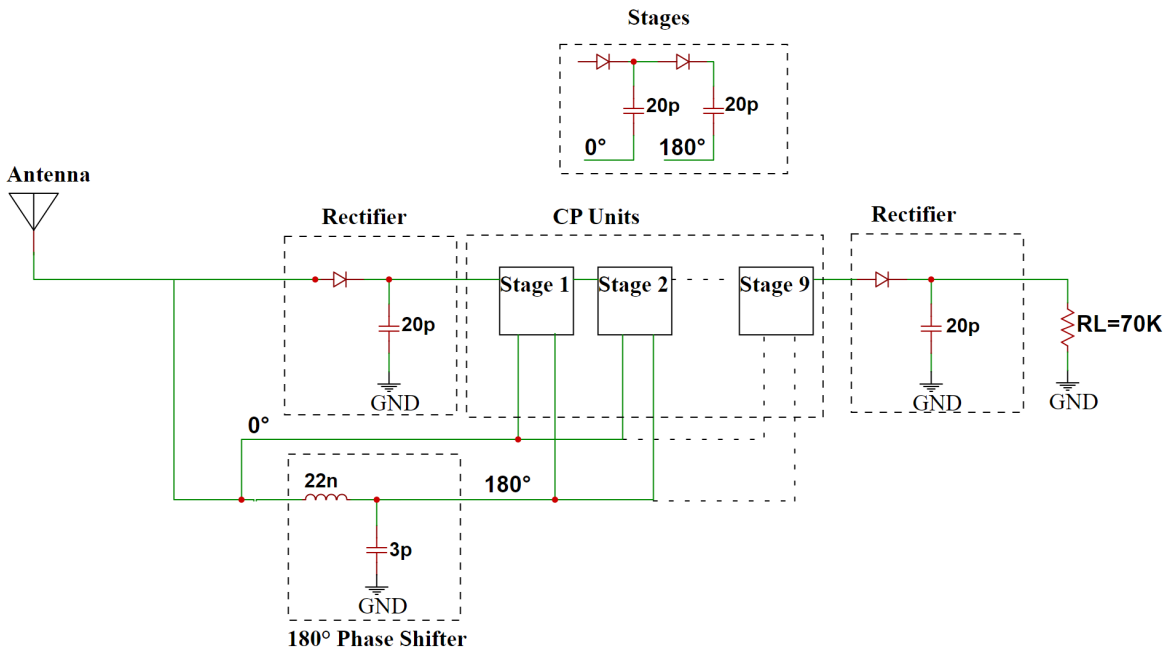


Figure 2. 6 900MHz RF-EH Block Diagram

In particular, for the 900MHz system, we calculated and optimized the values for $L_1$ and $C_1$ using equation 1.1, which were found to be 21.7nH and 3pF, respectively, and optimized to values available in the market.

We selected the SMS7621-079LF Schottky Diode and Surface Mount Device (SMD) components for the diode. According to the diode's data sheet, this particular diode can function up to frequencies as high as 24GHz. This selection was crucial in ensuring the components adequately handled and optimized the 900MHz frequency.

Following the simulations' optimization, measurement, and efficiency calculation, we established the optimal number of charge pump stages for the RF Energy Harvesting (RF-EH) system operating at 900MHz. The determination of these stages was critical in achieving the highest possible efficiency for the RF-EH system at this frequency.

The simulation results have provided key insights into the operation of the RF-EH system at the 900MHz frequency. Figures 2. 7 and 2. 8 display the input and output signals for the system at its peak efficiency.

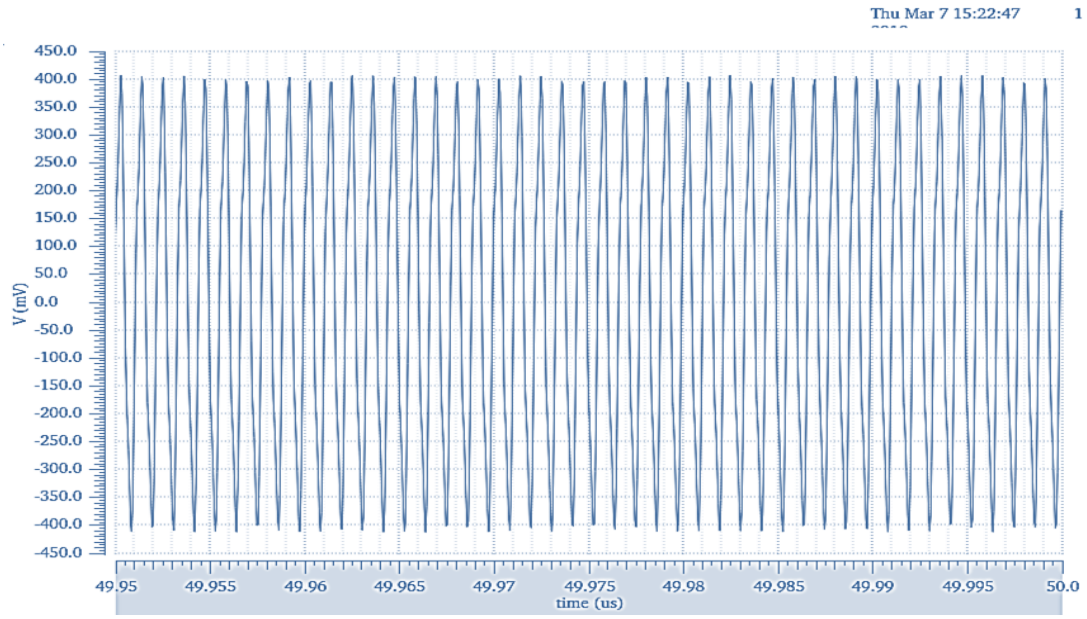


Figure 2. 7 900MHz Input 0dBm

Figure 2. 7 shows the 900MHz RF input signal. It represents the RF energy that the system harvests and converts into a usable form of power. This input signal corresponds to the input power values tabulated.

Figure 2. 8 presents the DC output of the RF-EH system at 900MHz frequency at its peak efficiency. This figure represents the converted power, readily usable for low-power devices and systems. The measurements reflected in this figure align with the output power data in Table 2.1.

These figures visually represent the effective operation of the RF-EH system at 900MHz. The subsequent steps involve translating these simulated results into a physical prototype and further testing to validate the design's real-world efficiency and feasibility.

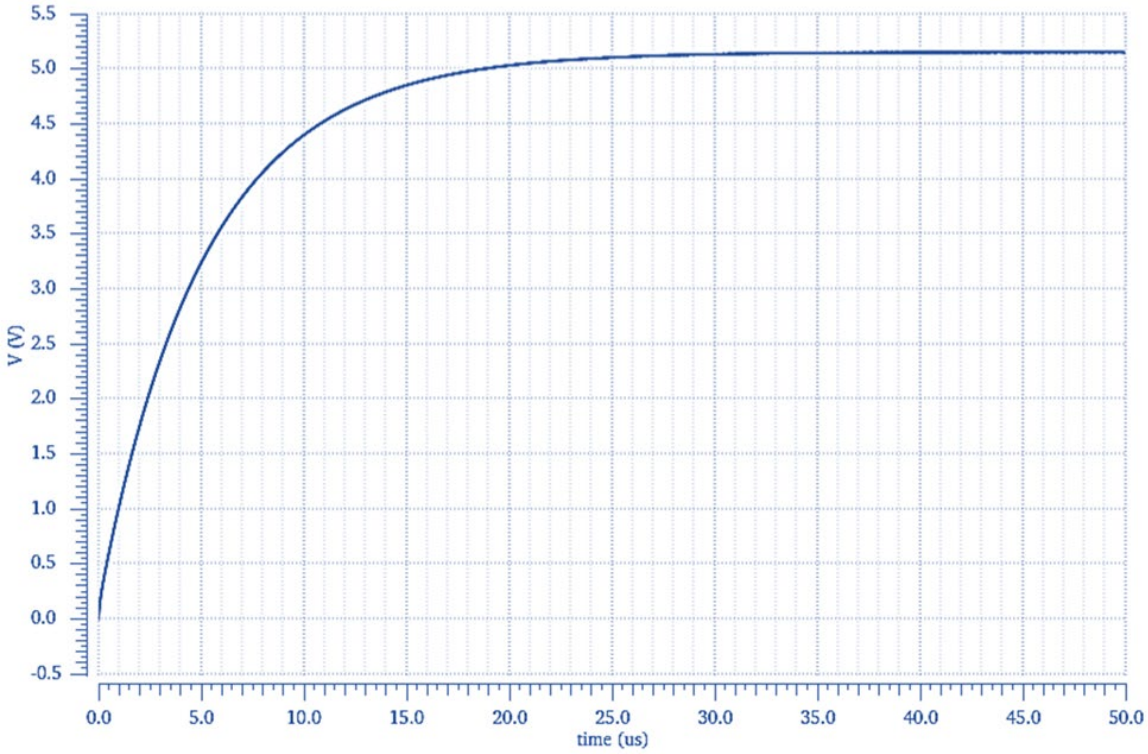


Figure 2. 8 900MHz Dc Output

Figure 2. 8 presents the DC output of the RF-EH system at 900MHz frequency at its peak efficiency. This figure represents the converted power, readily usable for low-power devices and systems. The measurements reflected in this figure align with the output power data in Table 2. 3.

Table 2. 3 below presents the input and output power measurements, along with the calculated efficiency of the system. The different stages of the charge pump are also included in the table to demonstrate the correlation between the charge pump stages and the system's overall efficiency.

Table 2. 2 900MHz RF-EH System Efficiency Calculation

| # of CP | $V_{rms}$ | $I_{rms}$(A) | $V_{dc}$ (V) | $I_{dc}$ (A) | $P_{in}$ (W) | $P_{out}$ (W) | η (%) |
|---|---|---|---|---|---|---|---|
| 7 | 2.840E-01 | 4.41E-03 | 4.814 | 6.877E-05 | 1.25E-03 | 3.311E-04 | 26.41 |
| 8 | 2.768E-01 | 4.29E-03 | 4.888 | 6.983E-05 | 1.19E-03 | 3.413E-04 | 28.76 |
| 9 | 2.688E-01 | 4.11E-03 | 5.40 | 7.770E-05 | 1.10E-03 | 4.196E-04 | 37.99 |

These results indicate that the efficiency of the RF-EH system can be maximized through careful optimization of the charge pump stages. Subsequent sections will explore translating these findings into a practical PCB design and prototype, along with wireless testing to confirm the system's functionality in real-world scenarios.

Following the successful proof of concept of the EH system at a 1MHz frequency, the next step was to prototype the proposed Energy Harvester at a 900MHz signal. Due to numerous constraints, including the need to use Surface Mount Device (SMD) components unsuitable for breadboard use due to their size, prototyping on a breadboard was deemed unviable. Thus, the selected alternative was to implement the design on a printed circuit board (PCB).

The 900MHz input signal was introduced using a Vector Network Analyzer (VNA). For this purpose, we incorporated an SMA connector in the design to facilitate VNA connectivity to the PCB prototype. To measure the output voltage, header pins were added. An additional SMD LED was also installed to visualize the output voltage. Figure 2. 9 depicts the completed 900MHz PCB prototype.

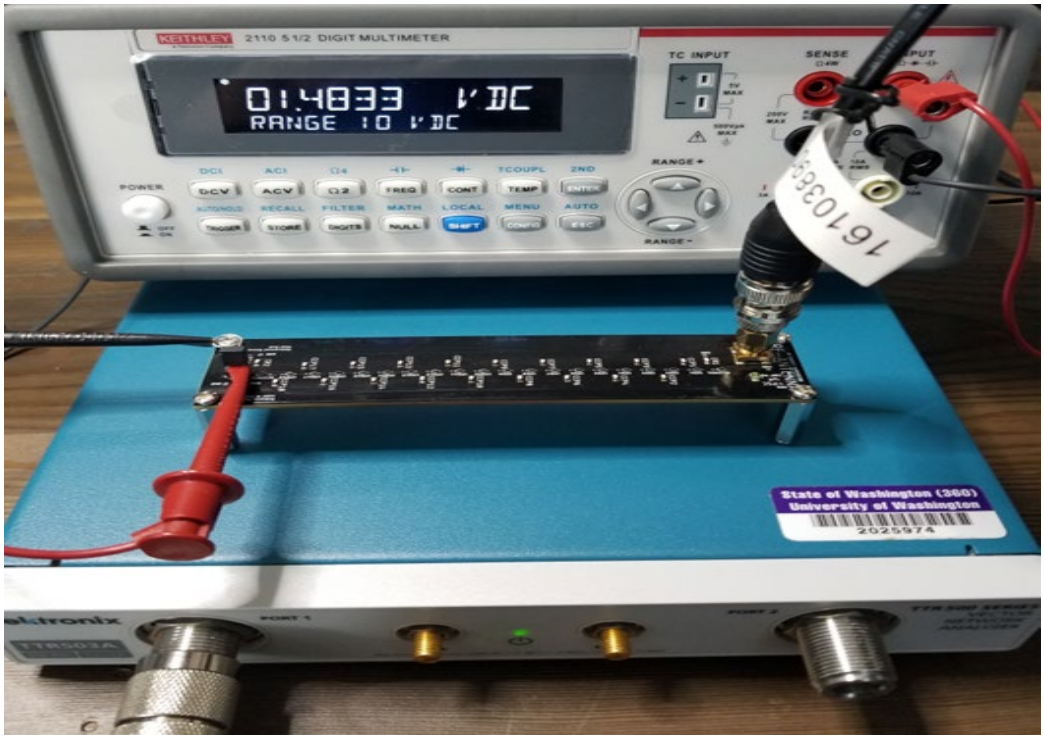


Figure 2. 9 900MHz Prototype

As demonstrated in Figure 2.9, the system effectively converted 330µW of 900MHz RF input into 1.48V DC with an efficiency of 6.7%, powering the LED, which consumed about 22µW. This performance is equivalent to wirelessly lighting up the same LED with a power of 1mW and utilizing transmit/receive antennas, each with a 5dBi gain, spanning a distance of half a meter.

Despite the prototype's success, it was observed that the maximum conversion efficiency was not achieved due to several factors. These include inherent resistance, the dielectric constant of the PCB material, and power reflection due to impedance mismatch between the VNA and the PCB prototype. These factors were not considered in the initial Cadence simulations.

Nonetheless, an output voltage that successfully powered an LED consuming 22 µW was recorded. This result confirmed the feasibility of the Radio Frequency Energy Harvesting system concept.

### 2.3.3 *Wireless testing of the PCB*

Upon completing the 900MHz circuit tests, an impedance-matching network was established utilizing the Vector Network Analyzer (VNA). The calculation of the impedance matching network was made possible by determining the reflection and power coefficients using a Smith chart.

Optimization of the impedance matching to 50Ω was achieved by employing both series and shunt capacitors with values of 0.3pF and 0.9pF, respectively. A 20kΩ pulldown resistor was also incorporated to provide a direct current (DC) path. The block diagram illustrating the wireless testing setup is shown in Figure 2. 10.

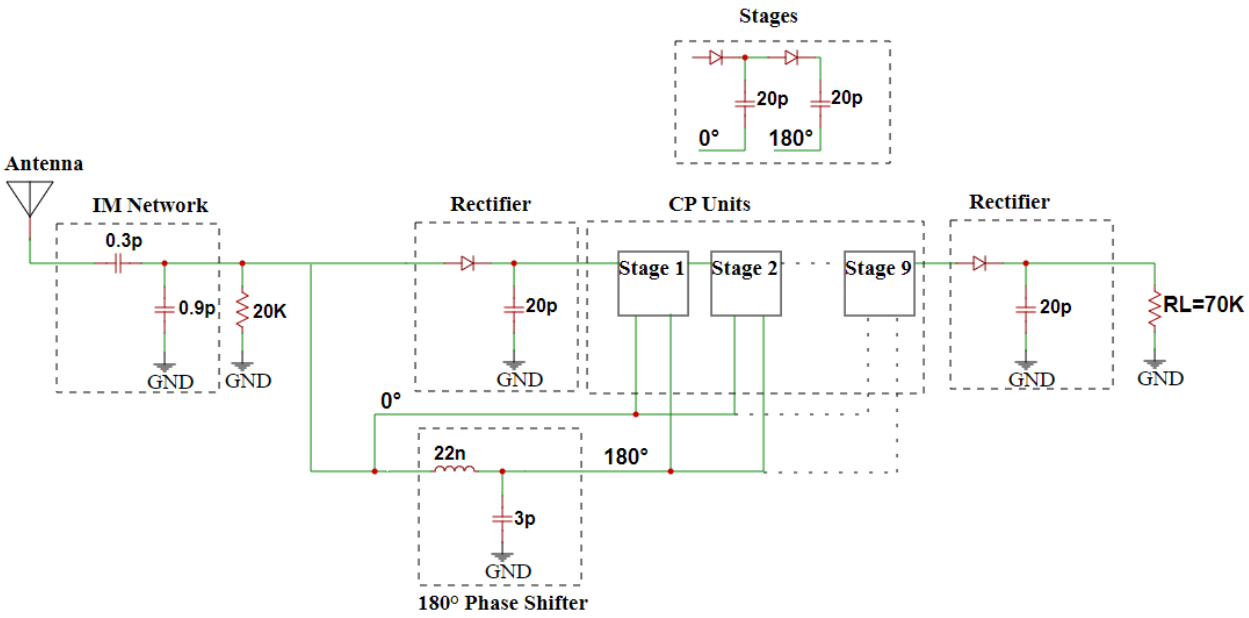


Figure 2. 10 900MHz RF-EH with IM Network

The RF Energy Harvester with the impedance matching board demonstrated superior performance during the wireless testing, as depicted in Figure 2. 11.

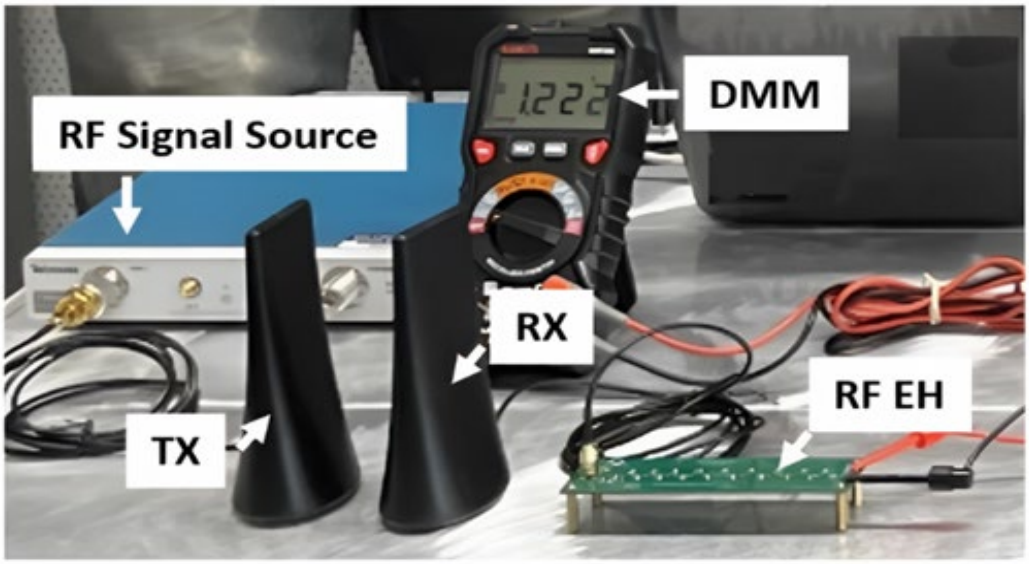


Figure 2. 11 Wireless Demonstration of 900MHz RF-EH with IM Network

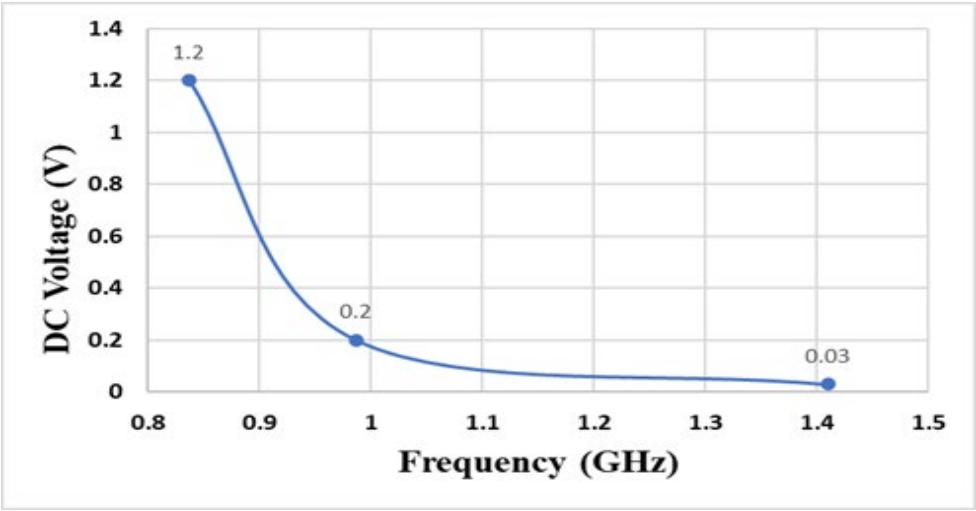


Figure 2. 12 900MHz wireless testing DC output voltage versus frequency

Figure 2. 11 showcases the test setup of the RF Energy Harvester wireless demonstration equipped with an impedance matching board. The transmitting antenna, depicted as the small black tower, is connected to an RF signal source (the blue box). The receiving antenna (also represented

as a small black tower) is connected to the RF-EH on the PCB (green PCB with stand) for wireless testing. The DC voltage generated can be observed on the Digital Multimeter (DMM) connected across the 70kΩ load resistor on the PCB.

Figure 2. 12 presents the measured DC output voltage results at various RF signal frequencies. Due to the input reflection characteristics of the transmitting and receiving antennas, the maximum DC voltage is generated at around 850MHz. The distance maintained between transmitting and receiving antennas during this testing phase was approximately 5 cm.

These wireless demonstration results validate the effectiveness of the impedance-matching network in the RF Energy Harvester, especially in a real-world testing scenario. This approach highlights the viability and the promising future of RF Energy Harvesting systems.

# Chapter 3. DESIGN AND SIMULATION OF THE RF ENERGY HARVESTER IC

The RF energy harvester (RF-EH) system undergoes a comprehensive optimization process to maximize its performance and power transfer efficiency. This optimization encompasses various aspects, including the diode size, the number of stages in the charge pump, the 180-degree phase shifter, and impedance matching.

The diode size is carefully optimized to achieve the highest energy conversion efficiency. The RF-EH system can effectively handle the desired power levels and minimize losses during energy conversion by selecting an appropriate diode size.

The number of stages in the charge pump also plays a crucial role in optimizing the RF-EH system. The optimal number of stages is determined through simulation and analysis to ensure efficient power extraction and voltage boosting from the RF signal. This optimization process aims to find the balance between power efficiency and circuit complexity.

Furthermore, the design and optimization of the 180-degree phase shifter are vital for achieving accurate phase shifting and synchronization within the RF-EH system. The desired 180-degree phase shift at the designated frequency is attained by fine-tuning the phase shifter circuit parameters, enabling optimal energy harvesting from the RF signals.

Impedance matching is another critical aspect of RF-EH system optimization. By optimizing the impedance matching network, maximum power transfer between the antenna and the energy harvesting circuit is achieved, enhancing overall system efficiency.

The optimization process involves iterative design adjustments, simulations, and performance evaluations. Figures and simulation results will be provided to showcase the effectiveness of the optimization techniques employed in the RF-EH system. These visual

representations will help demonstrate the improvements achieved through the optimization process, validating enhanced performance, power transfer efficiency, and overall effectiveness of the RF-EH system.

The optimization of the RF-EH system, covering diode size, number of stages in the charge pump, 180-degree phase shifter, and impedance matching, results in a highly efficient and effective energy harvesting solution. The achieved optimization ensures maximum power transfer, accurate phase shifting, and improved overall performance of the RF-EH system.

## 3.1 Overview of the Design Process

The design process of the proposed novel RF energy harvester operating at 2.4GHz is presented in this section. The schematic design of the RF energy harvester is similar to the 900MHz design, with essential modifications to the 180° phase shifter, number of CP stages, and other components to accommodate the higher operating frequency.

The block diagram of the proposed RF energy harvester is shown in Figure 3. 1 The charge pump (CP) remains based on the original concept of the Dickson CP, but with the input clock signals replaced by out-of-phase RF signals. The incoming RF signal is split between the RF-DC rectifier and 180° phase shifter inputs. The rectified DC voltage level acts as the reference voltage for the CP, and the out-of-phase RF signals across the CP stages continually increase the DC voltage level to reach the desired DC voltage across the load. The amount of DC power the load can consume depends on the available RF input power and the overall conversion efficiency of the RF energy harvester.

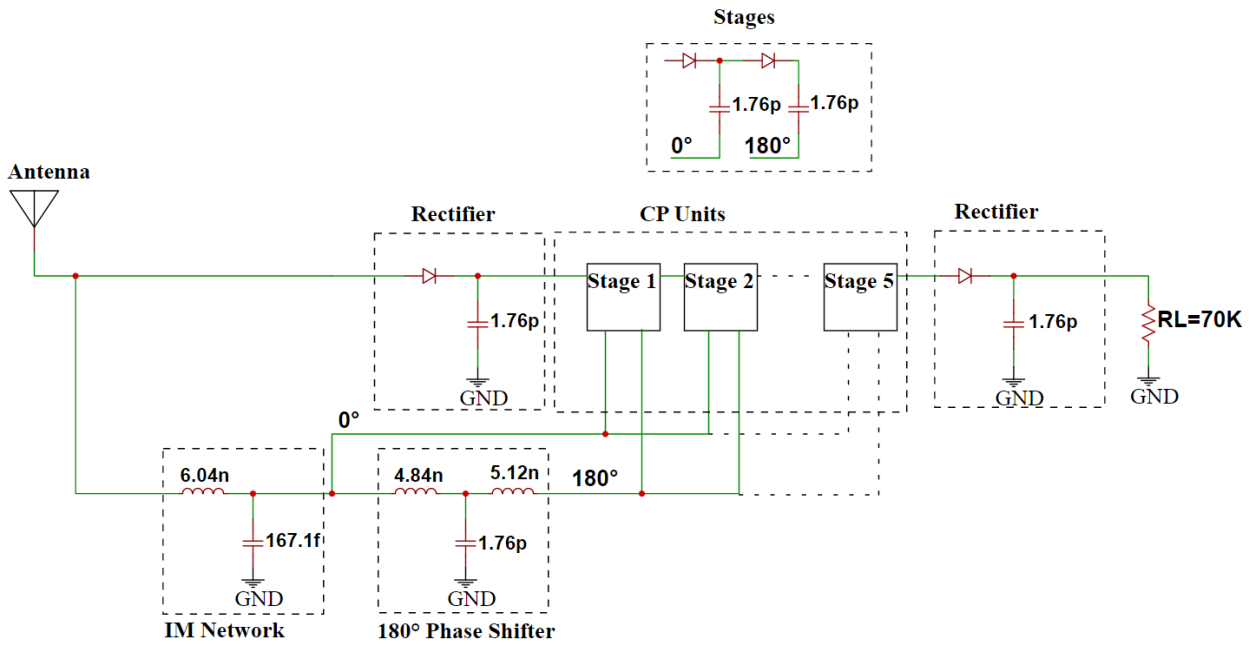


Figure 3. 1 RF Energy Harvester Block Diagram

## 3.2 Design Specifications and Requirements

The proposed RF energy harvester is designed for the 2.4GHz frequency range, a common frequency for Wi-Fi and Bluetooth communications. The design requirements for the energy harvester are defined by the intended applications, which include powering low-power electronic devices in wireless sensor networks and IoT applications.

The critical design specifications for the RF energy harvester include high energy conversion efficiency, compact size, and compatibility with CMOS fabrication processes. The harvester should be able to efficiently convert ambient RF signals into usable DC power despite the typically low power density of ambient RF signals.

The harvester should also provide sufficient power for small-scale electronic devices, typically in the range of microwatts to milliwatts. It should operate continuously without needing external power sources or batteries.

To calculate the received power ($P_r$) in watts, we can use the Friis transmission equation. This equation is usually written in dB form, but it can be rewritten in linear form as follows:

$$P_r = P_t * \frac{(G_t * G_r * \lambda^2)}{(4\pi d)^2} \qquad (3.\ 1)$$

Where:

$P_t$ is the transmitted power (in watts)

$G_t$ is the gain of the transmitting antenna

$G_r$ is the gain of the receiving antenna

λ is the wavelength (in meters)

d is the distance between the antennas (in meters)

For a frequency of 2.4 GHz, the wavelength λ can be calculated as the speed of light (c) divided by the frequency (f), so

$$\lambda = \frac{c}{f} \qquad (3.\ 2)$$

$$\lambda = \frac{c}{f} = \frac{\frac{3*10^8 m}{s}}{2.4*10^9\ Hz} = 0.125\ m$$

Given that:

$P_t$ = 4 W (the maximum allowed EIRP in the US)

$G_t$ = 1 (we will assume a simple isotropic radiator, which has a gain of 1)

$G_r = 10^{\frac{6}{10}} = 3.98$ (converting from dBi to linear gain)

λ = 0.125 m

d = 1 m

We can substitute these values into the equation to get:

$$P_r = 4\,W * \frac{(1 * 3.98 * 0.125^2 m^2)}{(4\pi * 1m)^2} \approx 1.58 * 10^{-3} W$$

So, at a distance of 1 meter from a 4 W transmitter, a standard receiving antenna with a gain of 6 dBi would receive approximately 1.58 milliwatts of power at a frequency of 2.4 GHz. This received power value is slightly higher than 0 dBm, which is 1mW, showing that an input power of 0 dBm at the receiving antenna is a reasonable value to work with.

## 3.1 Simulation and Optimization of the Design

The RF energy harvester (RF-EH) system undergoes a comprehensive optimization process to maximize its performance and power transfer efficiency. This optimization encompasses various aspects, including the diode size, the number of stages in the charge pump, the 180-degree phase shifter, and impedance matching.

The diode size is carefully optimized to achieve the highest energy conversion efficiency. The RF-EH system can effectively handle the desired power levels and minimize losses during energy conversion by selecting an appropriate diode size.

The number of stages in the charge pump also plays a crucial role in optimizing the RF-EH system. The optimal number of stages is determined through simulation and analysis to ensure efficient power extraction and voltage boosting from the RF signal. This optimization process aims to find the balance between power efficiency and circuit complexity.

Furthermore, the design and optimization of the 180-degree phase shifter are vital for achieving accurate phase shifting and synchronization within the RF-EH system. The desired 180-degree phase shift at the designated frequency is attained by fine-tuning the phase shifter circuit parameters, enabling optimal energy harvesting from the RF signals.

Impedance matching is another critical aspect of RF-EH system optimization. By optimizing the impedance matching network, maximum power transfer between the antenna and the energy harvesting circuit is achieved, enhancing overall system efficiency.

The optimization process involves iterative design adjustments, simulations, and performance evaluations. Figures and simulation results will be provided to showcase the effectiveness of the optimization techniques employed in the RF-EH system. These visual representations will help demonstrate the improvements achieved through the optimization process, validating the enhanced performance, power transfer efficiency, and overall effectiveness of the RF-EH system.

The optimization of the RF-EH system, covering diode size, number of stages in the charge pump, 180-degree phase shifter, and impedance matching, results in a highly efficient and effective energy harvesting solution. The achieved optimization ensures maximum power transfer, accurate phase shifting, and improved overall performance of the RF-EH system.

## 3.2 Design of the rectifier circuit

The rectifier circuit is a fundamental component of the RF energy harvester, responsible for converting the RF signals captured by the antenna into DC power. In this design, the rectifier circuit comprises a single transistor diode and a shunt capacitor, which acts as a peak detector.

The RF energy harvester (RF-EH) rectifier utilizes Schottky Barrier Diode (SBD) instead of NMOS or regular diodes, providing several advantages for efficient energy conversion.

SBD diodes are chosen explicitly for rectification due to their unique characteristics. Unlike regular diodes, SBD diodes have a lower forward voltage drop, which reduces power losses during energy conversion. This lower voltage drop translates into improved overall efficiency, allowing for higher power extraction from the RF signal.

Furthermore, SBD diodes offer faster switching speeds than NMOS and regular diodes. This attribute is particularly beneficial in high-frequency applications, such as RF energy harvesting in the GHz range. The fast-switching speed of SBD diodes ensures swift and accurate energy transfer from the RF signal to the energy harvesting circuit, maximizing the efficiency of the rectification process.

Another advantage of SBD diodes is their lower leakage current. This characteristic contributes to reduced power losses and improved efficiency during energy conversion. By minimizing leakage current, the rectifier can achieve a higher energy conversion ratio and generate a more substantial power output, enhancing the overall performance of the RF-EH system.

Lastly, SBD diodes demonstrate better temperature stability than NMOS and regular diodes. This stability ensures consistent and reliable performance of the rectifier across a wide range of operating temperatures, making it suitable for various environmental conditions.

By incorporating SBD diodes into the rectifier design of the RF-EH system, the energy conversion process becomes more efficient, leading to higher power extraction from the RF signal. The use of SBD diodes helps to minimize power losses, improve switching speed, reduce leakage current, and enhance temperature stability. These advantages collectively contribute to the overall effectiveness and reliability of the RF-EH system, providing a viable solution for harvesting RF energy in wireless sensor networks and IoT applications.

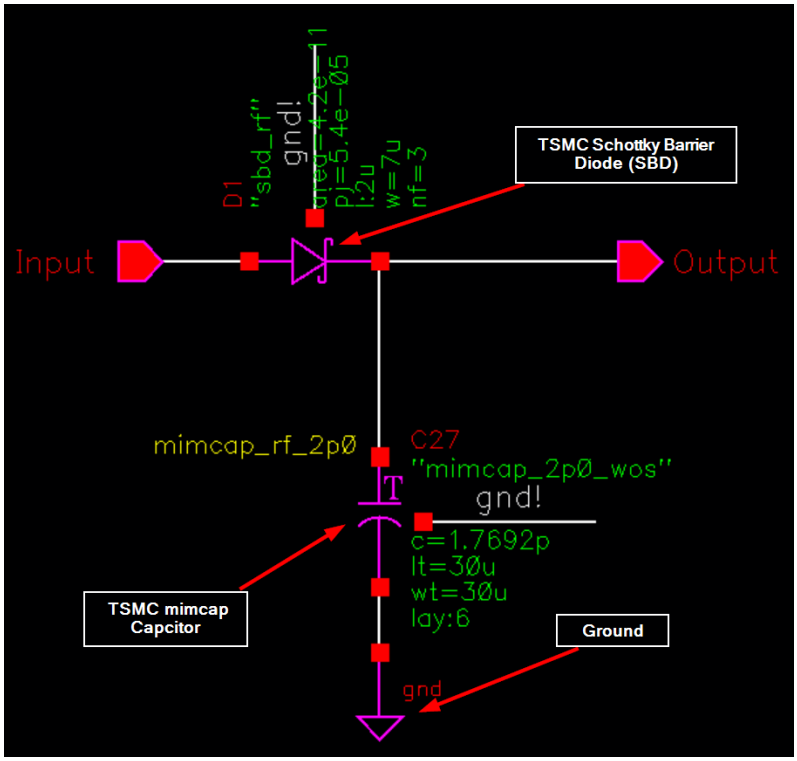


Figure 3. 2 First Rectifier used before CPs at the source

The design parameters for the rectifier circuit Figure 3. 2, such as the capacitance of the shunt capacitor, are optimized based on the target operating frequency of 2.4GHz to ensure maximum rectification efficiency.

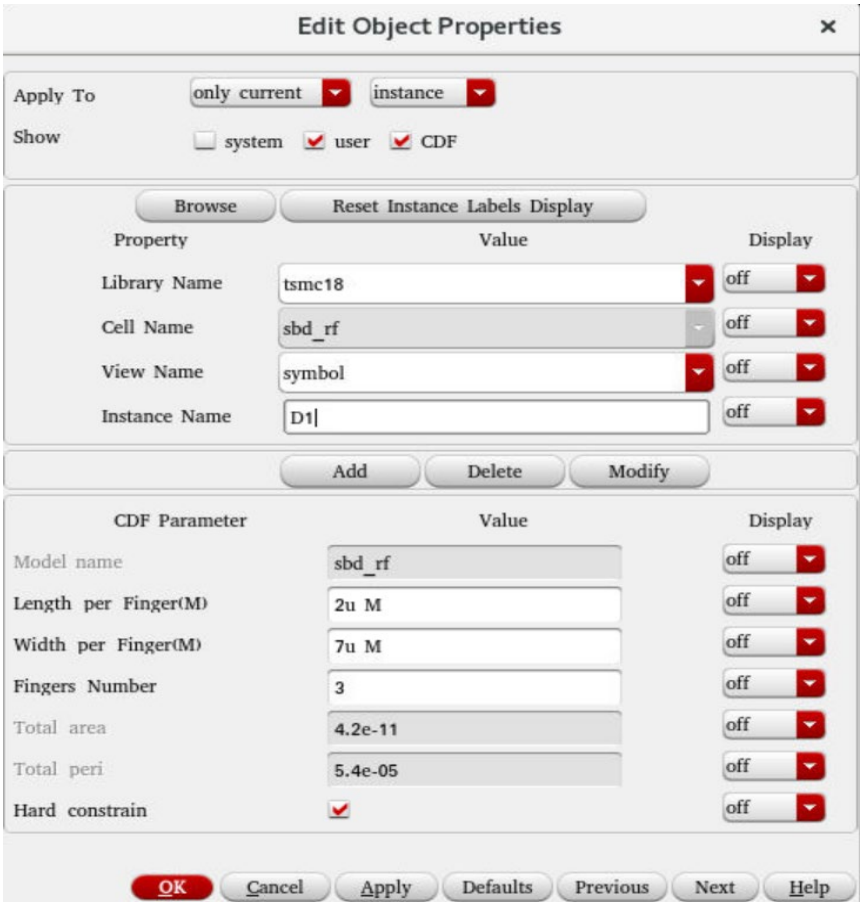


Figure 3. 3 First Rectifier Diode Specification

Figure 3. 3 presents the diode specifications used in the first source rectifier. The diode's size and number of fingers are carefully selected through circuit optimization to achieve improved performance and desired results.

The appropriate diode size and the number of fingers are determined by optimizing the circuit to ensure optimal rectification efficiency. This optimization process involves considering diode characteristics, power requirements, and design constraints. The size of the diode influences its current handling capacity, while the number of fingers affects the overall effective area for current conduction.

Through the optimization process, the diode's dimensions and finger configuration are adjusted to maximize the rectification efficiency, minimize power losses, and enhance the overall performance of the rectifier circuit. By selecting the optimal diode size and number of fingers, the rectifier can effectively convert the alternating current (AC) input into direct current (DC) output with improved efficiency and performance.

By carefully considering the specifications of the diode and employing circuit optimization techniques, the first source rectifier can achieve enhanced results, ensuring efficient energy conversion in the RF energy harvester system.

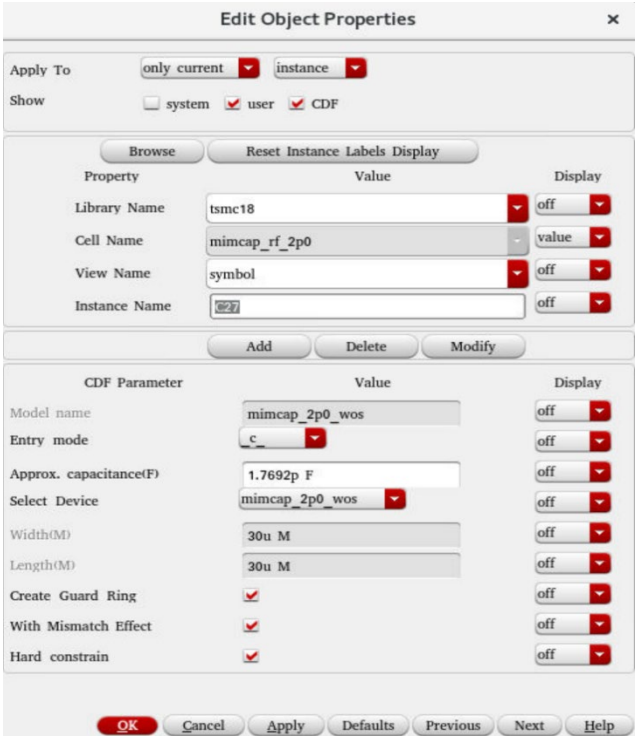


Figure 3. 4MIMCAP Specifications

For the design, MIMCAP (Metal-Insulator-Metal Capacitor) has been selected. MIMCAP capacitors offer several advantages that align with the requirements of the design. They are

compatible with CMOS technology, enabling seamless integration into the RF energy harvester IC. MIMCAP capacitors also provide high capacitance density, allowing compact circuit design and efficient space utilization. Additionally, MIMCAP capacitors exhibit low leakage current, enhancing overall efficiency and minimizing power losses during energy conversion. By utilizing MIMCAP capacitors, the design can benefit from their compatibility, high capacitance density, and low leakage current, facilitating efficient and reliable energy harvesting in RF-based systems.

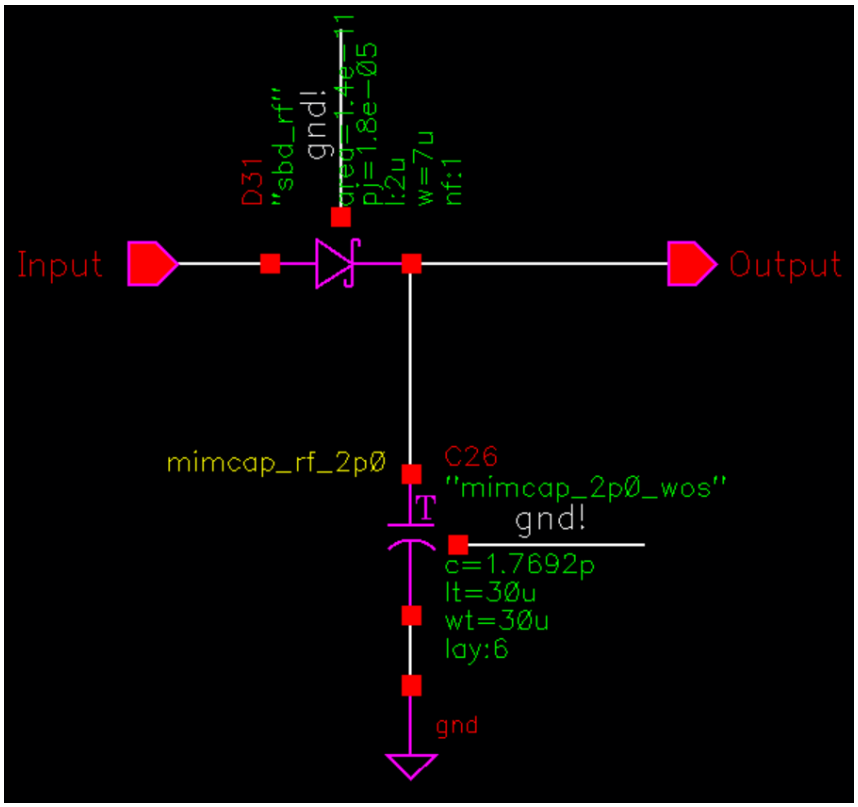


Figure 3. 5 Second Rectifier used before the load

The circuit's second rectifier, Figure 3. 5, serves the purpose of smoothing the DC output at the load. It is crucial in converting the pulsating DC signal from the first rectifier into a more stable and consistent DC voltage.

To achieve this, the second rectifier follows the exact specifications as the first rectifier, with the exception of the number of fingers, which is set to 1. By reducing the number of fingers to 1, the second rectifier effectively modifies the current conduction characteristics, allowing for a smoother output waveform.

The rectifier specifications, including the size, layout, and other parameters, are carefully determined through optimization. The optimization process considers factors such as power requirements, voltage levels, and design constraints to achieve the desired performance and efficiency.

By employing a second rectifier with optimized specifications, the circuit ensures that the DC output at the load remains stable and free from fluctuations or ripples. This helps maintain a consistent power supply to the load, enabling reliable operation of the downstream components and facilitating the intended functionality of the RF energy harvester system.

## 3.3 Design of the 180° Phase Shifter

The ideal 180° phase shifter circuit Figure 3. 6 is designed and simulated using the Cadence Spectre and circuit simulator. The RF signal frequency chosen for this design is 2.4GHz, a common frequency band used in Wi-Fi and Bluetooth communication systems. The design parameters are L1, C1 for the 180° phase shifter,

$$\omega^2 L_1 C_1 = 2.0 \qquad (3.\ 3)$$

Equation (1) is used for conventional 180° phase shifters.

$C1 = 1.76p\ F \quad f = 2.4GHz \qquad \omega = 2 * \pi * f$

$(2 * \pi * 2.4 * 10^9)^2 * L_1 * 1.76 * 10^{12} = 2 \qquad L_1 = 4.79 * 10^9\ H \quad L_1 = 4.79n\ H$

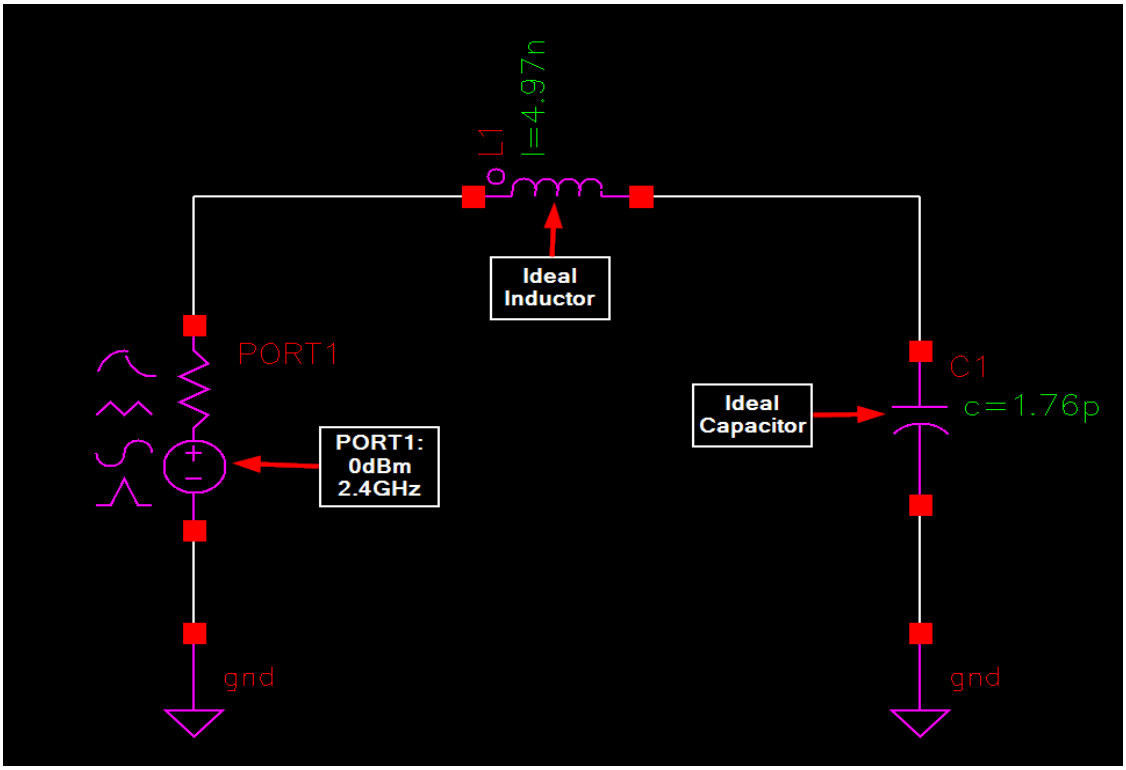


Figure 3. 6 Ideal 180-Degree Phase Shifter Circuit Schematic

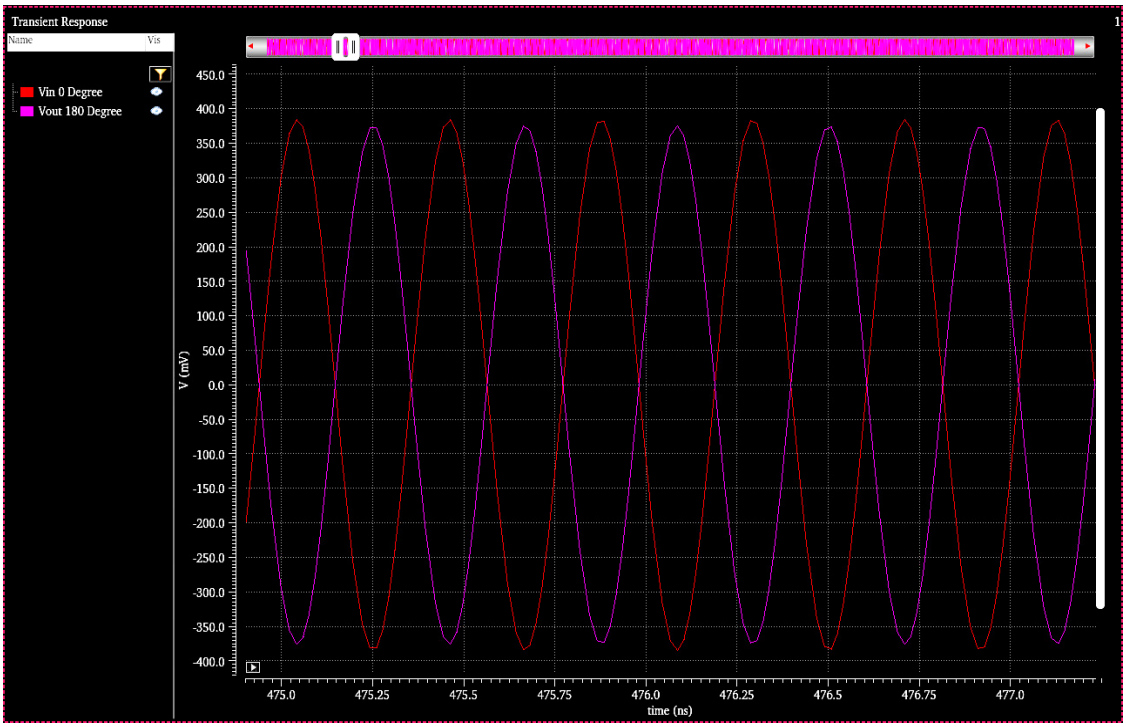


Figure 3. 7 Input and Output of 180-Degree Phase Shifter

When designing a 180-degree phase shifter circuit, it is commonly achieved by utilizing specific circuit configurations and equations. Based on the chosen components, these equations can accurately predict the phase shift in ideal conditions. Equation 1, for instance, might have been used in your simulation to determine the expected phase shift. However, it is essential to note that ideal components assume perfect behavior, disregarding any imperfections or limitations that may occur in real-world scenarios.

In practice, when implementing the designed components and integrating the phase shifter circuit into the rest of the system (Figure 3. 8), issues may arise that prevent the phase shifter from functioning correctly (Figure 3. 9). These issues can occur due to several factors, such as component tolerances, parasitic effects, impedance mismatches, or interference from neighboring components.

Component tolerances refer to variations in the values of the actual components compared to their ideal values, which can affect the overall performance and accuracy of the circuit. Parasitic effects, such as stray capacitance and inductance, can also introduce unpredictable behavior and impact the phase shift.

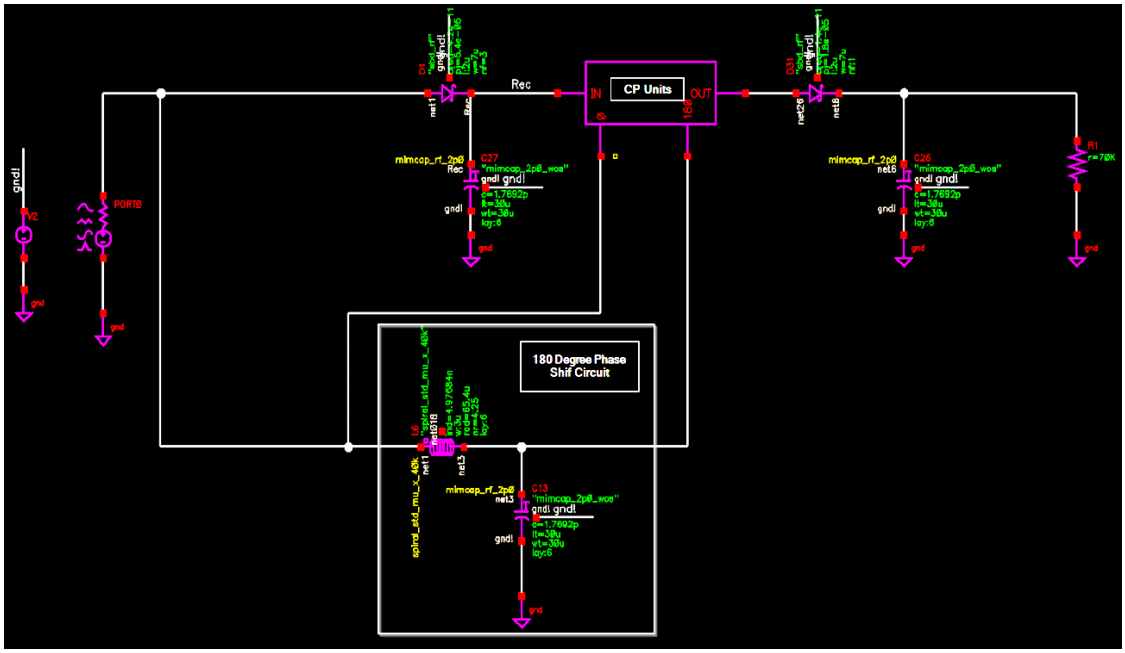


Figure 3. 8 Phase Shifter Circuit in RF-EH Circuit

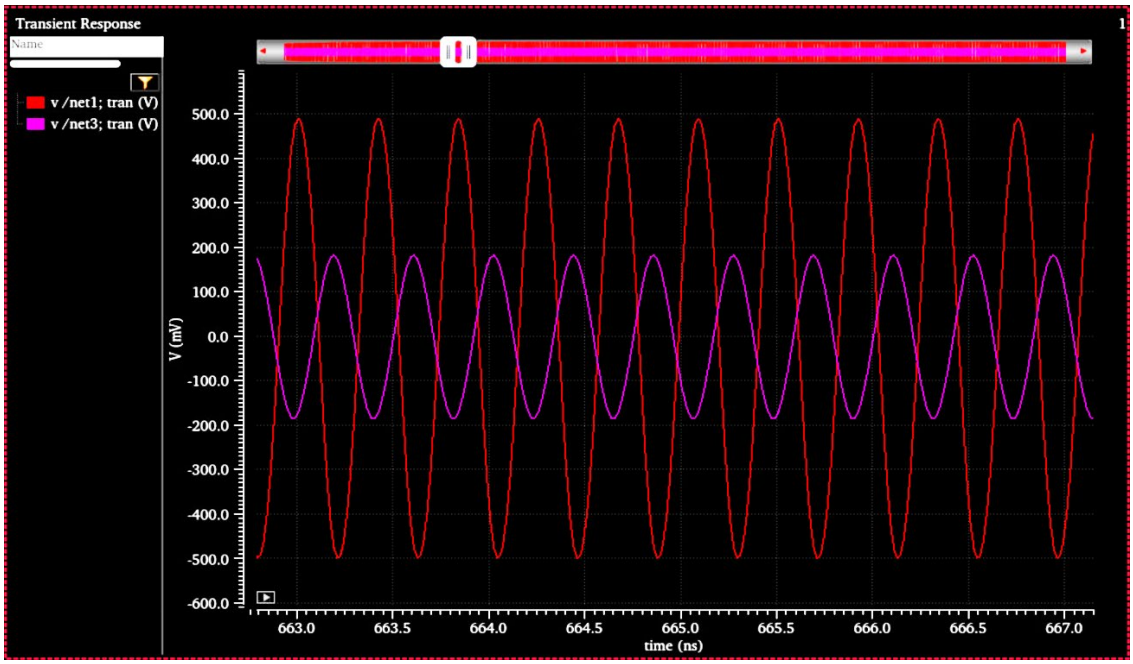


Figure 3. 9 Input and Output of the Phase Shift Circuit

Impedance mismatches can occur when the characteristic impedance of the phase shifter circuit does not match that of the surrounding components or transmission lines, leading to

reflections and distortion of the signal. Interference from neighboring components or signals can also influence the phase shift and degrade the circuit's performance.

A revised design has been implemented to address the mismatch and discrepancies in the 180° phase shifter circuit. The updated phase shifter incorporates one series inductor (L1), another series inductor (L2), and a shunt capacitor (C1). This configuration ensures that two out-of-phase RF signals are generated with equal amplitude but a 180° phase difference at the desired frequency.

The value of inductor L1 has been optimized to approximately 4.84nH, carefully selected to achieve the desired phase shift. Similarly, the second inductor, L2, has undergone optimization and has a value of approximately 5.12nH. These specific inductor values are chosen to achieve the desired phase shift accurately.

The capacitor C1 retains its previous value of 1.76pF as it continues to fulfill the required role in the phase shifter circuit.

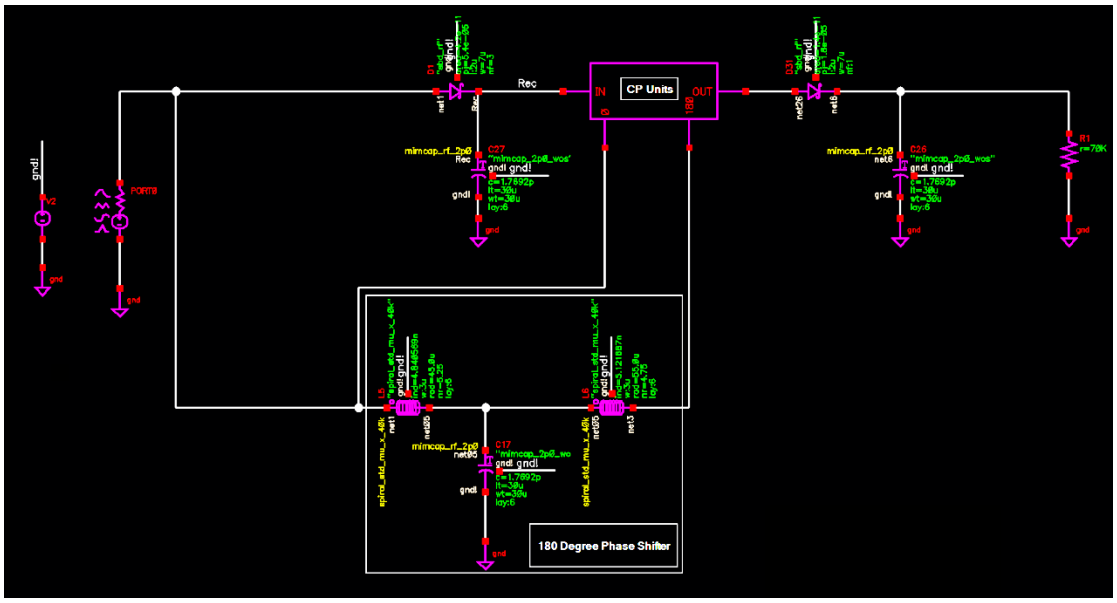


Figure 3. 10 Revised Phase Shifter Design

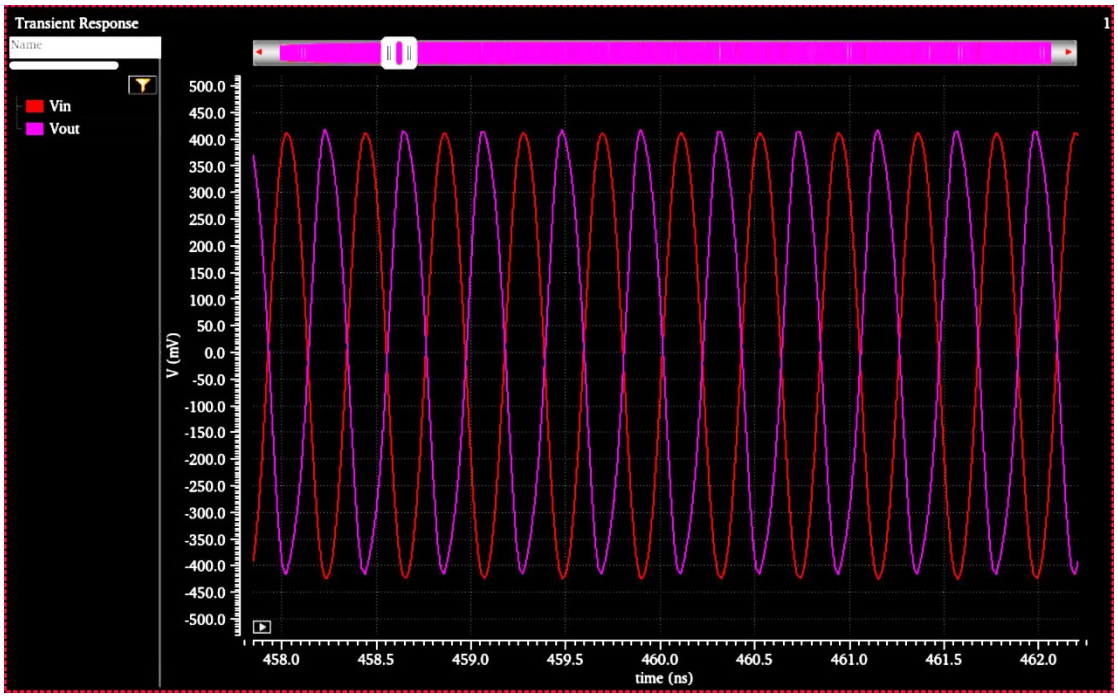


Figure 3. 11 Input and Output of the Revised Phase Shifter

By incorporating these revised component values in Figure 3. 10, the issues of mismatch and discrepancies with the design kit components have been mitigated in the phase shifter

circuit. This update has improved performance, ensuring the desired 180° phase shift at the designated frequency.

Figure 3. 11 depicts the phase shifter's input and output signals, showcasing the 180-degree phase difference between them. The output signal aligns as expected with the desired phase shift, indicating the successful correction of the initial issues. This validation through the input and output signals confirms the functionality and effectiveness of the revised phase shifter design.

## 3.4 Design of the Voltage Multiplier Circuit

The voltage multiplier circuit, also known as the charge pump, is another crucial component of the RF energy harvester. The charge pump increases the DC voltage level produced by the rectifier circuit to meet the power requirements of the target electronic devices.

The proposed charge pump is based on the Dickson charge pump concept. However, instead of conventional clock signals, the charge pump in this design is driven by out-of-phase RF signals generated by the 180° phase shifter. This modification enhances the charge pump's performance at the target operating frequency of 2.4GHz.

The charge pump stages are designed with Schottky Barrier Diode in series and shunt capacitors. The values of these shunt capacitors are optimized to ensure maximum voltage multiplication efficiency at the 2.4GHz frequency. Figure 3. 12 depicts a single stage of the Dickson Charge pump. In Figure 3. 13, The RF-EH circuit design consists of 5 stages of CP units in series.

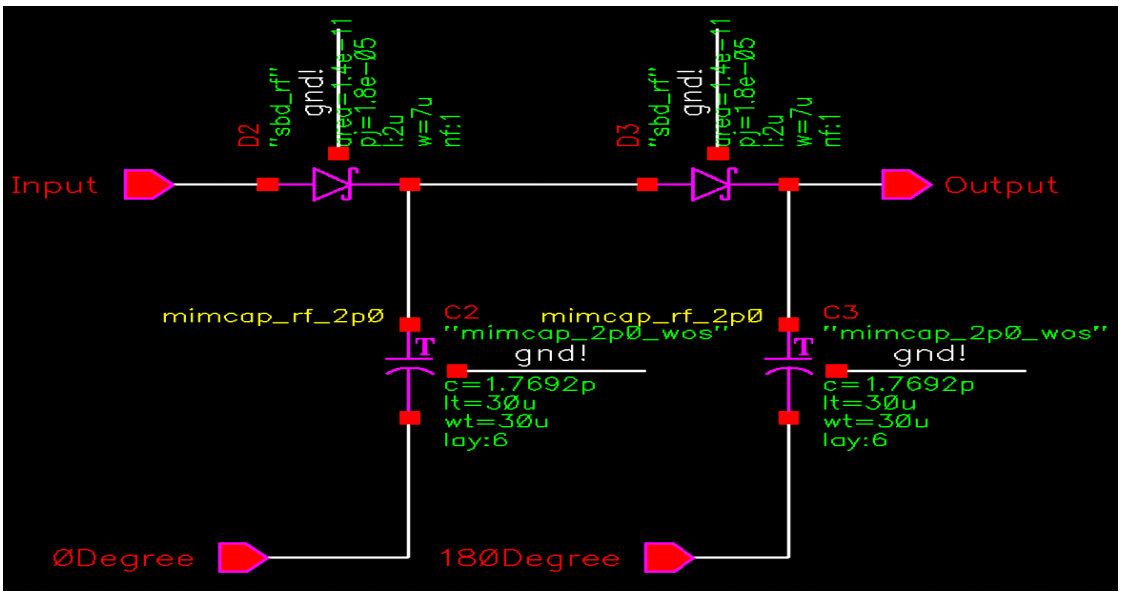


Figure 3. 12 One Unit of Charge Pump (CP)

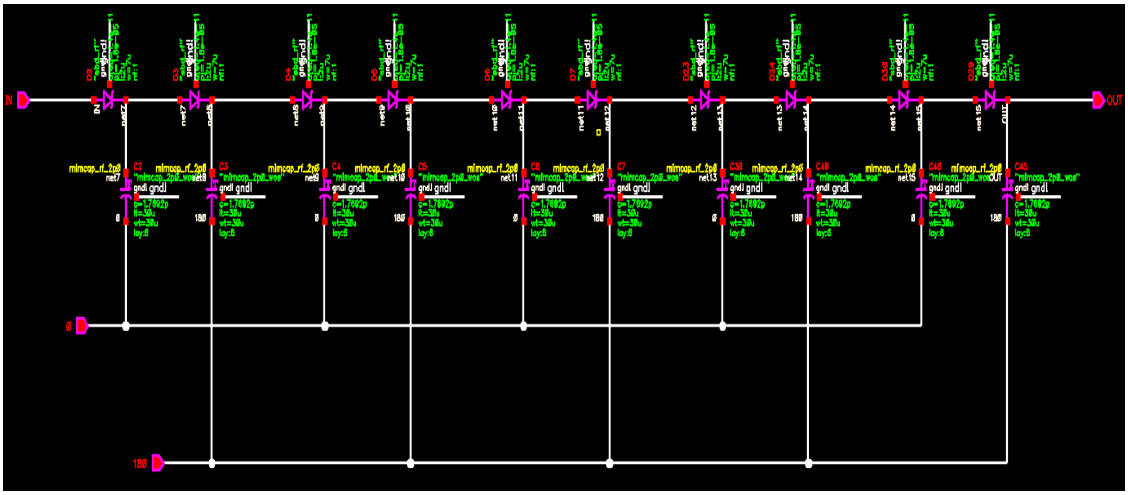

Figure 3. 13 Five Units used in the RF-EH

The number of stages is optimized by testing the circuit with variations in the quantity of Charge Pump (CP) units. This involves adding or removing a CP unit and analyzing the impact on the circuit's efficiency. Table 3. 1 presents the results of adjusting the number of CP units within the design. The input power is 0dBM, and the output power is collocated across a 70K Ω load.

Table 3. 1 2.4GHz CP Units Optimization

| CP(Unit) | $V_{rms}$(V) | $I_{rms}$(A) | $V_{dc}$(V) | $I_{dc}$(A) | $P_{in}$(W) | $P_{out}$(W) | η% |
|---|---|---|---|---|---|---|---|
| 4 | .357 | .184 | 2.59 | 3.75E-05 | 6.54E-04 | 9.71E-05 | 14.84 |
| 5 | .296 | .305 | 3.38 | 4.83E-05 | 9.01E-04 | 1.63E-04 | 18.11 |
| 6 | .264 | .395 | 3.14 | 4.50E-05 | 1.04E-03 | 1.41E-04 | 13.53 |

## 3.5 Input and Output Power Analysis

The input power for our RF energy harvester is supplied at a frequency of 2.4GHz with a magnitude of 0dBm, equivalent to 1mW. A PORT supplies this power to the shared node between the rectifier circuit and the 180-degree phase shifter. The power distribution at this shared node was a challenge in our design, as the node splits the input power into two distinct branches.

To study the power distribution at this node, we employed two PORTs, PORT 1 before the rectifier and PORT 2 before the 180° Phase shifter circuit, and supplied a total power of 0dBm across both ports. We then varied the power for each port by ±10% for our analysis.

From the analysis of Table 3. 2, we found that much of the power needed to be directed toward the 180-degree phase shifter circuit. We introduced a matching network into the branch leading to the phase shifter to optimize this power distribution. This network minimizes power reflection and maximizes power transfer to the phase shifter.

After running S-parameter simulations, we optimized the matching network to act as an impedance-matching network for the entire circuit.

Table 3. 2 2 Port Analysis input power

| PORT1 (dBm) | PORT2 (dBm) | $R_L(\Omega)$ | $V_{dc}$(V) | $I_{dc}$(A) | $P_{in}$(W) | $P_{out}$(W) | η% |
|---|---|---|---|---|---|---|---|
| -10.0 | -0.46 | 70K | 3.03 | 4.34E-05 | 1.00E-03 | 1.32E-04 | 13.15 |
| -7.0 | -0.97 | 70K | 2.79 | 3.98E-05 | 1.00E-03 | 1.11E-04 | 11.10 |
| -5.2 | -1.55 | 70K | 2.5 | 3.58E-05 | 1.00E-03 | 8.95E-05 | 8.95 |
| -4.0 | -2.22 | 70K | 2.2 | 3.16E-05 | 1.00E-03 | 6.94E-05 | 6.94 |
| -3.0 | -3.01 | 70K | 1.88 | 2.69E-05 | 1.00E-03 | 5.06E-05 | 5.05 |
| -2.2 | -3.98 | 70K | 1.51 | 2.17E-05 | 1.00E-03 | 3.27E-05 | 3.27 |
| -1.5 | -5.23 | 70K | 1.12 | 1.61E-05 | 1.00E-03 | 1.80E-05 | 1.80 |
| -1.0 | -6.99 | 70K | 0.744 | 1.01E-05 | 1.00E-03 | 7.48E-06 | 0.74 |

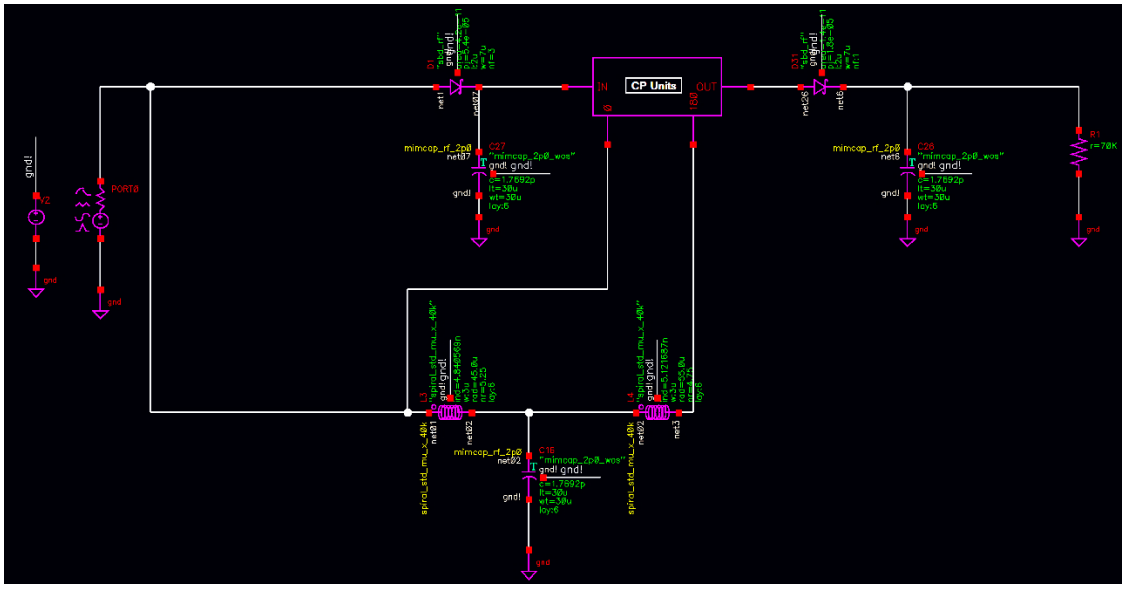


Figure 3. 14 The RF-EH Circuit Without IM Network

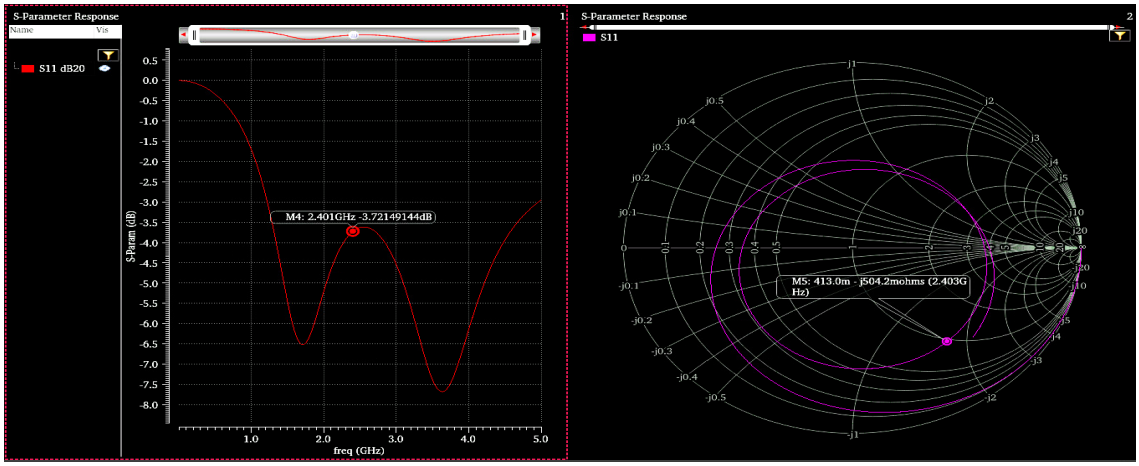


Figure 3. 15 The RF-EH Without IM S-Parameter Analysis

Figure 3. 14 presents the RF energy harvesting (EH) circuit without the impedance matching (IM) network preceding the 180-degree phase shifter. The absence of an IM network in this setup means the circuit is not ideally optimized for maximum power transfer.

Figure 3. 15 provides an S-parameter analysis of the circuit from Figure 3. 14. The analysis reveals that the circuit is not perfectly matched at 2.4 GHz. The power reflection indicates that a considerable amount of power is being reflected rather than effectively transferred to the load.

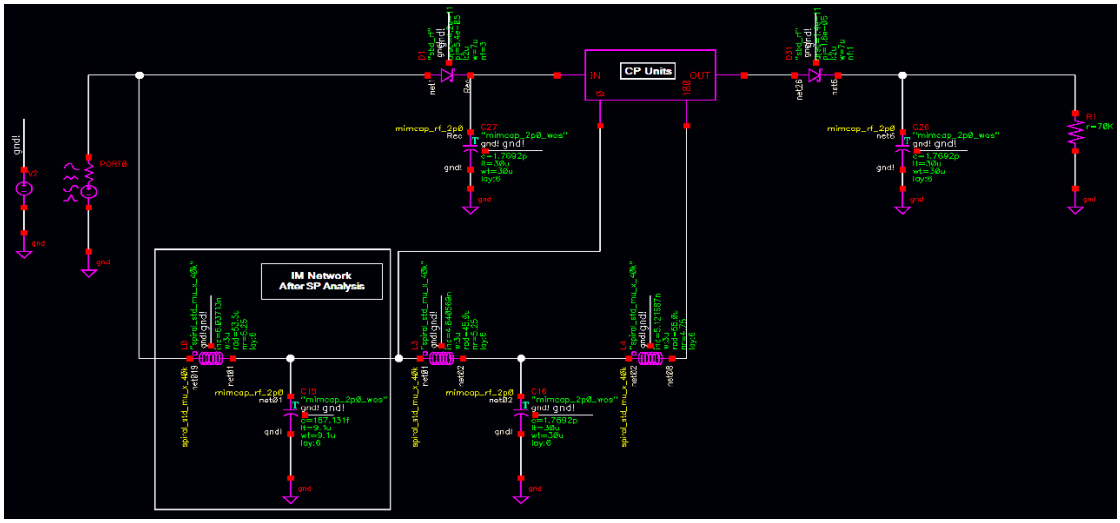


Figure 3. 16 The RF-EH Circuit with IM Network

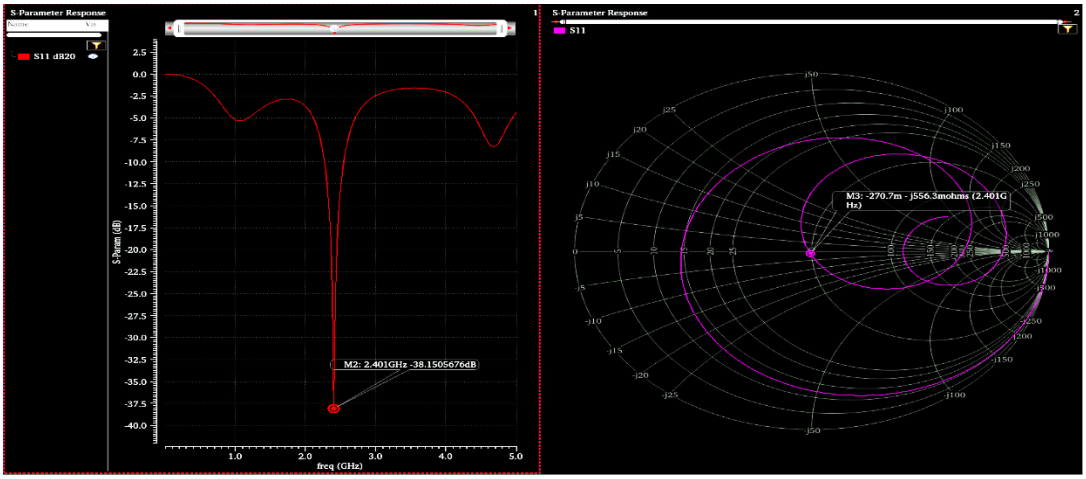


Figure 3. 17 The RF-EH With IM S-Parameter Analysis

Figure 3. 16 showcases the same RF-EH circuit, now featuring an IM network before the 180-degree phase shifter. The IM network integration aims to optimize the circuit for maximum power transfer.

Figure 3. 17, the S-parameter analysis of the revised circuit from Figure 3. 16, shows significant improvements. The circuit is now matched to a 50-ohm input at 2.4 GHz, exhibiting a substantially improve. This dramatic decrease in power reflection ensures maximum power transfer to the load, which ultimately enhances the overall efficiency of the RF energy harvester.

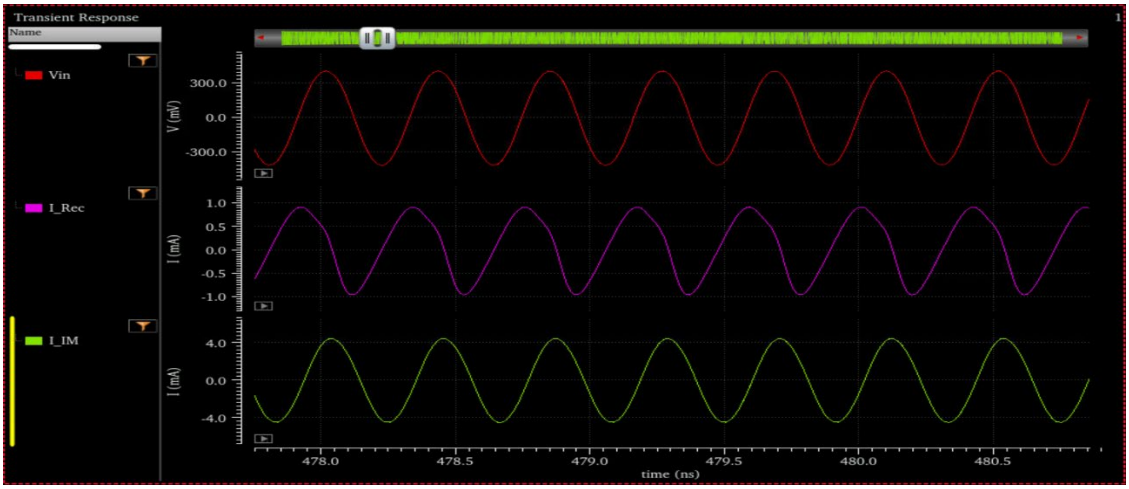


Figure 3. 18 RF-EH Power Input Simulation

Figure 3. 18 illustrates the transient simulation results obtained after incorporating the impedance matching (IM) network before the 180-degree phase shifter. The figure consists of three graphs detailing a specific aspect of the circuit's performance.

The first graph depicts the input voltage ($V_{in}$) at the IM network and the rectifier. The second graph shows the current measurement at the rectifier ($I_{Rec}$), and the third graph displays the current ($I_{IM}$) at the IM network.

To calculate the input power distribution, we use the following equations and RMS value of result from the graph:

Power going to the rectifier ($P_{Rec}$) is calculated by $P_{Rec} = I_{Recrms} * V_{inrms}$ (3. 4)

And power going to the IM network ($P_{IM}$) is given by $P_{IM} = I_{IMrms} * V_{inrms}$ (3. 5)

Given $V_{inrms} = 295.6 * 10^{-3}V$, $I_{Recrms} = 648.5 * 10^{-6}A, I_{IMrms} = 3.079 * 10^{-3}A$, we can now compute the corresponding power values.

$$P_{Rec} = 295.6 * 10^{-3}V * 648.5 * 10^{-6}A = 0.192\,mW$$

$$P_{IM} = 295.6 * 10^{-3}V * 3.079 * 10^{-3}A = 0.91\,mW$$

Now, let's calculate the percentage of power going to the IM network and the rectifier.

The total input power $P_{in}$ is the sum of $P_{IM}$ and $P_{Rec}$.

$P_{in} = P_{IM} + P_{Rec}$ (3. 6)

$0.192mW + .91mW = 1.102mW$

Hence, the percentage of power going to the Rectifier is:

$\left(\frac{P_{Rec}}{P_{in}}\right) * 100$ (3. 7)

$\left(\frac{0.192\ mW}{1.102mW}\right) * 100 = 17.42\%$

Similarly, the percentage of power going to the IM network is:

$\left(\frac{P_{IM}}{P_{in}}\right) * 100$ (3. 8)

$$= \left(\frac{0.91\,mW}{1.102mW}\right) * 100 = 82.58\%$$

These results suggest that most input power is directed toward the rectifier.

The input power at the port is calculated using the equation:

$$P_{in} = V_{rms} * I_{rms} \qquad (3.9)$$

The DC output power is calculated using the equation:

$$P_{out} = V_{dc} * I_{dc} \qquad (3.10)$$

And the efficiency of the circuit is calculated using the equation:

$$\eta\% = \left(\frac{P_{out}}{P_{in}}\right) * 100\% \qquad (3.11)$$

Our RF energy harvester was designed for an input power of 0dBm and Load resistance: of 70kΩ. At this power level and the frequency of 2.4GHz, the parameters of our circuit are as follows:

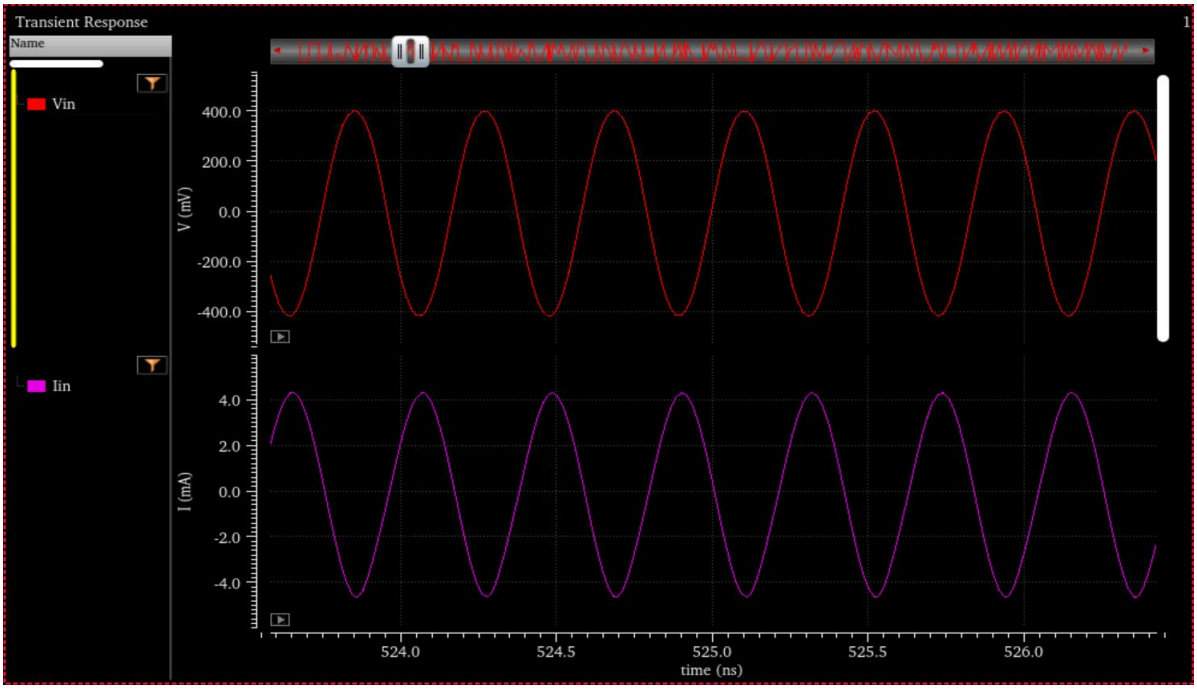


Figure 3. 19 Input Transient Analysis of RF-EH

From Figure 3. 19 calculated the $V_{rms}$ and $I_{rms}$ of the input source to calculate the efficiency.

$V_{rms} = 2.96 * 10^{-1} V$

$I_{rms} = 3.05 * 10^{-3} A$

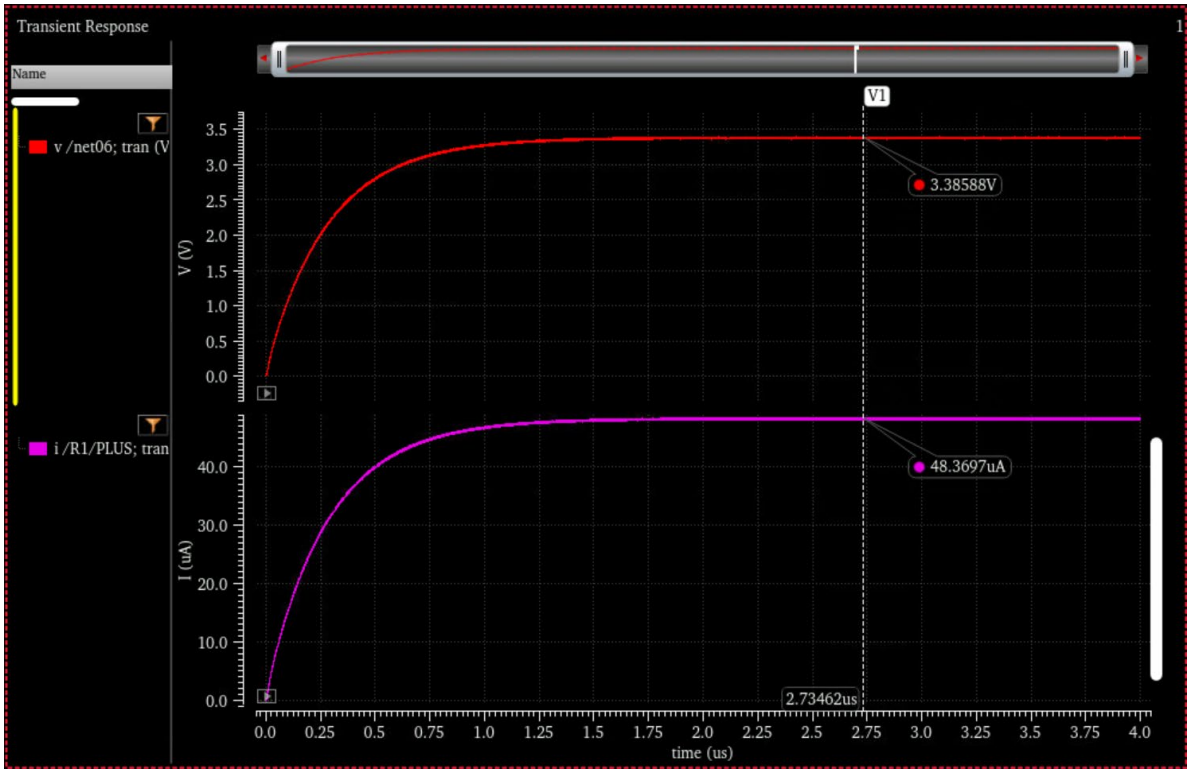


Figure 3. 20 DC Output Transient Analysis of RF-EH

From Figure 3. 20 we can visually determine the DC voltage and current of the RF-EH.

$V_{dc} = 3.38V$

$I_{dc} = 4.83 * 10^{-5} A$

Substituting these values into the above equations, we find:

$$P_{in} = 9.01 * 10^{-4} W P_{out} = 1.63 * 10^{-4} W$$

$\eta\% = 18.11\%$

The selection of an appropriate load for an RF Energy Harvester is a crucial design step, and it is an integral part of the system's optimization. Essentially, the load value directly impacts the performance of the system, particularly the energy conversion efficiency. This can be observed in the experiments documented in Table 3. 3, where the system's efficiency is calculated using different loads, ranging from 5K to 1M ohm.

While considering these different loads, it was found that the optimal efficiency was achieved at a load of 70K ohms for an input power of 0 dBm. This implies that our RF Energy Harvester circuit is most effective when the load is set to 70K ohms under these input conditions.

There are several reasons why the 70K ohm load was the most efficient. One key reason relates to the concept of impedance matching. In RF circuits, energy transfer is most efficient when the load impedance matches the source impedance. In this case, the 70K ohm load provided the best impedance match for the 0 dBm input power, maximizing energy transfer and, thus, efficiency.

Moreover, the selected load affects the operational region of the rectifier diode in the harvester. The 70K ohm load ensures that the diode operates in a region where it most effectively rectifies the incoming RF signal. Hence, load selection is a critical aspect of designing an efficient RF Energy Harvester, and it must be chosen carefully to match the expected input power and other system parameters.

Table 3. 3 DC Load Analysis

| Frequency (Hz) | PORT (dBm) | $R_L$(Ω) | $V_{rms}$(V) | $I_{rms}$(A) | $V_{dc}$(V) | $I_{dc}$(A) | $P_{in}$(W) | $P_{out}$(W) | η% |
|---|---|---|---|---|---|---|---|---|---|
| 2.4G | 0 | 5K | 2.97E-01 | 3.32E-03 | 4.48E-01 | 8.96E-05 | 9.85E-04 | 1.63E-04 | 16.57 |
| 2.4G | 0 | 10K | 2.94E-01 | 3.30E-03 | 8.40E-01 | 8.40E-05 | 9.70E-04 | 4.01E-05 | 4.14 |
| 2.4G | 0 | 20K | 2.92E-01 | 3.25E-03 | 1.48E+00 | 7.47E-05 | 9.49E-04 | 1.11E-04 | 11.65 |
| 2.4G | 0 | 70K | 2.96E-01 | 3.05E-03 | 3.38E+00 | 4.83E-05 | 9.01E-04 | 1.63E-04 | 18.11 |
| 2.4G | 0 | 100K | 3.00E-01 | 2.97E-03 | 3.97E+00 | 3.98E-05 | 8.89E-04 | 1.58E-04 | 17.77 |
| 2.4G | 0 | 500K | 3.21E-01 | 2.66E-03 | 6.07E+00 | 1.22E-05 | 8.53E-04 | 7.41E-05 | 8.68 |
| 2.4G | 0 | 1M | 3.27E-01 | 2.58E-03 | 6.60E+00 | 6.50E-06 | 8.43E-04 | 4.29E-05 | 5.09 |

The efficiency of RF Energy Harvesters is known to fluctuate with varying input power levels, primarily attributed to three significant factors: impedance matching, rectification non-linearity, and component losses.

Impedance matching involves the design of a network within the RF Energy Harvester to optimize power transfer from the source to the load at a particular input power level. When the system operates at this "matched" input power, it achieves maximum efficiency. However, deviations from this input power level may result in a sub-optimal impedance match, thereby causing a decrease in efficiency.

Furthermore, the efficiency variation can also be ascribed to the non-linearity of rectification. RF Energy Harvesters commonly utilize a rectifier circuit to convert the incoming RF energy into DC power. The rectifier's non-linear characteristics imply that its efficiency varies with the input power. Lower input power levels utilize a smaller portion of the rectifier's

curve, typically yielding lower efficiency. As the input power escalates, the curve's usage extends, often leading to improved efficiency. However, excessively high input power levels might drive the rectifier into a region characterized by reduced efficiency.

Component losses also contribute to the efficiency variation. These losses, exhibited by the components used in the RF Energy Harvester, such as the rectifier diode, matching network, and load, vary with the input power level. Lower power levels may emphasize the power loss due to the diode's forward voltage drop, thus decreasing efficiency. Conversely, higher power levels may escalate resistive losses in the matching network and load, impacting efficiency adversely.

Table 3. 4 presents the efficiency results of the RF Energy Harvester with varying input power and five units of CP. The table shows that the maximum efficiency of 32.11% is achieved with an input power of 10dBm. Thus, these results suggest that higher efficiency can be achieved if the circuit is optimized for different power inputs, either higher or lower than 0dBm. This improvement can be achieved by increasing the number of charge pump stages and optimizing the circuit, demonstrating the potential for further improvement of RF Energy Harvesters' efficiency.

Table 3. 4 Efficiency Calculation for Different Power Inputs

| Frequency (Hz) | PORT (dBm) | $R_L$(Ω) | $V_{rms}$(V) | $I_{rms}$(A) | $V_{dc}$(V) | $I_{dc}$(A) | $P_{in}$(W) | $P_{out}$(W) | η% |
|---|---|---|---|---|---|---|---|---|---|
| 2.4G | -10 | 70K | 7.41E-02 | 1.34E-03 | 2.57E-01 | 3.65E-06 | 9.96E-05 | 9.38E-07 | 0.94 |
| 2.4G | -5 | 70K | 1.49E-01 | 2.05E-03 | 1.22E+00 | 1.76E-05 | 3.05E-04 | 2.15E-05 | 7.03 |
| 2.4G | 0 | 70K | 2.96E-01 | 3.05E-03 | 3.38E+00 | 4.83E-05 | 9.01E-04 | 1.63E-04 | 18.11 |
| 2.4G | 5 | 70K | 5.61E-01 | 4.94E-03 | 7.23E+00 | 1.03E-04 | 2.77E-03 | 7.47E-04 | 26.95 |
| 2.4G | 10 | 70K | 1.05E+00 | 8.14E-03 | 13.83E+00 | 1.98E-04 | 8.52E-03 | 2.74E-03 | 32.11 |
| 2.4G | 11 | 70K | 1.18E+00 | 8.79E-03 | 1.48E+01 | 2.12E-04 | 1.04E-02 | 3.14E-05 | 30.18 |

## 3.6 CONCLUSION

In this chapter, we have detailed the design and simulation of our proposed RF Energy Harvester IC. Starting with an overview of the design process and the specifications and requirements guiding our design, we delved into the intricate design elements and optimization methods of our RF Energy Harvester IC.

The rectifier circuit, 180° Phase Shifter, and Voltage Multiplier Circuit were individually designed, and their characteristics were thoroughly analyzed. They were then brought together to form the holistic RF Energy Harvester IC. The circuit's performance was optimized through simulation and analysis, considering multiple variables, including the number of charge pump stages, component selection, and input power levels.

Following the simulations and optimization, we conducted an in-depth analysis of the input and output power of our RF Energy Harvester IC. These analyses helped us gain insights into the design's power conversion efficiency and performance. Our findings indicate that careful

optimization of the design and component selection can significantly enhance the efficiency of the RF Energy Harvester.

The work presented in this chapter underscores the potential of RF Energy Harvesting as a viable and sustainable power source for wireless devices, particularly in the era of IoT. Further research and development can undoubtedly refine these designs, improve efficiency, and broaden the scope of applications that can benefit from this technology.

# Chapter 4. LAYOUT AND FABRICATION PREPARATION OF THE RF ENERGY HARVESTER IC

This chapter focuses on preparing the IC layout using Cadence Virtuoso's TSMC 180nm technology, ensuring it is ready for tape-out. While the physical tape-out process will not be executed for this thesis project due to time constraints, every necessary preparation and verification step has been undertaken as if it would proceed to this stage.

## 4.1 Layout Design Using Cadence Virtuoso

The RF Energy Harvester IC layout design was carried out using Cadence Virtuoso, a leading CAD tool for IC design. The layout design process involved careful placement of components and meticulous routing of connections. Given the operating frequency of 2.4 GHz, attention was paid to minimizing parasitic effects that could impact the circuit's performance.

The objective during the layout phase was to create an IC that is compact and cost-effective without compromising on energy harvesting capabilities. In Figure 4. 1, the final dimension of the IC layout is approximately 0.655mm x 0.936mm. The layout includes a Ground-Signal-Ground (GSG) input pad configuration and a four-pin DC output on the left.

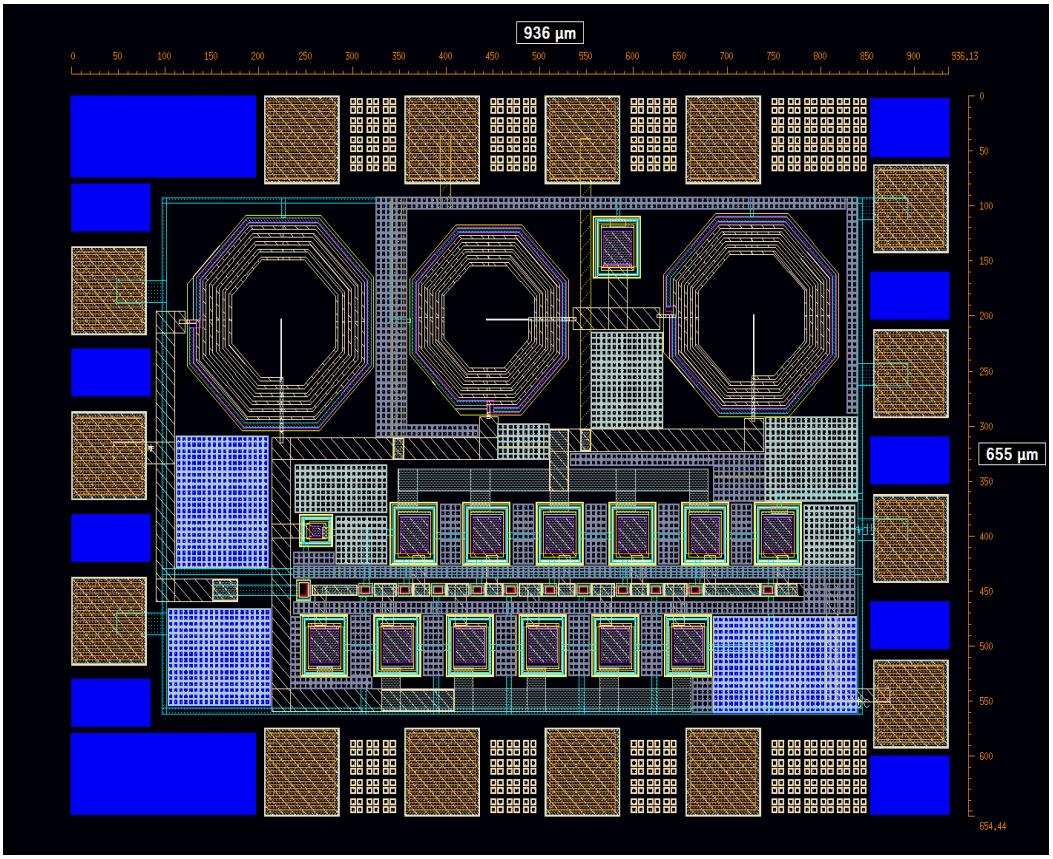


Figure 4. 1 Layout of RF Energy Harvester (0.66mm x 0.94mm)

The layout design was initiated by creating pad cells essential for signal transmission, power supply, and measurements. The pads in this design were carefully constructed using all six metal layers (Metal 1 to Metal 6), allowing for robust connections and improved reliability. These metals were interconnected via a stack of vias that facilitated a robust connection across all layers, thereby enhancing the overall reliability and integrity of the pad structure. In Figure 4. 2, each metal layer was designed with dimensions of 80 µm x 80 µm to ensure adequate contact and bonding area.

On top of these metal layers, a pad layer with dimensions of 70 µm x 70 µm was placed. This arrangement was designed to preserve the design's uniformity and offer a secure and

reliable bonding surface. The distance between the pads was set at 70 µm. This specific spacing was chosen in alignment with the capabilities of the available probing equipment in the lab, ensuring an optimal setup for testing and measurement.

The pad placements were strategically decided to cater to the circuit's functional requirements. The left pads were utilized to connect the RF signal input, serving as the point of interaction for the energy harvesting functionality. On the other hand, the right pads were purposed for measuring the DC output, enabling the assessment of circuit performance. The upper pads served a dual role; they were used for grounding, an essential aspect of any RF circuit design, and measuring the 180-degree phase shifter, a critical component of our design.

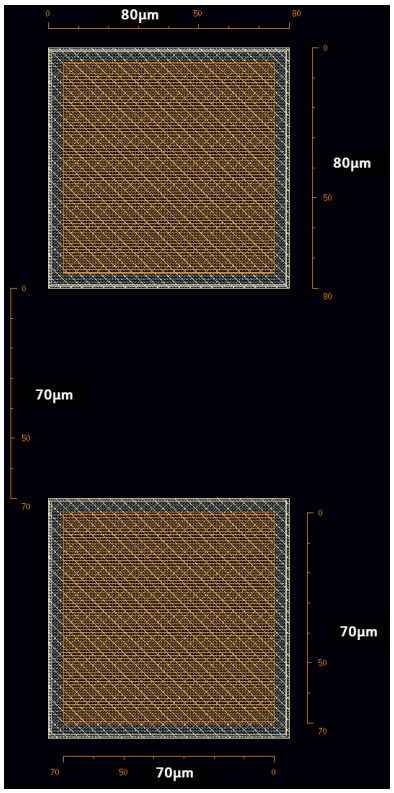


Figure 4. 2 Pads Structure and Dimensions (0.08mmX0.08mm)

## 4.2 Design Rule Check (DRC)

A Design Rule Check (DRC) was conducted following the layout design. DRC is an essential step in the IC design process, verifying that the layout meets the foundry's established set of design rules. These rules are crucial to ensure the IC can be fabricated reliably and operate as expected. The DRC checks for spacing, width, enclosure, and other parameters violations. Any violations identified were corrected in the layout.

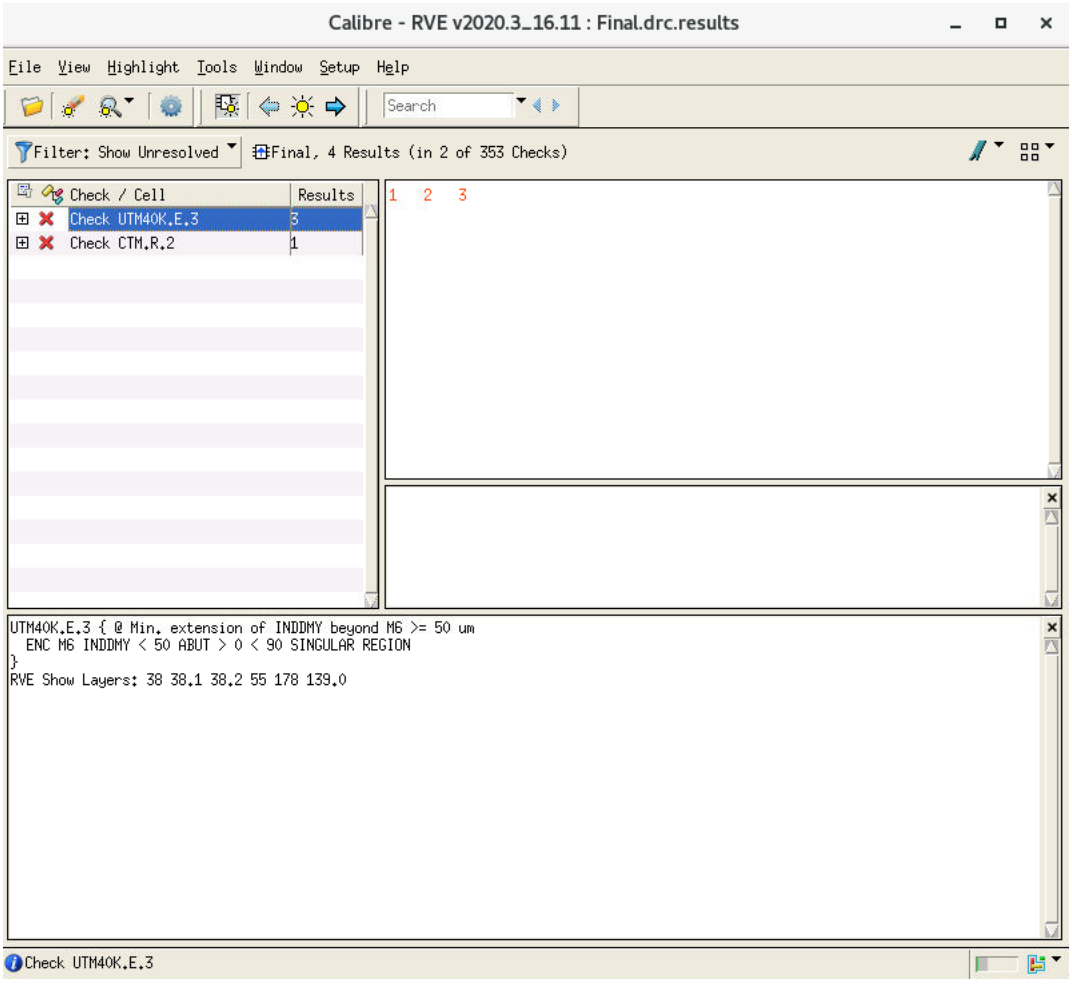


Figure 4. 3 DRC RVE Result

In the process of design layout verification, Design Rule Check (DRC) is a crucial step to ensure that the proposed IC design complies with the manufacturing capabilities of the foundry. During this step, the design is checked against a set of rules defined by the foundry to prevent fabrication issues and improve yield.

A series of errors were uncovered upon executing the Design Rule Check (DRC) for the proposed layout, leveraging the TSMC 180nm process. These errors, specifically RULECHECK PO.R.3, RULECHECK M1.R.1, RULECHECK M2.R.1, RULECHECK M3.R.1, RULECHECK M4.R.1, RULECHECK M5.R.1, RULECHECK UTM40K.R.1, and, mainly arose due to the insufficient density of various metal layers within the design.

To address these and conform to the specific density criteria for different metal layers defined by the foundry, dummy metal wires have been incorporated around the IC, enhancing the metal layer density. All the above rule checks have been integrated into the layout design, ensuring it complies with the foundry's regulations and is well-suited for manufacturing.

Furthermore, in Figure 4. 3, the error RULECHECK UTM40K.E.3 and RULECHECK CTM.R.2 was identified, a known issue with the TSMC design kit inductor. It is understood that this specific error does not pose any problems for manufacturing and can be safely ignored in the process.

This completes the DRC check for the proposed RF energy harvester IC layout, providing a clear path toward manufacturing-ready design. The following section details the Layout Versus Schematic (LVS) check for the proposed design, a necessary step to ensure the layout corresponds to the schematic.

## 4.3 Layout Versus Schematic (LVS) Check

After the DRC, a Layout Versus Schematic (LVS) check was performed. This verification step ensures that the layout matches the original schematic and that no errors were introduced during the layout design process. The LVS check ensures that the drawn layout and the schematic are functionally identical, verifying that all nodes and components are correctly interconnected. The LVS check resulted in no errors, indicating a successful match between the layout and the schematic.

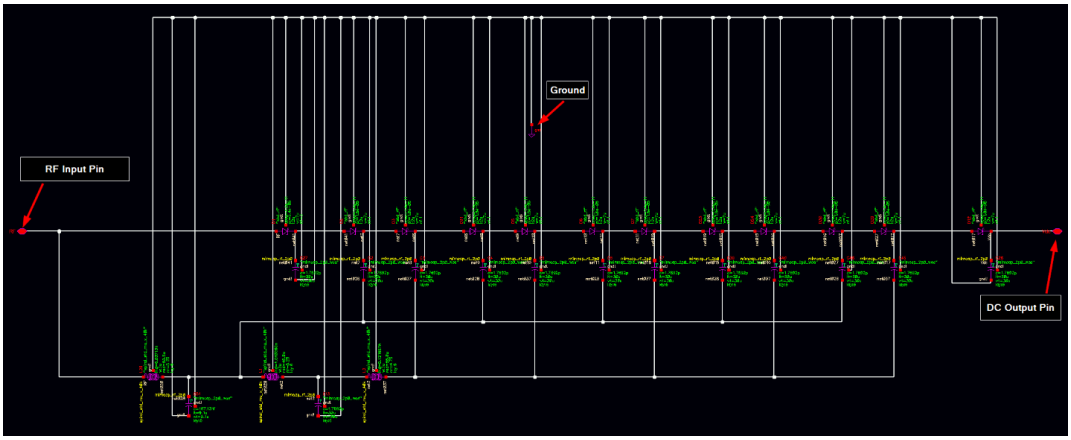


Figure 4. 4 Schematic for running LVS

To conduct the LVS check, a specialized schematic (as shown in Figure 4. 4) is prepared. This schematic is unique in that it contains no source (PORT) but uses pins to designate the input and output points of the circuit. It is crucial to mention that all sources should be connected to a single ground to ensure the integrity of the circuit during the LVS process.

The design layout (Figure 4. 3) is then compared with this schematic to identify differences. The layout and schematic must match perfectly to pass the LVS check, ensuring the layout correctly represents the intended schematic design.

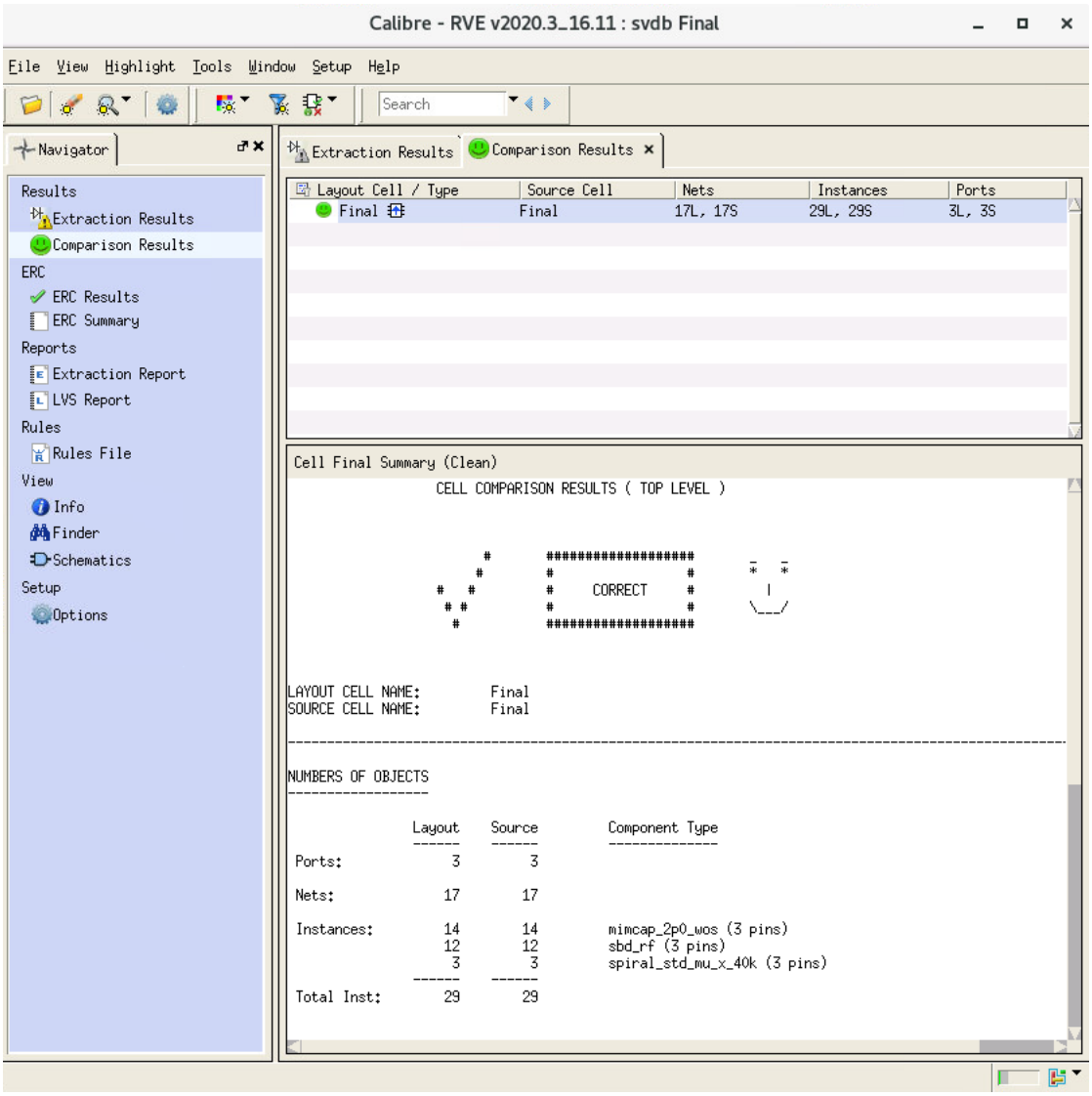


Figure 4. 5 LVS RVE Results

Continuing with the LVS check, the results obtained after a comparison between the layout and the schematic are presented in Figure 4. 5 The LVS results provide a detailed overview of the consistencies and discrepancies in the schematic (Figure 4. 4) and the layout (Figure 4. 1).

Notably, the LVS check results validate that the number of Ports, Nets, and Instances in the layout perfectly accord with the schematic design. This alignment underscores the successful replication of the schematic in the layout. It ensures that the integrated circuit, as designed in the

layout, will function as anticipated when fabricated, as it is a precise physical manifestation of the schematic design.

The LVS check's successful completion significantly reduces the risk of performance issues after fabrication, making it a critical step toward the tape-out process. The verified layout can then proceed toward the subsequent phases of the IC design flow, setting the stage for eventual fabrication.

## 4.4 CONCLUSION

This chapter covered the layout design process and the essential verification checks, DRC and LVS. Although the actual tape-out and fabrication process will not be carried out within the scope of this thesis due to time constraints, the IC layout was prepared meticulously, adhering to all necessary steps to ensure it is fabrication-ready.

# Chapter 5. CONCLUSION AND FUTURE WORK

In this final chapter, we reflect on the research journey that has led to the proposed RF Energy Harvester circuit's design, simulation, and layout for 2.4 GHz frequency. This work has revealed insightful findings and provided valuable contributions to the field of RF energy harvesting.

The main objective of this thesis was to explore the potential of RF energy harvesting as a viable solution for powering low-energy devices, particularly in IoT networks. This was achieved by designing and simulating an innovative RF Energy Harvester that balanced power efficiency and sensitivity at a high-frequency range.

We begin this chapter by summarizing the key findings and outcomes of the thesis, focusing on the insights derived from each stage of the research process. This is followed by an assessment of the work's contributions to the field of RF energy harvesting and related areas.

The chapter also discusses potential avenues for future research, building upon the findings of this work and addressing the challenges encountered during the research process. Lastly, we close with some concluding remarks on the value and implications of this work for the broader field of RF energy harvesting.

This chapter serves as an opportunity to step back and assess the full scope of the work undertaken, the progress made, and the potential future trajectories this research opens up for more sustainable and efficient energy practices.

## 5.1 SUMMARY OF THE THESIS

This study focused on designing, simulating, and optimizing a Radio Frequency Energy Harvester (RF-EH) using a 180nm Complementary Metal-Oxide-Semiconductor (CMOS) process. The RF-EH, operating in the 2.4 GHz ISM band, has shown promise in converting

ambient RF energy into usable DC power. The proposed design encompasses a rectifier circuit, a 180-degree phase shifter, and a charge pump-based voltage multiplier. The RF-EH operates optimally at 0 dBm input power, achieving an efficiency of 18.11% with a load resistance of 70kΩ and five stages of CP. Additionally, the system retains substantial efficacy at an input power of 10 dBm, reaching a peak efficiency of 32.11%.

## 5.2 CONTRIBUTIONS TO THE FIELD

The work conducted for this thesis has several significant contributions to the field. Firstly, the RF Energy Harvester design proposed in this work introduced a novel approach to RF energy harvesting by utilizing out-of-phase RF signals in a charge pump circuit, enhancing its efficiency.

Additionally, designing, simulating, and verifying the layout design provided valuable insights into the complexities and challenges associated with RF energy harvesting circuits, particularly at a high-frequency range like 2.4 GHz. This work also underscores the importance of careful analysis, simulation, and layout design in achieving desired performance parameters.

## 5.3 FUTURE DIRECTIONS FOR RESEARCH

The design presented in this work can serve as a foundation for future research in RF energy harvesting. Several areas warrant further exploration. Firstly, the design's efficiency can be further optimized by investigating more advanced charge pump and rectifier configurations and exploring alternative phase shifter designs.

Secondly, research can be directed toward realizing the proposed design's full tape-out and fabrication process. Such an undertaking would provide valuable data on the actual performance of the circuit in comparison to the simulated results.

Lastly, future work could look into designing the RF energy harvester for different frequency ranges and power inputs, integrating the design into larger IoT systems, and evaluating its performance in real-world applications.

## 5.4 CONCLUDING REMARKS

In conclusion, this thesis has significantly enhanced our understanding of RF energy harvesting at high frequencies. The design and simulation of the RF Energy Harvester presented in this work have illustrated the potential of such circuits in powering IoT devices and contributing to more sustainable energy practices.

The challenges faced, and the solutions proposed throughout this work have underscored the importance of rigorous design and analysis processes. This work serves as a steppingstone for future research endeavors to improve RF energy harvesting technologies and their applications in our increasingly connected world.

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