Wafer-scale High-bandwidth Germanium on Silicon Photodetectors for Communications Applications

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Li He

To my family

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Abstract

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The Silicon-on-Insulator (SOI) material system has emerged as a potentially attractive platform for integrated optics, due to the intrinsic low-cost of silicon manufacturing. An especially attractive application is that of telecommunications. One key component for telecommunications applications is high-performance photodetectors, which convert an optical signal to an electrical signal. The key performance metrics for waveguide-coupled photodetectors include low dark current, high responsivity and high bandwidth. In addition, the cross-wafer performance and defectivity is also of great importance, on which the yield of eventual systems will rely. Here I report the first cross-wafer data for waveguide-coupled Ge-on-Si photodetectors based on vertical p-i-n configuration. The performance across the whole wafer is relatively uniform and exhibits low defectivity.

Detectors working at speeds up to 20 GHz with 4V reverse bias are achieved, with high responsivities of 0.5 A/W. I describe the testing and characterization methods used to measure the performance of these devices, and identify the source of the bandwidth limitations, and show how these photodetectors are optimal for use at telecom wavelengths, consisting of light with a free-space wavelength near 1550 nm. Finally, a path forward for optimizing the devices in this process is presented. Based on our measurements, using only modest changes in device geometry, it should be possible to improve bandwidths to 70 GHz or more, and responsivities to 1 A/W or more. I propose specific device geometries to implement this improvement. This level of performance is sufficient for SOI based Ge photodetectors to implement even the most high-bandwidth optical telecommunications systems, and should help to make SOI an important platform for integrated optics.

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Chapter 1 Introduction and overview

1.1 Introduction to SOI platform

Silicon has become dominant in the electronics industry over the past few decades. Silicon is not the best material for individual electronic device performance in many cases; for example, superior transistor performance can frequently be obtained in III-V material systems [1]. But due to the low cost and high yield possible on this platform, the most complex electronics systems are nonetheless constructed in silicon [2].

Silicon-On-Insulator has recently emerged as a type of silicon wafer with a number of unique advantages relating to electronics performance. Fig. 1.1 (a) shows the typical geometry of SOI wafer. A thin layer of Silicon with thickness typical varies from tens of nanometers to a few microns [3] is deposited on buried oxide layer (BOX) and active devices are built on the top silicon layer. A silicon handle layer is added to the bottom of BOX to ensure the mechanical strength.

Figure 1.1 (a) Typical geometry of SOI wafer. (b) an 8'' SOI wafer [4].

Silicon-on-Insulator is also an attractive material system for optics in the near infrared region (NIR). Due to the high refractive index contrast between silicon (3.48) and silicon oxide (1.46), SOI geometry provides strong optical confinement capability for telecommunication wavelengths. Also the material absorption of silicon in NIR is low [5], making it possible to achieve low loss optical waveguide on SOI platform with ultra-compact mode profile [6]. Moreover, by taking advantages of the properties of silicon, such as the free carrier effect and capability of growing Germanium on Silicon, many types of opto-electronic devices have been demonstrated on SOI platform. For example, high-performance opto-electronic modulators [7] and photodetectors [8] operating at gigahertz speeds have been achieved in recent years. These results make SOI an attractive platform for integrated optics in the NIR.

1.2 Silicon photonics in optical communication

Optical communications have been experiencing rapid expansion over the few decades, due to the ultra-high bandwidth and ultra-low losses that the optical fibers can offer [9]. For a typical optical communication system, light emitted from laser is modulated by the optical modulator before being sent via optical fibers. Photodetectors at other end of optical fibers can convert the optical signals back to electrical signals for further processing. The applications of optical communications include optic fiber communications [9] and optical interconnections, where optical waveguides are used to connect each cores within computers [10]. SOI platform is likely to be useful in terms of optical communications for many reasons, such as the low cost and high yields, large-

scale integration of optical devices with small footprint, as well as the potential possibility of integration with electronics.

The challenge for silicon photonics as the platform for optical communication in the NIR is that it does not provide the best device performance in many case compared with other III-V materials, the conventional platform for opto-electronic devices. There are many examples of this. For one, it has until recently been impossible to build a laser of any kind in silicon due to the indirect bandgap. Strained Germanium based lasers have recently been demonstrated [11-14], but the performance remains far below what can be achieved in III-V based materials, and is presently not good enough for optical communications applications. In photodetector technology, silicon has until recently had inferior performance to III-V based detectors, though there has been a recent demonstration of 100 GHz+ photodetectors in silicon, based on a lateral p-i-n junction [15]. But the question of yield and cross-wafer uniformity remains completely unaddressed; given the costs of manufacturing a single wafer, if silicon is to be competitive it must be possible to build thousands, if not millions, of devices on a single wafer.

1.3 Germanium photodetectors on silicon on insulator platform

At this point, photodetectors on SOI platform is based on Germanium-on-Silicon structure (Ge-on-Si). Ge is chosen to be the light absorption material of photodetectors due to its relatively high absorption coefficient in the NIR, as well as the capability of Ge growth on top of silicon layer in the CMOS compatible process [8]. The typical type of

Ge-on-Si photodetectors is based on p-i-n configuration, where light absorption occurs within depletion region of a p-i-n diode and optical-generated free carriers can be swept out quickly, due to the strong electric field in this region. Ge-on-Si photodetectors based on photoconductive effect and avalanche effect have also been investigated with the responsivity goes beyond the quantum limitation [16]. These detectors with high responsivity are of great significance in terms of small signal detection.

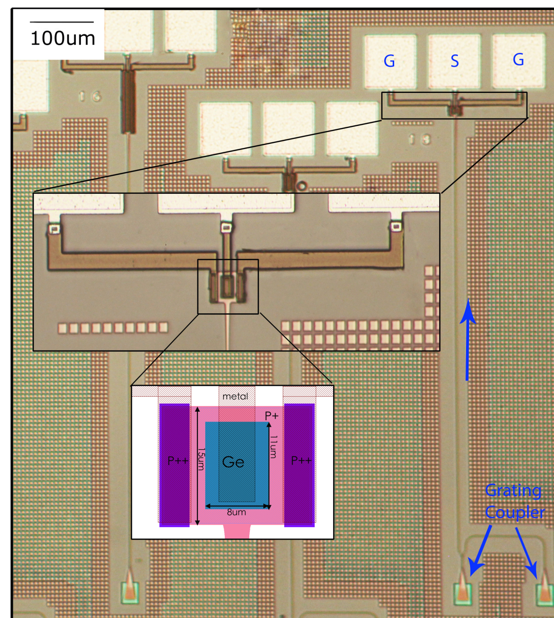

Figure 1.2 The lateral layout of fabricated Ge-on-Si calibration structure; light is directed into detector through grating couplers [17].

The key performance metrics of photodetectors include low dark current, high responsivity and high operating bandwidth. Due to the small footprint, the dark current of a Ge-on-Si photodetector can be reduce to around 10 nA [18], although it suffers from high dark current density due to high dislocation density within Ge film. On the part of detector responsivity, with waveguide-coupled geometries, most part of incident light can

be absorbed and it is expected to achieve high responsivity approach to quantum limitation for detectors without internal gain mechanics.

1.4 Outline of results, analysis and path to improvement

In this thesis, I report a waveguide-coupled germanium-on-silicon photodetector design based on vertical p-i-n configuration. The device shows high operating bandwidth of 20 GHz at 4V reverse-bias, with responsivity of 0.5 A/W. Besides, the cross-wafer detector performance has also been examined and relative uniformity in device performance and low defectivity is observed. Moreover, theoretical models are developed and the comparison with measured data is conducted in order to identify the performance limitations to the current devices. Based on these models and measurements, I propose specific device geometries that may improve the bandwidth up to 70 GHz and the responsivity close to 1 A/W or more in this process, hopefully maintaining the high level of uniformity and yield observed here, while simultaneously achieving performance to rival that of III-V detectors.

Chapter 2 Motivation and fabrication for Ge-on-Si photodetectors

2.1 Material property of germanium

Ge is a promising material to be used for light absorption on silicon platform. Ge is an indirect band gap material with direct band gap of 0.8 eV and indirect band gap of 0.664 eV at room temperature [19]. Due to its small bandgap, germanium has relatively high absorption coefficient for wavelengths ranging from visible light to the NIR and is used as the absorption material of photodetectors in optical communications. In addition, it is possible to selectively grow Ge on a Si wafer since they have the same crystal structure, though the relatively large lattice mismatch (4.2%) makes it difficult to achieve Ge on Si with low dislocation density. Due to both the relatively high absorption coefficient and the capability of Ge growth on Si, Ge has been used for photodetector fabrication on the silicon platform. Another consideration is the widespread use of so-called BiCMOS processes, which utilize Si-Ge based transistors [20].

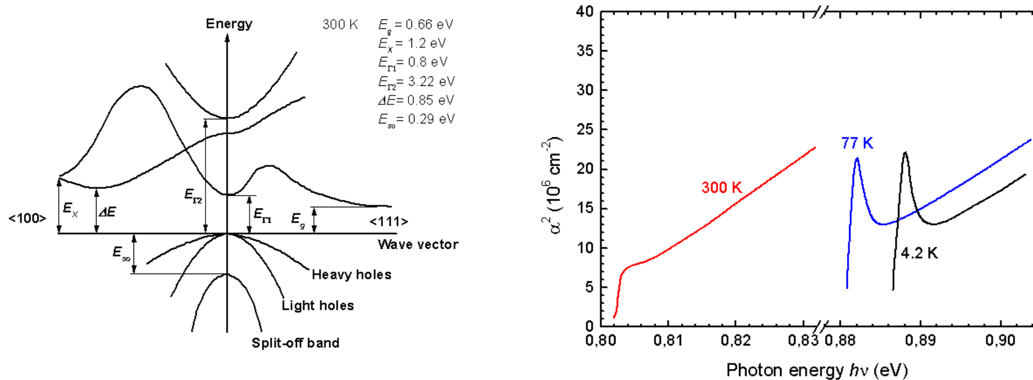

Figure 2. 1 (a) Band diagram of bulk Ge at room temperature. (b) Absorption spectrum for Ge at different temperature [19].

2.2 Growth of germanium on silicon substrate

As mentioned previously, to achieve Ge film on Silicon substrate with high quality is challenging due to the relatively large mismatch (4.2%) in terms of atom lattice. For example, the direct transition between Si and Ge layers will introduce high threading dislocation density [8], which function as a recombination centers and increases dark current of detector.

At present, there are two main strategies have been successfully developed to resolve this problem: to either utilize a graded SiGe layer [8] or thin Ge layer grown under low temperature as the buffer layer [8] before the growth of main Ge film so as to avoid the abrupt atom lattice change. For the latter approach, which is adopted for our device fabrication, a thin Ge layer with thickness of tens nanometers is directly grown on silicon layer under low temperature (around 350 °C) before the growth of main Ge film. With the help of thin Ge buffer layer, the transition of atom lattice is smoother and one can grown the second Ge layer easily. With the introduction of buffer layer in Ge growth process, it is reported that Ge film on Si with low dislocation density on the order of 10^6 cm^{-2} [21] have been achieved with the two-step Ge growth approach.

In addition, other approaches such as wafer bonding between silicon wafer and Ge wafer [22] that are also able to achieve high-quality Ge layer on Si exist, though they associated with more complicated fabrication processes.

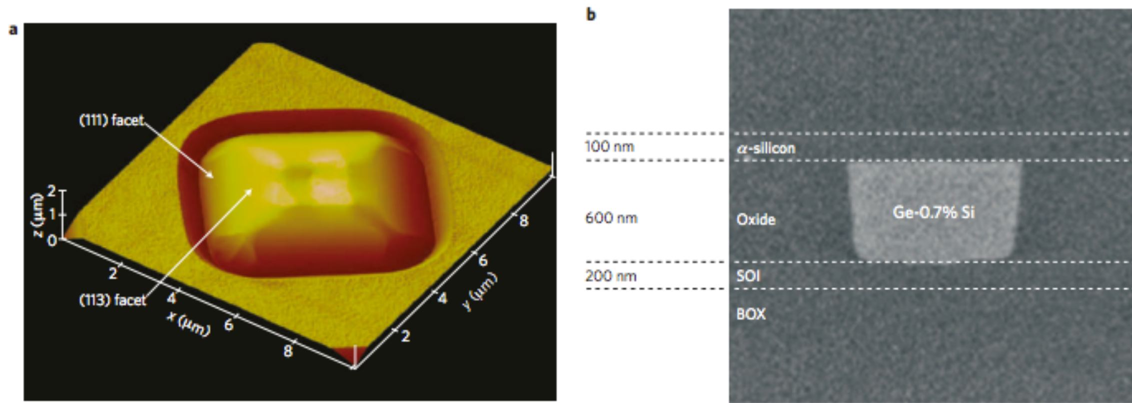

Figure 2.2 Selective growth of germanium on silicon substrate. (a) Atomic force microscope image of a selectively grown Ge mesa in a SiO_2 window. (b) Selectively, trench-filled Ge. Process-integrated structure of a p-i-n diode using Ge-0.7% Si on a SOI substrate [8].

2.3 Germanium with tensile-strain

For bulk Ge, as shown in Fig. 2.1 (b), the absorption coefficient decreases greatly for wavelengths longer than 1550 nm, since the photon energy is smaller than the direct band gap energy and phonons are needed to assist the light absorption process, which has less possibility to occur compared with direct band gap transition. For example, the absorption coefficient of bulk Ge is reported to be only 0.2 dB/μm.

The existence of tensile strain can shrink the Ge's band gap and hence tune the optoelectronic properties of Ge film [11-14]. For example, recent research shows that detector length of 10 μm is enough to absorb incident optical light completely [23]. Fortunately tensile-strain is usually introduced into Ge film as desired during the growth of Ge. For two-step Ge growth technique, since the atomic lattice of Ge is larger than that of Si, compressed strain exists within Ge film after the growth of first thin Ge buffer

layer. However, the second Ge growth process occurs under high temperature and the Ge layer formed during the second step is target around hundreds nanometers, much thicker than the buffer layer. As a result, it is tensile strain instead of compressive strain that exists in Ge film after the thermal annealing step [8].

2.4 Doping techniques

In the field of semiconductors, ion implantation is a widely used technique by which the electrical property of semiconductor material can be changed and p-n junctions are formed. In the process of ion implantation, dopants are accelerated externally to high speed before impinging on the target wafer. Due to the high kinetic energy dopants can penetrate into substrate material and finally be stopped by collisions with substrate atoms and drag from electrons, staying within substrate material [24]. Thermal annealing is followed to activate dopants and recover the damages resulted from dopants penetration.

Note that the donor/acceptor concentration is a function of position within the substrate material, since the doping penetration is in fact a random process and penetration depth of dopants usually has a statistical distribution. One can modify doping recipes, such as dose concentration, ion energy as well as species of dopants to achieve doping profile according to different applications. For example, in order to reduce the resistance between metal electrodes and silicon substrate, a n-type doped recipe is used with target doping concentration up to 1e20 cm^{-3} to form the ohmic contact.

In addition to ion implantation, there are other doping techniques existing that introduce dopants into semiconductor materials. For example, the in-situ doping can introduce the dopants into materials as they are deposited [25]. Also one can achieve very high doping concentration by using diffusion doping approach, which is based on the dopant diffusion into substrate materials under high temperatures [25].

The doping profile in Ge film is of great importance in terms of device performance and extra attention should be paid on Ge implantation recipe. For example, the high peak doping concentration up to 1e20 cm^{-3} is desired to form a good contact with metal electrodes. Besides, the tail of doping profile should be reasonably short with the purpose of achieving wider intrinsic region. In particularly, the dopant concentration should decrease from the order of 1e20 cm^{-3} to 1e16 cm^{-3} within 150~200 nm. The Sentaurus Monte Carlo model [26] is used to simulate the doping profile (Fig 2.3) of implantation recipe used for our device. Unfortunately ion implantation is somehow process-dependent and careful calibration work need to be done in order to achieve good agreement between theory model and measured results.

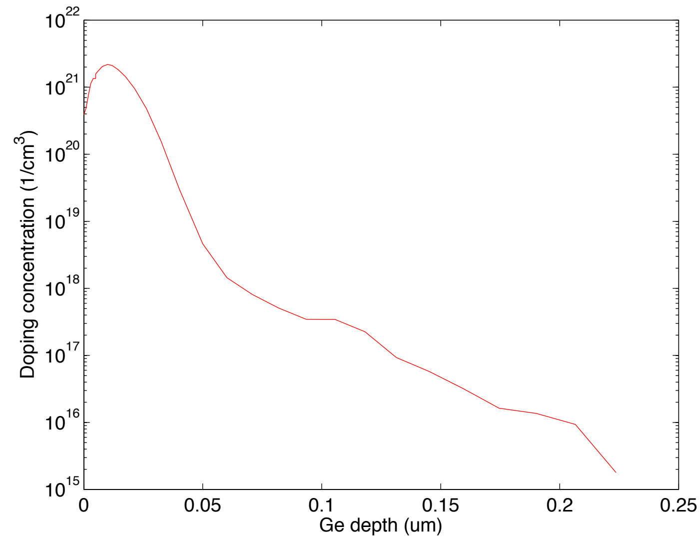

Figure 2.3 Doping profile before thermal annealing activation for phosphorus penetrates into Ge film.

Chapter 3 Performance metrics of photodetectors

3.1 Mechanics of p-i-n photodetectors

The p-i-n diode is the most popular configuration for semiconductor photodetectors, though light absorption materials may vary based on different material platform. This is due to the intrinsic advantage of p-i-n junction that strong build-in voltage within depletion region that can sweep out free carriers excited by incident photons effectively. The mechanics for a p-i-n detector is quite straightforward (Fig 3.1): a wide intrinsic region of p-i-n diode can be used to absorb light effectively due to the large depletion area. Optical-generated electron-hole-pairs (EHPs) within depletion region will be separated towards the two electrodes without recombination and eventually contributing to the photocurrent. Usually reverse bias is applied to the p-i-n diode in order to enhance the electric fields and reduce parasitic capacitance so that device performance can be further improved.

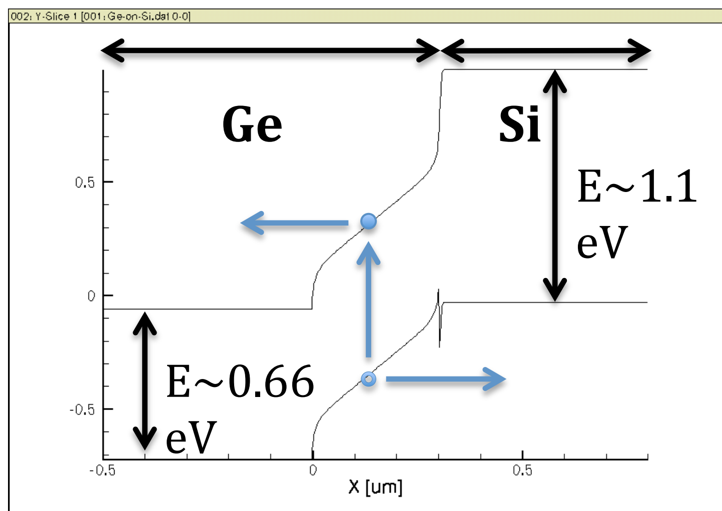

Figure 3. 1 Band diagram of Ge-on-Si p-i-n photodetector, the n and i region is made of Ge while p region is made of Si.

3.2 Responsivity

The responsivity of photodetectors is defined as the ratio of photocurrent to incident light intensity with unit of A/W. For detectors without any internal gain mechanics, if all incident photons contributed to the generation of EHPs and all of them were finally collected by electrodes, then the responsivity would reach its maximum value, which is called quantum limitation. For wavelength at 1550 nm, the maximum responsivity can be determined as:

$$\mathcal{R} = \frac{I}{P} = \frac{e\lambda}{hc_0} = 1.25\ A/W \qquad (3.1)$$

Unfortunately loss is inevitable in the process of light absorption and not all optical-generated EHPs can contribute to the photocurrent. For this reason the responsivity turns out to be smaller than quantum limitation. For example, light absorption may occur in the quasi-neutral region and free carriers generated at this region will not contribute to the photocurrent for detectors. Photons will also be dissipated if they touch the metal contacts or simply not be absorbed due to the limited absorption ability for detectors with finite length.

For some applications where responsivity higher than quantum limitation may be needed, one could either add amplification circuits after detectors or use detectors with internal gain. The common types of detectors with internal gain are avalanche photodetectors (APDs), phototransistors [27] and photoconductive detectors, among which APDs are the most commonly used one in applications like fiber optic communication and area of fundamental research. The most attractive feature of APDs is the extremely high gain,

which can be up to 10^5 to 10^6 [28]. On the other hand, APDs are also notorious for their high noise and high operating voltage.

3.3 Dark current

The dark current is defined as the measured reverse bias current of the photodetector without light illumination. Basic knowledge of semiconductor device informs us that the dark current of a p-i-n diode comes from two components: (1) For an ideal p-i-n junction under thermal equilibrium, the forward diffusion current balances with reverse drift current and the net current is zero. Once an external reverse bias is applied, the voltage is almost drop across depletion region and the effective barrier height increase, which turn out to impede forward diffusion current and leads to net reverse current; (2) In practice, free carrier generation within depletion region, due to the high density of recombination centers, dominates the reverse leaking current [2]. Based on Shockley-Hall-Read theory, for indirect band gap materials like Si and Ge, most of free carriers are generated and recombined with the help of local states (recombination center) within the band gap instead of directly transition between valence band and conduction band. For the depletion region of a p-i-n junction, with the assumption of equal hole and electron capture cross sections, the net free carrier generation rate is [2]:

$$U = \frac{n_i^2\left(1-e^{\frac{qV_a}{kT}}\right)}{\left(p+n+2n_i\cosh\left(\frac{E_t-E_i}{kT}\right)\right)\tau_0} \tag{3.2}$$

When reverse bias is applied, the net generation rate is positive, which means there are reverse current J_r contributing to the total leaking current [2]:

$$J_r = q\int_{-x_p}^{x_n} U dx \tag{3.3}$$

The reverse current J_r is proportional to the defects concentration, since

$$\tau_0 = \frac{1}{N_t \sigma v_{th}} \tag{3.4}$$

where N_t is the density of defects within depletion region.

High dark current is detrimental for practical applications like high-speed optical interconnection, including high power consumption and small signal to noise ratio (SNR). For the former one, the power consumption of detectors without light illumination is proportional to the product of reverse bias and dark current, since detectors are usually working under reverse-bias to improve frequency response. For this reason, to decrease the dark current to a low level is essential to achieve detectors with low power consumption. On the part of noise in detectors, dark shot current is one of the major components and can be calculated with following formula:

$$I_n = \sqrt{2qI_{dark}B} \tag{3.5}$$

Where q is the electron charge and B is device bandwidth. Apparently low dark current is also beneficial to reduce dark shot current as to improve the SNR.

3.4 RC bandwidth

One of the attractive features of Ge-on-Si p-i-n detector is the potential high operating speed, which makes it to be useful in high-speed communications applications. One of the limitations to photodetector bandwidth is the long RC charging time results from the large parasitic capacitance and resistance.

a. Junction capacitance

For a homogeneous p-i-n junction with uniform doping concentration on both sides, depletion approximation can be used to analysis the junction behavior, where we assume electric fields only exist within depletion region while the quasi-neutral region is under equilibrium. With these assumptions, one can readily write down the build-in voltage as a function doping concentration under thermal equilibrium [2]:

$$\phi_i = \frac{KT}{q} \ln\left(\frac{N_d N_a}{n_i^2}\right) \tag{3.6}$$

K: Boltzmann constant;

q : electron charge;

n_i: intrinsic carrier concentration;

N_d: donor concentration;

N_a: acceptor concentration.

Moreover, according to Gauss's law, the total charge within depletion region must be zero in order to ensure no electric fields in quasi-neutral region. This requirement can be written as:

$$N_d x_n = N_a x_p \tag{3.7}$$

To combine equations (3.6) and (3.7), considering the length of intrinsic region, the whole width of depletion region is:

$$L = x_n + x_p + w = \left[\frac{2\epsilon_s}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(\phi_i - V_a)\right]^{\frac{1}{2}} + w \tag{3.8}$$

ε_s material permittivity;

V_a: applied reverse bias;

Note that applied reverse bias can expand the depletion region. If the applied reverse bias has a small change, like under the condition of light illumination, the edge of depletion region would also move. Suppose the edge of depletion region on n side move from x_n to x (x_n - x is small with small signal assumption), the corresponding space charge change within depletion region is:

$$dQ = N_d(x - x_n) = N_d dx \tag{3.9}$$

According to Gauss's law, this will induce the change in electric field within depletion region:

$$dE = \frac{dQ}{\epsilon_s} \tag{3.10}$$

One can readily obtain the potential change as a function of electric field change as:

$$dV = dE * L = \frac{dQ}{\epsilon_s} * L \tag{3.11}$$

So the behavior of p-i-n junction with reverse bias can be described as a capacitor:

$$C_d = \frac{dQ}{dV} = \frac{\epsilon_s}{L} \tag{3.12}$$

Once the light is turn on, an amount of photo-generated carriers will contribute to the expansion of depletion region before the formation of the steady photocurrent. This is equivalent to charge a parallel RC circuit with a steady current source.

The real situation is more complicated than the simple homogeneous p-i-n junction analyzed above for two reasons: (1) for Ge-on-Si photodetector, a hetero p-i-n junction is formed, since the p region is made of Si while the n and intrinsic region are made of Ge; (2) the doping concentration in both p and n region is a function of position instead of uniform distribution. No analytical solution exists for the junction capacitance in this case and numerical method is needed in order to obtain accurate solution based on the material

property of Si and Ge. Hopefully, accurate prediction of detector capacitance is unnecessary and parallel capacitor approximation can always provide a reasonable estimation as long as the effective capacitor area is large enough compared with depletion depth.

b. Lumped-element model

As a rule of thumb, a circuit element can be treated as lumped once its maximum size is 1/20 of wavelength [29]. For an element with dielectric constant of 12 (Si), the corresponding maximum size is about 86 μm for 50 GHz. This suggests that waveguide-coupled Ge-on-Si photodetector can be modeled with a simple lumped element method to the first order as long as the length of the detector is less than 80 μm for frequency lower than 50 GHz. The typical equivalent circuit model of Ge-on-Si photodetectors is shown in Fig. 3.2, where C_d is the parasitic capacitance of p-i-n diode, while R_l is load resistance, usually it is transmission line with 50Ω impedance. R_d is the parasitic resistance, mainly comes from n type and p type doped Ge and Si region. Note that metal pads (80 x 80 μm for following designs) are used to couple electrical signal into and out of devices, this is equivalent to add a metal pad capacitor C_p paralleling with load resistor, though it is not the intrinsic capacitance associated with detector itself. Based on lumped-element analysis we obtain the 3dB bandwidth for the following circuit model as:

$$f_{3dB} = \frac{1}{2\pi(R_d+R_l)C_d} \tag{3.13}$$

where the pad capacitance is ignored in above RC bandwidth calculation.

Limited by the relatively small light absorption coefficient of Ge at 1550 nm, Ge film with lateral dimension on the order of 100 μm^2 is usually used to ensure completely light absorption [30]. The consequence is that large parasitic capacitance associated with the Ge film impedes response speed.

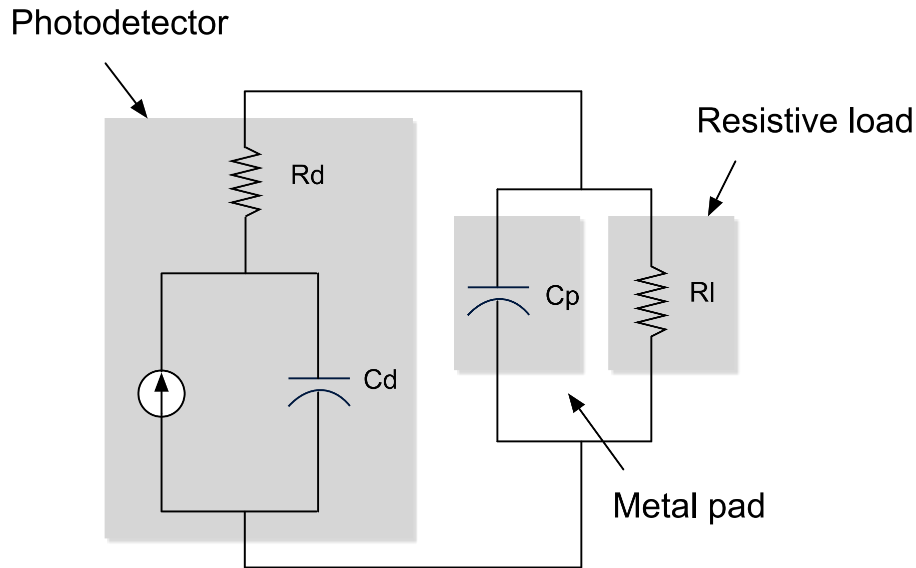

Figure 3.2 Equivalent lumped-element model for Ge-on-Si photodetectors

3.5 Transit-time bandwidth

The device speed is usually limited by the long RC charging time, since thin Ge film with thickness less than 1 μm is used and detector lateral dimension is on the order of 100 μm^2 in order to achieve high responsivity. However transit time begins to impede device bandwidth once detector dimension shrinks so that RC charging time is small enough compared with transit time.

After the free carriers are generated by photo-absorption, they will be swept out of the active region by the build-in electric fields without recombination and finally collected by electrodes. However, since the mobility of free carriers is a finite number, the long travel distance can degrade the speed response. We estimate the transit-time bandwidth in the following way, where we assume device speed is only affected by transit time and no other factors (like RC charging time) need to be taken into account. We also suppose the depletion region start from 0 to L and uniform optical generation within depletion region:

$$P(t) = hv * n_0 Lexp(i\omega t) \tag{3.14}$$

Then the collected photocurrent can be written as:

$$i(t) = e * \int_0^L n_0 exp\left[i\omega\left(t - \frac{x}{v}\right)\right] dx \tag{3.15}$$

Where v is the velocity of free carrier.

$$i(t) = -e\frac{vn_0}{i\omega} exp(i\omega t) \int_0^L exp\left(-\frac{i\omega x}{v}\right) d\left(-\frac{i\omega x}{v}\right)$$

(3.16)

$$= -e\frac{vn_0}{i\omega} exp(i\omega t)\, exp\left(-\frac{i\omega x}{v}\right)|_0^L = e\frac{vn_0}{i\omega} exp\,(i\omega t)\left[1 - exp\left(-\frac{i\omega L}{v}\right)\right]$$

The ratio between photocurrent and incident light intensity is:

$$\mathcal{R} = \left|\frac{i(t)}{P(t)}\right| = \frac{e}{hv} * \frac{v}{\omega L}\left|1 - exp\left(-\frac{i\omega L}{v}\right)\right| = \frac{e}{hv} * \frac{1}{\omega\tau}|1 - exp(-i\omega\tau)| \tag{3.17}$$

where $\tau = L/v$ is transit time for free carriers to cross the depletion region. When the incident light only contains DC component,

$$\mathcal{R} = \frac{e}{hv} \tag{3.18}$$

The responsivity would decrease as frequency increase. The 3 dB frequency is defined so that the responsivity reduce to $\frac{1}{\sqrt{2}}$ of it for DC component,

$$\mathcal{R} = \frac{e}{h\upsilon} * \frac{1}{\omega_{3dB}\tau} |1 - exp(-i\omega_{3dB}\tau)| = \frac{e}{h\upsilon} * \frac{1}{\sqrt{2}} \tag{3.19}$$

So that

$$f_{3dB} = 0.44/\tau \tag{3.20}$$

This equation reveals that the 3 dB bandwidth is inversely proportional to transit time. If we set the width of depletion region and saturation velocity of free carrier to be 500 nm and 6 x 10^6 cm/s, respectively, the 3 dB bandwidth determined by transit time is limited to be around 53 GHz. Transit time is determined by electric fields intensity, free carrier mobility and separation of the two electrodes. In order to ensure free carriers travel at saturation speed with low external reverse bias, one needs to design the doping condition so as to achieve large build-in electric field. Besides, high-quality Ge layer is also important for free carrier saturation velocity since defects in Ge could reduce its mobility. Another practical way to relieve transit time limitation is to reduce the thickness of intrinsic region for p-i-n detector or the separation of the two electrodes for MSM detector. However, this would also increase parasitic capacitance associated with detector and aggravate RC charging time.

Chapter 4 Vertical p-i-n photodetectors

4.1 Geometry of vertical Ge-on-Si photodetectors

At present, either vertical or lateral p-i-n configurations have been demonstrated for waveguide-coupled Ge-on-Si detectors with high performance [31-33]. For waveguide-coupled detectors, both evanescent and butt coupling schemes can be used for light

coupling from Si waveguides to Ge layer. Here I present a vertical p-i-n Ge-on-Si detector design with operation speed up to 20 GHz at 4V reverse-bias. The cross-section view of the device is depicted in Fig 4.1. The 500 nm thick Ge layer is grown on active silicon layer of 220 nm. The p-i-n junction is formed by applying n type doping in Ge and p type doping in Si, respectively. Si p++ region and metal contacts are placed 2 μm and 2.5 μm away from the edge of Ge region to ensure these highly loss region will not touch the incident optical mode. Detectors with length vary from 15 to 100 μm were fabricated so as to explore the impact of detector length on its performance.

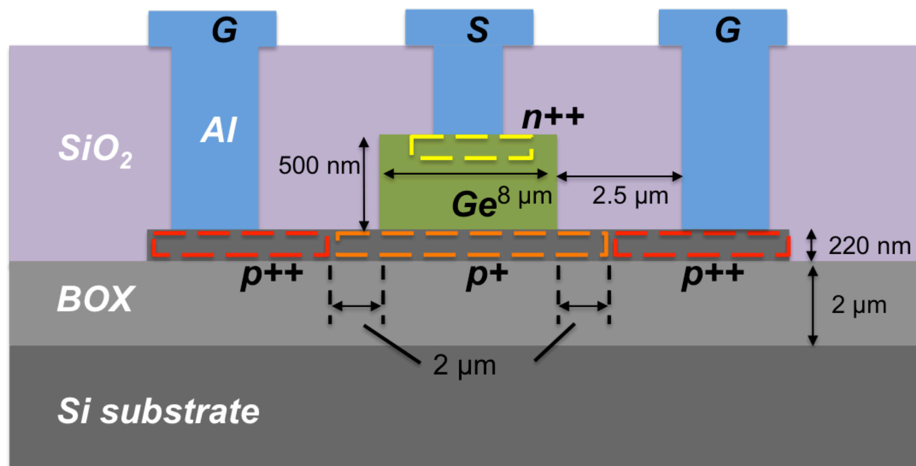

Figure 4.1 The vertical layout of Ge-on-Si detector.

4.2 Fabrication process

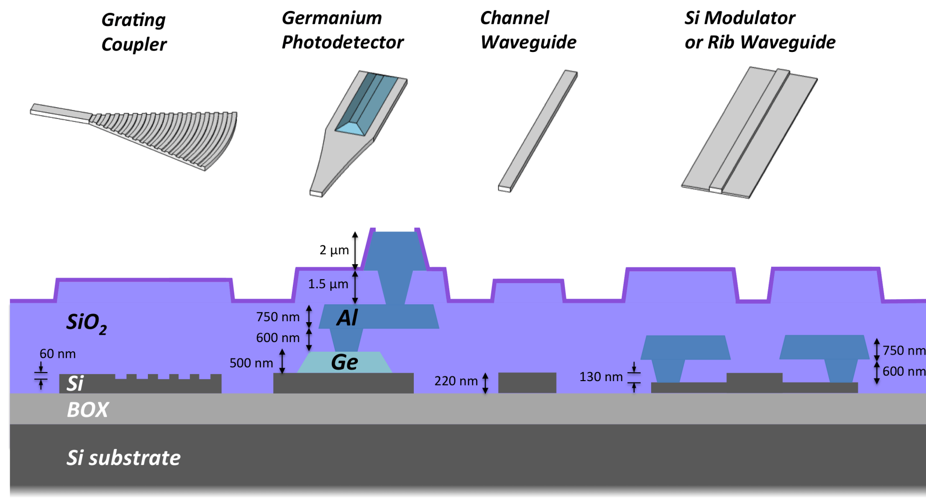

Figure 4.2 The cross-section view of the wafer, where photodetectors were built on [17].

Devices are fabricated on an 8’’ inch SOI wafer from SOITEC, in where other components such as modulators, grating couplers are also included [17]. The initial top Si layer is 220 nm thick sit on buried oxide layer (BOX) of 2 μm. Three partial etch steps were performed to define ridge waveguide. For all etch steps 248 nm photolithography was used. After the finish of all etch steps, various ion implantations were utilized to define p++, n++, p, n, p+ region in Si substrate, followed by the thermal annealing at 1030 C for 5 s for dopants activation. Then a SiO_2 mask layer was deposited and to grow Ge with a target thickness of 500 nm in the exposured region, which was not covered by the former deposited SiO_2 mask layer. After the selective growth of Ge, ion implantation into Ge was utilized to form the n++ region at top surface of Ge film, followed by a thermal annealing at 500 C for 5 min. Two layers of Aluminum were then deposited to form the metal vias and traces.

4.3 Layout and testing considerations

Fig. 4.3 shows the basic testing structure used to calibrate detector performance. We utilized a fiber array with polished facet to couple light into and out of the grating couplers (GC) [34]. The fiber array was titled during testing so that the GCs achieve maximum coupling efficiencies at 1550 nm. A polarization controller was placed in front of input port of the fiber array in order to ensure that only TE light was directed into the GC, since the GCs used are designed to support only TE polarization. In Fig. 4.3, the left GC is used to couple light from single mode optical fiber into silicon waveguides, followed by a Y-junction to split light into two branches. One of the branches of Y-junction is connected to detector while the other one is connected with the right GC. Since the two GCs are close to each other, with separation of 127 μm, we assume that the their coupling efficiencies are identical.

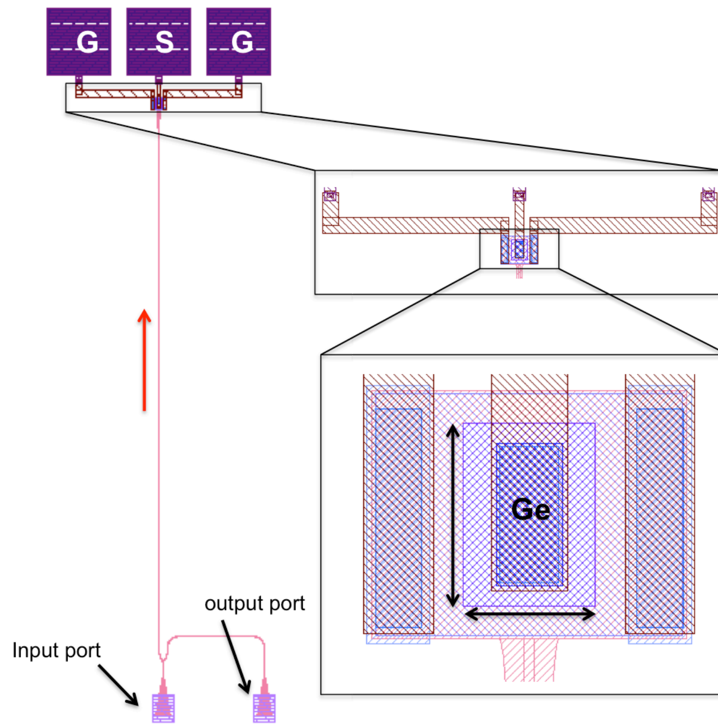

Figure 4.3 Experiment configuration for detector responsivity and dark current

The insertion loss of GCs and Y-junctions can be determined from corresponding testing structure shown in Fig. 4.4. Once both the insertion loss of GCs and Y-junctions are known, we could infer the actual optical power launched into detector. Three metal pads are used for RF probing, which are arranged as ground-signal-ground (GSG) configuration. External reverse bias can also be applied via these metal pads. We also control the experiment temperature and all characterization is done at 35°C.

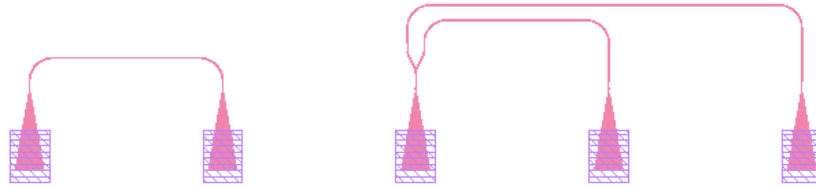

Figure 4.4 Testing structures for grating couplers (left) and Y-junctions (right). Optical radiation is directed into one coupler, and retrieved from the other coupler. Due to optical reciprocity, the losses for each individual GC can be determined. The Insertion loss of Y-junction can be determined once GC loss is known.

Chapter 5 Experimental overview and results

5.1 Dark current and responsivity measurement

Dark current is measured when laser is turn off and no optical power is incident into detectors via GCs. The device's I-V curve is obtained by sweeping the external bias voltage and measure the output current. The same steps are used for responsivity measurement, except that laser is turned on to provide incident light into detectors via GCs. The insertion loss of GCs and Y-junctions need to be measured in order to determine the actual amount of power that incident into detectors.

5.2 Capacitance measurement

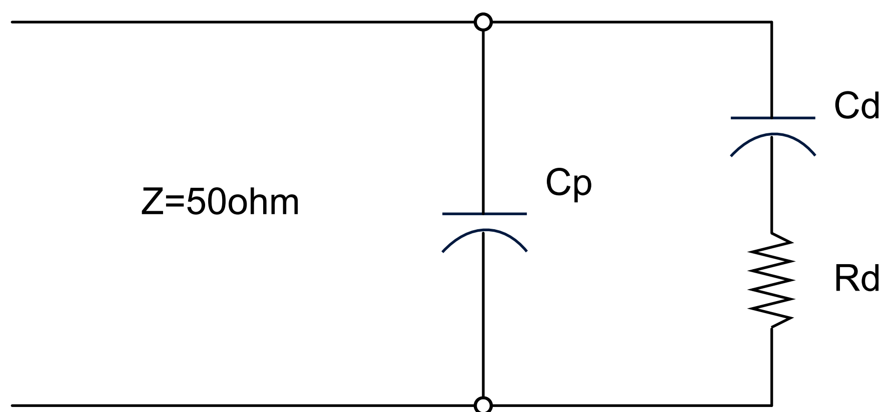

Figure 5.1 Equivalent lumped-element circuit for capacitance measurement configuration

We measure the capacitance of detectors by sending a signal with frequency ranging from 100 MHz to 1 GHz and testing the arg of S11 while keeping the detector without illumination. Fig. 5.1 shows the equivalent lumped element circuit of the experimental configuration. The equivalent load impedance can be written as:

$$Z_l = X + jY = C_p \parallel (C_d + R_d) = \frac{\frac{1}{j\omega C_p}\left(\frac{1}{j\omega C_d} + R_d\right)}{\frac{1}{j\omega C_p} + R_d + \frac{1}{j\omega C_d}}$$

$$= \frac{1 + j\omega R_d C_d}{R_d j\omega C_p j\omega C_d + j\omega C_d + j\omega C_p} \tag{5.1}$$

Since the frequency ω is on the order of 10^{10}, both detector and metal pad capacitance is on the order of 10^{14} and R_d is on the order of 10^2, we can simplify above equation by making some approximation,

$$Z_l = X + jY = \frac{R_d C_d}{C_p + C_d} - j\frac{1}{\omega(C_p + C_d)} \tag{5.2}$$

Where X and Y is on the order of 10^2 and 10^4, respectively. The reflection signal can be written as:

$$\Gamma = \frac{Z_l - R_l}{Z_l + R_l} = \frac{X + jY - R_l}{X + jY + R_l} = \frac{X^2 + Y^2 - R_l^2 + jY2R_l}{(X + R_l)^2 + Y^2} \tag{5.3}$$

Where R_l is the characteristic impedance of transmission line, which equal 50Ω in this experiment.

The arg of S_{11} can be expressed as:

$$arg(S_{11}) = arctan\left(\frac{2YR_l}{X^2+Y^2-R_l^2}\right) \approx \frac{2R_l}{Y} = -2\omega(C_p + C_d)R_l \qquad (5.4)$$

The capacitance of metal pads can be readily extracted from reference testing structures, which only include metal pad and trace line (see Fig. 5.2). Once we obtain the metal capacitance C_p, we can find the parasitic capacitance of detector.

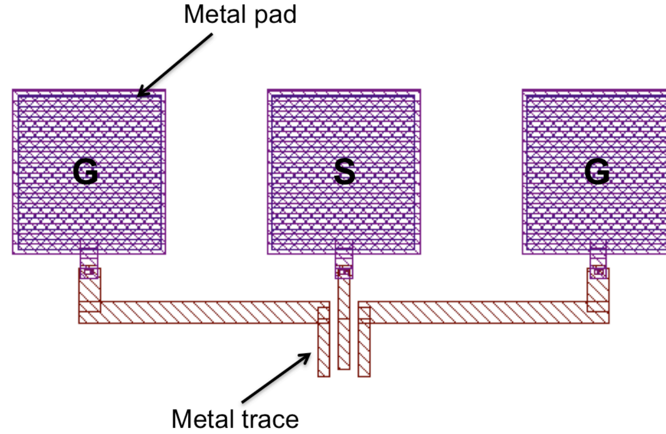

Figure 5.2 Reference testing structure for metal pad capacitance

5.3 Bandwidth measurement

The photodetector was probed with standard GSG RF probe with a characteristic impedance of 50Ω. A high-speed electro-optic modulator electrically driven by port 1 of the vector network analyzer (VNA) was placed in front of detector to modulate the optical signal, while the electrical output of photodetector was directed into port 2 of VNA. The 3 dB bandwidth of photodetector was determined from the S21 parameter of VNA. The standard set of RF calibrations was used before bandwidth measurement.

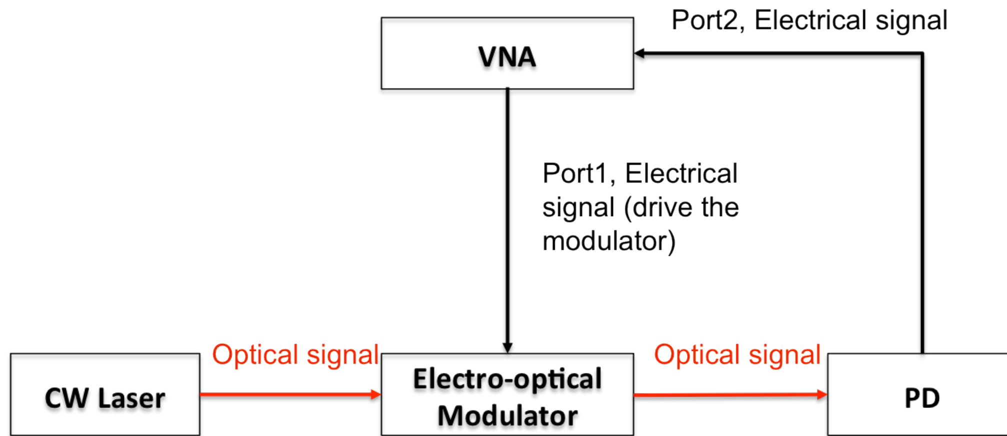

Figure 5.3 Experiment configuration for detector bandwidth measurement

5.4 Responsivity analysis

Cross-wafer data for responsivity

The cross-wafer responsivity data of 11 μm long detectors is shown in Fig. 5.4. Average on-chip responsivities of 0.54±0.05 A/W were achieved at 4V reverse-bias. Longer detectors were also measured and no big improvements in terms of responsivity were observed, which suggests that 11 μm long detector is enough to absorb incident light. The relatively low responsivity reveals that other source of loss may exist which degrades the responsivity.

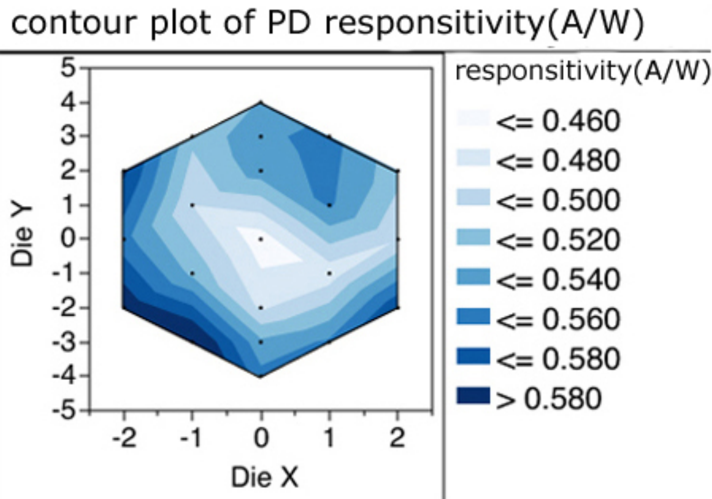

Figure 5.4 Cross-wafer data for Ge photodetector responsivity [17]

Sources of loss and methods for improvement

In order to fully understand the light absorption in Ge layers, we adopt 3D FDTD method [35] to simulate light propagation along the detector. In the following analysis the impact of metal contacts and doped Si/Ge are ignored for simplicity. Fig. 5.5 illustrates that the light is bounced up and down between Ge and Si layer along the direction of propagation, since multiple modes are excited within the Ge-on-Si structure and the difference in propagation constants of each mode leads to light interference along the detector. Since the generation rate of free carriers is proportional to light intensity, we could expect that the total absorption is not an exact exponential distribution due to the multi-modal nature. One needs to note that some modes exist with their main field components concentrated in Si substrate. As a result, a longer detector length is needed for light absorption for these modes. Therefore one needs to make sure that only a small amount of optical power couples into these modes. Fig. 5.6 shows the cross section view of the electric field

intensity, where light is well confined and only a tiny amount of power is scattered out of the Ge-on-Si structure.

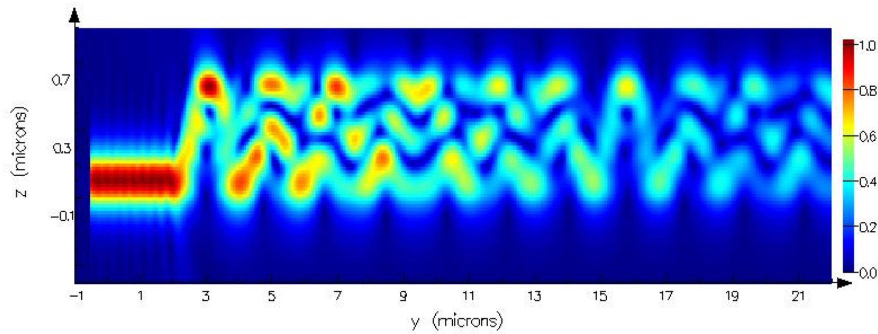

Figure 5.5 The lateral-section view of electric field intensity along the detector. The light bounces up and down within the Ge-on-Si structure.

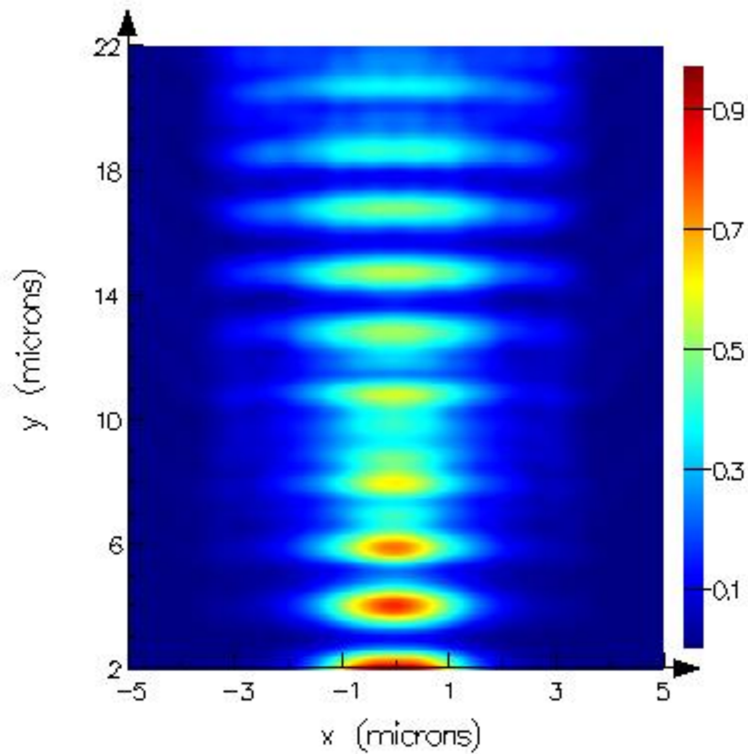

Figure 5.6 The cross-section view of electric field intensity along the detector.

Ideally, light would be evanescently coupled from substrate silicon into intrinsic Ge region and then generate free carriers without any additional loss. However, the reality is that light may be dissipated by many sources instead of contributing to photocurrent. First of all, the silicon waveguide is p-type doped to the order of 1e19 cm^{-3} to form the electrical path for free carrier extraction. This high doping introduces optical loss. The situation also applies to the n-type doped top Ge region. Moreover, metal on top of the Ge layer is also a highly absorptive part and may contribute the most to loss of responsivity.

Several solutions can be adopted to decrease the overlap between metal contacts and the optical mode, thus alleviating the impact of metal contact on detector responsivity: (1) one could move the metal contact from the center of top surface of the Ge layer to the sides so as to reduce the overlap between metal and optical mode [23]; (2) FDTD simulations show that for evanescent coupling, the optical mode is bounced up and down along the direction of propagation within detector. Another way to alleviate the problem is to use discrete metal contacts [36], placing these metal squares on the position where destructive interference occurs; (3) to increase the thickness of Ge film can also be beneficial for detector responsivity, since more optical power would concentrate within the Ge region; (4) to add a post-epitaxy thermal annealing step is able to improve the germanium quality and may improve the germanium absorption coefficient as well [33], which is equivalent to reducing the light dissipation from other sources.

5.5 Dark current analysis

Cross-wafer data for dark current

The cross-wafer average dark current was calibrated to be 4.8±0.4 μA for 11 μm long detectors at 4V reverse-bias. Fig. 5.7 shows the typical I-V sweep for detectors with different lengths. The dark current increases significantly once the applied reverse bias is larger than 4 V, where the avalanche process is triggered to amplify the leaking current.

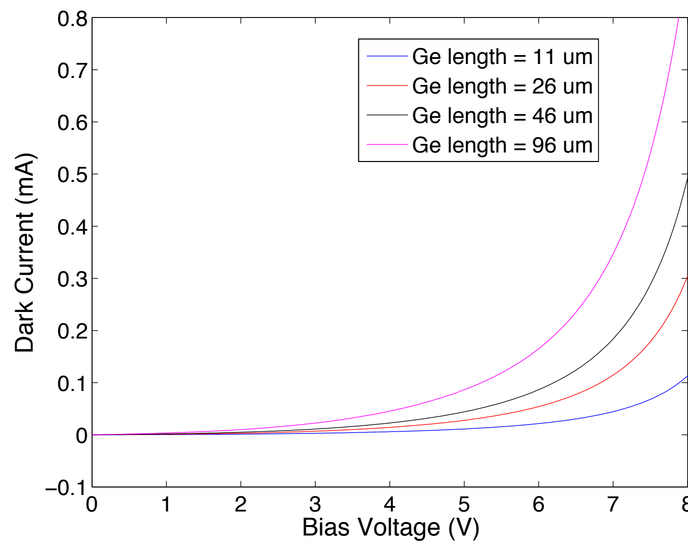

Figure 5.7 I-V curve of detectors without light illumination. Detectors with different Ge lengths were measured for comparison.

Also as we expected, Fig. 5.8 illustrates that the dark current is almost a linear function of detector length. Several 11 μm long detectors were tested and the average dark current is 4.8 μA with 4V reverse bias and 1.2 μA with 2V reverse bias, corresponding to dark current intensity of 5454 mA/cm^2 and 1363 mA/cm^2, respectively.

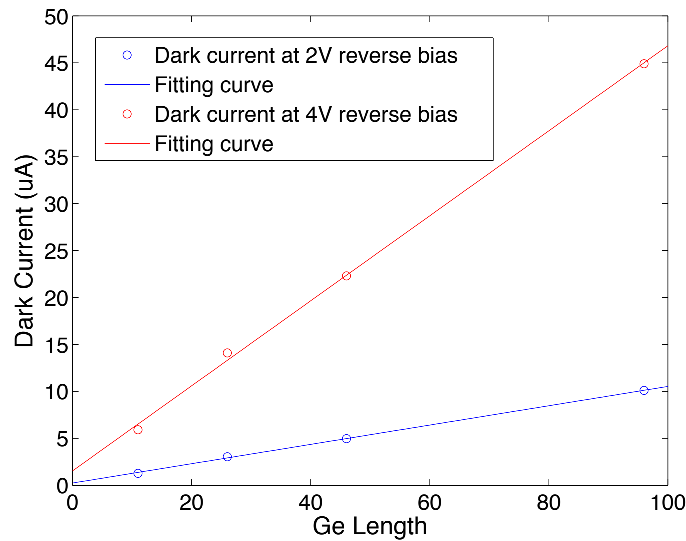

Figure 5.8 Dark current as a function of Ge length with 2V and 4V reverse-bias, respectively

Sources of dark current and methods for improvement

As discussed previously, the large number of defects within the depletion region function as recombination centers and are responsible for the dark current. For Ge-on-Si photodetectors, the primary source of defects is the threading dislocations due to the 4.2% lattice mismatch between Ge and Si. As a result, one would expect that the dark current should be almost a linear function of Ge area. Moreover, defects also exist at the interface between Ge and SiO_2 and surface generation at the sidewall would also aggravate the total dark current.

The measured dark current density is two orders of magnitude higher than what has been reported in literature [18,33] and suggests a poor quality of the Ge layer with a high defect concentration. This is attributed to the lack of a post-epitaxy thermal annealing step [33] that can reduce the defect concentration down one or two orders of magnitude.

The potential solutions for the high dark current density include: (1) to perform a low temperature thermal annealing step after the selective growth of Ge film, which has been demonstrated to be able to reduce the defects density of Ge down to 2.3×10^{6} cm^{-2} [21]. (2) one can also apply diffusion doping to the thin Ge buffer layer, which change the high defect density thin Ge layer to be part of quasi-neutral region of p-i-n diode, therefore reducing the leaking current under reverse bias. (3) improving the passivation of the sidewalls may further decrease dark current [23].

5.6 Bandwidth analysis

Cross-wafer data for bandwidth

The cross-wafer data for photodetector bandwidth is shown in Fig. 5.9. RF measurement shows that the average cross-wafer 3 dB bandwidths is 20.2±1.4 GHz with bias voltage of 4 V for 11 μm long detectors. We also examined device performance with small reverse bias. One device exhibits 3 dB bandwidth of 20 GHz with reverse bias voltage of 2V. The eye-pattern of a device working at 25 Gb/s is also shown in Fig. 5.10 (b).

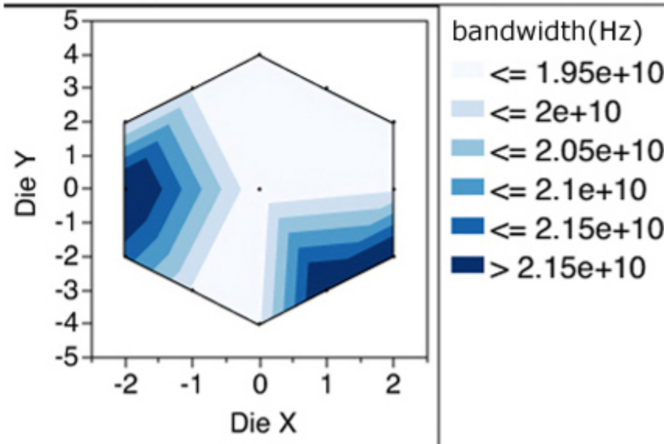

Figure 5.9 Cross-wafer data for Ge photodetector bandwidth [17]

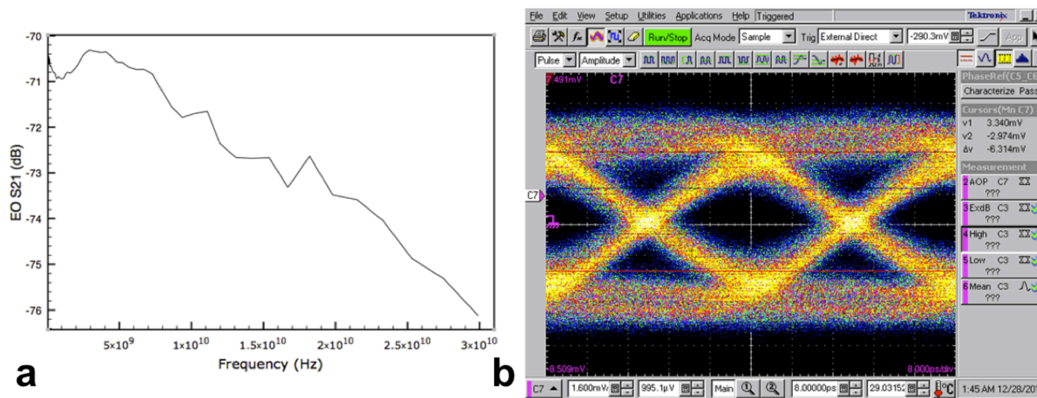

Figure 5.10 (a) the electro-optic S21 of a 11 µm long detector with 2 V reverse bias. (b) Eye-pattern at 25 Gb/s [17].

According to the formula to calculate transit time limited bandwidth, the ultimate bandwidth should be around 53 GHz for a detector with a depletion region of 500 nm. For our device the depletion region is even smaller than 500 nm (the measured detector

capacitance suggests that the depletion region is around 270 nm at 4 V reverse bias). As a result the conclusion can be drawn that the device speed is limited by RC charging time.

Detector capacitance

Fig 5.11 (a) illustrates the measured capacitance for a detector with a Ge dimension of 8 x 96 µm under a variety of reverse biases. The effective area (Ge with n++ type doped area) is 4 x 93.6 µm. Note that the detector capacitance decreases when increasing the bias voltage, and saturates when the applied bias voltage larger than 4V. When bias voltage is small, increasing the applied bias can expand the depletion region, and therefore decrease detector capacitance. This is the reason why larger reverse bias can improve detector bandwidth, where RC charging time is the speed limitation. Fig. 5.11 (b) shows the measured capacitance per unit length for two detectors with different lengths. The measured data is reasonably consistent; capacitance is around 2.1 fF/µm at 4V bias voltage.

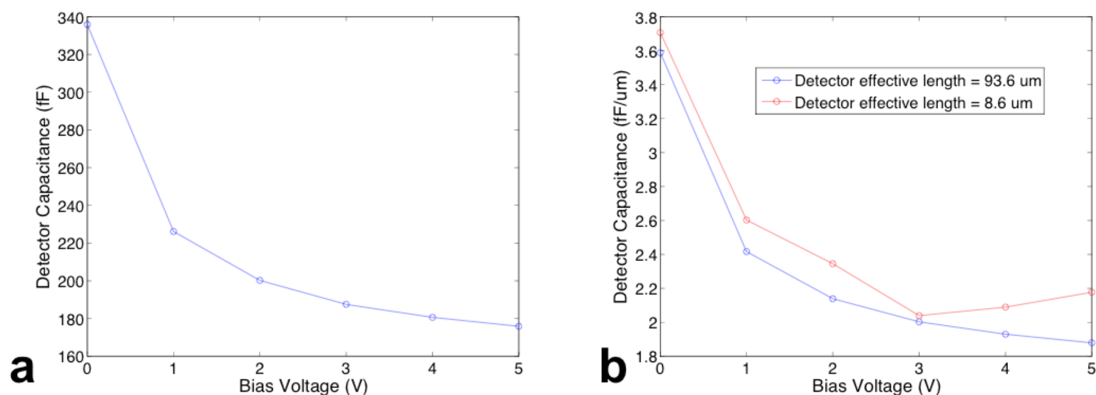

Figure 5.11 (a) measured capacitance for 100 µm long detector at different reverse bias; (b) measured capacitance per unit length for both 100 µm and 11 µm long detectors at different reverse-biases.

The capacitance attributed to 80 x 80 μm metal pads and traces was also measured to be 30.6 fF, which is even larger than the parasitic capacitance of the detector itself (for the short detector with effective length of 8.4 μm, the capacitance is 18 fF). For a detector working at higher speed (up to 70 GHz) the large capacitance due to metal pads would become a consideration.

Based on the parallel capacitor approximation we could calculate that the thickness of the depletion region is only 270 nm at bias voltage of 4V. The narrow depletion region of 270 nm at 4V bias implies that the dopant penetration depth is around 230 nm, deeper than we expected (as shown in Fig. 2.3). Hopefully better doping profiles can be achieved by optimizing doping techniques so that the dopant penetration depth is smaller than 150 nm. For example, one could tune the dopant energy and dose concentration to decrease the penetration depth. Another more complicated way is to use in-situ doping, since it occurs during the growth of Ge film, which enables more precise control of doping profile. The bottom line is that it is rational to expect higher bandwidth even with low working voltage, since wider depletion regions can reduce the detector capacitance effectively.

Detector resistance

From equation (3.13) we know that both parasitic resistance and capacitance of photodetectors determine the RC bandwidth so that the main approach to increase RC bandwidth is to come up with detectors design with small capacitance and resistance.

Sometimes it is more convenient and efficient to improve RC bandwidth by reducing detector resistance than capacitance, since the latter one is usually limited by other factors like responsivity and transit time bandwidth.

For vertical p-i-n detectors, parasitic resistance mainly comes from the quasi-neutral region of the p-i-n diode, where either n or p type doping is used to form the electrical path connecting the depletion region to the metal contacts. Detector resistance may also come from ohmic contact between the metal via and the heavily doped Si/Ge. Fortunately it is common to achieve contact resistance on the order to $10^{-6} \sim 10^{-7}$ Ω*cm^2 for CMOS processes, so it can be neglected in most cases.

From the basic knowledge on semiconductors we know that the resistance of a piece of material can be calculate as:

$$R = \frac{U}{I} = \frac{l}{nAe\mu} \tag{5.5}$$

l: resistor length;

A: resistor cross-section area;

e: electron charge;

μ: free carrier mobility;

n: free carrier concentration.

The above equation suggests that the Si substrate with moderate doping concentration dominates the total detector resistance due to lack of free carriers. Theoretically R can be readily reduced by heavily doping the Si substrate region to extremely high level, although carrier mobility may degrade slightly in heavier doping region. However, this

approach is problematic in practice since the Si substrate region would turn out to be highly absorptive for optical mode and a considerable amount of incident photons would be dissipated in this region so that device responsivity is degraded. In practice, a p+ doped Si substrate with doping concentration on the order of 1e19 cm^{-3} is used to extract electrical signal out of Ge depletion region, followed by a p++ doped Si region with doping concentration on the order of 1e21 cm^{-3} from where the optical mode is distant enough not to be disturbed.

The estimation of detector resistance is of great importance. It is essential for the prediction of a detector's RC bandwidth. In theory the detector resistance is predicable once we know relevant information about the material such as doping concentration, free carrier mobility as well as electric field distribution within the material. Unfortunately, some of the information cannot be obtained through simulations directly and comprehensive calibration work needs to be done in order to obtain reliable results. For example, the doping profile and carrier mobility are somewhat process-dependent and cannot be accurately predicted by simulation solely. Also, the electric field lines are actually curved instead of straight and uniformly distributed, which means one needs to discretize equation (5.5) when doing calculations in order to obtain accurate results. Here we perform the resistance simulation with Synopsys software as following: the structure (see Fig. 5. 12) is defined with Sprocess (which defines the structure through a virtual fabrication process) so that left side silicon is p+ doped, while the right side silicon is p++ doped. By adding two electrodes on both sides we are able to extract the silicon

resistance from the I-V curve in Sdevice [37]. However, more calibration work is needed to match simulation results and experiments.

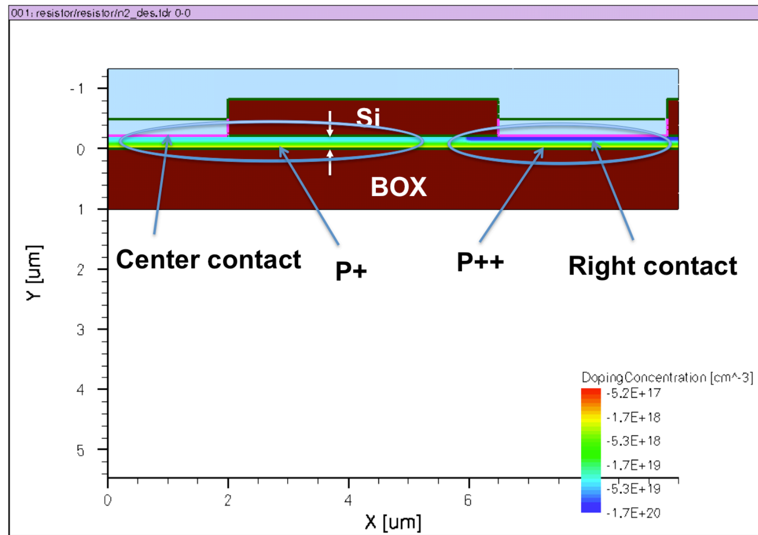

Figure 5.12 Sprocess doping concentration geometry for simulation of detector resistance

In addition an order of magnitude (OOM) calculation can also be done to estimate the upper bound of substrate resistance if the sheet resistance of doped Si is given. To be specific, we ignore the fringe effects that arise from curved electric fields at the two ends of the Si substrate (one end is the Ge/Si interface, the another is the interface of Si and metal via) and treat the Si substrate region as a regular bulk resistor. Then the resistance can be estimated with equation (5.5). These assumptions are plausible as long as the length of resistor is long enough so that edges of Si substrate are not the dominant part of resistance. The resistance can be calculated with following equation:

$$R_{bulk} = R_{sheet} * \frac{l}{w} \tag{5.6}$$

R_{sheet}: Sheet resistance of doped Si;

l: Length of resistor, which is the separation between Ge region and side metal contacts.

w : Width of resistor, which is the length of detector.

According to the lumped-element model of detector and the measured data for both detector bandwidth and pad capacitance, the detector resistance R_d is calculated to be 345Ω for the 11 μm long detectors, which is a fairly large value compared to the typical value reported in literature [23].

Many improvements can be made to the current design to reduce R_d significantly: (1) in the current design (Fig. 5.13), metal electrodes are placed 2 μm away from Ge edge to ensure little overlap with optical mode, which is over conservative of the potential absorption that electrodes may introduce, as FDTD simulation shows that optical mode is well confined within Ge region. One may reduce the separation to around 0.2 μm with the expectation of no degradation in responsivity at all; (2) one can further reduce the lateral length of the Si p+ region by shrinking the Ge width to a smaller value, depending on fabrication limitations. Additional improvement can be achieved by decreasing the edge distance between Ge n++ and Ge film.

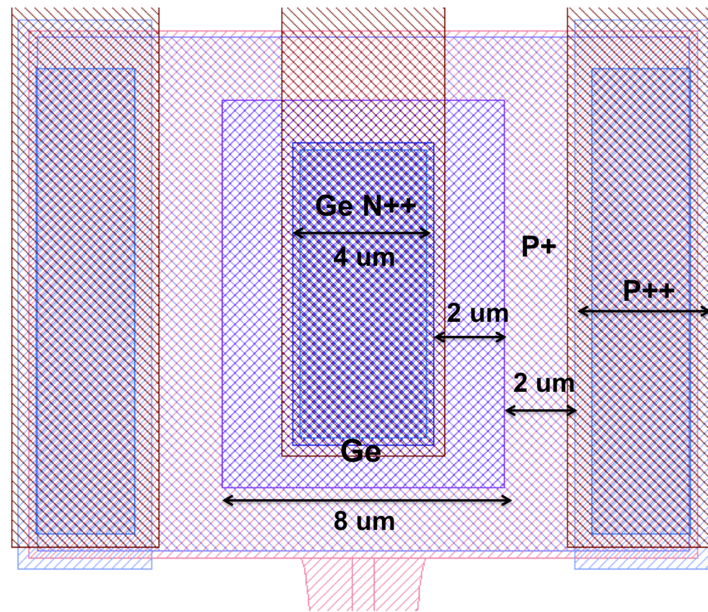

Figure 5.13 Vertical geometry of the 11 μm long detector.

Chapter 6 Proposed improved detector geometries

The previous discussion has shown that the limitation to current device bandwidth is the relatively large parasitic capacitance and resistance. Based on the model developed previously and measured data, I propose an improved detector design with more compact geometry, which is expected to improve the bandwidth up to 70 GHz and the responsivity close to 1 A/W in this process.

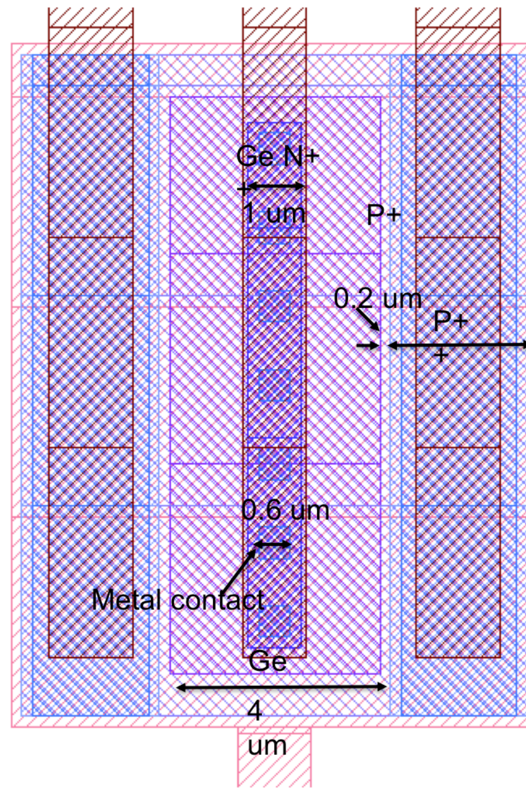

Figure 6.1 Proposed improved detector geometry.

In the new geometry (see Fig. 6.1), the width of Ge n++ region is reduced from 4 μm to 1 μm, while the length is kept the same. Based on the parasitic capacitor approximation and measured data, the detector capacitance is expected to decrease down to 1/4 of its original value, which is only 4.5 fF. The Si p++ doping region and metal contacts are only 0.2 μm away from the edge of Ge film to keep the size of the moderately doped Si substrate region as small as possible. By doing this, the simulated parasitic resistance can be reduced to smaller than 200Ω. In fact the decrease in the separation between the Ge film and Si n++/metal contact region will not degraded responsivity, since the optical mode is confined within Ge region tightly and the main portion of the optical power is absorbed in the first few microns of detector. Based on the lumped-element model of

photodetectors, the estimated RC bandwidth is as high as 106 GHz (metal pad capacitance of 20 fF is taken into account). The estimated depletion region of 270 nm corresponds to a transit time bandwidth of 98 GHz, which reveals that the actual device bandwidth is determined by both transit time bandwidth and RC bandwidth:

$$f_{3dB} = \frac{1}{\frac{1}{f_{tran}^2} + \frac{1}{f_{RC}^2}} \approx 70\ GHz \quad (6.1)$$

In terms of the responsivity, the discrete metal contacts on top of the Ge layer are adopted, being placed along the direction of light propagation periodically. As shown in Fig. 5.5, due to the multi-modal nature of light propagation in these detectors, it is possible to achieving small metal loss by locating metal squares at the position where the destructive interference occurs. Additionally, a post-epitaxy thermal annealing step has been demonstrated to improve Ge's quality and may also improve Ge's absorption coefficient. This can also reduce optical loss from other sources and improve detector responsivity. Detector responsivity around 1A/W is possible to achieve based on these modifications [33].

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