Characterization of Sneak Path Current Effect In a PEDOT: PSS-Based ReRAM Crossbar Array

Sri Vaishnavi Jamalapurapu

A thesis

submitted in partial fulfillment of the

requirements for the degree of

Master of Science in Electrical and Computer Engineering

University of Washington

2025

Committee:

Seungkeun Choi

Tadesse Ghirmai

Kaibao Nie

Program Authorized to Offer Degree:

Electrical and Computer Engineering

©Copyright 2025

Sri Vaishnavi Jamalapurapu

University of Washington

Abstract

Characterization of Sneak Path Current Effect in a PEDOT: PSS-Based ReRAM Crossbar Array

Sri Vaishnavi Jamalapurapu

Chair of the Supervisory Committee:

Seungkeun Choi

School of Science, Technology, Engineering & Mathematics

This thesis presents an experimental characterization of resistive switching memory crossbar devices fabricated on glass substrates with a structure of Cu/PEDOT: PSS/Ag, with a particular focus on understanding the impact of sneak-path currents on the switching performances. Resistive memory cells, particularly in crossbar configurations, are widely considered as promising memory technology due to their scalability, high density, non-volatility, and low power consumption. However, despite these advantages, they are prone to sneak-path currents—unintended leakage through unselected cells—which pose a significant challenge to performance and reliability in dense memory arrays.

In this work, I investigate how a ReRAM cell in a crossbar array responds to prolonged electrical stress by applying low-voltage cycling corresponding to a sneak-path conduction. The device has

a PEDOT:PSS as a switching layer sandwiched between Cu bottom electrode and Ag top electrode. The width of the electrodes is 10 µm and the crossbar array space is 60 µm. This research elaborates how a resistive switching memory cell in a crossbar array degrades its performance under various biasing conditions.

Three categories of electrical testing were conducted. First, cycling measurements under repeated ±2 V sweeps were used to assess endurance until hysteresis degradation. Devices showed stable switching behavior for up to 121 cycles, with well-defined LRS, HRS, and consistent Vset, Vreset values before breakdown. Second, voltage sweep experiments were designed to compare switching behaviors during an initial ±2 V sweep versus a final ±2 V sweep, following intermediate low-voltage steps from ±0.5 V to ±1.9 V. The results demonstrated that cumulative sneak-path conduction led to gradual hysteresis collapse and reduced switching margins. Finally, narrow-to-broad sweep testing evaluated whether limited low-voltage cycling could condition the device and influence future switching dynamics. Devices exposed only to narrow ranges remained non-switching, but subsequent full-range sweeps revealed altered I–V characteristics, confirming that sneak-path effects accumulate even in the absence of complete switching events.

Overall, the findings highlight that while selector-less resistive memory cells offer structural simplicity and potential scalability, their performance degrades under repeated low-voltage stress because of sneak-path current. This study provides experimental insights into how cumulative leakage conduction paths affect long-term device reliability, informing future strategies for robust ReRAM integration in compute-in-memory and neuromorphic architectures.

Table of Contents

ABSTRACT

ACKNOWLEDGEMENTS

Chapter 1. Introduction 1

1.1 State-of-the-art memory test 1

1.1.1 Static Random Access Memory (SRAM) 1

1.1.2 Dynamic Random Access Memory (DRAM) 2

1.1.3 Flash Memory 3

1.2 Volatile Vs Non-Volatile 4

1.3 Need for New Memory Technologies 5

1.4 Emerging Memory Technologies 6

Chapter 2. Resistive Random Access Memory (ReRAM) 11

2.1 History 11

2.2 Device Structure and Physical Mechanism 12

2.3 ReRAM Crossbar Arrays 13

2.3.1 Basic Unit Cell Structure 15

2.3.2 Array Configuration and Operation 15

2.3.3 3D Crossbar Arrays 16

2.3.4 Advantages of Crossbar-Based ReRAM Arrays 17

2.4 Traditional Fabrication & Characterization Techniques of Crossbar ReRAM 17

2.4.1 Fabrication Process Flow 18

2.4.2 Basic Operation Principle 19

2.4.3 Switching Modes in ReRAM 21

2.4.4 Practical Pulse-Based Operation in ReRAM Devices 24

2.4.5 Reading Current from a ReRAM Cell 30

2.5 Applications of ReRAM crossbar array 31

2.5.1 Neuromorphic Computing for Reinforcement Learning 32

2.5.2 In-Memory Computing for Edge AI and Image Processing 33

2.5.3 High-Performance Matrix–Vector Multiplication 33

2.5.4 Robust Deep Neural Network Inference 34

2.6 Sneak Path Currents of existing structure 35

CHAPTER 3: EXPERIMENTAL FABRICATION OF PROPOSED ReRAM DEVICES 39

3.1 Material Selection for ReRAM Devices 39

3.2 Fabrication Process 40

3.2.1 Bottom Electrode Fabrication 41

3.2.2: Switching Layer and Top Electrode Stack Definition 44

3.3 Optical Microscopy of Fabricated Devices 49

CHAPTER 4: ELECTRICAL CHARACTERIZATION AND MATHEMATICAL MODELS 52

4.1Testing Setup 52

4.2 Cycling Tests 53

4.2.1 Hysteresis Loops 54

4.2.2 Endurance 61

4.3 Characterization of Sneak Path Current Behavior through hysteresis 66

4.4 Effect of Step-Sweep Conditioning on Full ±2 V Switching Characteristics 73

4.4.1 Objective 73

4.4.2 Methodology 73

4.4.3 Results 82

4.5 Mathematical Modeling of Sneak Path Influence via Current Density Analysis 84

4.5.1 Motivation and Design Tradeoff 85

4.5.2 Theoretical Calculation of Current Density 86

4.5.3 Experimental Current Density Calculation 90

4.5.4 Voltage-Dependent Resistivity in Sneak-Path Modeling 92

5. CONCLUSION 94

References 97

List of Figures

Figure 1.1 Conventional 6T-SRAM cell with: pull up (PU), pull down (PD) and pass gate (PG) transistors [1] 1

Figure 1.2 Memory structure of a one-transistor one-capacitor (1T1C) DRAM array[2] 2

Figure 1.3 3D NAND Flash Memory 3

Figure 1.4 Illustration of the Von Neumann bottleneck 6

Figure 1.5 Basic structure of a resistive memory (ReRAM) cell 7

Figure 1.6 Cell structure of phase-change memory. 8

Figure 1.7 MJT cell for STT-MRAM. 3D structure of an MRAM cell based on a Magnetic Tunnel Junction (MTJ). 9

Figure 1.8 Structure of a Ferroelectric Field-Effect Transistor (FeFET). 10

Figure 2.1 ReRAM Memory Device Structure 13

Figure 2.2 Schematic of a ReRAM crossbar array showing intersecting wordlines and bitlines with resistive switching elements at each node 14

Figure 2.3: Crossbar array architecture for RRAM-based in-memory computing 16

Figure 2.4 Traditional Fabrication Process 19

Figure 2.5 Resistive switching mechanism in a metal–insulator–metal (MIM) ReRAM structure. 21

Figure 2.6 (a) Unipolar Switching b) Bipolar Switching 22

Figure 2.7 (a) Bipolar Switching Pulse Pattern (b) Typical hysteretic bipolar current–voltage (I– V) characteristics in metal– insulator–metal (MIM) structures. 26

Figure 2.8 (a) Unipolar Switching Pulse Pattern (b) Typical hysteretic unipolar current–voltage (I– V) characteristics in metal– insulator–metal (MIM) structures. 27

Figure 2.9 Pulse Calibration and Filament Dynamics in ReRAM Devices 28

Figure 2.10 Illustration of sneak-path current in a crossbar memory array. 36

Figure 2.11 Schematic of a 1T1R (one-transistor–one-resistor) ReRAM cell for sneak-path suppression[41]. 38

Figure 3.1: Substrates cleaned with piranha 41

Figure 3.2 (a): Spin coated NR9-1500PY resist 3000rpm for 30sec 42

Figure 3.2 (b): PR Spin coated glass substrate 42

Figure 3.3 (a): UV Lithography 43

Figure 3.3 (b): Developed PR 43

Figure 3.4: Thermally Evaporating Bottom Electrode Layer 44

Figure 3.5: After liftoff Bottom Electrode Silver 45

Figure 3.6: Spin coated NR9-1500PY resist 3000rpm for 30sec 45

Figure 3.7: PR Spin coated glass substrate 46

Figure 3.8 (a): UV Lithography 46

Figure 3.8 (b): Developed PR 47

Figure 3.9(a): Spin coat PEDOT: PSS at 1000rpm for 30sec 47

Figure 3.9 (b): Spin coated PEDOT: PSS 47

Figure 3.10: Thermally evaporated Cu 48

Figure 3.11: After liftoff ReRAM 48

Figure 3.12: ReRAM Array with coarse X coarse pattern with the width of bottom electrodes, switching layer and top electrodes as 10um and distance between the layers as $60\mu m$ 49

Figure 3.13: Optical Microscope of the bottom Ag Electrodes 50

Figure 3.14 (a): Edge1 of the crossbar array 50

Figure 3.14 (b): Edge2 of the crossbar array 50

Figure 3.15: Crossbar Array with the structure: Top Electrode Copper (Cu), Resistive Switching Layer is PEDOT: PSS, Bottom Electrode Layer Silver (Ag) 51

Figure 3.16: The visible grey extensions beyond the edges of the copper lines confirm that the switching layer (PEDOT: PSS) was selectively patterned only beneath the top electrodes 51

Figure 4.1 Testing setup 53

Figure 4.2 (a): I-V Characteristics of cell #1 Cycle 18 54

Figure 4.2 (b): ReRAM cell #1 for 104 Cycles 55

Figure 4.3 (a): I-V Characteristics of Cell #2 55

Figure 4.3 (b): ReRAM cell #2 for 113 Cycles 56

Figure 4.4 (a): I-V Characteristics of Cell #3 57

Figure 4.4 (b): ReRAM Cell #3 for 78 Cycles 57

Figure 4.5 (a): I-V Characteristics of Cell #4 58

Figure 4.5 (b): ReRAM Cell #4 for 63 Cycles 58

Figure 4.6 (a): I-V Characteristics of Cell #5 59

Figure 4.6 (b): ReRAM Cell #5 for 121 Cycles 60

Figure 4.7 (a): LRS, HRS Endurance of 104 Cycles 61

Figure 4.7 (b): Average set and reset voltages across 104 Cycles 62

Figure 4.8 (a): LRS, HRS Endurance of 113 Cycles 62

Figure 4.8 (b): Average set and reset voltages across 113 Cycles 63

Figure 4.9 (a): LRS, HRS Endurance of 78 Cycles 63

Figure 4.9 (b): Average set and reset voltages across 78 Cycles 64

Figure 4.10 (a): LRS, HRS Endurance of 63 Cycles 64

Figure 4.10 (b): Average set and reset voltages across 63 Cycles 65

Figure 4.11 (a): LRS, HRS Endurance of 121 Cycles 65

Figure 4.11 (b): Average set and reset voltages across 121 Cycles 66

Figure 4.12: Overlay of I–V Characteristics Across Voltage Sweeps 67

Figure 4.13 (a)-(o) I–V curves from **±0.5 V** to **±1.9 V** (one figure per voltage step), (p) First full ±2 V sweep (before low sweeps), (q) Second full ±2 V sweep (after low sweeps) 68

Figure 4.14 Hysteresis I-V loop comparison of first full ±2 V sweep (before low sweeps), second full ±2 V sweep (after low sweeps). 71

Figure 4.15 *(Left)* First full ±2 V sweep establishing baseline switching. *(Middle)* Narrow ±0.5 V sweep showing purely ohmic behavior with no resistive switching. *(Right)* Second full ±2 V sweep after low-voltage 74

cycling, showing minimal change in hysteresis compared to the initial sweep.

Figure 4.16 *(Left)* First full ±2 V sweep establishing baseline switching. *(Middle)* Narrow ±0.6 V sweep showing linear, ohmic behavior without resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling, indicating minimal change in hysteresis compared to the initial sweep. 75

Figure 4.17 *(Left)* First full ±2 V sweep demonstrating baseline switching characteristics. *(Middle)* Narrow ±0.7 V sweep showing ohmic conduction without evidence of switching. *(Right)* Second full ±2 V sweep after low-voltage cycling, indicating only minor variations in hysteresis relative to the first sweep. 75

Figure 4.18 *(Left)* First full ±2 V sweep showing baseline switching characteristics. *(Middle)* Narrow ±0.8 V sweep exhibiting a linear, ohmic response with no evidence of resistive switching. *(Right)* Second full ±2 V sweep following low voltage cycling, showing minimal change in hysteresis compared to the initial sweep 76

Figure 4.19 *(Left)* First full ±2 V sweep showing baseline switching. *(Middle)* Narrow ±0.9 V sweep with a purely ohmic I–V response, indicating no resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling, showing minimal change in hysteresis relative to the initial sweep. 76

Figure 4.20 *(Left)* First full ±2 V sweep showing baseline switching behavior. *(Middle)* Narrow ±1.0 V sweep displaying a linear, ohmic I–V response without resistive switching. *(Right)* Second full ±2 V sweep after low voltage cycling, showing minimal variation in hysteresis compared to the initial sweep. 77

Figure 4.21 (Left) First full ±2 V sweep showing the baseline switching curve. *(Middle)* Narrow ±1.1 V sweep producing an ohmic response with no indication of resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling, revealing minimal change in hysteresis compared to the initial sweep. 77

Figure 4.22 (Left) First full ±2 V sweep showing baseline switching. (Middle) Narrow ±1.2 V sweep exhibiting an almost linear I–V response with minimal switching features. (Right) Second full ±2 V sweep after low-voltage cycling, indicating little to no change in hysteresis relative to the initial sweep. 78

Figure 4.23 (Left) First full ±2 V sweep establishing baseline switching. (Middle) Narrow ±1.3 V sweep showing a predominantly ohmic I–V profile with minimal switching signatures. (Right) Second full ±2 V sweep after low-voltage cycling, displaying negligible change in hysteresis compared to the initial sweep. 78

Figure 4.24 (Left) First full ±2 V sweep showing the baseline switching response. (Middle) Narrow ±1.4 V sweep producing a linear I–V curve indicative of ohmic conduction with no resistive switching. (Right) Second 79

full ±2 V sweep after low-voltage cycling, revealing minimal change in hysteresis relative to the initial sweep.

Figure 4.25 (Left) First full ±2 V sweep showing baseline switching characteristics. (Middle) Narrow ±1.5 V sweep with a predominantly linear I–V response, indicating minimal resistive switching. (Right) Second full ±2 V sweep after low-voltage cycling, showing negligible change in hysteresis compared to the initial sweep. 79

Figure 4.26 (Left) First full ±2 V sweep showing baseline switching response. (Middle) Narrow ±1.6 V sweep producing a mostly linear I–V curve, indicating limited resistive switching activity. (Right) Second full ±2 V sweep after low-voltage cycling, revealing minimal change in hysteresis compared to the initial sweep. 80

Figure 4.27 (Left) First full ±2 V sweep showing baseline switching characteristics. (Middle) Narrow ±1.7 V sweep with a near-linear I–V curve, indicating minimal resistive switching.(Right) Second full ±2 V sweep after low-voltage cycling, showing negligible change in hysteresis compared to the initial sweep. 80

Figure 4.28(Left) First full ±2 V sweep showing the baseline switching curve. (Middle) Narrow ±1.8 V sweep producing a mostly linear I–V response with minimal switching. (Right) Second full ±2 V sweep after low-voltage cycling, revealing little to no change in hysteresis relative to the initial sweep. 81

Figure 4. 29 (Left) First full ±2 V sweep showing baseline switching characteristics. (Middle) Narrow ±1.9 V sweep displaying a mostly linear I–V curve with minimal signs of resistive switching. (Right) Second full ±2 V sweep after low-voltage cycling, showing negligible change in hysteresis compared to the initial sweep. 81

Figure 4.30 Slope based LRS and HRS across 17 consecutives ±2 V sweeps. 83

Figure 4.31 Variation of HRS/LRS ratio across 17 consecutive ±2 V sweeps. 83

Figure 4.32 Comparison of LRS and HRS values between the first and second ±2.0 V sweeps 84

Figure 4.33 Schematic of a crossbar ReRAM array with electrical probing setup 88

Figure 4.34 Schematic representation of sneak-path current in a ReRAM crossbar array cell. 89

Figure 4.35 Current Density vs. Spacing (V = 1.1 V) (Left). *Current Density vs. Voltage (d = 60 µm) (Right).* 91

Figure 4.36 shows the modeled resistivity vs. voltage curve for ρ_0=1.0 (arb. units) and k=1.5 V^{-1}. 93

List of Tables

Table 1.1: Feature Comparisons of SRAM, DRAM, Flash and ReRAM 4

Table 3.1 Advantages of the material stack 40

Table 4.1: Summary of Cycling Test 60

Table 4.2 LRS, HRS, ILRS, IHRS, and Voltage Range 72

Tables 4.3 Experimental Current Density J_{sneak} 91

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my advisor, Dr. Seungkeun Choi, for his invaluable guidance, encouragement, and insightful feedback throughout the course of my thesis. His expertise and support have been instrumental in shaping the direction and quality of my work. I would also like to extend thanks to Dr Tadesse Ghirmai, and Dr Kaibao Nie from the research committee for accepting my invitation

I am sincerely thankful to my family for their unconditional love, patience, and encouragement, which have been a constant source of strength. I also extend my heartfelt appreciation to my friends, whose understanding, motivation, and support have helped me navigate the challenges of this journey.

This thesis would not have been possible without the collective support and belief of these remarkable individuals.

1. INTRODUCTION

1.1 State-of-the-Art Memory Technologies

Modern digital systems rely on a hierarchy of memory technologies to balance speed, density, power consumption, and cost. Among the most widely used are Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM), and Flash memory. These technologies each serve specific roles in computing—from processor caches to main memory and mass storage.

1.1.1 Static Random Access Memory (SRAM)

SRAM uses six transistors per bit cell to store binary information in a latch configuration. Its design allows for extremely fast read and write access, making it ideal for cache memory in CPUs and GPUs. However, its large cell size (~100 F^2, where F is the feature size) limits its scalability and density, resulting in higher cost per bit. Furthermore, SRAM is volatile, requiring continuous power to retain data, and it consumes significant static power due to leakage currents [1].

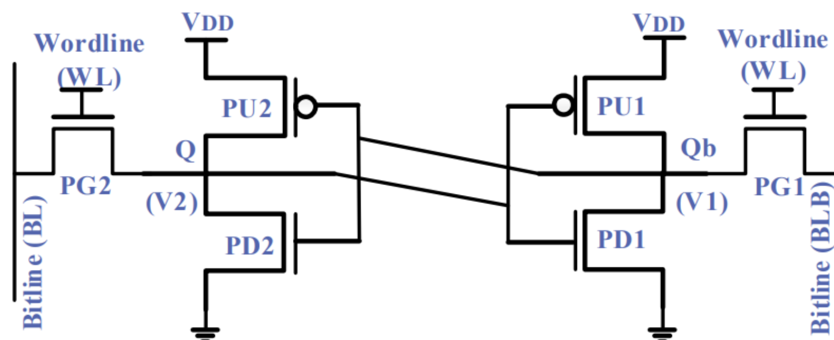


Figure 1.1 Conventional 6T-SRAM cell with: pull up (PU), pull down (PD) and pass gate (PG) transistors [1].

1.1.2 Dynamic Random Access Memory (DRAM)

DRAM stores data in a capacitor-transistor pair, with each bit represented by the presence or absence of charge in the capacitor. This design enables a smaller footprint (~6 F^2 per cell), offering higher density and lower cost compared to SRAM. DRAM serves as the primary working memory in most computing systems due to its moderate access speeds and scalability.

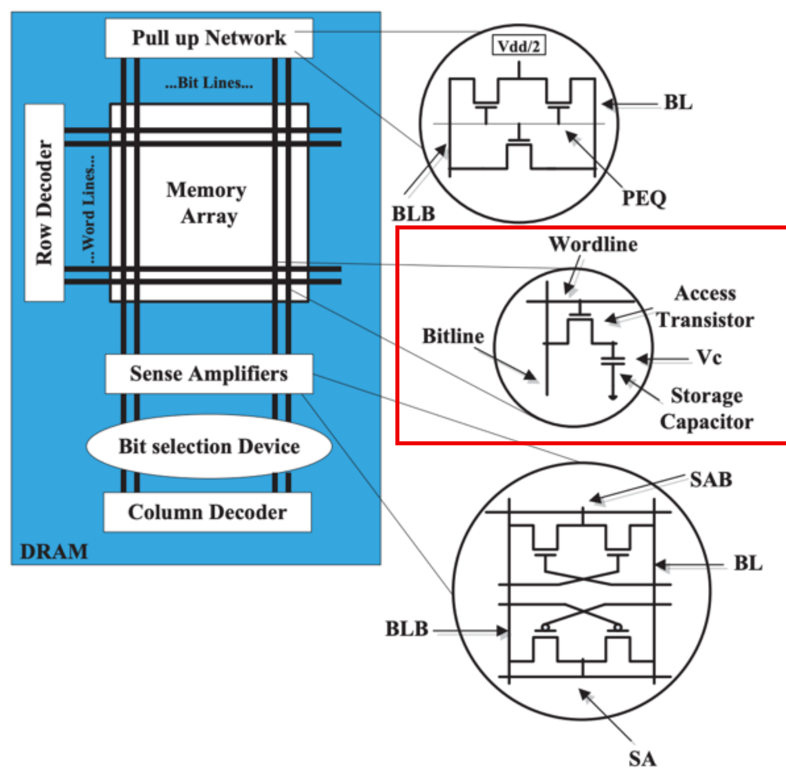


Figure 1.2 Memory structure of a one-transistor one-capacitor (1T1C) DRAM array[2].

However, the stored charge leaks over time, necessitating periodic refresh operations that increase energy consumption and reduce performance. Moreover, as device geometries shrink, maintaining sufficient capacitance becomes increasingly difficult, presenting a significant scaling challenge.

1.1.3 Flash Memory

Flash memory, particularly NAND Flash, is a widely adopted non-volatile storage medium used in solid-state drives, memory cards, and embedded systems. It operates by trapping charge in a floating gate or charge-trap layer within a transistor, allowing it to retain data without power. Flash excels in storage density and cost per bit, but its drawbacks include limited write endurance (typically 10^4–10^5 program/erase cycles), slow write/erase speeds, and high programming voltages [3]. Despite its ubiquity, flash technology faces increasing challenges in scaling, reliability, and write performance, particularly in data-intensive applications.

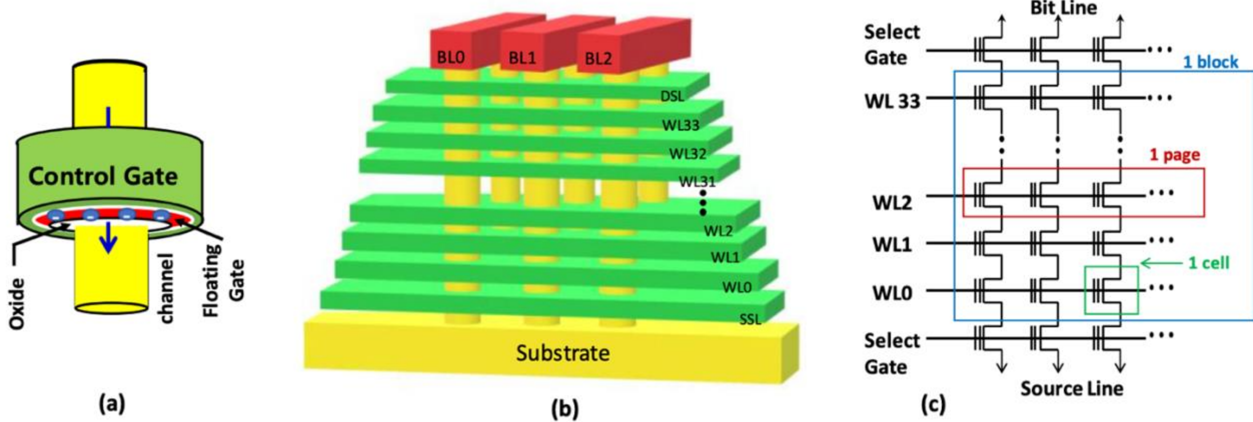


Figure 1.3 3D NAND Flash Memory: (a) 3D flash memory cell; (b) physical structure of a 3D NAND flash array; (c) transistor-level schematic of a NAND flash memory block, which consists of 34 pages in this example[4]

1.2 Volatile vs Non-Volatile Memory

The essential difference between volatile and non-volatile memory lies in data retention behavior after power-off. Volatile memories, such as SRAM and DRAM, lose their contents once power is removed. Non-volatile memories, such as Flash and emerging resistive memories, retain data without the need for continuous power [5], [6].

Table 1.1: Feature Comparisons of SRAM, DRAM, Flash and ReRAM

Feature	SRAM	DRAM	Flash	ReRAM
Type	Volatile	Volatile	Non-volatile	Non-volatile
Cell Size	Large	Medium	Small	Very Small
Speed	Very Fast	Fast	Slow	Fast
Power Efficiency	High Leakage	Refresh Cost	Efficient	Very Efficient
Endurance	High	Moderate	Low	High
Scalability	Low/	Moderate	High	High

Volatile memory excels in speed and is ideal for temporary storage and computation. However, it suffers from high standby power and volatility. DRAM, though denser than SRAM, is energy-inefficient due to refresh cycles.

Non-volatile memory technologies, led by Flash, provide persistent storage with no energy requirement for retention. But they are constrained by endurance limits and slower access times.

This performance gap between volatile and non-volatile memory has led to a fundamental bottleneck in computing, particularly under modern demands of energy efficiency and AI/edge computing workloads.[6]

1.3 The Need for New Memory Technologies

As computational systems evolve, conventional memory technologies are increasingly unable to meet the performance, endurance, and efficiency demands of modern applications. The following limitations have become apparent:

- **SRAM**: Not scalable beyond certain limits due to large cell size and leakage.
- **DRAM**: Energy-inefficient due to refresh requirements and faces fundamental scaling limits.
- **Flash**: Limited writing endurance and high program voltages restrict its use in high-write environments.

Additionally, the separation between memory and processing units in traditional Von Neumann architecture leads to excessive data movement, known as the **Von Neumann bottleneck** [7]. This is particularly problematic in AI and machine learning workloads, where large volumes of data must be repeatedly fetched and processed.

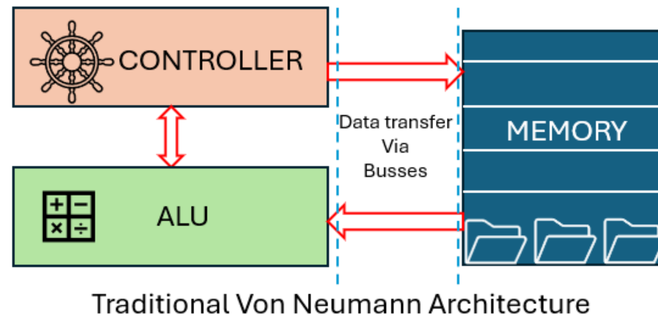


Figure 1.4 Illustration of the Von Neumann bottleneck. The architecture separates the processing unit (comprising the controller and arithmetic logic unit, ALU) from memory, requiring data to be transferred back and forth via shared buses. This separation creates a performance bottleneck known as the Von Neumann bottleneck, due to limited bus bandwidth and speed mismatch between computation and memory access.

To address these challenges, new memory technologies must:

- Be non-volatile.
- Offer low power, fast read/write access.
- Scale well with advanced fabrication nodes.
- Integrate seamlessly with logic circuitry.
- Support endurance levels sufficient for frequent updates.

1.4 Emerging memory technologies

Candidates such as Resistive Random Access Memory (ReRAM), Phase-Change Memory (PCM), and Magnetoresistive RAM (MRAM) are being investigated as potential replacements or supplements to existing technologies [8]. Among them, ReRAM stands out due to its simple

structure, scalability, fast operation, and low power consumption. It promises to bridge the gap between volatile and non-volatile performance, offering a path toward unified memory architectures.

Resistive Random Access Memory (ReRAM)

ReRAM stores data by changing the resistance of a metal–insulator–metal (MIM) structure through the formation and rupture of conductive filaments, typically driven by voltage-induced ion migration. It offers high speed, low power, simple 3D integration, and strong scalability. ReRAM is attractive for neuromorphic and in-memory computing due to its analog switching and multi-level storage capabilities. However, it suffers from variability in switching thresholds and endurance limitations depending on material systems [8].

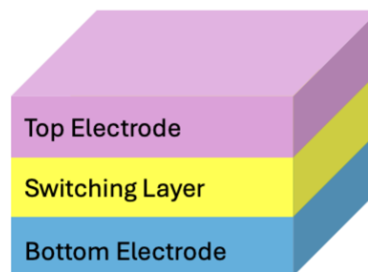


Figure 1.5 Basic structure of a resistive memory (ReRAM) cell. The device consists of a top electrode, a resistive switching layer, and a bottom electrode. The switching layer modulates resistance between a high-resistance state (HRS) and a low-resistance state (LRS) through the formation and rupture of conductive filaments.

Phase-Change Memory (PCM)

PCM exploits the resistivity difference between amorphous and crystalline states in chalcogenide materials (e.g., GeSbTe). It allows non-volatile storage with fast read access and moderate write speeds. PCM offers multi-bit capability, high scalability, and long retention times. The main challenges include high programming energy and material degradation over cycling, which affect endurance [8].

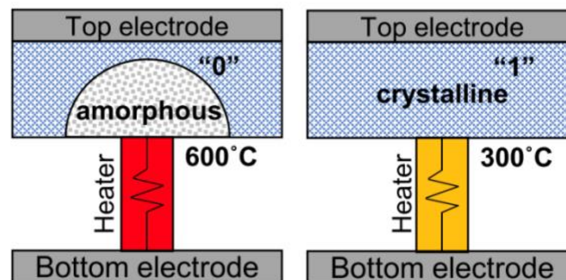


Figure 1.6 Cell structure of phase-change memory. (Left) amorphous state, (Right) crystalline state. Operating principle of a Phase-Change Memory (PCM) cell. A high-temperature pulse (~600 °C) causes the phase-change material to become **amorphous**, representing logic '0', while a moderate pulse (~300 °C) allows it to crystallize, storing logic '1'. Phase transitions are induced using a heater element between the bottom and top electrodes[9].

Magnetoresistive RAM (MRAM)

MRAM stores data using magnetic tunnel junctions (MTJs), where information is encoded by the relative magnetization direction of two ferromagnetic layers. It provides non-volatility, fast speed, virtually infinite endurance, and CMOS compatibility. Two main variants exist: toggle MRAM

and spin-transfer torque (STT) MRAM. While MRAM excels in endurance and speed, its density and write energy remain challenges for large-scale adoption [7].

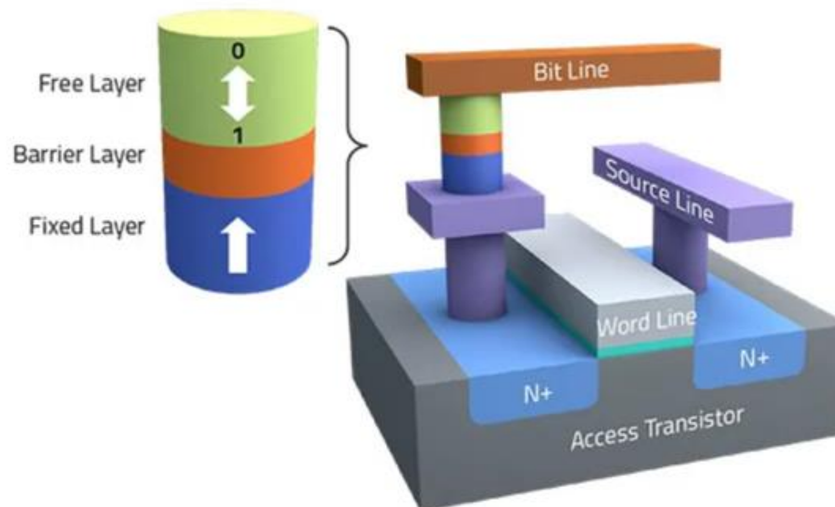


Figure 1.7 MJT cell for STT-MRAM. 3D structure of an MRAM cell based on a Magnetic Tunnel Junction (MTJ). The MTJ stack consists of a free layer, barrier layer, and fixed layer, where data is stored as resistance states based on magnetic alignment. Access is enabled via word, bit, and source lines with an underlying access transistor [10].

Ferroelectric RAM (FeRAM)

FeRAM relies on the polarization states of a ferroelectric capacitor (usually based on PZT or doped HfO_2) to store data. It combines the speed and low power of DRAM with non-volatility. FeRAM is radiation-hard and suitable for low-power embedded applications. However, it faces scaling limitations and lower density compared to Flash or ReRAM, which restrict broader adoption [7].

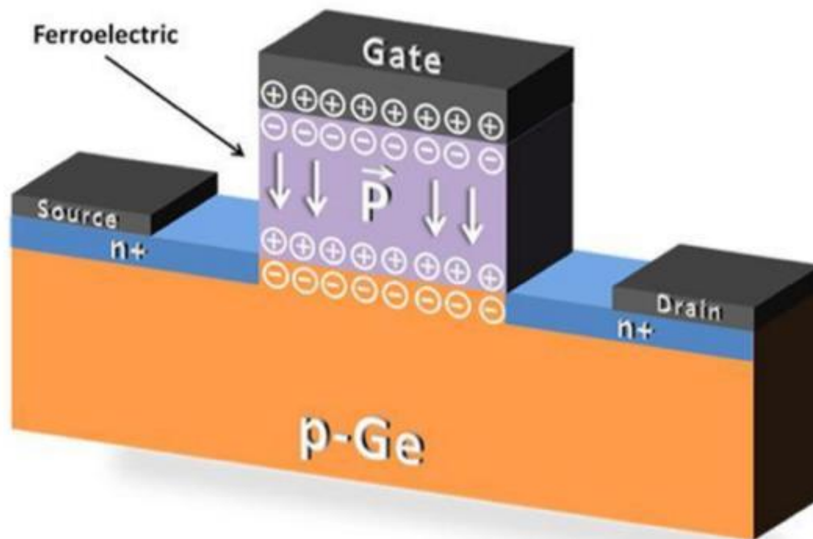


Figure 1.8 Structure of a Ferroelectric Field-Effect Transistor (FeFET). The device incorporates a ferroelectric layer in the gate stack, enabling non-volatile polarization states (P↑ or P↓) that modulate the channel conductivity. The source and drain regions are n^+ doped, while the substrate is p-type germanium (p-Ge), allowing charge control via ferroelectric polarization.[11]

CHAPTER 2: RESISTIVE RANDOM ACCESS MEMORY (ReRAM)

2.1 History

The development of Resistive Random-Access Memory (ReRAM) began in 1962, when Hickmott first observed resistive switching phenomena in metal oxides. This discovery initiated extensive research during the 1960s into various insulating materials—including Al_2O_3, NiO, SiO_2, Ta_2O_5, ZrO_2, TiO_2, and Nb_2O_5—for their suitability in resistive switching applications.

In 2000, researchers at the University of Houston reported resistive switching behavior in magneto resistive thin films, marking a significant step toward device-level realization. By 2002, Zhuang and colleagues successfully fabricated a 64-bit ReRAM array using a 0.5 µm CMOS process, demonstrating its compatibility with conventional semiconductor manufacturing technologies [12].

The following years saw growing industry interest. Notable early milestones included Samsung's development of binary transition-metal-oxide-based ReRAM, NEC's fabrication of a 1 kB test chip, and Infineon's demonstration of a 2 MB conductive-bridging RAM (CBRAM) device. A pivotal moment came in 2008 with the publication of "The Missing Memristor Found" by HP Labs, which connected theoretical memristor models to practical resistive switching devices, reinforcing ReRAM's potential for logic-in-memory and neuromorphic computing architectures [12].

From 2010 onwards, ReRAM commercialization accelerated. Unity Semiconductor developed a 64 MB ReRAM chip, while Stanford and Macronix introduced 3D vertical ReRAM structures between 2012 and 2013. In 2013, SanDisk and Toshiba announced a 32 Gbit bilayer ReRAM array, and Micron and Sony unveiled a 27 nm, 16 Gbit Cu-based CBRAM device in 2014. IMECAS advanced the technology further in 2016 with a four-layer 3D vertical ReRAM stack [13].

In 2017, TSMC announced its roadmap for embedded ReRAM in 22 nm technology nodes, targeting applications in low-power and high-performance computing. Since then, companies like Intel, Samsung, and TSMC have continued to explore embedded ReRAM for AI accelerators and edge devices. Notably, in 2021, Weebit Nano introduced a commercially viable embedded ReRAM solution, and TSMC demonstrated a 16 nm ReRAM device with improved endurance and reliability metrics[14].

ReRAM's evolution reflects its growing importance as a candidate for next-generation non-volatile memory, offering high density, low power consumption, and intrinsic suitability for neuromorphic and in-memory computing paradigms.

2.2 Device Structure and Physical Mechanism

A single ReRAM cell comprises three primary components: a top electrode (TE), a bottom electrode (BE), and a resistive switching layer (RSL) positioned between them. This configuration forms a metal–insulator–metal (MIM) structure, which is known for its simplicity, scalability, and compatibility with CMOS integration. While transition metal oxides such as HfO_2, TiO_2, and Ta_2O_5 are commonly used as the switching material, various other material systems—including

perovskites, chalcogenides, two-dimensional materials, and organic compounds—have also been investigated to achieve diverse switching behaviors and device functionalities.

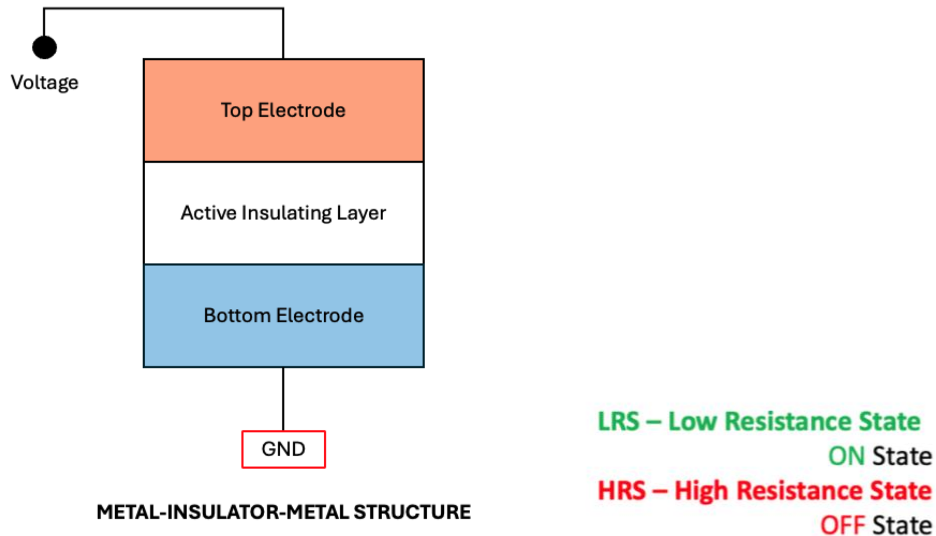


Figure 2.1 ReRAM Memory Device Structure. Schematic of a Metal–Insulator–Metal (MIM) structure. The stack comprises a top electrode, an active insulating (dielectric or switching) layer, and a bottom electrode. When a voltage is applied across the electrodes, the insulator modulates current flow, enabling its use in resistive switching devices such as ReRAM.

2.3 ReRAM Crossbar Arrays

The **ReRAM crossbar array** is a fundamental architecture enabling ultra-high-density non-volatile memory and emerging in-memory and neuromorphic computing paradigms. It's simple yet powerful layout consists of intersecting horizontal and vertical metal lines, with a ReRAM cell located at each cross-point. This architecture is prized for eliminating the need for individual access transistors, thus maximizing areal density and scalability.

Crossbar Array Architecture

The crossbar structure is composed of two perpendicular layers of conductive lines:

- **Wordlines (WLs):** Horizontal lines typically connected to the top electrodes (TE)**.**
- **Bitlines (BLs):** Vertical lines connected to the bottom electrodes (BE)**.**

At each intersection of a WL and BL lies a single ReRAM device. The resistive switching layer is sandwiched between the electrodes, forming a metal–insulator–metal (MIM) cell structure.

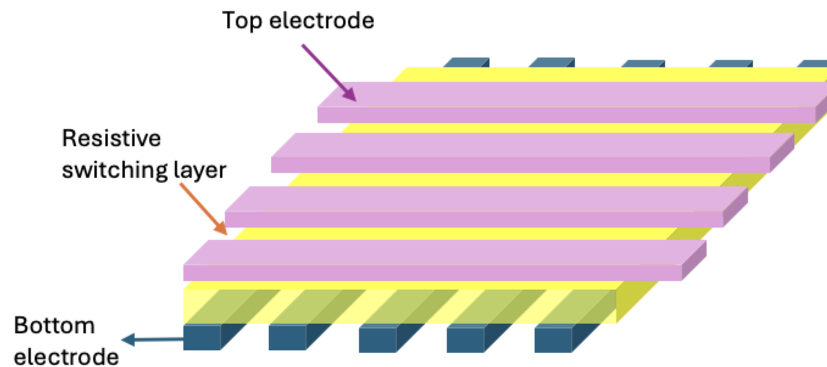


Figure 2.2 Schematic of a ReRAM crossbar array showing intersecting wordlines and bitlines with resistive switching elements at each node

2.3.1 Basic Unit Cell Structure

Each ReRAM memory cell comprises the following components:

- Top Electrode (TE): A conductive layer—commonly made from metals such as platinum (Pt), titanium nitride (TiN), or tungsten (W) that serves as the upper electrical contact.
- Resistive Switching Layer (RSL): A thin film positioned between the electrodes, responsible for the switching behavior. A wide variety of materials have been explored for this layer, including transition metal oxides, chalcogenides, perovskites, organic compounds, and two-dimensional (2D) materials.
- Bottom Electrode (BE): Typically constructed from Pt, Ti, doped polysilicon, or other conductive metals, functioning as the lower contact.

The resistive state of the device is governed by the redistribution of mobile species—such as ions, vacancies, or molecular defects—within the switching layer, which modulates the conductivity between a high-resistance state (HRS) and a low-resistance state (LRS).

2.3.2 Array Configuration and Operation

In a typical ReRAM crossbar array:

- Each memory cell acts as a programmable resistor at the WL/BL intersection.
- By applying a voltage across a specific WL and BL, a targeted cell can be:
  - Programmed (SET): Transitioned from HRS to LRS.
  - Erased (RESET): Transitioned from LRS back to HRS.
  - Read**:** Accessed via low voltage to determine its resistance state without disturbing the memory content.

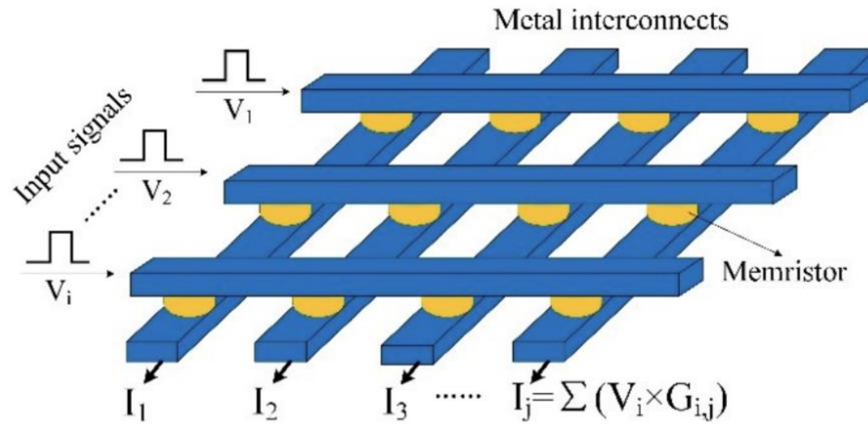


Figure 2.3 Crossbar array architecture for RRAM-based in-memory computing. Each intersection of the top and bottom electrodes hosts a resistive memory cell with conductance Gij. Input voltages Vi are applied to the word lines, and the resulting output currents Ij on the bit lines are computed as a weighted sum Ij=∑ViGij This structure enables efficient parallel matrix-vector multiplication for neuromorphic and compute-in-memory applications.[15]

2.3.3 3D Crossbar Arrays

To further enhance storage density, 3D vertical stacking of ReRAM crossbar arrays is employed. In this approach, multiple memory layers are fabricated on top of each other, each separated by insulating and interconnect layers.

This three-dimensional configuration drastically increases bit density without increasing the chip's footprint, making it ideal for:

- High-capacity memory modules
- In-memory processing cores
- Neuromorphic networks requiring massive parallelism

Recent advancements have demonstrated the feasibility of fabricating multi-layered ReRAM structures with precise layer alignment and reliable inter-layer connectivity, enabling compact and energy-efficient architectures for high-performance computing systems [16], [17].

2.3.4 Advantages of Crossbar-Based ReRAM Arrays

- **Transistor-less structure:** Crossbar arrays eliminate the need for access transistors (as in SRAM or DRAM), enabling a simpler fabrication process and reducing the memory cell size to as small as $4F^2$. V_{read}
- **CMOS compatibility:** ReRAM can be fabricated on top of existing CMOS layers, allowing hybrid systems that combine logic and memory within the same die [16].
- **Low-power operation:** Particularly in bipolar switching modes, ReRAM requires low-voltage SET/RESET transitions, offering significant energy savings [17].
- **Scalability:** Crossbar arrays scale well in both 2D and 3D, making them suitable for future generations of non-volatile memory, edge computing, and AI accelerators [18].

2.4 Traditional Fabrication & Characterization Techniques of Crossbar ReRAM

The fabrication of Resistive Random Access Memory (ReRAM) devices involves a series of precise nanofabrication steps tailored to construct high-performance, scalable, and CMOS-compatible non-volatile memory structures. The ReRAM cell, typically consisting of a **metal–insulator–metal (MIM)** configuration, relies on materials and processes that enable repeatable resistive switching through the formation and rupture of conductive filaments.

2.4.1 Fabrication Process Flow

One notable feature of fabricating ReRAM devices is that the resistive switching layer (RSL) is deposited uniformly across the entire wafer surface, covering both intended memory cell regions and surrounding non-active areas. This is typically achieved using deposition techniques such as atomic layer deposition (ALD) or physical vapor deposition (PVD), which provide precise control over thickness and composition.

After the uniform RSL deposition, the rest of the fabrication process follows conventional semiconductor methods. A bottom electrode (BE) layer—commonly platinum (Pt), titanium nitride (TiN), or tungsten (W)—is first deposited to serve as the lower contact. The RSL is then deposited across the wafer, followed by the top electrode (TE), often made from metals such as silver (Ag), aluminum (Al), or titanium (Ti).

Subsequent lithography and etching steps define the device structure, while passivation layers (e.g., SiO_2 or SiN) are added to protect against environmental degradation. The devices are then diced, packaged, and subjected to standard electrical characterization.

Fabricated devices undergo electrical testing to verify their functionality and reliability, including:

- Current–voltage (I–V) characterization for SET/RESET transitions
- Endurance testing across multiple cycles
- Retention analysis over time to ensure data stability
- Forming voltage and resistance-state distribution analysis to assess device variability

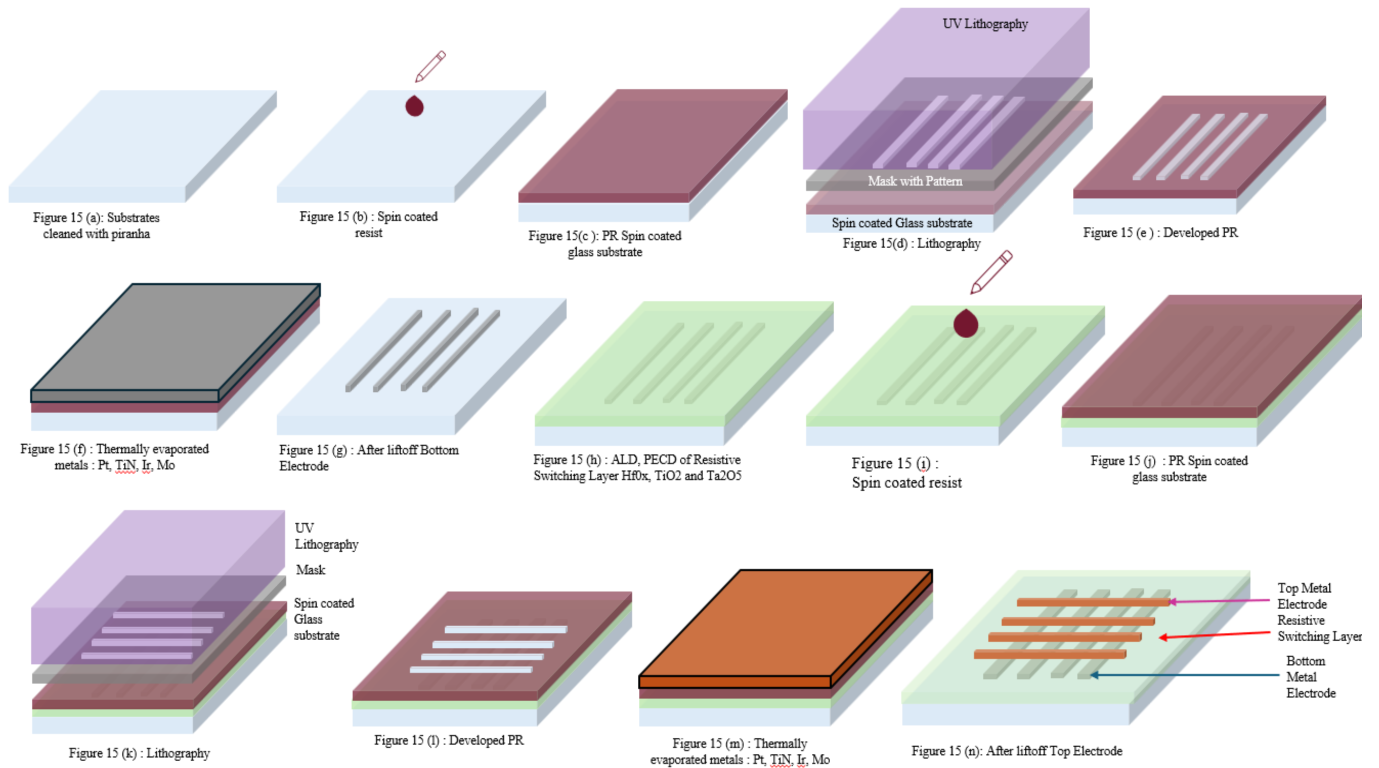


Figure 2.4 Traditional Fabrication Process

2.4.2 Basic Operation Principle

ReRAM operates on the principle of resistive switching, wherein the device can toggle between a high resistance state (HRS) and a low resistance state (LRS) under the application of external voltages. These two states correspond to the binary values "0" and "1" in digital logic. ReRAM operates on the principle of resistive switching, wherein the device can toggle between a high resistance state (HRS) and a low resistance state (LRS) under the application of external voltages. These two states correspond to the binary values "0" and "1" in digital logic. The switching mechanism typically involves the formation and dissolution of conductive filaments—nanoscale pathways that develop within the resistive switching layer. These filaments may form through various physical or chemical processes such as the migration of oxygen vacancies, metal cations,

or the reconfiguration of molecular structures, depending on the material system employed. When formed, the filament bridges the electrodes and provides a low-resistance path for current (LRS); its rupture restores the high-resistance state (HRS). Key operating stages include:

- **Electroforming**: A high voltage (forming voltage, V_x) is initially applied to form the first conductive filament. This is typically a one-time process that brings the virgin device into a switchable state.
- **SET Process** (*Vset*): A moderate positive or negative voltage is applied to reform the filament, switching the device from HRS to LRS (ON state).
- **RESET Process** (*Vreset*): An opposite-polarity voltage (in bipolar devices) or higher current (in unipolar devices) is used to disrupt the filament, restoring the device to HRS (OFF state).

These switching operations are non-volatile, meaning the resistance state is retained even when the power is removed. While I–V sweeps are typically used for device characterization, practical ReRAM operation relies on discrete voltage pulses. In bipolar devices, SET and RESET are triggered by opposite-polarity pulses, whereas in unipolar devices, both operations use same-polarity pulses with different current levels; a small read pulse is used to sense the resistance state without disturbing it.

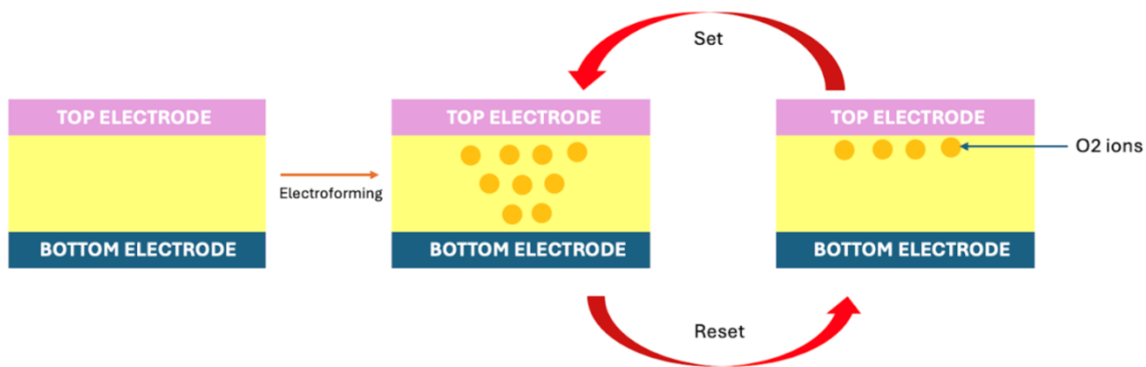


Figure 2.5 Resistive switching mechanism in a metal–insulator–metal (MIM) ReRAM structure. Initially, an **electroforming** step creates conductive filaments by inducing oxygen vacancy migration. The **SET** process forms a low-resistance state (LRS) through filament formation, while the **RESET** process ruptures the filament by reintroducing O_2 ions, returning the device to a high-resistance state (HRS).

2.4.3 Switching Modes in ReRAM

Resistive switching in ReRAM is generally classified into two categories based on the polarity of the applied voltage:

(a) Unipolar Switching

In unipolar ReRAM, both the SET and RESET operations occur under the same voltage polarity, typically distinguished by different current magnitudes. The switching mechanism is primarily thermally driven, with Joule heating playing a crucial role in the formation and rupture of conductive filaments within the resistive switching layer.

- **SET Operation:** A voltage pulse (e.g., +2.5 V) is applied with a compliance current limit to gradually form the conductive filament. A compliance current is applied to limit excessive filament growth, enabling the controlled formation of a conductive path and transitioning the device to a low resistance state (LRS).
- **RESET Operation:** A higher current pulse of the same polarity is applied to generate Joule heating, which breaks the filament and restores the device to the HRS. A higher current induces localized heating, which disrupts the filament and returns the device to a high resistance state (HRS).
- **READ Pulse**: As in bipolar devices, a low-magnitude pulse is used to sense the resistance without triggering switching.

A major challenge in unipolar switching is maintaining thermal stability and avoiding permanent breakdown, which requires careful regulation of both current and voltage during operation.

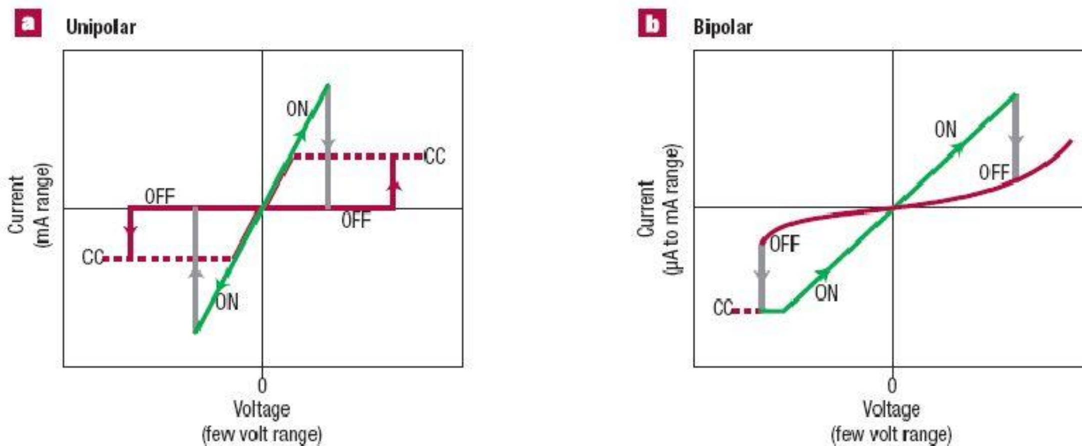


Figure 2.6: a) Unipolar Switching b) Bipolar Switching [19]

(b) Bipolar Switching

In bipolar ReRAM, the SET and RESET operations are triggered by voltages of opposite polarity, allowing directional control over the resistive switching process.

- **SET Operation:** A moderate positive pulse is applied (e.g., +1.5 V to +2 V) to form or reform the conductive filament, transitioning the device from HRS to LRS. Application of a voltage with one polarity causes mobile charge carriers within the switching layer to migrate, leading to the formation of a conductive filament and transition to the low resistance state (LRS).
- **RESET Operation:** A negative pulse (e.g., −1.5 V to −2 V) is applied to rupture the filament and return the device to the HRS. Reversing the voltage polarity drives the redistribution or removal of these carriers, disrupting the conductive path and restoring the high resistance state (HRS).
- **READ Pulse**: A small, non-destructive pulse (e.g., ±0.1 V to ±0.3 V) is applied to detect the current level without altering the resistance state. The current is compared to a reference threshold to determine logic “0” or “1”.

Bipolar switching is primarily field driven, relying on electrochemical and interfacial processes rather than thermal effects. This mode typically allows for lower power consumption and finer control over resistance modulation compared to unipolar switching. As a result, bipolar ReRAM is often favored in applications requiring high endurance, low energy operation, and precise tunability, such as embedded systems and neuromorphic computing.

2.4.4 Practical Pulse-Based Operation in ReRAM Devices

In practical memory applications, ReRAM devices are not operated using voltage sweeps. While sweeping voltages is useful for device characterization, it is not suited for actual operation. ReRAM switching is governed by filamentary mechanisms—where conductive paths are formed and ruptured inside the resistive switching layer. Applying a voltage sweep can unintentionally strengthen, weaken, or partially form these filaments, leading to unpredictable behavior such as unstable switching, degraded endurance, or even permanent damage to the cell [20]. Consequently, voltage sweeping is unsuitable for routine programming or reliable readout in dense memory arrays.

Instead, ReRAM devices are controlled using precisely defined voltage pulses. These pulses are short in duration and specifically designed to initiate a clear transition between the high-resistance state (HRS) and the low-resistance state (LRS). SET pulses are used to form the conductive filament, while RESET pulses rupture it. This pulse-driven mode of operation ensures deterministic switching and preserves device integrity over repeated cycles [21]. Moreover, pulse-based control allows for better uniformity, improved energy efficiency, and higher endurance compared to voltage sweep-based approaches.

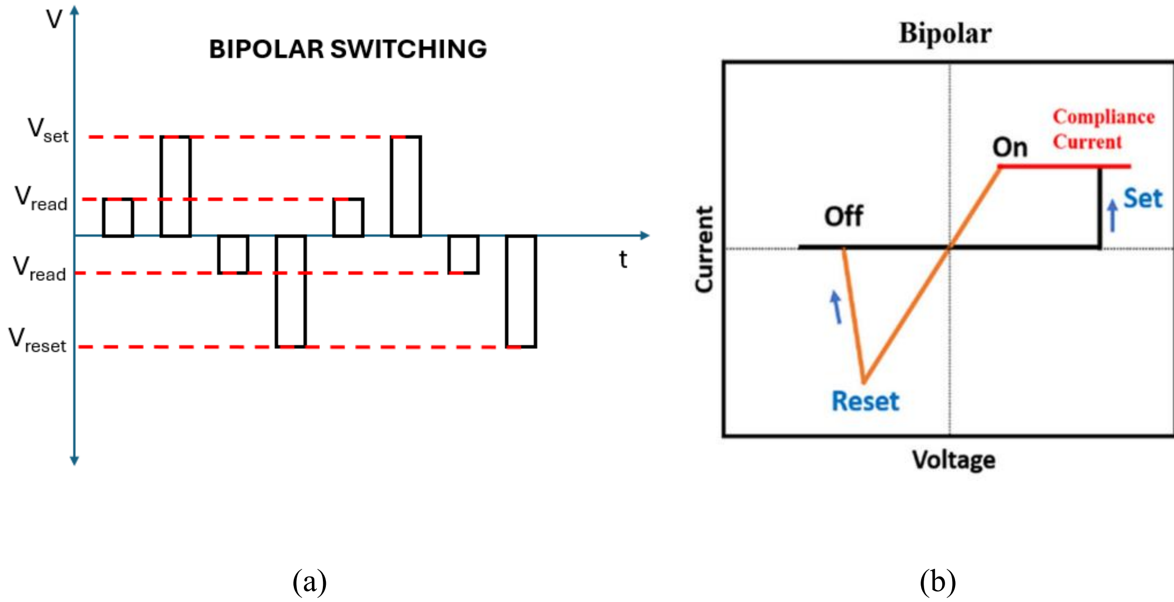
Depending on the switching mode, the polarity and shape of the pulses differ: In bipolar ReRAM, SET and RESET operations are performed using pulses of opposite polarity. One polarity causes ion migration and filament growth (SET), while the opposite polarity pulse breaks the filament (RESET). In unipolar ReRAM, both operations use the same polarity but differ in pulse amplitude or current compliance. The RESET operation typically involves higher thermal energy (Joule heating) to rupture the filament. The READ operation is implemented using a small-amplitude,

short-duration pulse that is sufficient to detect the cell's resistance state without disturbing it. Since the read pulse is non-destructive, it can be applied repeatedly without affecting the long-term reliability of the device [22].

A key consideration is that low voltage sweeps, or underpowered pulses are not effective during SET/RESET characterization. Applying sub-threshold voltages or narrow sweeps can lead to partial filament formation, resulting in ambiguous intermediate resistance states. These partial states may act as inadvertent current paths—causing sneak path currents that affect adjacent cells in the array. To prevent this, it is essential to apply well-calibrated, high-magnitude pulses that clearly differentiate the device between HRS and LRS, thus ensuring reliable switching and minimal interference from neighboring cells.

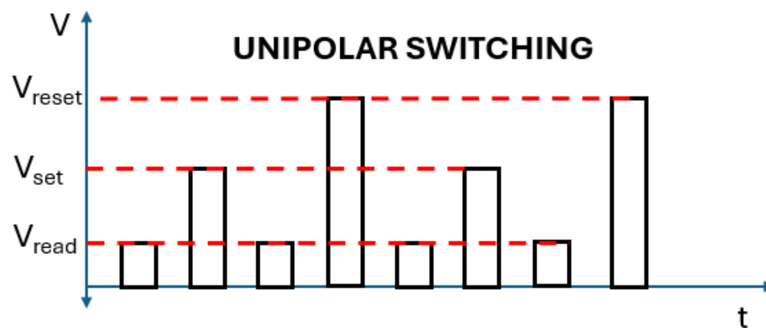
Beyond reliability, ReRAM also offers a significant speed advantage over traditional volatile memories such as DRAM. In DRAM, reading a memory cell requires accessing a small capacitor and sensing the voltage change through a sense amplifier—a process that is inherently limited by capacitive charging time and the need for signal amplification. In contrast, ReRAM readout is achieved by applying a voltage pulse across a resistive cell and measuring the current response almost instantaneously. This direct sensing approach makes ReRAM inherently faster for read operations, particularly in scenarios requiring rapid memory access and minimal latency.

To further illustrate these principles, Figures 2.5, 2.6, and 2.7 show how SET, RESET, and READ pulses are applied in both unipolar and bipolar configurations, as well as how filament formation and rupture occur within the device. These diagrams also explain the pulse calibration sequence used during testing and characterization.

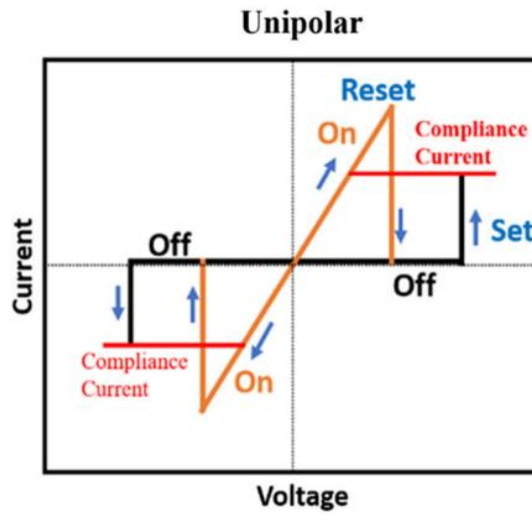


(a) (b)

Figure 2.7 (a) Bipolar Switching Pulse Pattern: A time-domain representation of voltage pulses applied to a ReRAM cell under bipolar operation. SET and RESET states are induced by alternating polarity pulses, while intermediate low-voltage pulses are used for read operations. This bidirectional switching ensures well-defined transitions between HRS and LRS. (b) Typical hysteretic bipolar current–voltage (I– V) characteristics in metal– insulator–metal (MIM) structures. [23]

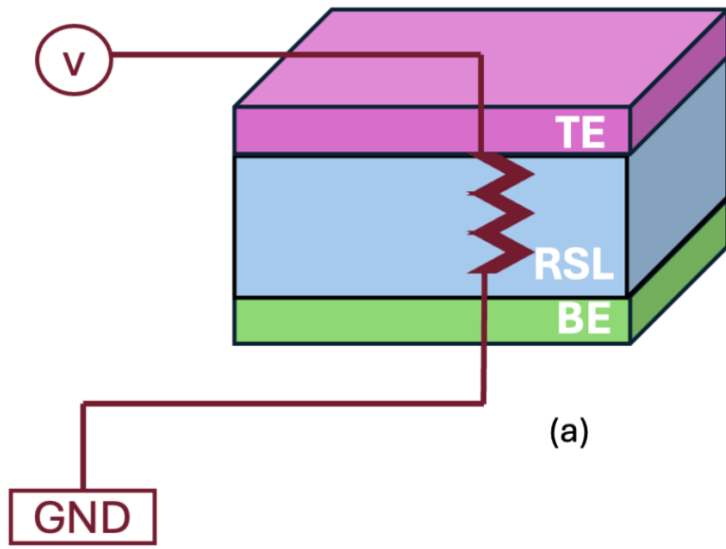


(a)

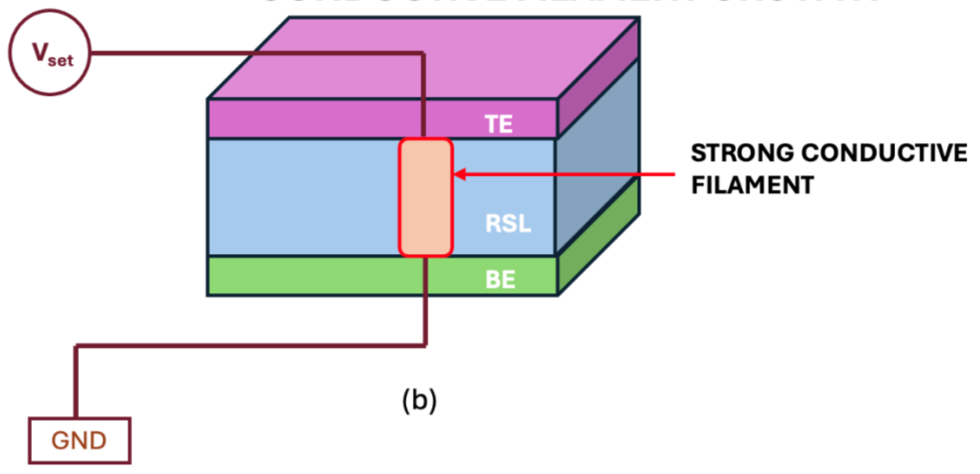


(b)

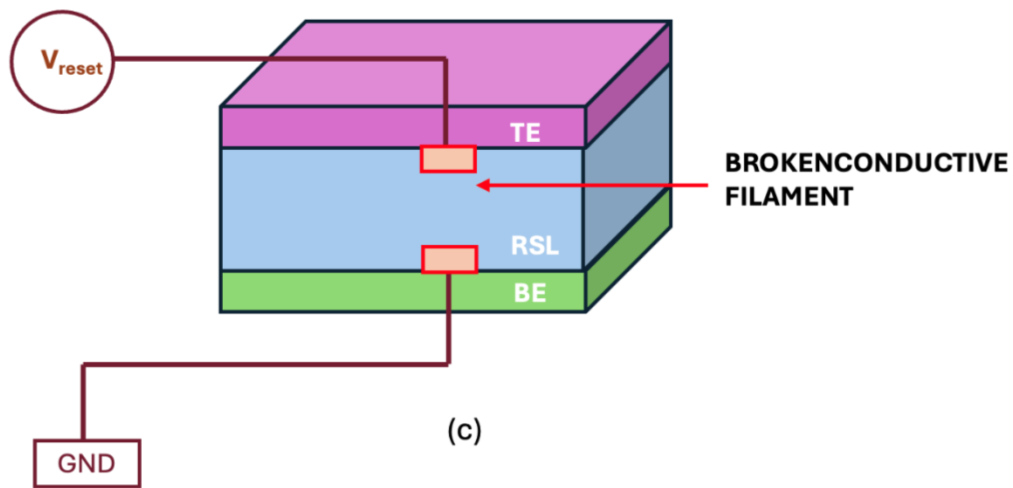
Figure 2.8 (a) Unipolar Switching Pulse Pattern: Voltage pulse profile for unipolar switching in ReRAM. All SET, RESET, and READ operations occur with the same polarity. The SET pulse initiates filament formation, the RESET pulse ruptures the filament via higher Joule heating, and the READ pulse senses the state without affecting it. (b) Typical hysteretic unipolar current–voltage (I– V) characteristics in metal– insulator–metal (MIM) structures. [23]

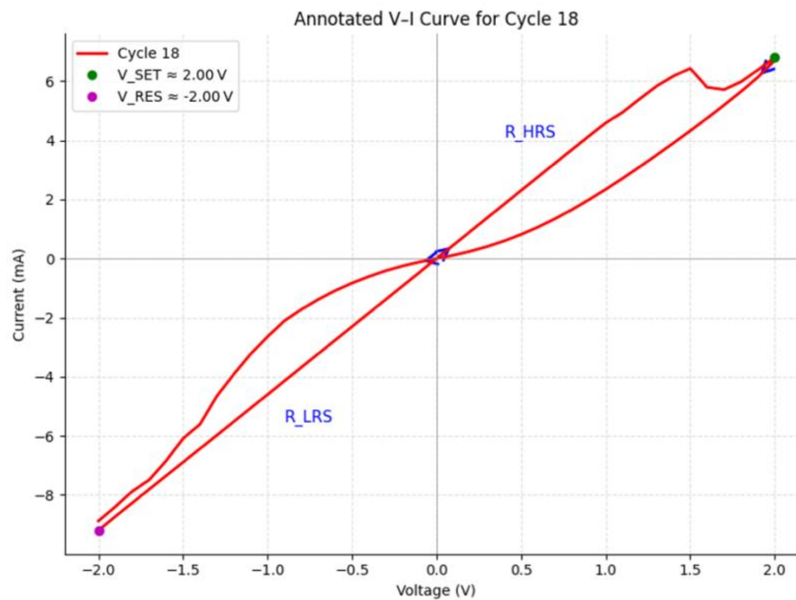


(a)



(b)





(d)

Figure 2.9 Pulse Calibration and Filament Dynamics in ReRAM Devices (a) Basic schematic of ReRAM test setup with voltage applied to the top electrode. (b) SET operation: A higher magnitude voltage pulse forms a stable conductive filament between TE and BE. (c) RESET operation: A high-energy pulse breaks the filament, restoring HRS. (d) A representative I–V curve

showing distinct resistance states (LRS and HRS) and the SET/RESET voltages after multiple cycles.

In conclusion, ReRAM devices are fundamentally pulse-operated systems, where the correct application of pulse amplitude, duration, and polarity is crucial for accurate and reliable switching. Avoiding low-voltage sweep-based testing is essential to maintain the device's integrity and prevent sneak path interference. The pulse-based model not only enhances performance and endurance but also enables faster readout speeds compared to conventional DRAM architecture, solidifying ReRAM's position as a leading candidate for next-generation memory solutions.

2.4.5 Reading Current from a ReRAM Cell

The read mechanism in ReRAM is based on a simple yet efficient current-sensing approach, where the cell's resistance state is determined by measuring I_{read} under a controlled V_{read}. Reading data from a ReRAM cell involves measuring the current flow when a small read voltage is applied, enabling differentiation between distinct resistance states that correspond to binary data values.

Read Operation Principle

The read operation in a ReRAM cell is performed by applying a low read voltage (V_{read}), typically in the range of 0.1V to 0.5V, across the memory cell. This voltage is significantly lower than the programming voltages used for the SET (low-resistance state, LRS) and RESET (high-resistance state, HRS) operations to prevent unintentional switching. The applied voltage induces a current (I_{read}) through the cell, which is measured to determine its resistance state.

Current Sensing and Data Interpretation

The read current (I_{read}) is measured using a current-sensing circuit, such as a sense amplifier or a current mirror circuit. The resistance state of the ReRAM cell is interpreted based on the magnitude of I_{read}, as follows:

- If high current is detected ($I_{read}>I_{ref}$), the cell is in the Low-Resistance State (LRS), representing a stored logic "1".

- If low current is detected ($I_{read}<I_{ref}$), the cell is in the High-Resistance State (HRS), corresponding to a logic "0".

A reference current (I_{ref}) is pre-defined to distinguish between LRS and HRS, ensuring reliable read operations. The measured current is compared against I_{ref} using a differential amplifier or a current comparator. Once classified, the binary data is output to the memory controller for further processing.

2.5 Applications of ReRAM crossbar array

Resistive Random Access Memory (ReRAM) crossbar arrays have emerged as a versatile platform for both data storage and computation. Their intrinsic properties — high density, parallelism, multi-level storage capability, and compatibility with analog operations — make them attractive for a range of applications from neuromorphic computing to energy-efficient AI acceleration. This section highlights four major advantages of ReRAM crossbar arrays, supported by recent studies demonstrating their practical potential.

This section explores the diverse applications of ReRAM arrays, highlighting their role in embedded memory, artificial intelligence, biomedical devices, and next-generation logic-in-memory architecture. As research and development continue, ReRAM is expected to play a critical role in shaping the future of computing and data storage solutions.

2.5.1 Neuromorphic Computing for Reinforcement Learning

ReRAM crossbar arrays are particularly well-suited for neuromorphic architectures that emulate biological synapses, enabling **in situ learning** without the need for extensive data transfers. This approach addresses the von Neumann bottleneck and improves both speed and energy efficiency.

In *"Reinforcement Learning with Analogue Memristor Arrays",* a three-layer 1T1R memristor network was used to solve the cart–pole and mountain car problems via a hybrid analog–digital learning algorithm. The hardware performed direct synaptic weight updates, eliminating the need for pre-defined models and achieving robust training with significant energy savings.

Similarly, Zidan et al. (Nat. Electron., 2022)[24] demonstrated a memristor-based neuromorphic core capable of real-time learning for edge devices, achieving over 100× energy efficiency improvements compared to GPU-based RL implementations. Wang et al. (IEEE TED, 2021) [25] further advanced this field by employing multi-level conductance states in HfO_2-based RRAM for spiking neural networks, achieving 92% MNIST accuracy with on-chip training.

These works collectively demonstrate that ReRAM-based neuromorphic platforms can deliver fast, energy-efficient reinforcement learning suitable for embedded and autonomous systems.

2.5.2 In-Memory Computing for Edge AI and Image Processing

A defining advantage of ReRAM crossbar arrays is their ability to combine storage and computation in the same physical location, enabling in-memory computing (IMC). This drastically reduces the energy and time costs associated with shuttling data between separate memory and processing units.

In *"In-Memory Computing with Memristor Arrays*[26]*",* Li et al. implemented a 128 × 64 1T1R crossbar array for image edge detection, executing convolution operations directly within the array. The result was a substantial reduction in both energy consumption and computation time compared to conventional methods.

Expanding on this, Hu et al. (Nature, 2018)[27] presented a large-scale hybrid CMOS–memristor processor for image classification, reporting a 10× energy reduction over GPU inference. More recently, Yao et al. (Nat. Commun., 2020)[28] demonstrated a mixed-precision approach where high-accuracy operations were combined with analog in-memory computation, enabling efficient object recognition with significant throughput gains.

These studies show that ReRAM-based IMC is highly suited to real-time, low-power tasks in edge AI and embedded vision systems.

2.5.3 High-Performance Matrix–Vector Multiplication

Matrix–vector multiplication (MVM) is a fundamental operation in AI, signal processing, and scientific computing. The parallel current summation capability of ReRAM crossbars allows direct mapping of matrix weights to device conductance, enabling extremely efficient MVM operations.

Xia et al. [29] investigated device-level and circuit-level non-idealities, such as nonlinear I–V behavior and interconnect resistance and developed an optimization flow that improved recognition accuracy by 10.98% and reduced energy consumption by 26.4% for an SVM classifier on MNIST.

Earlier, Shafiee et al. (ISCA, 2016)[30] introduced PRIME, an in-memory ReRAM architecture that achieved up to 236× improvement in energy efficiency for CNN inference compared to traditional architecture. Chi et al. (ISSCC, 2016)[31] also demonstrated an RRAM-based accelerator delivering 30 TOPS/W for deep learning workloads.

These findings establish that, when carefully optimized, ReRAM-based MVM engines can outperform conventional hardware accelerators in both speed and power efficiency.

2.5.4 Robust Deep Neural Network Inference

For ReRAM-based AI accelerators, resilience to device variation is critical. Variations in conductance during programming and retention can degrade the accuracy of deep neural network (DNN) inference if left uncompensated.

The SWIPE framework [32]addresses this issue by introducing a Single-Write In-memory Program–Verify approach. SWIPE leverages bit-sliced architecture and statistical variation modeling to achieve accurate writes at 5×–10× lower cost than traditional program–verify schemes, maintaining <1% accuracy loss even under 4.8×–7.7× higher variation levels.

Sun et al. (IEEE TCAS-I, 2022)[33] proposed adaptive closed-loop programming, recovering up to 15% of lost accuracy for CIFAR-10 classification in high-variation scenarios. Together, these

methods show that robust programming and variation-aware training make ReRAM arrays viable for large-scale, high-accuracy neural network inference.

Summary

ReRAM crossbar arrays have demonstrated unique strengths across multiple domains:

- **Neuromorphic computing** — fast, energy-efficient reinforcement learning and spiking neural networks.
- **In-memory computing** — reduced data movement for low-power edge AI and real-time vision.
- **Matrix–vector multiplication** — highly parallel, energy-efficient execution of AI and scientific workloads.
- **Robust DNN inference** — accuracy preservation under significant device variation.

As fabrication techniques mature and variation control improves, these advantages position ReRAM crossbar arrays as a cornerstone technology for next-generation computing and storage architectures.

2.6 Sneak Path Currents of existing structure

Sneak-path currents are a major limitation in Resistive Random Access Memory (ReRAM) crossbar architectures. In typical designs, the resistive switching layer is deposited uniformly across the substrate, covering both active and non-active areas of the array. This uniform coverage allows **unintended conductive paths** to form through unselected cells when a bias voltage is

applied to a selected cell. As a result, unwanted leakage currents—commonly referred to as *sneak paths*—flow through neighbouring cells, distorting read and write operations, degrading device reliability, and increasing standby power consumption [34].

Causes and Scaling Impact

In a crossbar array, each memory cell is positioned at the intersection of a wordline and a bitline. When voltage is applied to a selected cell, **shared conductive pathways** through adjacent unselected cells can form due to the continuous resistive switching layer [34][35]. This causes *cross-talk interference*, making it difficult to distinguish between high-resistance state (HRS) and low-resistance state (LRS) values during read operations.

The problem becomes more severe as array size increases. In high-density designs, cumulative leakage from multiple unselected cells drastically reduces **read margin**, increases energy loss, and accelerates device variability. These factors limit the scalability of ReRAM for **ultra-high-density storage and computing applications[36]**.

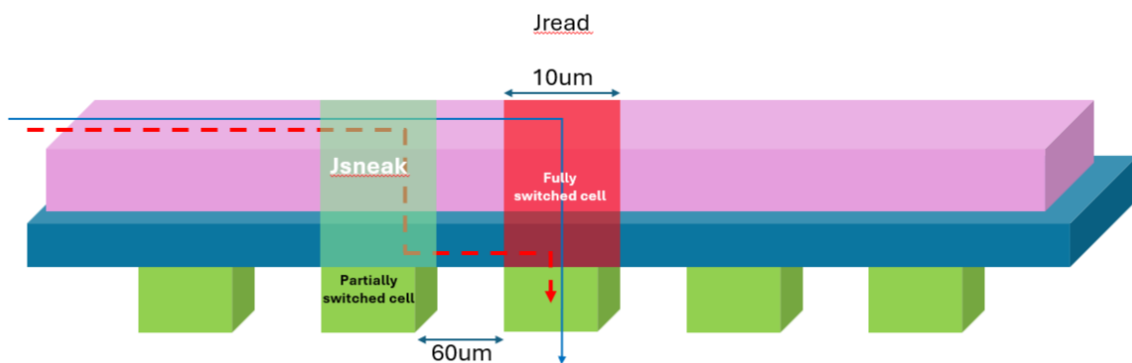


Figure 2.10 Illustration of sneak-path current in a crossbar memory array. While the desired current flows through the selected cell, unwanted sneak-path current (I_{sneak}-path) flows through adjacent unselected cells, potentially leading to incorrect readouts and degraded memory performance.

Material and Structural Approaches

One effective strategy for sneak-path suppression is the adoption of bilayer resistive switching stacks. In such devices, two dielectric layers with distinct electrical properties are combined to produce intrinsic nonlinearity in the I–V characteristics. This nonlinearity helps block low-voltage leakage in unselected cells, thereby improving read margins even in selector-less (1R) architectures.

Examples include ZrO_x/HfO_x bilayers, which demonstrate both improved resistive switching stability and enhanced synaptic characteristics for neuromorphic applications [37], and Al_2O_3-based bilayers, which exhibit multilevel resistive switching capabilities while simultaneously suppressing sneak currents[35].

The role of bilayers in sneak-path suppression is particularly important: the additional dielectric interface creates an energy barrier or series resistance that limits unwanted leakage currents through unselected cells. In effect, the bilayer structure forces sneak-path conduction to remain in the high-resistance state (HRS)**,** while still allowing selected cells to switch into the low-resistance state (LRS) under sufficient bias.

Another important approach is geometrical confinement of the resistive switching region. By using patterned deposition, insulating sidewalls, or locally defined RSL regions, leakage paths can be reduced by physically restricting possible conduction routes[38]. In 3D stacked architectures, alternating insulating and conducting layers increase the effective path resistance between unintended nodes, further mitigating leakage.

Architectural Mitigation Methods

Several device and array architectures have been implemented to address sneak-path currents:

- **Selector Integration** – **1D1R** (diode + ReRAM), **1S1R** (threshold switch + ReRAM), and **1T1R** (transistor + ReRAM) configurations ensure that only the targeted cell conducts current. While highly effective, they add fabrication complexity and consume additional footprint [39].
- **Complementary Resistive Switching (CRS)** – CRS pairs two cells in anti-series with opposite resistance states, maintaining a high overall resistance during standby, effectively suppressing sneak paths without external selectors[40].

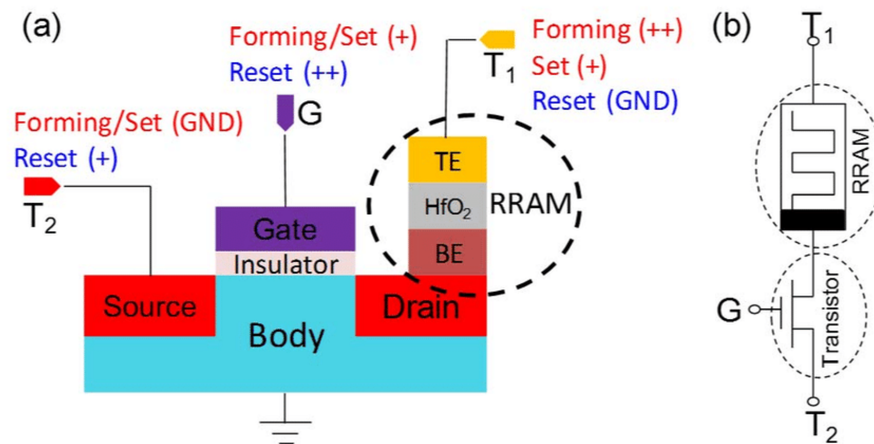


Figure 2.11 Schematic of a **1T1R (one-transistor–one-resistor) ReRAM cell** for sneak-path suppression[41]. (a) Device-level configuration showing the RRAM stack (TE/HfO_2/BE) connected in series with a MOSFET selector transistor. The gate controls access to the memory cell, ensuring that only the selected device is activated during forming, SET, and RESET operations, while unselected cells remain electrically isolated.

(b) Equivalent circuit representation of the 1T1R cell, where the transistor acts as an access selector in series with the RRAM device, effectively blocking leakage and suppressing sneak-path currents in crossbar arrays.

Analytical Modelling and Bias Schemes

Analytical and equivalent-circuit models describe sneak-path behavior as a function of array size, resistance ratio, and bias conditions. These models help determine the optimal HRS/LRS ratio and selector nonlinearity for reliable operation.

Algorithmic and Coding-Based Mitigation

Beyond physical and architectural methods, algorithmic techniques are emerging to combat **sneak-path interference (SPI)**. Coding-based methods restrict the arrangement of logical data to minimize the probability of activating leakage-prone patterns, while SPI-aware detection algorithms dynamically adjust read thresholds to counteract interference effects[42][43]. These approaches can be combined with hardware-level mitigation for further improvements in high-density ReRAM arrays.

CHAPTER 3: EXPERIMENTAL FABRICATION OF PROPOSED ReRAM DEVICES

3.1 Material Selection for ReRAM Devices

Material selection plays a critical role in determining the switching characteristics, endurance, and power efficiency of ReRAM devices. In this study, we employed a three-layer metal–insulator–metal (MIM) structure composed of silver (Ag) as the bottom electrode, PEDOT: PSS as the switching layer, and copper (Cu) as the top electrode.

Silver is widely used in ReRAM devices due to its excellent electrical conductivity and its ability to facilitate filamentary switching via the electrochemical metallization (ECM) mechanism. Ag ions readily migrate under an electric field, forming conductive filaments that enable low voltage switching and fast response times.

The resistive switching layer in our devices is based on PEDOT: PSS (poly(3,4-ethylenedioxythiophene): polystyrene sulfonate), a conductive polymer blend known for its solution processability, mechanical flexibility, and electrochemical stability[44]. PEDOT: PSS has demonstrated reproducible bipolar resistive switching behavior with excellent endurance and data retention.

Copper is selected as the top electrode owing to its moderate mobility and established role in ReRAM switching via Cu filament formation. In combination with PEDOT: PSS, Cu has been shown to yield stable bipolar switching characteristics, often with low SET/RESET voltages and acceptable endurance[45]. Its low cost, CMOS compatibility, and ability to integrate into flexible

substrates further support its use in emerging memory systems. This material stack supports energy-efficient, analog-tunable, and scalable ReRAM architecture, making it well-suited for future neuromorphic, flexible, and low-power memory applications.

Table 3.1 Advantages of the material stack

Layer	**Material**	**Key Advantages**
Bottom Electrode	Silver (Ag)	High conductivity, ECM switching, low SET voltage
Switching Layer	PEDOT: PSS	Solution processable, analog switching, flexible, low voltage
Top Electrode	Copper (Cu)	Filamentary switching, CMOS-compatible, cost-effective

3.2 Fabrication Process

The fabrication of ReRAM devices was performed on glass substrates using standard microfabrication techniques, including photolithography, spin-coating, and thermal evaporation. The device architecture is based on a planar crossbar array comprising a bottom electrode (BE), a PEDOT: PSS-based switching layer, and a top electrode (TE). Each fabrication stage was carried out under cleanroom conditions to ensure process reliability and device uniformity.

3.2.1 Bottom Electrode Fabrication

The process began with thorough cleaning of the glass substrate using piranha solution (3:1 H_2SO_4:H_2O_2), followed by rinsing with deionized water and drying with a nitrogen blow gun, as shown in Figure 3.1. A layer of negative photoresist (NR9-1500PY) was spin-coated at 3000 rpm for 30 seconds and soft-baked to remove residual solvents, as shown in Figure 3.2. UV lithography was performed using a patterned chrome mask to define the bottom electrode geometry, as shown in Figure 3.3. Since this is a negative photoresist, a post exposure bake was performed on a hotplate at 100°C for 10 minutes.

After development in a RD6 photoresist developer, the devices were all rinsed with a DI water and dried. A bilayer of chromium (Cr, ~5 nm) and silver (Ag, ~100 nm) were deposited using thermal evaporation (Angstrom Engineering Covap II) under high vacuum, as shown in Figure 3.4. Chromium served as an adhesion layer between the silver and the glass substrate. Following deposition, a lift-off process, Figure 3.5, was executed using acetone to remove the unwanted metal and photoresist, leaving well-defined bottom electrode lines on the substrate.

Figure 3.1 : Substrates cleaned with piranha

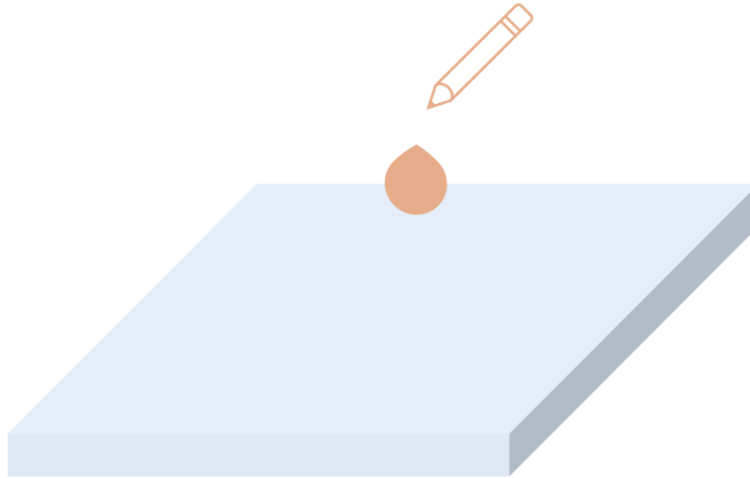


Figure 3.2 (a) : Spin coated NR9-1500PY resist 3000rpm for 30sec

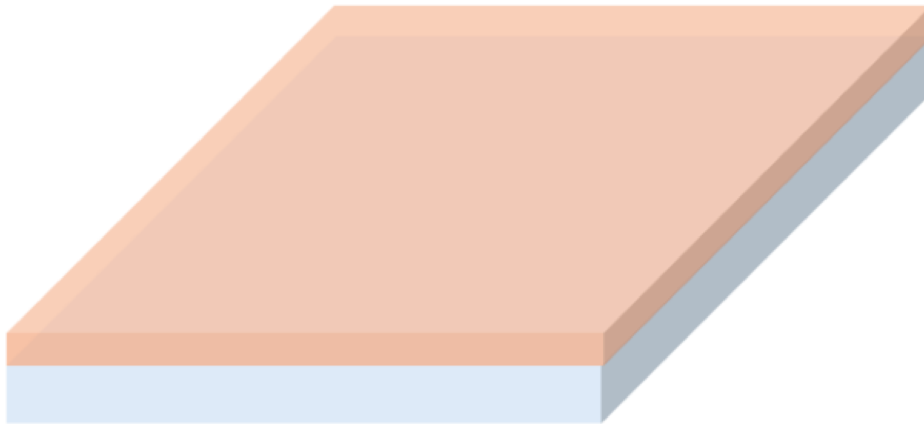


Figure 3.2 (b) : PR Spin coated glass substrate

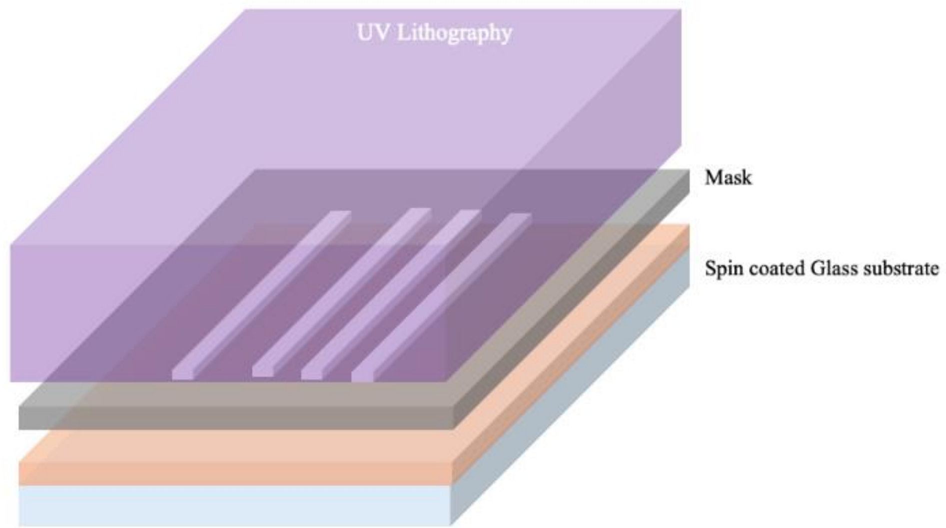


Figure 3.3 (a) : UV Lithography

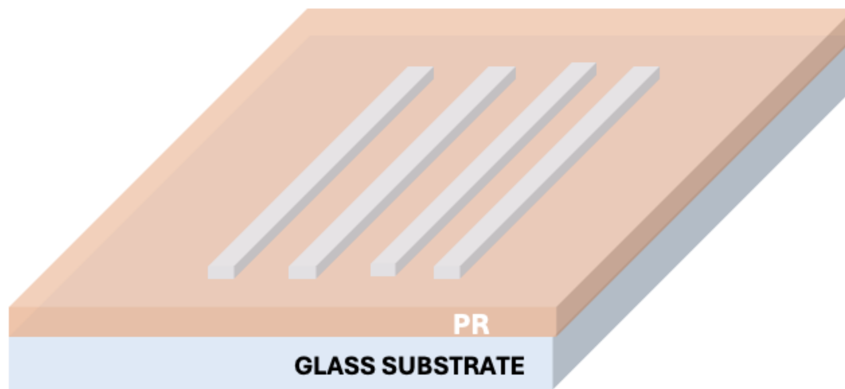


Figure 3.3 (b) : Developed PR

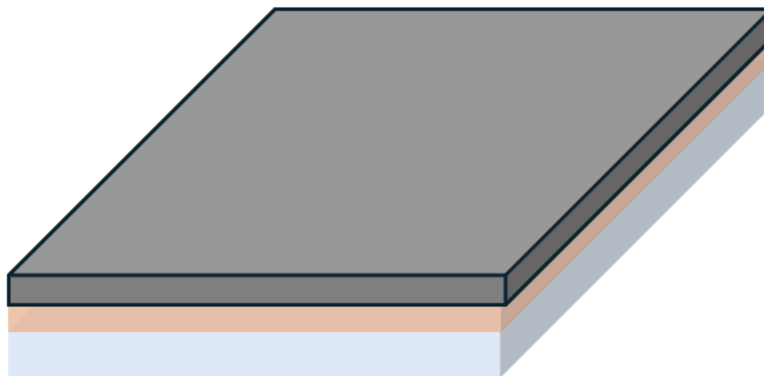


Figure 3.4: Thermally Evaporating Bottom Electrode Layer

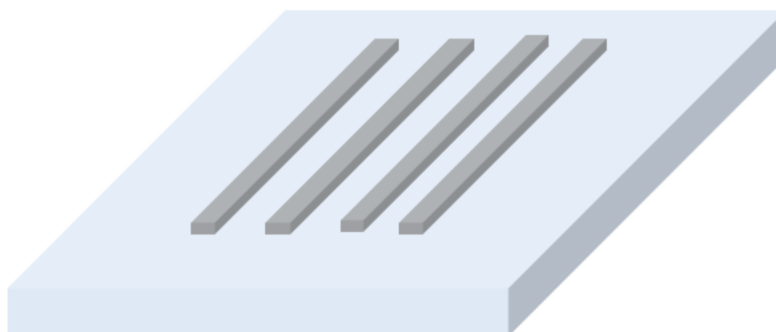


Figure 3.5: After liftoff Bottom Electrode Silver

3.2.2: Switching Layer and Top Electrode Stack Definition

Following bottom electrode formation, a negative photoresist was spin-coated again at 3000 rpm for 30 seconds, as shown Figures 3.6 and 3.7, and patterned via UV lithography using a second mask, as shown in Figure 3.8. The overlapping area between the bottom and the top electrode is defined as an active switching area.

PEDOT:PSS solution was then spin-coated onto the patterned substrate at 1000 rpm for 30 seconds followed by thermal annealing on a hotplate at 110°C for 10 minutes, as shown in Figure 3.9.

Without any development or intermediate lift-off, the substrate proceeded directly to top electrode deposition.

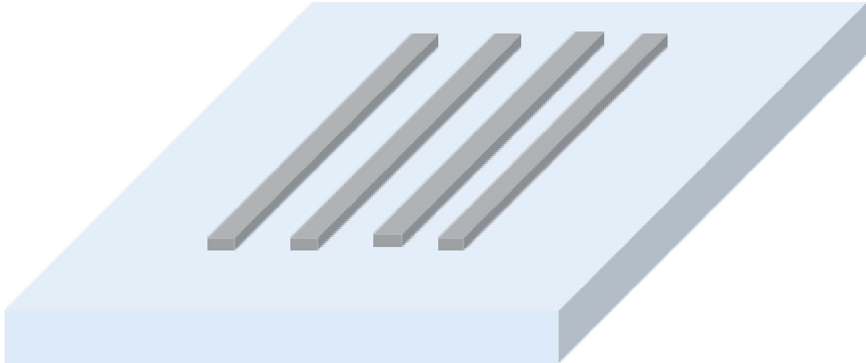


Figure 3.5: After liftoff Bottom Electrode Silver

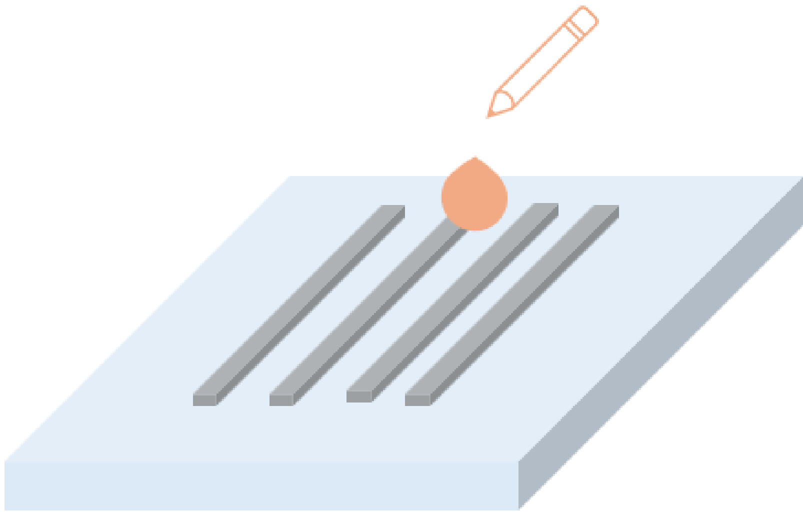


Figure 3.6: Spin coated NR9-1500PY resist 3000rpm for 30sec

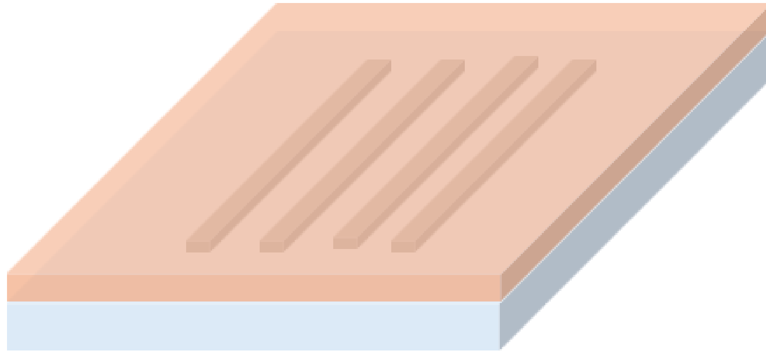


Figure 3.7 : PR Spin coated glass substrate

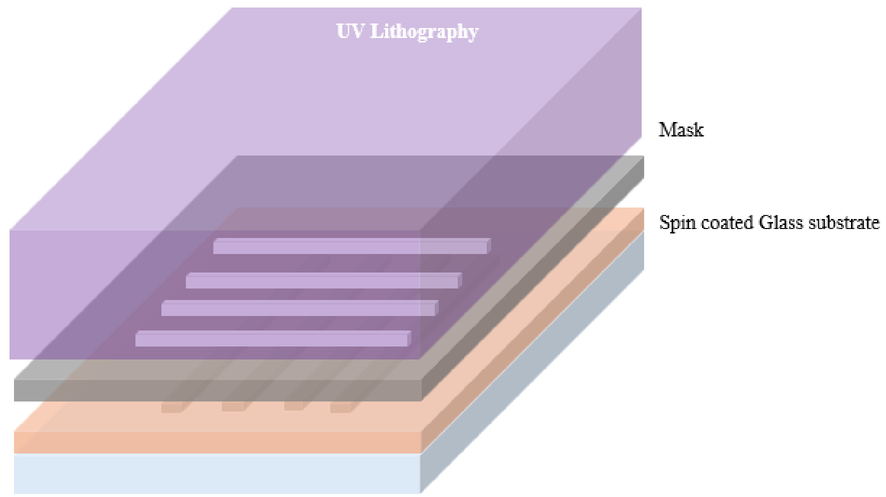


Figure 3.8 (a) : UV Lithography

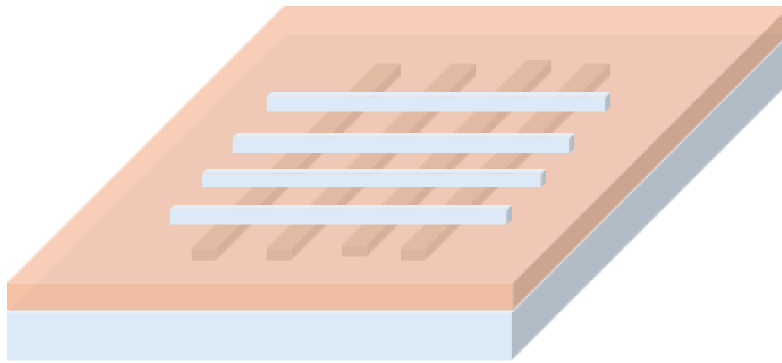


Figure 3.8 (b) :Developed PR

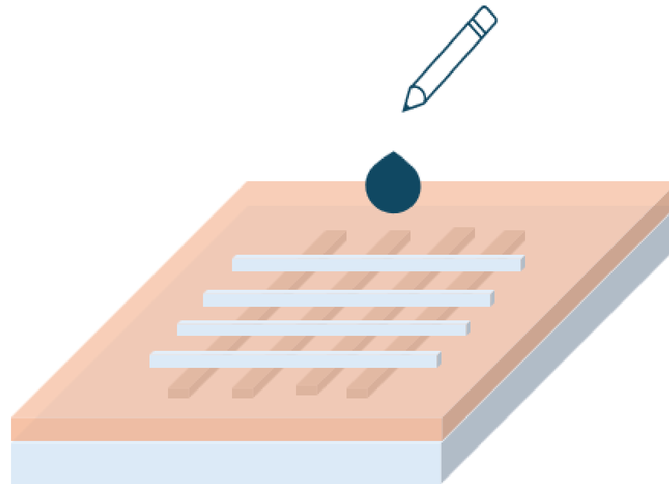


Figure 3.9(a) :Spin coat PEDOT : PSS at 1000rpm for 30sec

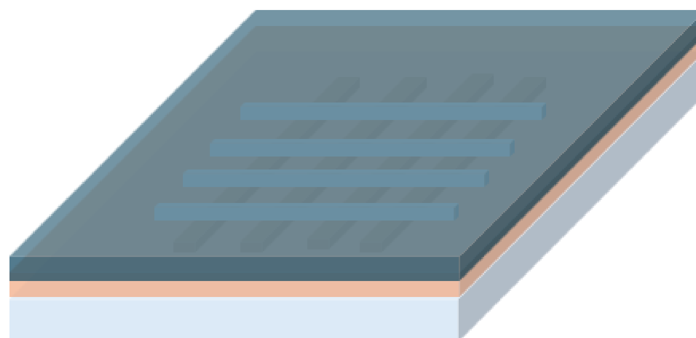


Figure 3.9 (b): Spin coated PEDOT:PSS

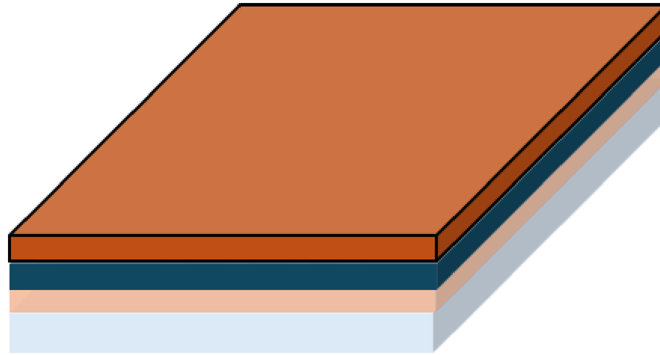


Figure 3.10 : Thermally evaporated Cu

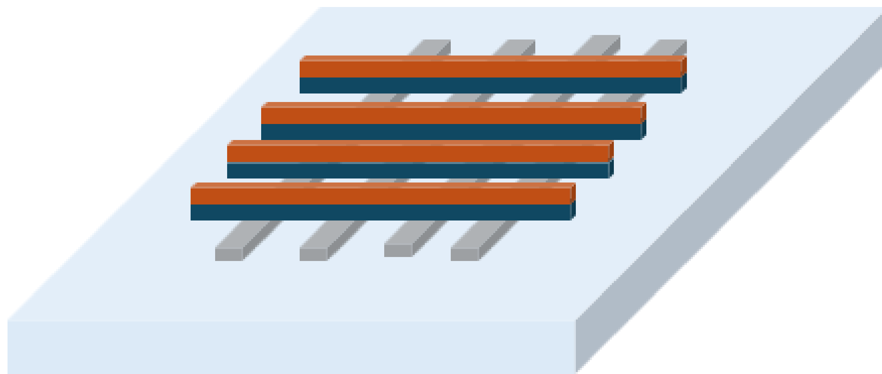


Figure 3.11 : After liftoff ReRAM

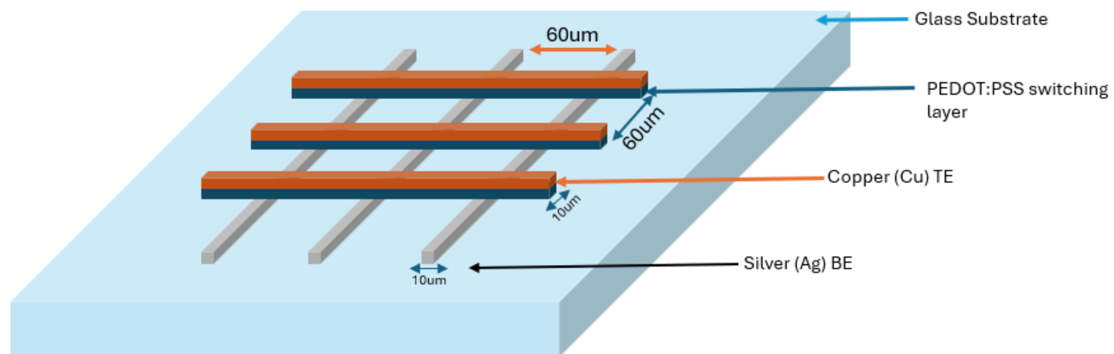


Figure 3.12 : ReRAM Array with coarse X coarse pattern with the width of bottom electrodes, switching layer and top electrodes as 10um and distance between the layers as 60um

A 70 nm layer of copper (Cu) was deposited by thermal evaporation directly onto the PEDOT: PSS-coated and resist-patterned substrate, as shown in Figure 3.10. This completed the stack of the top electrode over the switching layer.

Lift-off was then performed using acetone, which simultaneously removed the unwanted photoresist, excess PEDOT: PSS, and copper, as shown in Figure 3.11. This ensured that only the regions defined by the mask retained the Cu/PEDOT: PSS stack, forming the active MIM junctions above the bottom electrodes. The final device structure is shown in Figure 3.12.

3.3 Optical Microscopy of Fabricated Devices

To verify the pattern fidelity and alignment accuracy of the fabricated ReRAM crossbar arrays, all devices were inspected under the optical microscope after each major lithography step. The images below highlight key structural features such as electrode definition, layer coverage, and mask alignment.

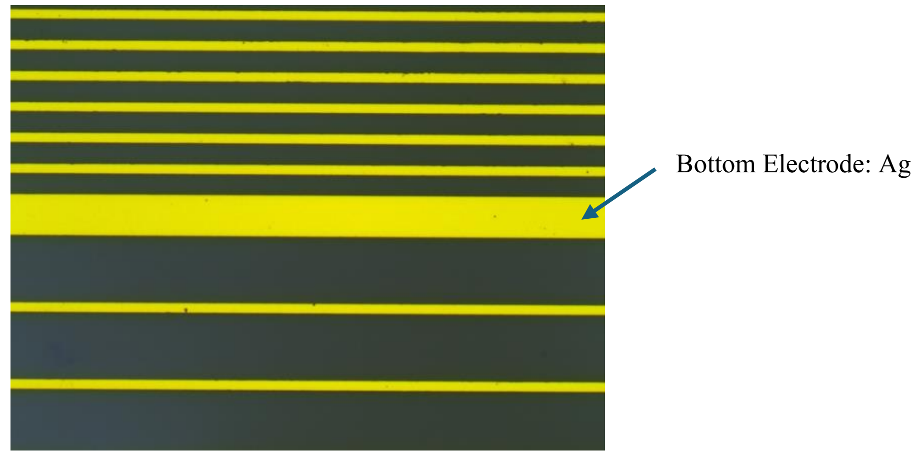


Figure 3.13: Optical microscope image of the bottom Ag Electrodes

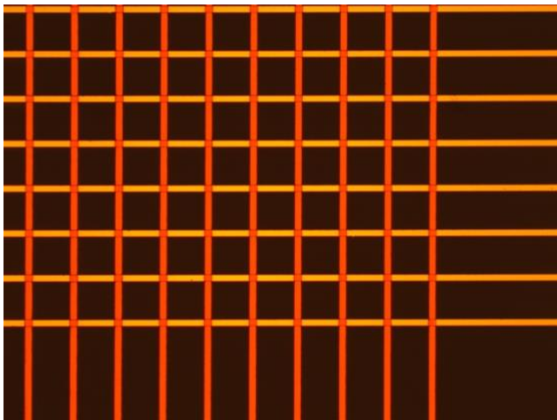


Figure 3.14 (a): Edge1 of the crossbar array

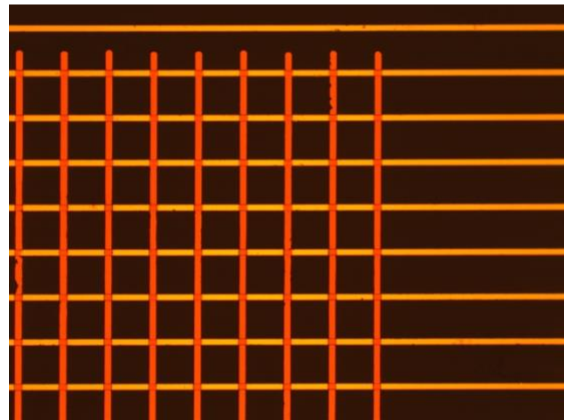


Figure 3.14 (b): Edge2 of the crossbar array

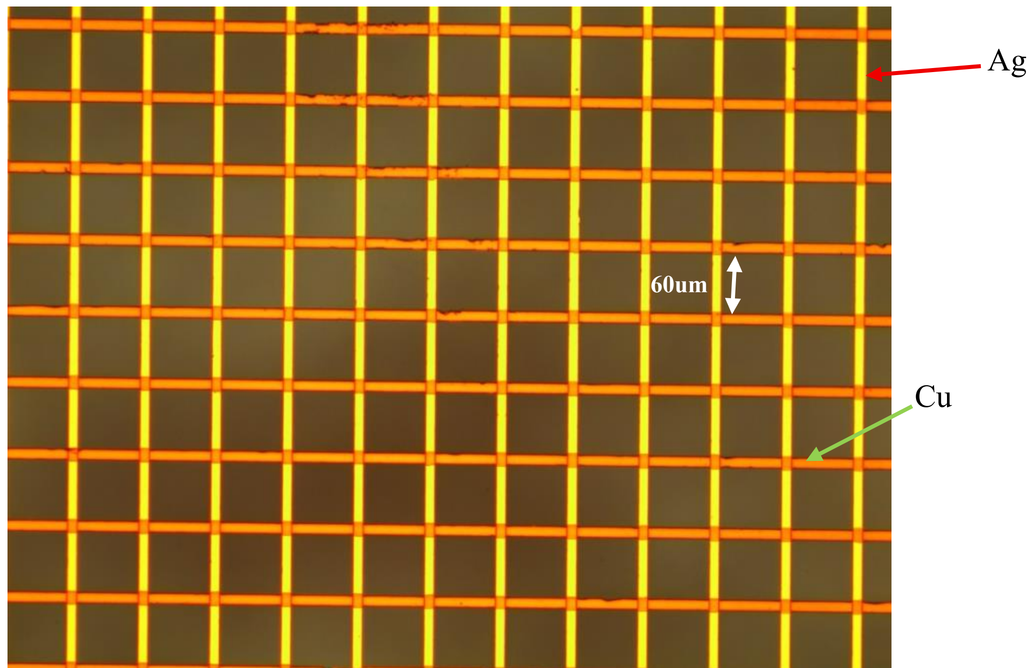


Figure 3.15: Crossbar Array with the structure: Top Electrode Copper (Cu), Resistive Switching Layer is PEDOT: PSS, Bottom Electrode Layer Silver (Ag)

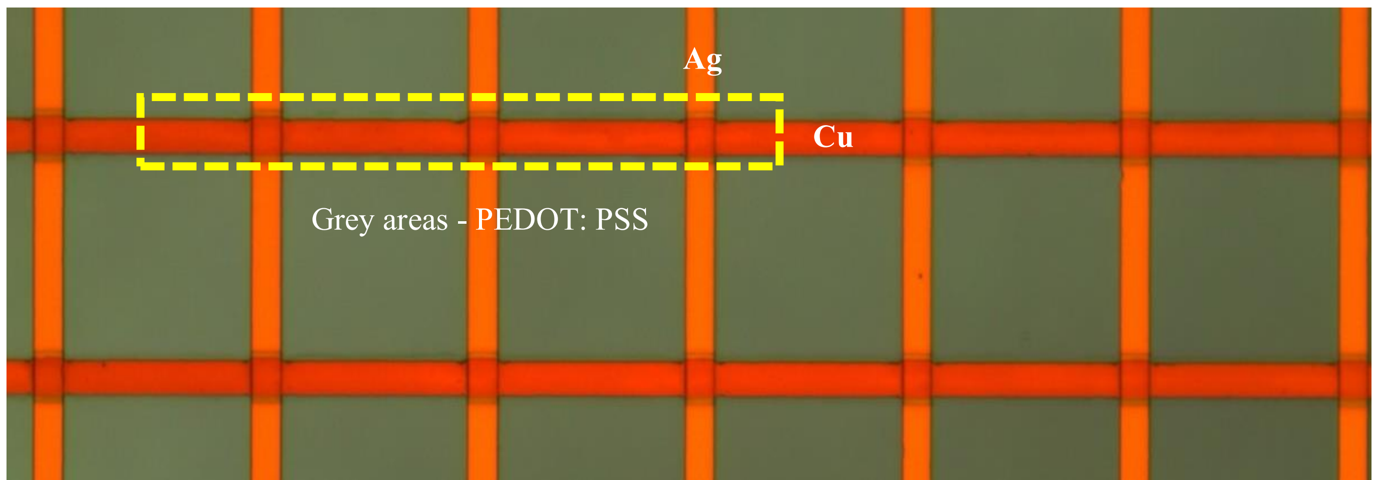
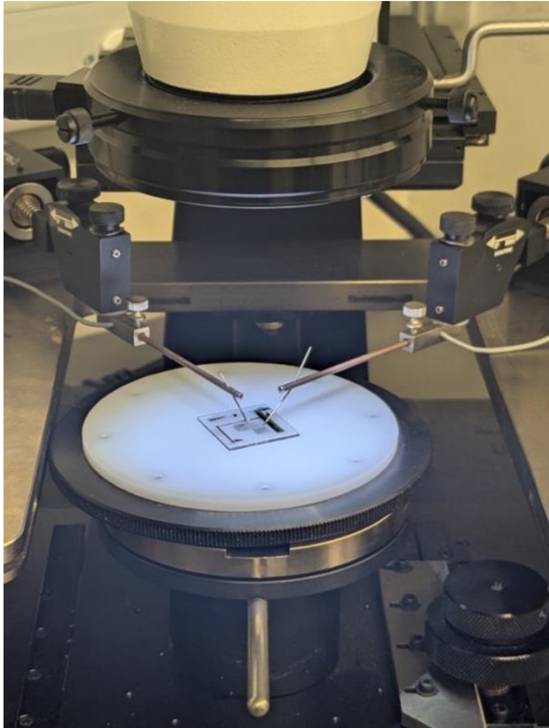


Figure 3.16: The visible grey extensions beyond the edges of the copper lines confirm that the switching layer (PEDOT: PSS) was selectively patterned only beneath the top electrodes

CHAPTER 4: ELECTRICAL CHARACTERIZATION OF ReRAM ARRAYS

4.1 Testing Setup

The electrical testing of ReRAM arrays was carried out using the Keithley 4200-SCS Semiconductor Characterization System connected to a manual probe station. Microscopic probes were used to contact the top and bottom electrodes of the array cells. This setup allowed us to apply voltage and measure current across selected crosspoints. All tests were performed at room temperature under normal lab conditions. The system was used to conduct various types of tests discussed in the upcoming sections, including cycling tests, endurance measurements, sneak path current characterization through hysteresis, and pre-sweep conditioning followed by hysteresis loop evaluation. This setup provided a reliable and repeatable way to study the electrical behavior of different ReRAM cells in the array.



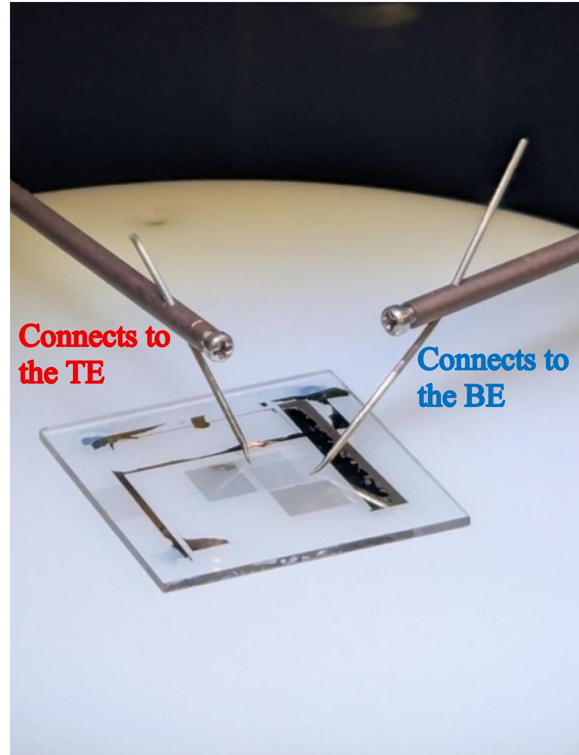


Figure 4.1 Testing setup. Electrical characterization setup using a Keithley characterization system integrated with a microscope-assisted probe station. Tungsten probe tips are precisely positioned on the top and bottom electrodes of the fabricated ReRAM crossbar array to perform accurate I–V measurements and resistance state analysis.

4.2 Cycling Tests

Cycling tests are performed to evaluate the reliability and switching stability of ReRAM cells over repeated operations. In this section, ReRAM crossbar arrays are subjected to repeated voltage sweeps from −2 V to +2 V until device performance begins to degrade. Each subsection presents results for individual devices across different array sizes.

4.2.1 Hysteresis Loops

To evaluate the switching behavior of ReRAM cells, I–V hysteresis loops were recorded at various cycle points during endurance testing. These loops provide insight into the set/reset dynamics, resistance window stability, and any early signs of degradation.

The I–V curves of all tested devices show a typical bipolar resistive switching behavior:

- When a positive bias is applied to the top electrode (Cu), the device switches from a high resistance state (HRS) to a low resistance state (LRS) and this is the SET process.
- Applying a negative voltage reverses the switching, breaking the conductive filament and returning the device to HRS — the RESET process.

Each I–V plot shows a sharp current increase at the SET voltage and a drop during RESET, with a pronounced hysteresis loop.

Cell #1

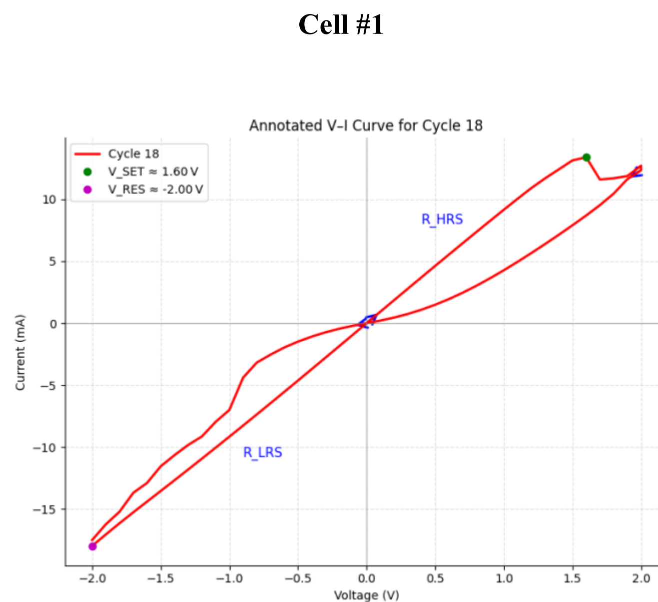


Figure 4.2 (a): I-V Characteristics of cell #1 Cycle 18

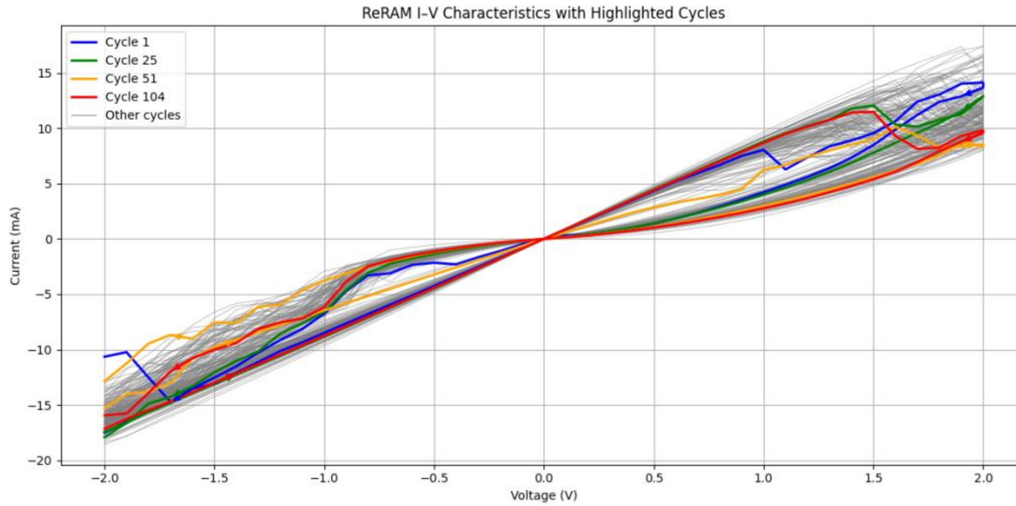


Figure 4.2 (b): ReRAM cell #1 for 104 Cycles

- ReRAM Device 2, with top electrode 4 and bottom electrode 5, was tested over a voltage range of (−2 V to +2 V) until its I–V characteristics showed signs of significant degradation.
- The device maintained stable performance up to 104 cycles. The blue curve represents cycle 1, the green curve corresponds to cycle 25, the orange curve corresponds to cycle 51, and the red indicates cycle 104.

Cell # 2

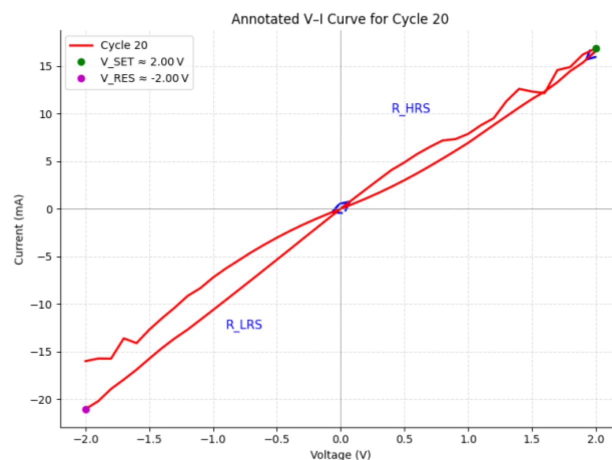


Figure 4.3 (a): I-V Characteristics of Cell #2

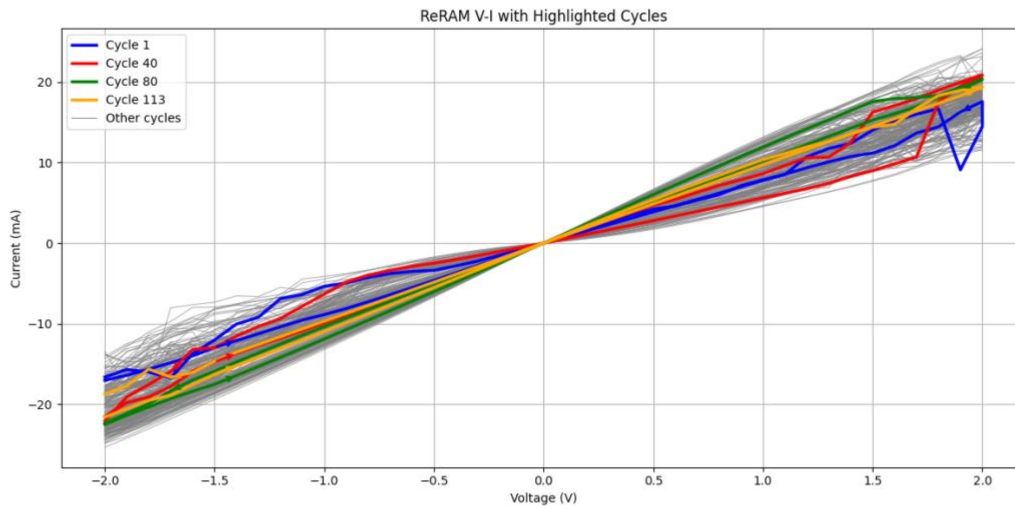


Figure 4.3 (b): ReRAM cell #2 for 113 Cycles

- ReRAM Device 2, with top electrode 2 and bottom electrode 2, was tested over a voltage range of (−2 V to +2 V) until it's I–V characteristics showed signs of degradation.
- The device maintained stable performance up to 113 cycles. The blue curve represents cycle 1, the red curve represents cycle 40, the green curve represents cycle 80 and the orange corresponds to cycle 113.

Cell #3

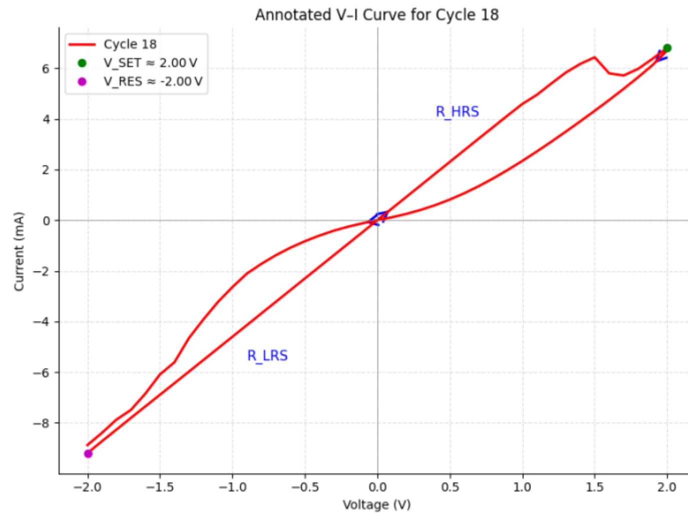


Figure 4.4 (a): I-V Characteristics of Cell #3

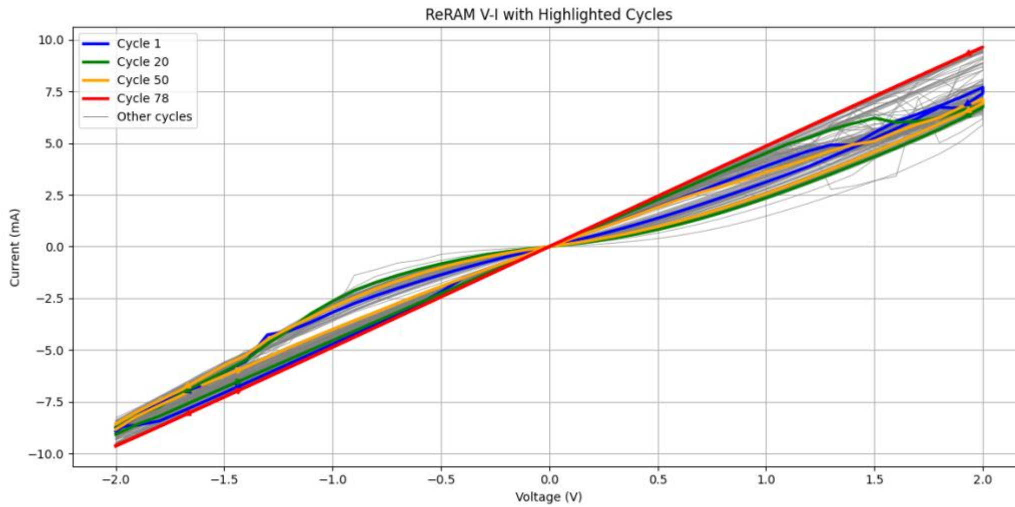


Figure 4.4 (b): ReRAM Cell #3 for 78 Cycles

- ReRAM Device 2, with top electrode 2 and bottom electrode 2, was tested over a voltage range of (−2 V to +2 V) until it's I–V characteristics showed signs of degradation.

- The device maintained stable performance up to 78 cycles. The blue curve represents cycle 1, the green curve represents cycle 20, the orange corresponds to cycle 50, and the red indicates cycle78.

Cell #4

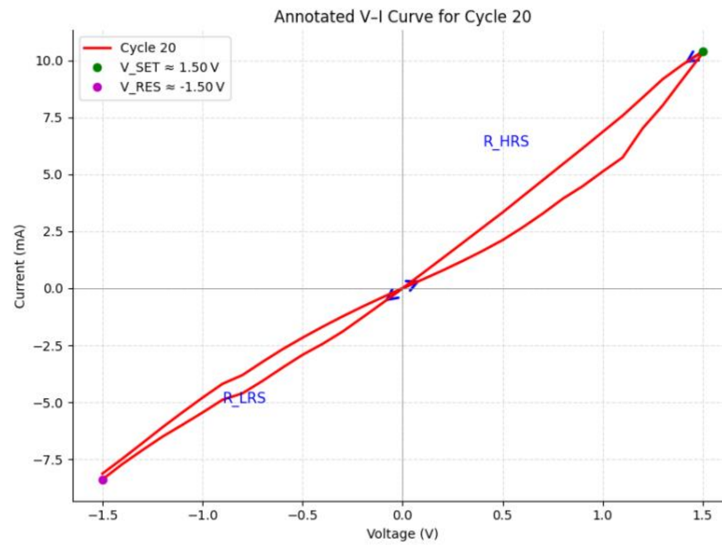


Figure 4.5 (a): I-V Characteristics of Cell #4

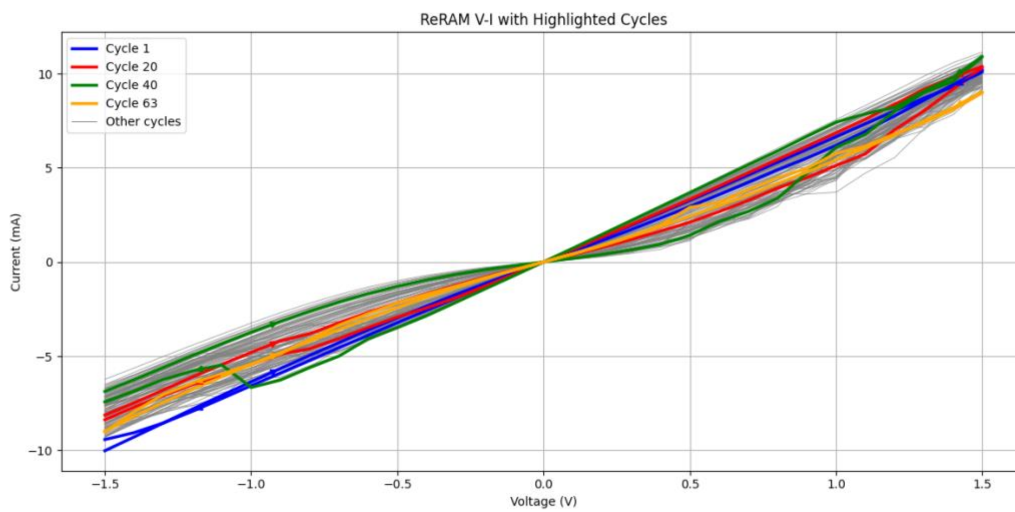


Figure 4.5 (b): ReRAM Cell #4 for 63 Cycles

- ReRAM Device 2, with top electrode 2 and bottom electrode 2, was tested over a voltage range of (−2 V to +2 V) until it's I–V characteristics showed signs of degradation.
- The device maintained stable performance up to 63 cycles. The blue curve represents cycle 1, the red curve represents cycle 20, the green curve represents cycle 40 and the orange corresponds to cycle 63.

Cell #5

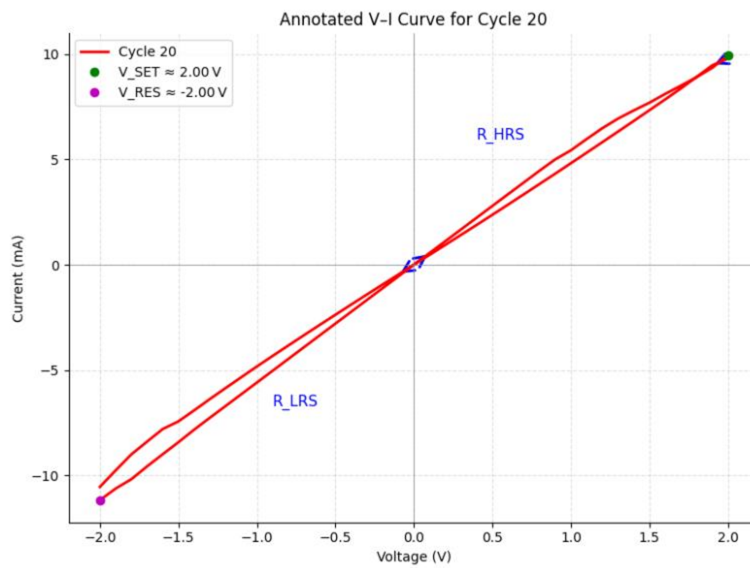


Figure 4.6 (a): I-V Characteristics of Cell #5

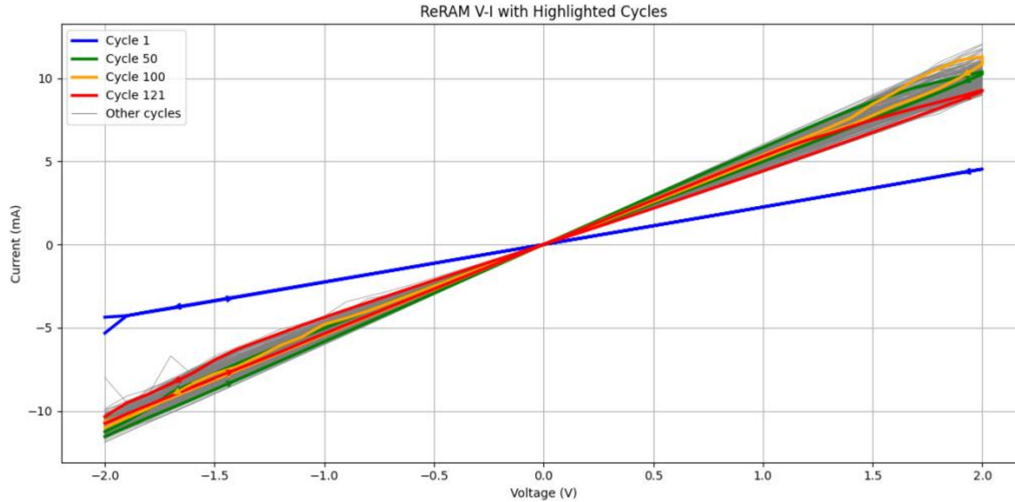


Figure 4.6 (b): ReRAM Cell #5 for 121 Cycles

- ReRAM Device 2, with top electrode 2 and bottom electrode 2, was tested over a voltage range of (−2 V to +2 V) until it's I–V characteristics showed signs of degradation.
- The device maintained stable performance up to 121 cycles. The blue curve represents cycle 1, the green curve represents cycle 50, the orange curve represents cycle 100 and the red corresponds to cycle 121.

Table 4. 1 Summary of Cycling Test

Memory cell #	# of completed cycles
1	104
2	113
3	78
4	63
5	121

4.2.2 Endurance

Endurance is defined as the ability of a ReRAM device to reliably undergo repeated switching between the high resistance state (HRS) and low resistance state (LRS) without significant degradation. This section presents the endurance characteristics of various ReRAM arrays by analyzing the stability of resistance states and switching voltages across multiple cycles.

Cell #1

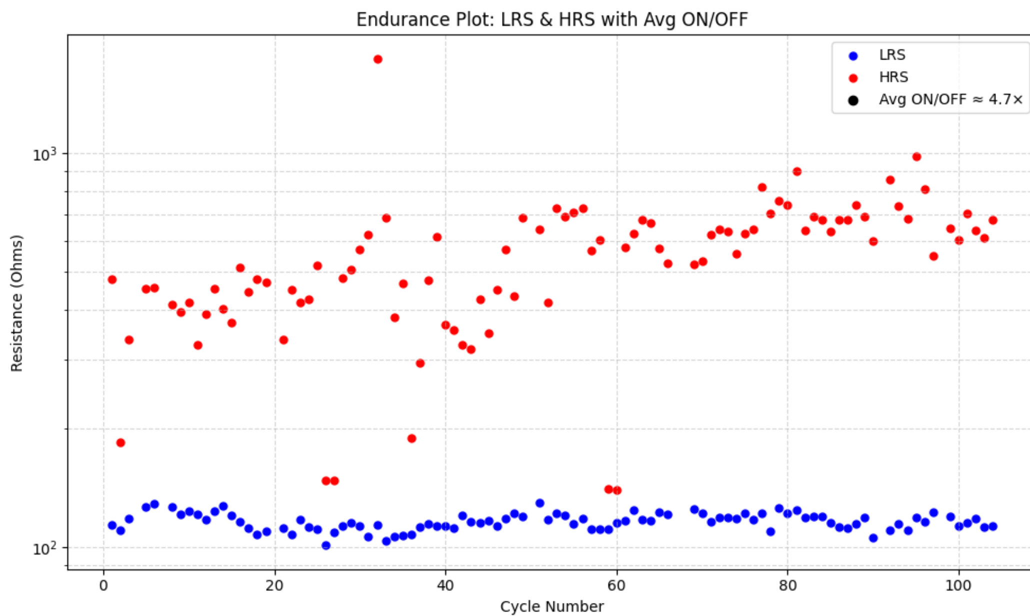


Figure 4.7 (a): LRS, HRS Endurance of 104 Cycles

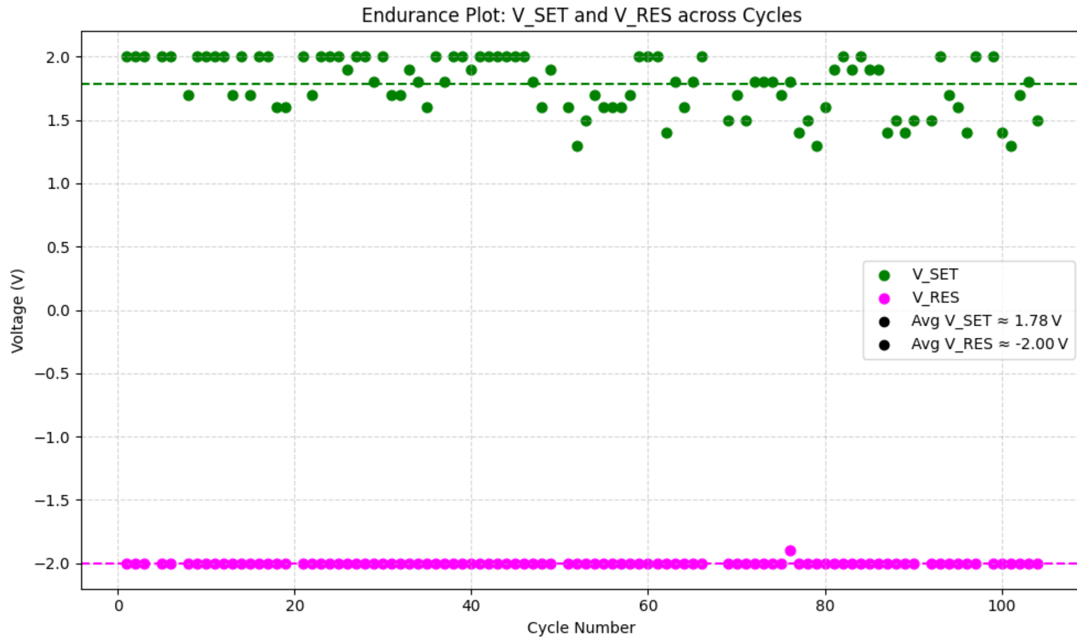


Figure 4.7 (b): Average set and reset voltages across 104 Cycles

- The above figure shows stable LRS and HRS values of 104 cycles with a voltage range of (-2v, +2v) with an average ON/OFF ratio being 4.7x

Cell #2

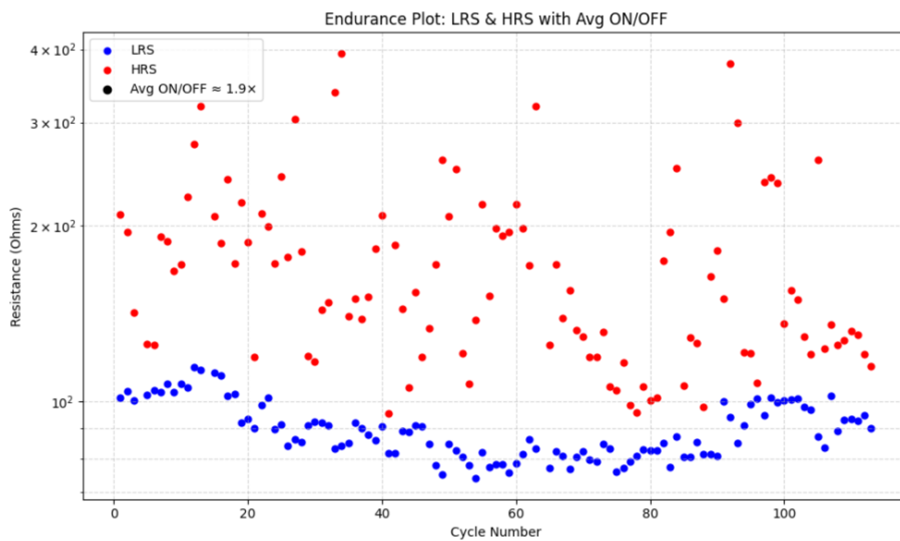


Figure 4.8 (a): LRS, HRS Endurance of 113 Cycles

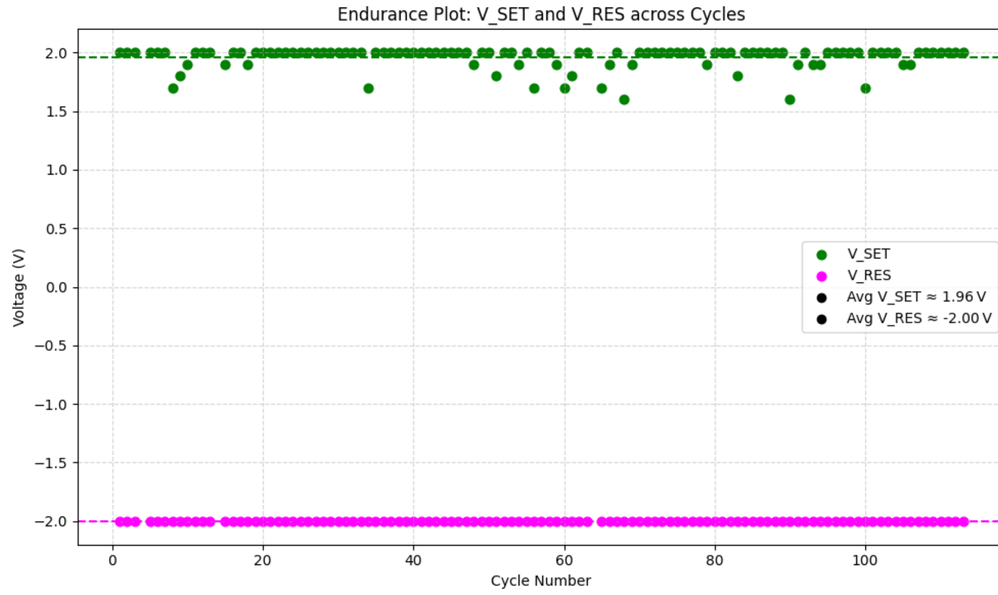


Figure 4.8 (b): Average set and reset voltages across 113 Cycles

- The above figure shows stable LRS and HRS values of 113 cycles with a voltage range of (-2v, +2v) with an average ON/OFF ratio being 1.9x

Cell #3

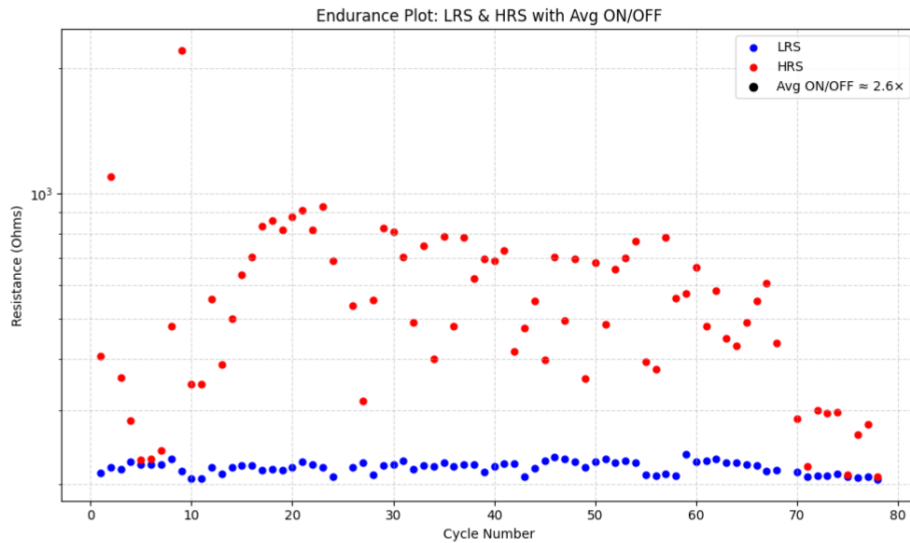


Figure 4.9 (a): LRS, HRS Endurance of 78 Cycles

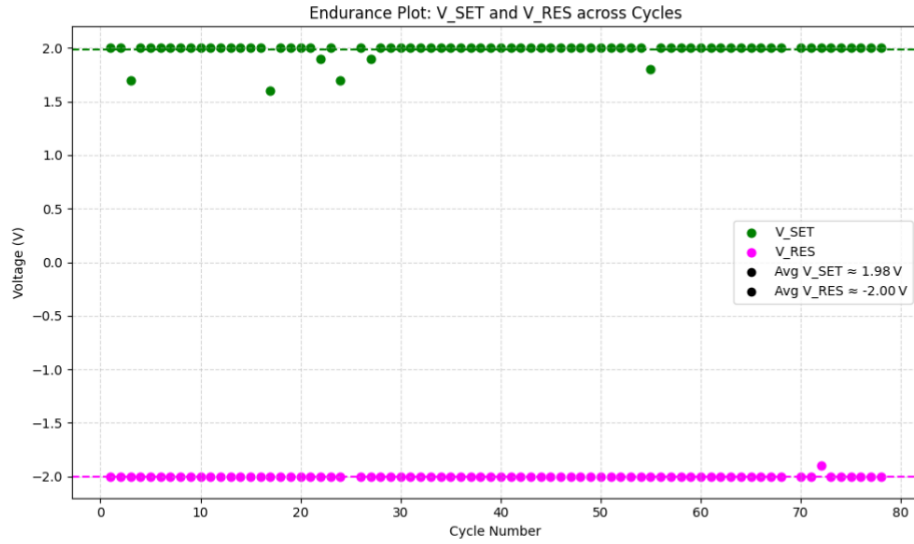


Figure 4.9 (b): Average set and reset voltages across 78 Cycles

- The above figure shows stable LRS and HRS values of 78 cycles with a voltage range of (-2v, +2v) with an average ON/OFF ratio being 2.6x

Cell #4

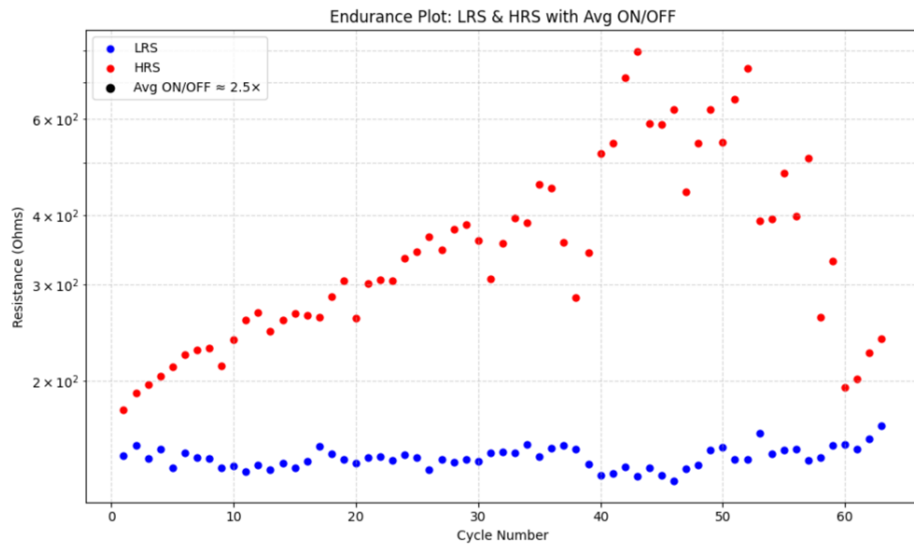


Figure 4.10 (a): LRS, HRS Endurance of 63 Cycles

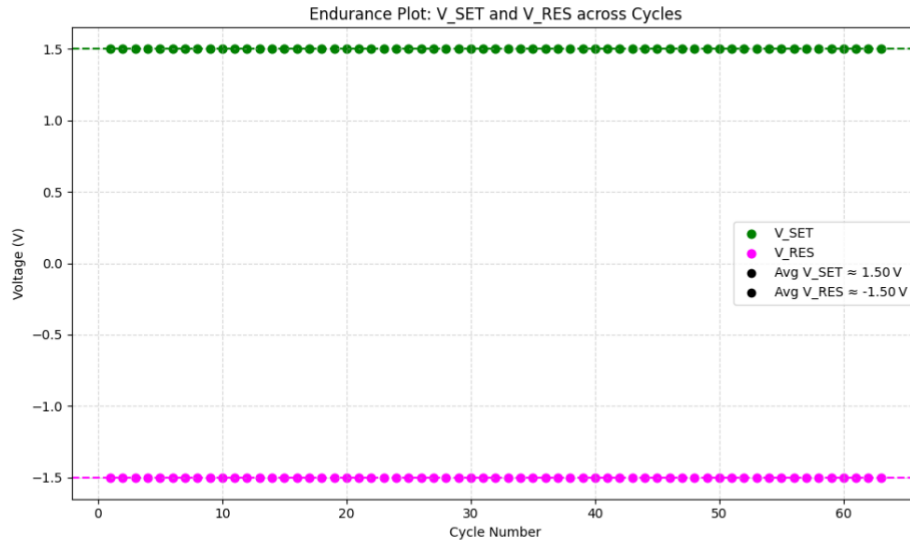


Figure 4.10 (b): Average set and reset voltages across 63 Cycles

- The above figure shows stable LRS and HRS values of 63 cycles with a voltage range of (-2v, +2v) with an average ON/OFF ratio being 2.5x

Cell #5

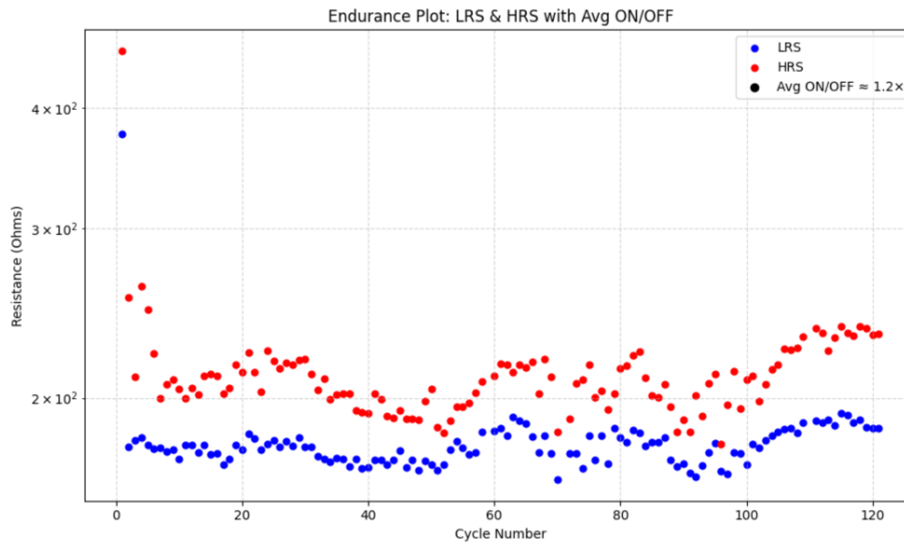


Figure 4.11 (a): LRS, HRS Endurance of 121 Cycles

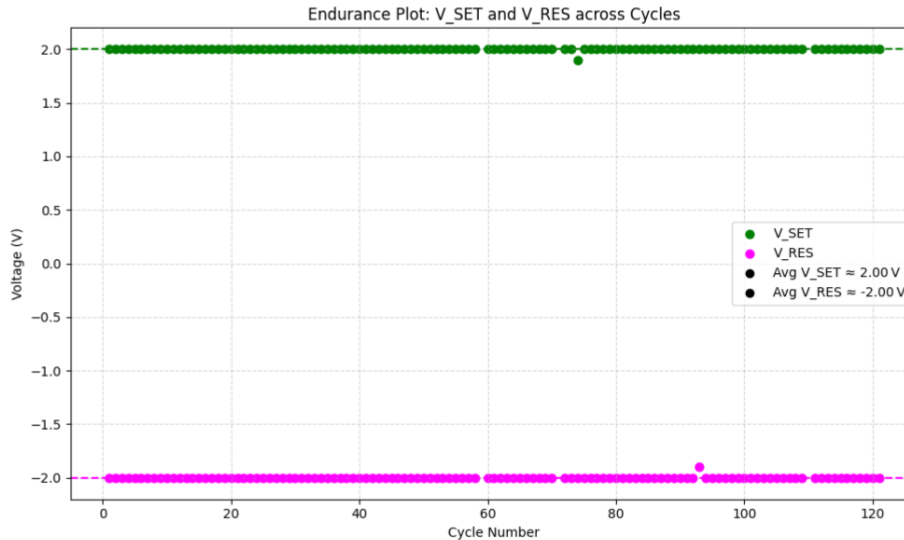


Figure 4.11 (b): Average set and reset voltages across 121 Cycles

- The above figure shows stable LRS and HRS values of 121 cycles with a voltage range of (-2v, +2v) with an average ON/OFF ratio being 1.2x

4.3 Characterization of Sneak Path Current Behavior through hysteresis

Sneak path currents are unintended leakage currents that flow through unselected cells in passive ReRAM crossbar arrays, often interfering with accurate read or write operations. These currents can induce false switching events and distort the hysteresis response of neighboring cells, particularly during low- to mid-range voltage operations.

To investigate this behavior, a progressive voltage sweep protocol was designed. The testing sequence began with an initial ±2 V sweep to establish baseline switching behavior. This was followed by a series of narrow-range voltage sweeps from ±0.5 V to ±1.9 V, increasing in 0.1 V steps. Each sweep range was applied for 5 cycles, allowing the device to experience partial

biasing that could condition or perturb nearby cells. The sequence concluded with another ±2 V sweep to determine whether any changes in switching characteristics had occurred due to earlier low-voltage exposure.

The I–V responses at ±0.5 V and ±0.6 V showed linear behavior with no signs of resistive switching, confirming that these voltages were below the device's switching threshold. However, at ±0.7 V, slight increases in current were observed, and by ±0.8 V, well-formed hysteresis loops began to emerge. This indicates that sneak-path-assisted switching is likely initiated near 0.8 V**.** As the voltage increased, the switching loops became more defined, and by the final ±2 V sweep, the original hysteresis behavior was largely impacted. This experiment demonstrates that even sub-threshold voltages, when applied cumulatively or sequentially, can trigger sneak paths that alter the device's electrical response. Identifying this threshold is crucial for designing reliable ReRAM arrays and preventing false reads or unintended switching.

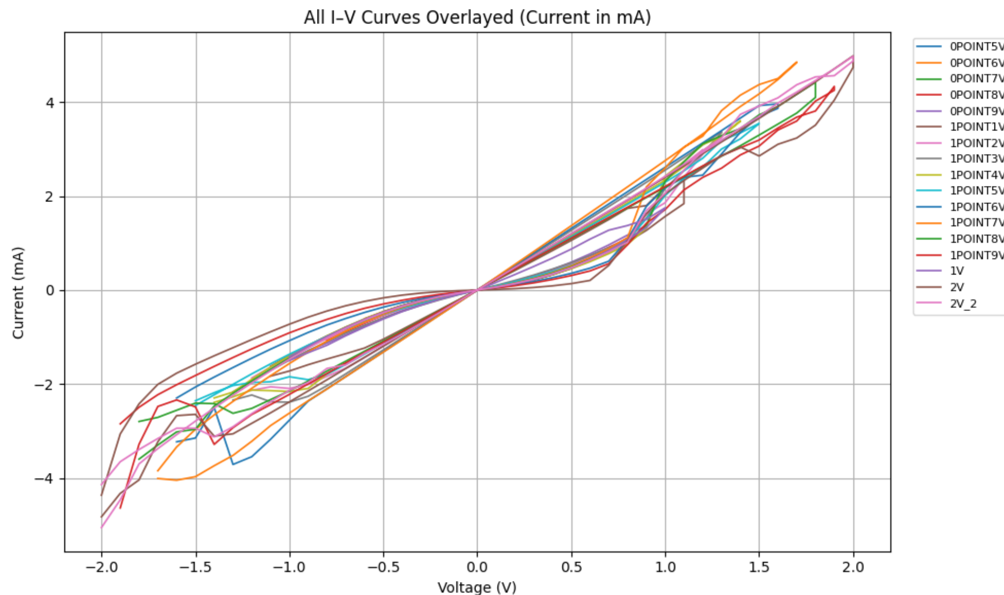
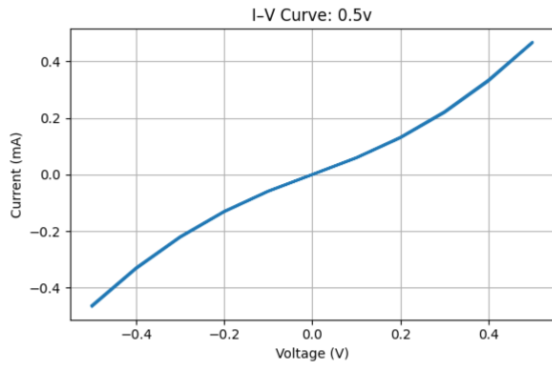
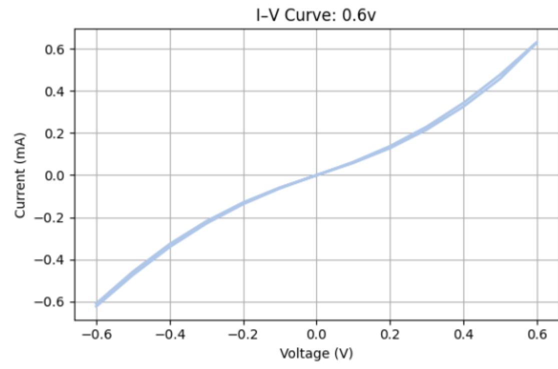


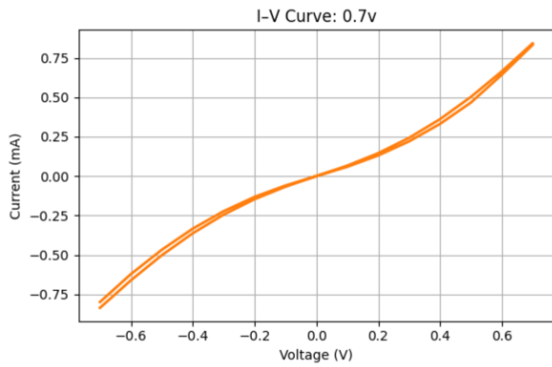
Figure 4.12: Overlay of I–V Characteristics Across Voltage Sweeps



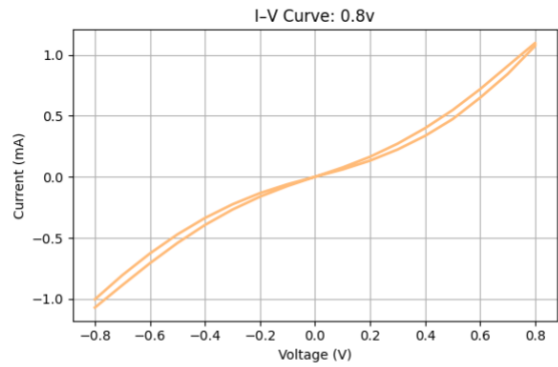
(a)



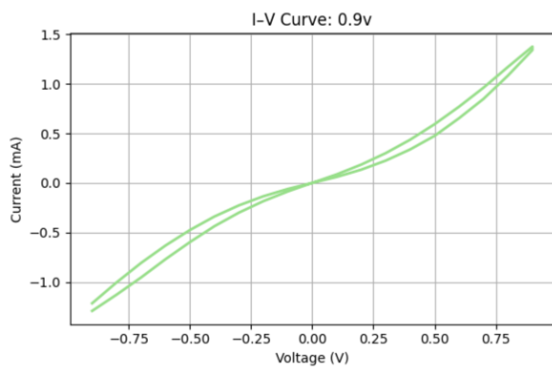
(b)



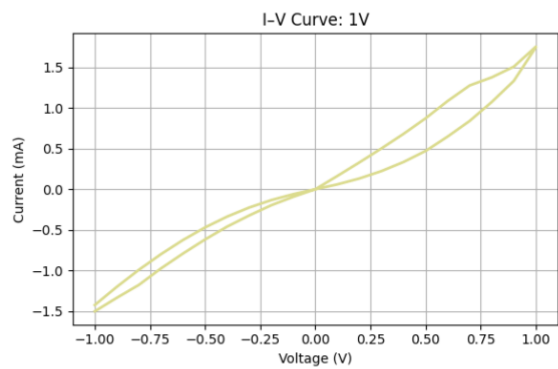
(c)



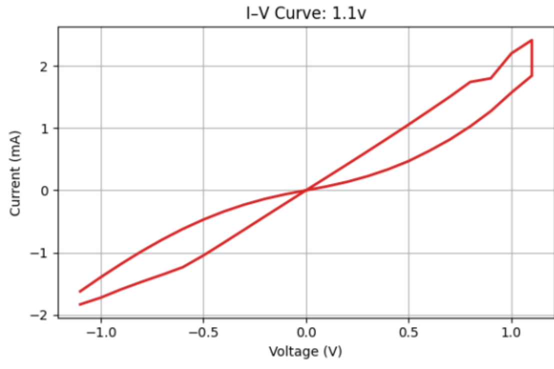
(d)



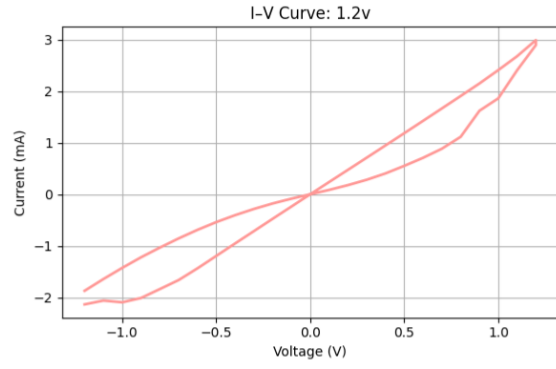
(e)



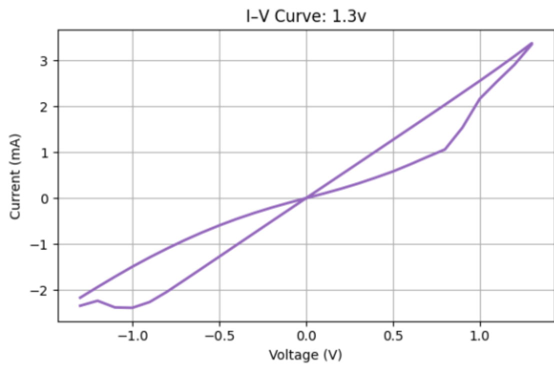
(f)



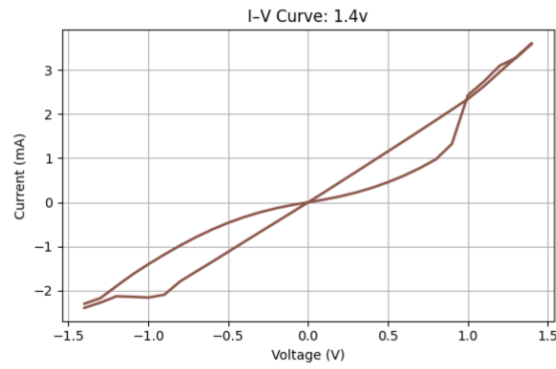
(g)



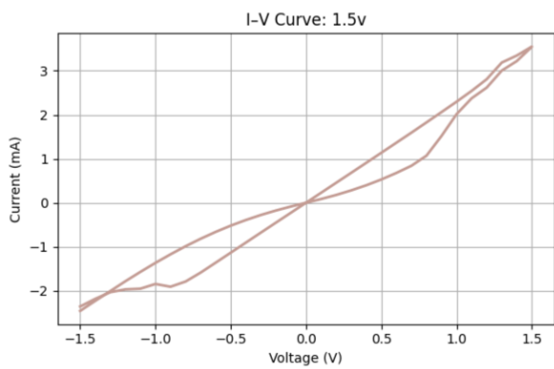
(h)



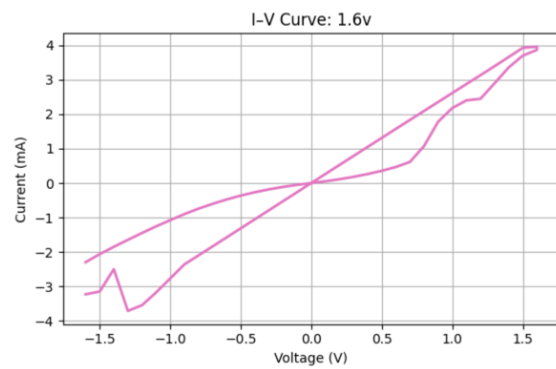
(i)



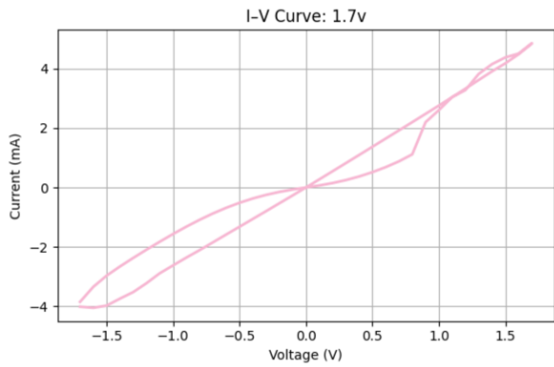
(j)

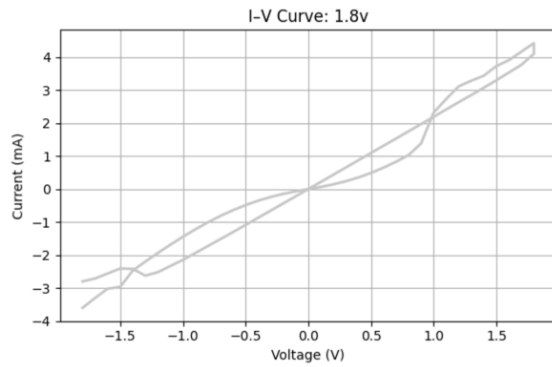


(k)



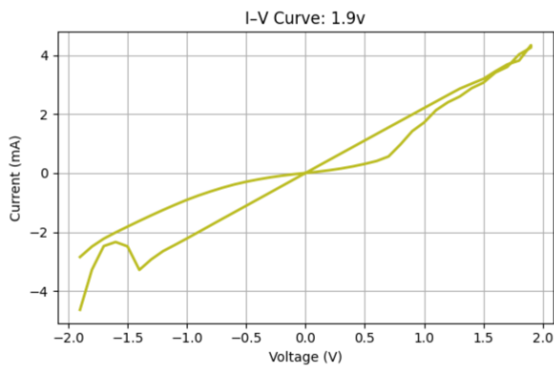
(l)

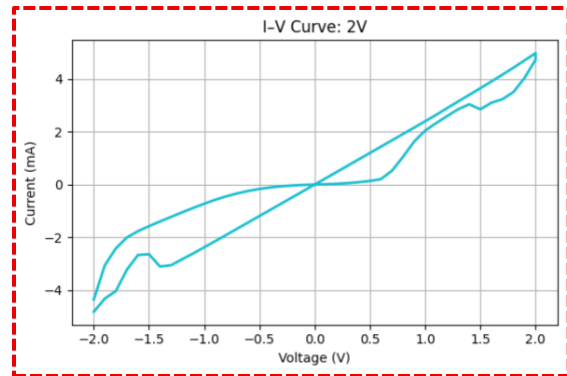




(m)

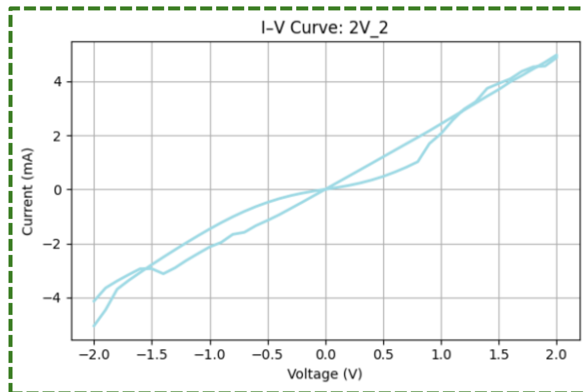
(n)





(o)

(p)



(q)

Figure 4.13 (a)-(o) I–V curves from ±0.5 V to ±1.9 V (one figure per voltage step), (p) First full ±2 V sweep (before low sweeps), (q) Second full ±2 V sweep (after low sweeps)

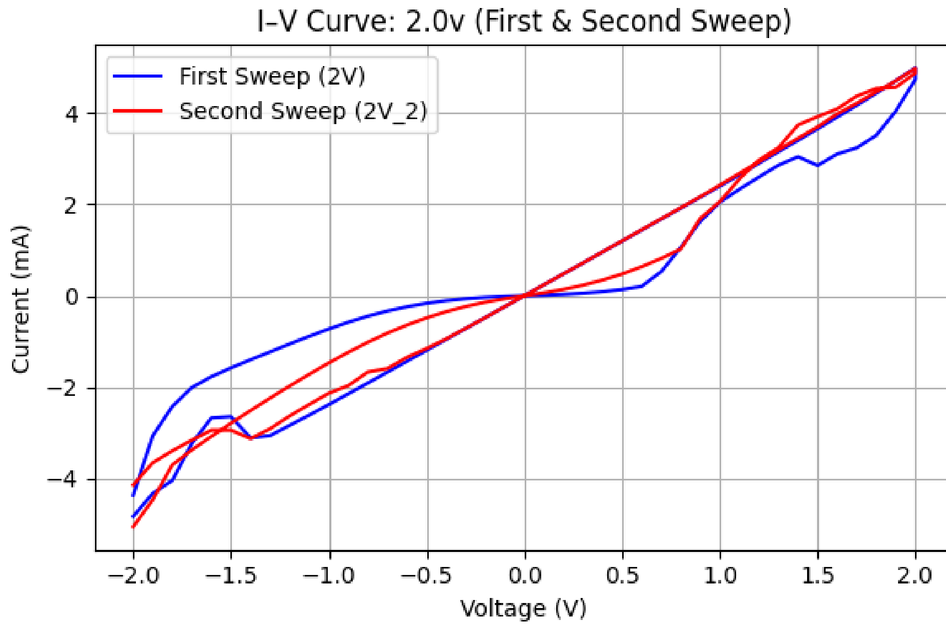


Figure 4.14 Hysteresis I-V loop comparison of first full ±2 V sweep (before low sweeps), second full ±2 V sweep (after low sweeps). The shift in loop shape and the reduced hysteresis area in the second sweep indicate possible partial filament formation or modification induced by prior low-voltage biasing, consistent with sneak-path current effects. The decrease in loop area further signifies the device's reduced ability to retain its resistive state for longer durations, suggesting degradation in memory stability.

Table 4.2: LRS, HRS, ILRS, IHRS, and Voltage Range

Voltage (V)	LRS (ohms)	HRS (ohms)	ILRS (mA)	IHRS (mA)
2	526.28	3655.36	-3.230	0.137
0.5	1074.24	1072.71	0.465	-0.466
0.6	953.48	963.49	0.629	-0.623
0.7	830.08	838.22	0.843	-0.835
0.8	830.90	747.25	0.842	-1.071
0.9	653.97	696.58	1.376	-1.292
1	549.02	1343.60	1.275	0.223
1.1	459.88	1185.58	1.740	0.337
1.2	418.93	562.41	2.148	-2.134
1.3	391.65	419.03	2.553	-2.386
1.4	437.31	513.89	0.457	-2.141
1.5	496.64	636.50	2.014	-2.357
1.6	505.15	350.17	1.782	-3.712
1.7	384.41	1341.42	2.601	0.149
1.8	402.20	495.51	3.729	-2.624
1.9	548.27	426.15	-3.283	-3.285
2	486.38	1050.51	-3.701	0.476

This table summarizes key switching metrics extracted from each sweep. The highlighted rows (first and second ±2 V) show how resistance states and current levels evolve before and after the progressive low-voltage sweeps, indicating the influence of sneak-path conditioning. The last ±2 V full sweep shows a **71.26 % lower HRS** and a **7.58 % lower LRS** compared to the initial ±2 V full sweep.

4.4 Effect of Step-Sweep Conditioning on Full ±2 V Switching Characteristics

4.4.1 Objective

Following the sneak-path voltage studies in Section 4.3, an additional experiment was conducted to investigate how partial voltage sweeps of varying magnitude influence the subsequent full ±2 V switching behavior. The key aim was to quantify whether low-voltage preconditioning induces partial filament growth or modifies trap states in a way that alters the hysteresis characteristics when the device is returned to a full sweep.

This test also directly evaluates the magnitude of sneak-path currents and partial switching effects caused by sub-threshold biasing, by comparing each ±2 V sweep only to the most recent ±2 V sweep rather than to the initial state.

4.4.2 Methodology

To prove the effect of partial sweep conditioning, a step-sweep protocol was employed, in which a single device underwent an alternating sequence of:

1. **Partial Sweep:** A narrow voltage sweep with a specific peak value (±0.5 V, ±0.6 V, …, ±1.9 V), applied symmetrically around 0 V.
2. **Full Sweep:** An immediate ±2 V sweep applied to the same cell without intermediate rest or reset.

Data processing:

- LRS and HRS values from each full ±2 V sweep (2 V_n) were compared only to the values from the immediately preceding full sweep (2 V_{n-1}).
- The percentage change in LRS and HRS was calculated to isolate the effect of the intervening partial sweep from cumulative aging effects.
- By structuring the experiment in this way, any difference between 2 V sweeps can be attributed to the preceding partial sweep voltage rather than general cycling degradation.

This methodology mimics real-world array conditions in which unselected cells experience partial bias prior to full programming events, thereby allowing direct assessment of sneak-path conditioning in a controlled, single-device setup.

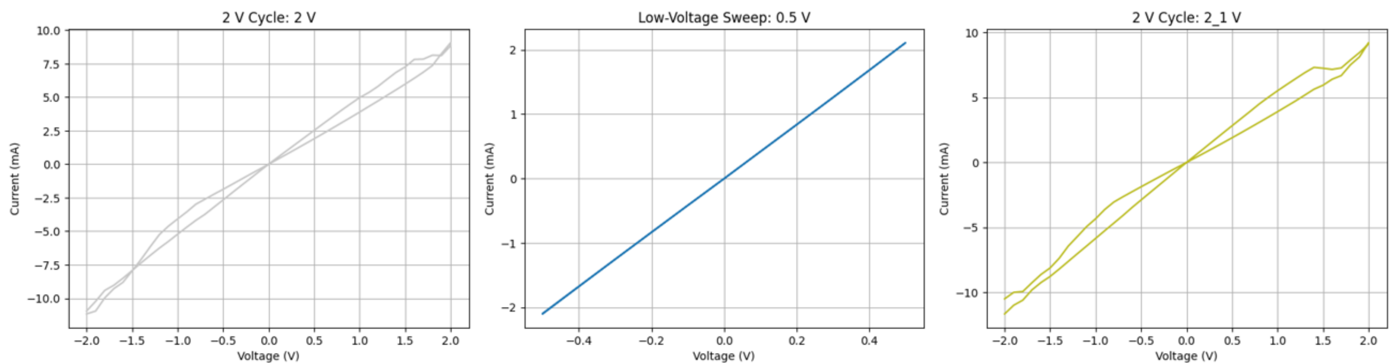


Figure 4.15 *(Left)* First full ±2 V sweep establishing baseline switching. *(Middle)* Narrow ±0.5 V sweep showing purely ohmic behavior with no resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

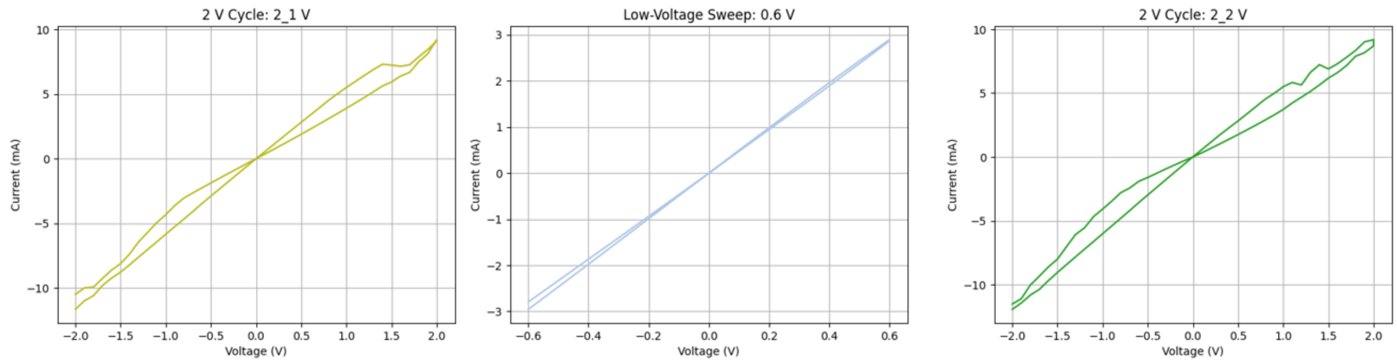


Figure 4.16 *(Left)* First full ±2 V sweep establishing baseline switching. *(Middle)* Narrow ±0.6 V sweep showing linear, ohmic behavior without resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

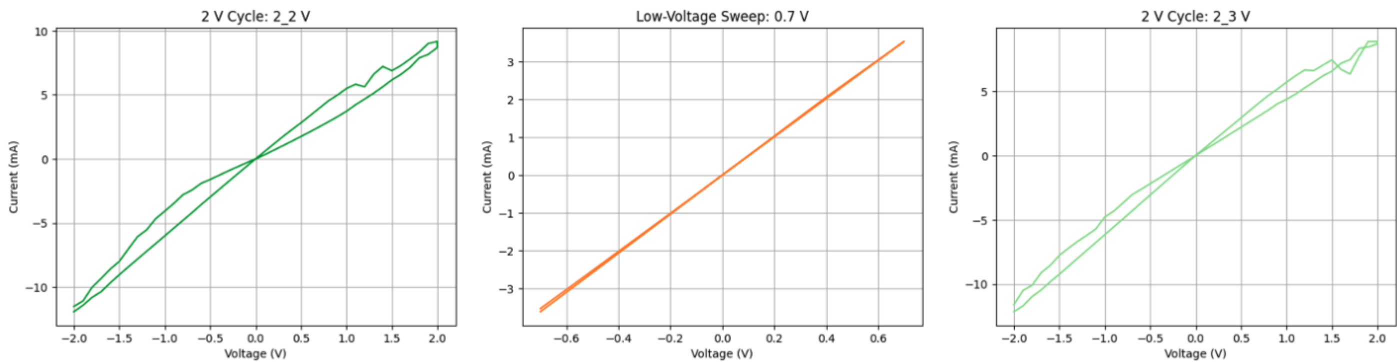


Figure 4.17 *(Left)* First full ±2 V sweep demonstrating baseline switching characteristics. *(Middle)* Narrow ±0.7 V sweep showing ohmic conduction without evidence of switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

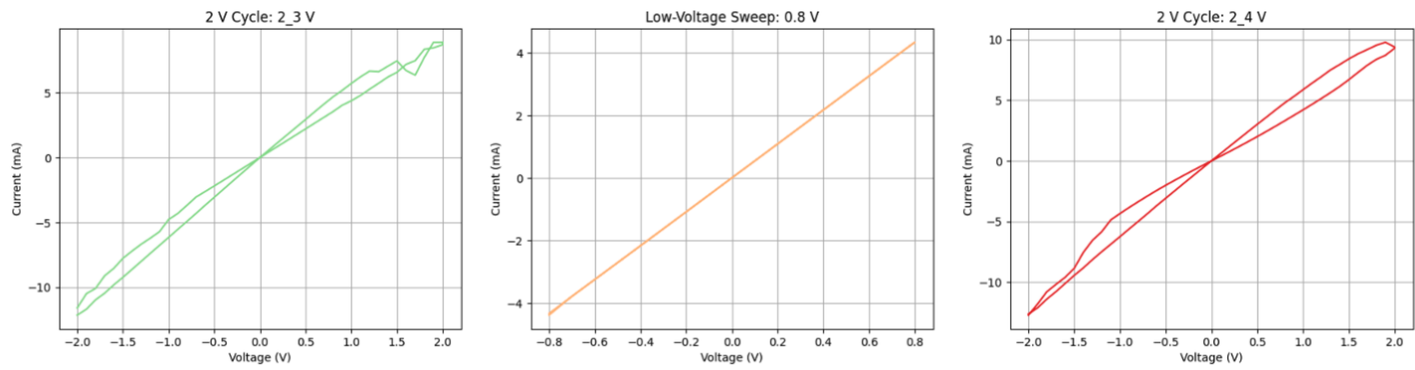


Figure 4.18 *(Left)* First full ±2 V sweep showing baseline switching characteristics. *(Middle)* Narrow ±0.8 V sweep exhibiting a linear, ohmic response with no evidence of resistive switching. *(Right)* Second full ±2 V sweep following low voltage cycling.

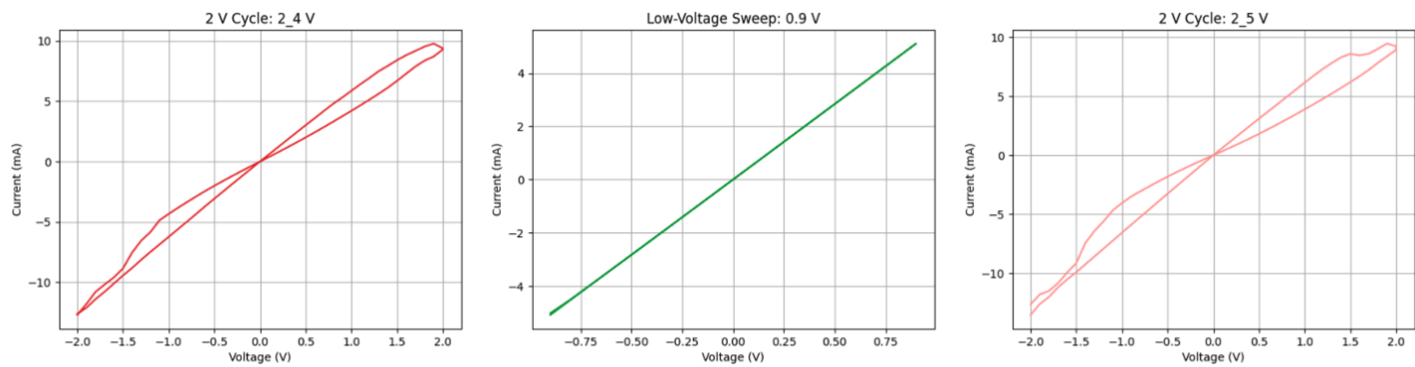


Figure 4.19 *(Left)* First full ±2 V sweep showing baseline switching. *(Middle)* Narrow ±0.9 V sweep with a purely ohmic I–V response, indicating no resistive switching.*(Right)* Second full ±2 V sweep after low-voltage cycling.

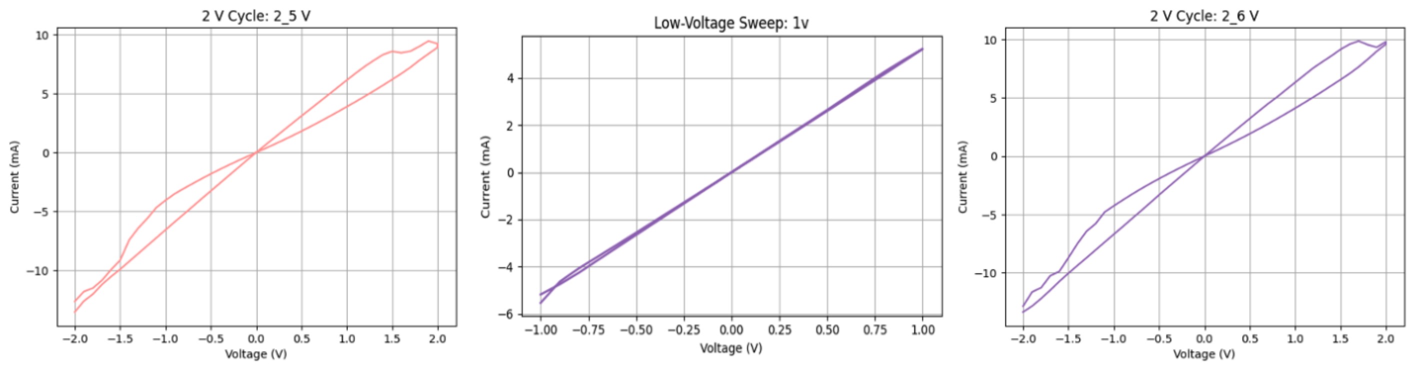


Figure 4.20 *(Left)* First full ±2 V sweep showing baseline switching behavior. *(Middle)* Narrow ±1.0 V sweep displaying a linear, ohmic I–V response without resistive switching. *(Right)* Second full ±2 V sweep after low voltage cycling.

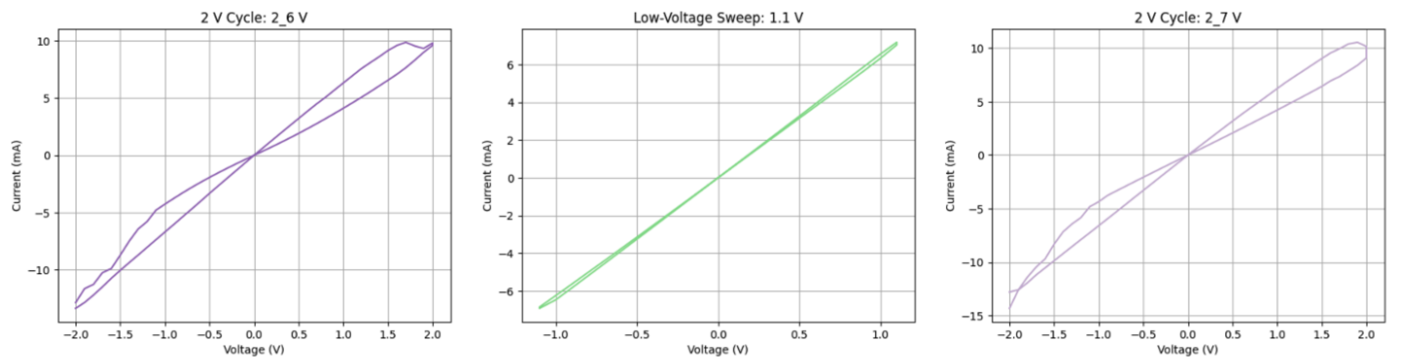


Figure 4.21 (Left) First full ±2 V sweep showing the baseline switching curve. *(Middle)* Narrow ±1.1 V sweep producing an ohmic response with no indication of resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

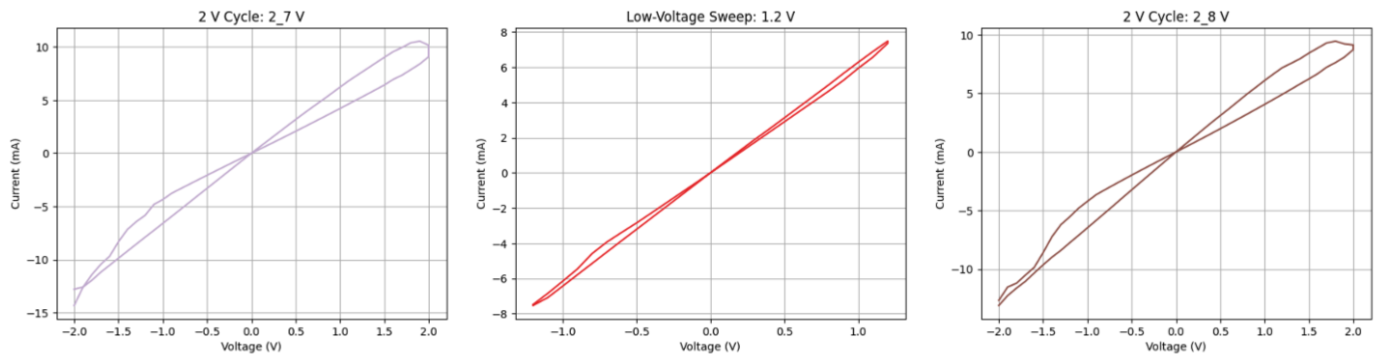


Figure 4.22 *(Left)* First full ±2 V sweep showing baseline switching. *(Middle)* Narrow ±1.2 V sweep exhibiting an almost linear I–V response with minimal switching features. *(Right)* Second full ±2 V sweep after low-voltage cycling.

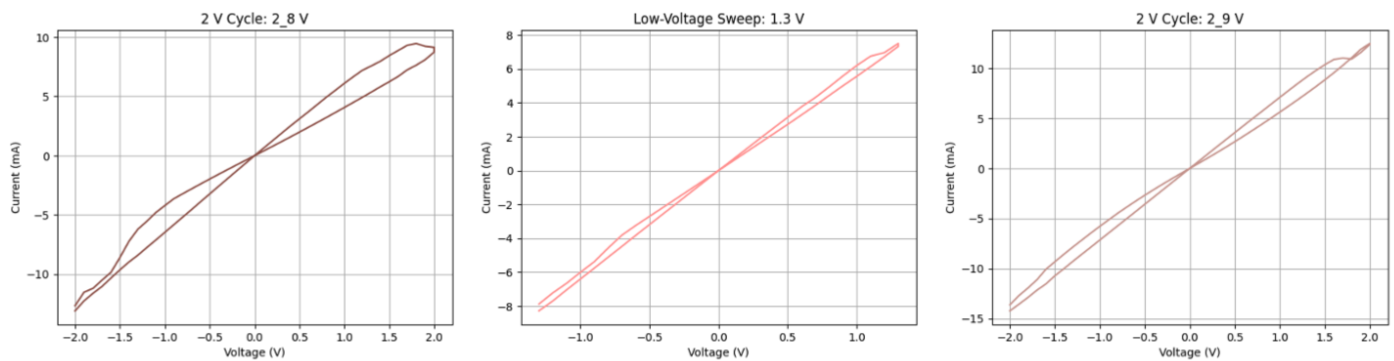


Figure 4.23 *(Left)* First full ±2 V sweep establishing baseline switching. *(Middle)* Narrow ±1.3 V sweep showing a predominantly ohmic I–V profile with minimal switching signatures. *(Right)* Second full ±2 V sweep after low-voltage cycling.

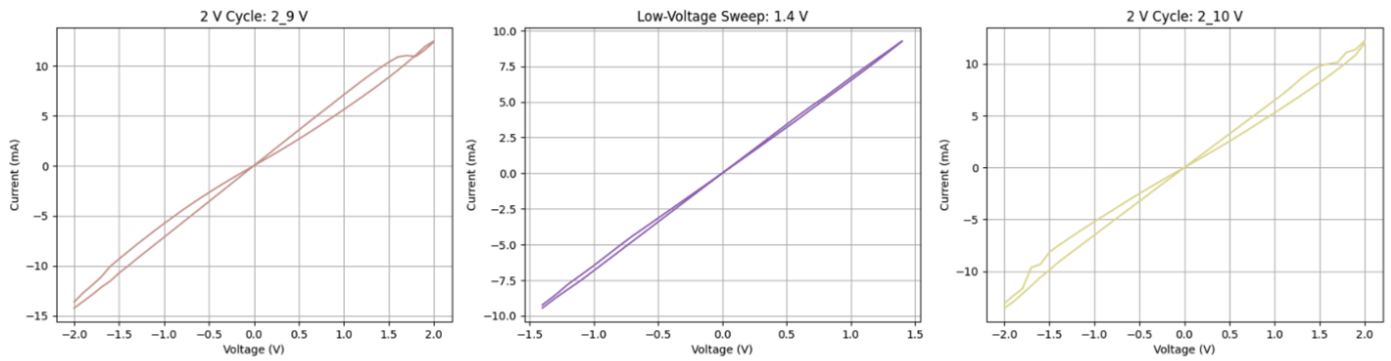


Figure 4.24 *(Left)* First full ±2 V sweep showing the baseline switching response. *(Middle)* Narrow ±1.4 V sweep producing a linear I–V curve indicative of ohmic conduction with no resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

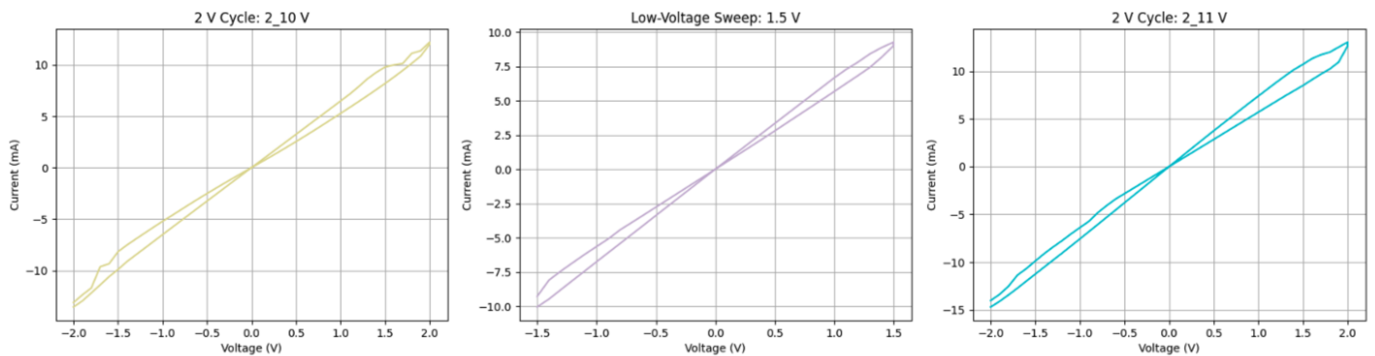


Figure 4.25 *(Left)* First full ±2 V sweep showing baseline switching characteristics. *(Middle)* Narrow ±1.5 V sweep with a predominantly linear I–V response, indicating minimal resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

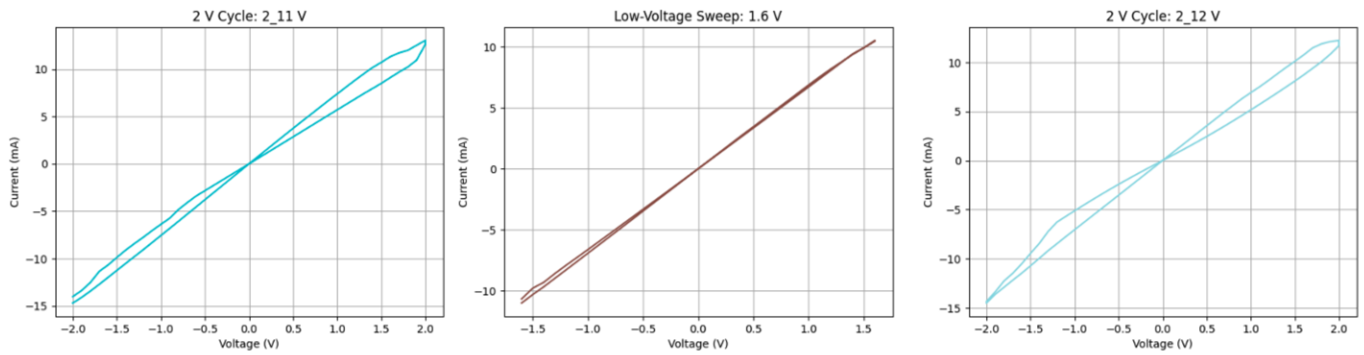


Figure 4.26 *(Left)* First full ±2 V sweep showing baseline switching response. *(Middle)* Narrow ±1.6 V sweep producing a mostly linear I–V curve, indicating limited resistive switching activity. *(Right)* Second full ±2 V sweep after low-voltage cycling.

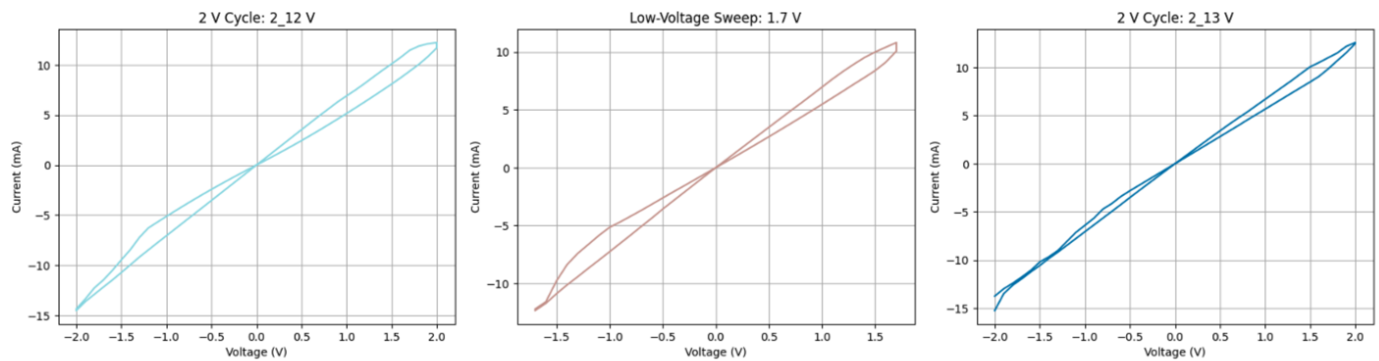


Figure 4.27 (Left) First full ±2 V sweep showing baseline switching characteristics. *(Middle)* Narrow ±1.7 V sweep with a near-linear I–V curve, indicating minimal resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

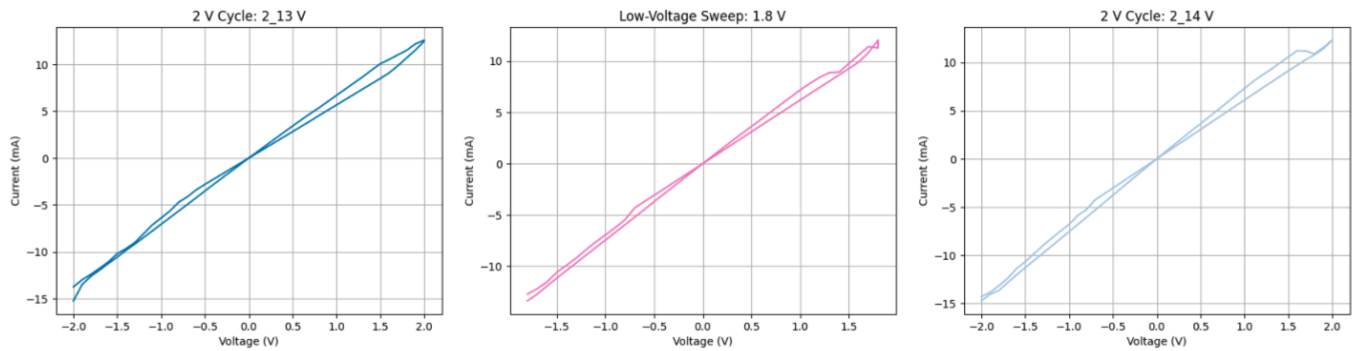


Figure 4.28 (Left) First full ±2 V sweep showing the baseline switching curve. *(Middle)* Narrow ±1.8 V sweep producing a mostly linear I–V response with minimal switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

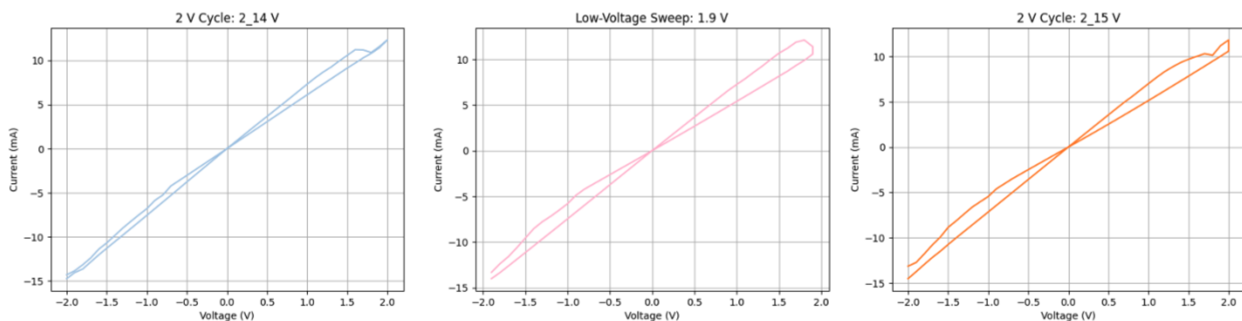


Figure 4. 29 (Left) First full ±2 V sweep showing baseline switching characteristics. *(Middle)* Narrow ±1.9 V sweep displaying a mostly linear I–V curve with minimal signs of resistive switching. *(Right)* Second full ±2 V sweep after low-voltage cycling.

4.4.3 Results

The data reveal three distinct behaviors across the step-sweep series:

(a) Low-voltage region (±0.5 V to ±0.8 V)

- LRS changes were small (<~8%), indicating limited influence on conductive filament cross-section.
- HRS exhibited modest increases (up to ~12%), consistent with slight reinforcement of the OFF state due to insufficient activation of conductive pathways.

(b) Mid-voltage region (±0.9 V to ±1.3 V)

- Both LRS and HRS changes became more pronounced.
- Large negative HRS shifts occurred at certain steps (e.g., −22.96% at 2 V_2→2 V_3, −24.85% at 2 V_8→2 V_9), suggesting partial reconnection of residual filaments during the narrow sweep.
- These drops in HRS point to increased leakage or inadvertent filament bridging caused by mid-range partial sweeps.

(c) High-voltage region (±1.4 V to ±1.9 V)

- LRS fluctuations were more significant, including an +8.69% recovery at 2 V_{14}→2 V_{15}.
- HRS shifts alternated between increases and decreases, indicating an unstable balance between filament rupture and re-growth.
- By the final sweep (2 V_{16}), both states had degraded substantially compared to the baseline — LRS by **−24.26%** and HRS by **−27.91%**.

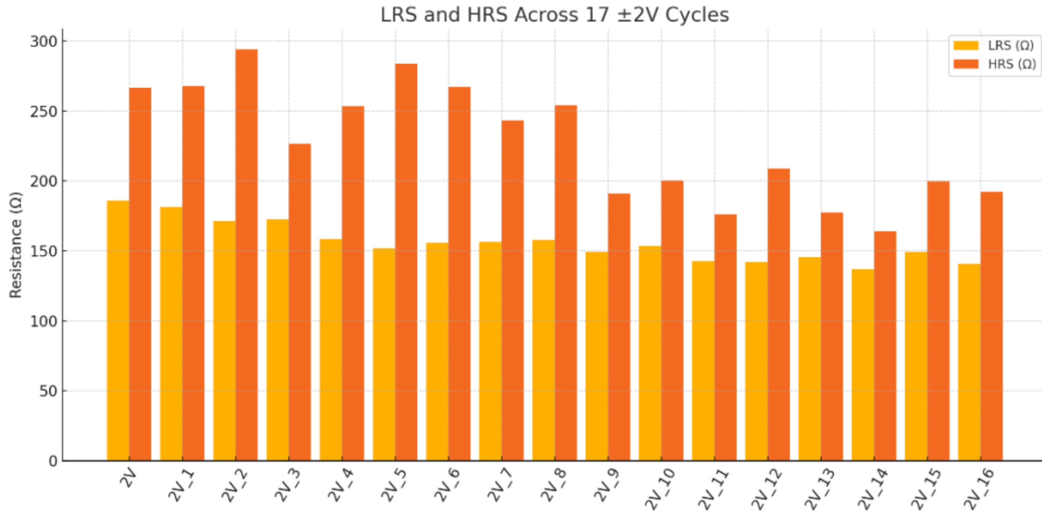


Figure 4.30 Slope-based LRS and HRS across 17 consecutives ±2 V sweeps. A noticeable decline in the HRS/LRS ratio emerges after cycle 9, indicating a reduced read margin driven by LRS rising and/or HRS falling in later cycles, i.e., onset of degradation beyond cycle 9.

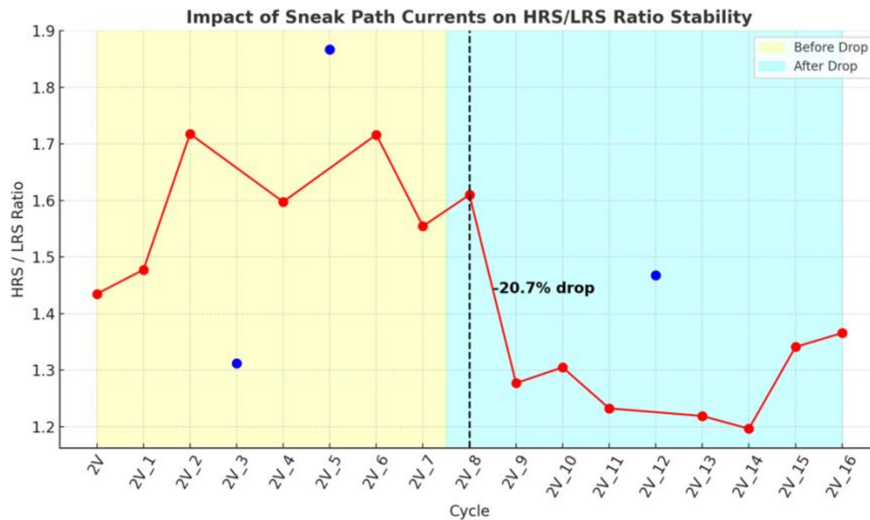


Figure 4.31 Variation of HRS/LRS ratio across 17 consecutive ±2 V sweeps. A sharp 20.7% drop in the ratio occurs after cycle 9, marking the onset of significant degradation, likely influenced by sneak-path current effects. The yellow zone represents stable operation before the drop, while the blue zone indicates degraded stability after the drop.

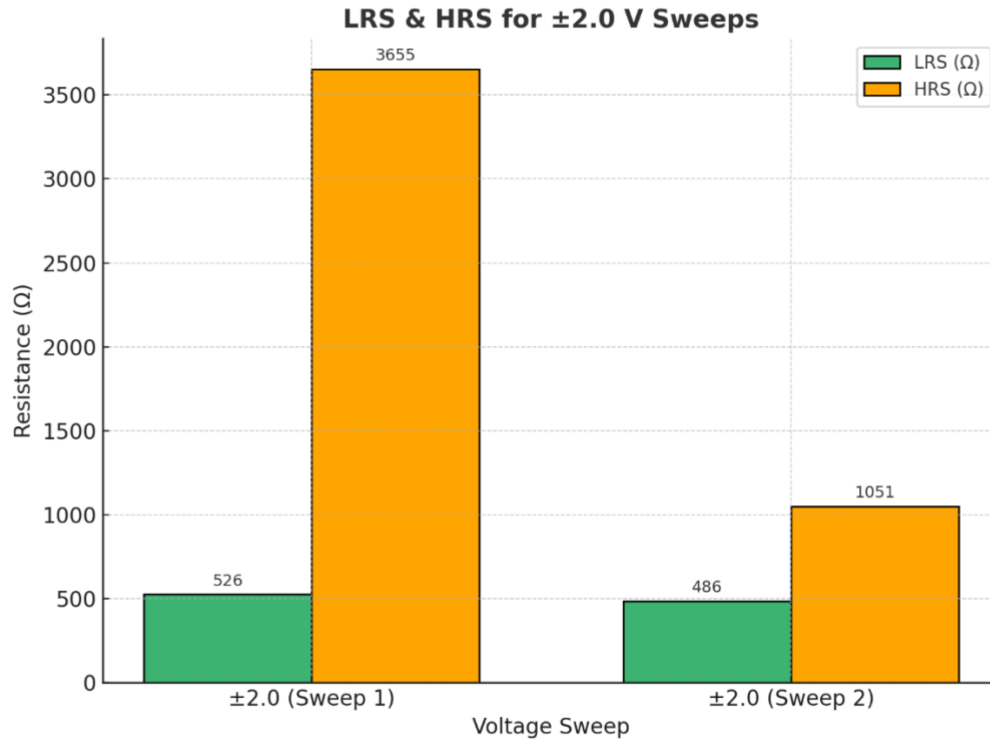


Figure 4.32 Comparison of LRS and HRS values between the first and second ±2.0 V sweeps. The second sweep shows a drop in HRS from 3655 Ω to 1051 Ω and a slight reduction in LRS from 526 Ω to 486 Ω, indicating a significant narrowing of the resistance window after low-voltage cycling.

4.5 Mathematical Modeling of Sneak Path Influence via Current Density Analysis

In the previous sections, we demonstrated that sneak-path currents can arise even in optimized ReRAM architectures when subjected to narrow voltage sweeps. Although structural enhancements—such as placing the conductive resistive switching layer (RSL) directly beneath the top electrode—help suppress lateral leakage, parasitic currents may still affect the read

operation. To gain a deeper understanding and guide further device-level design improvements, we developed a mathematical model to relate current density to the distance between electrodes**.**

4.5.1 Motivation and Design Tradeoff

Our goal was to quantify how the geometric spacing between electrodes influences the current density and, consequently, the magnitude of sneak-path interference. By calculating theoretical current density values at different voltages and distances, we were able to determine the thresholds at which sneak currents significantly influence the measured read current.

We observed that when the inter-electrode distance was 60 µm, the threshold current density ($J_{threshold}$) at 1.1 V was approximately 501 µA/µm², which was high enough to influence the read operation at 2 V. This indicated a critical current density threshold above which sneak-paths could distort sensing accuracy.

To reduce sneak-path influence at 1.1 V, either the spacing between the electrodes should be increased or the voltage ranges should be carefully tuned, thereby reducing the corresponding $J_{threshold}$ to the threshold.

Current Density Modeling in ReRAM Structures

Two complementary models were used to examine the influence of **spacing** and **voltage** on current density relative to a defined sneak-path threshold (500.91 µA/µm²):

1. **Fixed Voltage Model (V = 1.1 V) – Current Density vs. Spacing**

   At a constant bias of 1.1 V, the current density decreases non-linearly with increasing electrode spacing. For small spacings (d < 60 μm), the current density remains above the threshold (black curve), indicating a high probability of sneak-path interference. Increasing the spacing beyond this point (red curve) reduces current density below the threshold, minimizing interference.

2. **Fixed Spacing Model (d = 60 μm) – Current Density vs. Voltage**

   With spacing fixed at 60 μm, the current density scales linearly with applied voltage. At low voltages (V < 1.1 V), the density remains below the threshold (red curve), but higher voltages push it above threshold (black curve), creating conditions for sneak-path currents.

Key Insight:

While **increasing spacing** at a fixed voltage can effectively suppress sneak-path currents, **reducing voltage** at a fixed spacing can achieve the same outcome. The models thus provide dual strategies—geometric design or bias control—for maintaining current densities below the interference threshold.

4.5.2 Theoretical Calculation of Current Density

The theoretical model uses Ohm's law context because the sneak-path currents observed in ReRAM crossbar arrays are predominantly ohmic in nature. These currents typically arise from leakage through unselected or partially active cells, which do not undergo full resistive switching. As a result, the current-voltage (I–V) relationship across these paths remains largely linear within the sub-threshold voltage range, where no filamentary switching takes place.

In contrast, the actual resistive switching behavior of selected ReRAM cells is non-linear, governed by complex filament formation and rupture mechanisms that depend on factors such as field strength, thermal effects, and ion migration. These non-linear effects dominate only when the applied voltage surpasses a specific threshold required to induce a SET or RESET event.
Since sneak paths operate below this threshold, the devices along these unintended routes remain in their high-resistance state (HRS) and exhibit a linear, resistive conduction profile.

Therefore, Ohm's law $J = \frac{V}{\rho \cdot d}$ provides a valid and accurate approximation to model and analyze the influence of these unwanted currents on the readout process. It allows for a simplified, yet physically meaningful, estimation of current densities and helps establish design tradeoffs such as optimal electrode spacing to minimize sneak-path interference. To quantify the relationship between current density and the distance between electrodes, we begin with the basic relation from Ohm's law:

$$R = \rho \cdot \frac{d}{A}$$

where,

- R is the resistance (Ω)
- ρ is the resistivity of the PEDOT: PSS material (Ω·cm)
- d is the distance between electrodes (60 μm)
- A is the cross-sectional area = width of the top electrode × thickness of the PEDOT: PSS layer.

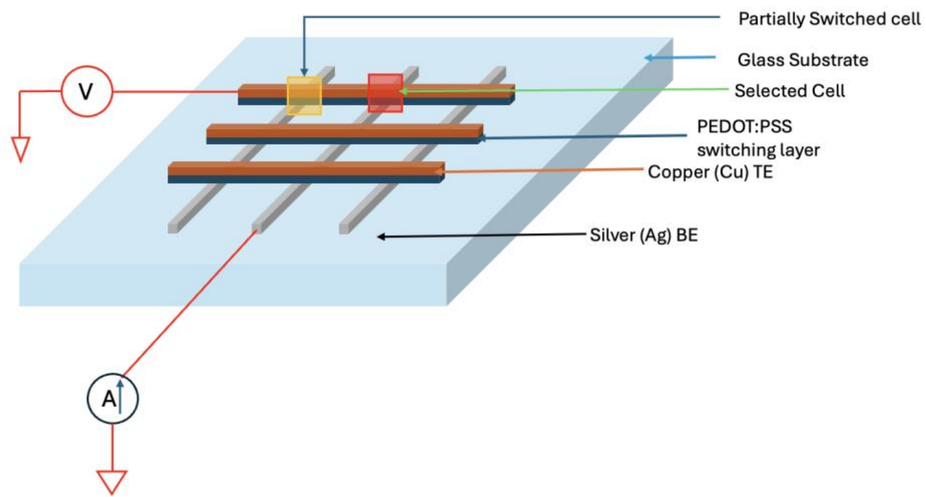


Figure 4.33 Schematic of a crossbar ReRAM array with electrical probing setup. The device is built on a glass substrate, with bottom electrodes (BEs) made of silver (Ag) and top electrodes (TEs) made of copper (Cu). The active switching layer consists of PEDOT:PSS, deposited between the TE and BE. The figure shows a selected memory cell at the intersection of orthogonal electrodes, where voltage (V) is applied across the TE and current (I) is measured through the BE using an ammeter. This configuration allows for I–V characterization of individual ReRAM cells.

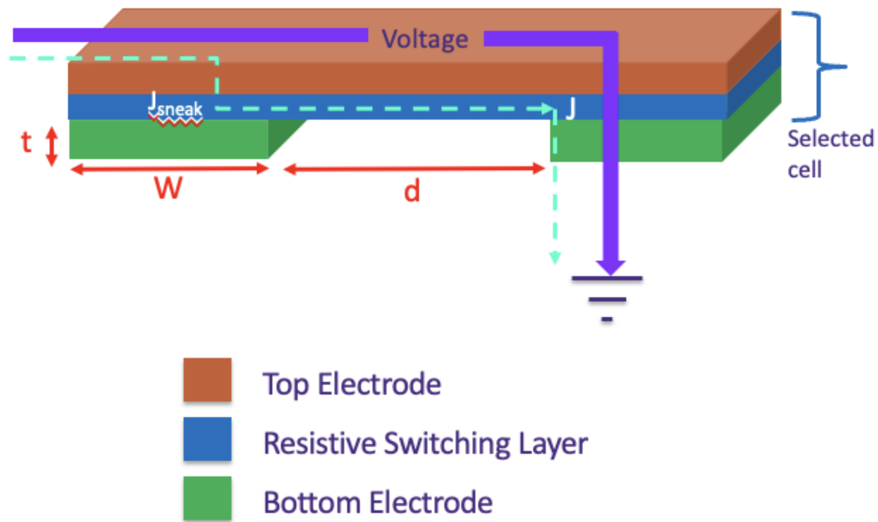


Figure 4.34 Schematic representation of sneak-path current in a ReRAM crossbar array cell. The selected cell consists of a top electrode (TE), resistive switching layer (RSL), and bottom electrode (BE). The applied voltage across the selected cell drives the intended read/write current (J), while unintended leakage current (Jsneak) can flow through unselected regions due to the uniform RSL deposition. Geometric parameters include electrode thickness (*t*), electrode width (*W*), and spacing between electrodes (*d*), which influence the magnitude of sneak-path currents.

The current through the material is given by:

$$I = \frac{V}{R} = V \times \frac{A}{\rho d}$$

Since current density J is defined as current per unit area:

$$J = \frac{I}{A} = \frac{V}{\rho \cdot d}$$

Thus, we obtain the theoretical relationship:

$$J = \frac{V}{\rho \cdot d}$$

This equation shows that for a fixed resistivity (ρ, Ω·cm) and voltage, the current density, J (μA/μm²) is inversely proportional to the electrode spacing, d (μm). Reducing the distance increases current density, while increasing the distance decreases it, which is useful for minimizing sneak-path effects.

4.5.3 Experimental Current Density Calculation

To validate the theoretical relationship, experimental current density was calculated using actual measured resistance and device dimensions.

Given:

- $R_{eq} = 3655\ \Omega$
- w = 10 μm, t = 60 nm, d = 60 μm

Step 1: Estimate Resistivity (ρ) from Measured Resistance

We use the relation: R = ρ · (d / A), rearranged as:

$$\rho = R \times \frac{A}{d}$$

Substituting values:

$$A = w \times t = 10\ \mu m \times 60\ nm = 10 \times 60 \times 10^{-6} \times 10^{-4}\ cm^2$$

$$A = 6 \times 10^{-7}\ cm^2,\ d = 60\ \mu m = 6 \times 10^{-3}\ cm$$

$$\rho = (3655 \times 6 \times 10^{-7}) / (6 \times 10^{-3}) = 0.00366\ \Omega\cdot\text{cm}$$

Step 2: Experimental Current Density (J_{exp})

Using:

$$J_{sneak} = \frac{V}{\rho \cdot d}$$

where d is in µm and $\rho = 0.00366\ \Omega\cdot\text{cm}$

Table 4.3 Experimental Current Density J_{sneak}

Voltage (V)	**Current Density J_{sneak} (µA/µm²)**
1.1	500.90

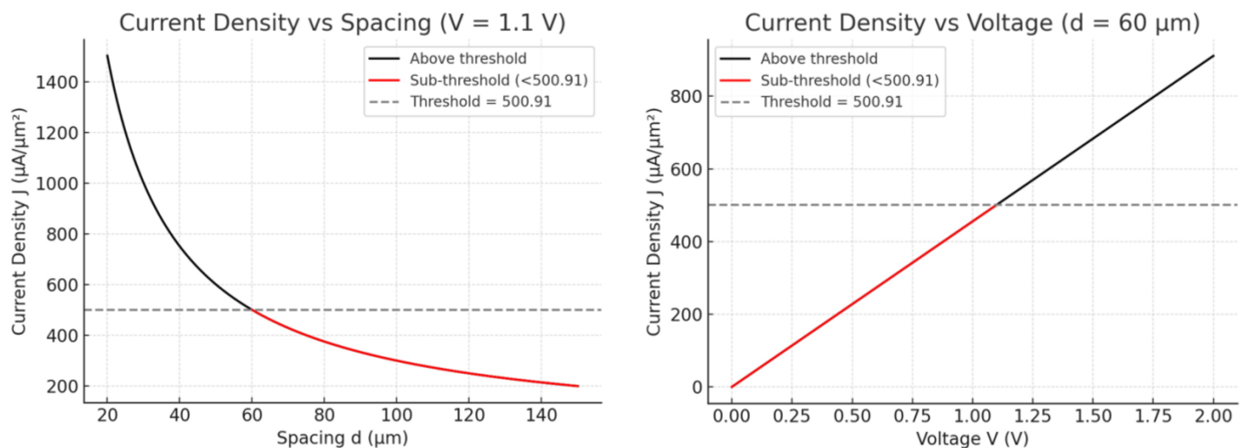


Figure 4.35 *Current Density vs. Spacing (V = 1.1 V) (Left).* The plot shows the effect of electrode spacing on current density at a fixed bias. Current density decreases non-linearly with increasing spacing, with values above the threshold (500.91 µA/µm²) shown in black and sub-threshold values in red. Increasing spacing beyond ~60 µm effectively suppresses sneak-path currents. *Current Density vs. Voltage (d = 60 µm) (Right).* The plot illustrates the linear increase of current

density with applied voltage at fixed spacing. Voltages below ~1.1 V (red) keep the density below the threshold, whereas higher voltages (black) exceed it, indicating a greater risk of sneak-path interference.

4.5.4 Voltage-Dependent Resistivity in Sneak-Path Modeling

While the preceding models assumed a constant resistivity (ρ) for the resistive switching layer (RSL), in practice PEDOT:PSS-based ReRAM devices typically exhibit a voltage-dependent resistivity due to changes in transport mechanisms. At low bias, conduction is dominated by insulating behavior and hopping through localized states. As the applied voltage increases, mechanisms such as trap-assisted tunneling, space-charge-limited conduction (SCLC), and polaron/bipolaron transport progressively reduce the effective resistivity of the film [46][47].

To incorporate this effect into sneak-path analysis, the Ohmic model is extended as:

$$J(V,d) = \frac{V}{\rho(V) \times d}$$

where ρ(V) follows an exponential decay relationship:

$$\rho\,(V) = \rho_0\, e^{-kV}$$

Here,

- ρ_0 is the resistivity at V=0,
- k is a decay constant determined experimentally,
- V is the applied voltage,
- d is the electrode spacing.

This exponential law is not a universal transport model, but a phenomenological approximation motivated by the behavior of conducting polymers. Previous studies of PEDOT:PSS conduction have reported nonlinear, field-dependent transport, often fitted with exponential or power-law dependencies [46][47]. Thus, adopting this exponential form allows the sneak-path model to remain analytically simple while still reflecting the experimentally observed trend that resistivity decreases rapidly with bias.

The threshold in the plot is simply:

$$\rho_{threshold}=0.3$$

so "above threshold" means $\rho(V)>0.3$, and "sub-threshold" means $\rho(V)<0.3$.

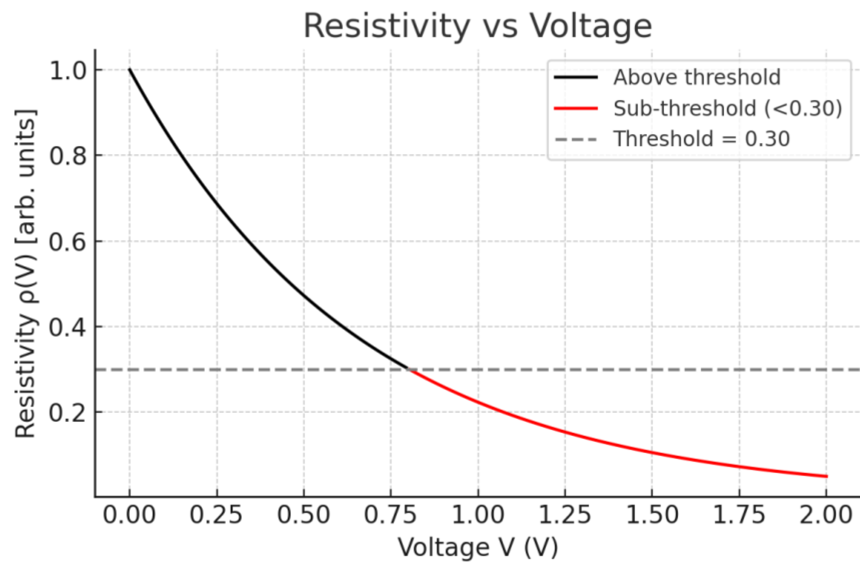


Figure 4.36: Resistivity Vs Voltage

Figure 4.36 shows the modeled resistivity vs. voltage curve for $\rho_0=1.0$ (arb. units) and $k=1.5\ V^{-1}$. Above a threshold resistivity ($t_{threshold}$), sneak-path currents are minimal (black region), while below

this threshold (red region) the risk of interference increases substantially. By incorporating $\rho(V)$ into the current density calculation, the fixed-spacing model in Figure 4.17 can be refined to reflect non-linear scaling with voltage. This is especially relevant for bias-dependent sneak-path suppression strategies, where lowering the read voltage can maintain $J(V)$ below the interference threshold even without increasing d.

5. CONCLUSION

This thesis has undertaken an extensive investigation into the development, characterization, and modeling of Resistive Random Access Memory (ReRAM) crossbar arrays, with a focus on addressing the persistent challenge of sneak path currents. Through a combination of theoretical analysis, experimental fabrication, electrical testing, and mathematical modeling, the work has demonstrated both the potential and limitations of ReRAM-based memory systems — particularly when aiming for dense, scalable, and energy-efficient architecture.

The journey began by identifying the critical bottlenecks in conventional memory technologies — SRAM, DRAM, and Flash — all of which suffer from either volatility, scalability limits, high energy consumption, or poor endurance. ReRAM, in contrast, emerges as a highly promising non-volatile alternative that combines fast switching, low power operation, and structural simplicity, especially when deployed in crossbar arrays. Its compatibility with CMOS processes and suitability for 3D stacking makes it a strong candidate for next-generation computing applications, including in-memory and neuromorphic systems.

The experimental component of this thesis focused on the fabrication of ReRAM crossbar arrays using a novel material stack: Silver (Ag) as the bottom electrode, PEDOT: PSS as the resistive switching layer, and Copper (Cu) as the top electrode. This stack was chosen for its ease of fabrication, CMOS compatibility, and well-documented switching behavior. Devices fabricated using this process exhibited stable bipolar switching, low forming voltages, and endurance over multiple cycles. Electrical characterization confirmed the presence of well-defined hysteresis loops and a clear distinction between high-resistance (HRS) and low-resistance states (LRS).

However, one of the most critical insights from this study was the observation that sneak path currents can still emerge, even in devices with structurally optimized RSL confinement. Through carefully designed hysteresis loop tracking**,** voltage sweep progression, and preconditioning tests**,** it was shown that sneak-path-induced switching begins to manifest at narrow voltage ranges, particularly around ±0.7 V to ±0.8 V**.** These results confirmed that structural confinement alone is insufficient to eliminate leakage currents and false switching in high-density crossbar architectures.

To address sneak-path interference, a **comprehensive mathematical model** was developed to quantify the relationship between **current density (J)**, **electrode spacing (S)**, and **applied voltage (V)**. Two scenarios were considered:

1. **Fixed Voltage Model** – At constant voltage, reducing the spacing between electrodes increases current density. While this enhances read performance, it also amplifies sneak-path effects. Increasing spacing suppresses sneak currents but results in lower read currents and higher power consumption.
2. **Fixed Spacing Model** – At constant electrode spacing, increasing voltage linearly raises current density. Low voltages keep the device below the sneak-path threshold, whereas higher voltages push it above the threshold, increasing the likelihood of interference.

These models highlight a fundamental tradeoff: **geometric design (spacing)** and **electrical bias (voltage)** can be tuned independently to balance read accuracy, power efficiency, and sneak-path suppression.

This tradeoff was illustrated across voltages and spacing, highlighting an important design constraint for ReRAM systems. The modeling further showed that maintaining the current density below a threshold of approximately 501µA/µm² can help avoid sneak-path interference during read operations.

In summary, this thesis not only advances the fabrication and characterization of polymer-based ReRAM devices but also contributes a detailed, application-ready model for understanding and controlling one of the most significant barriers to ReRAM scalability — sneak path currents. The insights and methodologies developed here are broadly applicable to the design of next-generation non-volatile memory systems and set the stage for future innovations in energy-efficient computing.

References

[1] W. Gul, M. Shams, and D. Al-Khalili, “SRAM Cell Design Challenges in Modern Deep Sub-Micron Technologies: An Overview,” *Micromachines*, vol. 13, no. 8, p. 1332, Aug. 2022, doi: 10.3390/mi13081332.

[2] N. Anagnostopoulos, S. Katzenbeisser, J. Chandy, and F. Tehranipoor, “An Overview of DRAM-Based Security Primitives,” *Cryptography*, vol. 2, no. 2, p. 7, Mar. 2018, doi: 10.3390/cryptography2020007.

[3] H. Jo, J. Kim, Y. Cho, H. Shim, J. Sim, and H. Shin, “Investigation of Endurance Characteristics in 3-D NAND Flash Memory With Trap Profile Analysis,” *IEEE Trans. Electron Devices*, vol. 71, no. 3, pp. 1852–1857, Mar. 2024, doi: 10.1109/TED.2024.3350565.

[4] M. Raquibuzzaman, A. Milenkovic, and B. Ray, “EXPRESS: Exploiting Energy–Accuracy Tradeoffs in 3D NAND Flash Memory for Energy-Efficient Storage,” *Electronics*, vol. 11, no. 3, p. 424, Jan. 2022, doi: 10.3390/electronics11030424.

[5] D. Le, B. Arig, M. Isik, I. C. Dikmen, and T. Karadag, “A Review of Memory Wall for Neuromorphic Computing,” Feb. 24, 2025, *arXiv*: arXiv:2502.16823. doi: 10.48550/arXiv.2502.16823.

[6] P. Jangra and M. Duhan, “Performance-based comparative study of existing and emerging non-volatile memories: a review,” *J. Opt.*, vol. 52, no. 4, pp. 2395–2409, Dec. 2023, doi: 10.1007/s12596-022-01058-w.

[7] X. Zou, S. Xu, X. Chen, L. Yan, and Y. Han, “Breaking the von Neumann bottleneck: architecture-level processing-in-memory technology,” *Sci. China Inf. Sci.*, vol. 64, no. 6, p. 160404, June 2021, doi: 10.1007/s11432-020-3227-1.

[8] M. Si, H.-Y. Cheng, T. Ando, G. Hu, and P. D. Ye, “Overview and outlook of emerging non-volatile memories,” *MRS Bull.*, vol. 46, no. 10, pp. 946–958, Oct. 2021, doi: 10.1557/s43577-021-00204-2.

[9] H. Lee, M. Kim, H. Kim, H. Kim, and H.-J. Lee, “Integration and Boost of a Read-Modify-Write Module in Phase Change Memory System,” *IEEE Trans. Comput.*, vol. 68, no. 12, pp. 1772–1784, Dec. 2019, doi: 10.1109/TC.2019.2933826.

[10] Y. Miura and M. Shirai, “Theoretical Study on Tunneling Magnetoresistance of Magnetic Tunnel Tunctions with $D{{0}_{22}}\hbox{-}{\hbox{Mn}}_{3}Z$ ($Z = {\hbox{Ga}},{\hbox{Ge}}$),” *IEEE Trans. Magn.*, vol. 50, no. 1, pp. 1–4, Jan. 2014, doi: 10.1109/TMAG.2013.2276625.

[11] A. A. Demkov, K. D. Fredrickson, H. Seo, and A. O’Hara, “First-Principles Modeling of Interface Effects in Oxides,” in *Handbook of Materials Modeling*, W. Andreoni and S. Yip, Eds., Cham: Springer International Publishing, 2019, pp. 1–30. doi: 10.1007/978-3-319-50257-1_58-1.

[12] F. Zahoor *et al.*, “Resistive random access memory: introduction to device mechanism, materials and application to neuromorphic computing,” *Discov. Nano*, vol. 18, no. 1, p. 36, Mar. 2023, doi: 10.1186/s11671-023-03775-y.

[13] W. Banerjee, “Challenges and Applications of Emerging Nonvolatile Memory Devices,” *Electronics*, vol. 9, no. 6, p. 1029, June 2020, doi: 10.3390/electronics9061029.

[14] F. Zahoor *et al.*, “Resistive random access memory: introduction to device mechanism, materials and application to neuromorphic computing,” *Discov. Nano*, vol. 18, no. 1, p. 36, Mar. 2023, doi: 10.1186/s11671-023-03775-y.

[15] J. Fu, Z. Liao, and J. Wang, “Cycle-to-cycle Variation Enabled Energy Efficient Privacy Preserving Technology in ANN,” in *2020 IEEE 33rd International System-on-Chip Conference (SOCC)*, Las Vegas, NV, USA: IEEE, Sept. 2020, pp. 66–71. doi: 10.1109/SOCC49529.2020.9524794.

[16] Z. Wang *et al.*, “Reinforcement learning with analogue memristor arrays,” *Nat. Electron.*, vol. 2, no. 3, pp. 115–124, Mar. 2019, doi: 10.1038/s41928-019-0221-6.

[17] C. Ding, Y. Ren, Z. Liu, and N. Wong, “Transforming memristor noises into computational innovations,” *Commun. Mater.*, vol. 6, no. 1, p. 149, July 2025, doi: 10.1038/s43246-025-00876-2.

[18] H. Bao *et al.*, “Toward memristive in-memory computing: principles and applications,” *Front. Optoelectron.*, vol. 15, no. 1, p. 23, Dec. 2022, doi: 10.1007/s12200-022-00025-4.

[19] F. Zhuge, B. Fu, and H. Cao, “Advances in Resistive Switching Memories Based on Graphene Oxide,” in *New Progress on Graphene Research*, J. R. Gong, Ed., InTech, 2013. doi: 10.5772/51260.

[20] D. Ielmini and G. Pedretti, “Resistive Switching Random-Access Memory (RRAM): Applications and Requirements for Memory and Computing,” *Chem. Rev.*, vol. 125, no. 12, pp. 5584–5625, June 2025, doi: 10.1021/acs.chemrev.4c00845.

[21] S. Pechmann *et al.*, “A Versatile, Voltage-Pulse Based Read and Programming Circuit for Multi-Level RRAM Cells,” *Electronics*, vol. 10, no. 5, p. 530, Feb. 2021, doi: 10.3390/electronics10050530.

[22] V. Mahboubi, Á. Gómez, A. Calomarde, D. Arumí, R. Rodríguez, and S. Manich, “On the Fine Tuning of RRAM Resistance Under Variability Using Current Pulses at SET,” in *2024 IEEE 30th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, Rennes, France: IEEE, July 2024, pp. 1–7. doi: 10.1109/IOLTS60994.2024.10616054.

[23] X. Hong, D. J. Loy, P. A. Dananjaya, F. Tan, C. Ng, and W. Lew, “Oxide-based RRAM materials for neuromorphic computing,” *J. Mater. Sci.*, vol. 53, no. 12, pp. 8720–8746, June 2018, doi: 10.1007/s10853-018-2134-6.

[24] M. A. Zidan, J. P. Strachan, and W. D. Lu, “The future of electronics based on memristive systems,” *Nat. Electron.*, vol. 1, no. 1, pp. 22–29, Jan. 2018, doi: 10.1038/s41928-017-0006-8.

[25] P. Wang, C. Ruan, W. Wang, and Y. Zhao, “Design of a Novel Reverse Magnetic System for Planar Three-Beam Array,” *IEEE Trans. Electron Devices*, vol. 72, no. 7, pp. 3861–3867, July 2025, doi: 10.1109/TED.2025.3571703.

[26] C. Li *et al.*, “In-Memory Computing with Memristor Arrays,” in *2018 IEEE International Memory Workshop (IMW)*, Kyoto: IEEE, May 2018, pp. 1–4. doi: 10.1109/IMW.2018.8388838.

[27] J. H. Hu *et al.*, “Evolved Cas9 variants with broad PAM compatibility and high DNA specificity,” *Nature*, vol. 556, no. 7699, pp. 57–63, Apr. 2018, doi: 10.1038/nature26155.

[28] J. Yao *et al.*, “Single-cell transcriptomic analysis in a mouse model deciphers cell transition states in the multistep development of esophageal cancer,” *Nat. Commun.*, vol. 11, no. 1, p. 3715, July 2020, doi: 10.1038/s41467-020-17492-y.

[29] Z. Xia *et al.*, "Dynamic analyses of alternative polyadenylation from RNA-seq reveal a 3′-UTR landscape across seven tumour types," *Nat. Commun.*, vol. 5, no. 1, p. 5274, Nov. 2014, doi: 10.1038/ncomms6274.
[30] A. Shafiee *et al.*, "ISAAC: A Convolutional Neural Network Accelerator with In-Situ Analog Arithmetic in Crossbars," in *2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA)*, Seoul, South Korea: IEEE, June 2016, pp. 14–26. doi: 10.1109/ISCA.2016.12.
[31] F. Gerfers, P.-H. Hsieh, D. Markovc, J. Deguchi, and E. Karl, "Introduction to the Special Issue on the 2020 IEEE International Solid-State Circuits Conference (ISSCC)," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 3–6, Jan. 2021, doi: 10.1109/JSSC.2020.3037445.
[32] S. K. Gonugondla, A. D. Patil, and N. R. Shanbhag, "SWIPE: enhancing robustness of ReRAM crossbars for in-memory computing," in *Proceedings of the 39th International Conference on Computer-Aided Design*, Virtual Event USA: ACM, Nov. 2020, pp. 1–9. doi: 10.1145/3400302.3415642.
[33] W. Sun *et al.*, "A Survey of Computing-in-Memory Processor: From Circuit to Application," *IEEE Open J. Solid-State Circuits Soc.*, vol. 4, pp. 25–42, 2024, doi: 10.1109/OJSSCS.2023.3328290.
[34] Y.-C. Chen, C.-C. Lin, and Y.-F. Chang, "Post-Moore Memory Technology: Sneak Path Current (SPC) Phenomena on RRAM Crossbar Array and Solutions," *Micromachines*, vol. 12, no. 1, p. 50, Jan. 2021, doi: 10.3390/mi12010050.
[35] S. K. Vishwanath, H. Woo, and S. Jeon, "Enhancement of resistive switching properties in $Al_2 O_3$ bilayer-based atomic switches: multilevel resistive switching," *Nanotechnology*, vol. 29, no. 23, p. 235202, June 2018, doi: 10.1088/1361-6528/aab6a3.
[36] X.-X. Xu, Q. Luo, T.-C. Gong, H.-B. Lv, Q. Liu, and M. Liu, "Resistive switching memory for high density storage and computing*," *Chin. Phys. B*, vol. 30, no. 5, p. 058702, May 2021, doi: 10.1088/1674-1056/abe0c4.
[37] H. Ji, Y. Lee, J. Heo, and S. Kim, "Improved resistive and synaptic switching performances in bilayer ZrOx/HfOx devices," *J. Alloys Compd.*, vol. 962, p. 171096, Nov. 2023, doi: 10.1016/j.jallcom.2023.171096.
[38] R. Joshi and J. M. Acken, "Sneak Path Characterization in Memristor Crossbar Circuits," *Int. J. Electron.*, vol. 108, no. 8, pp. 1255–1272, Aug. 2021, doi: 10.1080/00207217.2020.1843716.
[39] Jiantao Zhou, Kuk-Hwan Kim, and Wei Lu, "Crossbar RRAM Arrays: Selector Device Requirements During Read Operation," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1369–1376, May 2014, doi: 10.1109/TED.2014.2310200.
[40] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nat. Mater.*, vol. 6, no. 11, pp. 833–840, Nov. 2007, doi: 10.1038/nmat2023.
[41] Z.-R. Wang *et al.*, "Functionally Complete Boolean Logic in 1T1R Resistive Random Access Memory," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 179–182, Feb. 2017, doi: 10.1109/LED.2016.2645946.
[42] Y. Ben-Hur and Y. Cassuto, "Detection and Coding Schemes for Sneak-Path Interference in Resistive Memory Arrays," *IEEE Trans. Commun.*, vol. 67, no. 6, pp. 3821–3833, June 2019, doi: 10.1109/TCOMM.2019.2897762.
[43] X. Zhong, K. Cai, G. Song, and N. Raghavan, "Deep Learning Based Detection for Mitigating Sneak Path Interference in Resistive Memory Arrays," in *2020 IEEE*

International Conference on Consumer Electronics - Asia (ICCE-Asia), Seoul, Korea (South): IEEE, Nov. 2020, pp. 1–4. doi: 10.1109/ICCE-Asia49877.2020.9277380.
[44] A. Moazzeni, S. Hamedi, and Z. Kordrostami, "Switching characteristic of fabricated nonvolatile bipolar resistive switching memory (ReRAM) using PEDOT: PSS/GO," *Solid-State Electron.*, vol. 188, p. 108208, Feb. 2022, doi: 10.1016/j.sse.2021.108208.
[45] H. Yuan, T. Wan, and H. Bai, "Resistive Switching Characteristic of Cu Electrode-Based RRAM Device," *Electronics*, vol. 12, no. 6, p. 1471, Mar. 2023, doi: 10.3390/electronics12061471.
[46] Y. Yang *et al.*, "Electrochemical dynamics of nanoscale metallic inclusions in dielectrics," *Nat. Commun.*, vol. 5, no. 1, p. 4232, June 2014, doi: 10.1038/ncomms5232.
[47] A. J. Heeger, "Semiconducting and metallic polymers: the fourth generation of polymeric materials," *Synth. Met.*, vol. 125, no. 1, pp. 23–42, Nov. 2001, doi: 10.1016/S0379-6779(01)00509-4.