Radio Frequency Synthesis for Power-Constrained Systems

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Abstract

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DEDICATION

“So long, and thanks for all the fish.” - Douglas Adams

Chapter 1

INTRODUCTION

Advancements in sensor technology, energy storage, energy harvesting and integrated circuit manufacturing will enable a generation of wireless sensor networks capable of providing an entirely new sensing and communication paradigm. Such developments will concurrently revolutionize applications as seemingly disparate as neuroscience and industrial process control. The wave of innovation spanning the areas of semiconductor process technology, very large scale integrated (VLSI) circuit design, digital signal processing, digital communication and microfabrication that swept the cellular communication space will continue to have a transformative effect on industry, culture, and society at large. However, while these technologies will continue to allow for incremental improvements in the handheld device market spawning further growth, newer, burgeoning technologies are beginning to steer these industries' research efforts in entirely new directions.

Today, applications of wireless sensor nodes (WSNs) include health and home monitoring, automotive, smart buildings, predictive maintenance, indoor positioning and active RFID tags [44]. A typical WSN combines sensing, signal processing and RF communication circuits into a single, compact sensor system. The limited lifetime typically associated with these systems, generally due to power dissipated in the RF subsystem, has implications with regard to their widespread adoption for a given application. Additionally, the concurrent requirements of long lifetime and small form factor associated with many of the above applications do not align well with current battery technology [32]. Certain applications are more sensitive to these issues than others. For implanted and body-worn devices, frequent battery replacement has undesirable effects that range from inconvenient, for external devices such as fitness monitors, to those that may be life-threatening in cases where replacement would require surgery. Similar considerations apply to the employment of smart home/building WSNs, particularly in scenarios that compel the placement of sensors in hard-to-reach locales. Such concerns not only place strict limits on the power dissipated by these systems, but also urge the pursuit of alternative energy sources, ideally those capable of providing uninterrupted power indefinitely.

In typical commercial wireless applications (e.g., cellular) where communication occurs over distances of several kilometers, the majority of node power dissipation occurs in the RF power amplifier (PA), requiring extremely efficient PA design to minimize loss. For the applications considered here, the distance between transmitter and receiver is often only a few meters, so the required power output of the transmitter is low, generally less than 0 dBm (1 mW). For this reason, high PA efficiency alone is not sufficient to ensure economic use of available energy stores. In addition to lower transmit power, the required data rates for many sensing applications is quite low compared to conventional paradigms, and burst-mode operation may be employed [7]. As a result of these differences, many design strategies used in conventional radios are inappropriate for wireless sensor systems, and both architectural and circuit-level innovations are needed in order to cope with the stringent power limitations imposed by this growing technology space.

1.1 Application Space

The global efficiency of a transceiver drops off quickly as the output power is reduced, due to monopolization of a typical power budget by the PA. As has been noted, as transmitted power is decreased, the energy consumed by components other than the PA begins to have a notable impact on efficiency. In particular, power used by the local oscillator (LO) generation circuit places a significant strain on the system energy resources in severely energy-constrained scenarios [31]. Additionally, the long lock time ($> 10\,\mu s$) of a typical frequency synthesizer places an upper bound on the extent to which the radio may be duty cycled, limiting its viability for burst-mode transmission. Designs which employ an LO based on a free-running oscillator, such as the one proposed in [5], eliminate this handicap at the expense of inferior frequency stability, and require a frequency correction/calibration loop at the receiver end to compensate. The resulting link asymmetry is impractical for mesh-type sensor networks in which each node may function both as a transmitter and receiver.

The wide deployment of wireless sensors for various applications will require self-sufficient energy sources that are capable of powering nodes with expected lifetimes of 10 years or more. The need for energy autonomy presents a unique challenge for such devices, as their power sources should provide enough power to maintain an adequate (application specific) duty cycle and must typically occupy a relatively small form factor, particularly in the wearable devices and implantable space [24].

In the following section, an example wireless sensor node designed for biopotential recording applications is presented. When duty-cycled, the system is capable of being powered entirely by ambient sources (i.e., no battery is needed).

1.2 A Energy-Harvesting Wireless Sensor Node

In [5], a fully autonomous wireless sensor node capable of sustained operation from a thermoelectric energy harvester, or, TEG, was demonstrated. The node consists of four, highly integrated primary sections, including: 1) power management, 2) analog front end (AFE), 3) digital signal processing (DSP), and 4) RF transmitter (TX). A block diagram of the system is shown in Figure 3.1.1. The power management section includes a step-up DC-DC (boost) converter based on the design presented in [6], which boosts the TEG voltage from as low as 30 mV to a global V_{DD} of 1.35 V. Following a kick-start event, whereby the control circuitry of the boost converter is engaged with a minimum potential of 600 mV, the TEG/boost converter are together able to serve indefinitely as a power source for the rest of the system. The kick-

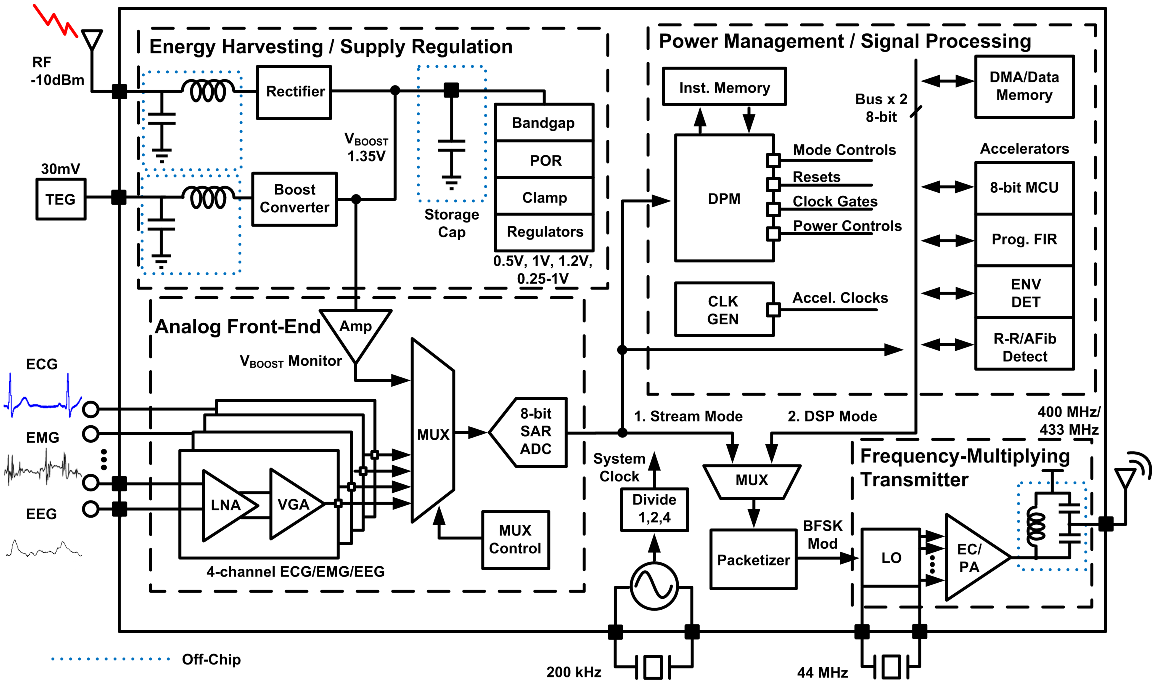

Figure 1.1: Batteryless sensor node block diagram.

start voltage is nominally provided by an RF rectifier with incident power as low as −10 dBm, though other startup mechanisms are possible. The rest of the power management section comprises a low-voltage bandgap reference, four sub-µW linear regulators, providing supply voltages for AFE, DSP and TX, and a programmable switched-capacitor DC-DC converter. The switched-cap converter offers a variable output between 250 mV and 1 V, enabling dynamic voltage scaling (DVS) for certain elements of the DSP section.

1.2.1 Power Management

The design of the power management portion of the system is critical to achieving overall energy efficiency. The low voltage TEG input is boosted and subsequently regulated. All biases are generated on chip . Supply regulation is provided by four sub-µW linear regulators: 1.2 V (AFE), 0.5 V (DSP), 1 V (TX local oscillator (LO)), and 0.5 V (TX power amplifier (PA)). A programmable switched-capacitor DC-DC converter provides an output from 0.25 V to 1 V in increments of 50 mV. A 3-bit resistor DAC (RDAC) generates a reference for the desired output level based on a control word from the DPM. The arrangement of the capacitors in the array varies according to the desired output voltage, in a manner similar to the one proposed in [34]. An external capacitor minimized the ripple voltage at the output. The subthreshold DSP accelerators can either be connected to the 0.5 V supply or the variable supply (switched-capacitor DC-DC converter) through PMOS headers, enabling DVS for additional power savings.

1.2.2 Analog Front End

The AFE contains four AC-coupled fully-differential analog input channels, each consisting of a low-noise amplifier (LNA) followed by a digitally-controlled variable-gain amplifier (VGA). Digitally selectable gain and bandwidth settings allow the chip to be configured for various biopotential sensing paradigms, including electrocardiography (ECG), electromyography (EMG), and electroencephalography (EEG). Analog waveforms are sampled and digitized by an 8-bit SAR ADC. The resulting data is either sent directly to the TX for transmission, or undergoes additional processing by the DSP. Biosignal band energy and R-R interval extraction for atrial fibrillation (AFib) event detection are some examples.

1.2.3 Low Power RF Transmitter

The transmitter is based on the design presented in [31]. It combines injection locking and frequency multiplication based on edge combining to achieve extremely low power operation. An N-stage ring oscillator is injection-locked to a quartz crystal oscillator with frequency f_{RF}/N. A 3-stage example is shown in Figure 1.2. In the design, N edges (N is equal to 3 in this example) of the ring oscillator are logically AND-ed and wire OR-ed in the output stage (PA) to generate an RF current, I_{RF}, at a frequency equal to Nf_{RO}. The primary advantage of this design is that the oscillator is allowed to operate at a much lower frequency than the RF carrier, reducing the amount of circuitry in the TX running at 400 MHz. The individual MOS devices in the PA are driven at f_{RF}/N, and their collective switching activity produces I_{RF} at the desired carrier frequency. In a typical frequency synthesizer, i.e., a phase-locked loop (PLL), the oscillator runs at f_{RF} and is controlled by a an explicit feedback loop, whose finite bandwidth limits the minimum start-up/frequency switching time of the system. The reduction of the LO frequency by N and the utilization of injection locking are the key techniques that enable ultra-low power operation without sacrificing performance.

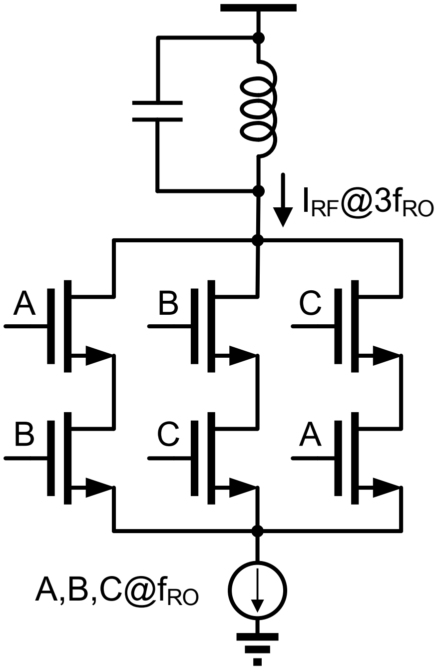

Figure 1.2: Frequency-multiplying PA.

1.2.4 Experimental Results

The system was fabricated in a 0.13 µm CMOS process and occupies 8.25 mm^2. A micrograph of the chip is shown in Figure 1.3. At 100% TX duty cycle, the entire chip dissipates 174 µW from the 1.35 V boost converter output. With 38% (measured) efficiency, this translates to 458 µW supplied by the harvester. The TX constitutes 92% (160 µW) of the total power usage. It should be noted that both the TX and the boost converter efficiency are serious bottlenecks in achieving overall energy autonomy.

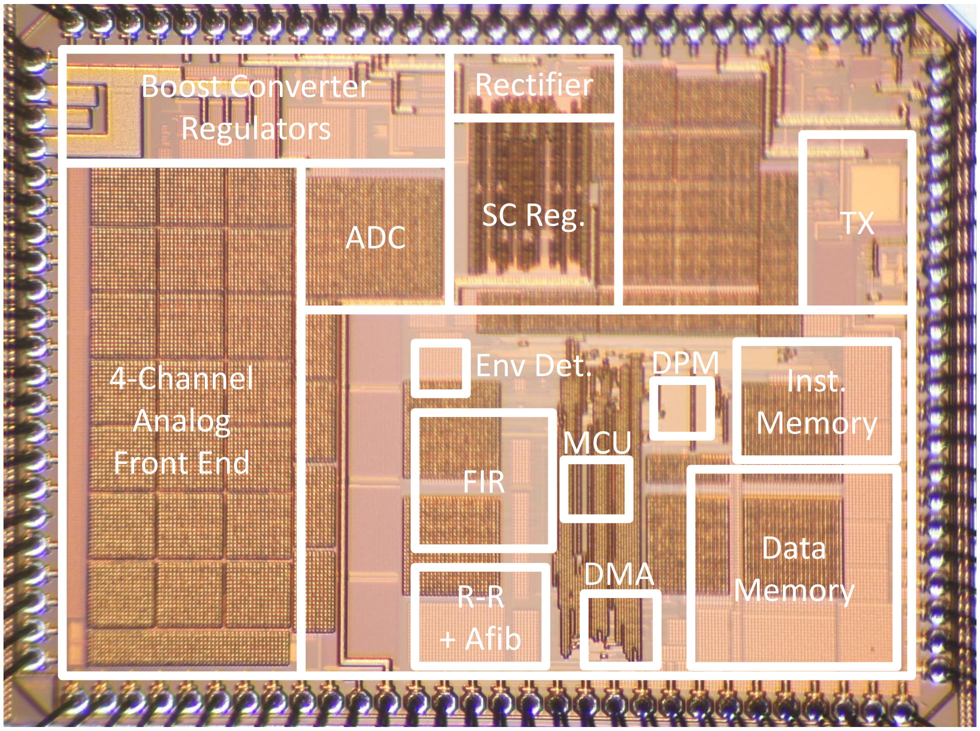

Figure 1.3: BASN chip micrograph.

1.3 LO Synthesis

The preceding design example is illustrative of the importance of LO power minimization in wireless sensor nodes. In spite of the fact that the power consumed by the frequency-multiplying TX is the lowest reported to-date, the overall system power dissipation is nonetheless dominated by the LO/TX. Further, the TX architecture is not amenable to multi-band applications, as its output frequency is a fixed integer multiple of that of the crystal oscillator. In light of these concerns, the design of a frequency synthesizer for communication with/between wireless sensor nodes should proceed with the following considerations:

1. Power consumption should be as low as possible without eschewing performance demands (e.g., settling time, phase noise).

2. Because the transceiver is designed to be part of a large system, and chip area must be shared with power management, analog signal conditioning and digital signal processing circuitry, area usage should be minimized.

3. Fast start-up is desirable, in line with application/standard requirements.

4. Phase noise performance and frequency selectivity should be aligned with the targeted radio standard/application.

1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 is intended to serve as an overview of frequency synthesis for wireless applications, with a focus on power reduction techniques. Chapter 3 gives a detailed description of the design of a fractional-N frequency synthesizer for body-worn and implantable devices, including measured performance results. Chapter 4 details the design and performance of an ultra-low-voltage all-digital phase locked loop (ADPLL) intended for enery-harvesting applications. The design presented in Chapter 5 builds upon that of Chapter 4, with considerations for improving performance and reducing power consumption. Finally, concluding remarks and potential future research directions are provided in Chapter 6.

Chapter 2

AN OVERVIEW OF FREQUENCY SYNTHESIS

Phase-locked loops (or, simply, PLLs) are used in myriad applications, including clock generation and recovery, FM radio demodulation, and frequency synthesis. Their ubiquity can be attributed to their versatility, in that the various design parameters governing the dynamics of PLLs can be adjusted to achieve different performance goals. For example, the loop bandwidth of a PLL can be made wide to suppress close-in phase noise of an RF oscillator, as is typically done in frequency synthesizers, or narrow to suppress frequency variations exhibited by an external clock source, as is the case for clock jitter cleaners. This chapter is intended to give an overview of PLL design for RF applications. As the focus of this thesis is frequency synthesis, all performance-related discussions herein will bear this application in mind.

2.1 Phase-locked Loop Basics

A basic block diagram of a PLL is shown in Figure 2.1. Employed as a frequency synthesizer, the goal of the PLL is to make the output frequency, f_{out}, equal to some integer multiple of the input frequency, f_{in}. In the locked, steady state (as $t \to \infty$), the following relation should hold:

$$f_{out} = N f_{in} \tag{2.1}$$

where N is the modulus of the frequency divider, as shown in the figure. A phase difference, typically referred to as a phase error, between the (divided) output clock and the input clock causes an increase or decrease in the frequency of the oscillator, depending on the sign of the phase error. Phase errors are processed by the phase detector such that a positive phase error corresponds to the input phase leading the output phase, and a negative phase error corresponds to the opposite case. Assuming there is no sign inversion in the loop filter and that the oscillator has a positive voltage-to-frequency characteristic, this forms a negative feedback loop. As with any negative feedback loop, high open-loop gain is needed in order to make the closed-loop relation of Equation (2.1) impervious to variations in the individual component parameters. Fortunately, the inherent frequency-to-phase conversion that occurs between the oscillator and the phase detector (i.e., the controlled variable is frequency and the detected variable, phase) provides an intrinsic integration, ensuring that the low-frequency (DC) gain in the forward path is infinite. In other words, the steady-state frequency error is zero. This single integration in the forward path is not, however, sufficient to ensure a zero steady-state phase error, and there is always some finite phase error associated with any output frequency that is not equal to the free-running frequency of the oscillator (i.e., a phase error of zero implies that the output frequency is equal to the free-running frequency). This limitation can be overcome by adding an additional integrator to the loop filter, the details of which will be discussed in subsequent sections.

2.2 Basic Synthesizer Architectures

2.2.1 Analog Frequency Synthesizers

The charge-pump phase-locked loop (CP-PLL), first analyzed in detail by Gardner in [16], has dominated the frequency synthesis arena for several decades. Its preeminence can be attributed to the ease with which a second integrator is included in the loop dynamics (the first being inherent to the use of phase as a loop variable), enabling zero steady-state phase error and greater noise suppression. These desirable characteristics are achieved, in contrast with other implementations, without the ad-

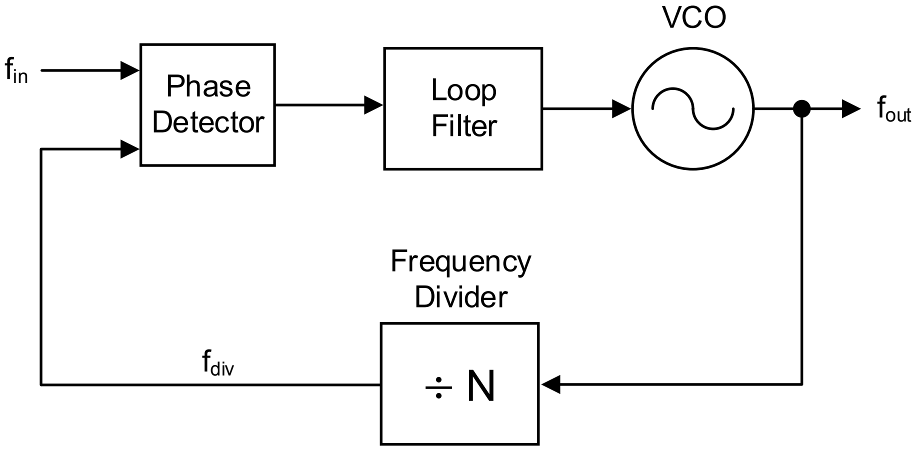

Figure 2.1: General PLL block diagram.

dition of an operational amplifier to the loop filter, the use of which adds complication to stability compensation and compels further noise and power considerations. This work focuses exclusively on charge-pump-based implementations of analog synthesizers, and thus only those components and techniques applicable to charge-pump PLLs are considered. For a more complete overview of synthesizer architectures, the reader is referred to [17][18][15][4].

A basic block diagram of a CP-PLL is shown in Figure 2.2. A description of its operation is given as follows. The phase/frequency of the voltage-controlled oscillator (VCO) (or frequency divider, for $N > 1$) is compared with that of the reference by the phase/frequency detector (PFD). The operation of the PFD can be modeled by a state machine with three possible states: up (+1), down (-1), and hold (0). The PFD output controls the polarity of the charge pump (CP) current, which is converted to a voltage by the loop filter impedance. The loop filter voltage determines the output frequency of the VCO based on its voltage-frequency characteristic, which is usually modeled as a linear gain with the y-intercept indicating its free-running, or center frequency. For RF applications, a frequency divider is typically inserted between the VCO and the PFD, as the desired output frequency is often 100s of times greater

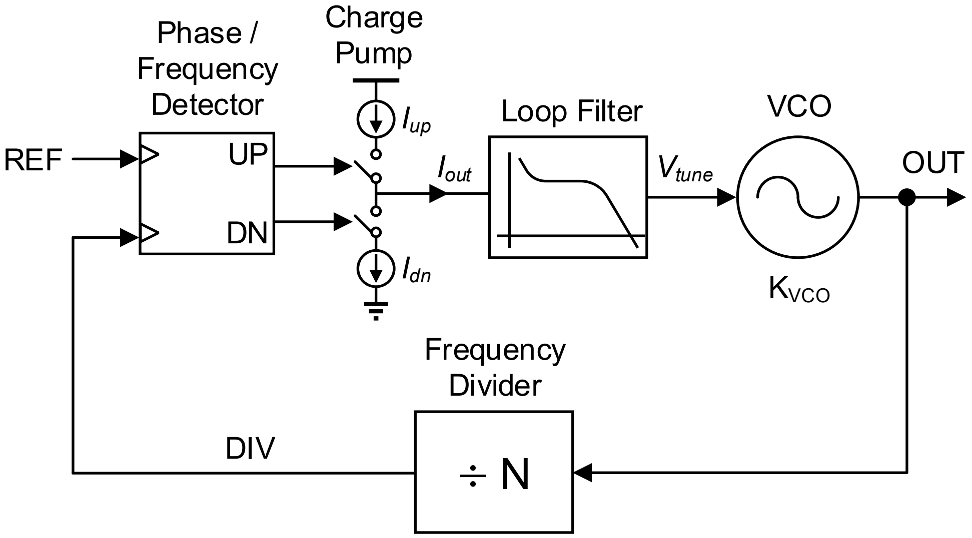

Figure 2.2: Block diagram of an integer-N charge-pump PLL.

than that of a typical frequency reference. For example, a synthesizer operating in the 2.4 GHz ISM (Industrial Scientific Medical) band might use a 24 MHz crystal oscillator reference, in which case N would be equal to 100. Due to manufacturing and cost limitations, crystal frequencies much above 100 MHz are uncommon. The ratio between the output and input frequencies is in general represented by N. If N is strictly an integer, then the loop is referred to as an integer-N phase-locked loop. If N is allowed to take on fractional values, then the loop is called a fractional-N phase-locked loop. Because frequency division is most often accomplished by some form of counting of the VCO periods, fractional-N operation is generally achieved by dithering the instantaneous value of N between two or more integer values, with the duty cycle of the dither determining its fractional value. Periodic modulation of N gives rise to undesirable spurious (discrete frequency) tones in the output spectrum of the PLL. For this reason, random dither, or more sophisticated techniques such as noise shaping, are often employed. The most common method of dithering the divider modulus involves the use of a digital $\Delta\Sigma$ modulator, also referred to as a

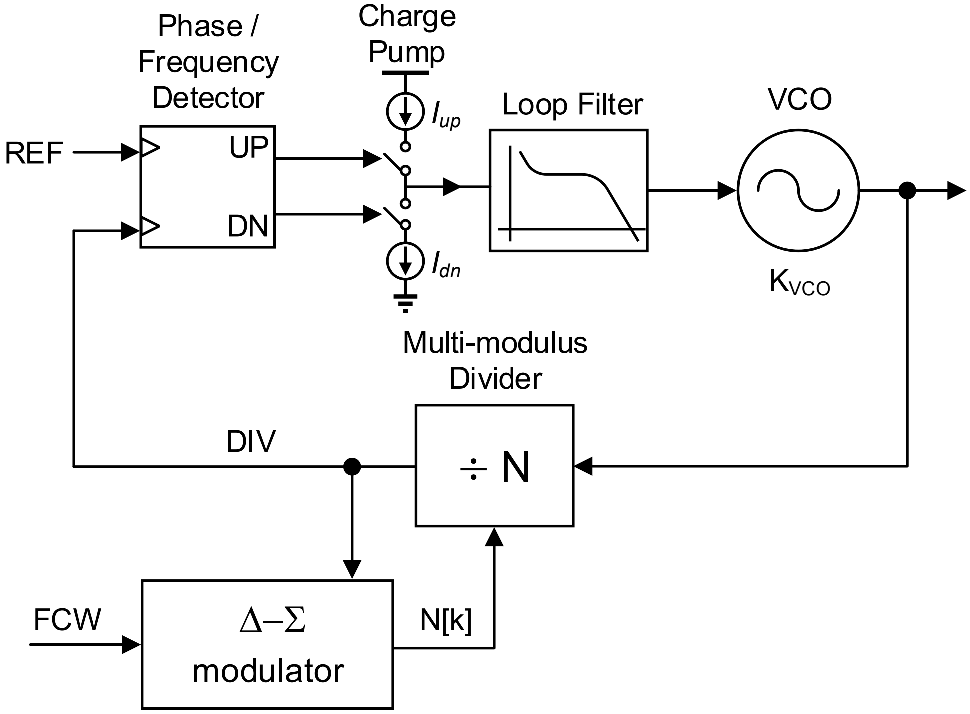

Figure 2.3: Typical implementation of a fractional-N charge-pump PLL using $\Delta\Sigma$ modulation.

DSM, as shown in Figure 2.3 [28][38]. The output of the DSM is a sequence of digital values generated in such a way as to concentrate the noise due to quantization at frequencies higher than the bandwidth of the PLL. In this way, the quantization noise is suppressed by the loop and, ideally, does not corrupt the output spectrum.

The choice of architecture (integer-N or fractional-N) is typically constrained by application and performance requirements. If tight channel spacing, i.e. fine frequency resolution, is needed, an integer-N design would compel a relatively low reference frequency, as the output frequency resolution directly determines the choice of reference. That is, the output frequency can only be changed in integer-valued steps, each of which is a multiple of the input frequency. If a fractional-N design is employed, these two specifications can be decoupled. It is often desirable to combine fine frequency resolution with a higher reference frequency. The reason for this relates to the discrete-time nature of the charge-pump PLL. Discrete-time stability concerns prevent the realization of a loop bandwidth greater than approximately one tenth of the reference frequency [16]. Because loop bandwidth has implications with regard to various performance metrics such as settling time and noise filtering, and because channel spacing is compelled by the application (or radio standard), it is extremely useful to make these two specifications independent of each other. Thus, fractional-N designs are rather common in wireless systems.

2.2.2 Digital Frequency Synthesizers

The last few decades have been witness to an explosion in the number of traditionally analog-intensive electronic system components being replaced by designs that are more digital in nature. This trend is largely the result of Moore's Law, which was the observation made in 1965 by Gordon Moore, co-founder of Intel Corporation, that the number of CMOS (complementary metal-oxide-semiconductor) transistors fabricated on a single die tended to double every 18 months (and would likely continue to do so) leading to an exponential decrease in the cost of implementing a given function in silicon-based hardware [30]. In addition to scaling trends, the gradual shift from analog to digital has also been motivated by the precision and robustness inherent to digital CMOS, contrasted with the process, temperature and voltage dependence, the general environmental sensitivity intrinsic to analog designs, whose performance is intimately linked to, and indeed based upon physical parameters of the transistors themselves. The migration has been further accelerated by increasingly lower supply voltages, arising from reliability concerns, limiting architectural freedom and signal dynamic range of voltage-mode analog designs.

The most common realization of a digital frequency synthesizer for RF applications is the TDC-based all-digital PLL [42]. A basic block diagram of the architecture is shown in Figure 2.4. Compared to the CP-PLL, the PFD-CP is replaced by a time-to-digital converter and digital phase detector. The loop filter, which is an impedance

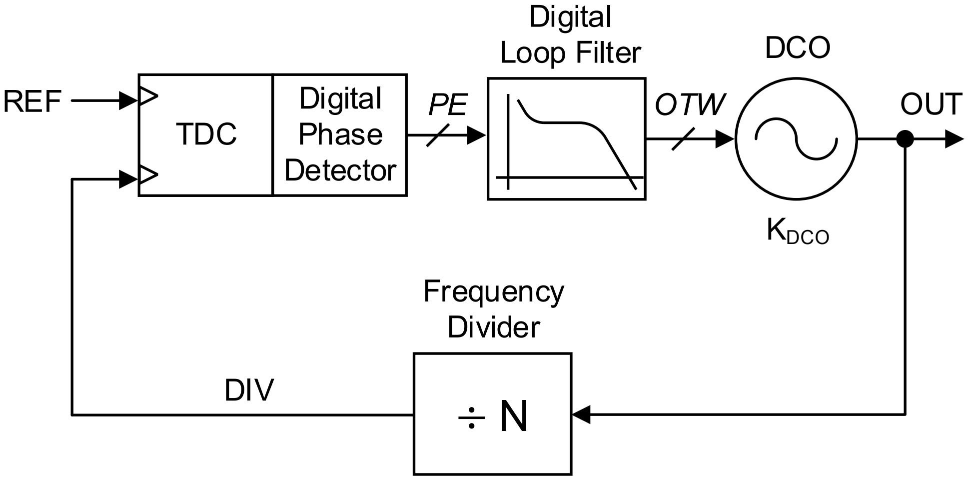

Figure 2.4: TDC-based ADPLL block diagram.

in the CP-PLL, is replaced by a digital filter. A digital-to-analog converter (DAC) is added to the oscillator to enable digital frequency tuning, forming what is typically referred to as a digitally-controlled oscillator (DCO). In steady state operation, the TDC digitizes the phase of the DCO and the quantized value is compared to a digital representation of the reference phase. The resulting digital representation of the phase error (PE) is processed by the loop filter and frequency of the DCO is increased or decreased accordingly.

2.3 PLL Building Blocks

In this section, a brief description of the primary building blocks of the PLL is given, focusing primarily on those structures which are relevant to integrated CP-PLLs. For each block, a linear model is developed that will be used in Section 2.4 to build a model of the entire PLL. The resulting linear model will then be used in the analysis of loop dynamics and noise properties in Section 2.4.

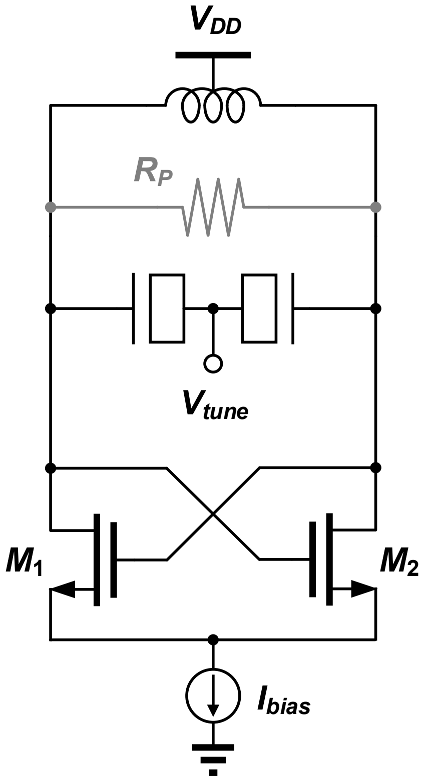

Figure 2.5: Voltage-controlled LC oscillator.

2.3.1 LC-VCOs

The treatment of the subject of oscillators presented here is intended to inform the material discussed in this and subsequent chapters, and is by no means comprehensive. For a more expansive and in-depth analysis of integrated VCOs, the reader is referred to [19] [20] [35].

In integrated frequency synthesizers, the two primary VCO architectures used are the voltage-controlled harmonic, or LC, oscillator (LC-VCO) and the voltage-controlled ring oscillator (VCRO). LC-VCOs exploit the resonant characteristic of a series or parallel connection of an inductor and a capacitor to generate an (approximately) sinusoidal oscillation. The inevitable energy loss in these components, due to the presence of finite resistance and modeled as R_P in Figure 2.5, is compensated for by the addition of a restoring circuit which periodically draws energy from the power supply and resupplies it to the resonant "tank". In this design, which utilizes a parallel resonant structure, the cross-coupled NMOS transistors M_1 and M_2 are said to provide a negative resistance, equal to $2/g_m$, in parallel with R_P that effectively "cancels" the tank losses. This negative resistance is in fact chosen to be greater in magnitude than R_P, and is nonlinear in the sense that as the differential voltage grows, at some point the effective transconductance diminishes, ultimately changing the polarity of the so-called negative resistance and halting the growth. In an average sense, the differential resistance looking into the drains of the cross-coupled pair is equal to $2/g_m$. Frequency tuning of the LC-VCO is typically accomplished using voltage-controlled capacitors, most often inversion-mode or accumulation-mode MOS capacitors for integrated oscillators [1]. In this sense, the LC-VCO is really a capacitance-controlled oscillator. Key considerations are linearity and tuning range, two properties that are often in opposition with each other due to the nonlinear voltage-capacitance characteristic of the MOS capacitance. For this reason, some combination of digitally-controlled capacitance (either MOS capacitors or switched metal capacitors) and voltage-controlled capacitance is frequently employed.

The oscillation frequency of the LC-VCO is approximately given by

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.2}$$

where L and C are the total parallel inductance and capacitance, respectively, connected across the differential outputs of the oscillator. We can separate the total capacitance into fixed and variable parts (this is typically done in the design process), obtaining

$$\omega_0 = \frac{1}{\sqrt{L(C_0 + C_{var})}} \tag{2.3}$$

Assuming C_{var} to be a linear function of the applied voltage V_{tune}, a desirable property, we have

$$\omega_0 = \frac{1}{\sqrt{L(C_0 + K_c V_{tune})}} \tag{2.4}$$

where K_c is the linear voltage-to-capacitance gain of the varactor. Assuming that $C_{fixed} >> K_c V_{tune}$ (a reasonable assumption for high linearity), the tuning gain in rad/s/V is given approximately by

$$\frac{d\omega_0}{dV_{tune}} \approx -\frac{\omega_0 K_c}{2C_0} \tag{2.5}$$

The phase-domain linear model of the LC-VCO consists of the proportional term given by Equation (2.5) multiplied by an integral term (represented by 1/s in the Laplace domain) to account for the frequency-to-phase conversion inherent to any oscillator.

2.3.2 Ring VCOs

VCOs based on ring oscillators are less common in wireless systems, but are widely used in digital systems for clocking applications. The primary reason for their absence in most RF applications is their inferior phase noise performance, a critical metric in both transmitters and receivers. A typical implementation of a VCRO is shown in Figure 2.6. The oscillator core consists of n delay stages, CMOS inverters in the case of a single-ended design, connected in feedback as shown. In the single-ended

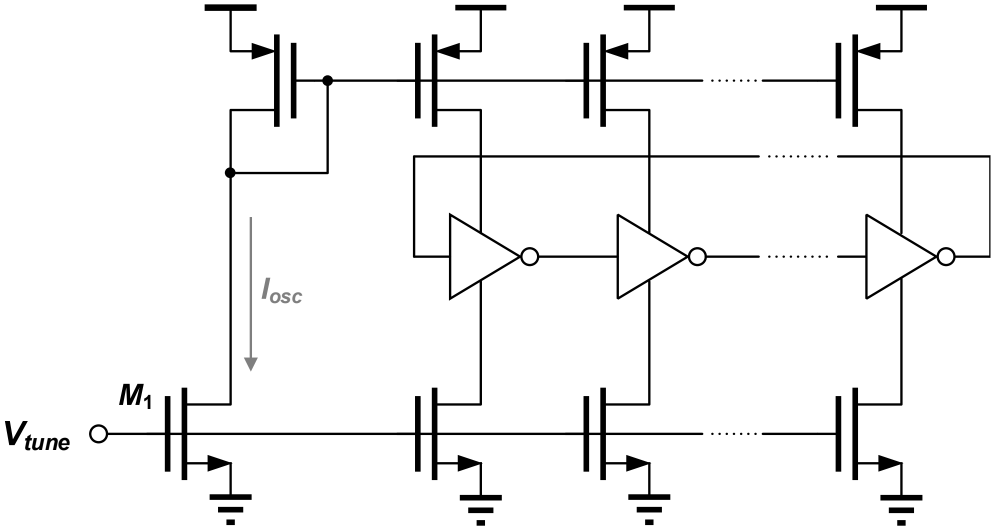

Figure 2.6: Typical implementation of a voltage-controlled ring oscillator.

case, an odd number of delay stages is needed to achieve oscillation, constraining n to be an odd number. The frequency of oscillation can be estimated by considering the propagation delay through each stage of the ring. The delay of a CMOS inverter can be approximated using the long channel MOS model as

$$\tau_{inv} = \frac{V_{DD}C_L}{2I_D} = \frac{V_{DD}C_L}{\mu C_{ox}(\frac{W}{L})(V_{DD} - V_{th})^2}, \tag{2.6}$$

where V_{DD} is the supply voltage, C_L is the load capacitance of each stage, I_D is the discharge current, equal the the MOS drain current, μ is carrier mobility, C_{ox} is the MOS oxide capacitance-per-unit-area, (W/L) is the transistor aspect ratio, and V_{th} is the threshold voltage. If the load capacitance C_L of each stage of the ring oscillator is taken to be the C_{gate} of the following stage, the delay is given as

$$\tau_{inv} = \frac{V_{DD}C_{gate}}{\mu C_{ox}(\frac{W}{L})(V_{DD} - V_{th})^2} \tag{2.7}$$

The use of Equation (2.7) assumes that the conducting transistor remains in saturation during the time that the output transitions to $V_{DD}/2$, a reasonable assumption if $V_{th} \approx V_{DD}/2$. A more precise determination of the inverter delay can be obtained using the method outlined in [39]. Frequency tuning of a ring oscillator is generally accomplished by limiting the current available to the individual delay stages of the ring, making it a current-controlled oscillator. In Figure 2.6, the current available to each delay stage is limited by the NMOS and PMOS current sources. Taking this current to be I_{osc}, the stage delay instead becomes

$$\tau_{inv} = \frac{V_{DD} C_{gate}}{2 I_{osc}}, \tag{2.8}$$

where I_{osc} is designed to produce the desired oscillation frequency. Voltage-to-current conversion is accomplished using a transconductance stage. This can accomplished by a single transistor, as with M_1 in Figure 2.6. Assuming identical sizing of all NMOS and PMOS transistors in Figure 2.6 (i.e., $(W/L)_n = (W/L)_p$), the oscillation frequency of the VCRO is given approximately by

$$f_{ring} = \frac{1}{2n\tau_{inv}} = \frac{I_{osc}}{2nV_{DD}C_{gate}} = \frac{I_0 + G_m V_{tune}}{2nV_{DD}C_{gate}} \tag{2.9}$$

In a practical implementation, a constant current would typically be connected, given by I_0 in (2.9), in parallel with M_1 to set the minimum oscillation frequency of the ring. Additionally, source degeneration is typically employed to achieve a more linear (voltage-to-frequency) gain characteristic. The tuning gain is thus well approximated as

$$\frac{df_{ring}}{dV_{tune}} = \frac{G_m V_{tune}}{2nV_{DD}C_{gate}} \tag{2.10}$$

2.3.3 Frequency Dividers

The list of possible implementations of frequency dividers is a lengthy one, ranging from CMOS register- and counter-based designs to those based on injection-locking either harmonic or ring oscillators to subharmonics of the VCO. Only a brief description of the basic principles and realizations is given here. The ideal frequency divider produces the relationship between the input and output frequencies given by

$$f_{div} = \frac{f_{in}}{N} \tag{2.11}$$

The input and output phase follow a analogous relationship, given by

$$\phi_{div} = \frac{\phi_{in}}{N} \tag{2.12}$$

Register-based designs are the most common, as division by $N = 2$ is readily accomplished by feeding back the complementary output of a flip-flop to its input, as shown in Figure 2.7. Higher values of N can be achieved by cascading multiple divide-by-2 stages, giving $N = 2^n$, where n is the number of stages. In a frequency synthesizer, it is typically desirable to make N variable, allowing the output frequency of the PLL to be changed. A frequency divider whose modulus can be changed is typically referred to as a multi-modulus divider. A more detailed treatment of frequency division techniques and divider architectures will be provided in Chapters 3 and 4.

2.3.4 Digital $\Delta\Sigma$ Modulators

Because the DSM is such a integral component in the implementation of fractional-N PLLs, some discussion of its operation is warranted here. The DSM and multi-modulus frequency divider comprise a digital-to-time converter whose raw resolution

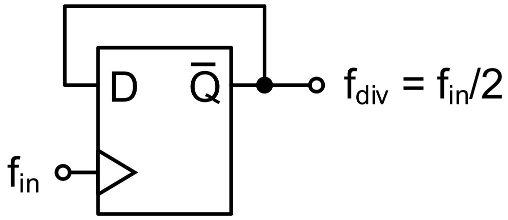

Figure 2.7: Register-based division by 2.

is given by that of the divider (i.e., one period of the VCO). The purpose of the DSM is to effectively filter the quantization noise such that very little appears in the passband of the PLL.

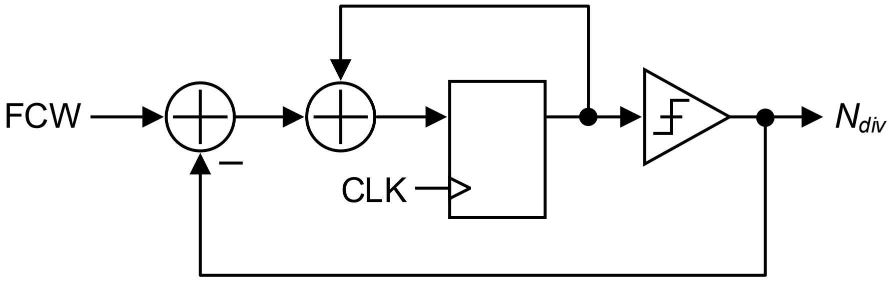

Figure 2.8: First-order ΔΣ modulator.

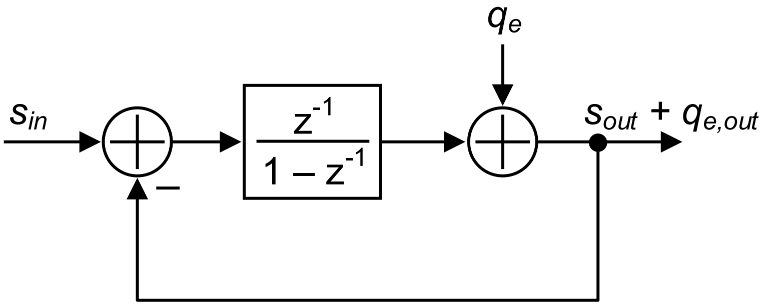

Figure 2.9: Linear model of first-order DSM

A block diagram of a first-order DSM is shown in Figure 2.8. The difference between the input digital word and the quantized output (hence the Δ) is accumulated (hence the Σ) and undergoes single-bit quantization. A discrete-time linear model of the first-order DSM is shown in Figure 2.9. The digital accumulator is modeled by its z-domain transfer function, and the quantizer is modeled by a unity multiplier (i.e., a wire) and additive quantization noise. Although in the first-order modulator the approximation of additive quantization noise is hardly defensible, for which reason the first-order DSM is rarely used in practice; it is nonetheless illustrative of the behavior of higher-order modulators [37]. Separating the signal component from the noise component at the output (permissible following the linearity assumption), we observe the noise transfer function (NTF) to be

$$\frac{q_{e,out}}{q_e} = 1 - z^{-1} \tag{2.13}$$

The "signal", in this case a constant digital value, passes unscathed through the modulator. Its transfer function is given by

$$\frac{s_{out}}{s_{in}} = z^{-1} \tag{2.14}$$

That is, the input signal experiences a simple delay while the quantization noise is shaped according to (2.14). If, instead of using a DSM, random dither of the divider modulus were used to achieve fractional control of the output frequency, the resulting quantization noise would produce output phase noise too high for most RF applications. For the first-order modulator, quantization noise shaping takes the form of a (discrete-time) differentiator. Higher order modulators, which employ more than one accumulator, provide greater in-band quantization noise suppression at the expense of increased growth out-of-band. The steeper slope of the quantization noise necessitates a higher-order loop, potentially compromising stability of the PLL.

2.3.5 Phase Detectors

The purpose of the phase detector is to produce an output proportional to the phase difference, ϕ_e, between its inputs, ϕ_{ref} and ϕ_{div}. A linear characteristic is desirable, and the gain of the phase detector is typically expressed as K_d. In charge-pump PLLs a tri-state phase detector, known as a phase-frequency detector (PFD), is generally used. In contrast with some other common phase detector implementations, such as the voltage mixer, the PFD operates on a sampled, discrete-time basis. As discussed in Section 2.4, operation of the loop in discrete time has implications with regard to loop stability.

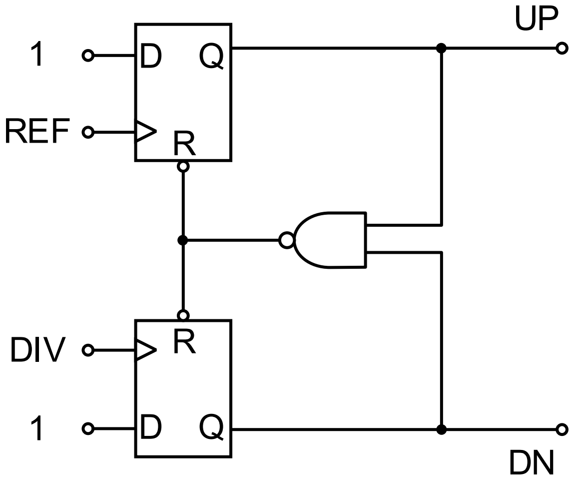

Figure 2.10: Phase-frequency detector.

A block diagram of the PFD is shown in Figure 2.10. The operation of the PFD is described as follows. When a positive reference edge arrives, assuming DIV is low (logical 0), the UP signal goes high due to the constant logical 1 connection to the data input of the register. When DIV goes high (logical 1), the DN signal and thus the second input to the NAND gate goes high. The '0' output of the NAND gate resets both flip-flops, so that both UP and DN are once again low. The operation is summarized by the finite state machine depicted in Figure 2.11. When

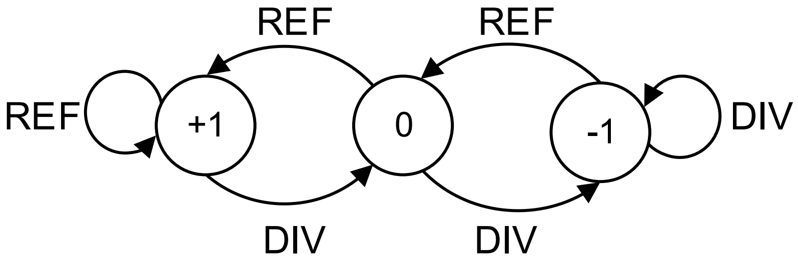

Figure 2.11: Finite state machine describing PFD operation.

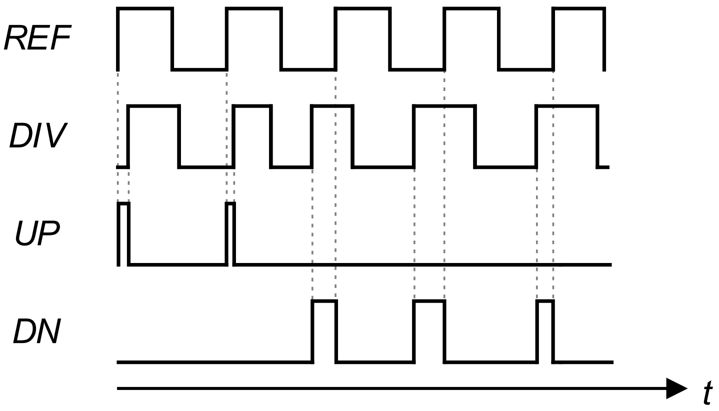

Figure 2.12: Time-domain operation of the PFD.

UP is high, a positive current I_{up} ($I_{out} = I_{up}$) is asserted on the loop filter, as shown in Figure 2.13. This corresponds to the +1 state of the state machine. DIV high corresponds, accordingly, to the -1 state of the state machine (producing $I_{out} = -I_{dn}$). The 0 state is reached when either a positive DIV edge follows a positive REF edge, or vice-versa. Consecutive DIV or REF transitions without a corresponding transition in the other keeps the PFD in either the +1 or -1 state, reflecting a frequency difference between the two clocks. A time-domain representation of the PFD operation is shown in Figure 2.12. The “on” time of the charge pump as a result of a phase error ϕ_e is given by [16]

$$t_p = |\phi_e|/\omega_i \tag{2.15}$$

where ϕ_e is the phase error, or the difference given by $\phi_{ref} - \phi_{div}$, and ω_i is the input (reference) frequency in radians per second. Assuming $I_{up} = I_{dn} = I_{cp}$, a charge pump current given by $I_{cp} \operatorname{sgn} \phi_e$ is delivered to the loop filter impedance for a duration of t_p seconds during each reference cycle. The effect of this current on the VCO frequency depends on the type of loop filter used. If the loop filter impedance contains an integral component, then the VCO frequency will increase or decrease by an amount proportional to the pulse width of the charge pump current. The average (positive or negative) output current of the charge pump is then given by

$$\overline{I_{out}} = \frac{I_{cp} t_p}{2\pi/\omega_i} = \frac{I_{cp}\phi_e}{2\pi} \tag{2.16}$$

from which we can derive the proportionality constants $1/2\pi$ and I_{cp} for the PFD and charge pump, respectively. These two blocks are often considered as a single unit and modeled as such. The transfer characteristic of the combined block is shown in Figure 2.14, where we can see that the average output current increases to a maximum value of I_{cp} when the phase error is equal to 2π.

2.3.6 Loop Filters

The charge pump output current needs to be converted to a voltage in order to change the VCO frequency. This is, of course, accomplished by an impedance, resulting in a rather simple loop filter design. For a type-II PLL, wherein a steady-state phase error of zero is attainable, a second integrator, in addition to the one inherent to the frequency-to-phase conversion of the VCO, is included in the loop filter transfer

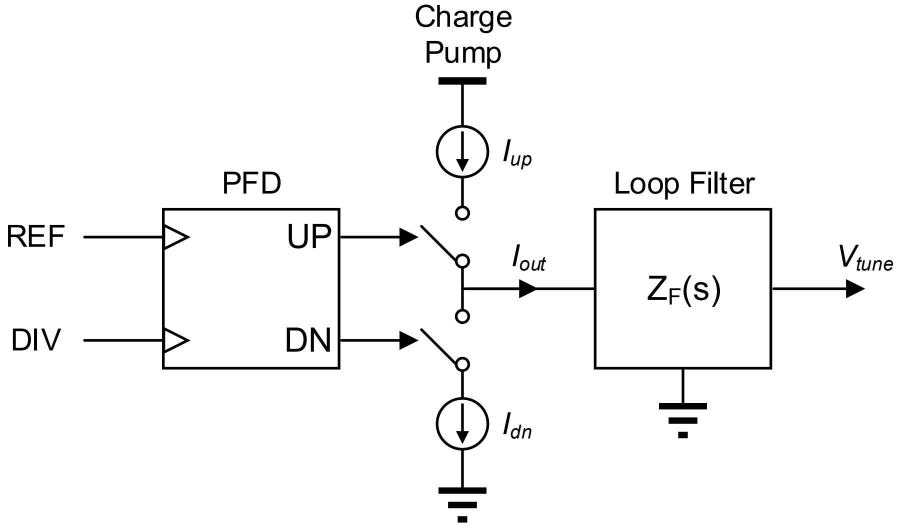

Figure 2.13: Charge pump driven by PFD and followed by a loop filter impedance.

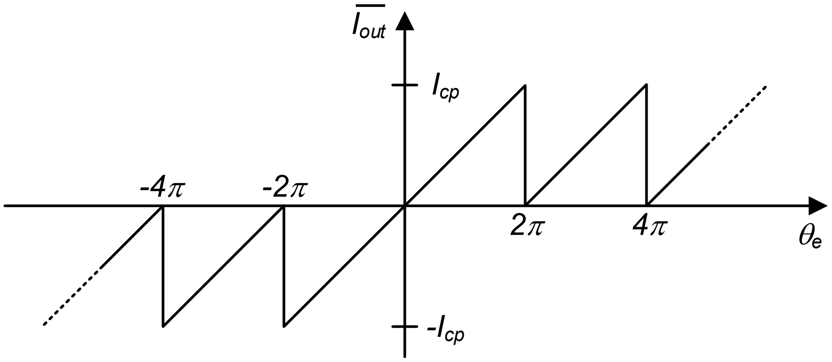

Figure 2.14: PFD-CP gain characteristic.

function. The integrator is typical realized as part of a proportional-plus-integral (PI) structure, chracterized by an equation of the form

$$Z_F(s) = \frac{K_F}{s}\frac{1+s/\omega_z}{1+s/\omega_p} \tag{2.17}$$

(2.17) is readily implemented in the charge-pump PLL as shown in Figure 2.15. In this configuration, C_1 provides the required integration while the series resistor R generates the zero, ω_z, needed for loop stability. C_2 serves to reduce the voltage ripple caused by the periodic current pulses produced by the charge pump. The s-domain transfer function for the type-II loop filter impedance is given as

$$Z_F(s) = \frac{\left(\frac{1}{sC_1} + R\right)\frac{1}{sC_2}}{\frac{1}{sC_1} + \frac{1}{sC_2} + R} = \frac{C_1}{C_2}\frac{(sRC_1 + 1)}{s\left(sRC_1 + \frac{C_1+C_2}{C_2}\right)} = \left(\frac{b-1}{b}\right)\left(\frac{1}{s}\right)\left(\frac{s/\omega_z + 1}{s/\omega_p + 1}\right) \tag{2.18}$$

where $\omega_z = 1/RC_1$ and $\omega_p = b/RC_1$. The constant b is defined as $1 + C_1/C_2$, and affects loop stability and settling time (discussed in Section 2.4). In fully integrated PLLs, typically part of larger systems such as transceivers, C_1 and C_2 are generally implemented as metal-insulator-metal (MIM) capacitors, and resistors are typically made from polycrystaline silicon. Additional, out-of-band poles are often included for further suppression of charge-pump-induced ripple, thermal noise from the current sources, and higher-order DSM quantization noise.

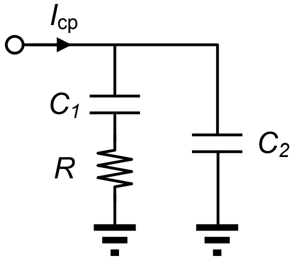

Figure 2.15: Passive loop filter for third order type-II charge-pump PLL.

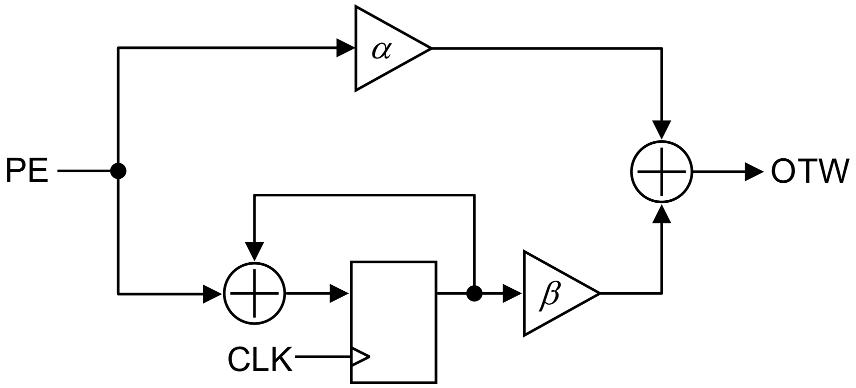

Figure 2.16: Digital PI loop filter.

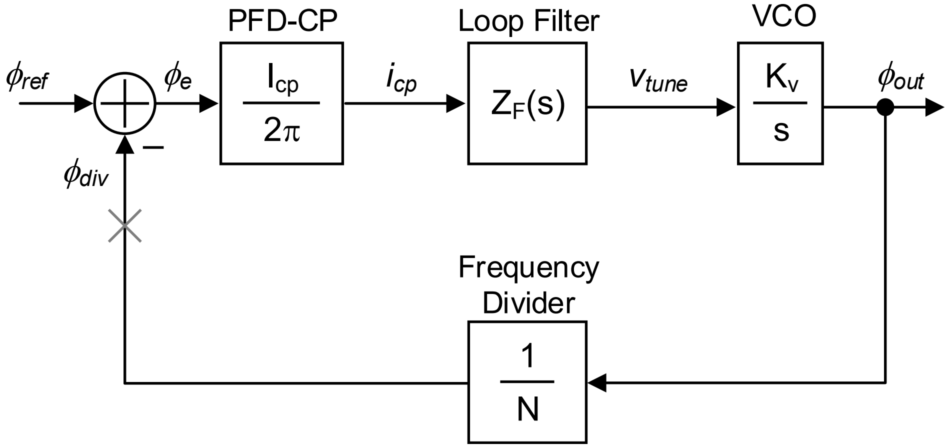

Figure 2.17: Linear model of the charge-pump PLL.

2.4 Loop Modeling

2.4.1 Linear Model

A linear, continuous-time model of the PLL, like the one shown in Figure 2.17, is typically employed in the analysis of loop dynamics and phase noise. The extent to which the linear approximation is justfied depends on the magnitude of the phase perturbations, which can generally be assumed to be small relative to the reference period. Although the charge pump PLL is in fact a sampled, discrete-time system, a linear time-invariant (LTI) approach can be safely be used as long as the loop bandwidth does not exceed approximately one tenth of the reference frequency [16]. Beyond this limit the delay introduced by the sampling action of the PFD produces a phase shift that can affect loop stability. Further, in spite of the fact that the locking process of the PLL (i.e., frequency and phase acquisition) is in general a nonlinear phenomenon, the settling to steady state of frequency and phase can be analyzed using a linear model if the transient begins sufficiently close to the final value. Additionally, certain loop characteristics of interest, such as steady-state phase error and lock-in range, are readily evaluated in this manner.

Using the linear model of Figure 2.17, developed block-by-block in the preceding section, the open-loop transfer function of the PLL can be obtained by breaking the loop as indicated in Figure 2.17, and is expressed as

$$G(s) = \frac{I_{cp} Z_F(s) K_v}{2\pi N s} \tag{2.19}$$

where I_{cp} is the charge pump current, $Z_F(s)$ is the loop filter impedance, K_v is the linear gain of the VCO, and N is the divider modulus. Typical magnitude and phase of $G(s)$ are illustrated in Figure 2.18. The closed-loop transfer function of the linearized charge-pump PLL is given by

$$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = N\frac{G(s)}{1+G(s)} = \frac{K_v I_{cp} Z_F(s)}{2\pi s + K_v I_{cp} Z_F(s)/N} = H(s) \tag{2.20}$$

A typical magnitude response for $H(s)$ is illustrated in Figure 2.19. At very low frequencies ($s \to 0$), $H(s)$ approaches N as expected. At high frequencies the response rolls off at -40 dB/dec. The amount of peaking present depends on the selection of various loop parameters, discussed below. Note that ϕ_{ref} and ϕ_{out} can be exchanged

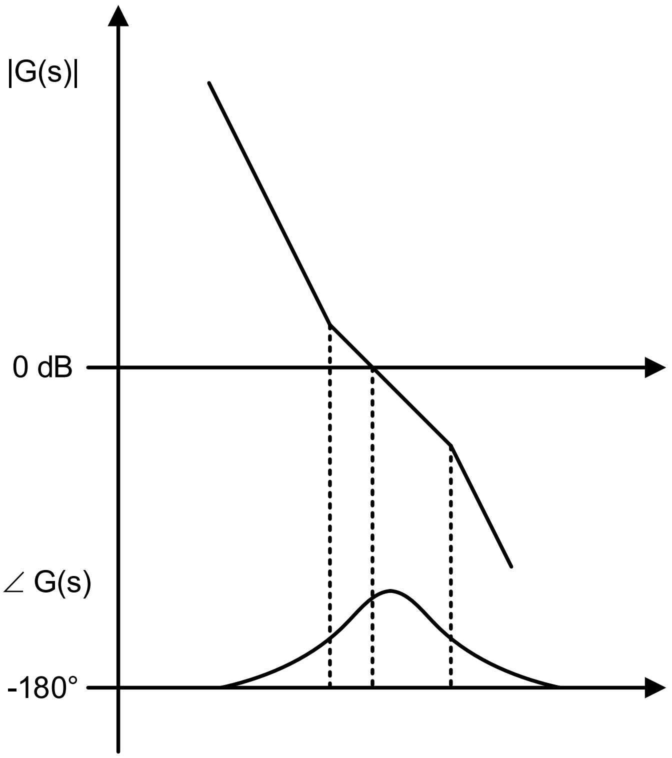

Figure 2.18: $20\log_{10}|G(s)|$ and $\angle G(s)$ for a third-order PLL.

with their frequency counterparts f_{ref} and f_{out}, and the transfer functions will be identical to (2.19) and (2.20).

2.4.2 Loop Dynamics

The linear model discussed above can be used to predict the transient response of the PLL to a change in input phase or frequency. The time the loop takes to settle to within some specified margin of the desired output frequency is often of interest when switching between RF frequency bands. The settling time can be calculated in a straightforward manner using the closed-loop transfer function $H(s)$. One particular metric of interest is the steady-state phase error that results from a step change in ei-

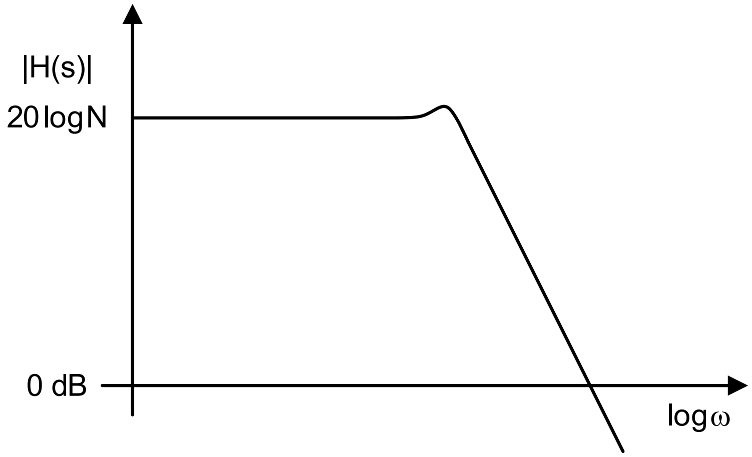

Figure 2.19: Magnitude response of $H(s)$.

ther phase or frequency. If the loop filter impedance is simply a constant independent of frequency, i.e., a resistance, $H(s)$ can be written as

$$H(s) = N\frac{G(s)}{1+G(s)} = \frac{K_v I_{cp} R}{2\pi s + K_v I_{cp} R/N} \tag{2.21}$$

(2.21) is the closed loop transfer function for a type-I (single integrator) CP-PLL. The steady-state phase error can be determined using the final value theorem, which allows the time domain behavior of the phase error to be determined from its frequency domain representation. That is,

$$\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s), \tag{2.22}$$

where $f(t)$ is the time-domain function and $F(s)$ its Laplace transform. The steady-state phase error resulting from a step change in phase (where $\phi_{ref}(s) = 1/s$) can thus be written as

$$\lim_{t\to\infty}\phi_e(t)=\lim_{s\to 0}\left[1-\frac{H(s)}{N}\right]=\lim_{s\to 0}\frac{s}{s+\frac{K_v I_{cp} R}{2\pi}}=0 \tag{2.23}$$

That is, the steady-state phase error resulting from a step change in *phase* for a type-I PLL is zero. A step change in frequency, which is equivalent to a ramp in phase, results in

$$\lim_{t\to\infty}\phi_e(t)=\lim_{s\to 0}\frac{1}{s+\frac{K_v I_{cp} R}{2\pi}}=\frac{2\pi}{K_V I_{cp} R}, \tag{2.24}$$

which is finite and depends on the loop gain of the PLL. A type-II PLL, which includes a second integrator in the open loop transfer function, responds to a frequency step with a zero steady-state phase error:

$$\lim_{t\to\infty}\phi_e(t)=\lim_{s\to 0}\frac{s}{s^2+\frac{K_v I_{cp} R}{2\pi}}=0, \tag{2.25}$$

underscoring the advantage of the type-II loop as well as the utility of the charge-pump PLL with its simple type-II loop filter.

2.4.3 Noise

Synthesizer performance requirements for narrowband wireless applications are primarily concerned with spectral purity, typically evaluated in terms of phase noise. Discussions of phase noise tend to delineate the output spectrum into two regions termed “close-in” and “far-off”or “out-of-band”. In terms of design specifications, these two regions can often be associated with specific PLL components whose noise tends to dominate that of the PLL in either one region of the spectrum or the other. The reason for this is that the loop responds differently to noise depending on where in the loop it is added. For example, as the primary role of the PLL in the present context is to provide a frequency reference whose long term behavior is more stable than that of a typical integrated oscillator operated in open loop (no feedback). The loop is used to suppress the long term variations in the output frequency due to noise sources inherent to the VCO, and thus the VCO's close-in noise is attenuated by the loop. This noise suppression, or, filtering, is generally expressed mathematically by the use of a linear time-invariant model of a feedback system.

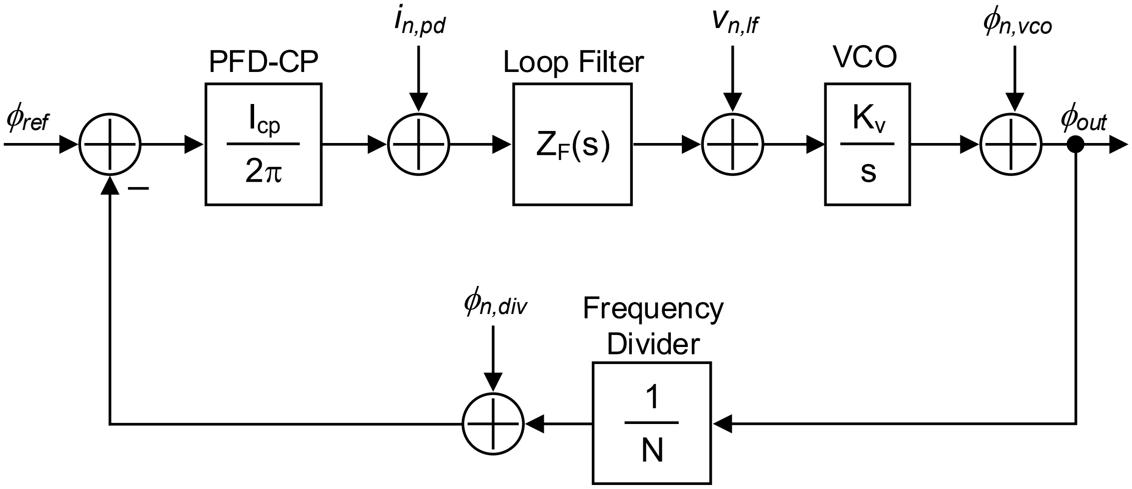

Figure 2.20: PLL linear phase-domain noise model.

The small-signal nature of typical noise sources in a PLL makes employment of the linear model presented above well-suited to phase noise analysis. Figure 2.20 details the linear phase-domain noise model of the PLL, with noise elements referred to the outputs of their respective sources. The individual noise sources can be referred to the input or the output of the PLL, depending on what is convenient for analysis. A noise source appearing at the input (or referred to the input) contributes to the phase noise at the output through the closed-loop transfer function $H(s)$. Conversely, a noise source appearing at the output of the PLL, such as the intrinsic phase noise of the VCO, is shaped by the high-pass transfer function given by

$$\frac{\phi_{out}(s)}{\phi_{n,VCO}(s)} = \frac{1}{1+G(s)} \tag{2.26}$$

That is, the noise from the VCO is attenuated by the loop at low frequency offsets (indeed, this is the purpose of the PLL), and passes directly to the output at high frequency offsets Input-referred noise sources are amplified by the divider modulus N at low offsets, and attentuated by the low-pass shape of $H(s)$ at high offsets.

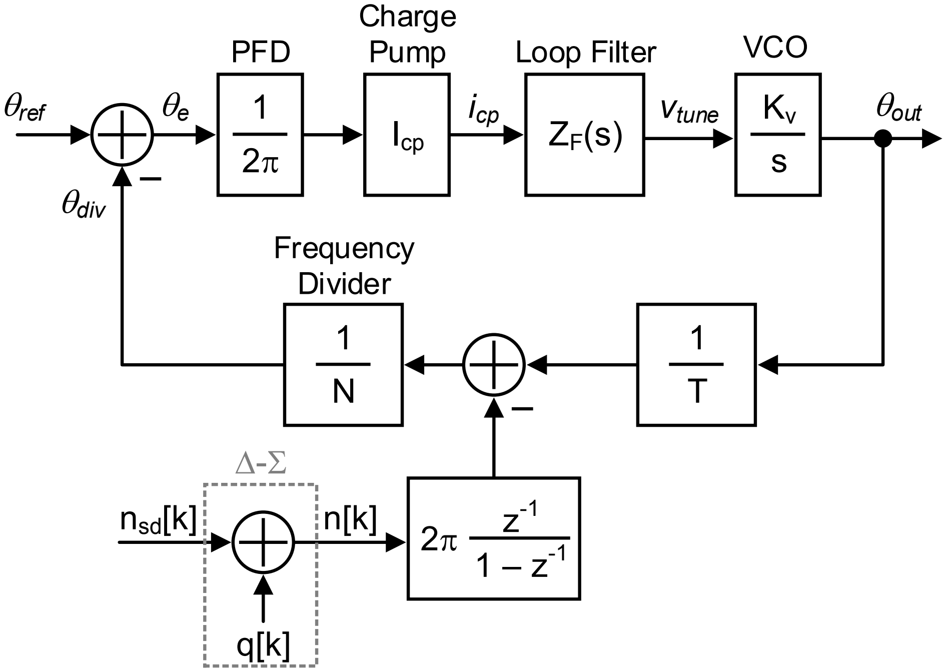

Figure 2.21: Linear frequency-domain model including Δ-Σ quantization noise.

Chapter 3

A CHARGE-PUMP FRACTIONAL-N FREQUENCY SYNTHESIZER FOR MICS APPLICATIONS

The power dissipation of the frequency multiplier-based transmitter described in Chapter 1 is the lowest reported to date for the MICS band. Further, the silicon area occupied by the frequency-multiplying TX constitutes a small fraction of the total die area due to the absence of integrated inductors, which typically dominate the size of integrated RF systems. However, a major drawback to the architecture is its reliance on a fixed integer ratio between the crystal oscillator and LO frequencies. This constraint is imposed by the extremely low "pullability" of the crystal resonator frequency, which is sufficient to allow FSK modulation at $200\,\mathrm{kbit\,s^{-1}}$, but limits operation to a single channel in the MICS band. A potential solution to this problem would be to include multiple crystals on a PCB and allow for the ability to switch between resonators (a technique employed in early FM radio design). Unfortunately, such a solution would significantly increase the size of the sensor node, in addition to its cost. Thus, the architecture is not simultaneously amenable to small form factor and shared use of the MICS band, making it impractical for commercial adoption. In addition, the frequency-multiplying approach is not readily adaptable to other frequency bands without increasing the number of delay elements in the injection-locked ring oscillator. This is due to the limited availability of quartz crystals with resonant frequencies above approximately 100 MHz. As observed in [31], increasing the number of ring elements exacerbates mismatch-related problems such as spurious tone generation, and is therefore undesirable.

Fractional-N frequency synthesis is undoubtedly the standard in RF LO generation. The primary reason for its widespread adoption is an avoidance of the tradeoff between bandwidth and frequency selectivity inherent to integer-N architectures; a tradeoff which results from the upper bound placed on loop bandwidth, for stability reasons, by the reference frequency (discussed in Chapter 2). It is this bandwidth limitation imposed on integer-N synthesizers that prevents the realization of fast start-up/locking times, a desirable feature for sensor node LO generation. Fractional-N synthesizers overcome this limitation by using a higher frequency reference clock (tens of MHz, typically the reference frequency of the PLL) to dither the instantaneous division modulus, N, of the frequency divider. Dithering results in an average value of N that depends on the duty cycle of the dither signal. A digital circuit known as a Δ-Σ modulator (pronounced "delta sigma") dithers (i.e., modulates) the instantaneous value of N in a manner that ensures that the resulting quantization noise concentrates at frequencies beyond the bandwidth of the PLL [28][38].

The vast majority of frequency synthesizers designed for RF applications employ oscillators based on resonant LC tanks. The superior phase noise performance of LC oscillators over ring oscillators and other integrated designs (for a given power dissipation) is the primary reason for their preferred use. However, the extremely small form factor of ring oscillators makes them attractive for clocking and medium-performance RF applications. Further, the large inductance value needed to achieve resonance at the relatively low frequency of the MICS band increases chip area and reduces Q factor. In addition to their size, another limitation of integrated LC oscillators is the minimum achievable power dissipation. While power can be traded with noise performance to some extent, a strict lower limit is placed by startup considerations on the current in an LC oscillator. The low data rate requirements, EIRP (equivalent isotropically radiated power limit of 25 µW), and relatively low carrier frequency (400 MHz) of the MICS band make it a potential application space for RF systems which utilize ring oscillators in the LO.

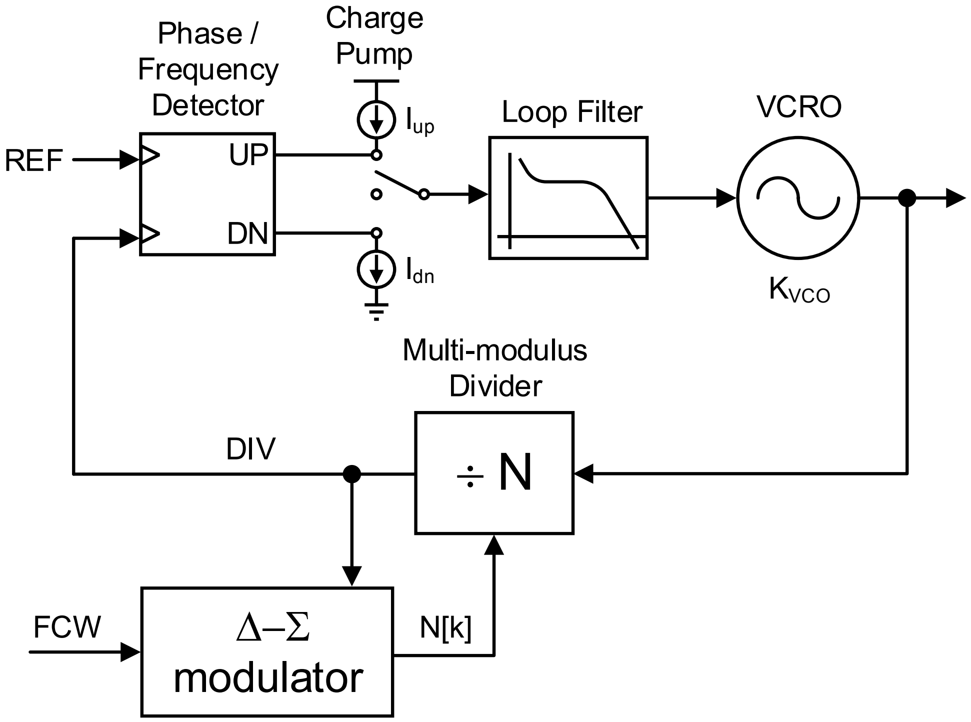

Figure 3.1: MICS band fractional-N synthesizer block diagram.

3.1 Proposed Design

In this chapter, a fractional-N synthesizer is presented which concurrently achieves low power dissipation ($< 500\,\mu\text{W}$) and small form factor ($< 0.25\,\text{mm}^2$). A voltage-controlled ring oscillator (VCRO) is used in place of an LC-VCO to limit both power dissipation and design area. In addition, a state-of-the-art deep submicron (minimum feature size of 65 nm) CMOS technology is used to ensure that the remaining blocks of the largely digital architecture constitute only a marginal increase in both the die area and power dissipation.

A block diagram of the proposed frequency synthesizer is shown in Figure 3.1. The design follows the basic fractional-N structure discussed in Chapter 2, and consists of the VCRO, phase-frequency detector (PFD), charge pump (CP), passive loop filter (LF), multi-modulus divider (MMD) and Δ-Σ modulator (DSM). Implementation details for the individual blocks are given in this section.

3.1.1 Voltage-Controlled Oscillator (VCO)

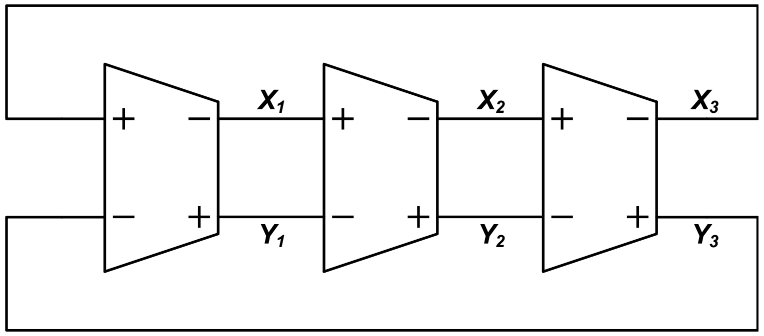

Figure 3.2: 3-stage differential ring oscillator.

The VCO comprises a 3-stage differential ring oscillator, illustrated in Figure 3.2. A schematic of the delay cell used in each of the three stages is given in Figure 3.3. The stage delay is adjusted by controlling the pull-up strength of the cross-coupled feedback pair formed by $M_{3,5}$. This is accomplished by selectively increasing or decreasing the gate bias of transistors M_4 and M_6. An increase in V_{tune} decreases the gate drive of $M_{4,6}$, limiting the current sourced by $M_{3,5}$ and increasing the stage delay. Conversely, a decrease in V_{tune} decreases the stage delay. Representing the stage delay by t_{delay}, the oscillation frequency of an N-stage VCRO is given as

$$f_{VCRO} = \frac{1}{T} = \frac{1}{2\sum\limits_{i=1}^{N} t_{delay}} \tag{3.1}$$

In the current design, the target frequency is given by

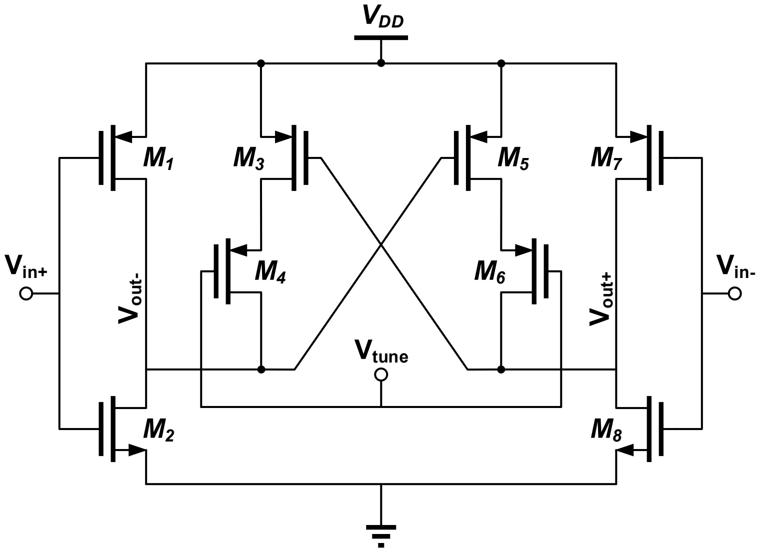

Figure 3.3: Delay cell used in the VCRO.

$$\begin{aligned} f_{VCRO} &= \frac{1}{2\sum_{i=1}^{3}(416\,\text{ps})} \\ &\approx 400\,\text{MHz} \end{aligned} \tag{3.2}$$

The stage delay, and consequently the oscillation frequency, is a strong function of supply voltage. As a result, the supply was used as a means of adjusting for process variations in the prototype design. However, a more robust method would be to include either programmable capacitance or transistor drive strength.

3.1.2 Multi-modulus Divider (MMD)

A schematic of the multi-modulus frequency divider is shown in Figure 3.4. Each stage of the divider comprises a 2/3 cell, shown in Figure 3.5. A detailed discussion of the operation of the individual divide-by-2/3 stages is given in [43]. The instantaneous division value is dithered by a third-order DSM, as described below. The MMD is an

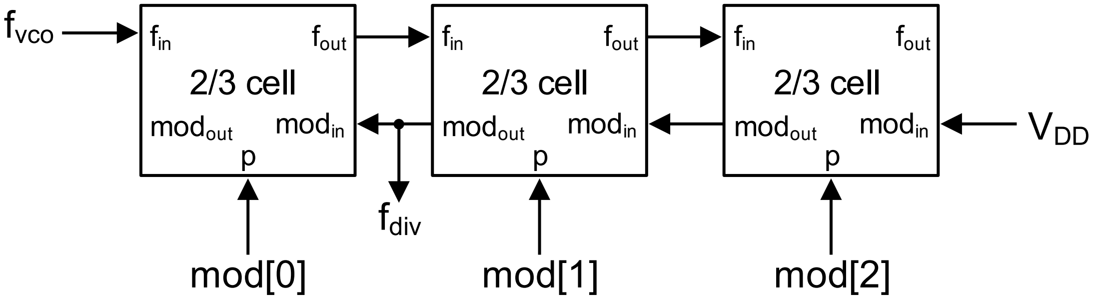

Figure 3.4: Multi-modulus divider.

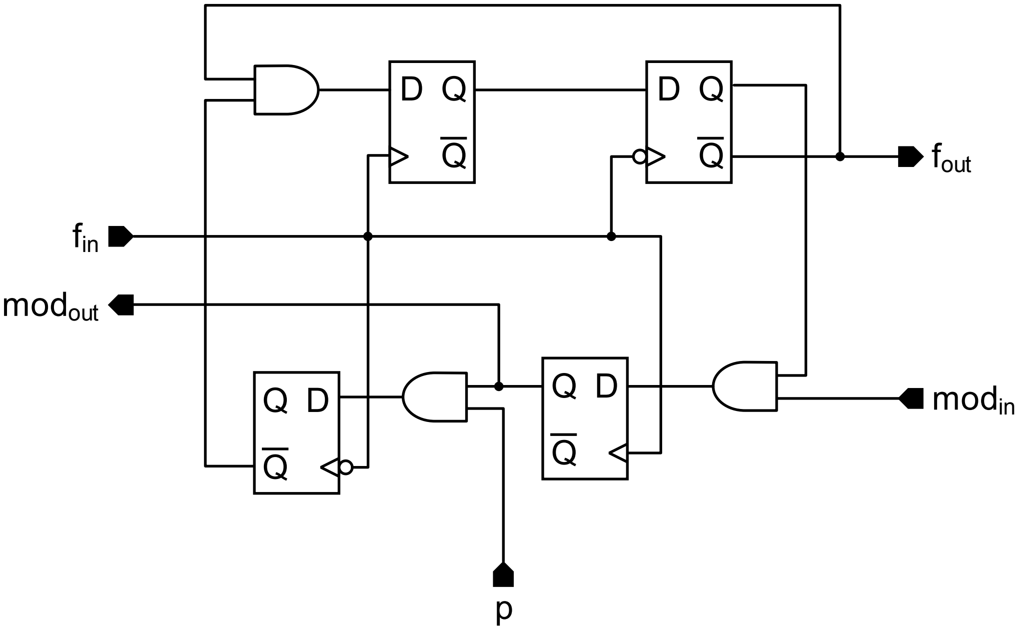

Figure 3.5: 2/3 divider cell.

all-digital design employing flip-flops and logic gates from a standard cell library in 65-nm CMOS, minimizing the power dissipation and silicon area used by the divider. Due to the high switching frequency achievable in the deep-submicron technology, no prescaler is required before the MMD. The absence of a frequency divider between the VCRO and the Δ-Σ-modulated MMD limits the amount of quantization noise seen at the output of the PLL, as discussed in Chapter 2.

3.1.3 Third-order Δ-Σ Modulator (MASH)

The instantaneous value of the 3-bit division modulus is controlled by a 3-stage MASH (for Multi-stAge noise-SHaping) Δ-Σ modulator [37], a block diagram of which is shown in Figure 3.6. The MASH DSM, in addition to the increased in-band noise suppression provided by the third order modulator, allows for the full range of the input to be utilized. In contrast, second and third order modulators such as those presented in [38] have limited input range due to saturation resulting from the presence of multiple accumulators in series. In the MASH structure, the higher order noise shaping is accomplished not by cascading multiple integrators in series, but by using the additional accumulator stages to process the quantization error from the previous stages, further reducing the close-in noise. In essence, the MASH modulator consists of multiple first-order modulators connected in parallel, whose outputs are combined together as a sum. Verilog code for the 3^{rd}-order MASH is given in Appendix A.

3.1.4 PFD / Charge Pump (PFD-CP)

The design of the phase detector follows the canonical PFD structure discussed in Chapter 2, with one important difference. In a fractional-N PLL whose divider modulus is dithered using Δ-Σ modulation, linearity is needed to preserve the shape of the filtered quantization noise so that it can be properly removed (by filtering) before appearing at the PLL output in the form of phase noise. If, instead, the high-pass filtered quantization noise encounters nonlinearity before the loop filter, various components of the high frequency noise can intermodulate, leading to significant noise folding in the passband of the PLL [33].

Inevitable mismatch between the UP and DN currents of the charge pump produces a nonlinear PFD-CP gain characteristic due to the resulting difference in the characteristic slopes for positive versus negative phase errors. In order to analyze the effect of mismatch on phase detector linearity, we can examine the change in loop

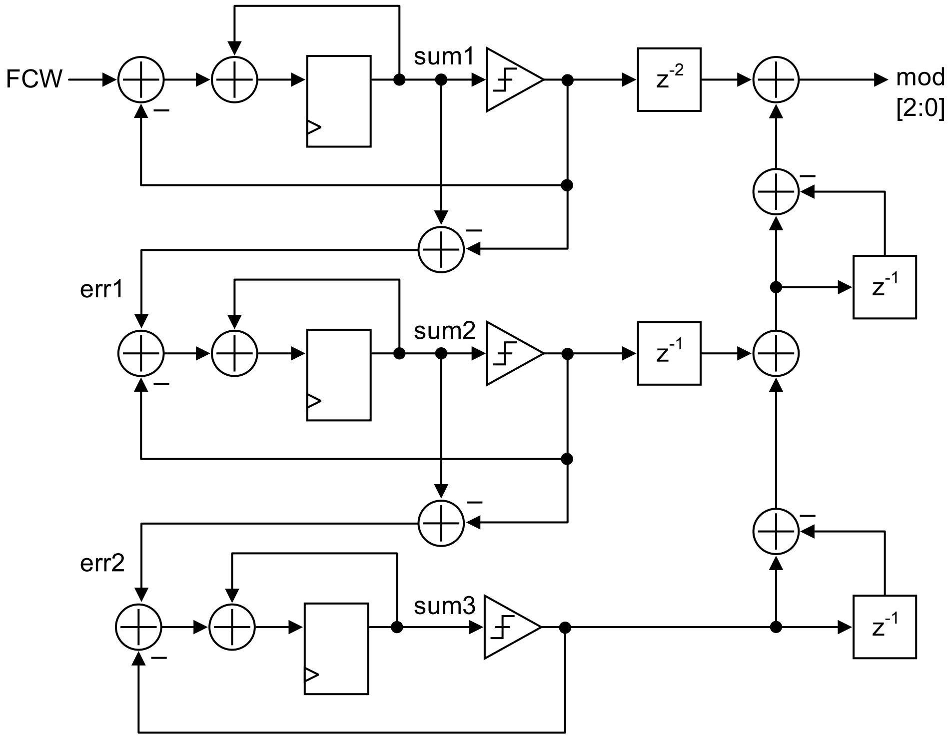

Figure 3.6: 3-stage MASH Δ-Σ modulator.

filter charge for both cases. First, we represent I_{up} in Figure 3.1 as the sum of a nominal current I_0 and mismatch current ΔI_1:

$$I_{up} = I_0 + \Delta I_1 \tag{3.3}$$

Similiarly, for I_{dn}, we have

$$I_{dn} = I_0 + \Delta I_2 \tag{3.4}$$

The mean value of the two currents, which we designate I_{cp} is given as

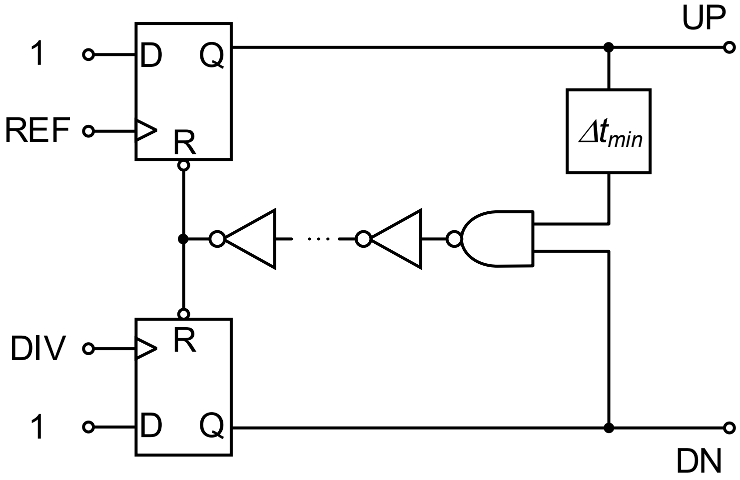

Figure 3.7: Modified PFD for fractional-N operation.

$$I_{cp} = \frac{2I_0 + \Delta I_1 + \Delta I_2}{2} \tag{3.5}$$

I_{up} and I_{dn} can thus be expressed as

$$I_{up} = I_{cp} + \frac{\Delta I_{cp}}{2} \tag{3.6}$$

and

$$I_{dn} = I_{cp} - \frac{\Delta I_{cp}}{2}, \tag{3.7}$$

where $\Delta I_{cp} = \Delta I_1 - \Delta I_2$.

Representing the phase error as $\Delta t = \theta_e / \omega_{REF}$ and the charge added/subtracted to the loop filter as ΔQ, we have, for positive phase errors (REF leads DIV in Figure 3.1, $\Delta t > 0$),

$$\Delta Q^{+} = I_{up}\Delta t = (I_{cp} + \frac{\Delta I_{cp}}{2})\Delta t, \tag{3.8}$$

where ΔI_{cp} is the mismatch between the UP and DN charge pump currents. Similarly, for negative phase errors (DIV leads REF, $\Delta t < 0$),

$$\Delta Q^{-} = I_{dn}\Delta t = (I_{cp} - \frac{\Delta I_{cp}}{2})\Delta t \tag{3.9}$$

Combining (3.8) and (3.9), the excess charge due to an arbitrary phase error is given as

$$\Delta Q = I_{cp}\Delta t + \frac{\Delta I_{cp}}{2}|\Delta t| \tag{3.10}$$

The first term of (3.10) is proportional to the phase error and constitutes a gain error (I_0 being the nominal charge pump current), while the second term is proportional to the absolute value of the phase error, contributing a nonlinearity to the phase detector characteristic. Figure 3.8 shows the dependence of error charge on phase error in the presence of charge pump current mismatch. Note that ΔQ_{max} corresponds to the error charge associated with the maximum phase error, $\theta_e = 2\pi$.

A straightforward means of linearizing the phase detector characteristic is to insert a fixed delay Δt_{min} into the feedback path of the UP signal as shown in Figure 3.7. The inclusion of Δt_{min} ensures that the two flip-flops are reset after a fixed period of time following the rising edge of the reference clock. In a fractional-N PLL using $\Delta - \Sigma$ modulation, the instantaneous period of the divided VCO clock is constantly changing. When the PLL is locked, the average period of the divider clock is equal to the reference clock, but the instantaneous phase error depends on the division

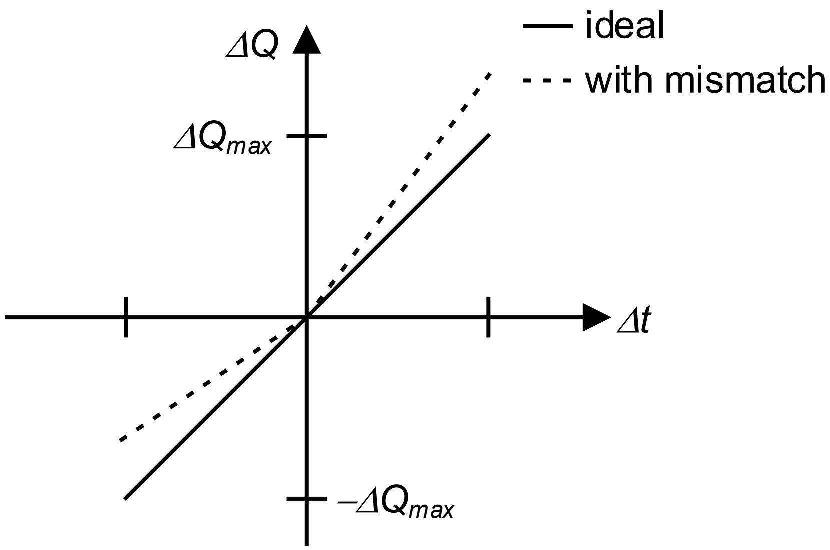

Figure 3.8: PFD-CP gain characteristic showing nonlinearity resulting from charge pump current mismatch.

modulus, and can be substantial. Δt_{min} should be greater than the maximum phase error that occurs in the locked state. Assuming this condition is satisfied, the charge added to the loop filter for a positive phase error ($\Delta t > 0$) is given as

$$\begin{aligned}\Delta Q^{+} &= (I_{cp} + \frac{\Delta I_{cp}}{2})\Delta t_{min} - (I_{cp} - \frac{\Delta I_{cp}}{2})(\Delta t_{min} - \Delta t),\\ &= \Delta I_{cp}\Delta t_{min} + (I_{cp} - \frac{\Delta I_{cp}}{2})\Delta t\end{aligned} \tag{3.11}$$

For a negative phase error ($\Delta t < 0$), the charge is given by

$$\begin{aligned}\Delta Q^{-} &= (I_{cp} + \frac{\Delta I_{cp}}{2})\Delta t_{min} - (I_{cp} - \frac{\Delta I_{cp}}{2})(\Delta t_{min} + \Delta t),\\ &= \Delta I_{cp}\Delta t_{min} + (\frac{\Delta I_{cp}}{2} - I_{cp})\Delta t\end{aligned} \tag{3.12}$$

For the linearized PFD, the excess charge due to an arbitrary phase error is thus given by

$$\Delta Q = (I_{cp} - \frac{\Delta I_{cp}}{2})\Delta t + I_{cp}\Delta t_{min} \tag{3.13}$$

Note that (3.13) consists of a linear term and and offset, and that the dependence on the absolute value of Δt, the source of the nonlinearity, has been eliminated.

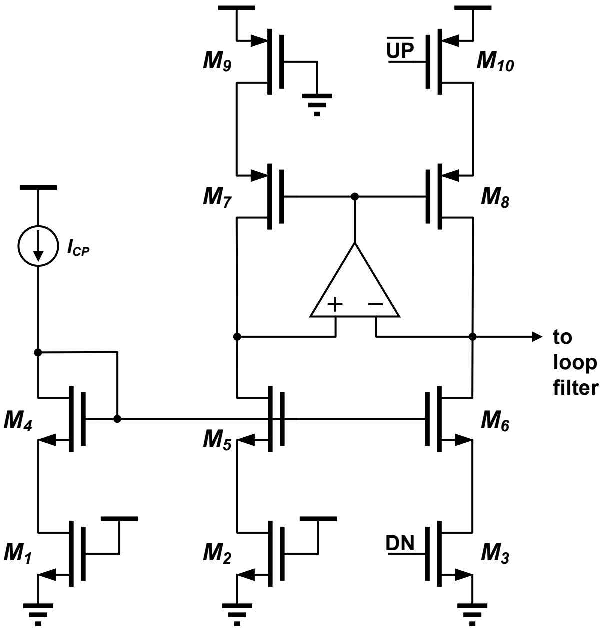

Figure 3.9: Charge pump schematic.

A schematic of the charge pump is shown in Figure 3.9. A source-switched architecture, consisting of switches $M_{3,10}$ connected to the source terminals of current sources $M_{6,8}$ (rather than their drain terminals) was used in order to improve switching speed [36]. An operational amplifier is used to ensure matching between the drain currents of M_7 and M_8, resulting equal values of I_{UP} and I_{DN}. Due to the low supply voltage (1 V), techniques commonly employed to boost the output impedance of current sources, such as cascoding, are impractical due to the additional headroom they require. The opamp, not pictured, uses a folded cascode structure with dual NMOS and PMOS input pairs. The use of dual input pairs allows the amplifier inputs and output voltage of the charge pump to swing from supply to ground while maintaining a relatively constant transconductance for the input pair(s) [2].

3.1.5 Loop Filter

The loop filter design follows the basic third order, type-II structure presented in Chapter 2, consisting of integrating capacitor C_1 and zero-stabilizing resistor R, in parallel with a second capacitor C_2 to reduce control voltage ripple. In order to further reduce movement of the VCO control voltage resulting from $\Delta - \Sigma$ dithering, an additional RC filter was inserted between the basic filter and the VCO.

3.2 Experimental Results

The proposed design was fabricated in a 65-nm CMOS process. The complete circuit draws 400 µA from a 1.1 V supply, resulting in a total power dissipation of 440 µW (of which approximately 75% is due to the VCO). The circuit occupies a silicon area of 0.3 mm^2, more than half of which is consumed by the capacitors of the integrated loop filter. A micrograph of the design is shown in Figure 3.10. The phase noise spectrum of the synthesizer operating in fractional-N mode is shown in Figure 3.11. Salient features of the noise plot include the $1/f^3$ region at low offset frequencies and the small “hump” appearing near 10 MHz offset from the carrier. This additional region of elevated output noise is due to the quantization noise-shaping action of the Δ-Σ modulator. In order to avoid stabilty problems, the order of the on-chip loop filter was limited to 2 poles. For a loop with a 3^{rd} order modulator, at least 3 poles are needed to adequately suppress this noise. A performance summary of the synthesizer is given in Table 3.1. The design is compared with several other state-of-the-art MICS

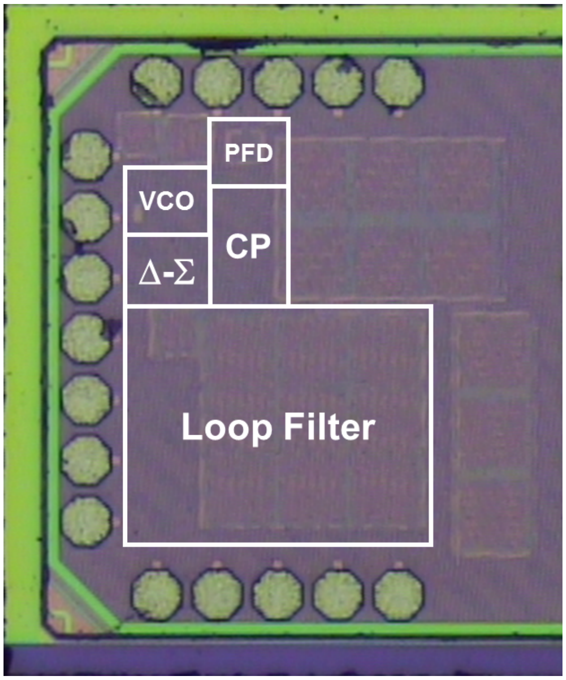

Figure 3.10: MICS band synthesizer chip micrograph.

band synthesizers in Table 3.2.

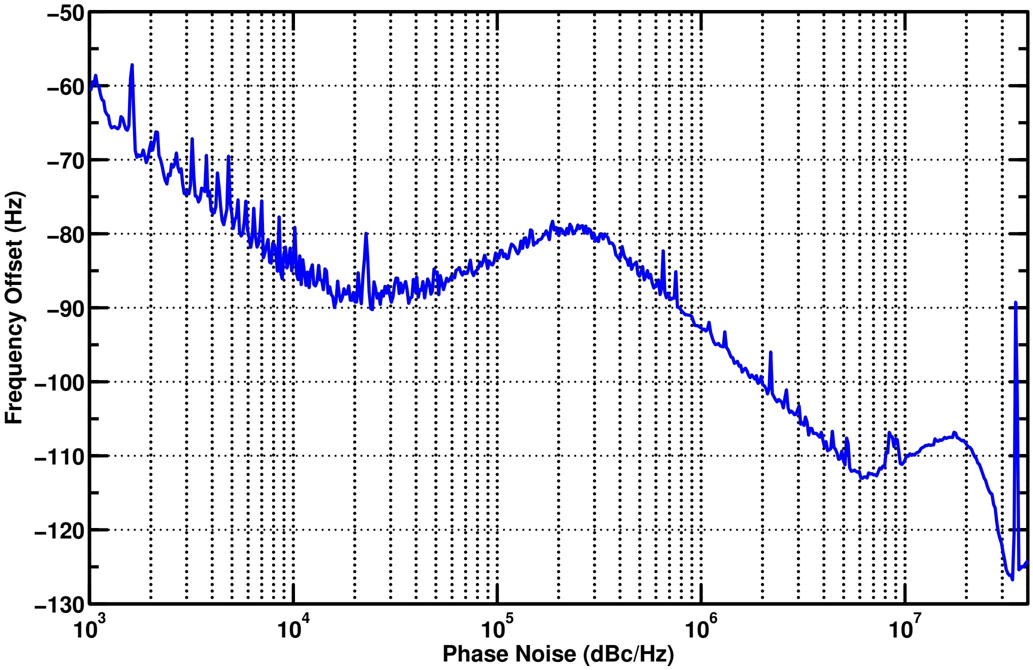

Figure 3.11: Fractional-N phase noise at 402.5 MHz.

Table 3.1: MICS band synthesizer design summary

Technology	65-nm CMOS
Chip area (mm^2)	0.3
Reference frequency (MHz)	35
Output frequency (GHz)	0.4
Power dissipation (µW)	440
VCO	350
PFD/CP	50
DIV/DSM	40
Phase noise (dBc/Hz)	-93 @ 1 MHz

Table 3.2: MICS PLL Performance Comparison

	[9]	[45]	[23]	This Work
Technology	130-nm	65-nm	180-nm	65-nm
Chip area (mm^2)	0.07	0.54	0.14	0.3
Architecture (MHz)	int-N	int-N	frac-N	frac-N
Output frequency (MHz)	400	400	400	400
Power dissipation (µW)	440	430	700	440
Phase noise @ 1 MHz (dBc/Hz)	-91.5	-100	-92.5	-93

From the 600-mV supply (V_{DDH})

Chapter 4

AN ULTRA-LOW-VOLTAGE ALL-DIGITAL PLL

Battery-free operation remains a significant challenge in the development and proliferation of short-haul wireless sensor systems whose continuous operation is crucial. The concurrent requirements of long (ideally indefinite) lifetime and small form factor associated with many wireless sensor applications do not align well with current battery technology, and ambient energy harvesting has shown promise as a means of providing energy indefinitely to such devices [3]. To date, most systems powered in this manner employ voltage-boosting circuits to generate supply voltages amenable to standard CMOS circuit architectures. In addition to increasing design complexity and chip area in order to accommodate DC-DC conversion circuits, operation at supply voltages much higher than the minimum required by the application introduces power overhead that could be alleviated by developing design techniques that make feasible operation at much lower voltages. Moreover, as shown in Chapter 1, the limited efficiency of voltage-boosting circuits further decreases the available node power.

In this chapter a 2 GHz all-digital phase locked loop (ADPLL) whose core components operate from a 300-mV supply is presented. Ultra-low voltage frequency division and phase/frequency quantization are performed by a ring oscillator that is superharmonically injection-locked to the digitally-controlled oscillator (DCO). An injection-locking technique is proposed which facilitates locking with no additional active devices, minimizing capacitive loading and maximizing the oscillation frequency of the divider at low voltage. The ADPLL is fabricated in a 65-nm CMOS process, and consumes a total of 780 µW, 720 µW from a 300-mV supply (V_{DDL}) and 60 µW from a 600-mV supply (V_{DDH}).

Several ultra-low voltage (i.e., sub-500-mV) CMOS radios have appeared in the literature [12][46]. The demonstration of a frequency synthesizer suitable for wireless applications and capable of operation at comparable supply levels, on the other hand, has been lacking. Prior to the current work, the lowest reported supply voltage for a multi-GHz RF frequency synthesizer was 500 mV [40]. Ultra-low-voltage charge-pump PLL's typically suffer from high VCO gain and, consequently, either sub-optimal loop dynamics or reduced charge pump current and increased phase noise [10]. Supply voltages as low as 300 mV supply precludes the use of traditional charge pump designs, since this value serves as the lower bound of what is required to maintain saturation operation for two stacked MOS transistors. In addition, RF frequency division is a significant challenge in the near- and subthreshold CMOS regimes, due to low overdrive and limited headroom. An all-digital synthesizer architecture inspired by [42] is proposed here as a means of circumventing the dynamic range penalties associated with low-voltage analog designs. We also present an injection-locking technique suitable for multi-GHz frequency division at ultra-low voltages.

4.1 Circuit Implementation

4.1.1 ADPLL Architecture

A block diagram of the all-digital frequency synthesizer is shown in Figure 4.1. DCO frequency evaluation is performed by combining the results of two separate measurements, referred to here as coarse and fine frequency measurements. Coarse estimation is provided by counting the number of output transitions of a divide-by-17 injection-locked ring oscillator (ILRO) that occur within each reference period. The fine measurement utilizes the multi-phase nature of the ILRO to achieve a resolution $2N$ times that of the coarse measurement, where N is the number of ILRO stages (17, in this case). An arithmetic frequency detector is used to compare the frequency control

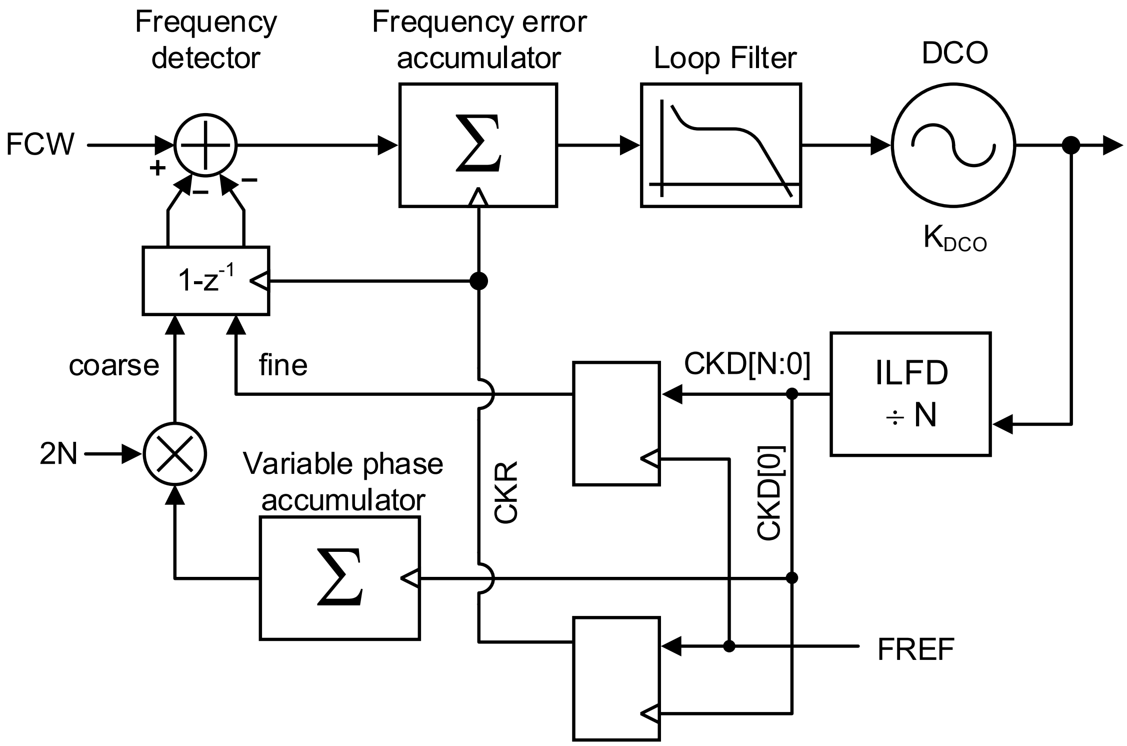

Figure 4.1: Low-voltage ADPLL block diagram.

word (FCW) with the quantized DCO frequency measurement, where the FCW is equal to 2 times the ratio of the desired output frequency to the reference frequency. The accumulated frequency error provides an estimate of the phase error, which is processed by the digital loop filter. The loop filter includes both a proportional path for Type-I operation and an integral path for Type-II. The PI filter is followed by two IIR filters for additional noise suppression. Shaded grey blocks correspond to synthesized logic operating from a 600-mV supply. Although there is no reason to believe that these blocks couldn't also be powered by the 300-mV supply, digital timing models were unavailable for this voltage during the design process.

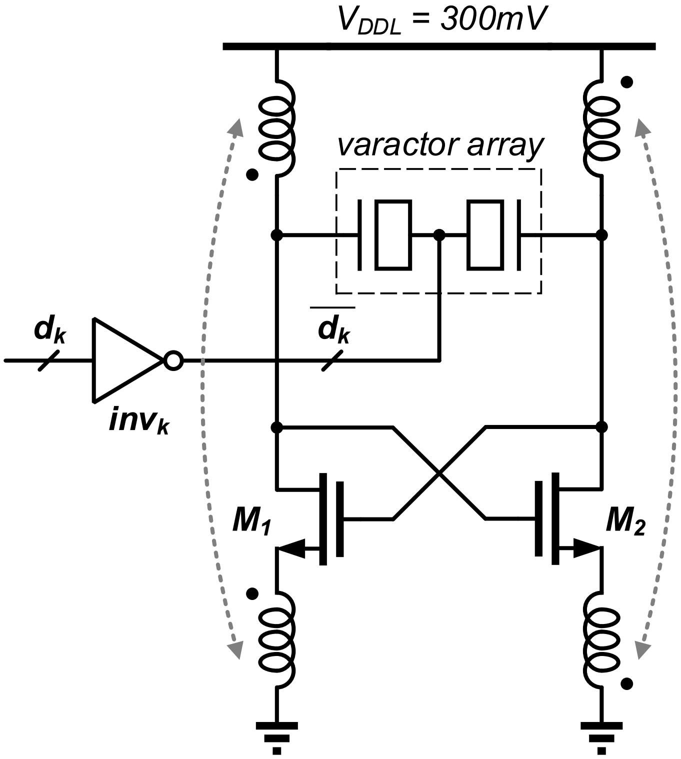

Figure 4.2: Transformer-feedback DCO schematic.

4.1.2 Transformer-feedback DCO (TF-DCO)

A circuit schematic for the DCO is shown in Figure 4.2. This oscillator employs the transformer-feedback approach outlined in [25], which increases the signal swing for a given supply voltage by magnetically coupling the drain and source nodes of M_1 and M_2. This technique improves noise performance and reduces the minimum supply voltage needed to sustain oscillation, allowing operation from the 300-mV supply. Coarse- and fine-tuning of the TF-DCO frequency are accomplished by switching the bottom plates of an array of MOS capacitors between V_{DDH} and ground. Using this method, a tracking gain of $K_{DCO} \approx 33\,\text{kHz/LSB}$ is achieved. The center frequency of the DCO can be adjusted via the on-chip serial-parallel interface.

4.1.3 Injection-locked frequency divider (ILFD)

The reduced current sourcing capabilities of MOS transistors operating in moderate or weak inversion makes the employment of conventional CMOS prescalers (static/dynamic latches) infeasible at multi-GHz frequencies for supply voltages in the vicinity of threshold (approximately 400 mV for this process). High-speed alternatives such as CML dividers are also impractical at low voltage due to voltage headroom concerns. The maximum input frequency for a TSPC register employed as a frequency divider is limited by the sum of the propogation delay through the latch and its setup time. From Figure 4.3 this can be seen to be approximately equal to

$$\begin{aligned} T_{in,min} &= t_{prop} + t_{setup} \\ &= 3\Delta t_{inv} \end{aligned} \tag{4.1}$$

(4.1) is slightly optimistic, as the presence of the precharge device (M_2) adds additional parasitic capacitance which further increases the delay through the latch and reduces the maximum input frequency to the divider. In addition to speed, the power dissipation of the frequency divider is also of interest. The dynamic power consumption of the TSPC divide-by-2 circuit is given by

$$\begin{aligned} P_{N=2} &= 3 \times C_{unit} {V_{DD}}^2 \frac{f_{in}}{2} \\ &= 1.5 \times C_{unit} {V_{DD}}^2 f_{in} \\ &= 1.5 \times P_{inv} \end{aligned} \tag{4.2}$$

That is, the power consumption of the divide-by-2 circuit is given approximately by that of 1.5 inverters toggling at the input frequency. In order to achieve division by values greater than 2, multiple such divide-by-2 circuits can be cascaded, as shown in Figure 4.4. In this case, the precharge transistor of each stage constitutes an additional

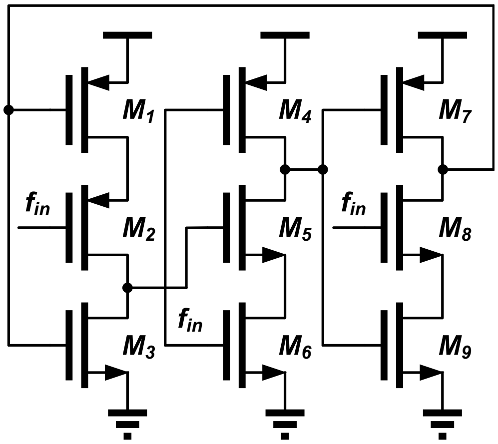

Figure 4.3: TSPC divide-by-2.

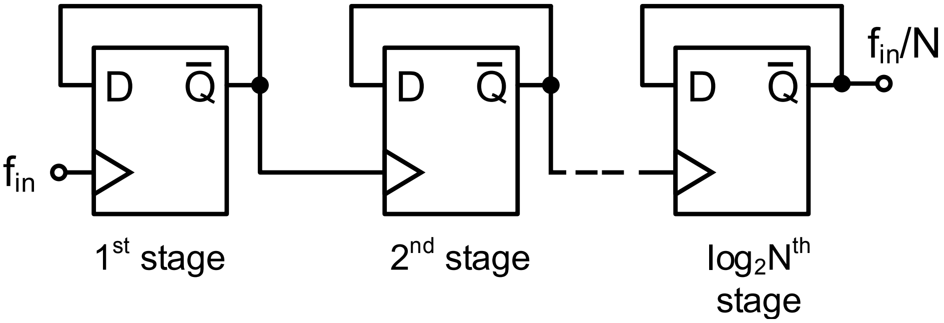

Figure 4.4: Division by N using cascaded divide-by-2 stages.

capacitive load to the preceding stage. The power consumption of a chain of divide-by-2 stages is given by a geometric series and saturates for values of N greater than approximately 16. Assuming this additional device presents a capacitance equal to $0.5 \times C_{unit}$, the power dissipated by the cascade is given by

$$
\begin{aligned}
P_N &= \frac{3.5}{2} C_{unit} {V_{DD}}^2 f_{in} \sum_{k=0}^{\log_2 N-1} \left(\frac{1}{2}\right)^k \\
&\approx 1.75 \times P_{inv} \left(1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right) \\
&\approx 3.3 \times P_{inv}
\end{aligned} \tag{4.3}
$$

In other words, for division by 16 (or higher), the power consumption of a cascade of dynamic divide-by-2 stages is approximately equal to the power dissipated by 3.3 inverters toggling at the input frequency. Due to the reduced frequency, additional stages contribute negligibly to the total power dissipation.

Injection-locked frequency dividers (ILFD) have often been touted as viable low-power alternatives to traditional approaches for high frequency division. The 3-stage ring oscillator shown in Figure 4.5 can be configured as a divide-by-3 circuit by injecting an RF current to a node common to each of the delay cells (e.g., the common source of either the NMOS or PMOS transistors in the ring, as suggested in the figure, with the individual ground connections to $M_{2,4,6}$ removed). In order to lock, the input period must satisfy the approximate relation given by

$$
T_{in} \approx 2\Delta t_{inv} \tag{4.4}
$$

That is, an injection-locked frequency divider based on a 3-stage ring oscillator can divide frequencies more than 1.5 times higher than those of which the TSPC divider is capable. A similar observation regarding the maximum input frequency of a divide-by-2 stage has also been made in [13], in which the dynamic frequency divider is likened to a 3-stage ring oscillator. The injection-locked divider also offers an rather substantial advantage in terms of power consumption. Using the divide-by-3 circuit shown in Figure 4.5, the power consumption can be computed by noting that there

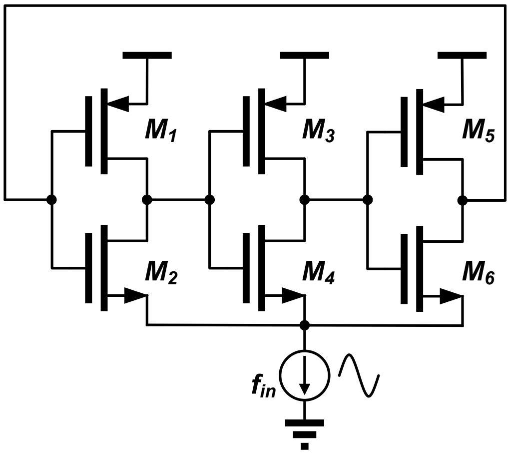

Figure 4.5: 3-stage ring oscillator for divide-by-3.

are three inverter stages toggling at the divided down frequency, f_{in}/N. As such, the power consumption of the injection-locked divide-by-3 stage is given by

$$\begin{aligned} P_{N=3} &= 3 \times C_{unit} {V_{DD}}^2 \frac{f_{in}}{3} \\ &= P_{inv} \end{aligned} \tag{4.5}$$

For division by N, where N is equal to the number of delay stages of the ring oscillator and is necessarily an odd number for single-ended designs, the power consumption is given as

$$\begin{aligned} P_{N} &= N \times C_{unit} {V_{DD}}^2 \frac{f_{in}}{N} \\ &= P_{inv} \end{aligned} \tag{4.6}$$

That is, the power dissipated by an injection-locked divider is precisely equal to that of a single inverter toggling at the input frequency. This result is independent of the value of N, as demonstrated by Equation (4.6). This is due to the fact that as the number of delay stages is increased, N also increases, and the oscillation frequency is reduced.

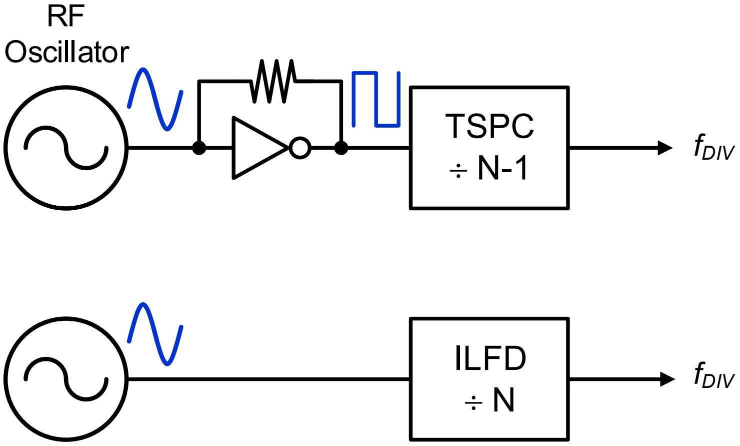

Figure 4.6: Interfacing the frequency divider with the VCO.

This trend can be exploited to reduce the power dissipated by the circuitry following the ILFD (e.g., an accumulator). An additional advantage of the ILFD is its ability to be driven directly by the VCO output, obviating the use of additional buffers that would be needed to produce a CMOS-friendly rail-to-rail signal (Figure 4.6). This constitutes an additional power savings equivalent to that of at least one inverter toggling at the RF (input) frequency. The power dissipated by the two different divider designs is plotted (normalized to P_{inv}) versus N in Figure 4.7. As discussed, the ILFD power remains a constant, regardless of the value of N, while the power of latch-based design grows as a geometric series with N. Including the additional power needed for the interface buffer, the power of the TSPC design saturates at approximately $4.3 \times P_{inv}$, more than 4 times higher than that of the ILFD. Reducing the effective number of devices operating at the RF frequency is of critical importance for energy-conscious designs.

A phase shift is required for the loop to oscillate at ω_1 instead of ω_0, where ω_0 is the free-running frequency and ω_1 is equal to or a subharmonic of the injection frequency. The required phase shift is typically achieved by “injecting” a current at the RF frequency into an appropriate node of the oscillator. A common means of

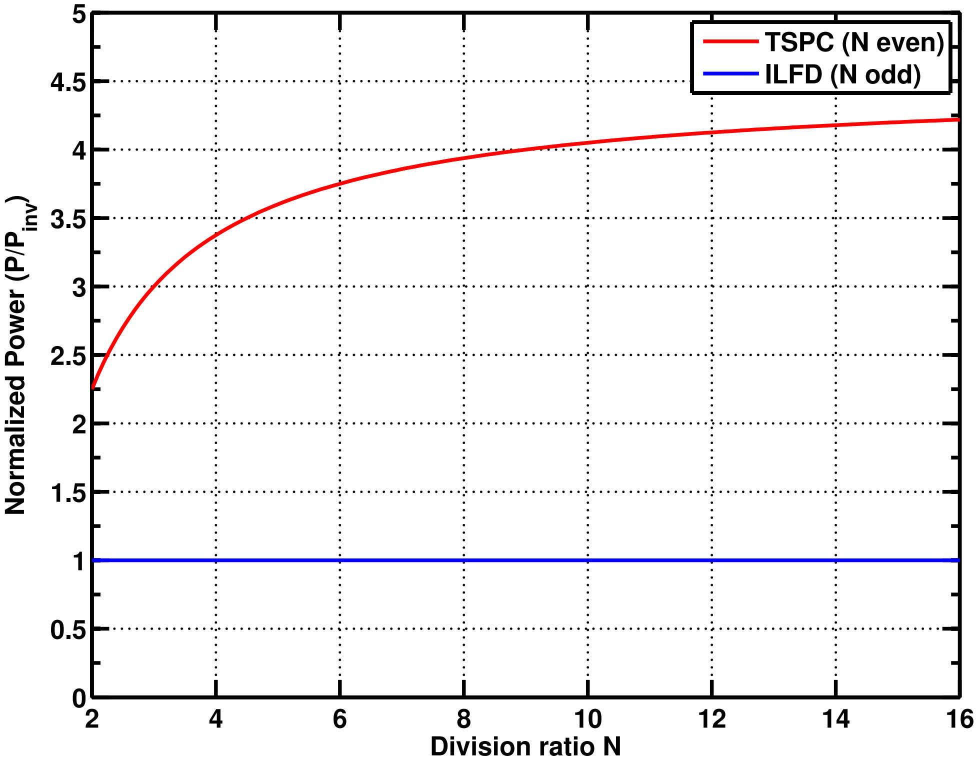

Figure 4.7: Power comparison for ILFD vs TSPC dividers.

achieving this is to include a tail transistor whose drain current contains both DC and RF components [8]. However, the stacking of additional transistors significantly limits the speed of the ring at low voltage. In the proposed design, RF current injection is achieved by applying the RF voltage directly to the bulk of the ring devices. The shared bulk implants of the NMOS and PMOS devices are AC-coupled to the source node of either M_1 or M_2 in TF-DCO (Figure 4.2) in order to minimize loading of the DCO tank and to minimize any forward bias of the source-to-bulk and drain-to-bulk junctions of the ring transistors. The proposed technique is illustrated in Figure 4.8. Bias voltages V_{BP} and V_{BN} can be adjusted between V_{DDL} and ground to control the free-running frequency of the ring. Thus, the free-running frequency can be calibrated to center the locking range near the desired frequency. In the current realization, these bias voltages were manually adjusted off-chip to obtain the desired frequency. However, the digital nature of the design makes it possible to accomplish this tuning in a closed-loop fashion as an automatic calibration. This calibration method is discussed further in Chapter 5.

As a performance metric of particular interest in injection-locked oscillators, the lock range of the ILFD can be evaluated with the aid of the perturbation projection vector (PPV) concept described in [14], which is equivalent to the better-known (numerical) impulse sensitivity function (ISF) [21]. The PPV provides a means of characterizing the response of a oscillator's phase to small perturbations, including those which are periodic. In order to lock to a given subharmonic of the input frequency, the PPV, which is a periodic function, must contain Fourier components near the fundamental frequency of the input. The required proximity to the fundamental depends on the ratio of the injection current amplitude to that of the free-running oscillator. The proposed injection method effectively achieves multiple phase injection, which widens the lock range by increasing the total phase shift due to injection [29]. This effect can also be explained using the PPV concept. The effective PPV of an oscillator under multi-input injection can be determined by summing the individual PPVs of the various nodes under injection. Due to the phase relationships between the different nodes of the ring oscillator, the combined PPV exhibits significant spectral content at the N^{th} harmonic of the fundamental frequency, while other harmonics are suppressed. These two characteristics (respectively) increase the lock range for division by N and decrease the lock range for division by other values, making it possible to achieve a wide lock range even when N is large. As remarked previously, because the power dissipation in the ILFD is independent of the number of stages, a higher division ratio may be employed to reduce the dynamic power usage in the digital circuitry needed to interface with the divider, particularly the counter used for coarse frequency measurement.

The method of injection locking employed in the present design utilizes the bulk-

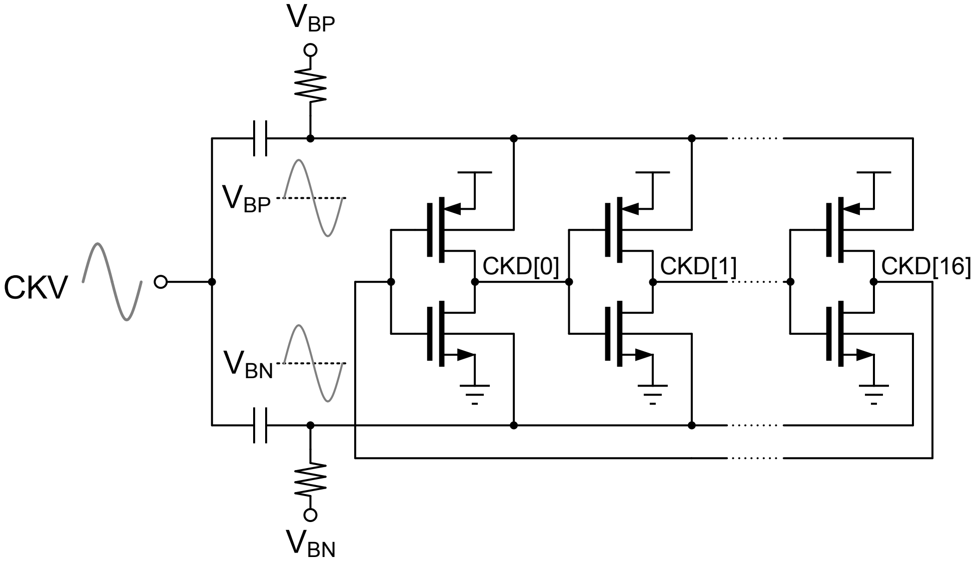

Figure 4.8: Injection-locked frequency divider.

source transconductance (g_{mb} in the linear model) as a means of avoiding the reduction in oscillation frequency associated with the addition of a tail current source (Figure 4.5) or transistors in parallel with the ring devices.

4.1.4 Phase Quantization

The phase accumulating nature of the ring oscillator makes measurement of the DCO phase/frequency possible without requiring a counter operating at the RF frequency. This is in general true of any frequency divider, but the additional phases of the ring increase the resolution of this measurement from NT_{DCO} to $T_{DCO}/2$. The method of fine phase/frequency quantization using the multiple phases of the ILFD is shown in Figure 4.10. The digital word consisting of bits D[16] through D[0] uniquely determines the oscillator state at the rising edge of CKR. Each state measurement is subtracted from the previous state index to determine the number of (excess) DCO half-periods that have elapsed during the last reference cycle. The frequency measurement is subsequently used to provide an estimate of the DCO phase, which is used in the calculation of the phase error. It is well known that the in-band phase noise of a TDC-based ADPLL is typically dominated by the quantization error associated with this measurement [42]. An inspection of (4.7) reveals that under injection locking, the in-band noise is independent of both the DCO period and the resolution of the phase error measurement and depends only on the sampling (reference) frequency. Note that because the DCO frequency measurement is taken as the difference between two independent measurements, the quantization noise power is twice that of the single measurement case for the same resolution. It should be noted that in practice, the first-order differencing operation is only required for the fine measurement (otherwise the measured values are ambiguous).

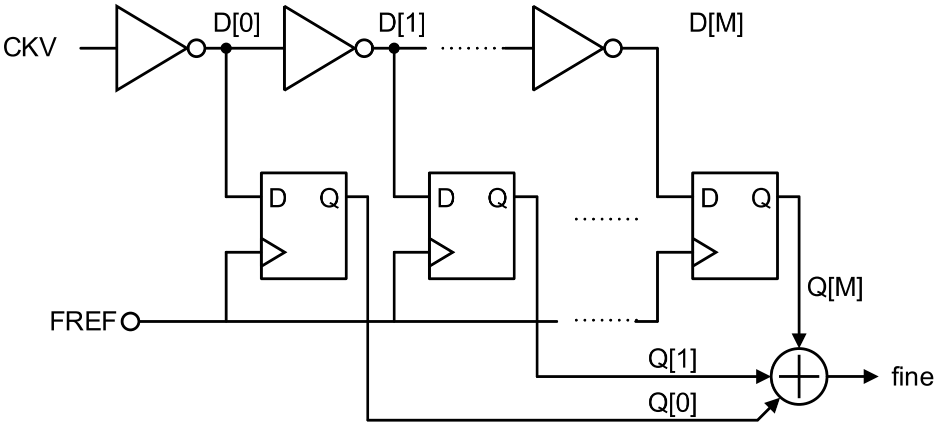

Figure 4.9: Conventional TDC.

$$L(\Delta f) = \frac{(2\pi)^2}{12}\left(\frac{\sqrt{2}\Delta t_{inv}}{T_{DCO}}\right)^2\frac{1}{f_{ref}} = \frac{(2\pi)^2}{12}\left(\frac{1}{\sqrt{2}}\right)^2\frac{1}{f_{ref}} \tag{4.7}$$

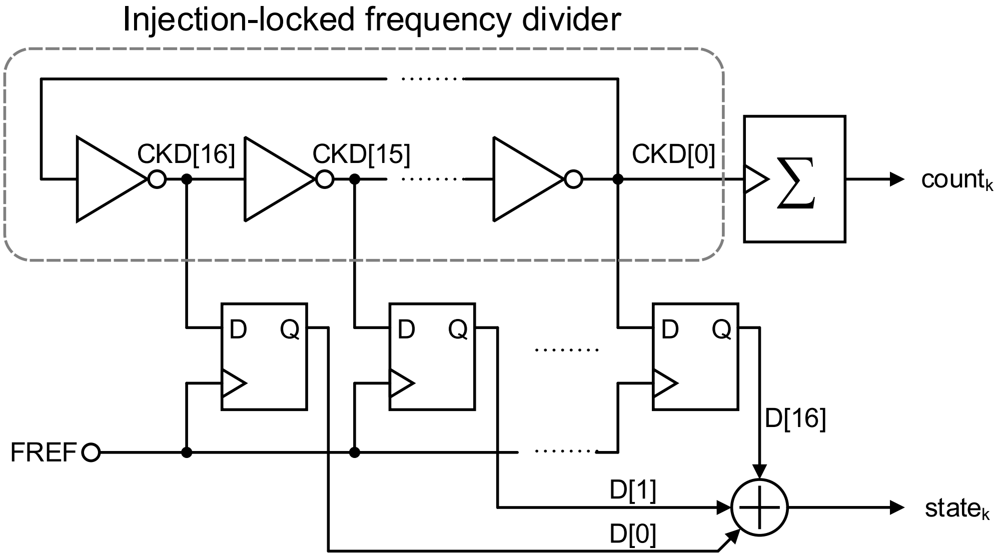

Figure 4.10: Method of phase quantization.

4.2 Experimental Results

A prototype of the design was fabricated in a general-purpose 65-nm CMOS technology. Low-V_t devices were employed in the TF-DCO and ILFD/PQ blocks. The circuit occupies an area of $0.552\,\text{mm}^2$, and its size is largely dominated by the transformers, as seen in the die photo (Figure 4.11). Measured output spectrum and phase noise of the ADPLL clocked by a 10 MHz reference and providing a 2.04 GHz output are shown in Figures 4.12 and 4.13, respectively. Equation (4.7) predicts an in-band noise level of −67 dBc/Hz, and best-case measurement results are within a few dB of this value (Figure 4.13). Figure 4.14 gives the measured phase noise as a function of output frequency at 10 kHz offset from the carrier. The lowest in-band phase noise is achieved when the output frequency is equal to $2kN$ times the reference frequency, where k is a positive integer. Mismatch between the delay stages of the ILFD increases the noise for other values of the FCW. In-band noise increases at the edges of the ILFD lock range, which can be inferred from Figure 4.14. The rather modest lock range exhibited by the design (around 80 MHz) results from the capacitive division that occurs when the DCO is AC-coupled to the bulk junctions of the ILFD devices. A larger coupling capacitance (C_c) would increase the lock range at the expense of additional (capacitive) loading to the DCO. A small value of C_c (1.2 pF) was used here as a result of having a fixed transformer inductance, resulting in division by approximately 3. Table 4.1 gives a performance summary of the design.

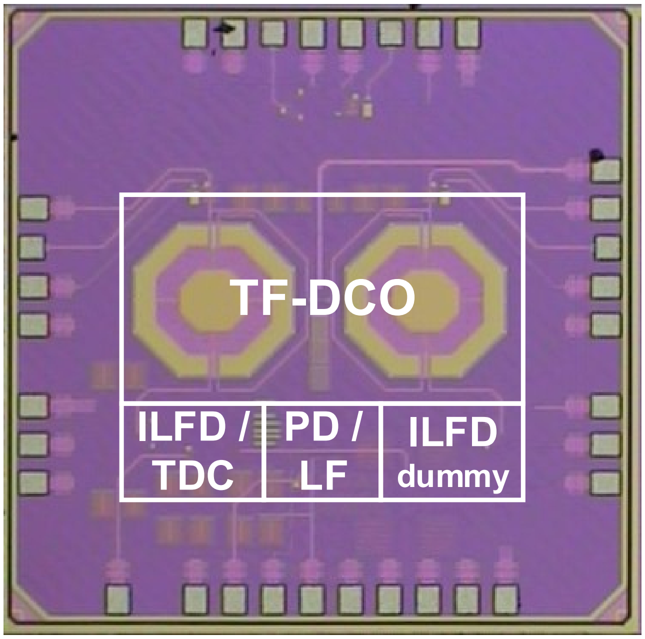

Figure 4.11: Chip micrograph.

4.3 Conclusion

An all-digital frequency synthesizer with critical components operating at 300 mV has been presented. A technique which facilitates injection-locking via the common bulk of the transistors in a ring oscillator has been proposed. The technique facilitates multi-GHz frequency division at near- and subthreshold supply levels and does not

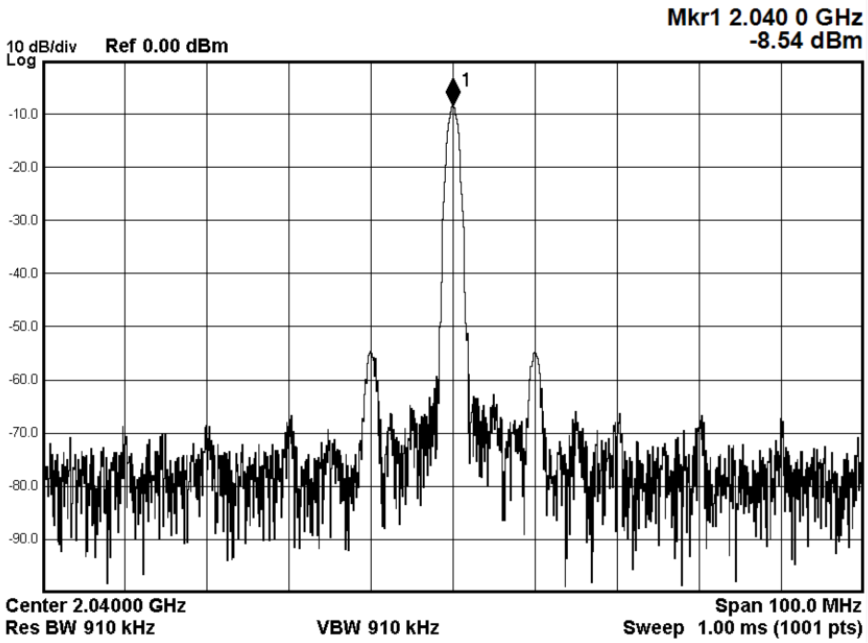

Figure 4.12: Measured output spectrum at 2.04 GHz

require additional devices in the ring. Further, exploitation of the phase locking of the ILRO to the DCO provides a means of performing phase/frequency estimation without requiring a separate quantizer.

It should be noted that comparable, or, indeed, better performance is achievable with typical supply levels and with similar power numbers, as in [11]. The aim of the present work was to explore the feasibililty of performing RF synthesis at voltage levels charateristic of various low-voltage energy harvesters. The use of a 300-mV supply necessitates larger aspect ratios in the ILFD delay cell transistors in order to guarantee a minimum inverter delay in the face of process variations and parasitic loading. The increased device sizes lead to higher power dissipation in the divider than what may be possible at higher supply levels. Further, it is clear that the proposed method of phase/frequency quantization sets a limit on the achievable close-in phase noise performance, in contrast with charge-pump based designs whose close-in noise

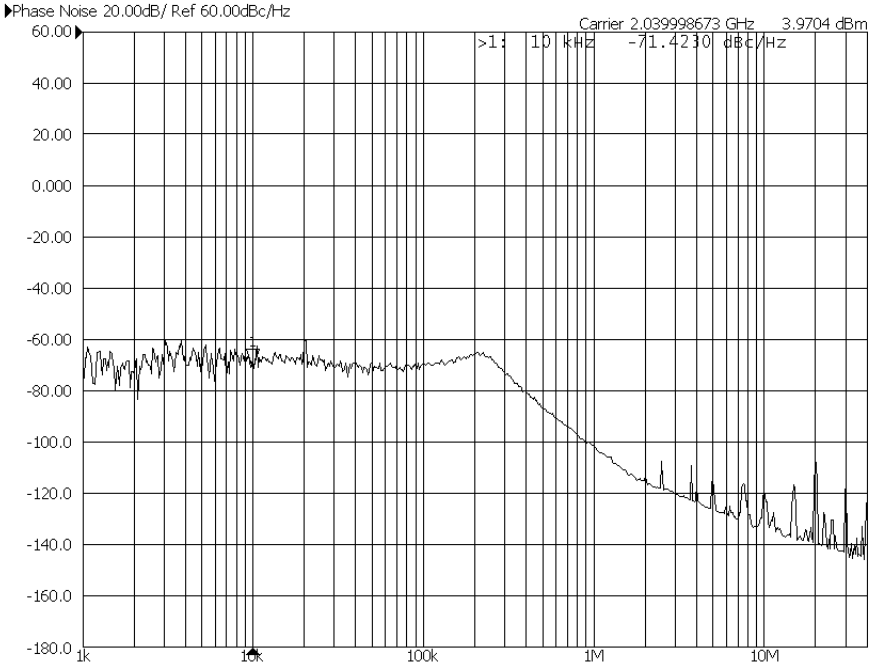

Figure 4.13: Measured phase noise.

can be reduced by trading it for increased power consumption. However, operating directly from harvested voltages offers the potential of eliminating the power overhead associated with voltage-boosting circuits.

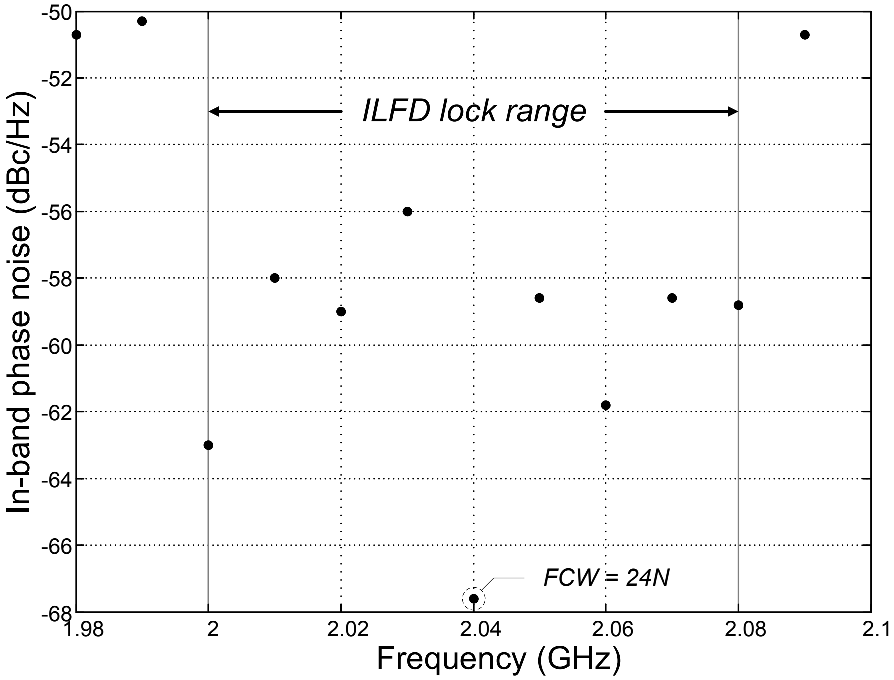

Figure 4.14: Phase noise versus frequency.

Table 4.1: ADPLL design summary

Technology	65-nm CMOS
Chip area (mm^2)	0.552
Reference frequency (MHz)	10
Output frequency (GHz)	2–2.08
Power dissipation (µW)	780
TF-DCO	600
ILFD/PQ	120
PD/LF	60[1]
Phase noise (dBc/Hz)	-67 @ 10 kHz
	-120 @ 3.5 MHz

[1] From the 600-mV supply (V_{DDH})

Table 4.2: Comparison with low-power/low-voltage PLLs

	This Work	[11]	[27]	[40]
Technology	65-nm	40-nm	90-nm	90-nm
Supply (V)	0.3/0.6	1	1.2	0.5/0.65
Chip area (mm^2)	0.59	0.2	0.75	0.14
Architecture	ADPLL	ADPLL	CP-PLL	CP-PLL
	TDC	TDC	Analog	Analog
Output frequency (GHz)	2	2.5	2.5	2.5
Power dissipation (mW)	0.78	0.86	1.1	6
Phase noise @ 10 kHz (dBc/Hz)	-67	-87	-80	-68
Phase noise @ 1 MHz (dBc/Hz)	-100	-120	-111	-113

From the 600-mV supply (V_{DDH})

Chapter 5

AN ULTRA-LOW-VOLTAGE ISM BAND PLL

The all-digital frequency synthesizer presented in Chapter 4 demonstrates the feasibility of accomplishing multi-GHz frequency synthesis at supply voltages significantly lower than typical values. However, a severe limitation of the proposed digital architecture is the minimum achievable in-band phase noise due to phase error quantization. This limitation is imposed by the fact that the quantization step used in the proposed method of phase/frequency estimation is defined precisely by the period of the DCO, or, more specifically, it is equal to a single half period. While this value represents an approximate lower bound on the gate delay achievable in the 65-nm process, the resulting noise may be unacceptable for certain applications. Further, this inflexibility with regard to noise limits the extent to which the design may be optimized for a given performance target. Although the dynamic range limitations associated with low supply voltages in analog designs are overcome by the use of a digital architecture, the rather coarse (raw) time resolution provided by an inverter biased with the same supply limits performance in a different manner. Time-to-digital converter architectures with sub-gate delay time resolution, such the Vernier architecture, typically necessitate high power dissipation in order to achieve significant performance (resolution) gains, and are therefore incompatible with energy-harvesting systems. In addition to these drawbacks, the use of a 300-mV supply compels weak inversion operation for all transistors, increasing susceptibility to threshold voltage variations and degrading yield.

The described limitations force a reconsideration of both the synthesizer architecture and target supply voltage. In this chapter we examine a digitally-assisted analog architecture as a means of overcoming the discussed deficiencies associated with the all digital design of the previous chapter. In this design, frequency acquisition is performed by an auxiliary digital loop which enables coarse tuning of the VCO over a wide frequency range. Phase lock is accomplished using an analog loop employing a charge pump and PFD for phase detection. A 400-mV supply is used, allowing adequate (fine) tuning of the VCO (with reasonable gain) as well as a reduction in the power dissipated by both the ILFD and the VCO. We proceed with a discussion of the synthesizer architecture and block-level implementation, followed by simulation results and concluding remarks.

5.1 Circuit Implentation

5.1.1 Synthesizer Architecture

A block diagram of the PLL is shown in Figure 5.1. As described in the chapter introduction, the core of the synthesizer is an architecturally typical charge-pump PLL with an LC-VCO. As with the ADPLL in Chapter 4, the 2.4-2.5 GHz VCO is injection-locked to a ring oscillator for integer division by N_1. Here again, injection locking increases the maximum frequency at which division is possible without resorting to power-hungry current mode designs, the employment of which is still tenuous at 400 mV due to limited voltage headroom. Following the ILFD is a multi-modulus divider (MMD) with instantaneous division value modulated by a third-order DSM. In tracking mode the analog path is engaged, and the phase/frequency of the MMD output (DIV) is compared to that of the reference (REF) by the PFD. The PFD provides digital control needed for the UP and DN currents of the charge pump. Finally, the charge pump current is fed to the loop filter to generate V_{tune}. However, due to the low supply, V_{tune} is constrained to remain within a 100-mV range centered on 200 mV to ensure that both the NMOS and PMOS current sources remain in saturation. This is accomplished by first performing frequency acquisition digitally

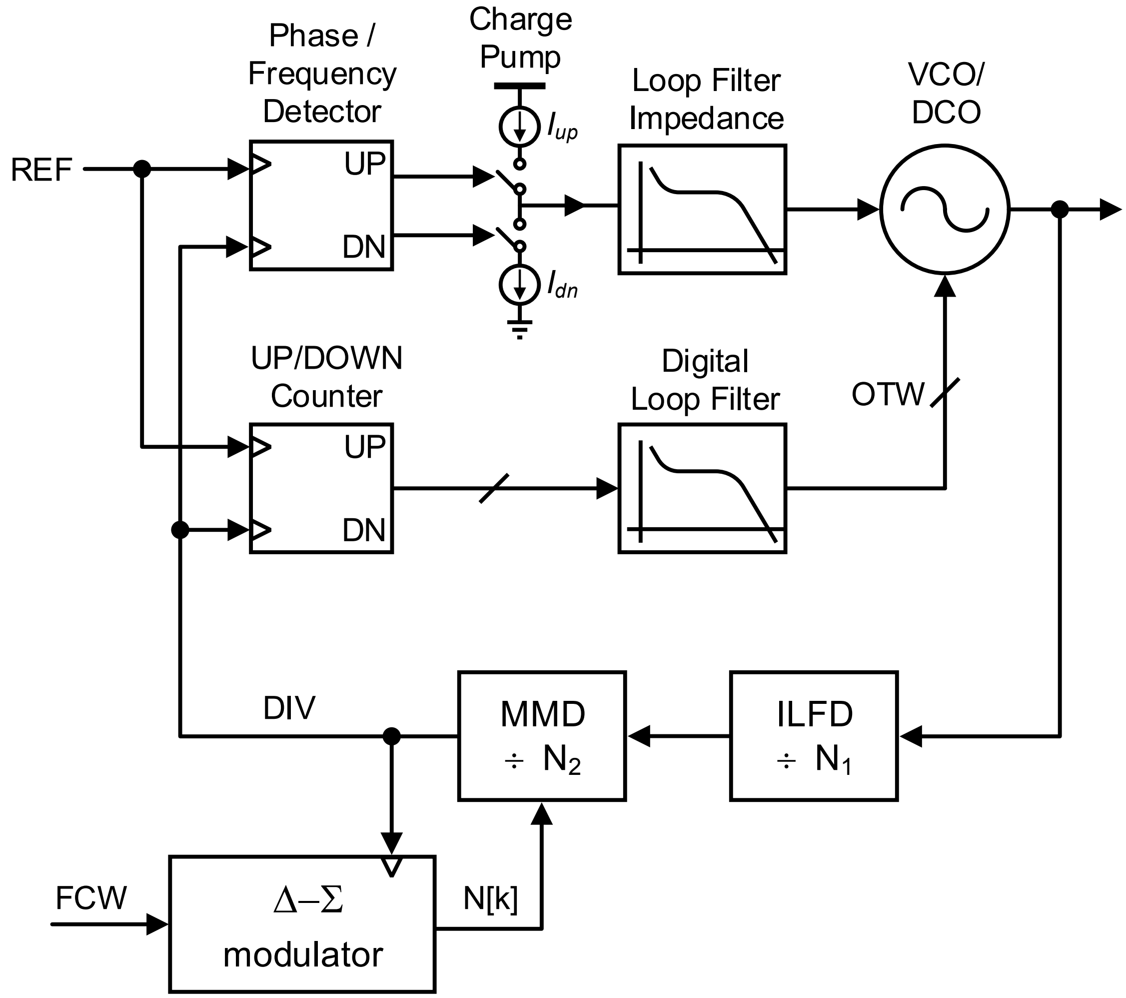

Figure 5.1: Block diagram of the low-voltage ISM-band frequency synthesizer.

while V_{tune} is held constant at 200 mV. Once the oscillator tuning word (OTW) has settled to within one LSB of the target frequency, the OTW is fixed and the analog loop is engaged.

Following is a description of the the design specifications for each of the major synthesizer components.

5.1.2 LC Voltage-Controlled Oscillator (LC-VCO)

Compared to the TF-DCO presented in Chapter 4, whose 300-mV supply necessitated the use of transformer feedback in order to achieve sufficient loop gain for sustained oscillation, a slightly higher supply voltage allows the use of a tail current source to control the DC current in the oscillator. In order to avoid the voltage headroom needed for a MOS current source (approximately 150 mV, nearly 40% of the supply voltage), as well as the power dissipated by additional bias circuitry, the current in the VCO can be regulated by selectively shorting the segments of a polysilicon resistor using digitally-controlled MOS switches, as shown in Figure 5.3. A resistor-based current source has the additional benefit of reduced flicker noise compared to the transistor-based current source [22]. The addition of a tail current source also affords more precise control over the power dissipation of the VCO compared to the TF-DCO. Minimizing power dissipated in the VCO implies operating in the current-limited, rather than the voltage-limited, regime. The minimum power dissipation of the LC-VCO depends on R_P, the g_m/I_D ratio of the transistors, and the supply voltage:

$$P_{min} = I_{bias} V_{dd} = \frac{4/R_P}{g_m/I_D} V_{dd} \tag{5.1}$$

For this design, a 3.8-nH inductor with a Q factor of approximately 20 was used. At 2.4 GHz, this yields an R_P given by

$$\begin{aligned} R_P &= \omega_0 L Q \\ &= 2\pi \cdot 2.4\,\mathrm{GHz} \cdot 3.8\,\mathrm{nH} \cdot 20 \\ &\approx 1.15\,\mathrm{k\Omega} \end{aligned} \tag{5.2}$$

If the transistors comprising the restoring (negative-g_m) circuit of the LC-VCO exhibit a transconductance efficiency of 15, a bias current of approximately 235 µA is required to sustain oscillation. However, the effective transconductance (designated by G_m) exhibited by the transistors in the large signal regime is in general lower than the small-signal value, from which the transconductance efficiency is derived. In [26], the ratio of small-signal to large-signal transconductance is estimated using describing functions to be

$$\frac{G_m}{g_m} = \frac{V_{dsat}}{V_1} \tag{5.3}$$

where V_1 is the amplitude of oscillation. If the oscillator is operated on the boundary between the current-limited and voltage-limited regimes, then $V_1 = V_{dd} = 400\,\mathrm{mV}$. Assuming a V_{dsat} of 150 mV, this yields

$$I_{bias} = \frac{4/R_P}{G_m/g_m \cdot g_m/I_D} \approx 618\,\mu\mathrm{A} \tag{5.4}$$

The minimum power dissipation, then, is calculated to be approximately 250 µW in this mode of operation. If, however, the oscillator is operated further into the current-mode regime, causing the voltage amplitude, given by $2I_{bias}R_P/\pi$, to be lower than V_{dd}, this value can be reduced further. Additionally, a g_m/I_D ratio as high as 20-25 is achievable if the transistors are operated in weak inversion. Assuming current-limited operation (i.e., $g_m \approx 2G_m$), this yields an approximate lower bound on I_{bias} of 280 µA, or a power dissipation of 112 µA. One constraint on the VCO's amplitude is its effect on the locking range of the injection-locked frequency divider, discussed in the next subsection.

The frequency of the VCO is tuned using a combination digital and analog means. An array digitally-controlled accumulation-mode MOS varactors is included for coarse frequency control. A single continuously-tuned varactor is used for fine frequency control and phase tracking. The 400-mV voltage supply puts a severe limit on the

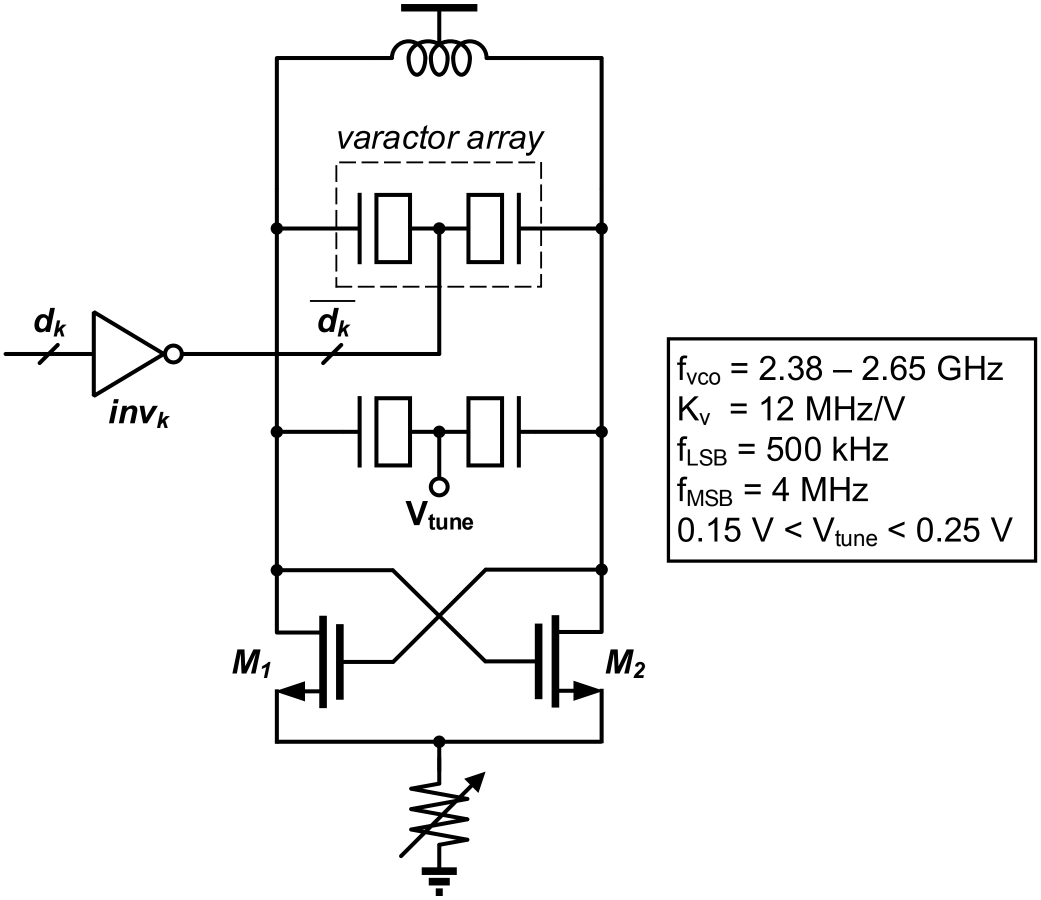

Figure 5.2: Voltage-controlled LC-oscillator with coarse digital tuning and adjustable tail current bias.

voltage range over which the oscillator can be tuned by analog means, so the ratio of LSB capacitance in the digital array to that of the fine tuning varactor is chosen to be greater than 2. A discussed, the fine-tuning capacitance is fixed at mid-supply during coarse frequency acquisition, and is connected to the loop filter voltage once the analog loop is engaged. A schematic of the VCO is given in Figure 5.2, along with the design details. The switched-resistor current source is shown schematically in Figure 5.3.

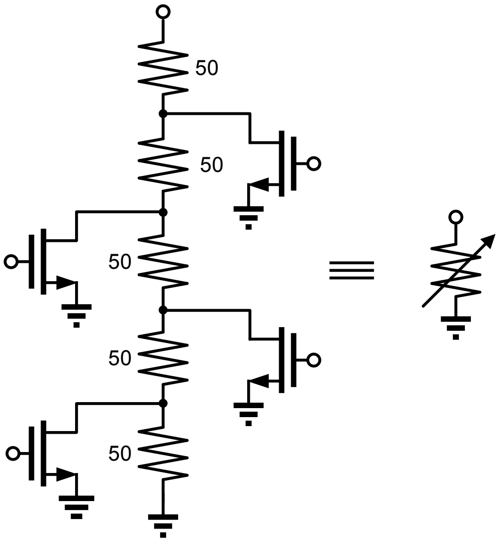

Figure 5.3: Digitally-controlled resistor-based current source.

5.1.3 Injection-locked Frequency Divider (ILFD)

As discussed in Chapter 4, frequency division at low voltage (i.e., near or below the transistor threshold voltage) can be performed at higher frequencies by injection locking than by conventional digital methods. Additionally, the power savings afforded by injection-locking makes it an obvious choice when extremely low-power operation is targeted. As discussed previously, the total power dissipated in the ILFD is approximately equal to that of a single inverter toggling at the VCO frequency, regardless of the number of stages. This implies that the number of stages can be increased arbitrarily in order to reduce the frequency of the ILFD output and thus the power dissipated by the subsequent digital circuitry. Another consideration is the minimum period that can be processed by a digital dual-modulus operated from a 400-mV supply. However, increasing the number of stages in the ring oscillator complicates the floor plan of the design and increases the routing complexity. A greater number of stages also requires a larger silicon area, so this number should be prudently selected. Further, when performing fractional division using $\Delta\Sigma$ modulation, phase noise due

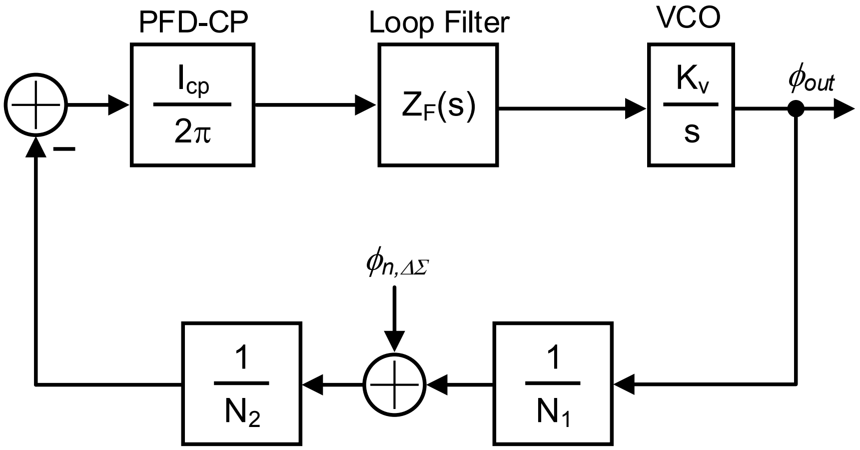

Figure 5.4: PLL noise model demonstrating the effect of prescaling on $\Delta\Sigma$ quantization noise.

to quantization is amplified by the modulus of the prescaler (the ILFD, in this case). This can be seen with the aid of Figure 5.4. The transfer function to output phase noise for the phase noise produced by $\Delta\Sigma$ quantization is given by

$$\frac{\phi_{out}}{\phi_{n,\Delta\Sigma}} = \frac{K_v I_{cp} Z_F(s)/N_2}{2\pi s + K_v I_{cp} Z_F(s)/N_1 N_2} \tag{5.5}$$

At low frequency offsets, (5.6) reduces to

$$\lim_{s\to 0} \frac{\phi_{out}}{\phi_{n,\Delta\Sigma}} = N_1 \tag{5.6}$$

Thus, compared with the expression given in Chapter 2, the phase noise due to $\Delta\Sigma$ modulation gets scaled up by a factor N_1 at low frequencies. This has the potential to significantly affect the phase noise at the output of the PLL, so it is desirable to make N_1 small enough to be able to neglect this particular source of phase noise. A 9-stage design is used here as a compromise between noise and power dissipation.

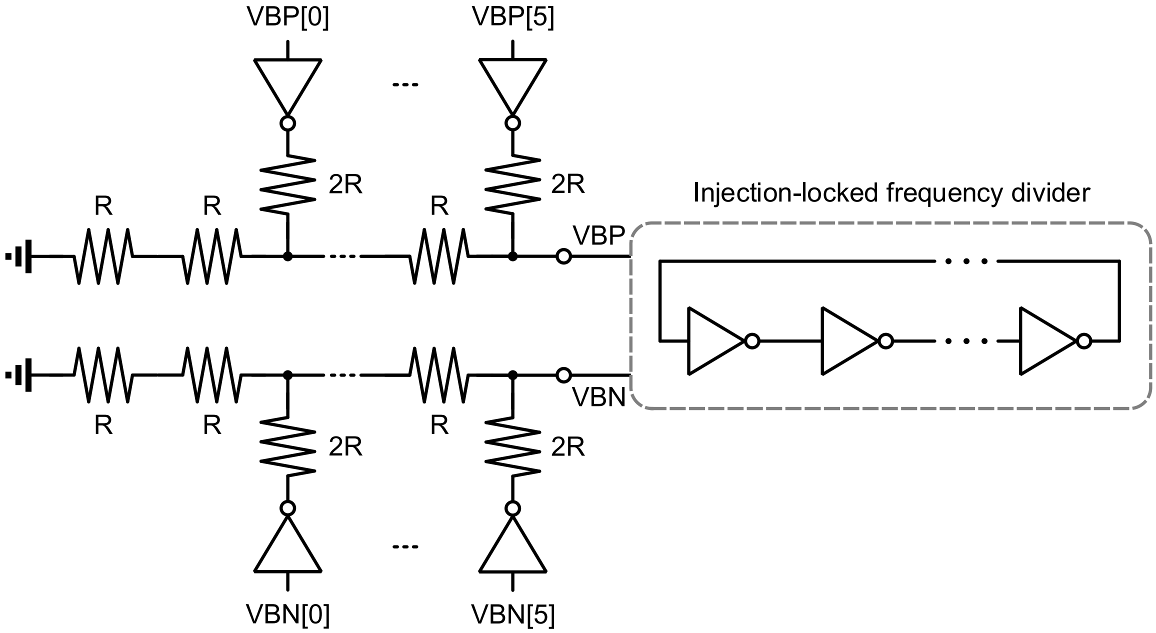

Figure 5.5: Digital control of ILFD free-running frequency.

In order to overcome the ILFD locking range limitation discussed in Chapter 4, an auxiliary loop can be added to provide coarse tuning of the free-running ILFD frequency prior to the PLL frequency/phase acquisition. Such coarse tuning eliminates the need for a divider than can be injection-locked over a wide range of frequencies, a limitation commonly attributed to injection-locked dividers. The auxiliary frequency tuning can be performed digitally, reusing the digital phase/frequency detector employed in the main loop (see Figure 5.1). Digital frequency control of the ILFD is readily accomplished by the R2R DAC structure shown schematically in Figure 5.5. The R2R DAC provides a programmable DC bias for the bulks of the ring transistors, allowing for digital control of the free-running frequency of the ring by adjusting the drive strength (via the large-signal bulk-source transconductance, g_{mb}) of the inverter devices.

5.1.4 Multi-modulus Divider (MMD)

The MMD in this design follows the same structure discussed in Chapter 3 for the MICS band PLL, except that it uses only two 2/3 stages as opposed to three. Only two of the four division values are used here, $N_2 = 4$ and $N_2 = 5$, making it a dual modulus divider. A single divide-by-2 stage is inserted after the ILFD output to further decrease the required frequency of operation of the MMD. Noise simulations, discussed later in this chapter, indicate that the amplified $\Delta\Sigma$ quantization noise remains negligible.

5.1.5 Third-order $\Delta\Sigma$ Modulator

Although the third-order MASH structure used in Chapter 3 for the MICS band PLL allows for full use of the input range and is simpler to design, the resulting instantaneous phase error "jumps" around more than in the case of the single bit modulator, exacerbating the nonlinearity issue discussed in Chapter 3. To avoid this issue, a third-order DSM based on the one presented in [38] is used here. A block diagram of the DSM is shown in Figure 5.6. Due to the cascading of multiple integrators in series, the input range is limited to 1/4 of its full-scale value. Using a 30-MHz reference, the 9-stage ILFD prescaler followed by a divide-by-2 stage and the 4/5 dual modulus divider, the minimum and maximum achievable output frequencies are given by

$$\begin{aligned} f_{min,max} &= 30\,\mathrm{MHz} \cdot (4.5 \pm 0.125) \cdot 18 \\ &= 2.43\,\mathrm{GHz} \pm 67.5\,\mathrm{MHz} \end{aligned} \tag{5.7}$$

The synthesizer can thus provide an output in the frequency range from 2.3625 GHz to 2.4975 GHz, with fractional frequency resolution set by the word size of the DSM.

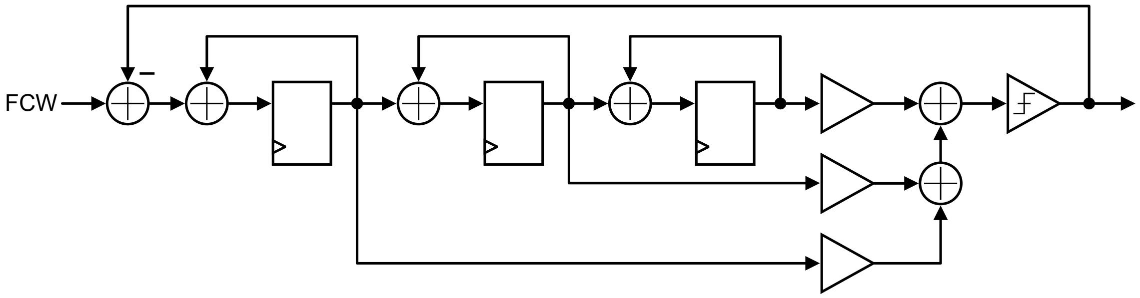

Figure 5.6: Third order ΔΣ modulator used for fractional division.

5.1.6 Low-Voltage Charge Pump

Conventional charge pump designs like the one described in Chapter 3 become exceedingly impractical as the supply voltage is reduced to well below 500 mV. Once again, digital design techniques become increasingly necessary to reach performance targets. Not only are traditional op-amp architectures difficult, or impossible, to implement, but even the employment of a simple current mirror is questionable with a supply voltage equal to approximately a single MOS transistor V_t. However, this fact ensures saturation operation of any transistor with its gate voltage connected to V_{DD}, as long as V_{ds} is kept above some minimum value, say $V_{DD}/2$. A switchable current source, such as is required in a charge-pump PLL, is thus realized by alternately driving the gate of a MOS transistor with the high and low supply voltages, namely V_{DD} and ground. This method avoids the difficulties of employing switches or current mirrors at 400 mV.

A simplified schematic of the proposed charge pump is shown in Figure 5.7. Individual PMOS and NMOS unit current sources are controlled by the digital control words CSP and CSN, respectively. Because the loop dynamics and output noise of the PLL depend heavily on the precise value of charge pump current, I_{cp}, as well as the matching between I_{up} and I_{dn} the number of unit current sources needing to be activated must be calibrated.

A drawback of the proposed charge pump architecture is the susceptibility of the output current to variations in the value of V_{DD} . Assuming sufficient dropout (i.e., a global supply of 500 mV or greater), a linear voltage regulator might be used to maintain a constant supply voltage.

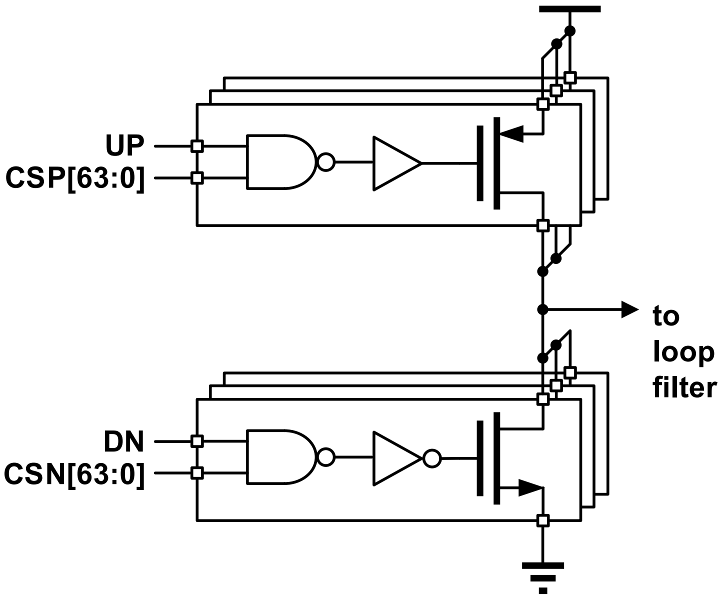

Figure 5.7: Low-voltage charge pump schematic.

5.2 Simulation Results

5.2.1 Noise

The simulated phase noise of the 400-mV PLL is shown in Figure 5.8. The plot was obtained by performing periodic steady-state (PSS) analyses on the individual blocks and using a linear model of the PLL to estimate the total output noise. In addition, a linear model of the delta-sigma quantization noise was employed. As expected, the flicker and thermal noise of the charge pump current sources dominates the noise performance at frequencies much lower than the bandwidth of the PLL, and the VCO phase noise dominates at large offsets. The modulator and loop are

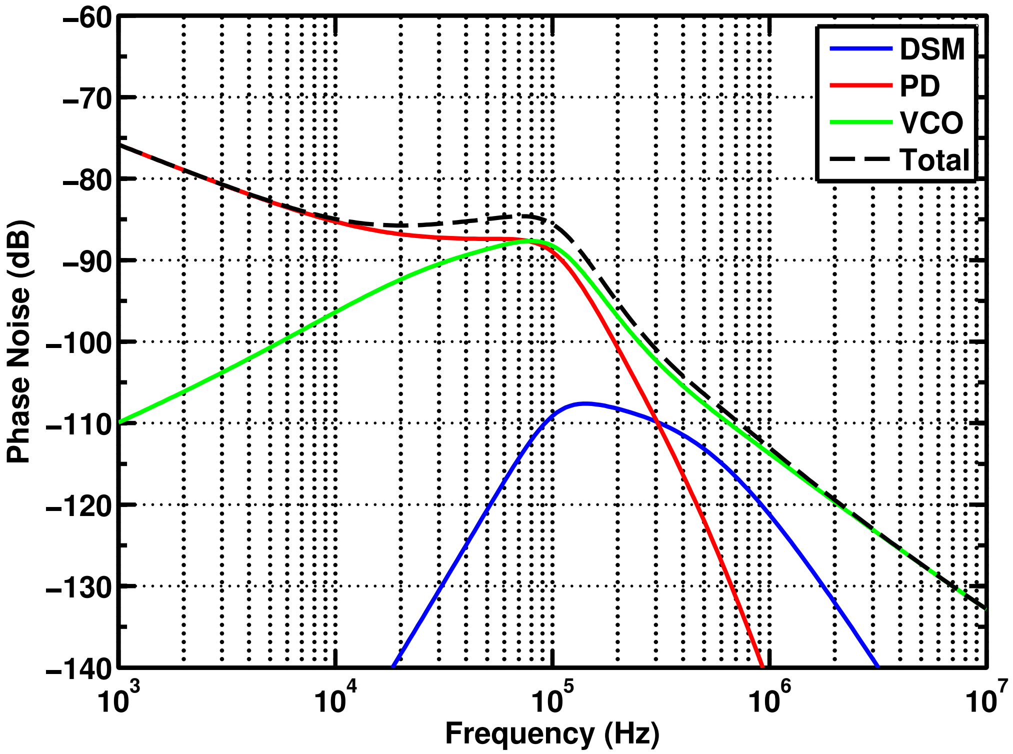

Figure 5.8: Simulated output phase noise (extracted simulation).

designed to minimize the impact of delta-sigma quantization noise on the total phase noise.

5.2.2 Phase Acquisition

Figure 5.9 shows the phase acquisition of the PLL in analog/tracking mode. Settling time is $< 100\,\mu$s, sufficient for Bluetooth and Zigbee applications.

Table 5.1 gives a summary of the simulated synthesizer performance. Key metrics are area, power, and phase noise. Both in-band (10 kHz frequency offset) and out-of-band (1 MHz frequency offset) phase noise results are provided. Simulated results are compared with the performance of several other state-of-the-art low power designs in Table 5.2.

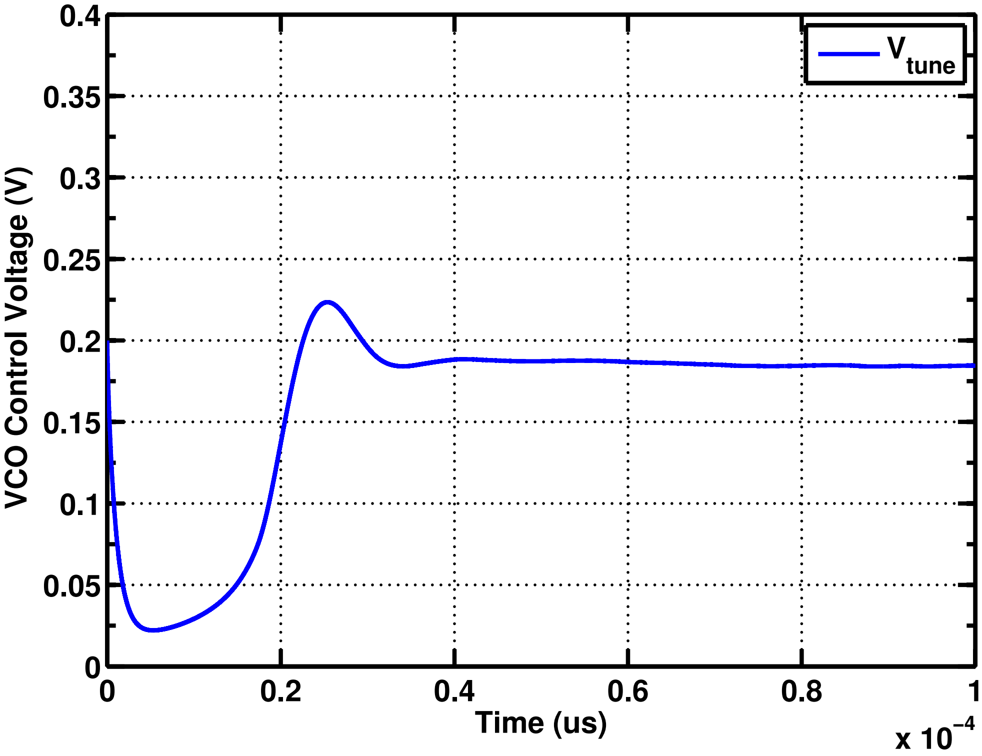

Figure 5.9: VCO control voltage during analog phase acquisition (simulated).

Table 5.1: Low-voltage ISM-band PLL performance summary (simulated results).

Technology	65-nm CMOS
Chip area (mm^2)	0.4
Reference frequency (MHz)	30
Output frequency (GHz)	2.4–2.5
Power dissipation (µW)	212
VCO	135
PFD/CP	22
ILFD + MMD	35
DSM	20
Phase noise (dBc/Hz)	-117 @ 1 MHz
	-85 @ 10 kHz

Table 5.2: Comparison with low-power/low-voltage PLLs

	This Work	[41]	[11]	[27]	[40]
Technology	65-nm	65-nm	40-nm	90-nm	90-nm
Supply (V)	0.4	0.3/0.6	1	1.2	0.5/0.65
Chip area (mm^2)	0.4	0.59	0.2	0.75	0.14
Architecture	CP-PLL	ADPLL	ADPLL	CP-PLL	CP-PLL
	Analog	TDC	TDC	Analog	Analog
Output frequency (GHz)	2.5	2	2.5	2.5	2.5
Power dissipation (mW)	0.21	0.78	0.86	1.1	6
Phase noise @ 10 kHz (dBc/Hz)	-85	-67	-87	-80	-68
Phase noise @ 1 MHz (dBc/Hz)	-117	-100	-120	-111	-113

Chapter 6

CONCLUSION

The primary challenges associated with low-voltage frequency synthesis are the accommodation of high-frequency (multi-GHz) signals with poor transistor drive strength, oscillator start-up, and low-noise phase detection. In both of the low-voltage designs presented in this thesis, frequency division is accomplished via injection-locking a ring oscillator to the VCO/DCO, utilizing the “back gate” of both the NMOS and PMOS devices of the delay elements for current injection at the RF frequency. It was shown in Chapter 4 that frequency division based on injection locking allows for lower power consumption and higher frequency operation than possible using digital techniques. Further, the proposed method of injection locking ensures that locking can be achieved while maintaining the maximum possible oscillation frequency of the free-running ring oscillator. This characteristic is important for low-voltage designs where an inverter delay is an order of magnitude (or more) greater than at nominal supply levels. For the all-digital design of Chapter 4, the multiple phases of the injection-locked ring-oscillator also serve as a means of quantizing the phase and frequency of the DCO, maintaining a measurement resolution of half the DCO period (the same as that afforded by an accumulator operated at the RF frequency). Finally, the bulk-biased design of the injection-locked frequency divider makes digital control of the free-running frequency (through the use of an R2R DAC) straightforward, enabling locking range requirements of the divider to be significantly relaxed.

This thesis serves as a demonstration of the feasibility of performing multi-GHz frequency synthesis at voltage levels typical of certain energy harvesting elements, namely, photovoltaic cells and thermoelectric generators. From the measurement results presented in Chapter 4 and the simulation results in Chapter 5, it is clear that this can be done without compromising performance needs, and that an sub-500 mV ISM band radio is achievable without the use of costly voltage boosting circuitry. The resulting increase in energy efficiency has the potential to enable complete energy autonomy for wireless sensor nodes.

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Appendix A

MICS BAND PLL VERILOG SOURCE CODE

```
//——————————————————————————————————————————
// Design Name : mash111
// File Name   : mash111.v
// Function    : 3-stage MASH delta sigma modulator with 17 bit input
//——————————————————————————————————————————

module mash111 (
frac_in,        // 17-bit digital input word
clk_in,         // Input clock
reset,          // Reset input
mod_out         // Sum of three quantizer outputs
);

//——————————Input Ports——————————
input  [16:0] frac_in;
input clk_in;
input reset;



//——————————Output Ports——————————
output reg        [2:0]  mod_out;

//—————————Internal Variables————————
reg               [16:0]  int1_dly;
reg               [16:0]  int2_dly;
reg               [16:0]  int3_dly;
reg               [16:0]  err1;
```

```
reg            [16:0]  err2;
reg            [16:0]  int1;
reg            [16:0]  int2;
reg            [16:0]  int3;
reg            [16:0]  mod1;
reg            [4:0]   q1;
reg            [4:0]   q1_dly1;
reg            [4:0]   q1_dly;
reg            [16:0]  mod2;
reg            [4:0]   q2;
reg            [4:0]   q2_dly;
reg            [16:0]  mod3;
reg            [4:0]   q3;
reg            [4:0]   q3_dly;
reg            [16:0]  u1;
reg            [16:0]  u2;
reg            [16:0]  u3;
reg            [16:0]  error1;
reg            [16:0]  error2;
reg            [4:0]   err_cancel1;
reg            [4:0]   err_cancel2;
reg            [4:0]   sum2;
reg            [4:0]   sum2_dly;
reg            [4:0]   mod_out_temp;



// Compute error signals, frac_in +1  and frac_in - 1
always @(*) begin

     err1 = frac_in + 17'b00100000000000000;
     err2 = frac_in + 17'b11100000000000000;
```

```
end


//——————————————First integrator——————————————
always @(posedge clk_in or posedge reset) begin

      if (reset)
        int1_dly <= 17'b00000000000000001;  // LSB is set to one to
            approximate an irrational number, int1_dly/FS
      else
        int1_dly <= int1;                    // update first integrator
            output

end

always @(*) begin

     int1 = u1 + int1_dly;                   // accumulate

end

//——————————————First quantizer——————————————
always @(*) begin

   if (int1_dly[16]) begin                   // MSB indicates sign
      u1   = err1;
      mod1 = 17'b11100000000000000;          // -1 quantizer output
      q1   = 5'b11111;                       // -1 quantizer output for
          error cacellation network
    end
   else begin
      u1   = err2;
```

```
      mod1 = 17'b00100000000000000;          // +1 quantizer output
      q1   = 5'b00001;                       // +1 quantizer output for
          error cancellation network
    end

end

always @(*) begin

     error1 = int1_dly - mod1;               // quantization error of first
         stage, fed to second stage

end

always @(posedge clk_in or posedge reset) begin

   if (reset)
     q1_dly1 <= 5'b00000;
   else
     q1_dly1 <= q1;                          // first quantizer output,
         delayed by one period

end

always @(posedge clk_in or posedge reset) begin

   if (reset)
     q1_dly <= 5'b00000;
   else
     q1_dly <= q1_dly1;                      // first quantizer output,
         delayed by two periods

end
```

```
//−−−−−−−−−−−−−−−−−−−−−−−−−−−−Second integrator−−−−−−−−−−−−−−−−−−−−−−−
always @(posedge clk_in or posedge reset) begin

      if (reset)
        int2_dly <= 17'b00000000000000000;
      else
        int2_dly <= int2;                    // update second integrator
            output

end

always @(*) begin

     u2 = error1 − mod2;                     // input to second integrator
     int2 = u2 + int2_dly;                   // accumulate

end

//−−−−−−−−−−−−−−−−−−−−−−−−−−−−Second quantizer−−−−−−−−−−−−−−−−−−−−−−−
always @(*) begin

   if (int2_dly[16]) begin                     // MSB indicates sign
      mod2 = 17'b11100000000000000;            // −1 quantizer output
      q2   = 5'b11111;                         // −1 quantizer output for
          error cacellation network
    end
   else begin
      mod2 = 17'b00100000000000000;            // +1 quantizer output
      q2   = 5'b00001;                         // +1 quantizer output for
          error cacellation network
```

```
    end

end

always @(posedge clk_in or posedge reset) begin

   if (reset)
     q2_dly <= 5'b00000;
   else
     q2_dly <= q2;                              // second quantizer output, delayed by one period

end

always @(*) begin

     error2 = int2_dly - mod2;                  // quantization error of second stage, fed to third stage

end

//----------------------Third integrator------------------
always @(posedge clk_in or posedge reset) begin

        if (reset)
          int3_dly <= 17'b00000000000000000;
        else
          int3_dly <= int3;                     // update output of third integrator

end

always @(*) begin
```

```
    u3 = error2 - mod3;                         // input to third integrator
    int3 = u3 + int3_dly;                       // accumulate

end

//----------------------Third quantizer-----------------
always @(*) begin

  if (int3_dly[16]) begin                       // MSB indicates sign
     mod3 = 17'b11100000000000000;              // -1 quantizer output
     q3   = 5'b11111;                           // -1 quantizer output for
         error cacellation network
   end
  else begin
     mod3 = 17'b00100000000000000;              // +1 quantizer output
     q3   = 5'b00001;                           // +1 quantizer output for
         error cacellation network
   end

end



//--------------------Error cancellation------------------
always @(posedge clk_in or posedge reset) begin

  if (reset)
    q3_dly <= 5'b00000;
  else
    q3_dly <= q3;                               // third quantizer output,
        delayed by one period
```

```
end

always @(*) begin                                  // third quantizer output is
    differentiated and
                                                   // added to second quantizer
                                                       output
    err_cancel2 = q3 - q3_dly;
   sum2 = q2_dly + err_cancel2;

end

always @(posedge clk_in or posedge reset) begin

  if (reset)
    sum2_dly <= 5'b00000;
  else
    sum2_dly <= sum2;

end

always @(*) begin

    err_cancel1 = sum2 - sum2_dly;             // difference between
        quantizers 2 and 3 is differentiated

end

always @(*) begin

mod_out_temp = q1_dly + err_cancel1;          // quantization error is
   removed from first quantizer output

end
```

```
always @(*) begin                                    // converts signed
    modulator output into 3-bit, unsigned number,
                                                     // so the average value
                                                        is shifted by +7 and
                                                        scaled by 1/2
    case (mod_out_temp)
        5'b00111: mod_out = mod_out_temp[2:0];       // +7 --> 7
        5'b00101: mod_out = 3'b110;                  // +5 --> 6
        5'b00011: mod_out = 3'b101;                  // +3 --> 5
        5'b00001: mod_out = 3'b100;                  // +1 --> 4
        5'b11111: mod_out = 3'b011;                  // -1 --> 3
        5'b11101: mod_out = 3'b010;                  // -3 --> 2
        5'b11011: mod_out = 3'b001;                  // -5 --> 1
        5'b11001: mod_out = 3'b000;                  // -7 --> 0

    endcase

end




endmodule
```

Appendix B

LVADPLL VERILOG SOURCE CODE

```
//------------------------------------------------------------
// Design Name : phase_detector
// File Name   : phase_detector.v
// Function    : Performs reference and variable phase
//               accumulation and compares the resultant
//               sums
//------------------------------------------------------------

module phase_detector (
ckr,
rst,
cycle_count,
fcw,
ro_state,
phase_error,
error_check1,
error_check0

);

//--------Input Ports--------
input ckr;                        // re-timed reference clock
input rst;                        // rst (duh)
input [9:0] fcw;                  // 'frequency control word' = E(fout
    )/fref
input [16:0] ro_state;            // instantaneous state of all 17
    divider phases
```

```
input [5:0] cycle_count;            // snapshot of coarse counter
input error_check0, error_check1;


//————Output Ports————
output reg [9:0] phase_error;       // phase error is ref. phase minus
    var. phase


//————Internal Variables————
reg [6:0] delay_index;
reg check_bit;
reg [6:0] osc_state;                // [k]th index of ring oscillator
    state
reg [6:0] osc_state1;               // [k−1]th index of ring oscillator
    state
reg [5:0] count_state;              // [k]th counter state
reg [5:0] count_state1;             // [k−1]th counter state
reg [9:0] fine_phase;               // FINE phase measurement
reg [5:0] coarse_phase;             // COARSE phase measurement
reg [2:0] wait_signal;
reg check_low;
reg check_high;


// Two separate measurements are made to determine the variable phase: '
    COARSE' and 'FINE'.
//
// COARSE measurement is performed by calculating the number of full
    cycles completed by the ring oscillator
// between consecutive rising edges of the re−timed reference clock (ckr
    ).
// This is done by observing the output of an external counter at each
```

```
    rising clock edge, and computing the difference between
// the values computed for consecutive cycles.  The external counter
    output changes 1/2 period before the rising edge of ckr.
//
// FINE measurement is performed by observing the state of the internal
    nodes of the ring oscillator
// at each rising edge of the (non-retimed) reference clock, and
    calculating the number of elapsed states
// (in excess of complete oscillator cycles).
// The difference between consecutive indices is calculated and the sign
     computed difference determines whether the FINE
// measurement result is added to or subtracted from that of the COARSE
    measurement.


always @(ro_state) begin                                          //
    Decode current index from oscillator state
  case (ro_state)
      default:                   delay_index = 7'd0;
      17'b10101010101010101: delay_index = 7'd0;
      17'b00101010101010101: delay_index = 7'd1;
      17'b01101010101010101: delay_index = 7'd2;
      17'b01001010101010101: delay_index = 7'd3;
      17'b01011010101010101: delay_index = 7'd4;
      17'b01010010101010101: delay_index = 7'd5;
      17'b01010110101010101: delay_index = 7'd6;
      17'b01010100101010101: delay_index = 7'd7;
      17'b01010101101010101: delay_index = 7'd8;
      17'b01010101001010101: delay_index = 7'd9;
      17'b01010101011010101: delay_index = 7'd10;
      17'b01010101010010101: delay_index = 7'd11;
      17'b01010101010110101: delay_index = 7'd12;
      17'b01010101010100101: delay_index = 7'd13;
```

```
      17'b01010101010101101: delay_index = 7'd14;
      17'b01010101010101001: delay_index = 7'd15;
      17'b01010101010101011: delay_index = 7'd16;
      17'b01010101010101010: delay_index = 7'd17;
      17'b11010101010101010: delay_index = 7'd18;
      17'b10010101010101010: delay_index = 7'd19;
      17'b10110101010101010: delay_index = 7'd20;
      17'b10100101010101010: delay_index = 7'd21;
      17'b10101101010101010: delay_index = 7'd22;
      17'b10101001010101010: delay_index = 7'd23;
      17'b10101011010101010: delay_index = 7'd24;
      17'b10101010010101010: delay_index = 7'd25;
      17'b10101010110101010: delay_index = 7'd26;
      17'b10101010100101010: delay_index = 7'd27;
      17'b10101010101101010: delay_index = 7'd28;
      17'b10101010101001010: delay_index = 7'd29;
      17'b10101010101011010: delay_index = 7'd30;
      17'b10101010101010010: delay_index = 7'd31;
      17'b10101010101010110: delay_index = 7'd32;
      17'b10101010101010100: delay_index = 7'd33;
    endcase
  end


always @(posedge ckr or posedge rst) begin
  if (rst) begin
    check_bit <= 1'b0;
    osc_state <= 7'b0;
    osc_state1 <= 7'b0;
    count_state <= 6'b0;
    count_state1 <= 6'b0;
    fine_phase <= 10'b0;
    coarse_phase <= 6'b0;
```

```
    wait_signal <= 3'b0;
    phase_error <= 10'd0;
    check_high <= 1'b0;
    check_low <= 1'b0;
  end

  else begin
    if (wait_signal < 3'd3) begin
                                                                    // a 'wait'
        period consisting of three reference cycles
      phase_error <= 10'd0;
                                                                           // is
         used following a rst to allow the variables used for
      wait_signal <= wait_signal + 1;
                                                                  // phase
         measurement to acquire valid values
      check_bit <= ro_state[0];
      osc_state <= delay_index;
      osc_state1 <= osc_state;
      count_state <= cycle_count;
      count_state1 <= count_state;
      fine_phase <= osc_state - osc_state1;
      coarse_phase <= count_state - count_state1;
      check_high <= error_check1;
      check_low <= error_check0;
    end

    else begin
      check_bit <= ro_state[0];
      osc_state <= delay_index;
      osc_state1 <= osc_state;
      count_state <= cycle_count;
      fine_phase <= osc_state - osc_state1;
```

```
coarse_phase <= count_state - count_state1;
check_high <= error_check1;
check_low <= error_check0;

case (check_bit)
  1'b0: begin
    if (check_low) begin
                                                              // if
       the LSB of ro_state and check_low are LOW simultaneously,
      coarse_phase <= count_state - count_state1;
                                            // there is a conflict between
         the COARSE and FINE phase
      phase_error <= phase_error + fcw - 34 * coarse_phase -
         fine_phase;     // measurements, resulting in an '
         overcount'
      count_state1 <= count_state;
    end
    else begin
      coarse_phase <= count_state - count_state1 - 1;
      phase_error <= phase_error + fcw - 34 * coarse_phase -
         fine_phase;
      count_state1 <= count_state - 1;
    end
  end

  1'b1: begin
    if (check_high) begin
                                                              // if the
       LSB of ro_state and check_high are are HIGH simultaneously
       ,
      coarse_phase <= count_state - count_state1 + 1;
                                         // again there is a conflict
         between the COARSE and FINE phase
```

```
          phase_error <= phase_error + fcw - 34 * coarse_phase -
              fine_phase;     // measurements, resulting in an '
              undercount'
          count_state1 <= count_state + 1;
        end
        else begin
          coarse_phase <= count_state - count_state1;
          phase_error <= phase_error + fcw - 34 * coarse_phase -
              fine_phase;
          count_state1 <= count_state;
        end
      end
    endcase

  end
 end
end

endmodule

//-----------------------------------------------------------------
// Design Name : filter_PI
// File Name   : filter_PI.v
// Function    : Proportional plus integral filter
//-----------------------------------------------------------------

module filter_PI (input [9:0] x,          // <10,8,s>  input of the filter
    . signed. 1 fractional, 1 sign and 8 integer bits
                  input          ckr,     // from 5-50MHz
                  input          rst,     // reset the accumulator flip
                      flop
                  input    [3:0] pmult,   // proportional multiplier,
                      expresed in number of bit shift: power(2,-2) to power
                      (2, -15)
```

```
            input    [3:0] imult,    // integrate multiplier, express
                in number of bit shift: power(2, −10)to power(2, −20)
            output reg [13:0] y);      // <14,12,u> output of the
                filter. Unsigned 14 bits, 3 integer bits and 11
                fractional bits

reg   [14:0] pmultx;                 //<15,12,s>
reg   [30:0] imultx;                 //<31,28,s>
reg   [30:0] accum;                  //<31,28,s>
reg   [30:0] accum_dly;              //latched version of accum
reg   [31:0] temp_accum;
wire  [14:0] accumout;              //<15, 12, s>
reg   [15:0] temp_y;                 // <16, 12, s>

// There is an additional inherent multiplication here, by the factor
    fref/2/LSB, where
// LSB is the frequency resolution of the DCO, given by fref/2/2^6.

assign accumout[14:0] = accum[30:16];

always @(*) begin // multiplication using bit−shift, retains (and
    extends) sign bit
    case (pmult) // from <10,8,s> to <15,12,s>
        4'b0000:  pmultx = { x[9], x, 4'b0 };        // power(2,−2)
        4'b0001:  pmultx = { {2{x[9]}}, x, 3'b0 };   // power(2,−3)
        4'b0010:  pmultx = { {3{x[9]}}, x, 2'b0 };   // power(2,−4)
        4'b0011:  pmultx = { {4{x[9]}}, x, 1'b0 };   // power(2,−5)
        4'b0100:  pmultx = { {5{x[9]}}, x };         // power(2,−6)
        4'b0101:  pmultx = { {6{x[9]}}, x[9:1] };    // power(2,−7)
        4'b0110:  pmultx = { {7{x[9]}}, x[9:2] };    // power(2,−8)
        4'b0111:  pmultx = { {8{x[9]}}, x[9:3] };    // power(2,−9)
        4'b1000:  pmultx = { {9{x[9]}}, x[9:4] };    // power(2,−10)
        4'b1001:  pmultx = { {10{x[9]}}, x[9:5] };   // power(2,−11)
```

```
            4'b1010:  pmultx = { {11{x[9]}}, x[9:6] };  // power(2,-12)
            4'b1011:  pmultx = { {12{x[9]}}, x[9:7] };  // power(2,-13)
            4'b1100:  pmultx = { {13{x[9]}}, x[9:8] };  // power(2,-14)
            4'b1101:  pmultx = { {14{x[9]}}, x[9] };    // power(2,-15)
            4'b1110:  pmultx = { {15{x[9]}} };          // power(2,-15)
            4'b1111:  pmultx = { {15{x[9]}} };          // power(2,-15)
        endcase
end

always @(*) begin // multiplication using bit-shift, retains (and
    extends) sign bit
     case (imult) // from <10,8,s> to <31,28,s>
            4'b0000:  imultx = { {9{x[9]}}, x[9:0], 12'b0 };  // power
                (2,-10)
            4'b0001:  imultx = { {10{x[9]}}, x[9:0], 11'b0 }; // power
                (2,-11)
            4'b0010:  imultx = { {11{x[9]}}, x[9:0], 10'b0 }; // power
                (2,-12)
            4'b0011:  imultx = { {12{x[9]}}, x[9:0], 9'b0 };  // power
                (2,-13)
            4'b0100:  imultx = { {13{x[9]}}, x[9:0], 8'b0 };  // power
                (2,-14)
            4'b0101:  imultx = { {14{x[9]}}, x[9:0], 7'b0 };  // power
                (2,-15)
            4'b0110:  imultx = { {15{x[9]}}, x[9:0], 6'b0 };  // power
                (2,-16)
            4'b0111:  imultx = { {16{x[9]}}, x[9:0], 5'b0 };  // power
                (2,-17)
            4'b1000:  imultx = { {17{x[9]}}, x[9:0], 4'b0 };  // power
                (2,-18)
            4'b1001:  imultx = { {18{x[9]}}, x[9:0], 3'b0 };  // power
                (2,-19)
            4'b1010:  imultx = { {19{x[9]}}, x[9:0], 2'b0 };  // power
```

```
            (2,−20)
        4'b1011:   imultx = { {20{x[9]}}, x[9:0], 1'b0 };   // power
            (2,−21)
        4'b1100:   imultx = { {21{x[9]}}, x[9:0] };          // power
            (2,−22)
        4'b1101:   imultx = { {21{x[9]}}, x[9:0] };          // power
            (2,−22)
        4'b1110:   imultx = { {21{x[9]}}, x[9:0] };          // power
            (2,−22)
        4'b1111:   imultx = { {21{x[9]}}, x[9:0] };          // power
            (2,−22)
     endcase
end

 // accumulator

always @(*) begin
    temp_accum = {accum_dly[30], accum_dly} + {imultx[30], imultx};   //
        extend sign and add

    case (temp_accum[31:30])    // overflow exception
        2'b01: accum = {temp_accum[31], {30{temp_accum[30]}} };
        2'b10: accum = {temp_accum[31], {30{temp_accum[30]}} };
        2'b11: accum = temp_accum[30:0];
        2'b00: accum = temp_accum[30:0];
    endcase
end

always @(posedge ckr or posedge rst)
    if (rst)
        accum_dly = 0;
    else
        accum_dly = accum;
```

```
always @(*) begin
    temp_y = {accumout[14], accumout[14:0]} + {pmultx[14], pmultx
        [14:0]}; // extend sign and add
    y = {~temp_y[14],temp_y[12:0]};     // signed to unsigned
    //case  (temp_y[15:14])
//          2'b11: y = 14'b00000000000000;
//          2'b10: y = 14'b00000000000000;
//          2'b01: y = 14'b11111111111111;
//          2'b00: y = temp_y[13:0];
//      endcase
end

endmodule
```

Appendix C

LVDLPLL VERILOG SOURCE CODE

```
//----------------------------------------------------------------
// Design Name : mod3_riley
// File Name   : mod3_riley.v
// Function    : 3rd order, 11-bit delta-sigma modulator
//               with 1-bit quantizer
//----------------------------------------------------------------

module mod3_riley (
frac_in ,          // 11-bit digital input word
clk_in ,           // Input clock
reset ,            // Reset input
mod_out            // Sum of three sequential integrator outputs
);

//-------------Input Ports-------------
input  [10:0] frac_in;
input  clk_in;
input  reset;



//-------------Output Ports-------------
output reg   mod_out;

//-----------Internal Variables---------
reg              [10:0] error;
reg              [12:0] integ_dly1;
reg              [13:0] integ_dly2;
```

```
reg          [16:0] integ_dly3;
wire         [10:0] err1;
wire         [10:0] err2;
wire         [12:0] integ1;
wire         [13:0] integ2;
wire         [16:0] integ3;
reg          [17:0] integ1_ext;
reg          [17:0] integ2_ext;
reg          [17:0] integ3_ext;
reg          [17:0] mod_sum;


// +1 corresponds to (division by) 5, -1 to 4
// as a 3rd order modulator, only 1/4 of the
// full scale range is usable, corresponding
// to the range 4.375 to 4.625
// Compute error signals, U+1 and U-1
assign err1 = frac_in + 11'b01000000000;
assign err2 = frac_in + 11'b11000000000;


// Choose appropriate error value, U+1 or U-1,
// determined by sign of accumulator output
always @(mod_sum[17]) begin

  if (mod_sum[17])
     error = err1;
  else
     error = err2;

end

// Compute weighted sum of all three accumulator outputs
```

```
always @(*) begin
       integ1_ext <= {{4{integ_dly1[12]}}, integ_dly1 , 1'b0};    // extend
            sign of first integrator output, multiply by 2
       integ2_ext <= {{4{integ_dly2[13]}}, integ_dly2};           // extend
            sign of second integrator output

       mod_sum <= integ1_ext + integ2_ext + { {3{integ_dly3[16]}},
           integ_dly3[16:2]};

end

// Reset or update first accumulator
always @(posedge clk_in or posedge reset) begin

      if (reset)
        integ_dly1 <= 13'b0000000000001;  // LSB is set to one to
            approximate an irrational number
      else
        integ_dly1 <= { {2{error[10]}}, error} + integ_dly1;

end

// Reset or update second accumulator
always @(posedge clk_in or posedge reset) begin

      if (reset)
        integ_dly2 <= 14'b00000000000000;
      else
        integ_dly2 <= {integ_dly1[12], integ_dly1} + integ_dly2;

end

// Reset or update third accumulator
```

```
always @(posedge clk_in or posedge reset) begin

     if (reset)
       integ_dly3 <= 17'b00000000000000000;
     else
       integ_dly3 <= { {3{integ_dly2[13]}}, integ_dly2} + integ_dly3;

end

always @(posedge clk_in or posedge reset) begin

    if (reset)
      mod_out <= 1'b0;
    else begin
      case (mod_sum[17])
        1'b1: mod_out <= 1'b0;              // +1 --> 4
        1'b0: mod_out <= 1'b1;              // -1 --> 5
      endcase
    end
end

endmodule
```