# Reference clock design for low power and low phase noise with temperature compensation

Jabeom Koo

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Reading Committee:

Brian P Otis, Chair

Gianluca Piazza

Visvesh Sathe

Program Authorized to Offer Degree:

Department of Electrical Engineering

University of Washington

**Abstract**

# Reference clock design for low power and low phase noise with temperature compensation

Jabeom Koo

Chair of the Supervisory Committee:
Associate Professor Brian P Otis
Department of Electrical Engineering

Low power and low phase noise RF frequency references are essential for applications such as high performance ADCs, high speed serial data links, and low power radios. They constitute a multi-billion dollar market in today's electronic industry. Quartz crystal is the most commonly used mineral for generating a reference clock. However, it needs a complicated manufacturing process, which increases cost, and it cannot be integrated with CMOS circuits. This is reason why wafer scale high-Q MEMS resonators are becoming attractive alternatives to quartz owing to their small size, low cost and integration potential.

However, oscillators using MEMS resonator perform poorly compared to quartz based oscillators in terms of close-in phase noise. Close-in phase noise is an important performance metric for a reference oscillator as it dominates the in-band phase noise of a frequency synthesizer in a radio. In addition, highly miniaturized MEMS resonator based oscillators have exhibited poor frequency stability over temperature. This characteristic is an issue, which limits the choice of the oscillator type in wireless application such as Bluetooth, Wi-Fi and GPS.

The first part of this thesis addresses the close-in phase noise issue and proposes circuits with MEMS resonator such as AlN contour mode resonator and FBAR (thin-Film Bulk-Acoustic Resonator) to demonstrate solutions for improving the phase noise and lowering the power consumption. The proposed oscillator with FBAR culminates in achieving more than 10dB lower phase noise than that of conventional oscillator with 350uW power consumption.

The following part of this thesis addresses the frequency drift of the reference clock when the temperature changes. The wireless application requires stringent and challenging spec. for the oscillator to generate a stable clock signal. For example, GPS needs to have less than 2ppm frequency drift over temperature. The first prototype of fully integrated oven-controlled temperature compensation system is thus introduced. This effort aims to have a ±1.6ppm stability reference clock with 150uK temperature resolution.

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# GLOSSARY

FBAR: thin-Film Bulk Acoustic Resonator

MBVD: Modfied-Butterworth-Van-Dyke model for FBAR resonators

QUARTZ CRYSTAL: State-of-art frequency reference used in radios

AlN CMR: Aluminum nitride Contour-mode resonators

PHASE NOISE: A measure of short term frequency stability of a reference clock

ALLAN DEVIATION: A measure of long term frequency stability of a reference clock

PPM: Part-per-million.

MEMS: Micro-Electro-Mechanical Systems

CMOS: Complementary Metal Oxide Semiconductor

TDC: Temperature-to-Digital Converter

DAC: Digital-to-Analog Converter

# ACKNOWLEDGEMENTS

Upon my arrival in Seattle 4 years ago, I felt very awkward as it was the first time I had landed in the US. The very first people I had met was my advisor, Brian Otis. He gave me a big smile and welcomed me. I cannot forget how enthusiastically he had explained the research topics he was working on. I would like to thank him for allowing me to join his group and supporting me during my entire Ph.D program. I have learned a lot from him directly and indirectly such as how to design circuit, being passionate about research, and who is the real advisor for students. Whenever there were moments of frustration because of failures in research or for private reasons, he has always supported and encouraged me. I would not have reached this stage without his sincere help and advice. I have always enjoyed my research due to the freedom it provided. He let me join other projects and allowed me to interact with other decent lab mates, from whom I have learned and eventually grew up as a researcher. I'm really grateful to meet such a great advisor. Any words cannot quite express my gratitude.

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## DEDICATION

To my parents

Kabmoon Koo

Miah Rhee

# Chapter 1.

# INTRODUCTION

## *1.1 Importance of the reference clock*

Reference oscillators are ubiquitous elements used in almost any electronics system and constitute a multi-billion dollar market in today's electronic industry. These oscillators are used for a wide range of applications for keeping track of real time, setting clock frequency for digital data transmission, frequency up and down conversion in RF transceivers and clocking of logic circuits. In general, the following properties are important for any oscillator technology [1-2]:

- Non-deterministic frequency stability: The frequency spectrum of an oscillator clock should ideally contain only a single frequency. In reality, the frequency clock of any oscillator shows short-term frequency fluctuation and hence a broadening of the frequency spectrum. This broadening is expressed in terms of phase-noise or jitter. These short-term fluctuations are caused by non-deterministic noise sources, such as flicker and white noise present in the oscillator loop. The noise can be filtered out in the oscillator loop by the frequency-selective element. An important figure of merit in this respect is the quality factor (Q-factor) of the frequency-selective element. High Q-factors translate into a narrow band filtering of the oscillator noise and are therefore beneficial in attaining low jitter or phase-noise [3].
- Deterministic frequency stability: The frequency of the oscillator should be stable under varying environmental conditions such as fluctuations in temperature. The deterministic frequency stability can be as low as a few parts-per-million (ppm) for MEMS-based oscillators and is typically more than a few hundred ppm up to a few thousand ppm for CMOS-based oscillators [4]. The low temperature drift in combination with the high Q-factor results in a stable oscillation frequency, since the high resonator Q results in the oscillation frequency being solely determined by the stability or the drift of the resonator.

- System integration and miniaturization: Almost any electronic system follows the trend of miniaturization and higher levels of functionalization. The components that build up these electronic systems should be made smaller and should allow for higher levels of system integration in order to accommodate this omnipresent trend. Therefore, the oscillator should be easy to integrate with other components such as MEMS-based resonator.

The phase noise, one of the properties mentioned above, directly impacts the performance of any electronic system. Also various radio standards (e.g. Wi-Fi, GPS, Bluetooth and WLAN) require oscillator circuits to have stringent frequency stability over a 100$^{o}$C temperature range. The next section specifies some of applications that use a reference clock, and describes how phase noise and frequency stability play a critical role in achieving the target performance of electronic system.

### *1.2 Phase noise from the local oscillator (LO) in an RF receiver.*

Phase noise present in the LO in a receiver can be modulated to the IF signal. As illustrated in Figure 1.1, the convolution of the desired signal and the interferer with the noisy LO spectrum results in a broadened down-converted interferer whose noise skirt corrupts the desired IF signal.

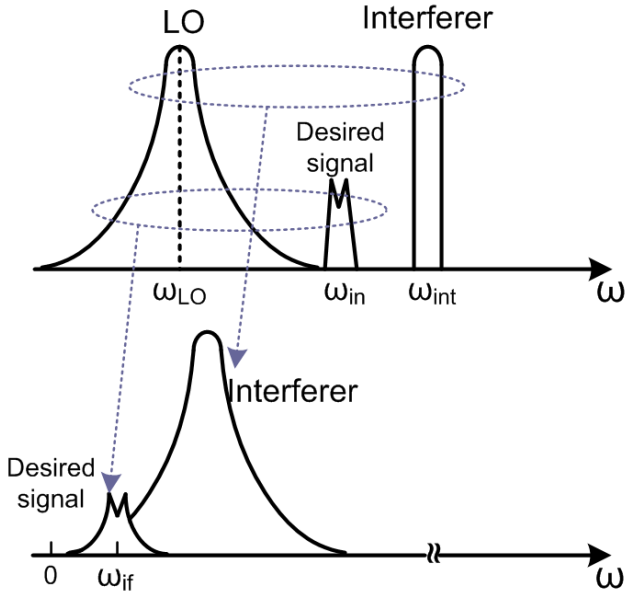
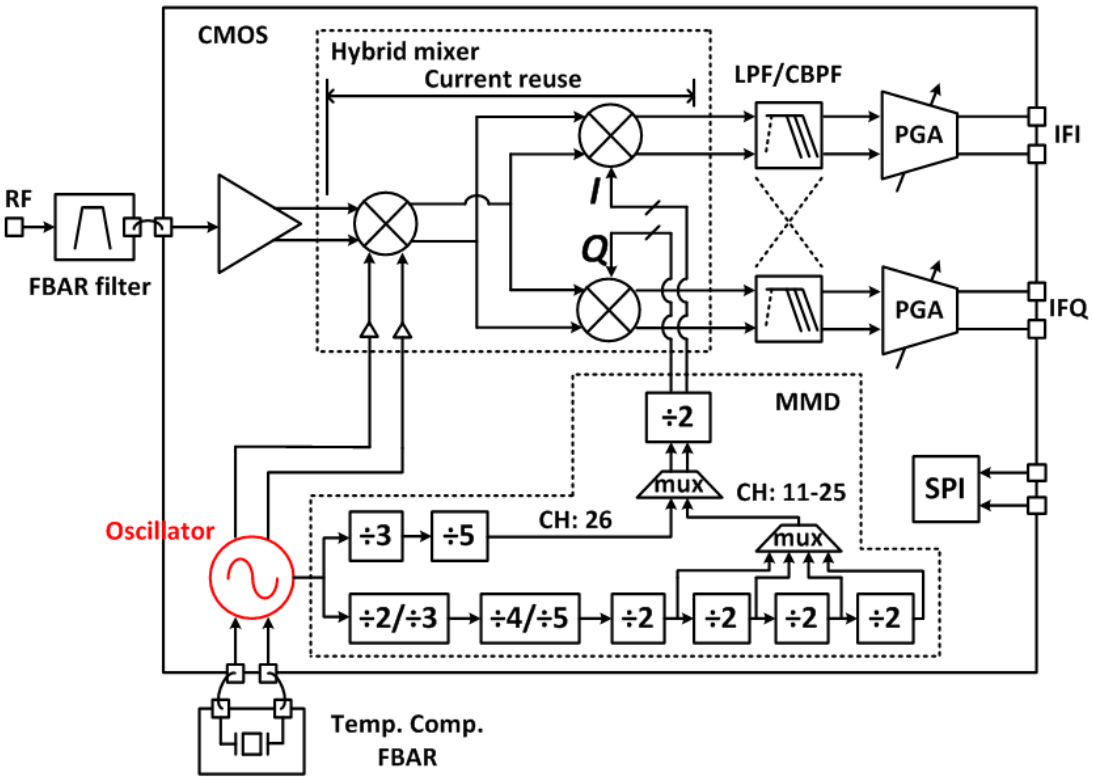
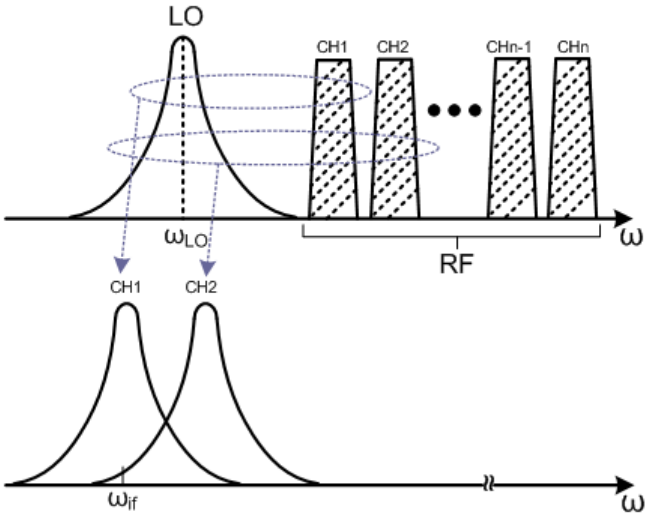



Figure 1.1. Signal down conversion with a noisy LO




a) Receiver for Zigbee application




b) Down converted channel with noisy LO

Figure 1.2 Block diagram of the receiver for (a) Zigbee application and (b) down converted channels with noisy LO

The noise in the LO can desensitize the receiver through reciprocal mixing. For more specific example, Figure 1.2(a) describes the block diagram of the Zigbee application where the 2.4GHz LO is used [5]. The Zigbee application has 16 channels, each channel having 5MHz channel spacing. If the phase noise of the LO is degraded enough to hurt its target spec. ( -105dBc/Hz @ 3.5MHz offset ), then the modulated IF channel would evade the adjacent channel and decrease the SNR. Therefore each radio standards limits the phase noise of the reference clock signal below a certain level according to the number of the channel and its spacing.

### *1.3 Reference clock used in Frac-N PLL*

In millimeter-wave (mm-Wave) applications, radios are often required to have very high bandwidth. Very wideband PLLs are required to perform high data-rate modulation as shown in Figure 1.3 [6]. With an increase in the reference frequency, the sampling frequency of the dithering algorithm in the fractional-N modulator increases, resulting in the reduction of quantization noise in the fractional-N modulator. A GHz-range low jitter fixed RF reference clock is necessary to boost the performance of an ultra-wideband PLL.

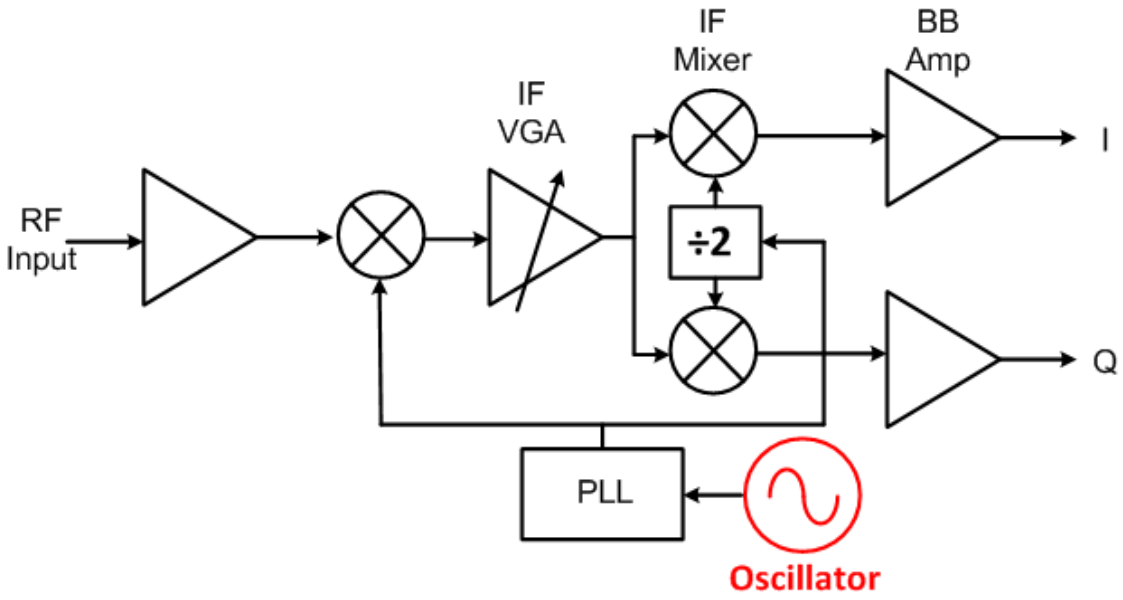



Figure 1.3 Block diagram of the 60GHz receiver with Frac-N PLL

*1.4 Sampling clock jitter effect on the data converters*

The low jitter clean reference clock is needed not only for the RF application, but also in the base band data processing. Once the RF signals are down converted into IF, they need to be transformed into a digital signal using an analog-to-digital converter (ADC). The analog to digital process relies upon a sample clock to indicate when a sample or snap shot of the analog signal will be taken. In order to accurately represent the analog data, the sample clock must be evenly spaced in time. Any deviation will result in a distortion of the digitization process. There is literature showing how the aperture uncertainty affects the ADC performance, especially the signal-to-noise ratio (SNR) [7]. The equation below shows how to calculate the associated maximum achievable resolutions, in SNR-bits.

$$\text{SNR bits} = \log_2\left(\frac{2}{\sqrt{3}\pi f_{samp}\tau_\sigma}\right) - 1 \qquad (1.1)$$

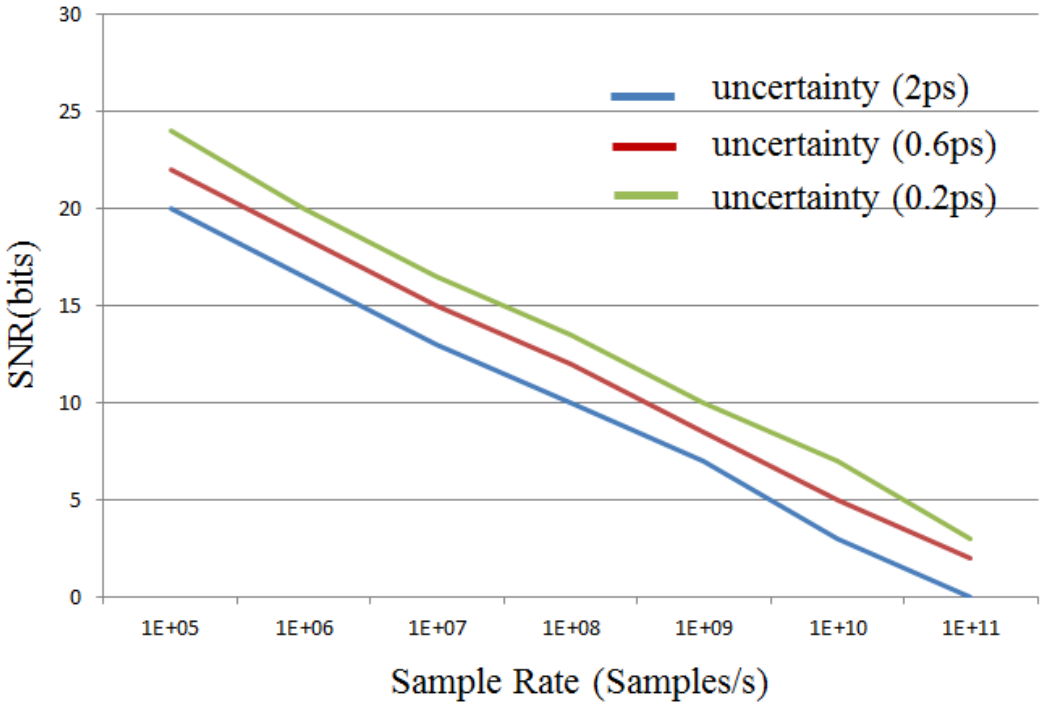



Figure 1.4 Signal-to-Noise ratio performance limitation due to aperture uncertainty

$f_{samp}$ and $\tau_\sigma$ represent the frequency of the sampling clock and the rms aperture jitter respectively. As shown in Figure 1.4, aperture jitter, in the range of 0.2ps to 2ps, limits SNR for the sampling frequency range of 2Ms/s to 4Gs/s.

### *1.5 Frequency drift of the oscillator under the temperature change*

Until now, the short-term frequency fluctuation of the oscillator, such as phase noise and jitter, has been highlighted to understand how it affects the wireless system as well as the base band data processing, and to confirm the needs of the state of the art technology related to the oscillator design.

However, the frequency drift of the oscillator under the temperature variation is also a very important spec. to be met in the various system applications [8-9]. Table 1 summarizes the frequency stability requirement for a few standards. Except for the USB application, all wireless systems require high frequency stability.

Table 1.1 Frequency stability specification for various standards

| **Wireless application** | **Frequency stability (ppm)** |
|---|---|
| **USB 3.0 host controller** | ±300 |
| **Wi-Fi** | ±20 |
| **WLAN** | ±20 |
| **Bluetooth** | ±20 |
| **GPS** | 1~2 |

### *1.6 Contribution of this thesis.*

As described in the subsection above, short-term frequency fluctuation of the oscillator and frequency drift over temperature change are critical properties to be mitigated in the wireless system. Therefore, my thesis will focus on

- **FBAR and AlN contour mode resonator overview**

  Chapter 2 gives an overview of the MEMS resonator such as FBAR and AlN contour mode resonator (CMR) and show their mechanism with each characteristic.

- **Close-in phase noise improvement technique**

  Chapter 3 mainly describes the proposed oscillator structure that can achieve low power consumption and low phase noise. It will analyze every detail of the design to show its advantages over the conventional structure. The proposed circuit achieves more than 10dB lower phase noise at close-in offset frequency with 350uW power consumption with 2GHz FBAR device. Further for the purpose of comparison, the performance of the conventional Colpitts oscillator using FBAR or AlN CMR device will be shown.

- **Oven controlled temperature compensation technique**

  Chapter 4 proceeds to depict the system for removing the temperature induced frequency drift. The sensor and heater are integrated into FBAR chip. The first prototype system will be introduced with its issue. Several issues in the first design were rectified and an improved version of the system was fabricated by using 65nm technology. The second version chip achieves ±1.6ppm frequency drift when the temperature changes from -10$^{o}$C to 80$^{o}$C. The temperature sensor has high resolution of 150uK.

# Chapter 2.

# QUARTZ REPLACEMENTS FOR REFERENCE CLOCK

## *2.1 Quartz replacement*

All wireless application such as Bluetooth, Wi-Fi and Zigbee operate at a specific frequency. This necessitates systems to have a reference clock. The current radio systems are still using quartz crystal to utilize its high quality factor ( > 100,000). But, quartz crystal is becoming a bottleneck in achieving small size and cost [10]. Figure 2.1 shows a deployable bio-signal system designed by the wireless sensing lab in University of Washington. The quartz crystal is comparative in size to the integrated IC on the PCB. As the size of the integrated chip keeps shrinking due to the development of technology, quartz crystal will be the biggest component in the wireless system in the near future.

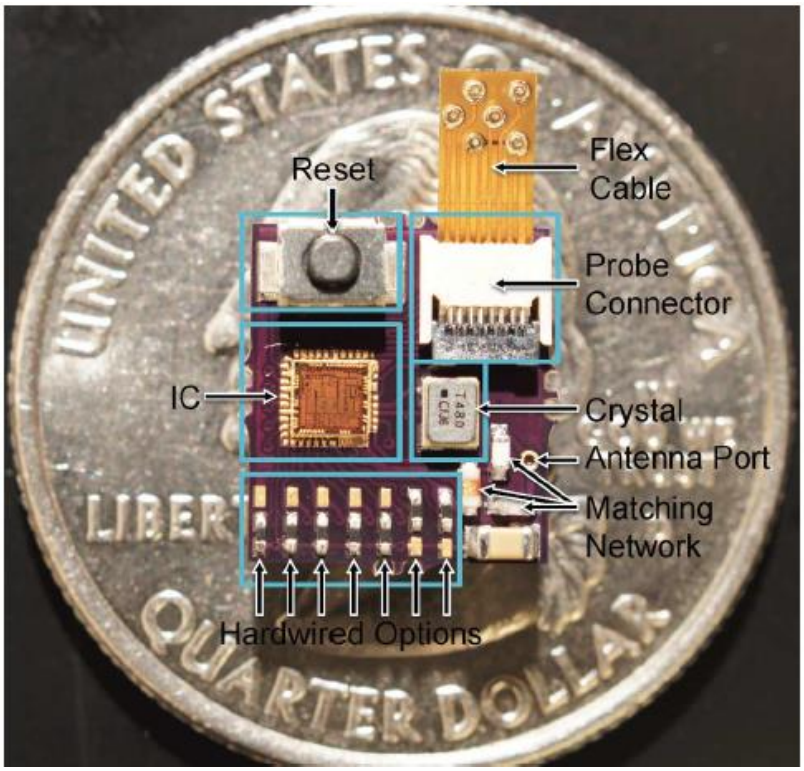



Figure 2.1 Deployable bio-signal system [11]

The resonant frequency of quartz crystal is normally 10MHz or so. However, the transceiver and receiver of wireless systems, such as BLE (Bluetooth low energy), WLAN and Zigbee applications, require a reference clock whose frequency is in the GHz frequency range. Therefore, frequency synthesizer is used to generate such high frequency reference clock from quartz crystal [12]. However, the power consumption of frequency synthesizer is very high. Hence, there has been a bottleneck in achieving low power system. Figure 2.2 shows an example of how all frequency synthesizer related blocks consume more than 35% of the receiver power [13].

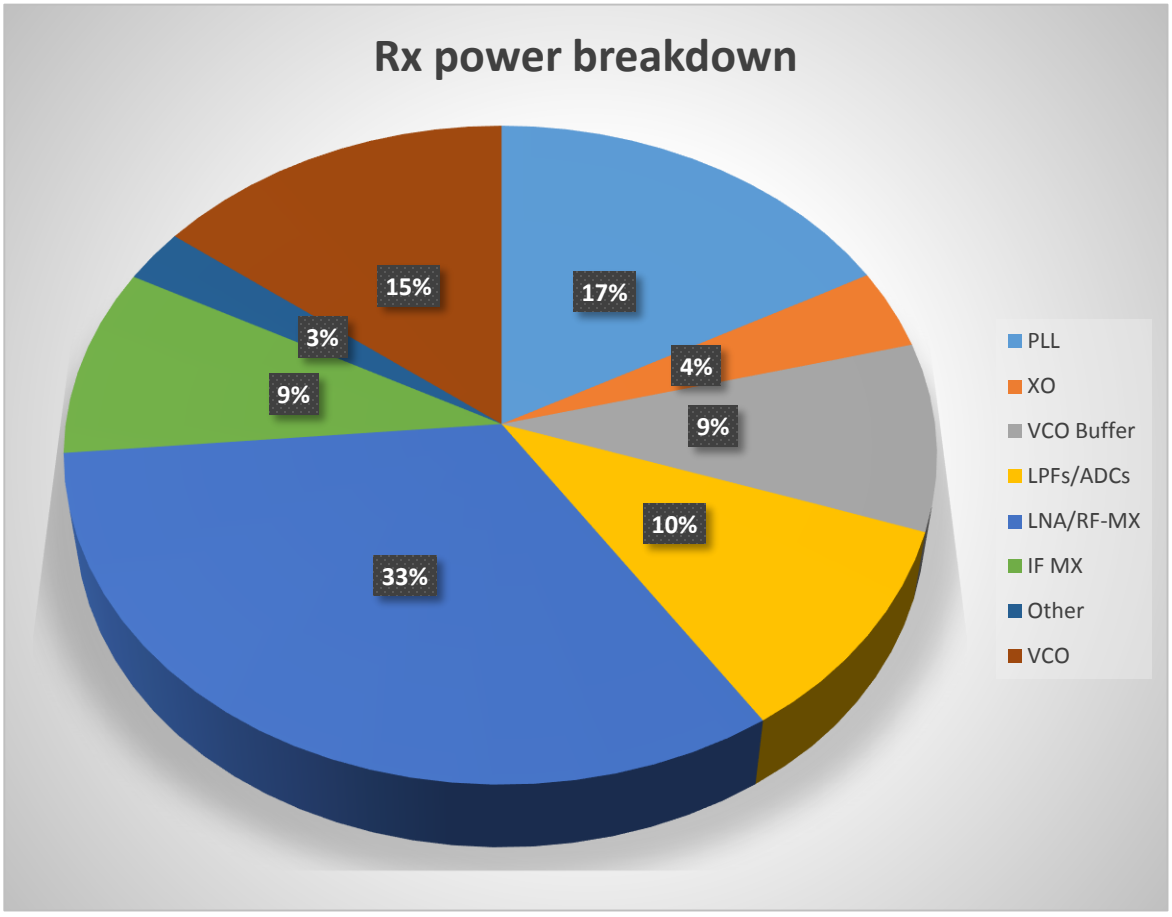


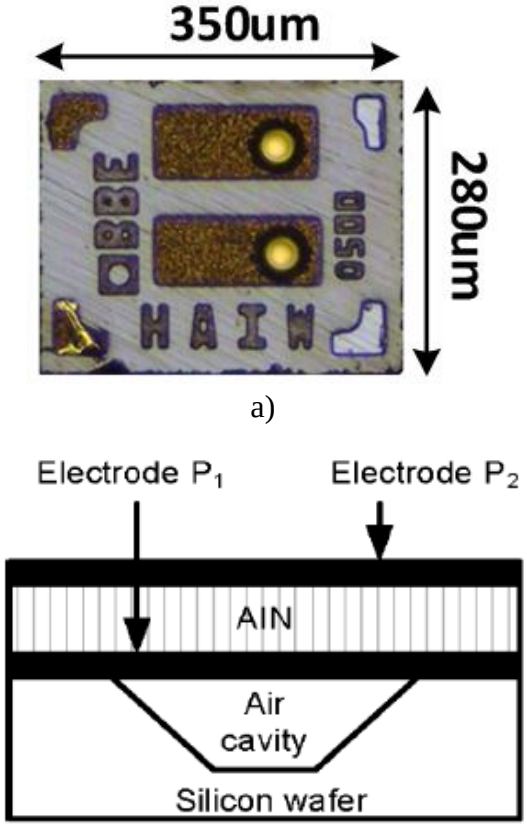

Figure 2.2 The measured Bluetooth low energy receiver power breakdown [13]

Next generation wireless systems need a new class of radios that offer cost/size benefit. A miniature, high quality factor (Q) resonator, fabricated using wafer-scale semiconductor processing will be a good alternative to quartz crystal and will enable us to achieve a sub $mm^3$ volume [10]. For example, resonators fabricated using MEMS (Micro-Electro-Mechanical-

Systems) technology such as FBAR (Film Bulk Acoustic Resonator) or AlN CMR (Aluminum Nitride Contour mode Resonator) have emerged as a very promising and competitive alternative due to their small form-factor, high operating frequency (up to GHz), and especially their possibility to be fully integrated with Integrated Circuits (IC) to form a single chip. Large scale MEMS-IC co-integration will lead to reduction in fabrication cost, routing parasitics and power consumption [14]. The following section gives a more detailed overview of both FBAR and AlN CMR.

## *2.2 Film Bulk Acoustic Resonator*

Film Bulk Acoustic Resonator (FBAR) are high Q piezoelectric bulk acoustic wave resonators operating in the GHz frequencies. A free standing membrane containing a piezoelectric material called aluminum nitride (AlN) is sandwiched between two Molybdenum electrodes. Figure 2.3 shows the die photo and the cross section respectively.




a)

b)

Figure 2.3 (a) Die photo of FBAR and (b) cross section view

The FBAR's Q factor is normally between 1500 and 2000 at parallel frequency and effective coupling coefficient is the order of 2% to 3%. Figure 2.4 shows the characteristic of FBAR over frequency. There are two key points to be focused on here, parallel frequency ($f_p$) and series frequency ($f_s$). Between these two points, FBAR operates like an inductor; otherwise it behaves like a capacitor. The maximum impedance can be obtained at parallel frequency and minimum impedance at series frequency. The high Q factors mentioned above are achieved at both points. Hence, in theory, oscillators using FBAR should operate at either parallel frequency or series frequency in order to take advantage of its high Q. In reality, however, capacitive loading from oscillators or any parasitic capacitance from wirebonding moves the oscillator's operating point away from series or parallel frequency.

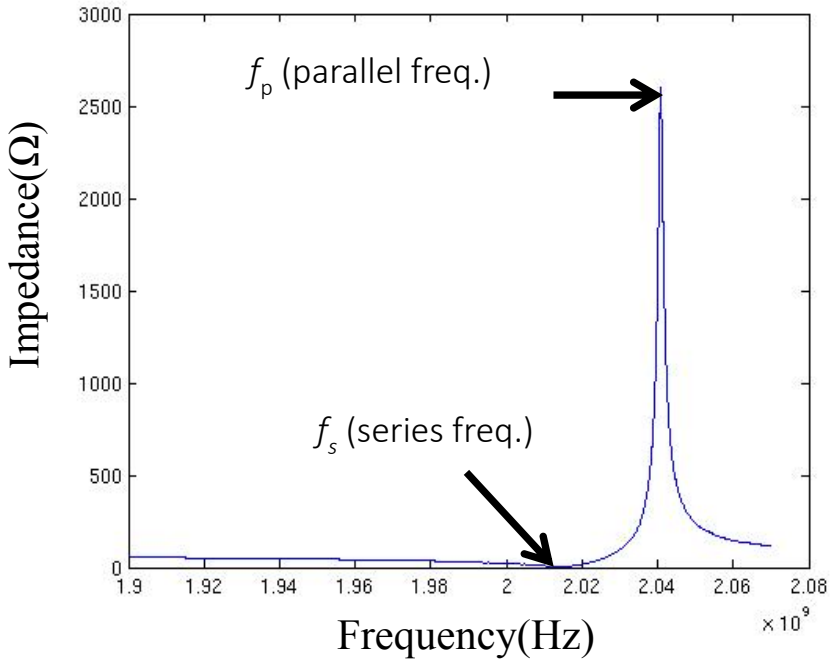
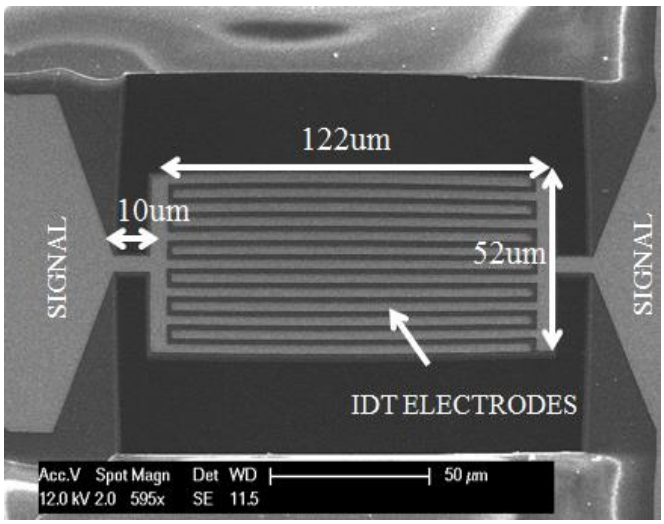


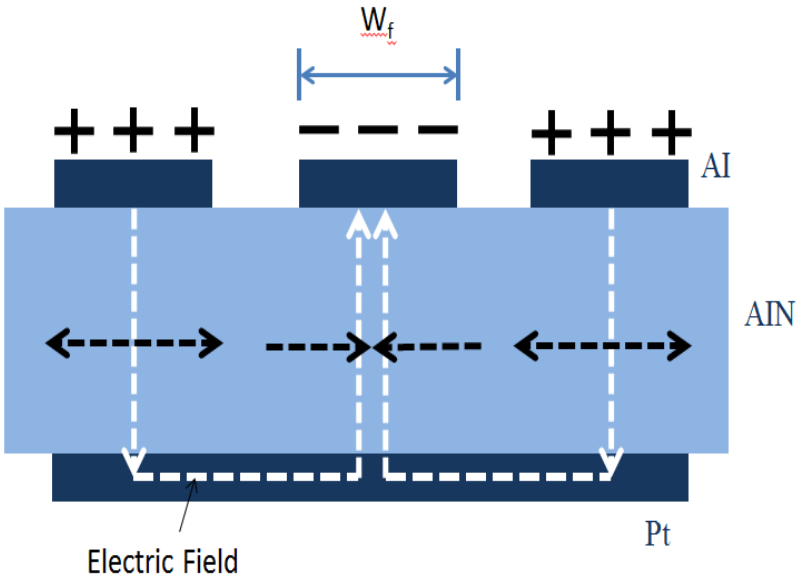

Figure 2.4 Impedance characteristic of FBAR over frequency

*2.3 Aluminum Nitride Contour-mode Resonator (AlN CMR)*

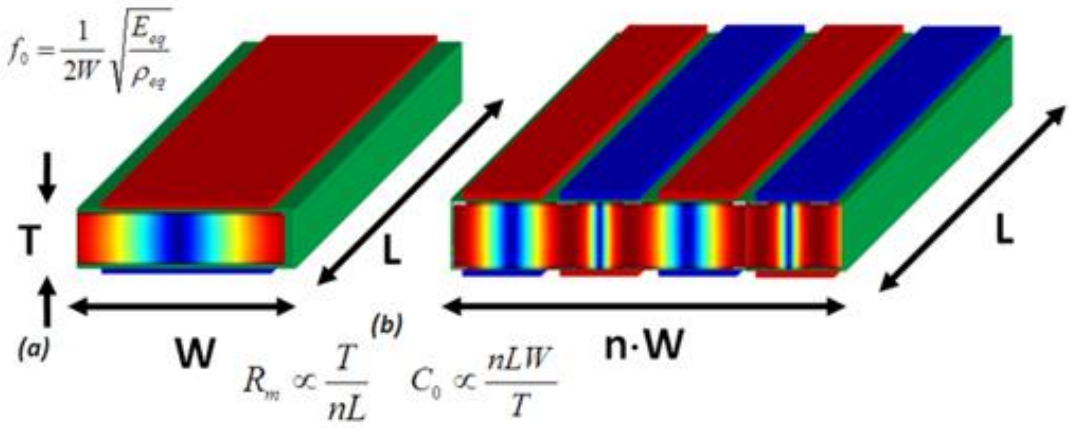
The Aluminum Nitride Contour-mode Resonator (AlN CMR) is formed by using a vibrating AlN plate sandwiched between a bottom metal plate (Pt) and a patterned top electrode (Al). Figure 2.5 shows the SEM picture of 1GHz AlN CMR and its cross section. Interdigitated metal lines connected alternatively to positive and ground voltages form the top electrode. These electrodes generate electric field lines which are the white dotted lines in Figure 2.5 (b) across the piezoelectric material (AlN) [15]. The field lines are directed primarily along the thickness of the film by the presence of the bottom floating plate.




(a)




(b)




(c)

Figure 2.5 (a) SEM picture of 1GHz AlN CMR, (b) the cross section and (c) frequency dependency over geometry of device

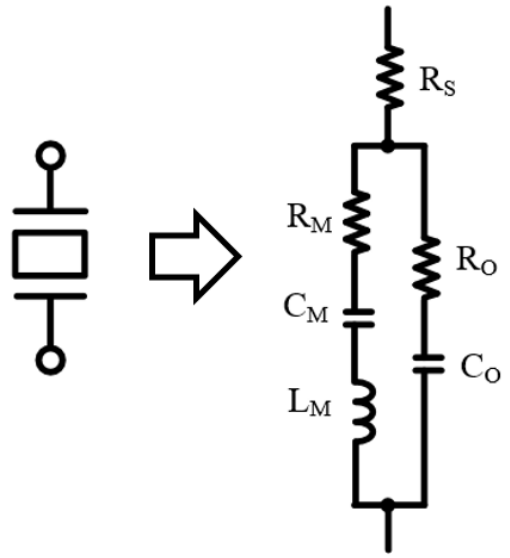
Table 2.1 $Kt^2$, Q and $R_p$ characteristic of AlN CMR

| **Aluminum Contour-mode Resonator** | | |
|---|---|---|
| **$R_p$ (Impedance @ $f_p$)** | **Q** | **$Kt^2$** |
| 19k~21k | 1000~4000 | 0.99% |

The resonance frequency ($f_r$) of this device is set by two parameters: the electrode pitch (or finger width ($W_f$)) and the acoustic velocity of the resonator stack $(E/\rho)^{1/2}$. Table 2 shows the three critical properties of AlN CMR. Compared to FBAR's, the coupling coefficient of AlN CMR is smaller, otherwise Q and $R_p$ are larger which lead to low phase noise and low power consumption of the oscillator.

Further, the electrical behavior can be represented using an equivalent circuit called the Modified Butterworth-Van Dyke (MBVD) model [16]. The finite-Q mechanical resonance is described by the motional branch $C_M$, $L_M$, and $R_M$, the electrical capacitance and loss existing in the piezoelectric transducer and substrate parasitics are all lumped into $C_O$ and $R_O$; finally $R_S$ is used

to account for the resistance of the routing pads and electrodes [14]. Figure 2.6 shows the circuit symbol and MBVD equivalent circuit of the AlN CMR device.




(a) (b)

Figure 2.6 (a) Circuit symbol and (b) MBVD equivalent circuit of AlN CMR

With the geometry and equivalent circuit parameters already known, the resonator can be further characterized by a physical model as expressed by the following equations [17]:

$$C_O \approx n\varepsilon_{33}\varepsilon_O \frac{WL}{T}, \qquad R_M = \frac{1}{n}\frac{\pi}{8}\frac{T}{L}\frac{\rho_{eq}^{1/2}}{E_{eq}^{3/2} d_{31}^2 Q_{su}},$$

$$C_M = n\frac{8}{\pi^2}\frac{WL}{T}E_{eq}d_{31}^2, \qquad L_M = \frac{1}{n}\frac{\rho_{eq}}{8}\frac{WT}{L}\frac{1}{E_{eq}^2 d_{31}^2},$$

$$w_s = 2\pi f_s = \frac{\pi}{W}\sqrt{\frac{E_{eq}}{\rho_{eq}}}$$

where $\varepsilon_O$ is the permittivity of free space, $\varepsilon_{33}$ is the dielectric constant of AlN along the c-axis; *L*, *W* and *T* refer to the length, width and thickness of the sub-resonator respectively; *n* is the number

of sub-resonators (fingers); $E_{eq}$ and $\rho_{eq}$ are the equivalent in-plane modulus of elasticity and mass density of AlN and the stacked electrodes; $d_{31}$ is the (3, 1) entry in the AlN's *d*-form piezoelectric coefficient matrix; $w_s$ is the series resonant frequency and $Q_{su}$ is the unloaded quality factor at series resonance [14].

# Chapter 3.

# TRANSFORMER COUPLED COLPITTS OSCILLATOR DESIGN

## *3.1 Introduction*

A variety of oscillator technologies exists today. For mainstream consumer-type applications, two technology families are distinguished as shown in table 2: mechanical and electrical oscillators. In mechanical oscillators, the frequency selective element is a MEMS-based mechanical resonator made from piezoelectric material such as FBAR and AlN CMR explained at previous chapter.

Table 3.1 Oscillator type

| **Type** | **Characteristic** |
|---|---|
| Mechanical Oscillator | • MEMS based resonator (ex. FBAR, AlN CMR)<br>• Quality factor (Q) ~ 2000<br>• FoM > 200dB<br>• Large size (ex. 350um x 280um for FBAR) |
| Electrical Oscillator | • On-chip inductor and Capacitor<br>• Quality factor (Q) of LC : 10~15<br>• FoM < 190dB<br>• Small size (ex. 140um x 140um for L in BLE application) |

$$\text{FoM} = -\text{L}(\Delta\text{f}) + 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log(P(mW))$$

These resonators have a high quality factor, and the oscillator using this can achieve lower phase noise compared to that of electrical oscillator. When the FOM is calculated with phase noise,

power consumption and operating frequency, MEMS based oscillators achieve around 200dB otherwise the state of the art electrical oscillators achieve around 190dB. In electrical oscillators, the frequency selective element is integrated on a chip and comprises an inductor and a capacitor. However, the quality factor of the inductor and the capacitor is smaller than that of the mechanical resonator. The use of electrical oscillators is, therefore, limited to applications where accuracy and noise specification is relaxed [1]. That's why the micro electromechanical systems (MEMS) resonators and oscillators have received a lot of press in the past 5 years.

In addition, piezoelectric materials such as aluminum nitride inherently offer lower electromechanical coupling coefficients ($Kt^2$) that achieve gigahertz frequencies and demonstrate high Q factors. Despite being a proven technology, FBARs and shear-mode quartz resonators do not permit economical manufacturing of a single-chip RF module, because multiple frequency selective arrays of piezoelectric resonators cannot be easily fabricated on the same substrate since film thickness determines the frequency [18]. For this reason, the device called AlN contour-mode resonator is also used in the oscillator design in this work since its fundamental frequency is determined by in-plane dimensions. This resonator is fabricated and given by a team led by Professor Gianluca Piazza at Carnegie Mellon University.

Given the fact that a resonator having high Q for low phase noise is provided, the circuit sustaining oscillation becomes the next stage to be investigated. Long story short, the proposed architecture helps to boost the performance more. A detailed analysis will follow later, but at first, the following sections describe in more detail about conventional oscillators in order to highlight the performance comparison.

### *3.2 CMOS Class-D VCO using LC*

Figure 3.1 shows the class-D oscillator using integrated LC. It is capable of an excellent phase noise performance even with a very low power supply compared to other LC oscillators [19]. However, due to the limited Q factor of the integrated inductor which is between 10 and 15, it is hard to achieve an electrical performance better than that of oscillators using MEMS-based resonator. It draws 10mA from 0.4V power supply. The phase noise at 10MHz offset from 4.8GHz is -143.5dBc/Hz.

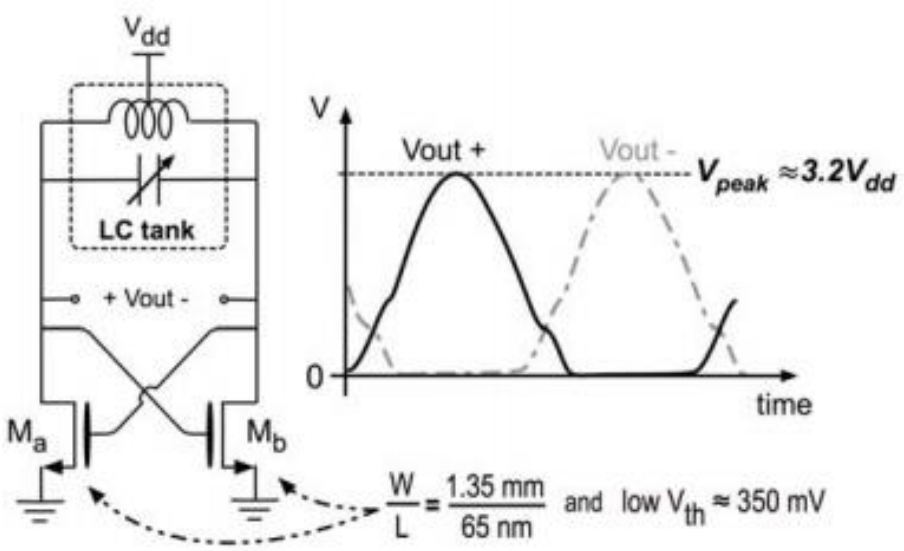



Figure 3.1 CMOS Class-D VCO

### *3.3 Differential Colpitts oscillator using FBAR*

Figure 3.2 represents the block diagram of differential Colpitts oscillator using 2.5GHz FBAR with single-ended structure. This oscillator is designed for the Zigbee receiver application [20]. An ac equivalent circuit of the single-transistor Colpitts oscillator is shown in Figure 3.3 for analysis purpose. It consists of a noninverting amplifier whose open-loop voltage gain is denoted by A, and a noninverting frequency-selective feedback network whose voltage gain is denoted by β. The load resistance is denoted by $R_L$. The closed-loop gain $A_f$ of the oscillator is given by [21]

$$A_f = \frac{v_O}{v_f} = \frac{A}{1 - A\beta} = \frac{A}{1 - T}$$

where T = Aβ is the loop gain, $v_o$ and $v_f$ are the output and the feedback voltages, respectively. As mentioned in the previous chapter, when FBAR operates between $f_p$ (parallel frequency) and $f_s$ (series frequency), we can assume that FBAR works as an inductor and $L_{MEMS}$ as shown in figure 3.3.

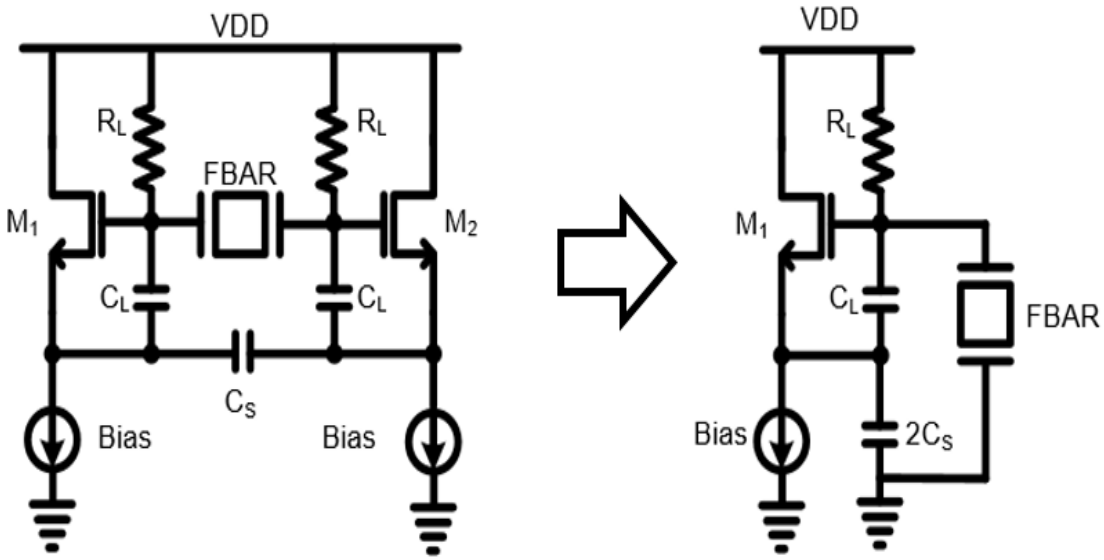



Figure 3.2. Block diagram of the differential colpitts oscillator and its equivalent single-ended structure

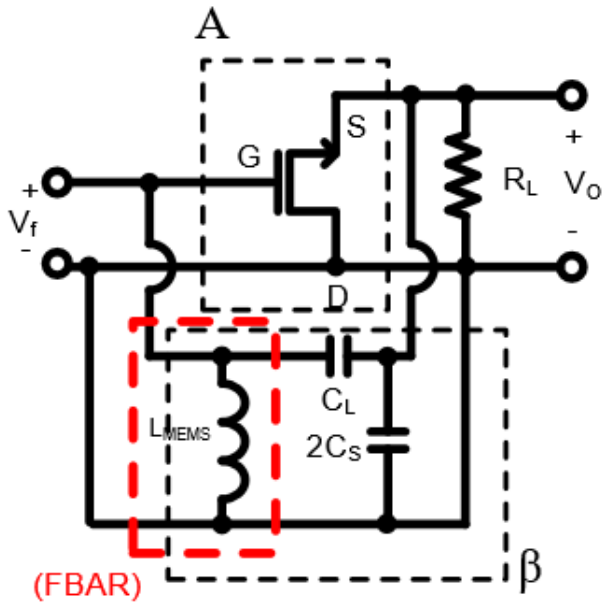



Figure 3.3 AC equivalent block diagram of the single-ended colpitts oscillator

The condition for steady-state oscillation at the oscillation frequency *f* is given by [21]

$$T(f) = A(f)\beta(f) = |T(f)|e^{j\emptyset T(f)} = 1 + (0 \times \mathrm{j})$$

The Barkhausen magnitude criterion for steady-state oscillation at the oscillation frequency *f* is given by

$$|T(f)| = 1$$

and the Barkhausen phase criterion for oscillation is

$$\emptyset_T(f) = 0 \pm n360^O$$

At *f*, the magnitude of the loop gain must be equal to unity and the phase shift around the loop must be zero. The criterion of the real part of the loop gain for oscillation is expressed as

$$Re[T(f)] = 1 \qquad (3.1)$$

and the criterion of the imaginary part of loop gain for oscillation is given by

$$Im[T(f)] = 0 \qquad (3.2)$$

In order for the oscillations to start and grow, the magnitude of the loop gain *T* must be greater than unity. A small signal model of the Colpitts oscillator is shown in Figure 3.4. The NMOS in Figure 3.3 is replaced by a voltage dependent current source $gmv_{gs}$ where $v_{gs} = v_f - v_O$. The current through the series combination of L and $C_1$ is

$$i = \frac{v_O}{(sL_{MEMS} + \frac{1}{sC_1})} = v_O\left(\frac{sC_1}{1+s^2L_{MEMS}C_1}\right) \qquad (3.3)$$

and the current through L is

$$i = \frac{v_f}{sL_{MEMS}} \qquad (3.4)$$

Equating (3.3) and (3.4), we have

$$v_O = v_f\left(\frac{s^2 L_{MEMS}C_1+1}{s^2 L_{MEMS}C_1}\right) \quad (3.5)$$

Applying KCL at the source of the NMOS in Figure 3.4, we have

$$v_O\left(\frac{sC_1}{s^2 L_{MEMS}C_1+1} + \frac{sC_2R_L+1}{R_L} + g_m v_O\right) - g_m v_f = 0 \quad (3.6)$$

Substituting (3.5) in (3.6), we have

$$v_f\left(\frac{s^2 L_{MEMS}C_1 + 1}{s^2 L_{MEMS}C_1}\right)\left(\frac{sC_1}{s^2 L_{MEMS}C_1 + 1} + \frac{sC_2R_L + 1}{R_L} + g_m\right) - g_m v_f = 0$$

Assuming $v_f \neq 0$ and simplifying the above equation leads to

$$(L_{MEMS}C_1C_2R_L)s^3 + (L_{MEMS}C_1)s^2 + R_L(C_1 + C_2)s + g_mR_L + 1 = 0$$

The above equation is the characteristic of the Colpitts oscillator [21]. Substituting $s = j\omega$ and rearranging the real and imaginary terms lead to

$$(1 + g_mR_L - \omega^2 L_{MEMS}C_1) + j[\omega R_L(C_1 + C_2) - \omega^3 L_{MEMS}C_1C_2R_L]$$

Equating the imaginary part to zero, the equation for the oscillation frequency is derived as

$$\omega_O = \frac{1}{\sqrt{L_{MEMS}\left(\frac{C_1C_2}{C_1 + C_2}\right)}} rad/s$$

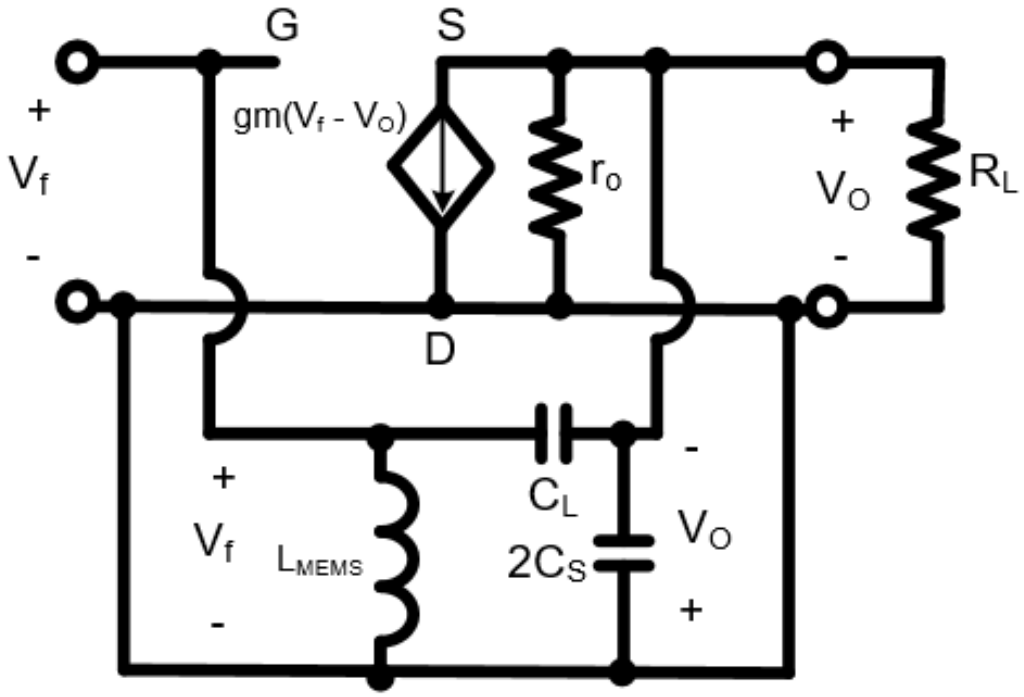



Figure 3.4 Small-signal model of the single-ended Colpitts oscillator

We have analyzed Colpitts oscillator for operating frequency. Now, it is time to derive the minimum transconductance ( $g_m$ ) needed for oscillation. It helps to evaluate the power consumption of the oscillator. First, it is essential to understand how the active device and other passive components, $C_1$ and $C_2$ in Colpitts oscillator case, lead to oscillation. To make the structure oscillate, the impedance looking at nodes connecting FBAR should be negative in order to cancel out the parasitic resistance inside FBAR. Figure 3.5 shows the simplified block diagram of the single-ended oscillator with test voltage. By deriving amount of current flowing out from the test voltage, impedance can be calculated.

As shown in Figure 3.5, *A* represents the capacitive network consisting of $C_1$ and $C_2$, which is $\frac{C_1}{C_1+C_2}$. The source voltage is equal to $AV_t$,and by applying KCL at the source, we get:

$$g_m(1-A)V_t = -i_t$$

$$g_m \frac{C_2}{C_1+C_2} V_t = -i_t$$

$$R_p = \left|\frac{V_t}{i_t}\right| = \frac{1}{g_m}(1 + \frac{C_1}{C_2})$$

The above equation indicates the impedance that will be canceled out (in this work, parallel impedance).

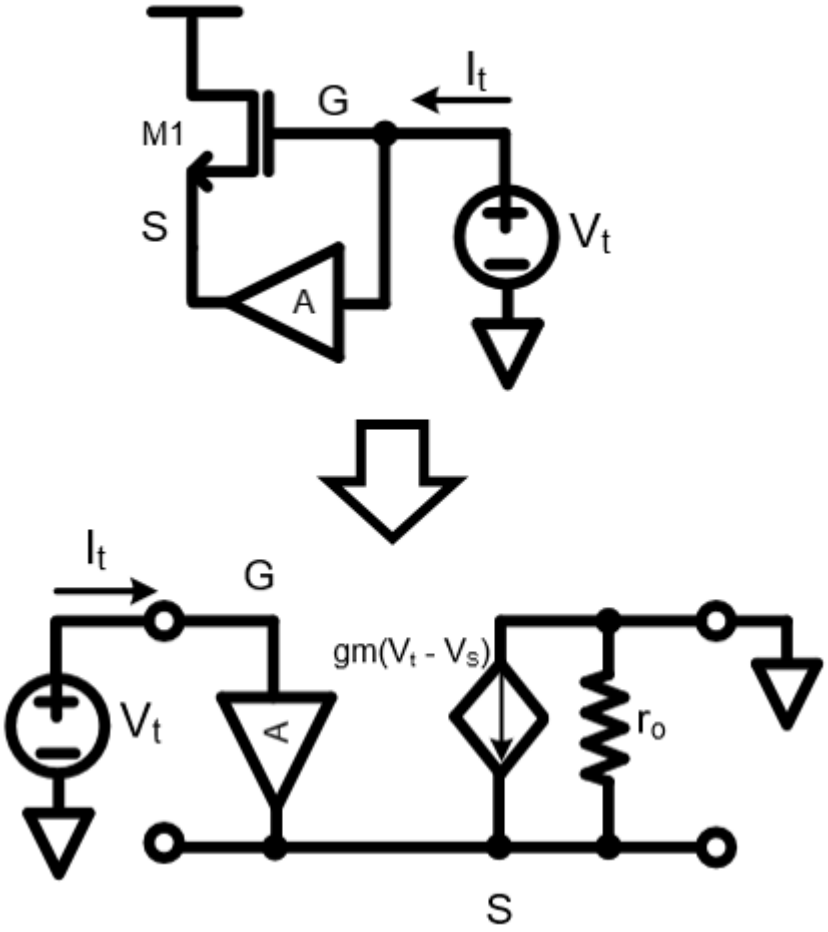



Figure 3.5 Small signal model with test voltage.

In other words, the minimum transconductance required for oscillator to have is shown below.

$$g_{m,min} = \frac{1}{R_p}(1 + \frac{C_1}{C_2})$$

Based on equation, to achieve the low power consumption, either $R_p$ needs to be smaller or capacitance ratio between $C_1$ and $C_2$ should be small. But, $C_2$ cannot be increased as much as we

want. Large capacitive loading moves the operating point to lower frequency than to parallel frequency resulting in lowering both quality factor and $R_p$. Then, enough loop gain cannot be obtained. In this work, 300fF is used for $C_2$ and 100fF for $C_1$.

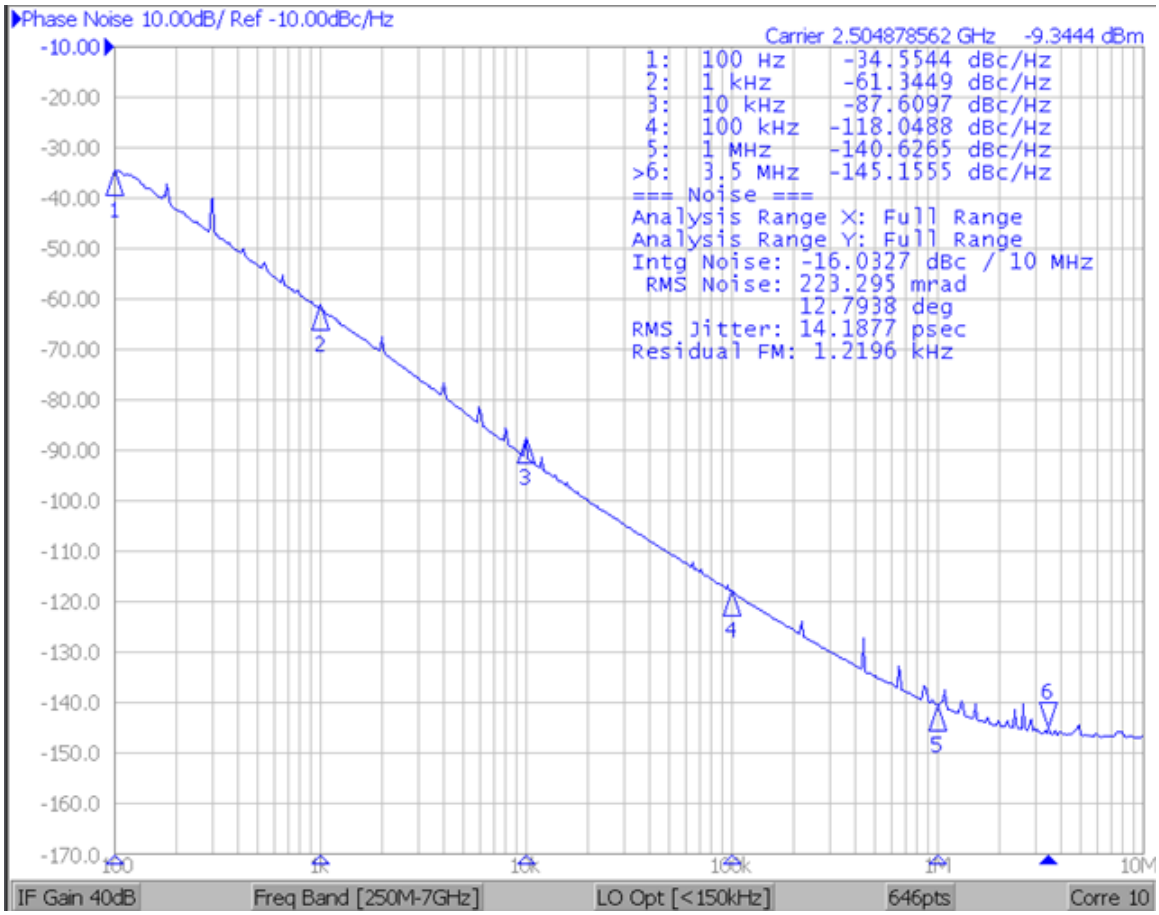



Figure 3.6 Measured phase noise of the Colpitts oscillator using FBAR

Figure 3.6 shows the test result of the Colpitts oscillator in terms of phase noise. This chip is fabricated by TSMC 65nm technology for the Zigbee receiver [20]. One thing I need to clarify is that when this chip was taped out, the back-lapping process was skipped because of our mistake. Back-lapping is one of the steps, where the chip is fabricated; grinding the backside of the chip. Normally, the thickness of the chip is 100um after this process. However, our chip has 800um thickness. That's why there is a huge difference in terms of height between FBAR and main chip resulting in longer wires are needed for wirebonding than other cases.

Figure 3.7 shows the die photo of it. On the top of the photo, you can check that long wires are used. I worried that parasitic components from those long wire may degrade the performance. Fortunately, phase noise at 3.5MHz offset frequency is much lower than Zigbee spec. (-105dBc/Hz). Table 3.2 summarizes the test result. Table 3.3 shows the detail phase noise result.

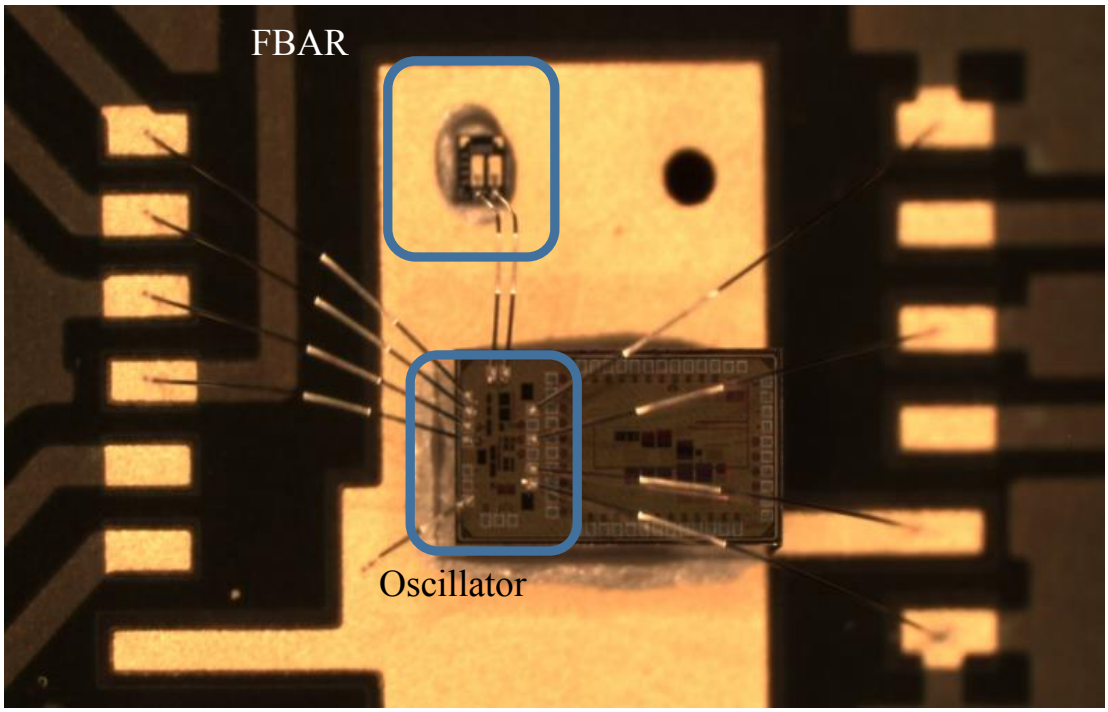



Figure 3.7 Die photo of Zigbee receiver with FBAR

Table 3.2 Summarized test result for Colpitts oscillator with FBAR

| **Test result summary** | |
|---|---|
| **Power supply** | 0.5V ~ 1V |
| **Power consumption** | 660uW at 0.5Vdd |
| **Operating freq.** | 2.5GHz |
| **Tech.** | 65nm CMOS technology |

Table 3.3 Measured phase noise performance

| | **1kHz** | **10kHz** | **100kHz** | **1MHz** | **3.5MHz** |
|---|---|---|---|---|---|
| **Test(dBc/Hz)** | -61.3 | -87 | -118 | -140 | -145 |
| **Zigbee spec.** | - | - | - | - | -105 |

### *3.4 Differential Colpitts oscillator using AlN CMR*

Same differential Colpitts oscillator shown in Figure 3.2 is utilized with the AlN CMR device [22]. As AlN CMR chips are already exposed to air, it was hard to dice them separately. Therefore, one die containing several devices has to be attached to the test board and only one of them can be used for wirebonding at that time. Figure 3.8 shows the die photo of this test. There are long wires between the oscillator and the AlN CMR device. This contributes to higher power consumption than the simulation result. This Colpitts oscillator is fabricated by IBM 130nm CMOS technology. The operating frequency is 1GHz with 1V power supply. Although it consumes large power, 4mW, the phase noise performance is really good compared to other oscillators using MEMS resonator. It achieves -173dBc/Hz at 1MHz offset frequency with 2.9ps RMS jitter. Table 3.4 and 3.5 shows detailed test results with phase noise at each offset frequency with the above FBAR result.

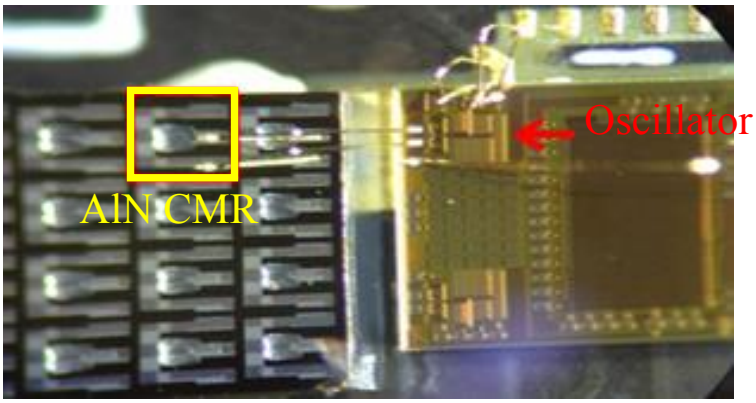



Figure 3.8 Die photo of Colpitts oscillator using AlN CMR

Table 3.4 Summarized test result of Colpitts oscillator using AlN CMR

| **Test result summary** | |
|---|---|
| **Power supply** | 1V |
| **Power consumption** | 4mW at 1Vdd |
| **Operating freq.** | 1.1GHz |
| **RMS Jitter** | 2.9ps |
| **Tech.** | 130nm CMOS technology |

Table 3.5 Measured phase noise of Colpitts oscillator using AlN CMR

| | **1kHz** | **10kHz** | **100kHz** | **1MHz** |
|---|---|---|---|---|
| **AlN CMR (dBc/Hz)** | -82.3 | -113 | -143 | -173 |
| **FBAR (scale)** | -68.9 | -94.6 | -125.6 | -147.6 |

Table 3.5 compares the phase noise of the oscillator using AlN CMR with FBAR oscillator. As FBAR based oscillator works at 2.5GHz, the measured phase noise values are scaled to 1.1GHz for a fair comparison. As you see, AlN CMR based Colpitts oscillator has superior phase noise performance over FBAR. This is because AlN CMR device has higher Q and $Kt^2$ compared to FBAR. However, one drawback is that the yield of it is pretty low. Among 5 devices, there is only one that is working. Figure 3.9 shows the phase noise shape. For the correct measurement, correlation number in source analyzer (E5052B Agilent) is set to maximum. The larger correlation number is, the more environment factors are taken into account in the equipment to subtract noise coming from them assuming those noise are uncorrelated. Although it takes several hours, more accurate result can be obtained. The * mark represents the noise floor of the equipment itself. If

the noise floor of the oscillator is lower than that of source analyzer, we may not be able to differentiate between them.

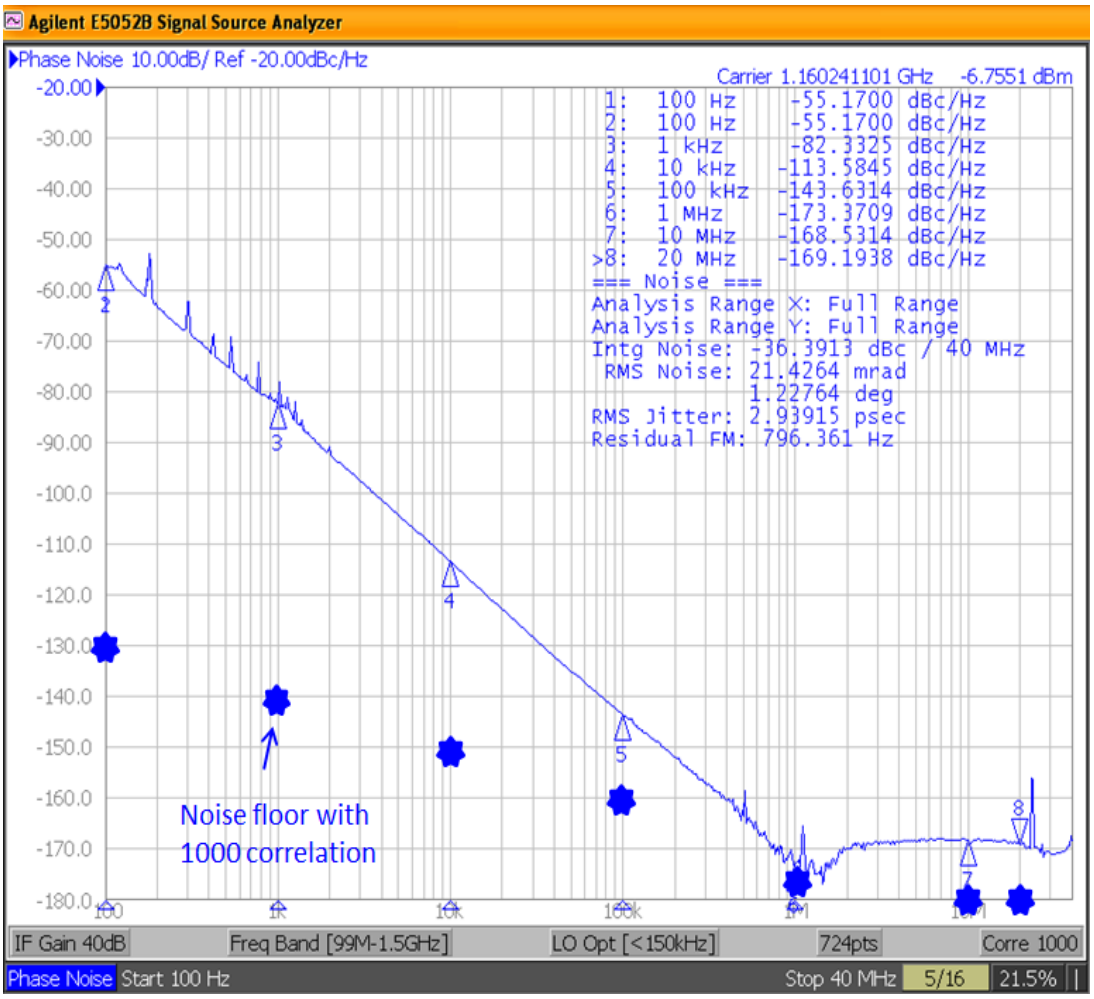
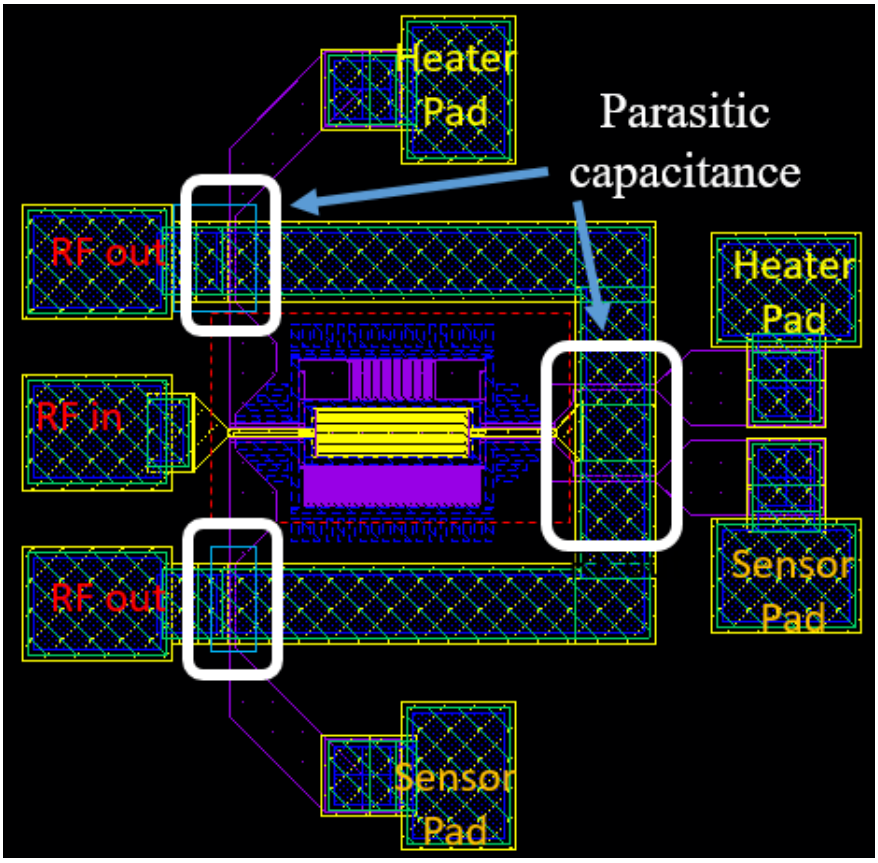


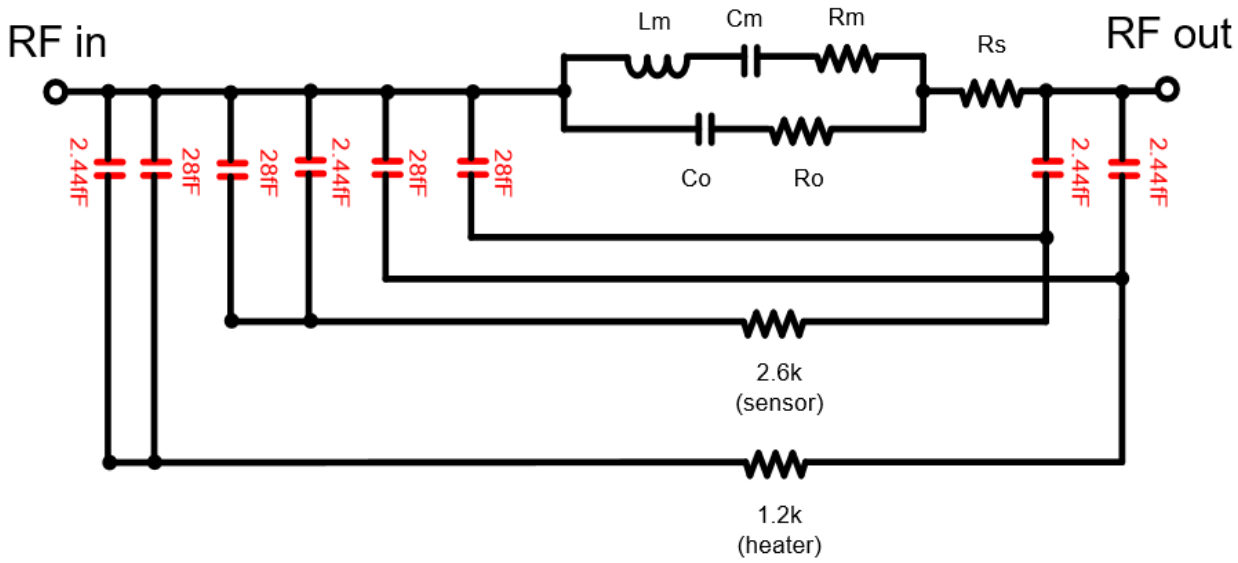

Figure 3.9 Measured Phase noise of AlN CMR with noise floor of test equipment

This test result is based on the AlN CMR device which was fabricated in 2012. Newly fabricated devices are received from Carnegie Mellon University team recently. Unfortunately, there are parasitic capacitances between the sensor and the heater, which are unavoidable due to its structure. Sensor and heater are essential components for building up temperature compensation system. Those components will be covered in detail in the later sections.

Figure 3.10 shows the layout of AlN CMR and indicate which spots contribute to such undesirable capacitance. The mBVD model is alos shown in order to show how these capacitors are connected to each other.




(a)




(b)

Figure 3.10 (a) Layout of the AlN CMR with specific area contributing parasitic capacitance and (b) its mBVD model

Due to the parasitic capacitances, the power consumption is larger and phase noise performance is higher compared to the simulation result. Another issue is that this device has spurious modes. Figure 3.11 shows the admittance changes according to frequency. In case of FBAR, there are only two frequencies where admittance (or impedance) has minimum and maximum as shown in Figure 2.4. But, AlN CMR has two parallel frequencies at which oscillator can work. For example, an oscillator can be tuned to work at spurious 2 modes. Since the impedance of this point is smaller than spurious 1 mode, it requires more power consumption than when the oscillator works at spurious 1 mode.

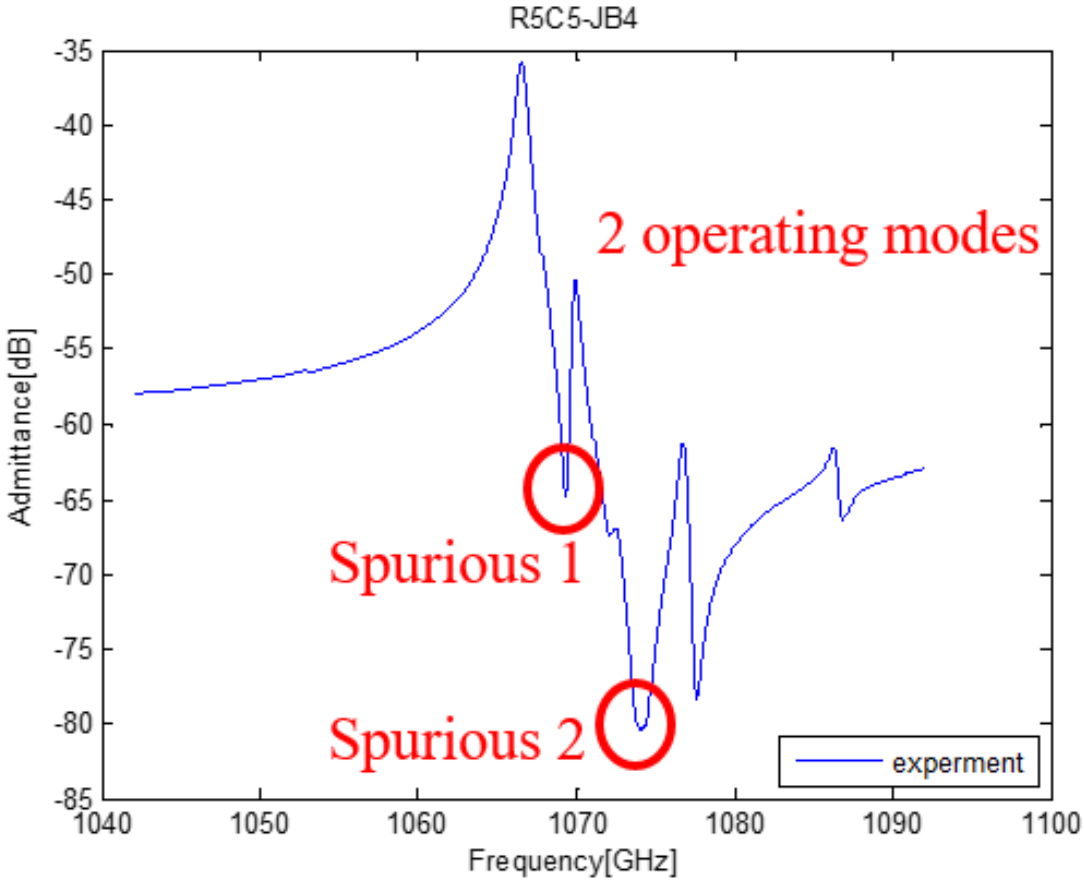



Figure 3.11 Admittance of AlN CMR according to frequency change.

The quality factor (Q) of two modes is also different from each other. That's why the measured phase noise is different even though the same type of Colpitts oscillator is used. Figure 3.12 represents two phase noise when oscillator works at spurious 1 or spurious 2 point. Figure 3.13 shows the result from spectrum analyzer. You can see that there is a tone at around 1GHz. To be

more specific, when the oscillator works at spurious 2, the frequency is 1.071GHz, and 1.068GHz at spurious 1 mode. Table 3.6 shows the phase noise value at each offset frequency in detail.

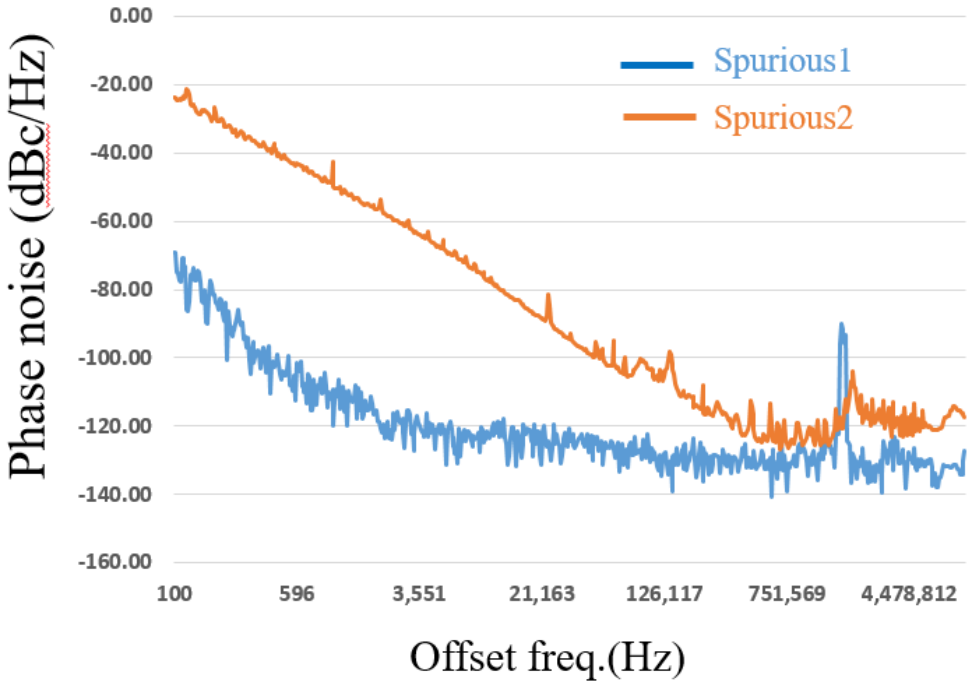



Figure 3.12 Two phase noise performances at different modes

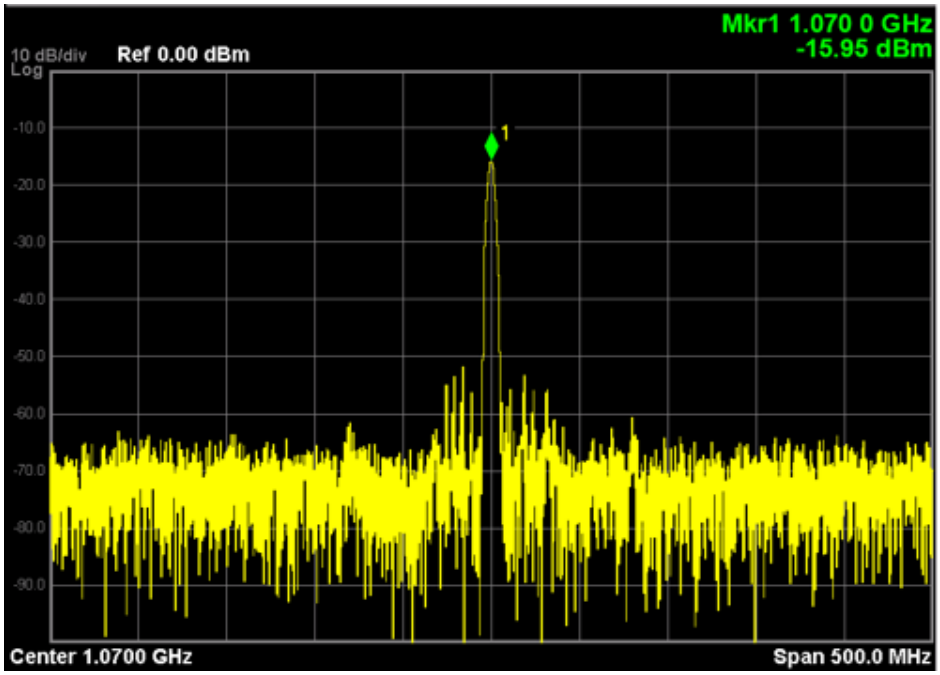



Figure 3.13 Operating frequency measured by frequency analyzer

Table 3.6 Measured phase noise of AlN CMR having two spurious modes

| | **100Hz** | **1kHz** | **10kHz** | **100kHz** | **1MHz** |
|---|---|---|---|---|---|
| **Spurious1 (dBc/Hz)** | -69.5 | -109.5 | -117 | -120.7 | -120 |
| **Spurious2 (dBc/Hz)** | -23.7 | -42.7 | -76.5 | -103 | -123 |

As you can see in Table 3.6, the phase noise performance at spurious 1 is excellent especially at close-in offset frequency. The power consumption is 1.2mW here. To see how this performance is better compared to other works, we need to calculate FOM with information such as operating frequency, phase noise measured, offset frequency and power consumption. The equation is given by

$$FoM = -L(\Delta f) + 20\log\left(\frac{f_O}{\Delta f}\right) - 10\log(P(mW))$$

where $\Delta f$ represents offset frequency where the phase noise is measured and $P$ means the power consumption with the unit of mW. $f_O$ and $L$ show the operating frequency and phase noise value respectively. Table 3.7 shows both mechanical and electrical type oscillators that use either MEMS resonators (ex. FBAR and AlN CMR) or on-chip inductors. The oscillator using recent AlN CMR, especially working at spurious 1 mode, shows the highest FoM.

Table 3.7 Performance comparison

| | $f_{osc}$ (GHz) | Power (mW) | Tech. | 1kHz | 10kHz | 100kHz | 1MHz | FoM |
|---|---|---|---|---|---|---|---|---|
| **AlN CMR Spurious mode** | 1.068 | 1.2 | 65nm | -109.5 | -117 | -120.7 | -120 | **229.2** |
| **[22] AlN CMR** | 1.16 | 4 | 130nm | -82.3 | -113 | -143 | -173 | 228 |
| **[20] FBAR** | 2.4 | 0.66 | 65nm | -61.3 | -87 | -118 | -140 | 209 |
| **[23] FBAR** | 1.55 | 11.3 | 130nm | - | - | - | -144.3 | 197 |
| **[24] LC** | 2.5 | 4 | 65nm | - | - | -100 | -128 | 189.9 |
| **[25] FBAR** | 2 | 0.022 | 180nm | - | - | -121 | -140 | 222 |
| **[26] FBAR** | 0.6 | 5.6 | 130nm | - | -126 | -140 | -150 | 198 |
| **[27] FBAR** | 1.5 | 1 | 350nm | - | -112 | -133 | -147 | 210 |

### *3.5 Tranformer coupled Colpitts Oscillator*

The previous section has depicted the Colpitts oscillator mechanism and also how the performance changes according to frequency selective elements used; this is shown in table 3.7. As you can see, there have been many efforts and researches to decrease phase noise with low cost, especially for close-in offset. That's because close-in phase noise is an important performance metric for a reference oscillator, as it dominates the in-band phase noise of a frequency synthesizer in a radio. Besides using MEMS resonators, there have been many other techniques from the circuit design perspective, wherein a large capacitor was placed parallel to the current source in order to minimize its thermal noise around second harmonic of the oscillation [28]. It is very simple to implement, but, there are trade-off between area due to a huge capacitor and noise filtering.

[29] introduces a technique to reduce AM-PM (amplitude modulation to phase modulation) arising from non-linear device parasitics by using compensation capacitor. However, parasitic capacitance, one of the major factors for AM-PM conversion can vary according to the size of the current source and process variation. It is also dependents on the amplitude of the output signal and current source.

The proposed oscillator therefore removes the current source of the oscillator, which is the main source of the up-converted thermal noise. The current source is necessary for high impedance to stop the differential-pair FETs in triode from loading the resonator in the LC oscillator [28]. It is also helpful for Colpitts oscillator to obtain enough loop gain [20]. The removal of the high impedance current source is compensated by using transformer and cross coupled capacitor to increase the loop gain and kick off the oscillation in this work. The proposed transformer coupled Colpitts oscillator, therefore, utilizes the benefits of conventional oscillator such as class C, D and Colpitts to decrease the close-in phase noise as well as power consumption.

Figure 3.14 shows the detail block diagram with the transformer where the turn ratio between primary and secondary inductor is 2 to 1. There are two reasons to choose 2:1 turn ratio. One is to increase the feedback loop gain to double, and the other reason is to utilize the secondary inductor as a balun. Since the center tap of the secondary inductor is connected to ground, the half of the inductor is used to feed the oscillator output directly to the gate of the Quasi-passive mixer [30]. If the signal across the FBAR resonator is used for an output, buffer is essential which leads to more power consumption added. One of the capacitor ($C_2$) in the feedback loop and one secondary

inductor ($L_{s1}$) constitute LC tank and have high impedance at their resonance frequency equivalent to operating frequency of the oscillator ($w_o$).

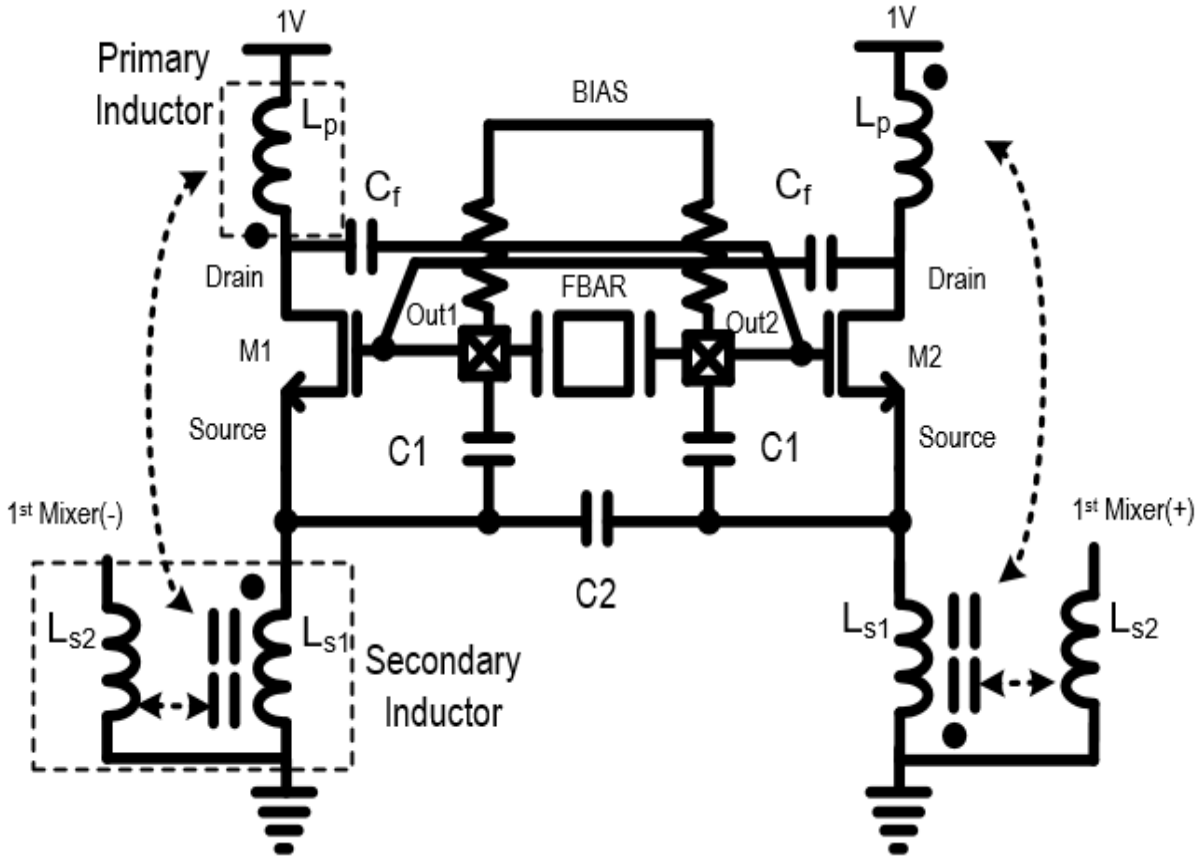
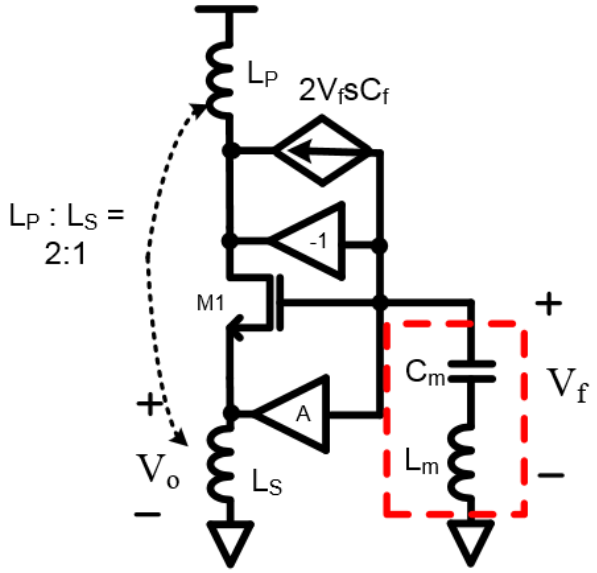



Figure 3.14 Block diagram of the transformer coupled Colpitts oscillator

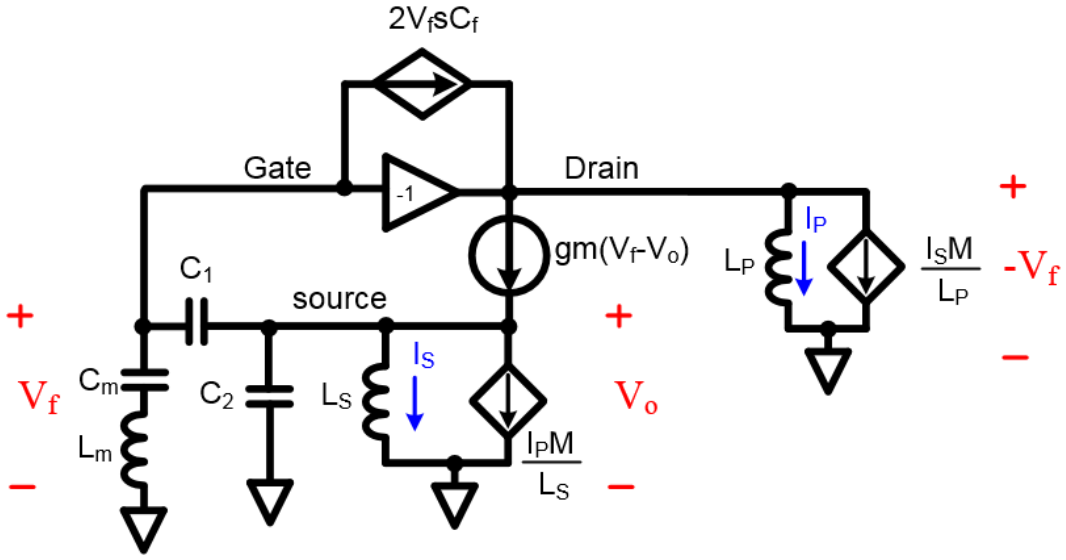
Now, it is essential to derive the minimum transconductance ($g_m$) that is needed for oscillation as shown at the section 3.3 to verify how this structure would be helpful in terms of power consumption. Figure 3.15 shows the single-ended version and its small signal model. *A* represents the capacitive network, $\frac{C_1}{C_1+C_2}$. -1 gain and current source connected in parallel with it show the cross coupled capacitor ($C_f$). Small signal model can be utilized to derive the operating frequency ($f_o$) first.

Applying KCL at gate node, we can have below equation.

$$V_o = \frac{V_f 2C_f}{C_1} + \frac{V_f C_m}{C_1(1 + s^2 L_m C_m)} + V_f$$




(a)




(b)

Figure 3.15 (a) Single-ended block diagram of transformer coupled oscillator and (b) its small signal model

The current flowing through the primary inductor is given by

$$I_P = -\frac{V_f}{sL_P}$$

Applying KCL at source node this time,

$$g_m V_f - g_m V_o = \frac{I_P M}{L_s} + \frac{V_o}{sL_s} + V_o sC_2 + (V_o - V_f)sC_1$$

If $I_P$ and $V_o$ are replaced by the first two equations above and re-arrange, the imaginary part is given by

$$Im[T(f)] = g_m 2C_f L_P L_S (1 + s^2 L_m C_m) + g_m L_P L_S = 0$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{C_m L_m}\left(\frac{2C_f + C_m}{2C_f}\right)}$$

Now, we can utilize Figure 3.15 to derive the necessary $g_m$ by applying test voltage to the gate and calculate the current coming out from it.

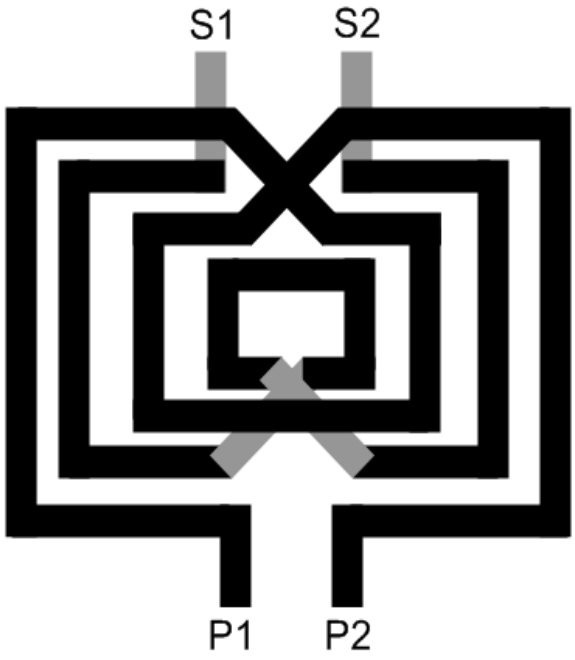
$$g_m = \frac{1}{R_p}\frac{2C_2 + 2C_1}{3C_2 + C_1}\frac{L_s}{L_s + M} \approx \frac{1}{R_p}\frac{2}{3}\frac{L_s}{L_s + M}$$

As shown in the above equation, the required $g_m$ is less than that of Colpitts oscillator. Since we figured out that transformer coupled Colpitts oscillator has benefits in terms of power consumption and 1/f noise conversion, it is time to dig into more detail how to implement the circuits. The following section will describe how to design transformer which is the key passive component.

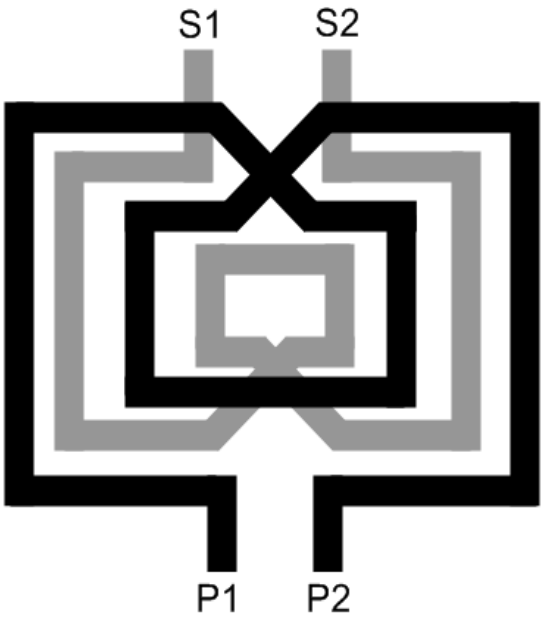
### *3.6 Transformer design*

The TSMC p-cell libraries offer a variety of passives, including inductors, capacitors and diodes. However, it does not have transformers. Therefore, it should be custom-made. The key parameters

to design for are self-inductance (L), quality factor (Q), and the coupling coefficient (k) given area constraints. Maximizing k results in higher effective inductance per area and reduces signal loss when magnetically coupled from the primary to the secondary coil [31]. There are two main transformer topologies: planar and stacked structure as shown in Figure 3.16.




(a)




(b)

Figure 3.16 (a) Planar and (b) stacked transformer structure

Planar structure where both the primary and secondary coils are drawn on the same metal layer, has medium Q, k, but large area. Conversely, stacked structure consisted of two metal layers, exhibits high k, L, but low Q as specified at table 3.7.

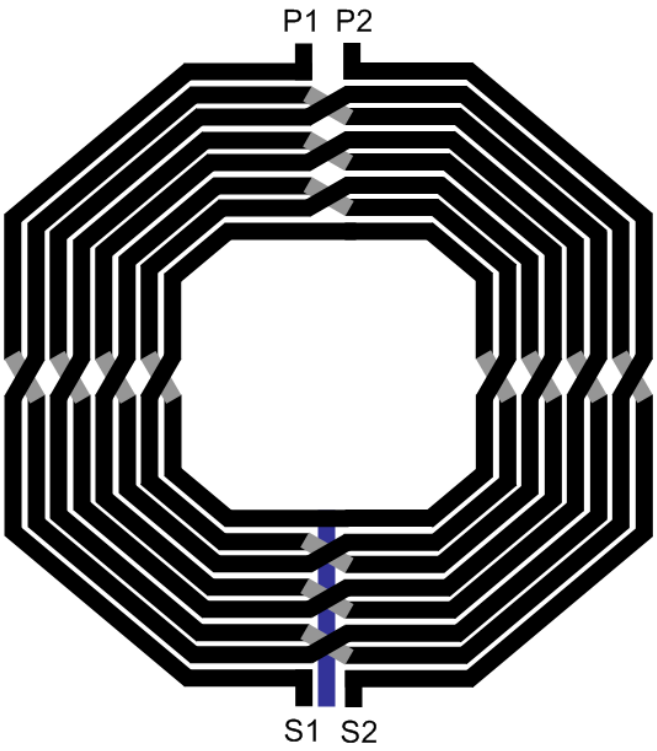
Table 3.8 Transformer topology and each characteristic.

| | **L** | **Q** | **k** | **Area** |
|---|---|---|---|---|
| **Stacked** | High | Low | High | Low |
| **Planar** | med | med | med | High |

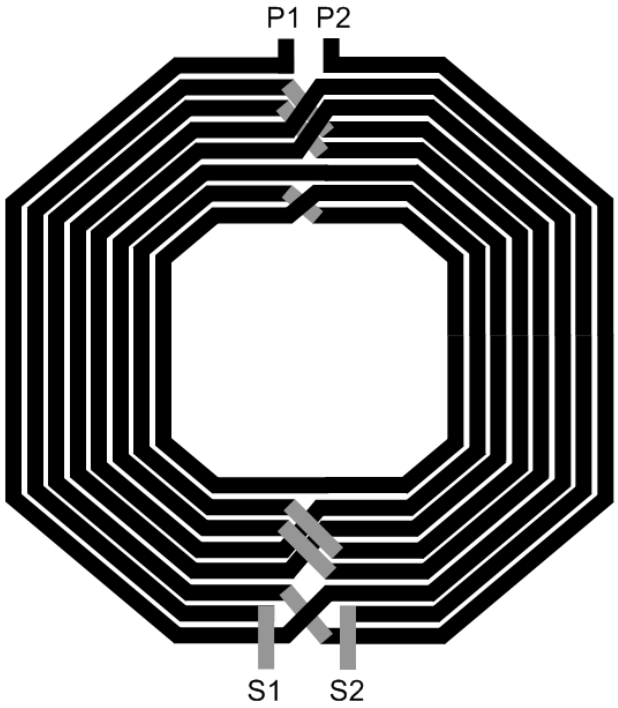
Based on the oscillator design, Q is a critical parameter for achieving low phase noise and lower power consumption. In TSMC library options, there is only one thick metal layer (M9) with low sheet resistance (0.005 Ω/sq). The next thickest metals (M8) has 4× higher sheet resistance, resulting in 4× lower Q. That's why the planar structure is used for this oscillator design.

As shown in Figure 3.16 (a), planar structure almost comprises of Metal 9 (Black line). Metal 8 (Gray line) is only used for intersaction part. However, the stacked transformer, Figure 3.16 (b) uses Metal 8 for secondary inductor, which leads to higher resistance and lower Q.

Figure 3.17 (a) shows the real transformer layout used for Bluetooth 4.1 application (BLE) and (b) is for 1GHz AlN CMR application. For Bluetooth application, the operating frequency of the oscillator is 2GHz, so the target inductances for both primary and secondary inductor can be achieved with smaller diameter and hence smaller area compared to 1GHz oscillator using AlN CMR. As the length of the inductor path is smaller, it is relatively easy to obtain the Q factor of 10 because the resistance in the coil is smaller than that of the 1GHz transformer. However, the transformer for AlN CMR is aimed for 1GHz operation. The length and its diameter should be drawn much larger which results in higher resistance and lower Q. The lower the Q, the higher the power consumption is necessary for the oscillator to start up. To maximize the Q, the width of the path of the inductor is doubled. Table 3.9 summarizes each transformer geometrics.




(a)




(b)

Figure 3.17 Transformer layout for (a) 2GHz BLE application and (b) 1GHz AlN CMR device

Table 3.9 Transformer geometry for BLE and AlN CMR

| | # of turn | Width (um) | Spacing (um) | Diameter (um) | Q | $L_{eff}$ (Primary) | $L_{eff}$ (secondary) |
|---|---|---|---|---|---|---|---|
| **BLE (2GHz)** | 8 | 5 | 2 | 140 | 10 | 6nH | 1.74nH |
| **AlN CMR (1GHz)** | 8 | 10 | 2 | 175 | 11 | 6.7nH | 3.4nH |

As shown in the table above, transformer for 1GHz AlN CMR requires larger diameter and wider width for maximizing the quality factor (Q).

## *3.7 Transformer design verification*

To gain an intuitive understanding of the transformer coupled oscillator and to run transient simulations, an electrical circuit model needs to be build up by using the S-parameter information from Advanced Design System (ADS) tool. We used a relatively simple but sufficiently accurate model as shown in Fig. 3.18. This model accounts for the coupling among different inductor sections, resistive loss, parasitic capacitance and substrate loss. The effect of inter-turn fringing capacitance is usually small because the adjacent turns are almost equipotential and therefore is neglected in our model [32]. The transformer for BLE application is already fabricated and tested to extract Q, inductance and k to verify if the electrical circuit model shown in Figure 3.18 is correct. For the exact comparison between test result and simulation, the de-embedding process needs to be performed. When the transformer is analyzed through the test, the test result contains any undesirable information caused by parasitic capacitors and resistors. Those components can come from either test cable or parasitic capacitance of the test PADs. The de-embedding technique removes this information from the test result to extract the characteristic of only the transformer. The standard de-embedding technique of Short-Open-Load calibration is used. Its procedure is as follows [33]:

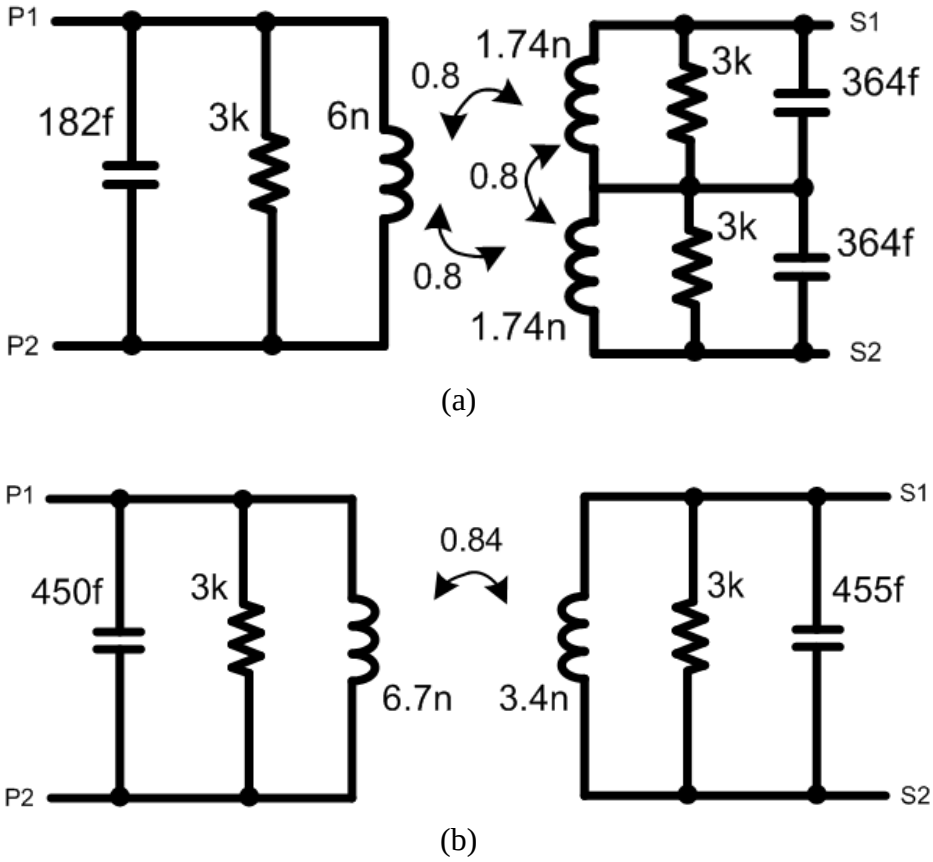



Figure 3.18 Electrical model of the transformer for (a) BLE application and (b) AlN CMR

1. DUT: S-to-Y ($Y_{DUT}$)
2. Open calibration: S-to-Y ($Y_O$)
3. $Y_{cor} = Y_{DUT} - Y_O$, Y-to-Z ($Z_{cor}$)
4. Short calibration: S-to-Y (Ys)
5. $Y_{scor} = Y_S - Y_O$, Y-to-Z ($Z_{scor}$)
6. $Z_{meas} = Z_{cor} - Z_{scor}$
7. $Z_{meas}$ to $S_{meas}$

Figure 3.19 shows the test structure for the de-embedding process. It does not contain a transformer core, but only a ground plane and Pads. Figure 3.20 graphically depicts how to implement process.

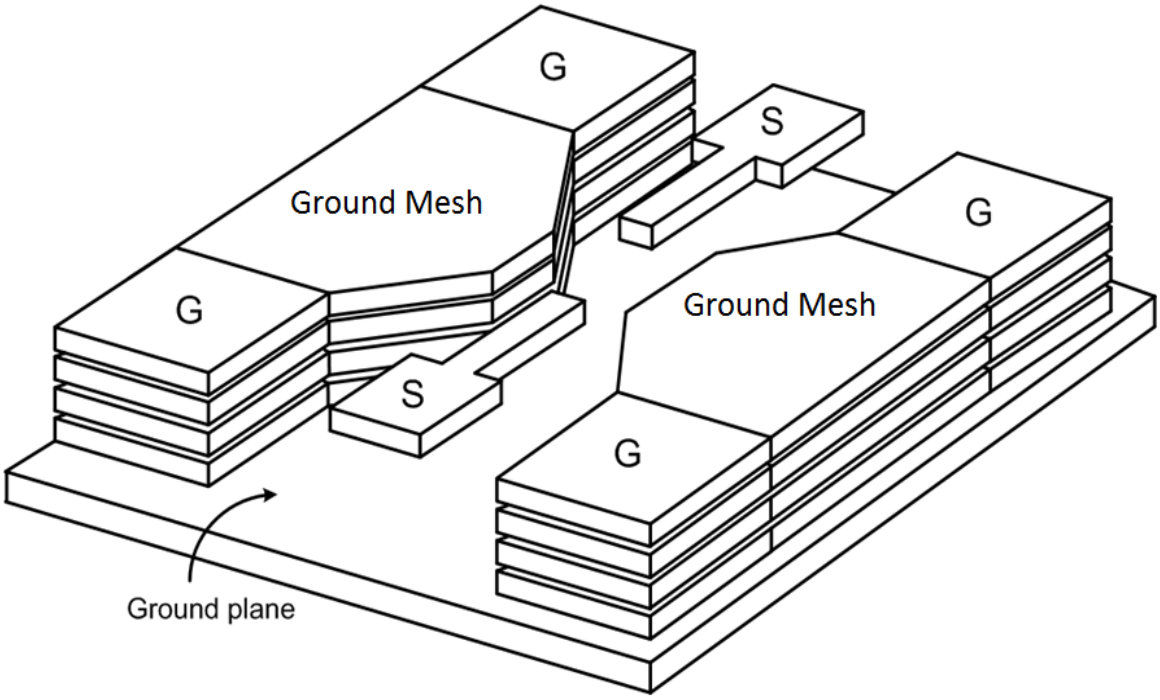



Figure 3.19 Test structure for extracting parasitic components from ground plane and test Pads.

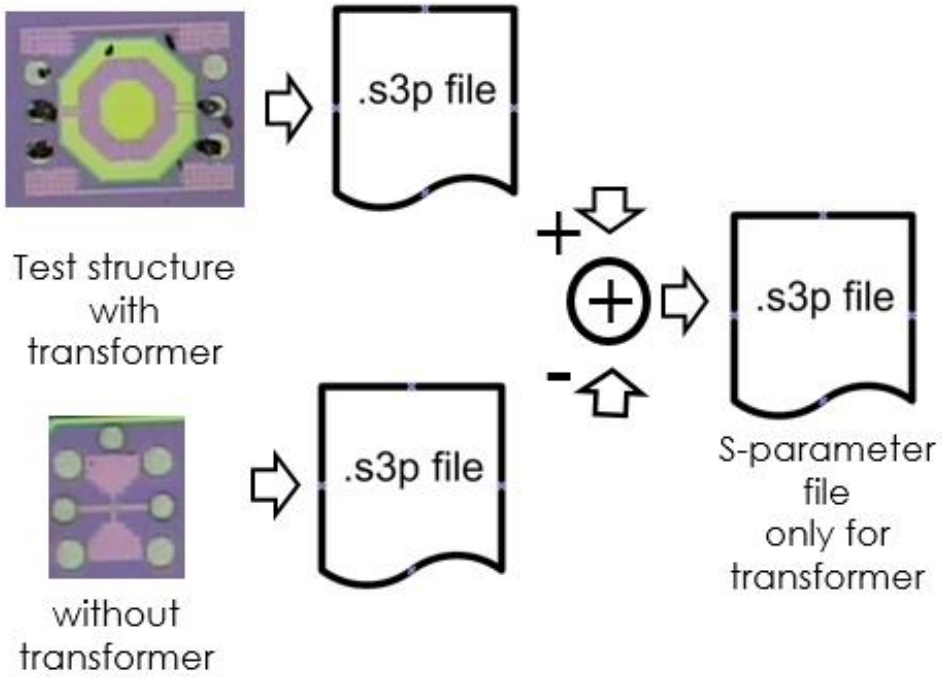
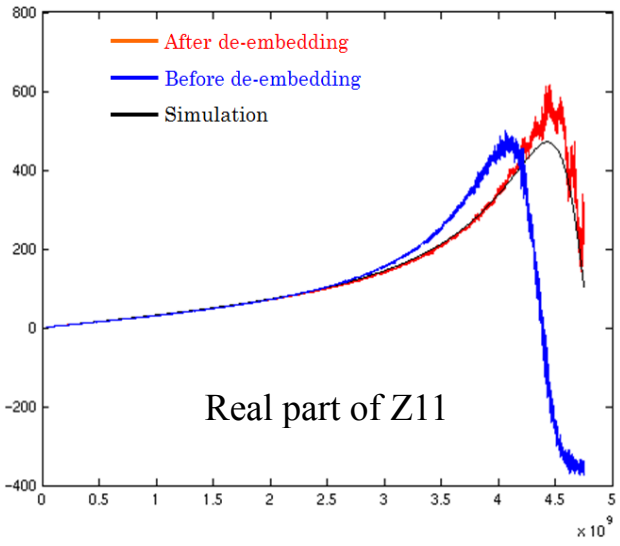



Figure 3.20 De-embedding process to extract transformer characteristic

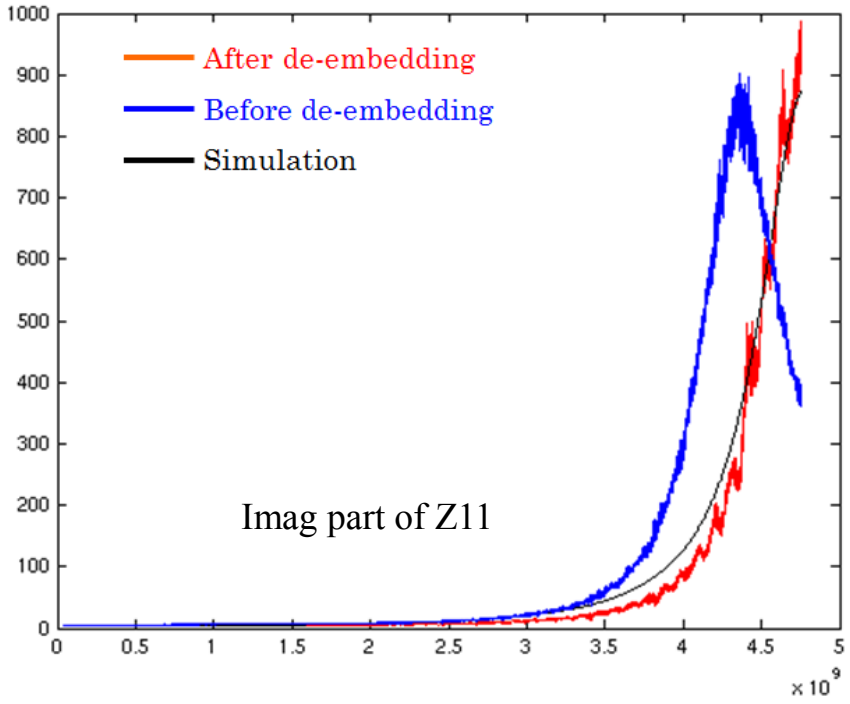
There are two test structures to be measured as shown in Figure 3.20. One is in the bottom of the figure that does not have any transformer core, but only Pads and a ground plane. It contains information related to all parasitic components. The other test structure has a transformer core inside. The S-parameter file from that test structure contains both the transformer core and parasitic information. With post processing such as subtracting S-parameter of the empty test structure from that of another structure having a transformer core, we can obtain an exact characteristic for transformer. With these files, we can tune the value of the electrical model that matches with the test result.

Figure 3.21 (a) shows the test result before and after the de-embedding process. It represents the real part of Z11 of the primary inductor. The blue graph represents the situation before the de-embedding process is applied. After all parasitic components are removed, we can see that the peak value of the blue graph moves to a higher frequency as it is marked by the red graph. With this information, each value in electrical model shown in Figure 3.18 can be tuned to have same result. Further, the black graph shows the simulation result with electrical model of the transformer, and you can see that it matches the test result.

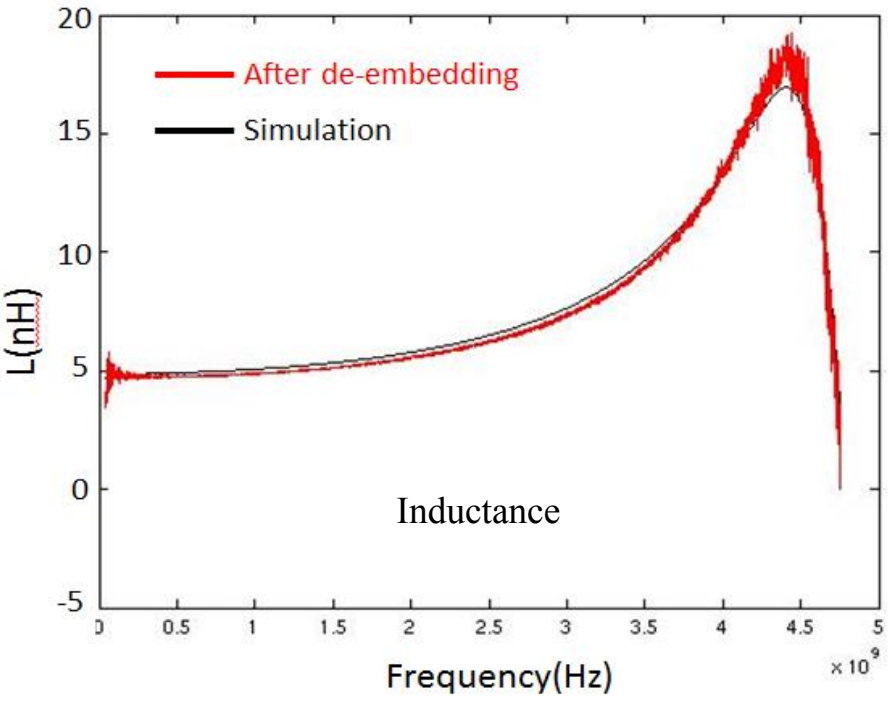
Figure 3.21 (b) represents the imaginary part of Z11 from the same inductor in the transformer. Simulation result from the electrical model is equal to the test result after de-embedding process at the interest frequency, 2GHz. Figure 3.21 (c) shows how the inductance varies according to frequency change. Figure 3.21 (d) represents the coupling coefficient between primary and secondary inductor. Although the test result and electrical model has difference of 0.1, 0.8 for



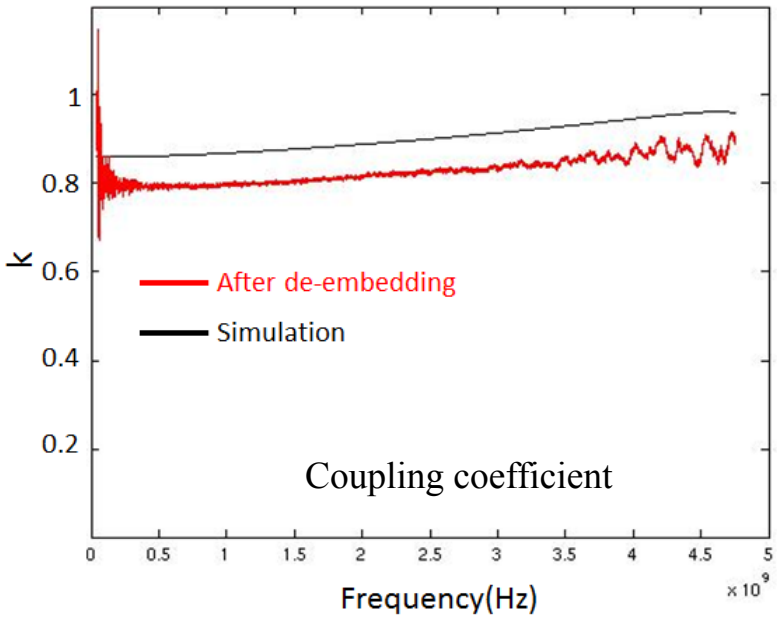

(a)


After de-embedding
Before de-embedding
Simulation
Imag part of Z11
1000
900
800
700
600
500
400
300
200
100
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
x 10^9

(b)


After de-embedding
Simulation
Inductance
L(nH)
20
15
10
5
0
-5
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
x 10^9
Frequency(Hz)

(c)




(d)

Figure 3.21 Test result with/without de-embedding process for (a) real and (b) imaginary part of Z11, (c) inductance and (d) coupling coefficient for transformer with simulation result of electrical model

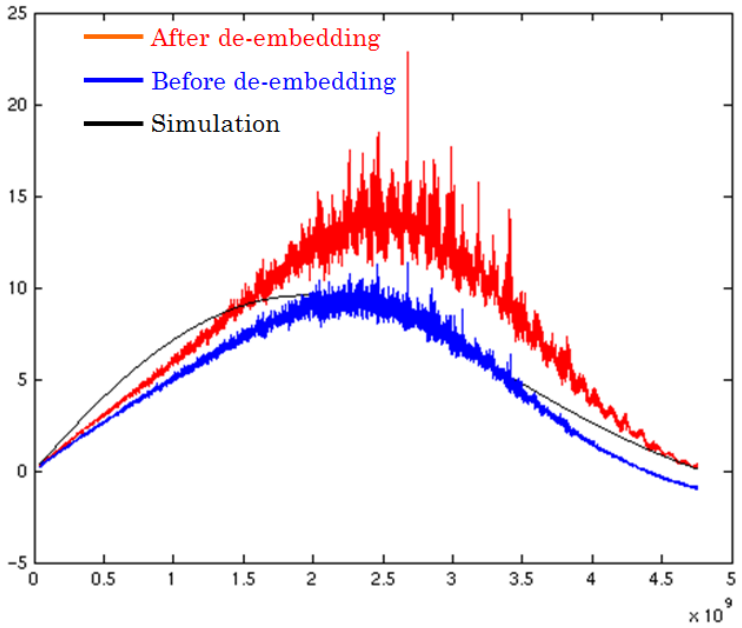



Figure 3.22 Quality factor (Q) of primary inductor

coupling coefficient in the real transformer is high enough to get loop gain to oscillate. With those S-parameters, quality factor (Q) for the primary inductor can be obtained as shown in Figure 3.22. For this plot, equation, $\frac{real(Z11)}{imaginary(Z11)}$, is used. As all parasitic components are removed, the real quality factor of the primary inductor is increased by around 3. Although the peak of the electrical model is moved down to lower frequency a little bit, it does affect little when the oscillator is optimized to interest frequency, 2GHz.

## *3.8 Test result of the transformer coupled Colpitts oscillator*

The technique for designing a transformer with the test result convinces that the circuit model of the transformer is accurate and good to use, and also verifies that the chosen method of designing the transformer is correct. With this model, oscillator is fabricated by using 65nm TSMC technology. Figure 3.23 shows the die photo with 2GHz FBAR device. The transformer coupled Colpitts oscillator has a dimension of 900um by 400um. As you can see, most of the area is taken by the transformer. The power supply used for oscillation is 1V. The oscillator can start at 200uW power consumption but 350uW is needed to have a large amplitude enough to measure the phase noise. Figure 3.24 shows the frequency spectrum result that there is a tone at 2GHz. When the phase noise is measured, -20dBm output amplitude is used.

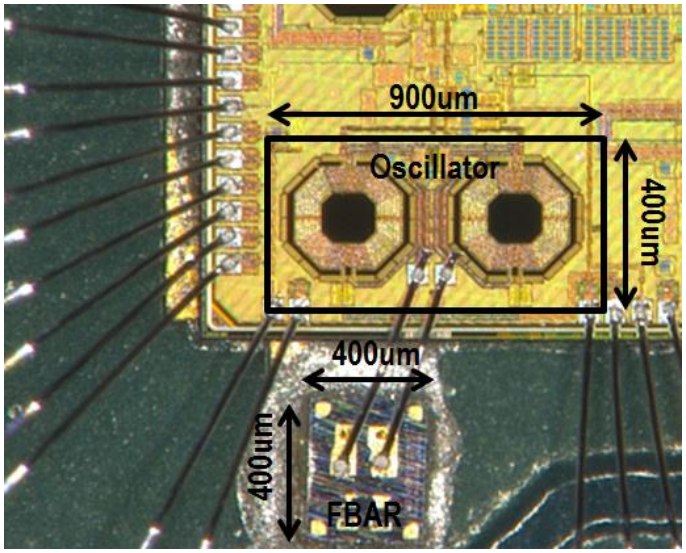



Figure 3.23 Die photo of the transformer coupled Colpitts oscillator with 2GHz FBAR

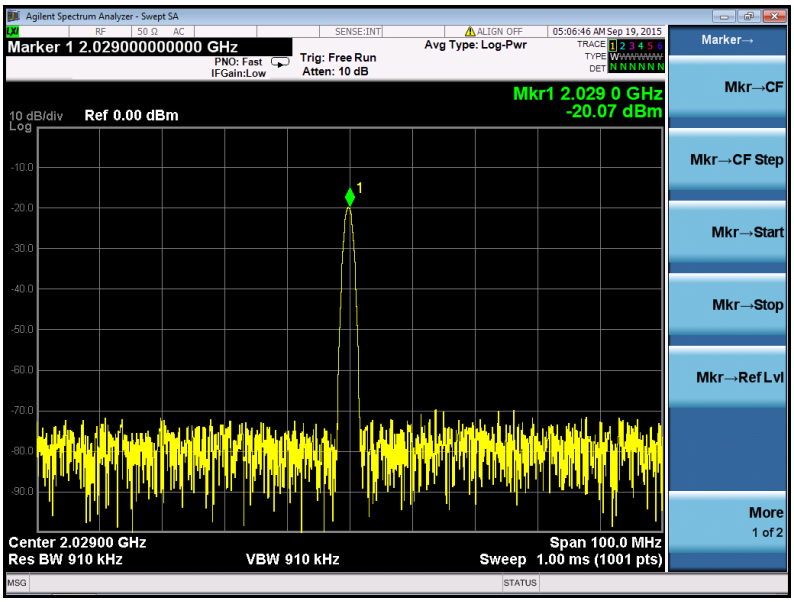



Figure 3.24 Test result from frequency spectrum analyzer

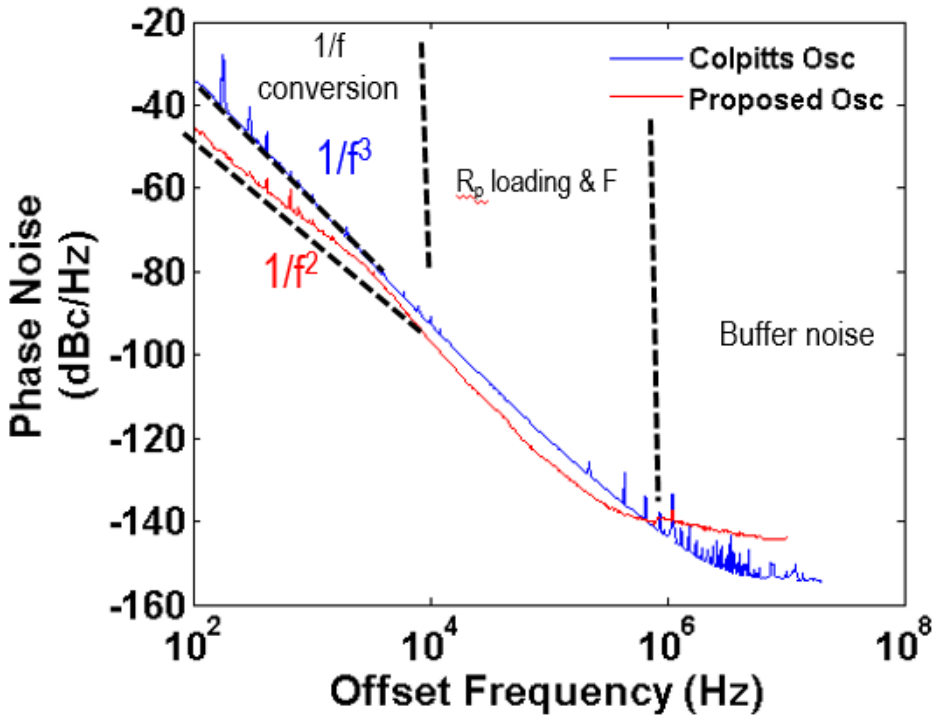



Figure 3.25 Measured phase noise performance with Colpitts oscillator

Figure 3.25 shows the measured phase noise. The phase noise measured from conventional Colpitts oscillator is used in the same plot for the purpose of comparison. You can see that the overall phase noise is improved. More specifically, at the close-in offset frequency, the slope decreases from $1/f^3$ to $1/f^2$.

Based on the noise profile of the oscillator that uses the MEMS resonator, the close-in phase noise up to 10kHz offset frequency is mainly dominated by 1/f noise conversion. The parallel impedance of the MEMS resonator ($R_p$) and oscillator's noise factor *F* affects up to 1MHz offset frequency. Noise factor expressed by the below equation has three noise contributions, the tank resistance, the active devices and the current source respectively.

$$F = 1 + \frac{4\gamma IR}{\pi V_O} + \gamma \frac{4}{9} g_{m,bias} R$$

Since active devices should be used for generating the equivalent negative resistance needed to sustain a steady-state oscillation, the first two terms are inevitable. However, the proposed oscillator does not use the current source, so the minimum noise factor is obtained. As a result, the phase noise up to 1MHz offset frequency has improved more than 10dB. There is a little hump in the middle offset frequency. That is contributed by the off-chip voltage regulator for power supply and bias voltage. When the power supply was directly connected for $V_{DD}$ and bias, there was larger hump. But, it is decreased when they are passed through the voltage regulator. It means that this hump is from off-chip regulator, not from the oscillator itself.

The phase noise at higher than 1MHz offset frequency is larger than the conventional Colpitts oscillator. The far out offset frequency is mainly contributed by either output amplitude or noise from output buffer. When I taped out the conventional Colpitts oscillator, I had enough area to use to put another same oscillator for test purpose and only one open drain buffer was used. The output amplitude of it was around -9dBm. But, for the recent tape out, the transformer coupled oscillator was used for BLE receiver system. As there was insufficient area to put one more oscillator, the output was pulled out from the system through buffer chain. Those harsh test environment contributes to higher phase noise at a far out offset frequency.

To clarify the phase noise improvement at close-in offset frequency, $V_{DD}$ of the oscillator is changed. Figure 3.26 shows how the phase noise changes when $V_{DD}$ varies from 1V to 0.65V. The amplitude of the output signal changes proportionally to the $V_{DD}$ value in general. That's why phase noise at 10MHz offset improves as $V_{DD}$ increases. However, close-in phase noise is consistent no matter what $V_{DD}$ value is. Figure 3.27 represents the same in detail.

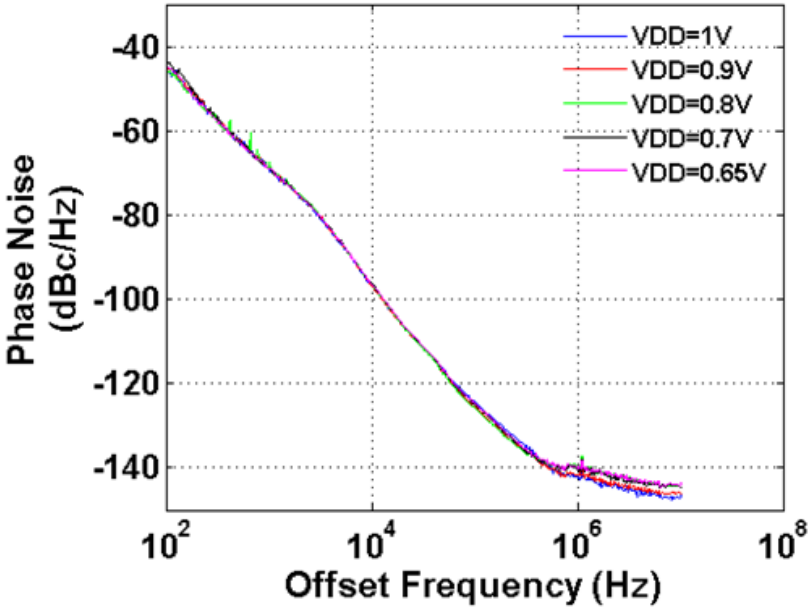



Figure 3.26 Phase noise plot with $V_{DD}$ change

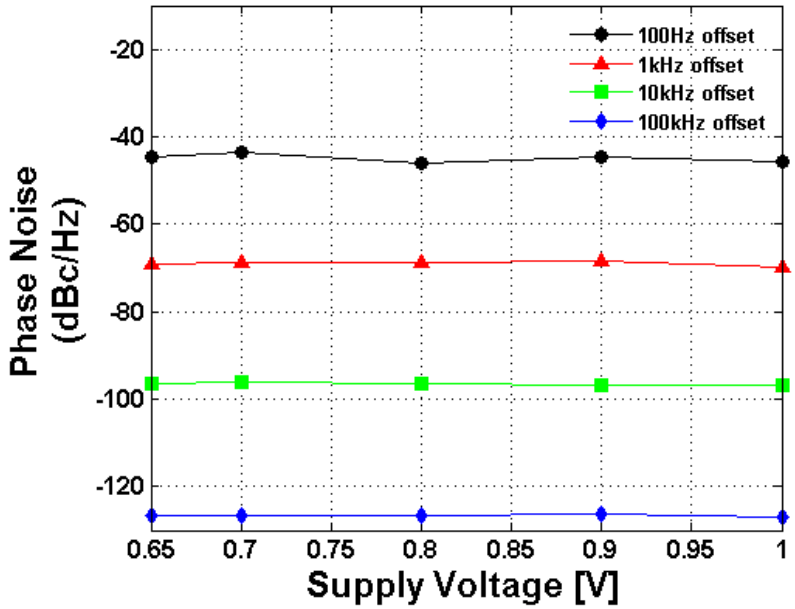



Figure 3.27 Phase noise at close-in offset frequency with variable $V_{DD}$

The performance of this work is compared with other previously published oscillators mainly in terms of close-in phase noise, power consumption and operating frequency as shown in table 3.10. The Figure of Merit (FOM) is computed at 100kHz offset. This structure achieves an FOM of 217dB with the low power consumption of 350uW. For the fair comparison, FBAR based oscillators were compared. Figure 3.28 represents how the FOM of this oscillator changes according to $V_{DD}$ variation. As already shown in Figure 3.27 that phase noise is constant, FOM is also constant.

Table 3.10 Performance summary of transformer coupled Colpitts oscillator and comparison table

| | $f_{osc}$ (GHz) | Power (mW) | Tech. | Phase nosie @ 1kHz (dBc/Hz) | Phase nosie @ 10kHz (dBc/Hz) | Phase nosie @ 100kHz (dBc/Hz) | FOM |
|---|---|---|---|---|---|---|---|
| **This work** | 2 | 0.35 | 65nm CMOS FBAR | -68.6 | -96.4 | -127 | **217** |
| **[20] Colpitts** | 2.4 | 0.66 | 65nm CMOS FBAR | -61 | -87.6 | -118 | 207 |
| **[19] Class-D VCO** | 2.5 | 4 | 65nm CMOS LC | - | - | -100 | 189.9 |
| **[34]** | 1.7 | 4.9 | Bipolar FBAR | -81.3 | -107.8 | -130 | 207 |
| **[23]** | 1.55 | 11.3 | 0.13um CMOS FBAR | -56 | -86 | -116 | 198 |

$$(FOM = -L(\Delta f) + 20\log\left(\frac{f_O}{\Delta f}\right) - 10\log P(mW))$$

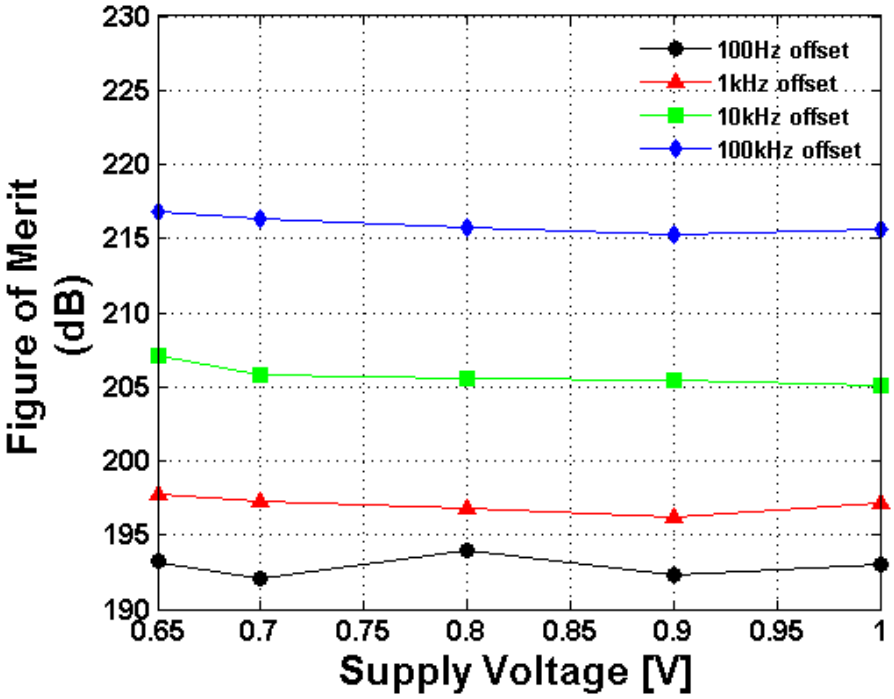



Figure 3.28 Figure of merit plot according to $V_{DD}$ change

# Chapter 4

# OVEN CONTROLLED TEMPERATURE COMPENSATION SYSTEM

## *4.1 Introduction*

As discussed in chapter 1, various wireless radio systems require a reference clock to achieve a high short term frequency stability. MEMS resonator based oscillators have shown superiority not only in phase noise performance, but also in cost/size compared to quartz crystal and on-chip frequency selective elements. However, as shown in table 4.1, FBAR based oscillator shows ±100ppm frequency drift over temperature change. This characteristic does not fit most wireless applications such as Wi-Fi, Bluetooth and WLAN. These systems require a stability lower than ±20 ppm. Even GPS requires more stringent specification ( < 2ppm ) for a wide temperature range (-40 to 110$^{o}$C for industrial and -10 to 70$^{o}$C for commercial applications). The state of the art radio architecture uses a temperature compensated resonator (ZDR) [20][35], but the stability still does not meet the requirement for GPS.

The oven-controlled crystal oscillator (OCXO) shows superior stability satisfying all wireless application requirements. But, we have to abandon all other benefits that have been discussed so far if crystal is chosen. In the light of this, the current thesis still insists on using the MEMS resonator based oscillator. The solution proposed is to both heat and monitor the resonator temperature at the same time. To make this possible, the oven-controlled temperature compensation system consists of a temperature-to-digital converter (TDC), digitally implemented integrator with 2$^{nd}$ order mesh type sigma delta modulator and current steering DAC. This system shows ±1.6ppm frequency stability over the 85$^{o}$C temperature range. This achievement can be achieved using a fully integrated heater and a sensor in a single chip allowing the design of miniaturized system. This had been an issue in the previous work [36]. Thus, high short term frequency stability as well as low frequency drift over temperature can be achieved simultaneously.

Table 4.1 Oscillator types and their frequency stabilities over the temperature change

| Osc. technology | Frequency stability (ppm) |
|---|---|
| **Ring osc.** | ±15000 |
| **LC osc.** | ±2000 |
| **FBAR osc.** | ±100 |
| **XTAL osc.** | ±20 |
| **OCXO** | 1~2 |

*4.2 Temperature compensated current source in Colpitts oscillator*

Before moving forward to the oven controlled temperature compensation system, we need to investigate how much the oscillator itself contributes to the frequency drift. It is already well known that resonator is the dominant source for the frequency drift. But it is also important to know how much CMOS circuit contributes to instability, and if there is a solution. That is because the heater does not stabilize the temperature of the oscillator, and it is essential to achieve less than 1 ppm stability in the future.

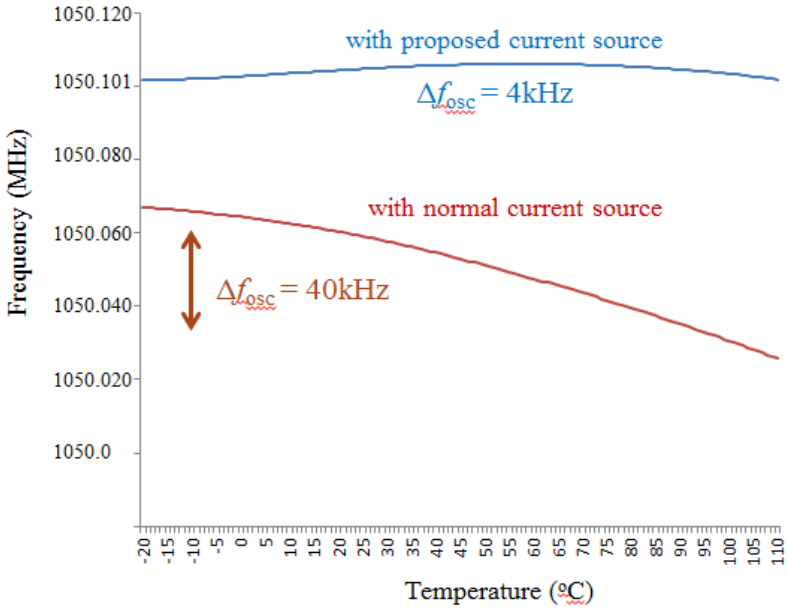



Figure 4.1 simulation result for resonance frequency drift with/without temperature compensated current source technique

Figure 4.1 shows the simulation result for frequency drift of the Colpitts oscillator with normal current source and temperature compensation technique. The ideal resonator which has no temperature dependency are used, which reveals the inherent frequency drift arising due to CMOS circuits.

To reduce the drift arising from CMOS, we must design a current source that compensates for the temperature drift of the oscillator. The addition-based current source is a good candidate to stabilize the oscillator frequency variation arising from the CMOS temperature coefficient [37]. Although its target is to compensate the bias current variation caused by process variation, we can modify the structure to allow a temperature compensation. The proposed technique allows us to tune the temperature coefficient of the current reference to cancel any residual frequency drift. Figure 4.2 is a block diagram of this technique with current source to compensate the frequency variation.

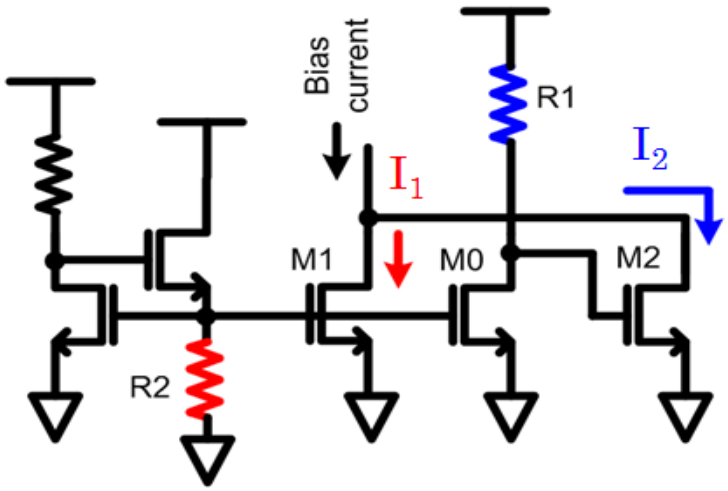
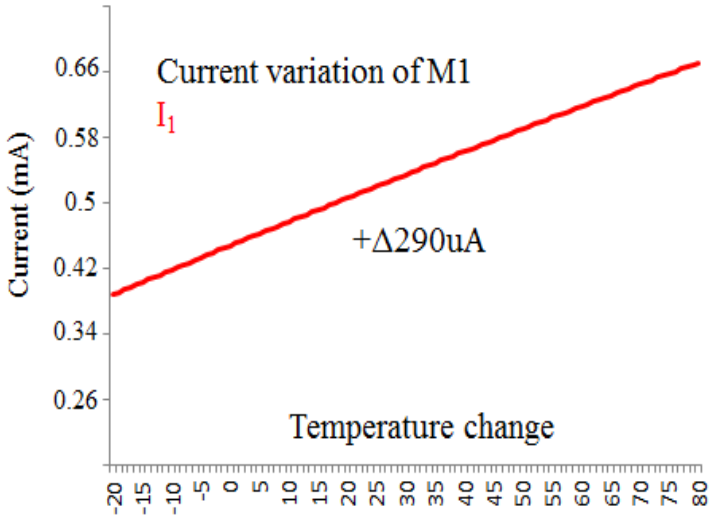
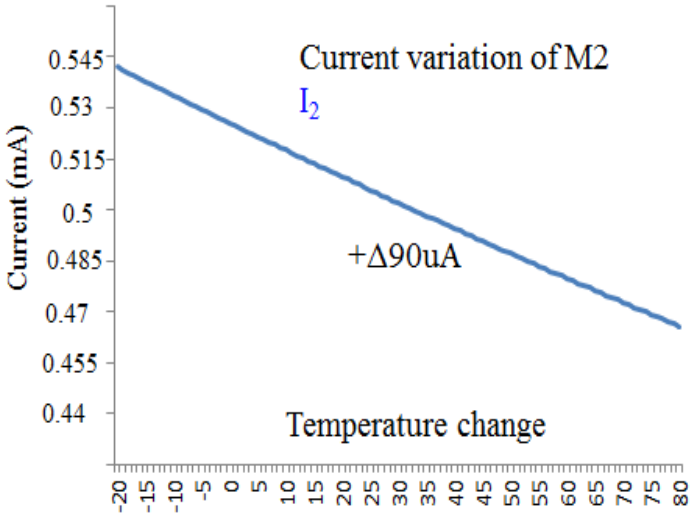



Figure 4.2 Temperature compensated current source

The two poly bias resistors (R1 and R2) are identical in value and layout. The resistance variation dominates the temperature coefficient of the current reference. The resistors have a positive temperature coefficient, leading to a decrease in the current in M2 as the temperature increases. Conversely, the current through M1 increases, allowing cancellation and tuning of the current temperature coefficient. Figure 4.3 depicts these behaviors. The overall simulated frequency drift of the oscillator, assuming the resonator temperature is completely stabilized and current source has zero temperature coefficient, is 40 kHz. With this proposed current source having total bias current with a positive temperature coefficient, the oscillation frequency variation is decreased to less than 4 kHz.




(a)




(b)

Figure 4.3 the current variation of (a) M1 and (b) M2 under the temperature change.

To verify this effectiveness, a test bench is set up as shown in Figure 4.4. As the temperature is swept from 0 $^{o}$C to 80 $^{o}$C, the total frequency change is -1777 ppm which is equal to -22ppm/$^{o}$C when the temperature compensating function is off. But, when the modified current source is on, the total frequency variation is decreased by 25 kHz over the whole temperature range, which means the frequency variation caused by oscillator decreases. Of course, the temperature variation due to the resonator remains same. Figure 4.5 shows the test result of a current variation with and without this current source, demonstrating the ability to tune the current temperature coefficient.

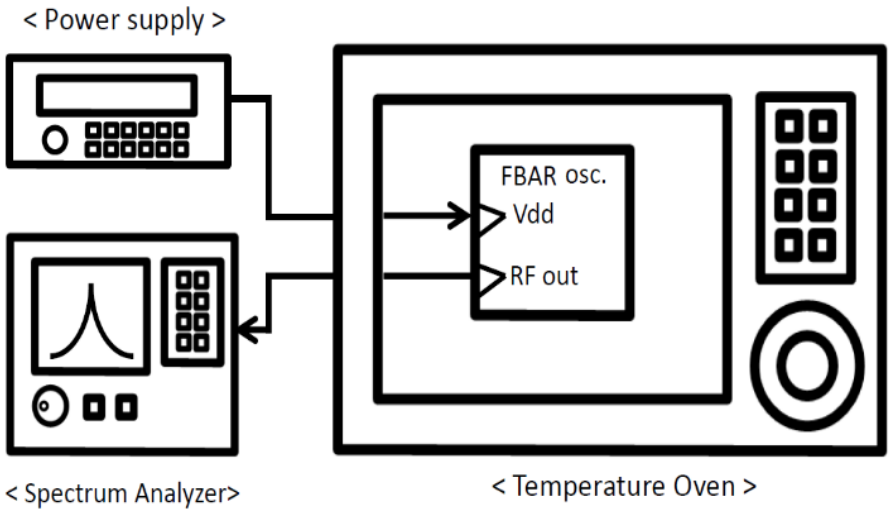



Figure 4.4 Block diagram for test bench

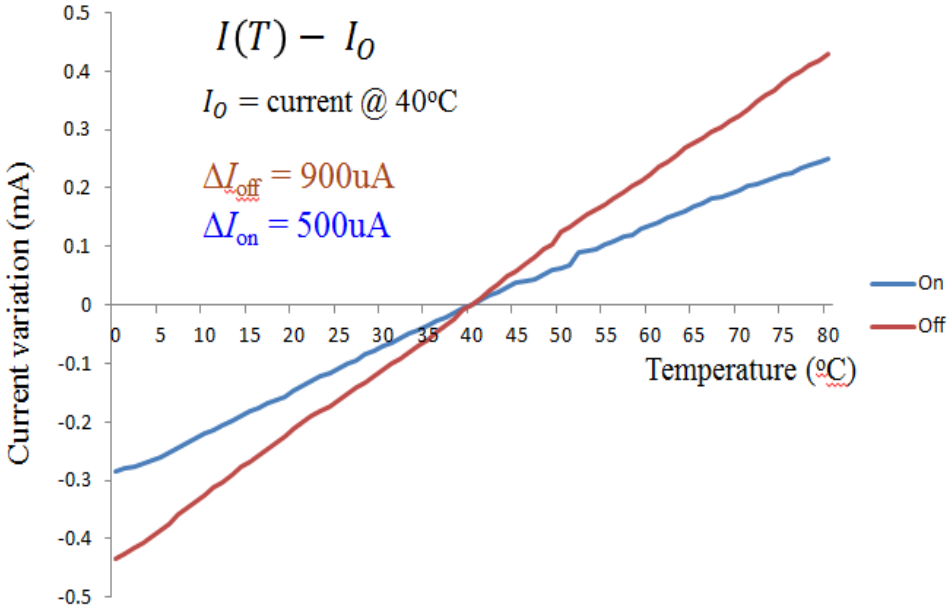



Figure 4.5 Test result with temperature compensated bias circuit.

### *4.3 Heater and Sensor*

To implement the on-chip oven controlled temperature compensated system, the two essential factors are heater and sensor. Figure 4.6 shows how FBAR has a sensor and a heater integrated in the same chip with piezoelectric material. The sensor is fabricated next to top electrodes, otherwise

the heater is deployed beneath the AlN layer, which minimizes the heat loss through air convection. The resistance of heater is 100ohm with a 2kohm sensor. Since the heater resistance is small, more current is needed to generate the same amount of heat compared to the AlN CMR heater which has higher resistance.

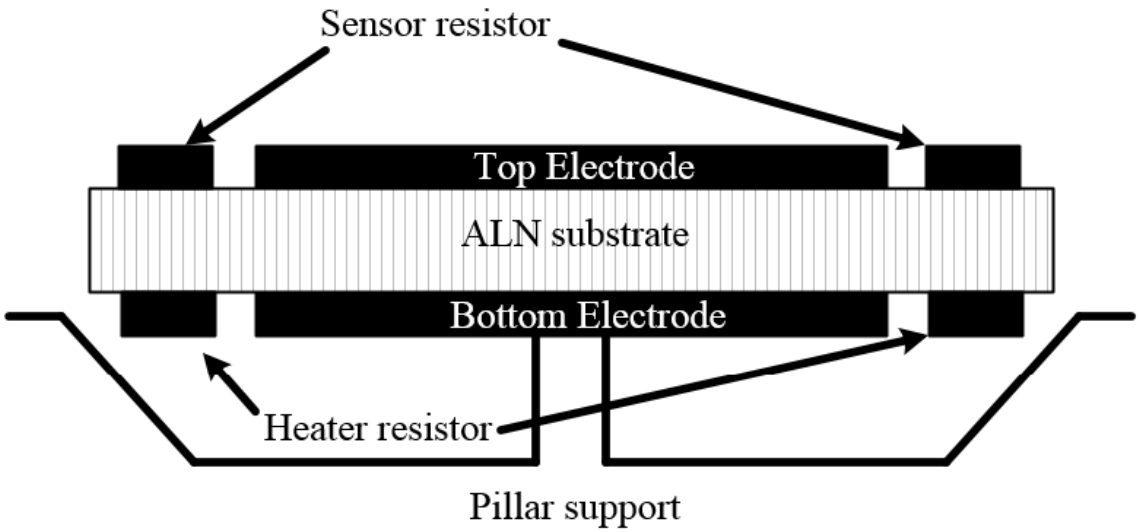



Figure 4.6 Block diagram of the FBAR with sensor and heater

In the case of AlN CMR device, as shown at Figure 4.7, the heater and sensor are integrated at the side of the resonator. Here the heater resistance is 1.2kohm. Although this high resistance helps to generate the same amount of heat with smaller current, the voltage drop across the heater limits the maximum current which current steering DAC can produce.

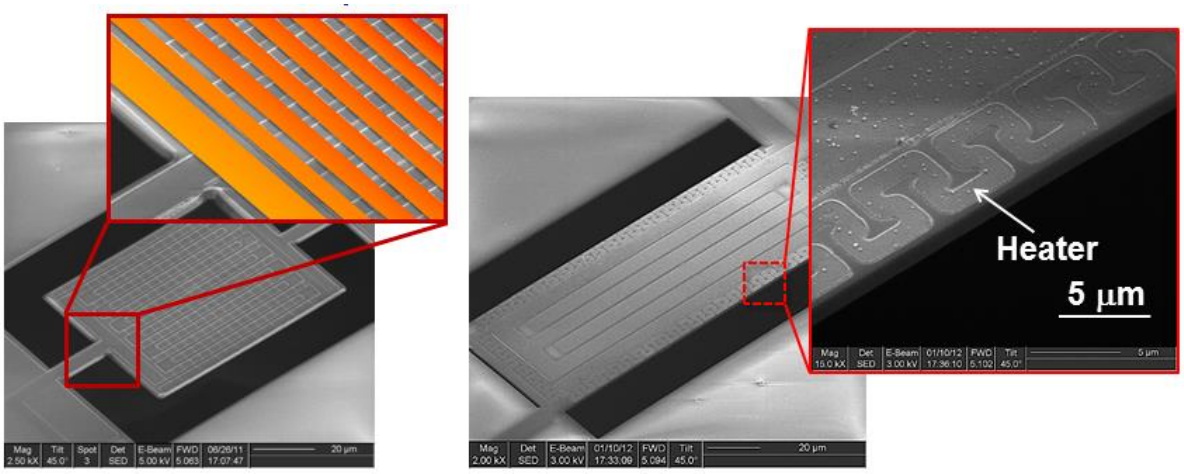



Figure 4.7 SEM photo for sensor and heater for AlN CMR

*4.4 Conventional temperature compensation system*

Before going over the oven controlled temperature compensation system, we need to see other works and check how to approach the lower frequency drift of the reference clock. There are two methodologies we can utilize. One is controlling the capacitor load of the oscillator. Figure 4.8 shows the impedance change of an FBAR device across frequency. As already mentioned in section 2.2, the oscillator should be operating either at parallel frequency or at series frequency in order to utilize its high quality factor (Q) at these two points. In this work, oscillator is optimized to operate at parallel frequency. In reality, however, the operating frequency is decreased from the ideal point due to capacitive loading. Therefore, the operating frequency can be controlled if we can have a capacitive array and control them.

Figure 4.9 shows the feedforward type architecture utilizing capacitive loading effect [38]. The temperature sensor detects the impedance variation according to the temperature change and converts to a digital value. As the FBAR device has a quadratic term in the frequency drift curve, polynomial generation block is needed to control the capacitor to quash down the quadratic curve as shown in Figure 4.8.

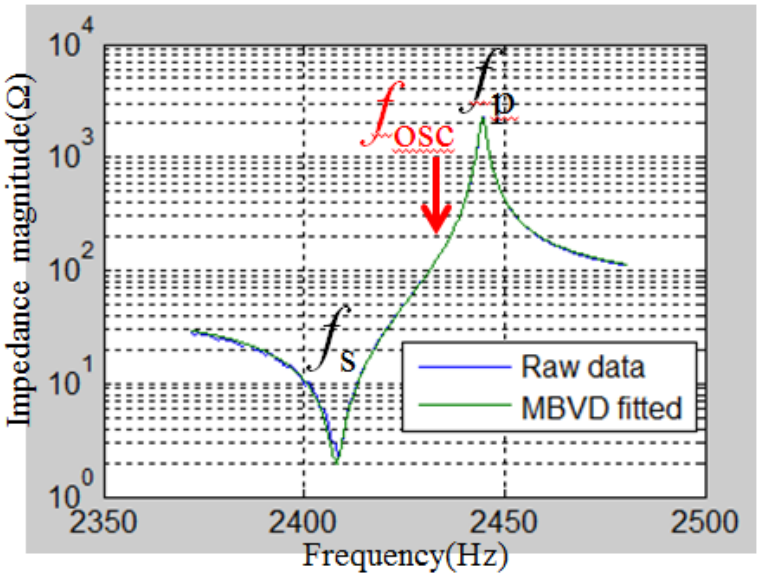
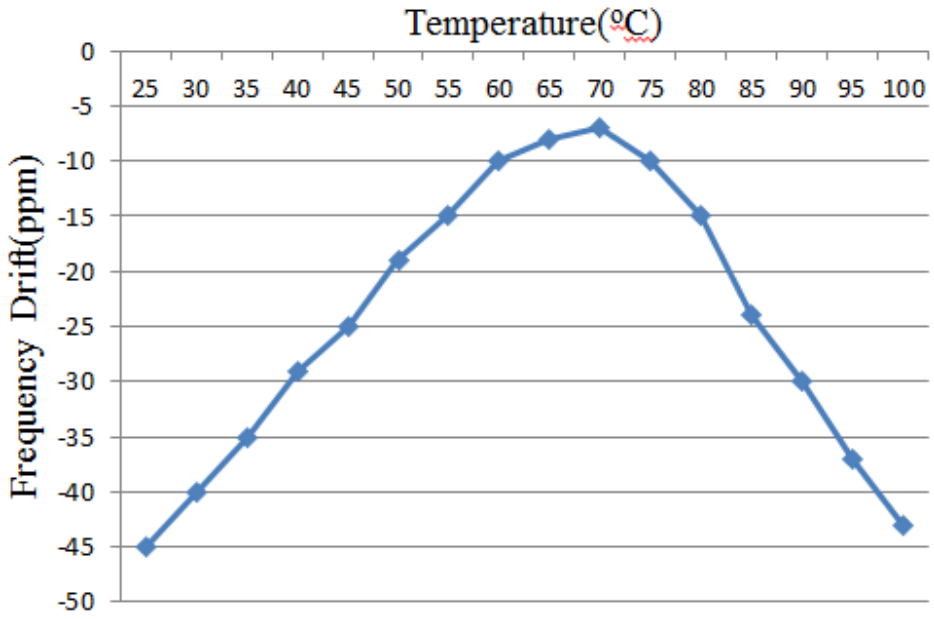
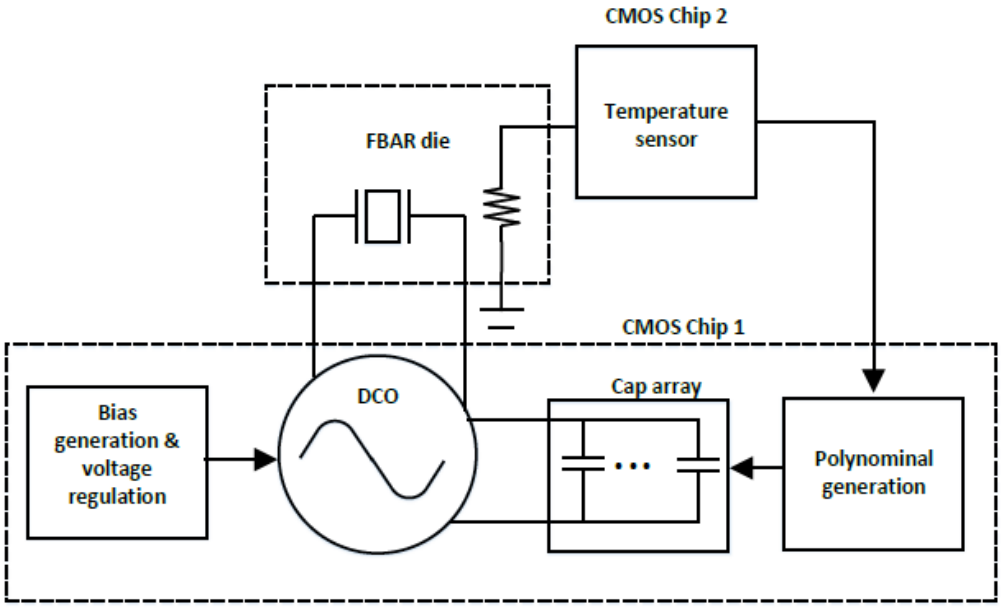



Figure 4.8 Impedance plot of a FBAR according to frequency




(a)

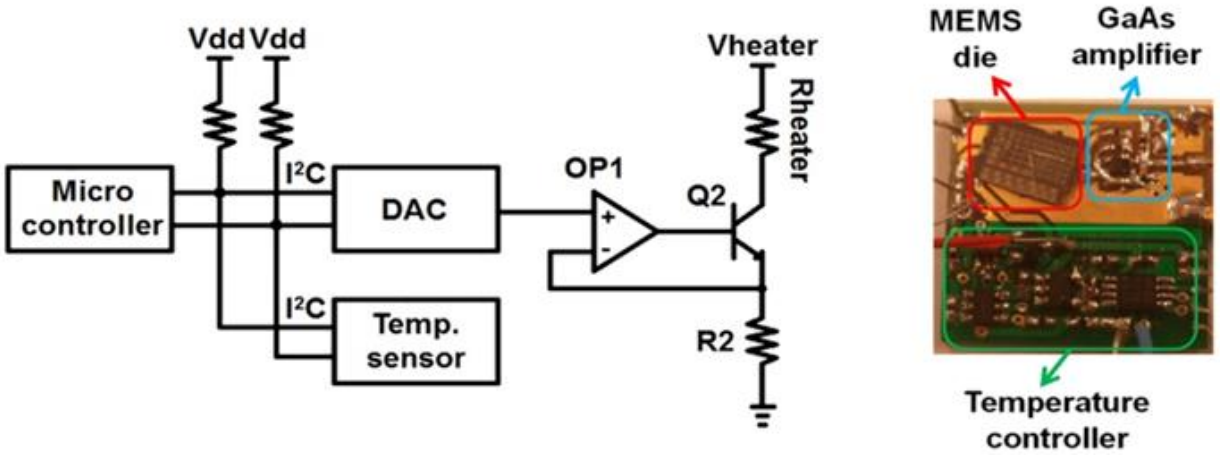



(b)

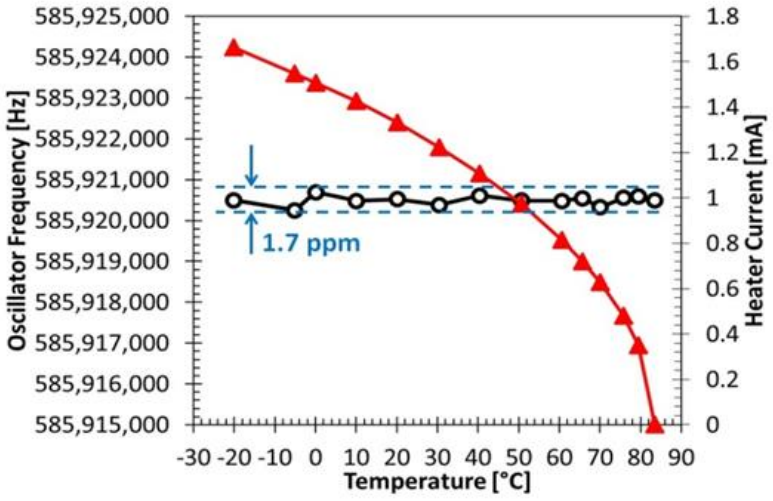
Figure 4.9 (a) frequency variation of the FBAR based oscillator without temperature compensation and (b) block diagram of the temperature compensation system

This type of system is feedforward which means the calibration for FBAR is needed before turning on the system. As shown in Figure 4.9 (a), the exact turn-over temperature point needs to be known to set the polynominal generation block.

The other methodology includes using a heater integrated with the resonator, which this work follows. There are several works that have used this methodology. For example, figure 4.10 (a) shows the block diagram of the conventional temperature compensation system using micro-controller and its chip photo. According to its test result as shown in figure 4.10 (b), it achieves less than 2ppm. But, it needs to use look up table based micro-controller, so that it is away from the goal for on-chip integration.




(a)




(b)

Figure 4.10 (a) Micro-controller based temperature compensation system with (b) its test result

The other work utilizes wheat stone bridge [36]. Figure 4.11 shows the block diagram of it. R4 represents the heater. The opamp in the figure controls the current flowing through it by making two input nodes have same voltage. The assumption here is that temperature coefficient of both R1 and R2 are the same. Although this work also generates pretty stable reference clock, two different technologies are used. For example, oscillator is fabricated by GaAs technology while other systems used CMOS. It has the same integration issue such as figure 4.10.

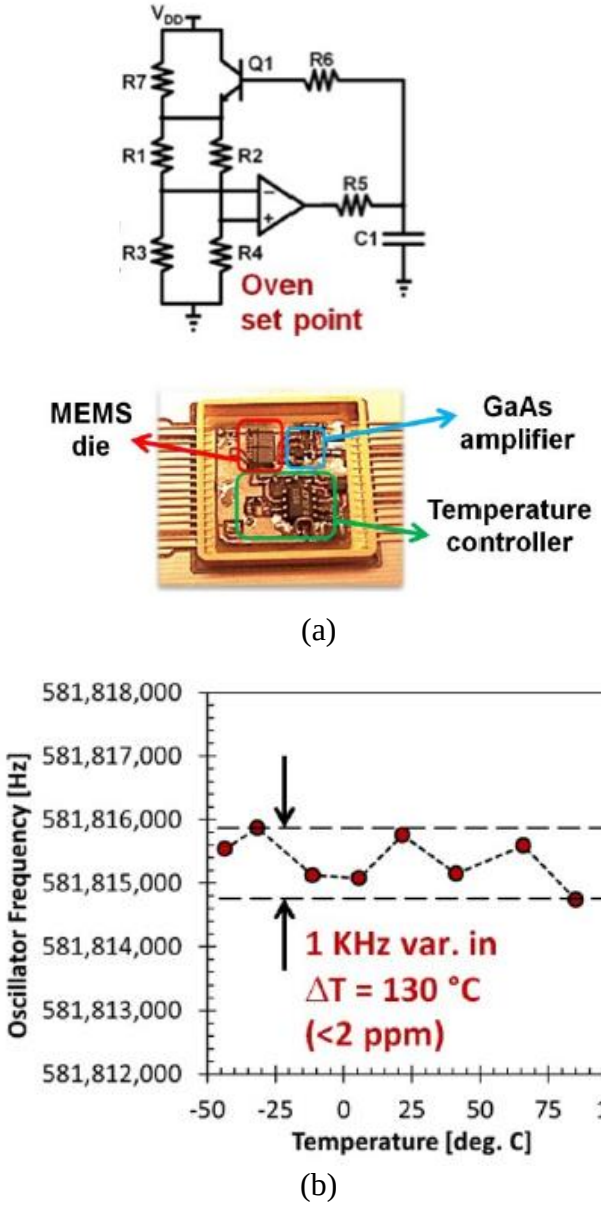



Figure 4.11 (a) Wheat stone bridge based temperature compensation system and (b) test result

*4.5 Oven controlled temperature compensation system*

Figure 4.12 represents the approach of this work. It uses the sensor integrated in the same resonator chip in order to monitor its temperature. Basically, a sensor is the resistor implemented by MEMS technology. Its resistance varies according to the changes in temperature. Temperature-to-digital converter (TDC) detects such resistance variations in real time and converts them to digital values consisting of 21 bit bus. This 21bits digital value represents the temperature of the resonator chip. The following digitally implemented integrator compares this with the target temperature value and accumulates the difference. If the temperature of the resonator chip is equal to the target, the difference of these two will decrease, and it eventually reaches '0'. Then, the accumulation will be stopped.

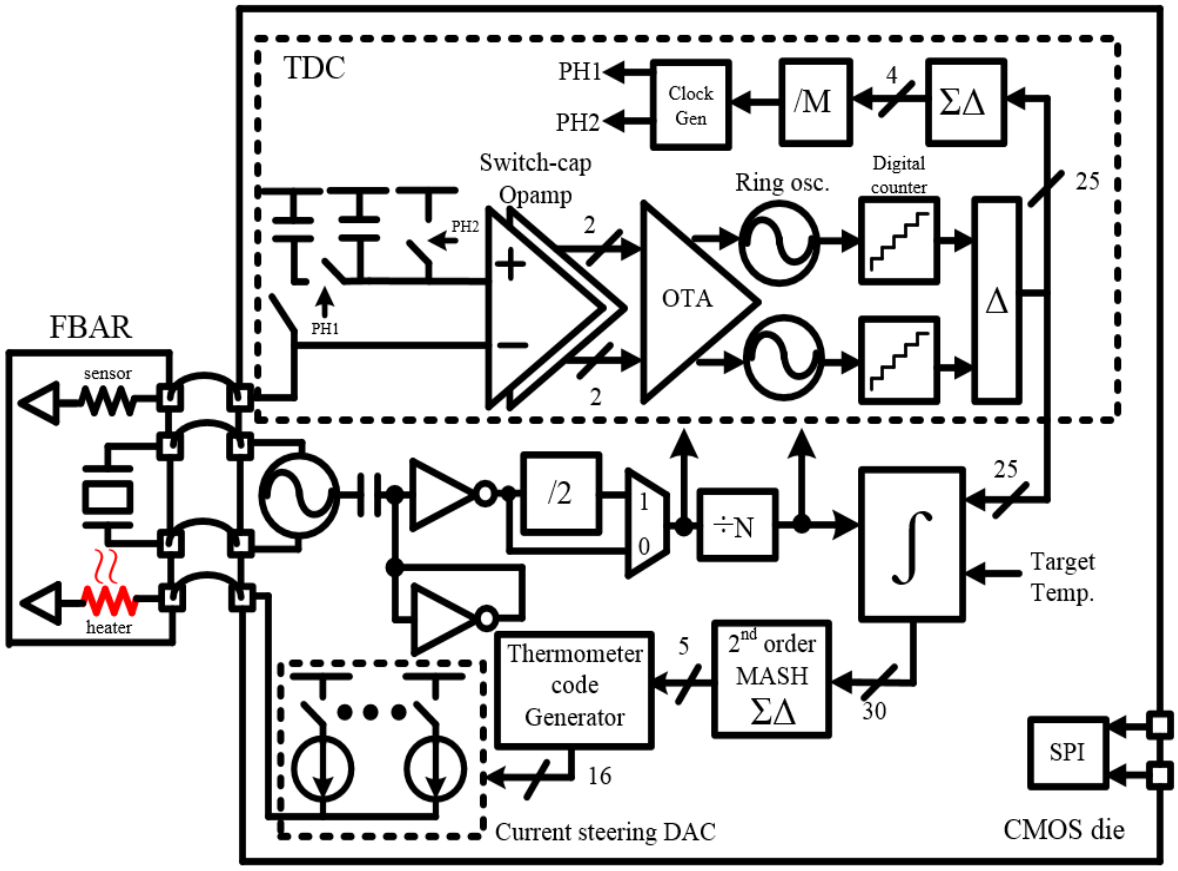



Figure 4.12 Block diagram of the oven controlled temperature compensation system

The output of the accumulator consisting of 40 bits cannot be directly connected to the current steering DAC. That's because the number of current source needed to be implemented would be $2^{40}$ if thermometer code is utilized to get low INL and DNL errors. It requires a huge area as well as large power consumption. Even if the binary control is used and 40 current sources are used, there will be other issues such as a mismatch between current sources and increased INL & DNL errors. That's why the 2nd order mesh type sigma delta modulator is used to change 40bits to 4 bits, maintaining the average value of 4bits in real time equal to an input of 40 bits. It allows the current steering DAC to have only $2^{16}$ current source with thermometer code control.

The current steering DAC can generate the output current up to 12mA to cover high temperature (80°C) with ±0.15 LSB DNL and INL errors. TDC shows superior resolution (150uK) compared to other temperature sensors [38][39][40]. As it is a negative feedback structure, it does not need calibration for the resonator chip. This lowers the test time and its time-to-market. From the following sections, each blocks will be described in more detail considering each test result.

### *4.6 Temperature to digital converter*

One of the key blocks for temperature compensation system is temperature-to-digital converter called TDC [41]. Figure 4.13 shows its entire block diagram. The front-end circuit consists of a resistive bridge that is balanced by digitally tuning a switch capacitor resistor. The resistance of the switch capacitor changes according to the frequency of the clock, clk_ph1 and clk_ph2 in the figure. The comparison of R1, sensor resistance, and switch capacitor is achieved by using a CMOS switch (sw1) to periodically short them together at 32kHz frequency. This 32kHz frequency clock is derived from FBAR based oscillator output.

In the steady state, both the sensor and switch capacitor resistance become equal, and the voltage of middle node becomes $V_{DD}/2$ when the switch (sw1) is closed. If there is a temperature change, the resistance of sensor will vary and the voltage of middle node will deviate from $V_{DD}/2$. Then, the amount of deviation will be amplified by the switch capacitor amplifier. OTA (Operational transconductance amplifier) changes the output voltage of switch capacitor amplifier to current. This current feeds to the current starving ring oscillator [42][43]. Two ring oscillators are used. The frequency of upper one as shown in figure 4.13 changes according to the front-end voltage. The other one on the bottom is utilized as a reference. The next stage, digital counter, records the

accumulated phase of each oscillator, and the digital count values are sampled. After sampling, the count values are compared with the previous values such that a fist-order difference operation is achieved. So, effectively, quantized frequency difference between the oscillators is obtained.

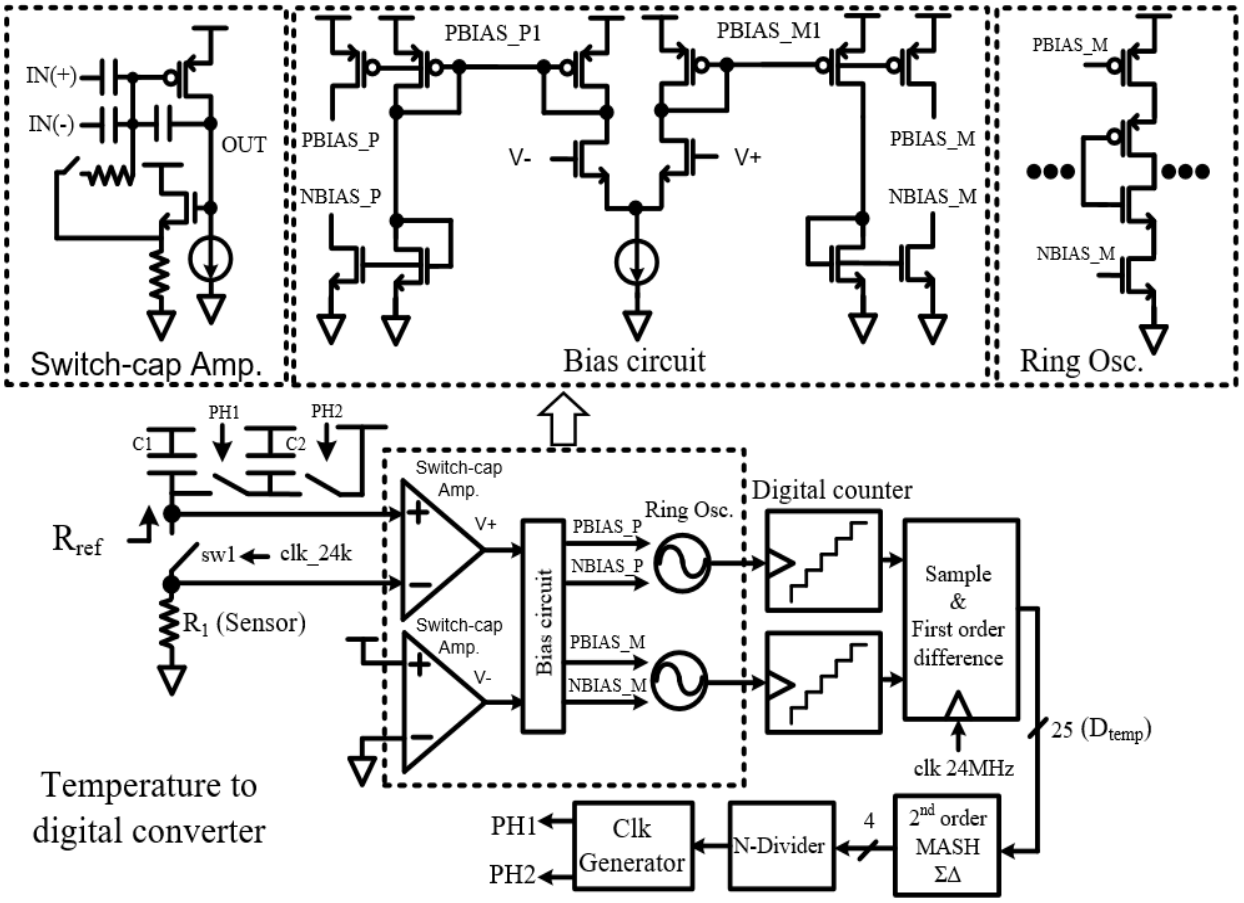



Figure 4.13 Block diagram of temperature to digital converter

This quantized digital value consisting of 25bits bus represents the temperature information on the resonator chip. The equation below represents the relationship between resistance of switch capacitor ($R_{ref}$), digital value ($D_{temp}$) and clock frequency (PH1, PH2).

$$R_{ref} = \frac{T_{PH1}}{C_2} D_{temp}$$

According to its value, clk generator block on the figure controls the frequency of both PH1 and PH2. To reduce the complexity of design, the 2nd order MASH type sigma delta modulator is used.

This decreases the number of bits from 25 bits to 4 bits. The average value of 4 bits output is the same with its 25 bits input value. The detailed structure of sigma modulator will be shown later.

### *4.7 Test result of temperature to digital converter with FBAR*

Figure 4.14 shows how the FBAR sensor is connected to the TDC front-end at the PCB test board. The first test I conducted is monitoring how digital output from TDC ($D_{temp}$) varies based on temperature change. As $D_{temp}$ has 25bits, due to limited area, I could not use 25 Pads. Instead, serializing block is included to convert 25 parallel bits to 1 bit stream data with two control signals (clock & Sync.) which are necessary for post processing. Since mixed signal oscilloscope supports only 16bits bus, the upper 16 bits among the 25 bits are monitored. Converting serialized data stream to parallel data is implemented through FPGA board (Altera DE1).

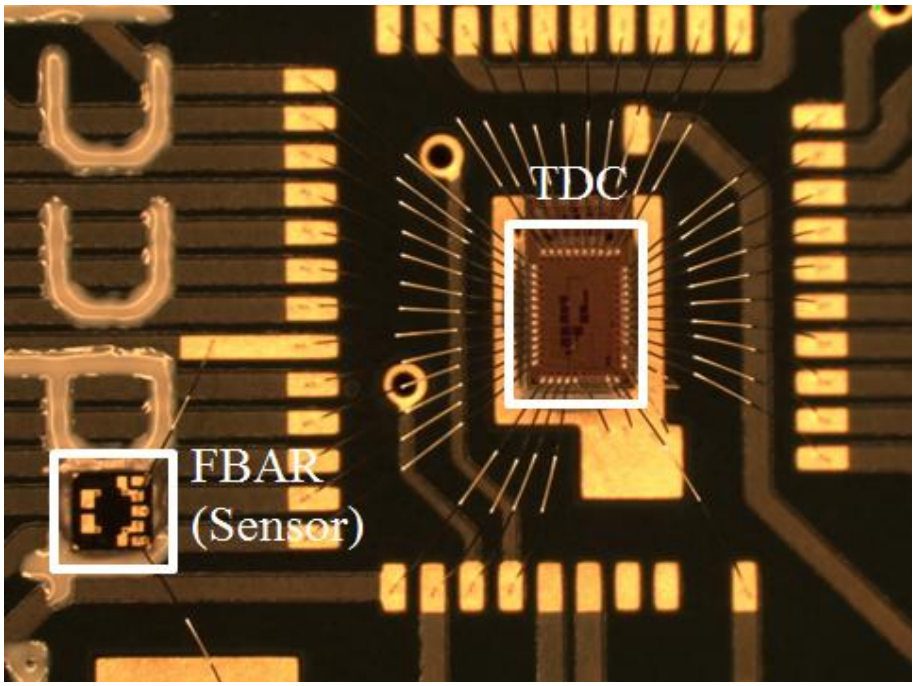



Figure 4.14 Die photo showing connection between FBAR sensor and TDC chip

When I taped out the first prototype of TDC and started testing in 2014, there was no temperature chamber to control the temperature of the chip. So, I put an entire test board in the oil tank. The temperature of the tank can be increased by using a heat plate as shown at Figure 4.15.

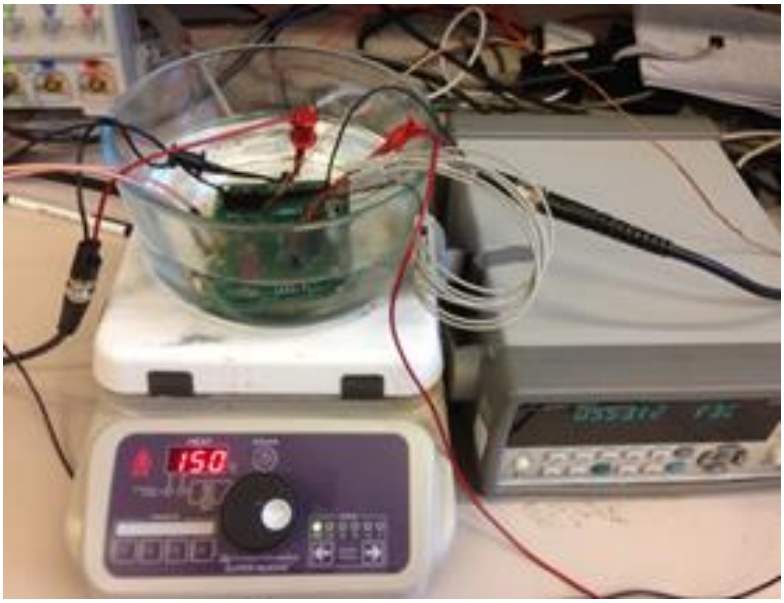



Figure 4.15 Test set up for TDC with oil tank and heat plate

As a heat plate is used, there is no way to cool down the temperature below the room temperature (25°C). The target operating power supply $V_{DD}$ for TDC was 750mV for low power consumption, but at low voltage the linearity was not good as shown in Figure 4.16. For the sake of comparison of linearity, another temperature sensor called RTD is attached beneath the test board.

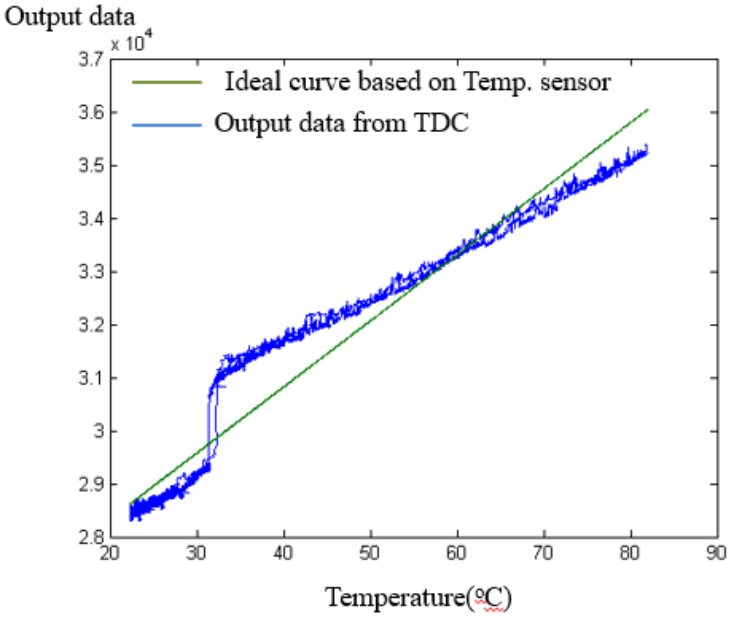



Figure 4.16 TDC output according to temperature with RTD

Since the impedance of RTD changes linearity, I can compare it with TDC output. The green curve represents RTD and the blue curve the TDC output. To obtain similar linearity with RTD, $V_{DD}$ is increased up to 980mV and a half frequency clock (500MHz) is used. There is a divider and an MUX between the oscillator output and the TDC clock input, so we can choose either 1GHz oscillator output or 500MHz. Figure 4.17 shows the best linearity obtained. Although the power consumption is 1.9mW, the TDC resolution is 150uK based on this test result.

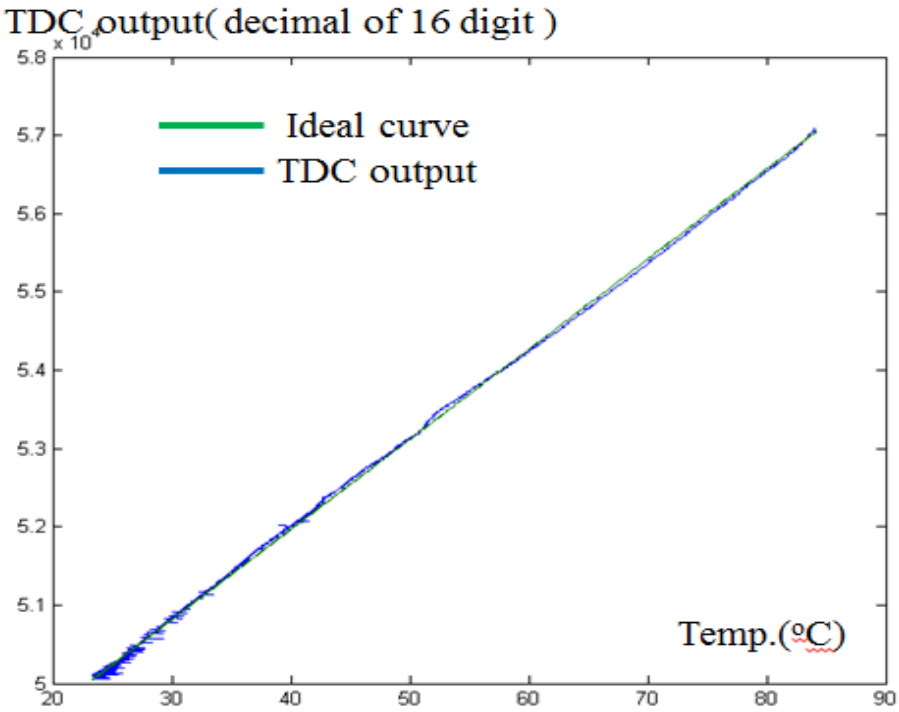
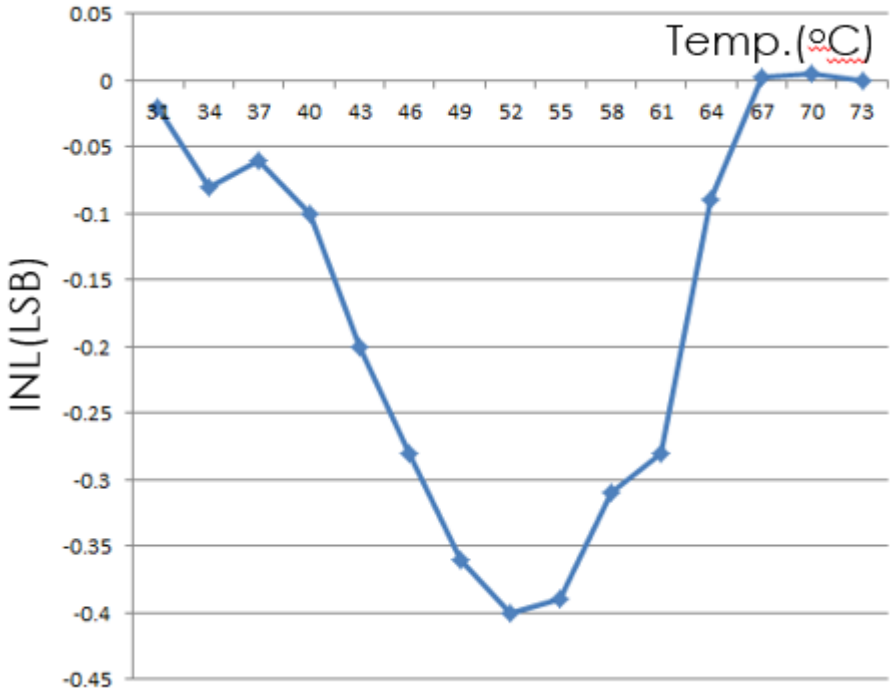


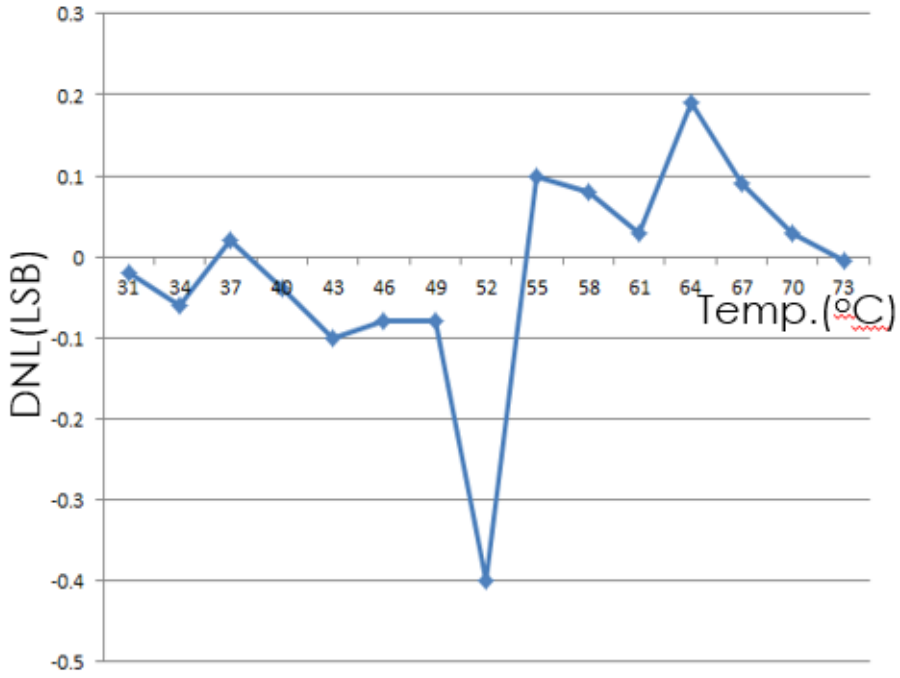

Figure 4.17 Best TDC linearity with 980mV $V_{DD}$.

Besides the linearity test, INL & DNL errors are calculated and plotted in Figure 4.18. INL & DNL errors are normal indications of accuracy when ADC performance needs to be compared with other works. As TDC also converts the analog information such as resistance variation to digital value according to the temperature, it makes sense to use INL & DNL calculation.

There are more than 80 points for temperature, leading to a complicated curve on the plot. In the end, 16 temperature points showing worst errors are selected. The maximum error from Figure 4.18 is 0.6LSB.




(a)




(b)

Figure 4.18 (a) INL and (b) DNL error from TDC

*4.8 Test result of temperature to digital converter with AlN CMR*

The test result until now is based on FBAR sensor. Another sensor in AlN CMR device is also used for TDC test to check if TDC functionality is same. Figure 4.19 shows die photo. After AlN CMR device is fabricated by Carnegie Mellon University MEMS fab, the resonator is exposed to air. So, we cannot get each device because chip can be damaged during dicing process. That's why AlN CMR chip has huge size and only one of them is connected through wire.

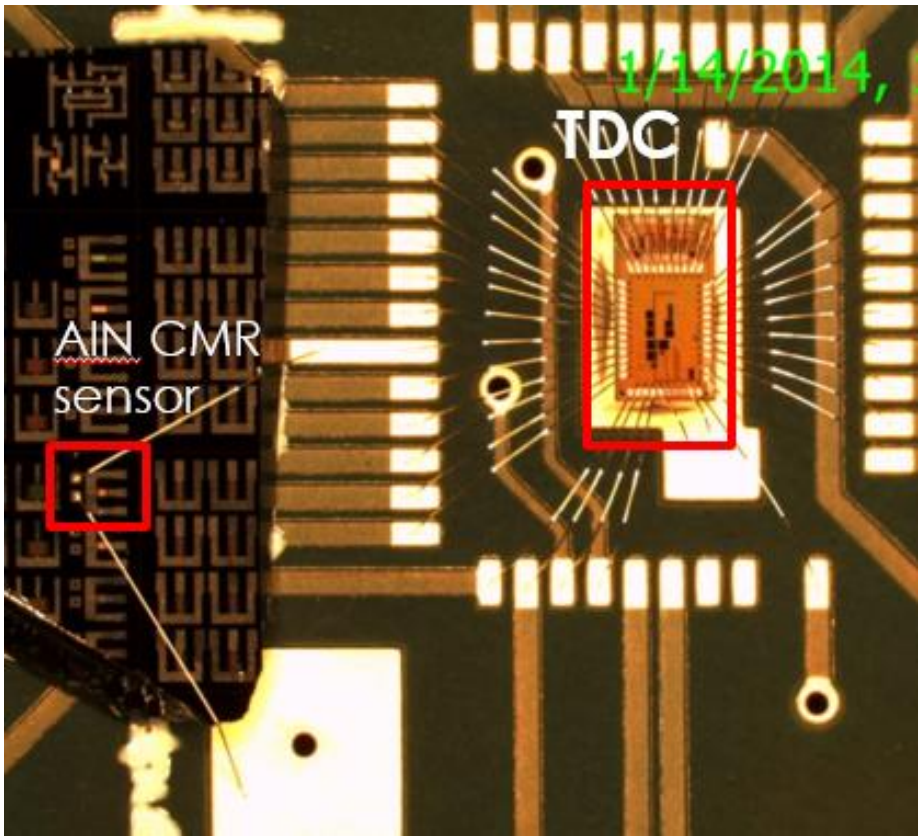



Figure 4.19 Die photo of TDC connected to AlN CMR sensor

When I start this test, a new temperature chamber arrives as shown in Figure 4.20, and the temperature of the boards can be controlled such that it can go below down to -40$^{o}$C and increase up to 120$^{o}$C. Figure 4.21 and 4.22 represents block diagram showing two types test set up. One is that I put only AlN CMR sensor inside the chamber and change the temperature from -40$^{o}$C to 100$^{o}$C. The purpose of this set up is for checking how wide the resistance of AlN CMR sensor varies. As shown in Figure 4.21, TDC can maintain a good linearity over a wide temperature range.


Figure 4.20 Temperature chamber used for TDC test

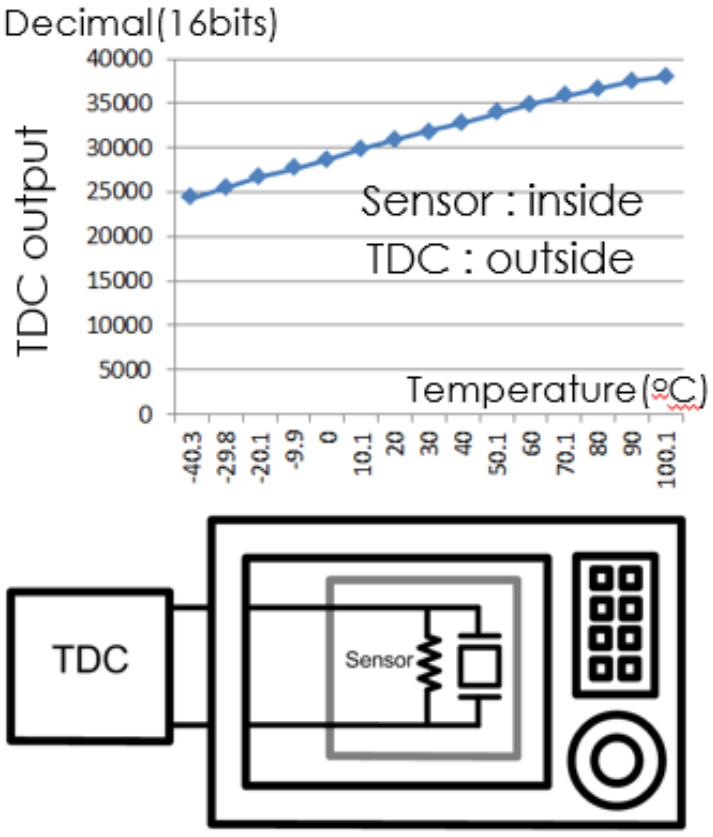



Figure 4.21 Test set up with sensor inside chamber

The other set up is where the AlN CMR sensor all TDC chips are put inside. There was an issue in this test. Figure 4.22 shows that TDC output values are dropped when the temperature goes below -10°C. This happens because of shift register inside TDC. Synthesized shift registers are for programming TDC before it starts working. This gives us the freedom to debug it whenever necessary. For some reason, however, these registers lose their stored value when the temperature goes below -10°C. That's why the lowest temperature limit has been set from -10°C since then.

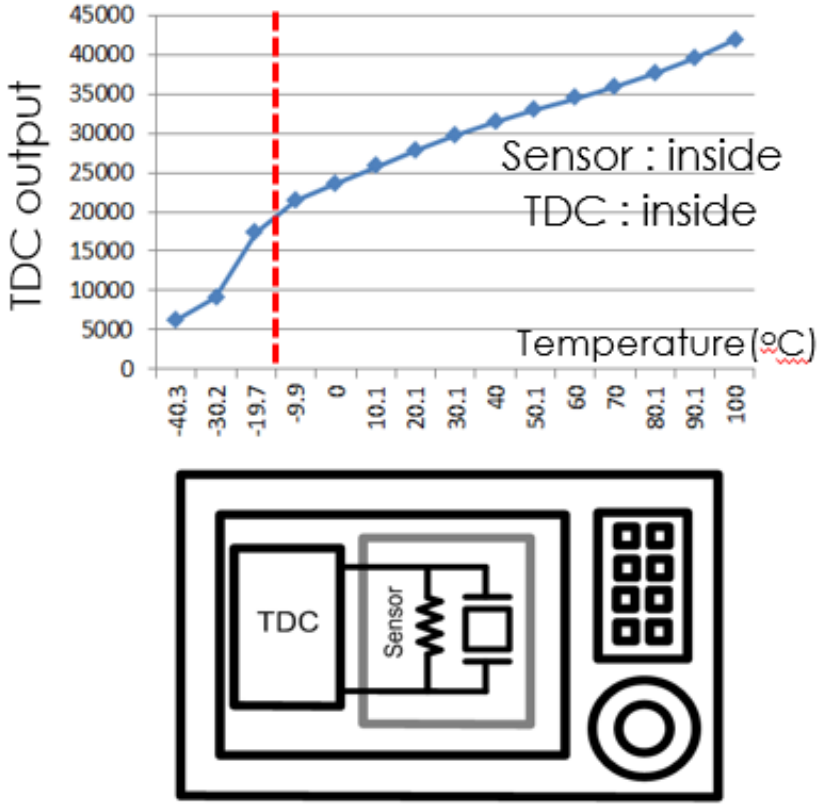



Figure 4.22 Test set up with all test chips inside

## *4.9 Detection range of temperature to digital converter*

The other characteristic of TDC I need to test is its detection range. There must be lowest and highest resistance values which TDC can detect. For this check, I had built a bunch of off-chip resistors connected in series as shown in Figure 4.23. The default resistance connected to TDC is 1.35kohm. Resistance can be increased by moving one of the taps connected to TDC next to the resistor. In this test set up, I can increase the resistance by 100ohm. To sum up, the TDC can detect

resistance from 1.5kohm to 3.6kohm. If either the FBAR or AlN CMR sensor changes within this range over temperature change, TDC will have no issue for its functionality.

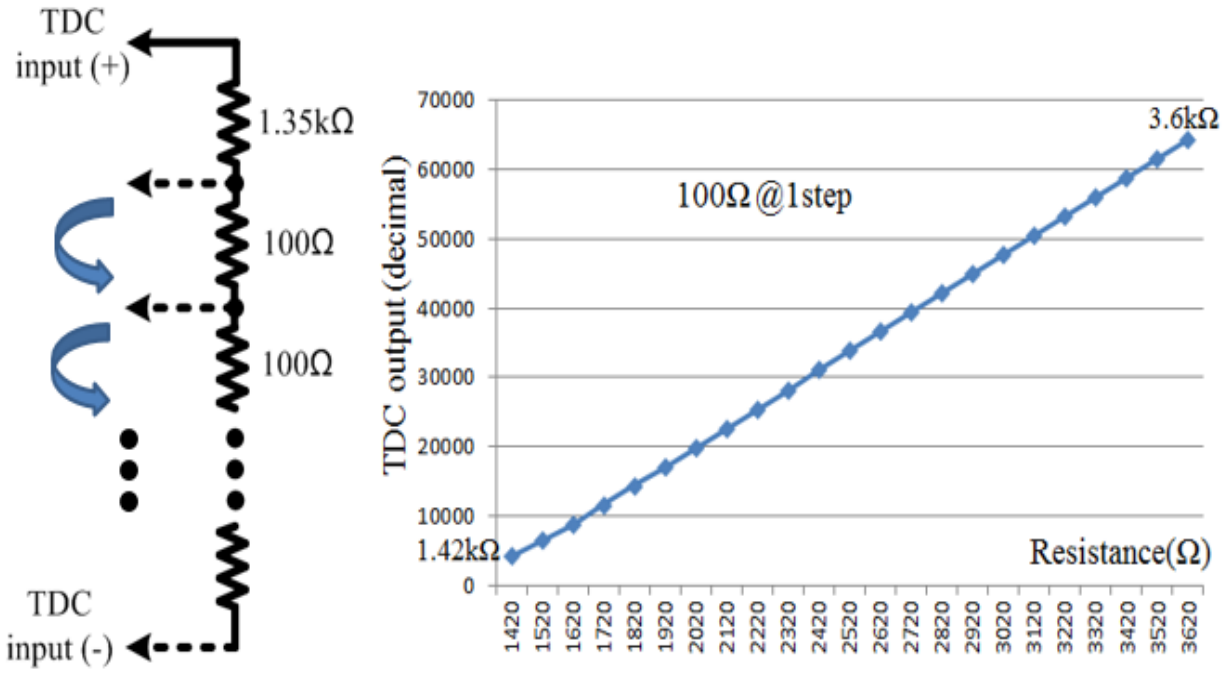



Figure 4.23 Test result for detection range of TDC

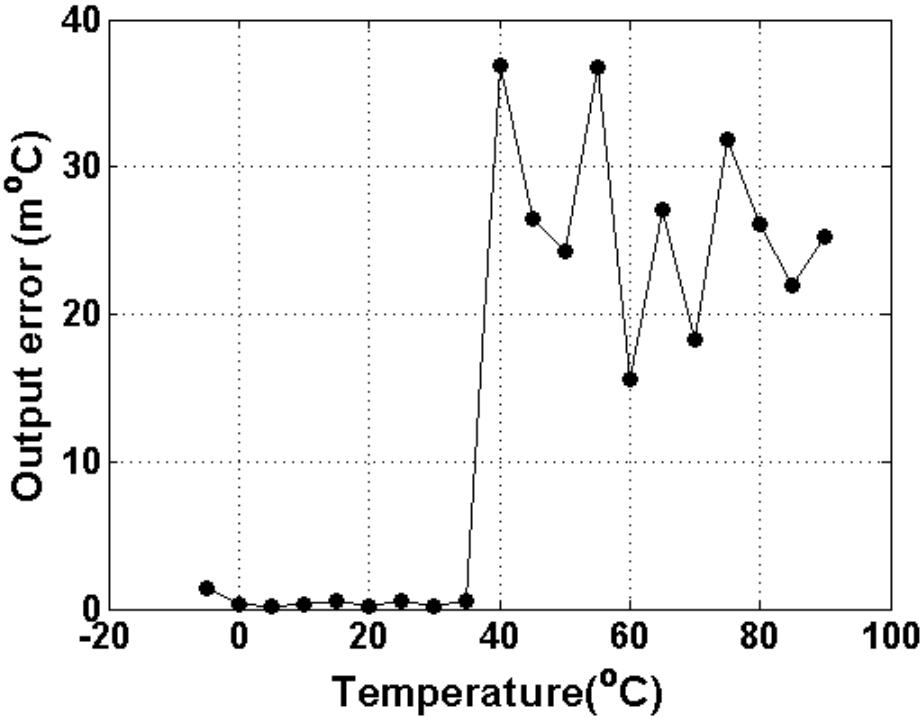



Figure 4.24 TDC output error

Figure 4.24 shows the output error of TDC. 100k samples are collected in real time and their standard deviation is calculated for TDC error at each temperature point. At low temperature (<40$^{o}$C), it has only 1m$^{o}$C error. But when the temperature increases above 40$^{o}$C, error increases up to 40m$^{o}$C. Fortunately, this error is low enough to achieve less than 2ppm frequency variation.

## *4.10 1$^{st}$ prototype for current steering DAC*

Another key block in oven controlled temperature compensation system is the current steering DAC. Basically, most of the DAC output is voltage [44][45], but it needs to control the current flowing through the heater. One of the difficulties for implementing current output DAC is that the output impedance is changed according to the amount of current. It can lead to degrading the INL and DNL characteristics. Figure 4.25 shows the 1$^{st}$ prototype of DAC. The input for DAC consists of 4bits which means the total number of current source is 16 ($2^{16}$). Each unit current source consists of a PMOS switch and a dummy NMOS (M3). By using current mirror M4 and M5, the currents are copied to the output stage. Op-amp and stacked NMOS are used in order to make both M4 and M5 drain voltage equal. Another thick NMOS thick devices are stacked on top of the normal device because high $V_{DD}$ is used. Figure 4.26 shows the simulation result. Each unit current source is turned on sequentially by 10ns steps. It is equivalent to 10Mbps of the input data rate.

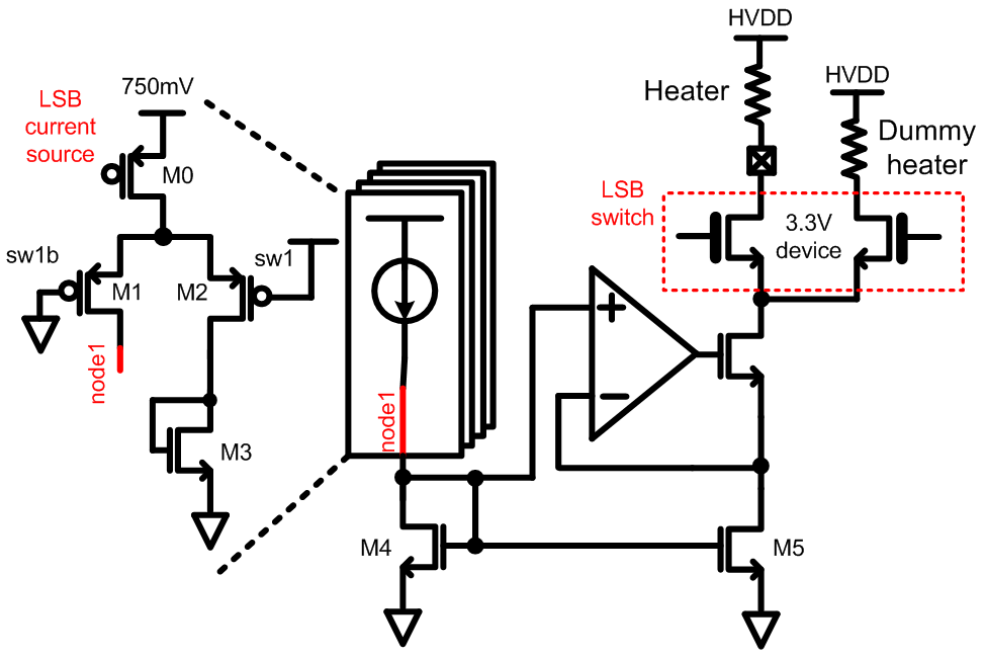



Figure 4.25 1$^{st}$ prototype current steering DAC

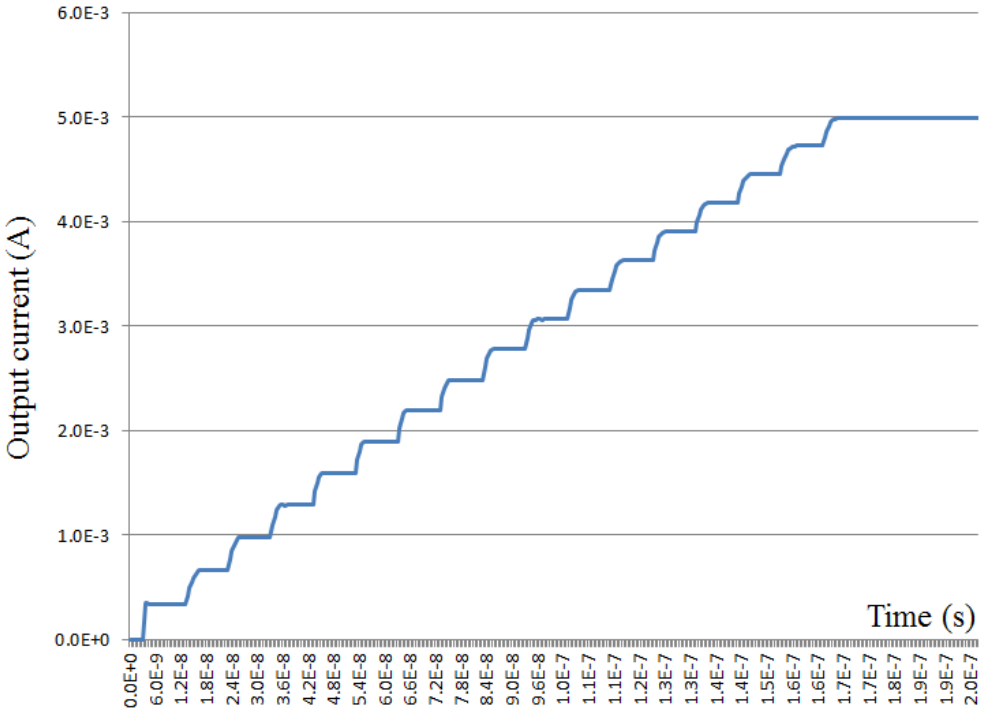
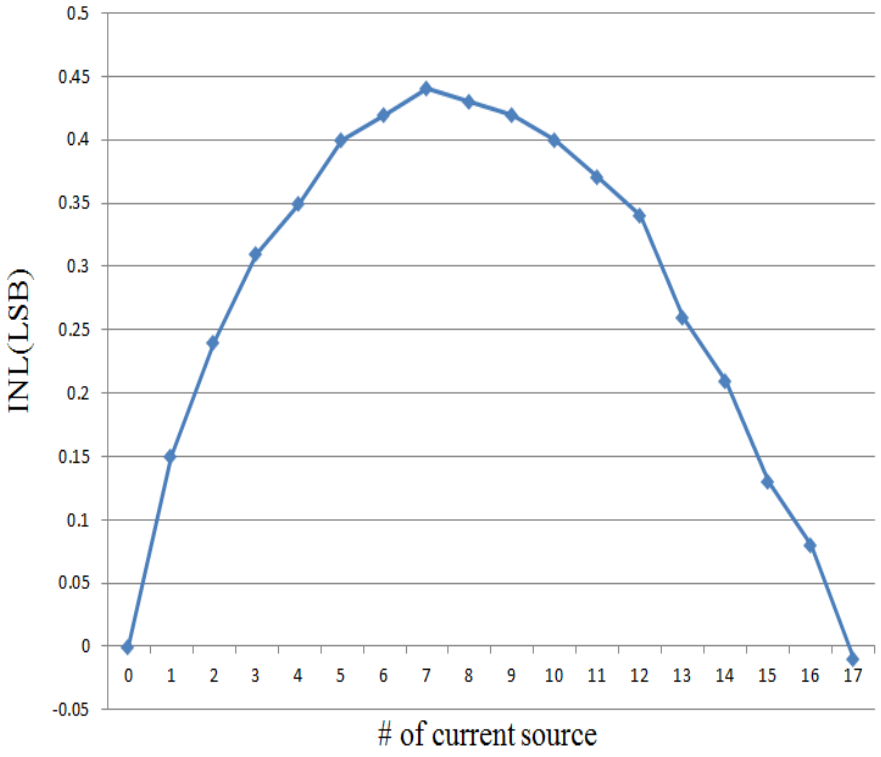
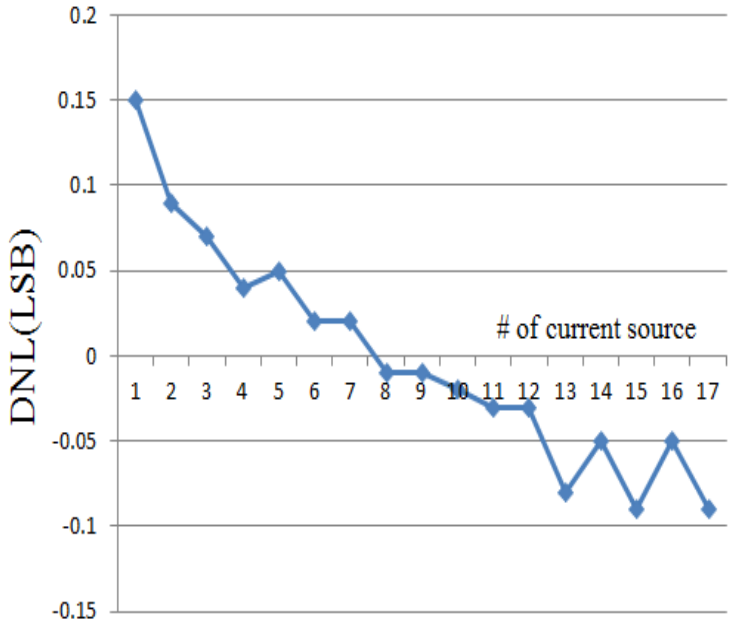



Figure 4.26 Simulation result with 20Mbps input data rate




(a)




(b)

Figure 4.27 (a) INL and (b) DNL error of 1st prototype current steering DAC

Figure 4.27 shows the INL & DNL errors. The maximum error is 0.45 LSB. Although the simulation result showed that it has high accuracy and had no problem to work up to 2V $V_{DD}$ for output stage, in real test, the NMOS stacked above M5 device was very vulnerable to high $V_{DD}$. I expected thick device used for switch of LSB input data would protect normal NMOS from high $V_{DD}$. But when it turned on, $V_{DS}$ was almost zero because thick device operated in linear region as a switch. That's why high VDD was directly connected to normal NMOS and broke it up. Even with 1.5V, there was a huge leakage current flowing through output stage.

*4.11 2nd prototype for current steering DAC*

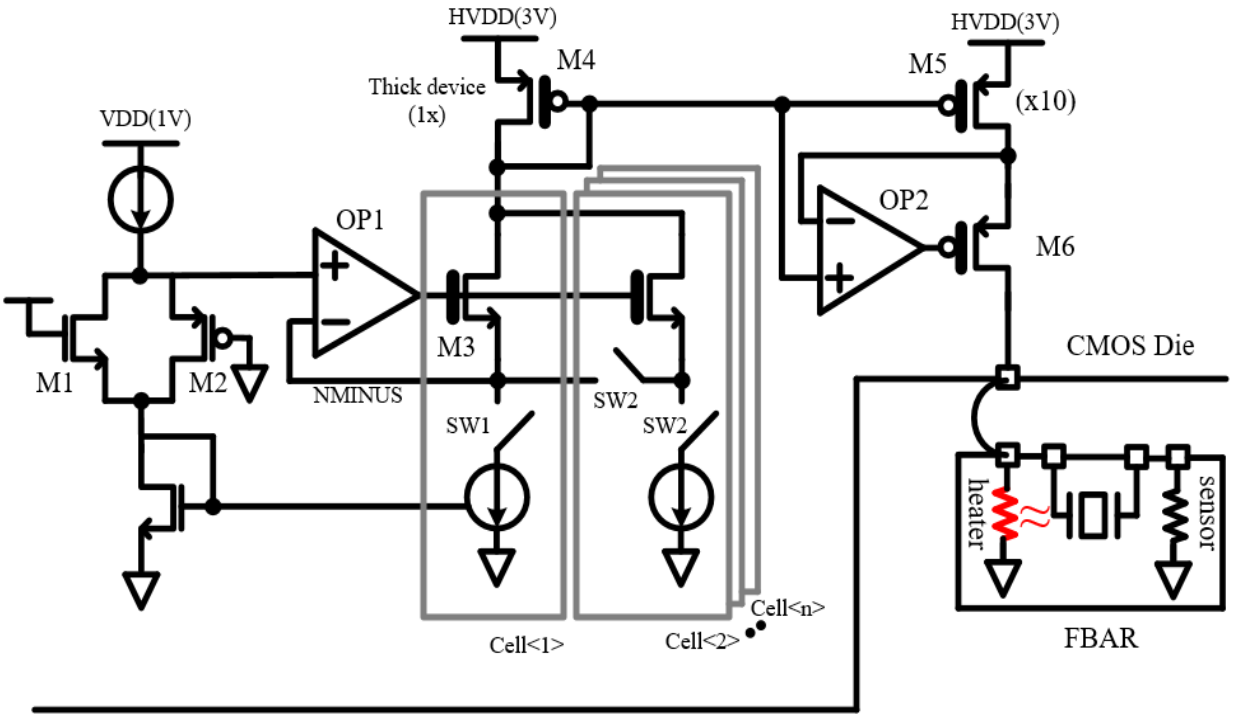
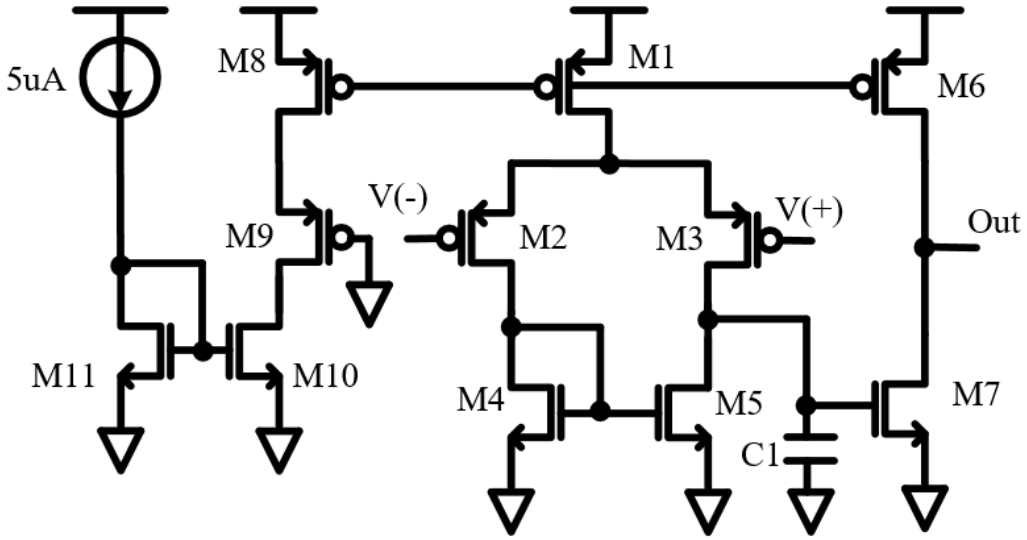



Figure 4.28 2nd prototype for current steering DAC

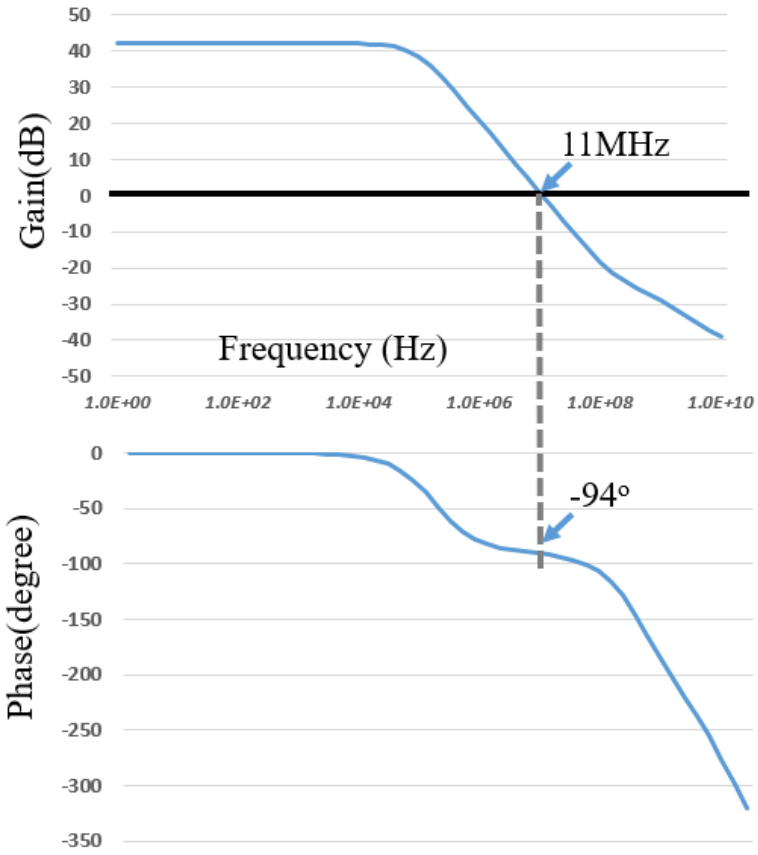
Figure 4.28 shows the modified current steering DAC which is robust to high $V_{DD}$ and has higher accuracy. It shows that the output stage is directly connected to the heater through wirebonding. The mechanism of operation is similar to 1st prototype. 17 number of current sources are used. As the digital input value varies by the thermometer control, the same amount of current sources are used. When the current sources are turning on sequentially, the voltage of the node which sums up all current changes as the output impedance looking at turned-on current sources decrease. It degrades the INL & DNL errors. Therefore, opamp (OP1) and M3 thick devices are used to maintain the output voltage of the current source to a certain value. This results in high output impedance leading to low DNL and INL errors.

Figure 4.29 shows the block diagram of opamp (OP1) and its gain and bandwidth simulation results. The bandwidth is the bottleneck of the DAC in terms of both operating frequency and accuracy. That's why it is important to design opamps (OP1 and OP2) carefully. Based on the simulation result in Figure 4.29 (b), the unity gain bandwidth is almost 10MHz with 86° phase

margin. The maximum input data rate will be 2MHz, so opamp (OP1) is able to maintain output impedance of current source high.

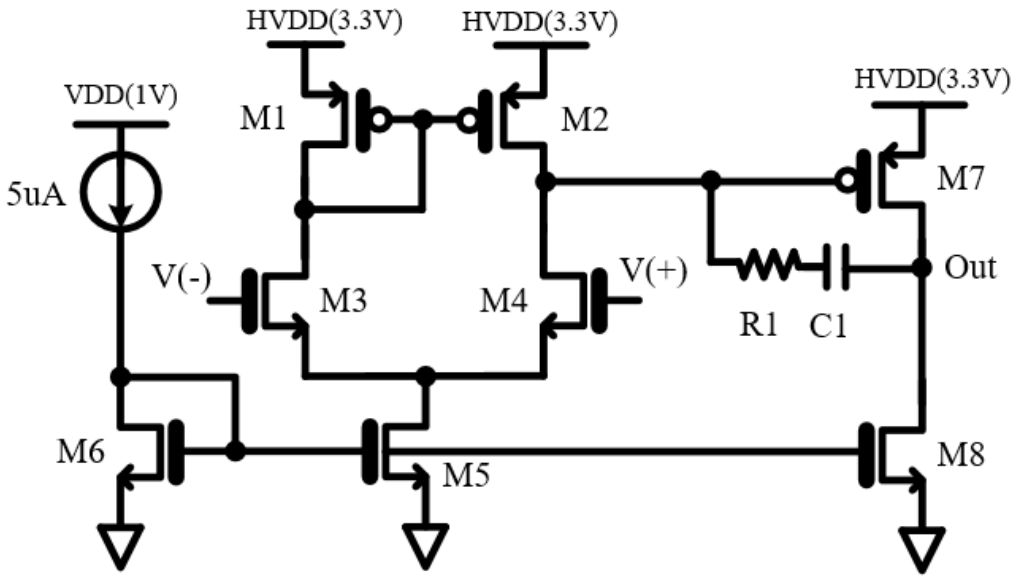



(a)

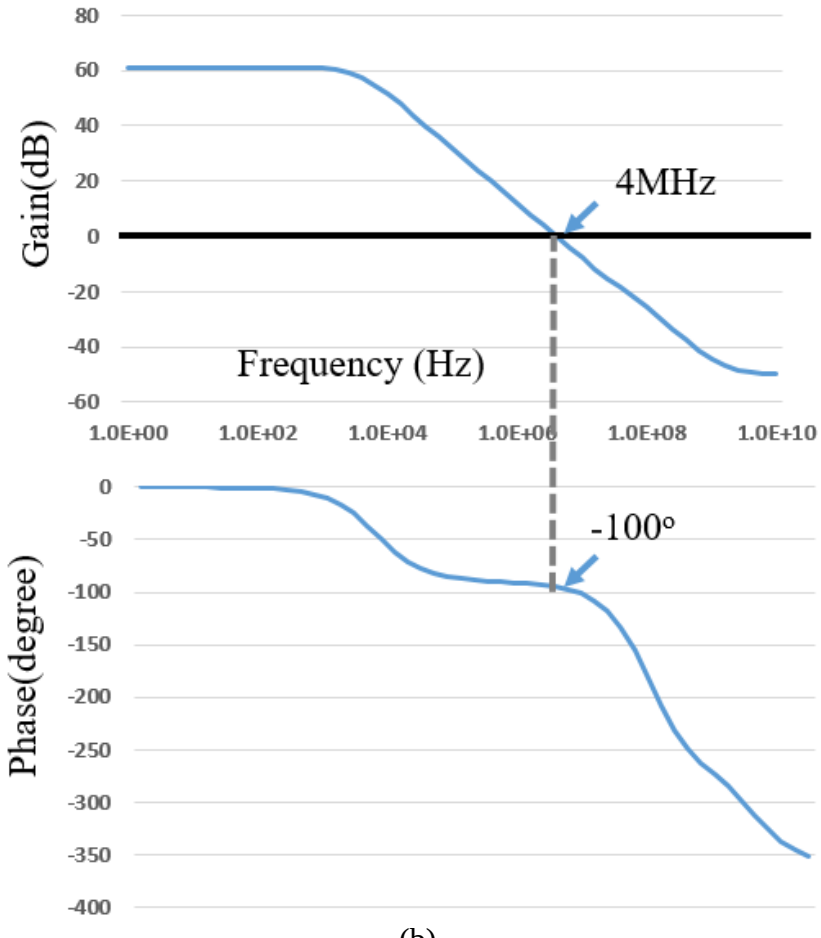



(b)

Figure 4.29 (a) Block diagram of opamp (OP1) used at DAC and (b) its gain with phase margin




(a)




(b)

Figure 4.30 (a) Block diagram of OP2 and (b) its post layout simulation result

Figure 4.30 shows another opamp (OP2) used at the output stage of DAC. To copy the summation of turned-on current into output stage, current mirrors (M4 & M5) are used. The maximum current to cover the whole temperature range (-5°C to 85°C) is almost 12mA. That's why 3.3V high $V_{DD}$ is needed because two PMOS in output stage should operate in the saturation mode. Considering $2V_{DS}$ with voltage drop through heater, 3.3V is necessary for enough head room. Due to high supply voltage, all devices used are thick 2.5V PMOS or NMOS, whose transconductance is low given the same size with the 1V normal device. It results in low unity gain bandwidth which is 4MHz, but it is high enough to cover the input data rate. The detail size of all devices is shown in Appendix A.

## *4.12 Test result of the current steering DAC*

The shift register can be programmed to feed the input data manually; the output current flowing through the heater can be monitored. The DAC is tuned to have 3.5mA of maximum output current first. Figure 4.31 shows how the output current changes according to the input data. For the comparison purpose, simulation result is also plotted in the same chart. As you can see, the test result exactly matches with the simulation result. At the max. input, the amount of current is slightly deviated from the ideal value (50uA), but its accuracy is high enough.

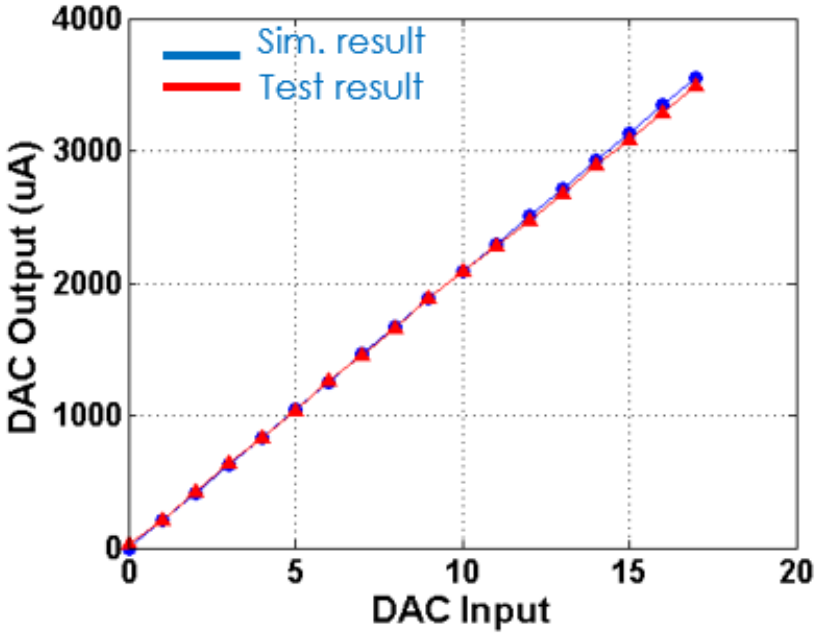



Figure 4.31 Test result of the current steering DAC

We can see the characteristic of DAC more clearly in terms of its error by using INL and DNL as shown in Figure 4.32. The maximum error is 0.25 LSB which is lower than 1st prototype DAC (0.4 LSB).

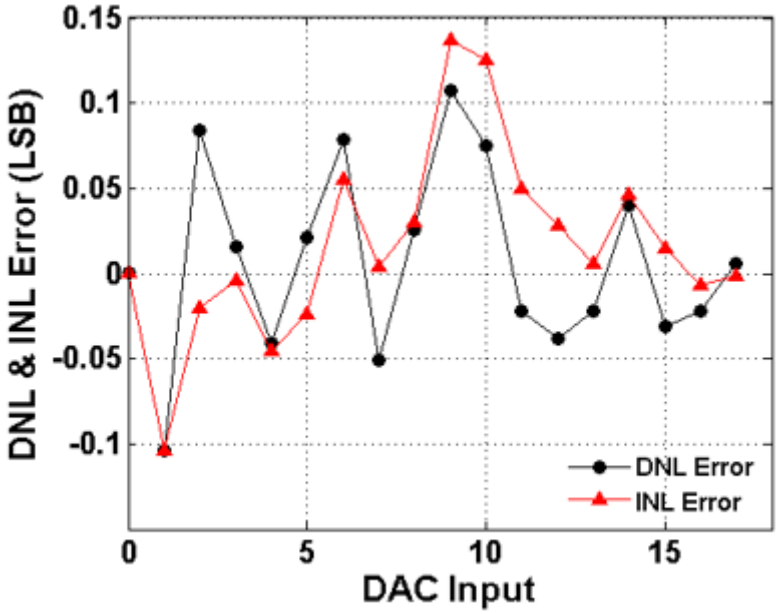



Figure 4.32 INL and DNL of the current steering DAC

*4.13 2nd order MASH type sigma delta modulator*

One of the key factors contributing to the high accuracy of DAC is that only 17 current sources are built up on the inside. This is possible because the input data only consists of 5 bits (4 bits + sign bit). Although the output of the digital integrator has 40 bits, the 2nd order MASH type sigma delta modulator shrinks those large number of bits into only 5 bits as shown in the Figure 4.33 [46]. This same type of sigma delta modulator is also used at TDC. The transfer function between input and output is given by:

$$\mathrm{V} = \mathrm{U} \times Z^{-2} + \mathrm{E1} \times [\mathrm{H2} - (1 - Z^{-1})Z^{-2}] - E2(1 - Z^{-1})H2$$

If you see Figure 4.33, there are two times bits truncation to shrink the number of bits. Then, there must be errors from that. E1 and E2 represents those errors induced by truncations. So, to remove the E1 error in order to minimize the difference between input and output, H2 filter should be made

equal to $(1-Z^{-1})Z^{-2}$ transfer function. Then, the output can be described using the below transfer function.

$$V = U \times Z^{-2} - E2(1 - Z^{-1})^2 Z^{-2}$$

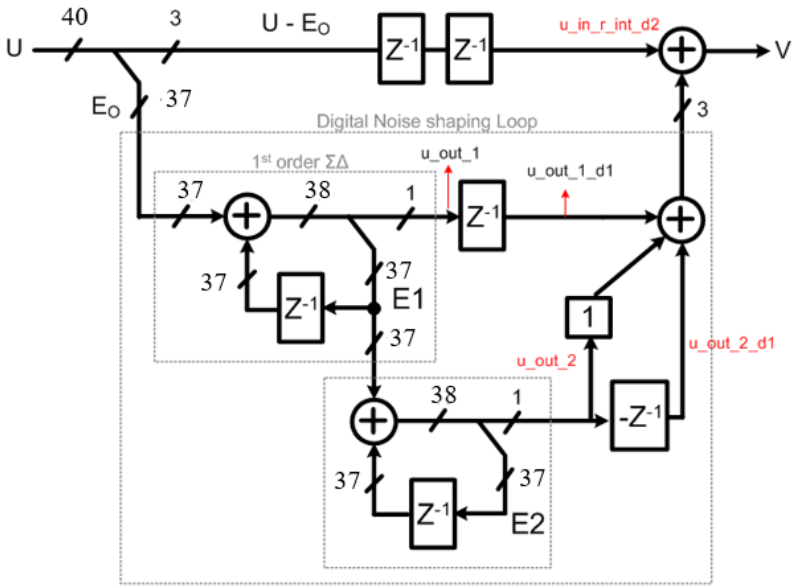



Figure 4.33 Block diagram of the 2nd order MASH type sigma delta modulator

## *4.14 Test result of the oven controlled temperature compensation system*

Now, I'm going to show you the test result of the oven controlled temperature compensation system. AlN CMR device has two spurious modes as shown in Figure 3.11 and cannot have fixed characteristics for constructing mBVD model. Therefore, it was difficult to optimize the transformer coupled oscillator. Fortunately, when I taped out the system, the capacitor array is integrated to make the oscillator work either with FBAR or AlN CMR. Thus, FBAR is used for temperature compensation system test.

Figure 4.34 shows the die photo of the system chip wirebonded with FBAR. The sensor and heater are connected to the TDC front-end and current steering DAC output respectively through PCB boards. For more information, heater resistance is around 120 ohm and sensor has 2kohm resistance which is within the TDC detection range as shown in Figure 4.23.

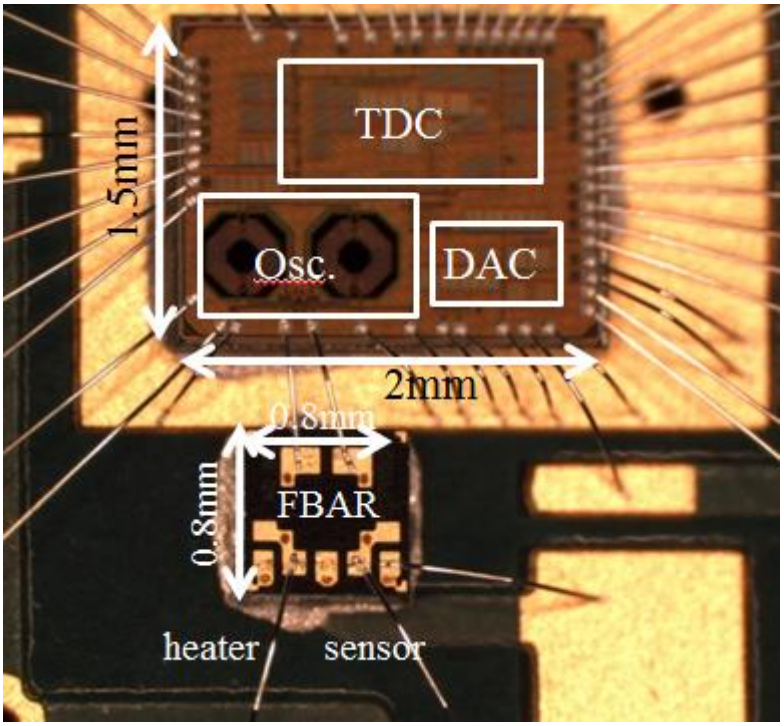



Figure 4.34 Die photo of the oven controlled temperature compensation system with FBAR.

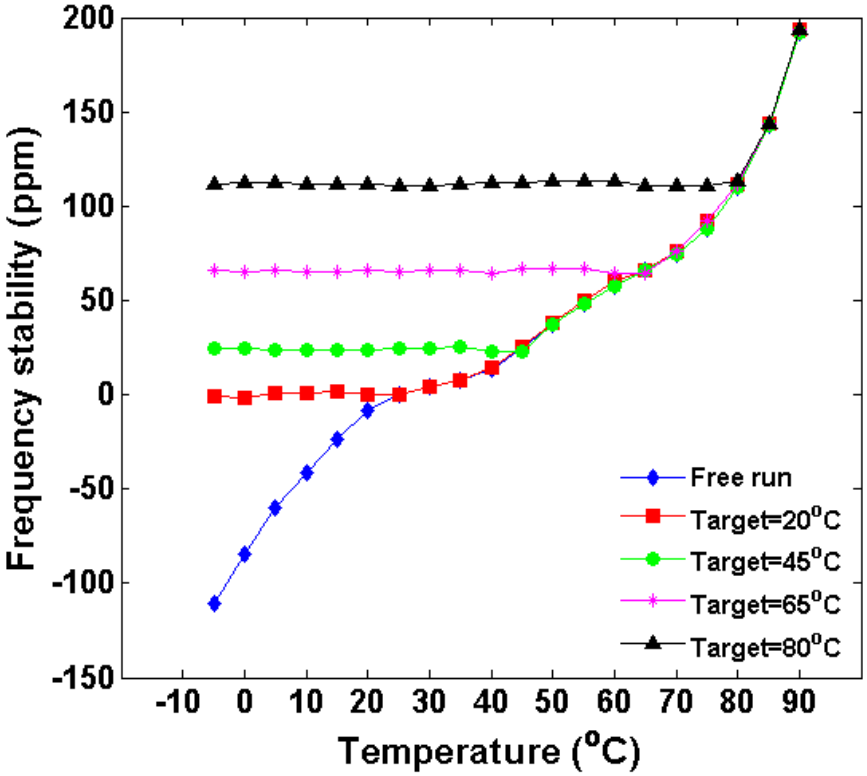
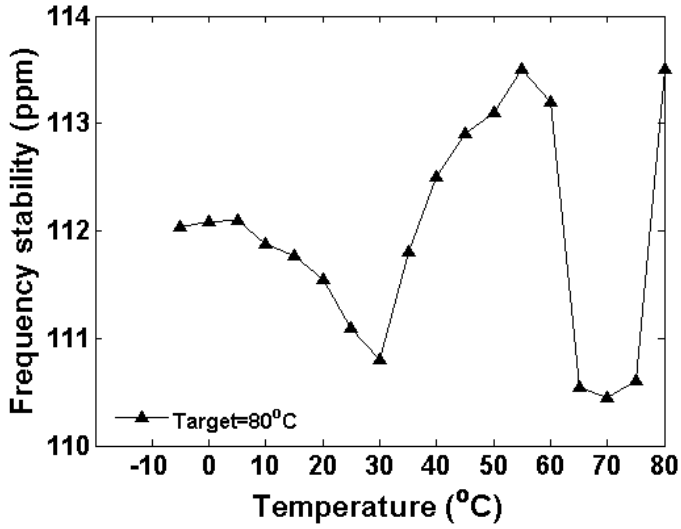
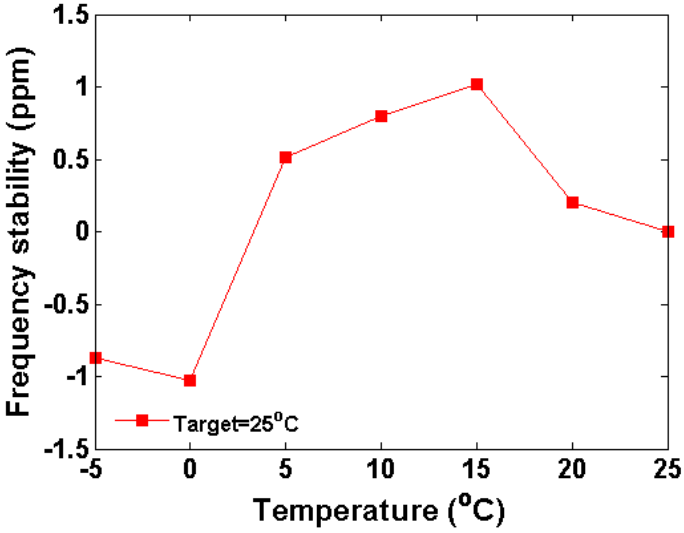



Figure 4.35 Frequency drift of the oscillator over the temperature change with system on and off

Figure 4.35 shows the frequency drift of the oscillator over the temperature change with system on and off. The blue graph represents how much the frequency varies when the system is off. The overall frequency change is around 300ppm which is larger than I expected. When the system is turned on and the shift registers are programmed to have the target temperature of 20°C, red curve shows that the frequency is stable until temperature reaches to 20°C. When the target temperature is set to 80°C, the oscillator output clock is stable until it reaches the target temperature. Figure 4.36 shows the detail test result of both low target temperature (20°C) and high target temperature (80°C). As shown in this plot, the maximum frequency drift is ±1.55ppm.




(a)




(b)

Figure 4.36 Frequency stability when the target temperature is set to (a) 20°C and (b) 80°C

It is interesting to see how the output current from current steering DAC changes when the temperature varies with various target temperatures. Figure 4.37 shows such results. When the target is programmed to have 80°C and the current temperature of the chip is -5°C, the maximum current, in this case 12mA, is required to generate heat for 80°C. As the temperature inside the chamber (Figure 4.20) increases, you can see that the output current from DAC decreases.

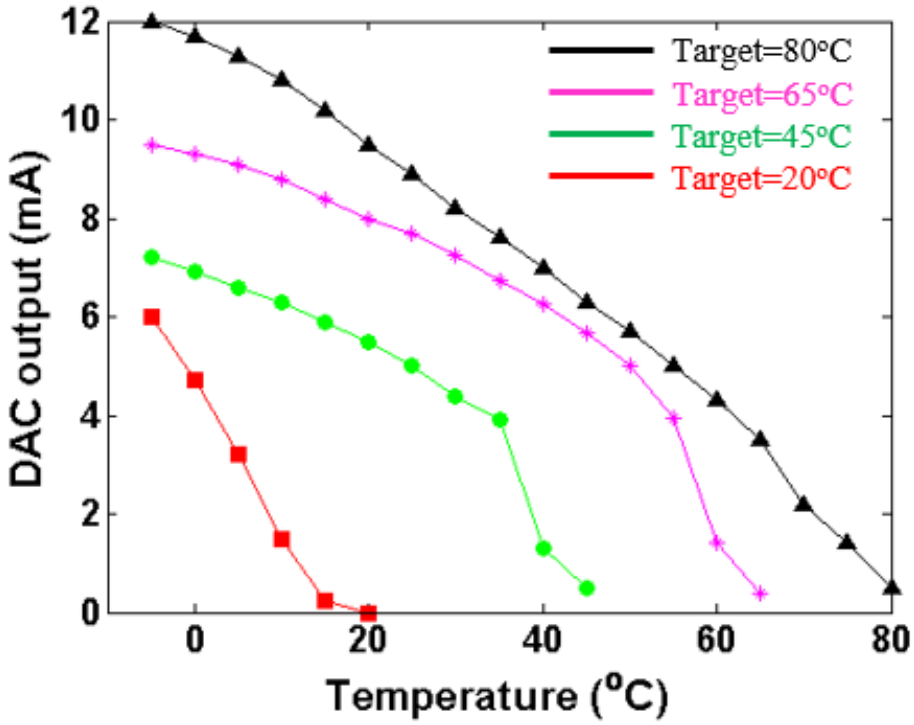



Figure 4.37 Output current variation of the DAC over temperature change with various target setting.

This oven controlled temperature compensation system is the first fully integrated work fabricated by 65nm CMOS technology with a size of 1.5mm x 2mm. The best test result (±1.55ppm) is obtained when 980mV $V_{DD}$ and a half frequency of the clock from oscillator are used for the system. The power consumption of the oscillator is only 250uW and 2.9mW is required for the other blocks. Compared to other state-of-the art temperature sensors, it achieves highest resolution (150uK). The other benefit is that it does not need calibrations for FBAR as it is a feedback system. Table 4.2 summarizes the performance and compares it with other works.

Table 4.2 Performance summary

| **Performance comparison** | | | | |
|---|---|---|---|---|
| | [36] | [41] | [38] | **This work** |
| Frequency | 582MHz | 1-330MHz | 750MHz | **750MHz** |
| Supply Voltage | 3 | 3.3 | 0.75 | **0.98(TDC)/3.3(DAC)** |
| Power consumption of osc./system | NA | 9.24mW/108mW | 0.45mW/1.1mW | **0.25mW/2.9mW** |
| Heater Power (Max.) | 9mW | NA | NA | **14mW** |
| Size (mm x mm) | 25x25 | 2.02x1.89 | 1.6x0.9(CMOS) 0.8x0.8(FBAR) | **1.5x2(CMOS) 0.8x0.8(FBAR)** |
| Temperature range ($^{o}$C) | -45 to 85 | -45 to 85 | 0 to 90 | **-5 to 90** |
| Stability (ppm) | 2 | ±0.5 | ±3 | **±1.55** |
| Phase noise@1MHz (normalized to 750MHz) | -147dBc/Hz | -124dBc/Hz | -145dBc/Hz | **-140dBc/Hz** |
| Allan deviation@0.1s (ppb) | NA | 5 | 8 | **4** |
| Temp. resolution (mK) | NA | 0.1 | 1.2 | **0.15** |
| No. of trim | NA | 12 | 4 | **2** |
| Tech. | GaAs p-HEMT | 0.18um | 65nm | **65nm** |

# Chapter 5.

# CONCLUSION AND FUTURE DIRECTION

The reference clock is an essential component in most electronic systems. That's why there are always specific requirements such as temperature characteristics and short-term frequency fluctuation (Phase noise). These days each person is using at least more than one portable device, and people connect with each other through wireless communication. Since the amount of data and their speed keep increasing, the environment for such wireless systems is getting increasingly stringent and harsher. More specifically, the noise skirt from reference clock affects the signal integrity of both transceiver and receiver leading to a limiting channel space.

This thesis addressed the issues that challenge the designing of the reference clock, which can achieve both low phase noise and power consumption. To kill these two birds with one stone, Thin-Film Buck acoustic resonator (FBAR) and AlN Contour mode resonator (AlN CMR) are introduced in this study with a novel oscillator architecture. FBAR and AlN CMR is the second to none alternative device to replace Quartz crystal as well as other types of resonators such as SAW (Surface Acoustic Wave). This thesis showed that the introduced oscillator broke up the trade-off between power consumption and phase noise. The AlN CMR device enables us to fabricate different resonance frequency devices on a wafer, and showed lower $Kt^2$ and higher quality factor resulting in lower phase noise. However, the presence of spurious modes made it difficult to optimize the oscillator design that can utilize its high quality factor. This necessitates more effort on future research.

Besides the phase noise requirement in wireless applications such as Wi-Fi, Bluetooth and GPS, frequency stability under temperature change is also a very important specification that needs to be satisfied. Although the introduced oscillator using MEMS based resonator helps to lower phase noise and achieve high figure-of-merit (FOM) compared to other state-of-the art oscillators, the resonator is the main contributor for frequency variation according to the temperature change. This thesis demonstrated the first fully integrated oven control system to mitigate the temperature effect on the reference clock. It showed low frequency drift (1.5ppm) with the highest resolution sensor (150uK), which meets the most stringent requirement for GPS application. As this system does

not require any calibration on the MEMS resonator because of its feedback structure, we can benefit from its characteristics of short test time and time-to-market. It can also lead to lower cost from the product perspective. Although an oven controlled system needs more power consumption than the state of the art capacitor controlled temperature compensation system [38], higher frequency stability and no calibration will definitely compensate this need.

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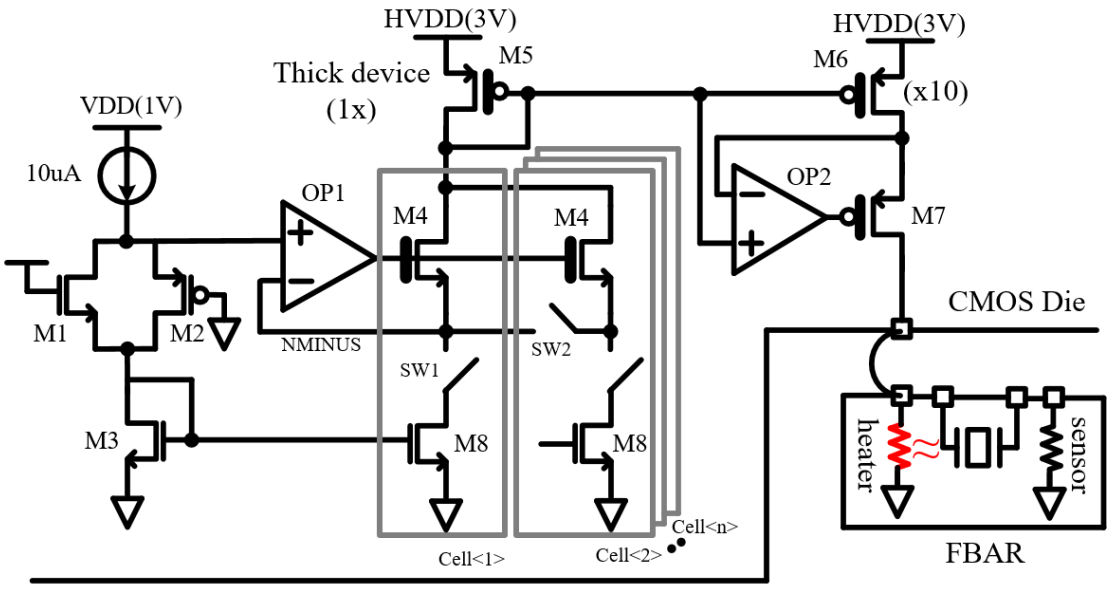
# Appendix A

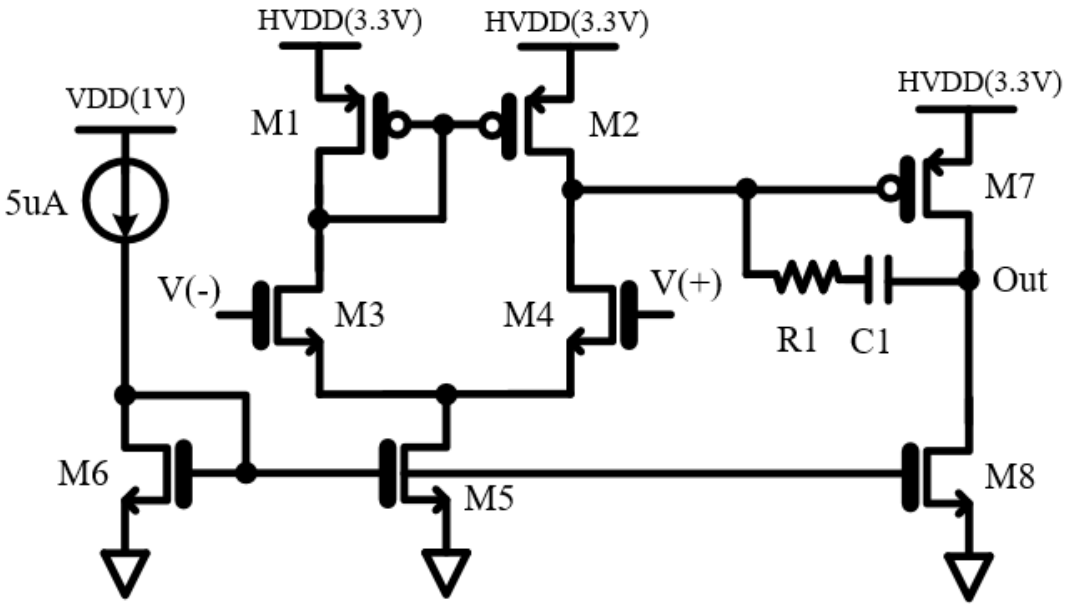
## CURRENT STEERING DAC SCHEMATIC




Block diagram of current steering DAC

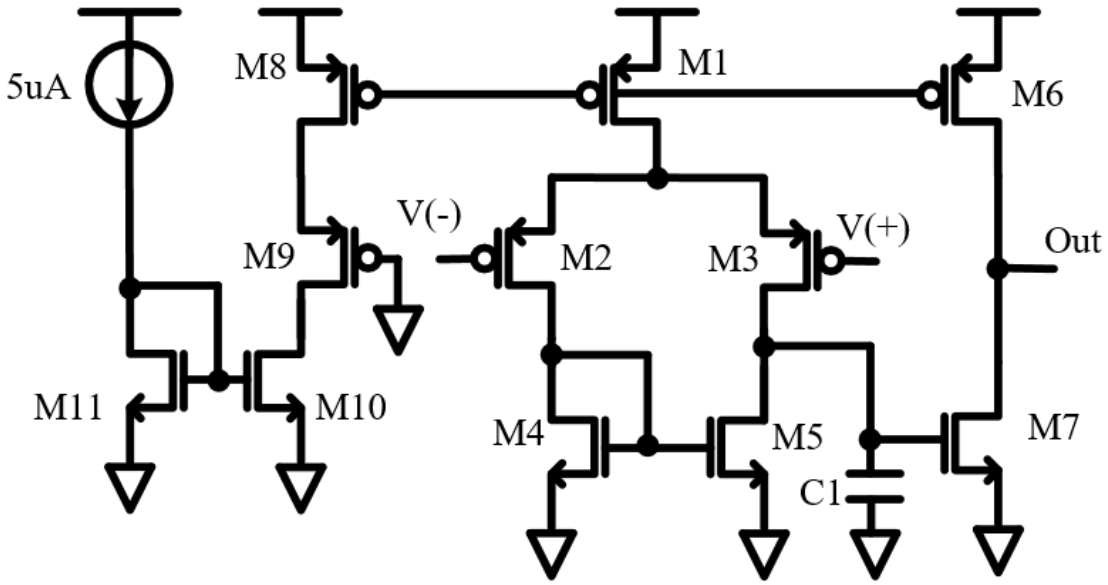
| | Device | Total width (um) | Length (um) | # of finger | # of device |
|---|---|---|---|---|---|
| M1 | nch(1V) | 10 | 0.08 | 2 | 1 |
| M2 | nch(1V) | 10 | 0.08 | 2 | 1 |
| M3 | nch(1V) | 2 | 0.2 | 1 | 1 |
| M4 | 2.5V thick with 3.3od | 40 | 0.5 | 20 | 2 |
| M5 | 2.5V thick with 3.3od | 40 | 0.4 | 20 | 1 |
| M6 | 2.5V thick with 3.3od | 400 | 0.4 | 200 | 1 |
| M7 | 2.5V thick with 3.3od | 400 | 0.4 | 200 | 1 |
| M8 | nch(1V) | 2 | 0.2 | 1 | 1 |
| SW1 | nch/pch(1V) | 10 | 0.2 | 2 | 1 |
| SW2 | nch(1V) | 5 | 0.08 | 1 | 1 |

*SW1 is a transmission gate with NMOS and PMOS connected in parallel like M1 and M2




Block diagram of OP2

| | Device | Total width (um) | Length (um) | # of finger | # of device |
|---|---|---|---|---|---|
| M1 | 2.5V thick with 3.3od | 40 | 0.4 | 10 | 1 |
| M2 | 2.5V thick with 3.3od | 40 | 0.4 | 10 | 1 |
| M3 | 2.5V thick with 3.3od | 20 | 0.5 | 10 | 1 |
| M4 | 2.5V thick with 3.3od | 20 | 0.5 | 10 | 1 |
| M5 | 2.5V thick with 3.3od | 40 | 0.5 | 10 | 1 |
| M6 | 2.5V thick with 3.3od | 40 | 0.5 | 20 | 1 |
| M7 | 2.5V thick with 3.3od | 120 | 0.4 | 30 | 1 |
| M8 | 2.5V thick with 3.3od | 60 | 0.5 | 20 | 1 |
| R1 | rppolywo (2kohm) | 2 | 10.5 | - | - |
| C1 | mimcap (2.5pF) | 35 | 35 | - | - |




Block diagram of OP1

| | Device | Total width (um) | Length (um) | # of finger | # of device |
|---|---|---|---|---|---|
| M1 | nch (1V) | 10 | 0.4 | 2 | 1 |
| M2 | nch (1V) | 5 | 0.4 | 1 | 1 |
| M3 | nch (1V) | 5 | 0.4 | 1 | 1 |
| M4 | nch (1V) | 2.5 | 0.4 | 1 | 1 |
| M5 | nch (1V) | 2.5 | 0.4 | 1 | 1 |
| M6 | nch (1V) | 50 | 0.15 | 10 | 1 |
| M7 | nch (1V) | 25 | 0.15 | 10 | 1 |
| M8 | nch (1V) | 10 | 0.4 | 2 | 1 |
| M9 | nch (1V) | 10 | 0.4 | 2 | 1 |
| M10 | nch (1V) | 2.5 | 0.4 | 1 | 1 |
| M11 | nch (1V) | 2.5 | 0.4 | 1 | 1 |