Low Power IC Design for Health Sensing

Jingren Gu

A thesis

submitted in partial fulfillment of the

requirements for the degree of

Master of Science in Electrical Engineering

University of Washington

2014

Committee:

Brian P. Otis

Jacques C. Rudell

Program Authorized to Offer Degree:

Department of Electrical Engineering

University of Washington

Abstract

Low Power IC Design for Health Sensing

Jingren Gu

Chairs of the Supervisory Committee:

Professor Brian P. Otis

Department of Electrical Engineering

This work proposes a new time-domain integration method to realize Electrochemical Impedance Spectroscopy (EIS). Unlike traditional EIS systems using Fast Fourier Transform (FFT) or Frequency Response Analyzer (FRA) based on a clean quadrature sinusoid stimulus, A single low-frequency, low-amplitude sinusoid stimulus is proposed by using a sinusoid DAC which fully eliminates the analog filter. The response current is integrated by a switched capacitor circuit which is synchronized by the proposed sinusoid DAC. The integration output is sampled and digitized by an 8-bit SAR ADC. The phase and amplitude information of target impedance can be extracted from the time-domain data. The error caused by harmonic generation in the sinusoid DAC can be suppressed by the time-domain integration. The (1×1.1) mm^2 prototype is fabricated in a 130nm CMOS process. It consumes 10μA from a 1.2V supply. Compared with the existing EIS systems, the test results show that the system can obtain a reasonable error with much smaller area and much lower power consumption.

Table of Contents

List of Figures

List of Tables

ACKNOWLEDGEMENTS

I would like to gratefully and sincerely thank Dr. Brian P. Otis for his guidance, understanding, and most importantly, his full support during my graduate studies at University of Washington. I would like to express my great gratitude to Dr. Jacques C. Rudell for his support and advice for my graduate study and research.

I would like to thank the Department of Electrical Engineering at University of Washington for giving me the opportunity to pursue my Master and work as a research assistant. I would like to specially thank the National Science Foundation for financial.

I am particularly grateful to all the colleagues in the Wireless Sensing lab for their input, great support and valuable discussion. I would like to thank Huanfen Yao for her help in the EIS project an Andrew R. Lingley for his help in the FMOS project. Without their support and help, I would not have achieved the current research progress.

Finally and most importantly, I would like to thank my family, and my friends, especially Sonia, Yu, and Peggy for their unending support and encourage

Chapter 1: Introduction

1.1 Background

Contact lenses are commonly considered medical devices and can be worn to correct vision. Reports show that more than 30 million people in the United States wear contact lenses [1]. We have been exploring the use of a contact lens as a platform to directly access tear fluid and realize non-invasive monitoring of human health. The conceptual diagram of the system is shown in Fig. 1.1. The proposed contact lens is equipped with a miniature antenna to harvest energy from incoming radio frequency (RF) radiation. It incorporates circuitry to control and read out the sensors, and integrates a miniature RF telecommunication module to convey the information to the outside world. A fully integrated active contact lens system for wirelessly and continuously monitoring glucose levels has been proposed [2]. In the current project, we continue to develop the function of this new interface with the human body for bacterial biofilm monitoring. A miniature electrochemical-impedance spectroscopy (EIS) sensor has been fabricated and validated to realize bacterial biofilm detection [3]. This work presents a complete, fully-integrated on-chip EIS system that can commensurate with the biosensor to realize continuous monitoring of microbial keratitis on a contact lens.

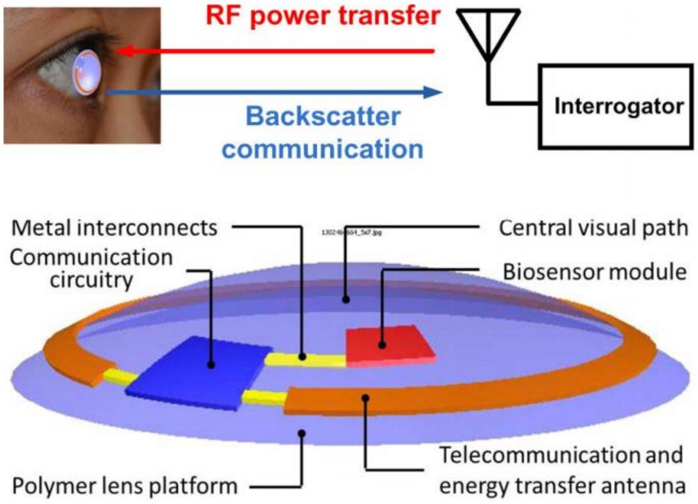


Figure 1.1 Conceptual diagram of an active contact lens system for wireless health monitoring [2].

1.2 Bacterial biofilm on contact lens

About 125 million people in the world wear contact lenses. It has been demonstrated that wearing contact lenses continue to be a significant risk factor for the development of acute sight-threatening corneal infections (microbial keratitis). The incidence rate reported is approximately 25.4 per 10,000 per year. With millions of individuals wearing contact lenses, even a small percentage of complications can constitute a major public health problem.

External ocular structures are frequently challenged by a variety of potentially pathogenic microorganisms. A few microbes can occur in the tear film and further invade and penetrate the intact epithelium of the conjunctiva or cornea, resulting in an infection. When an infection has started in one layer of the eye, it spreads to adjacent layers and tissues quite rapidly. Without proper and timely remedial action, it can lead to devastating and permanent damage to the functional integrity of the eye [4]. Sometimes, it can lead to blindness in 24 hours.

The involvement of microbes and their biofilms on the surfaces of contact lenses have been reported [5]. There is a slime consisting of organic molecules, lipids, and proteins deposited from tears on the contact lenses. It provides the surface for the microbe to bind and absorb. The attachment may lead to the development and growth of a bacterial biofilm on the contact lenses, resulting in a microbial keratitis. The two main bacteria causing microbial keratitis are *P. aeruginosa* and *S. aureus* [4]. If we are able to detect the formation of the two kinds of bacterial biofilms, early alarm can be made to the wearers and help promote early remedial action of microbial keratitis.

1.3 Electrochemical Impedance Spectroscopy for Biofilm detection

A wide variety of methods have been developed to realize biofilm detection based on optical, electrochemical, piezoelectric, and magnetic transducing systems. Among them, EIS represents a powerful method. EIS-based biosensors have the advantages of fast response, easy combination with microfabrication processes, and prospect for minimization of the devices.

The electrical property of an EIS sensor interface can be modeled as a complex impedance, as shown in Fig.1.2. In the model, R_Ω includes the ohmic resistance of the electrolyte solution and does not vary with the changing frequency. C_d is the capacitance of the double layer. R_{ct} is the charge-transfer resistance, existing if a redox probe is present in the electrolyte solution. W stands for the Warburg impedance, which results from the diffusion of ions from the bulk electrolyte to the electrode interface. It can be simplified into a resistor as the application process represents a mass transfer.

When biofilm forms on a sensor, the complex impedance is modified [6]. A small-amplitude and variable-frequency sinusoid is applied between sensor electrodes to allow tracking of complex impedance changes and, thus, biofilm formation. By comparing the amplitude and phase difference between the input signal and its response current, impedance information is acquired [7].

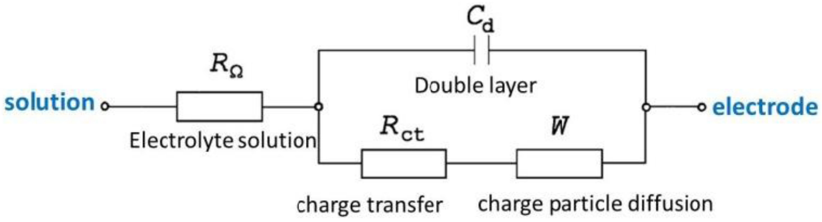


Figure 1.2 The general equivalent circuit for EIS [8].

According to the equivalent model in Fig. 1.2, the real part and the imaginary part of the impedance can be expressed as below. Note that the Warburg impedance has been neglected in the calculation since in this situation the charge-transfer resistance R_{ct} is dominant.

$$Z' = R_\Omega + R_{ct} / \left(1 + \omega^2 C_d^2 R_{ct}^2\right)$$

$$Z'' = -\omega C_d R_{ct}^2 / \left(1 + \omega^2 C_d^2 R_{ct}^2\right)$$

Applying this theoretical analysis, a typical shape of the impedance spectrum is presented as the form of a semicircle path (red dashed line) of the Nyquist plot, shown in Fig. 1.3.

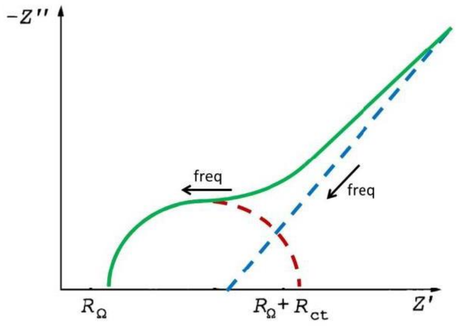


Figure 1.3 The schematic impedance spectrum presented in the form of a Nyquist plot [8].

In an electrochemical cell with a redox probe, there is a charge-transfer process across an interface. The bacterial cell attachment or the biofilm formation on the electrode surfaces would prevent the interfacial electron-transfer kinetics and increase the electron-transfer resistance. The difference of obtained resistance R_{ct} could provide the information about the surface cells or biofilms [3].

1.4 EIS based biosensor

For detection based on electrochemical impedance spectroscopy, a three-electrode design was employed here for the first generation of microbe sensors. As shown in Figure 1.4 (a), the sensor is designed as a zigzag shape for future encapsulation in contact lenses. Three large pads (2 mm × 4 mm) are used to make electrical connection with an external potentiostat. The sensor is composed of a large Au reference electrode (~3.2 mm^2) and two interdigitated Au electrode arrays, each having 48 fingers of 40 μm × 400 μm, with a spacing of 40 μm, as shown in Figure 1.4 (b). The key feature of the interdigitated design is to achieve a large active area and to improve the sensitivity [3].

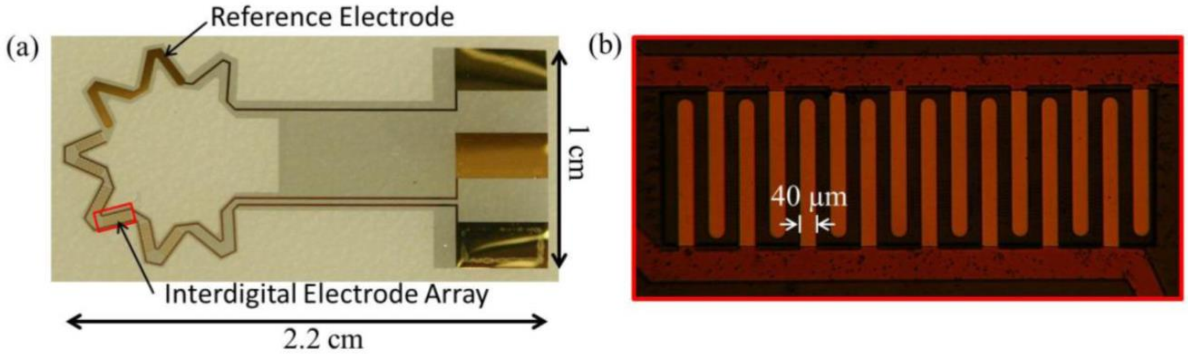


Figure 1.4 The design of the microbe sensor for E. coli: (a) the image of the sensor, (b) the enlarged image of the rectangular area [3].

The proposed EIS-based microbe sensor is tested on *E.coli* using commercial EIS equipment. Fig. 1.5 shows the results of impedance spectroscopy for antibody-treated (AB) and bare-sensor (CTL) samples after incubation in different *E.coli* solutions (0, 10^5, 10^6, 10^7, and 10^8 CFU/mL). It shows the electron-transfer resistance R_{ct} increases obviously from no cell up to 10^7 CFU/mL, but does not increase significantly from 10^7 to 10^8 CFU/mL [3].

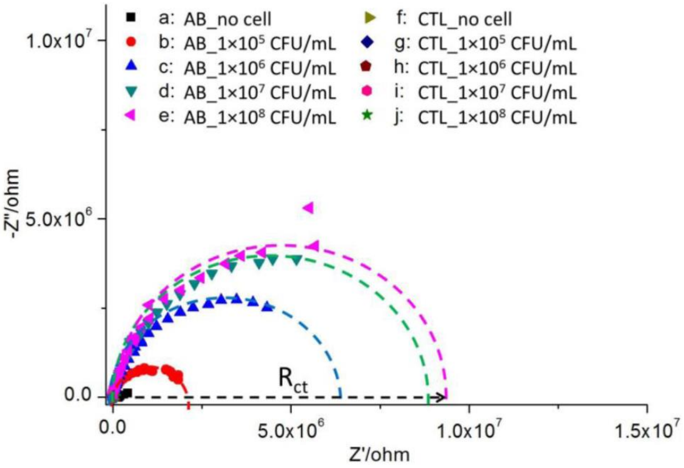


Figure 1.5 Impedance spectroscopy results of an antibody-treated sensor (AB) and bare sensor (CTL) in different concentrations of E.coli [3].

From Fig. 1.5, we can arrive at the conclusion that R_{ct} varies from 1 MΩ to 10 MΩ. This range can be used to design and test the EIS system.

1.5 Conclusion

In order to realize biofilm monitoring on contact lens, a fully-integrated biofilm detection system commensurating with a biosensor needs to be accomplished. The detection method of EIS has been selected because of its advantages. A functional EIS-based biosensor has been fabricated and validated [3]. An EIS circuitry system will be described in the following chapter. It will be validated to be able to co-work with the proposed biosensor.

Chapter 2: Methodology

2.1 Introduction

In this chapter, the common ways of realizing EIS on a chip, fast Fourier transform (FFT) and frequency–response analyzer (FRA), are discussed. To solve the disadvantages of the existing topologies, a new detection method is proposed. Based on the proposed time-domain integration method, the system's immunity to harmonics is effectively improved.

2.2 State of Art

First of all, the requirements of the EIS system to be wearable/implantable can be summarized as below:

1) Able to extract phase and amplitude information,
2) Small area and low power for the whole system,
3) Sinusoidal stimulus with ~10 mV and frequency range of ~100 Hz to ~10 kHz,
4) Reasonable error.

For EIS, the two most common ways are FFT, shown in **Error! Reference source not found.** and FRA, shown in Fig. 2. 2 [9]. These two ways will be discussed in detail below.

2.4.1 FFT

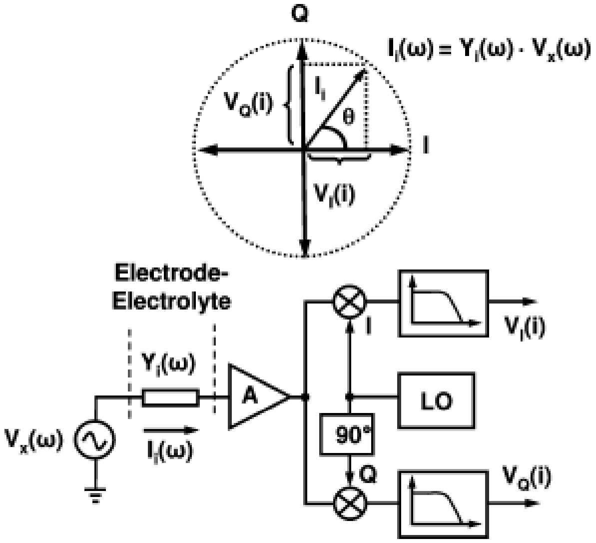


Figure 2.1 System architecture of the FFT method [10].

In order to explain the FFT method, we first assume that the input signal is:

$$V_x(\omega) = V_x \sin(\omega \mathrm{x})$$

After going through the target conductance $Y(\omega)$ and then being amplified by a tans-impedance amplifier (TIA), the response signal can be expressed as

$$V_i = AV_x \,|V_Y|\sin(\omega t + \theta) \ ,$$

where A stands for the gain of the TIA. If the output is mixed with its input signal $\sin(\omega t)$ and the quadrature of the input signal $\cos(\omega t)$, we can arrive at:

$$V_I(\omega) = V_I \cdot V_x = AV_X \,|V_Y|\sin(\omega t + \theta)\sin(\omega t) = \frac{AV_X\,|V_Y|}{2}[\cos(\theta) - \cos(2\omega t + \theta)] \qquad ,$$

$$V_Q(\omega) = V_Q \cdot V_X = AV_X \,|V_Y|\sin(\omega t + \theta)\cos(\omega t) = \frac{AV_X\,|V_Y|}{2}[\sin(\theta) + \sin(2\omega t + \theta)] \qquad .$$

If we use a low-pass filter to remove the high-frequency component, the reflections of the response signal on real and imaginary axes are obtained. Then phase information θ and absolute information Y_ω of the target conductance (or impedance) can be extracted through the equations as below:

$$|Y_i(\omega)| = \frac{\sqrt{V_I^2(i) + V_Q^2(i)}}{A \cdot |V_x(\omega)|}$$

$$\angle Y_i(\omega) = \tan^{-1}\left(\frac{V_Q(i)}{V_I(i)}\right)$$

The advantage of the method is its fast speed. However, the method is sensitive to harmonics. Assume that the input includes harmonics and can be expressed as:

$$\mathrm{V_{in}} = \mathrm{A_1}\sin(2\pi\mathrm{f} * \mathrm{t}) + \mathrm{A_3}\sin(2\pi * 3\mathrm{f} * \mathrm{t}) + \cdots$$

After going through the conductance Y (ω) and ideal TIA with a gain of G, the signal after a TIA is shown as below. (Here consider only the real part for simplicity; the imaginary part is similar.)

$$\begin{aligned}\mathrm{V_{real}} &= [\mathrm{GY_1A_1}\sin(2\pi\mathrm{f} * \mathrm{t} + \emptyset_1) + \mathrm{GY_3A_3}\sin(2\pi * 3\mathrm{f} * \mathrm{t} + \emptyset_3) + \cdots] * [\mathrm{A_1}\sin(2\pi\mathrm{f} * \mathrm{t}) \\ &\quad + \mathrm{A_3}\sin(2\pi * 3\mathrm{f} * \mathrm{t}) + \cdots] \\ &= \mathrm{GY_1A_1^2}/2 * \cos(\emptyset_1) + \mathrm{GY_3A_3^2}/2 * \cos(\emptyset_3) + \cdots\end{aligned}$$

The equation above indicates that the high-frequency components will also fall at DC, contributing to the error of the system. Note here that $\mathrm{Y_f}$ also increases with frequency. Therefore, this method requires a pure sinusoidal input. As a result, power- and area-hungry filters need to be designed after the sinusoid generator. Therefore, most existing works used external equipment [10] or off-chip components [11] to ensure a clean stimulus.

2.4.2 FRA

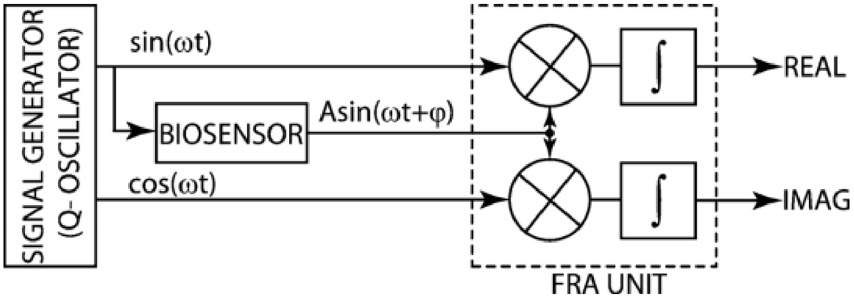


Figure 2.2 System architecture of FRA [12].

Similarly with the FFT method, the FRA method requires quadrature mixing. Additionally, it adds integration following the traditional QI mixing in order to eliminate high-frequency components at the mixer output. The signal after integration can be expressed as:

$$\begin{aligned}
Real &= \int_0^T \; Asin(\omega t + \phi) \times sin(\omega t)\,\mathrm{d}t, \\
&= \int_0^T 0.5 \times (A\cos(\phi) + \cos(2\omega t + \phi))\,\mathrm{d}t, \\
&= \frac{0.5T}{\pi} \times A\cos(\phi) \\
Imag &= \int_0^T A\sin(\omega t + \phi) \times \cos(\omega t)\,\mathrm{d}t, \\
&= \int_0^T 0.5 \times (A\sin(\phi) + \sin(2\omega t + \phi))\,\mathrm{d}t, \\
&= \frac{0.5T}{\pi} \times A\sin(\phi)
\end{aligned}$$

Through this method, the low-pass filters following the quadrature mixing in FFT can be omitted. However, it still requires a clean stimulus since mixing is still conducted. The harmonics, after mixing with itself or its quadrature still generates DC at output, which cannot be eliminated through integration. This problem — pointed out in the FFT method — is not solved. Additionally, the identical quadrature sinusoid generator is still needed on-chip, which is difficult, especially for EIS applications. Additional details will be given in the sinusoid-generator chapter.

2.5 The Proposed Detection Method: Time-domain Integration

Unlike traditional EIS systems which use a quadrature sinusoid stimulus, we propose a low-frequency, low-amplitude sinusoid stimulus, which is realized through a sinusoid DAC without the need for analog filtering. The error caused by harmonic generation can be suppressed through integration in detection. The proposed system is shown in Fig. 2.3. The stimulus is generated by a sinusoid DAC and the response current is integrated through a switched-capacitor integrator. The system is controlled through synchronized digital controls on the chip. A ring-oscillator VCO provides a fully-integrated clock for the system.

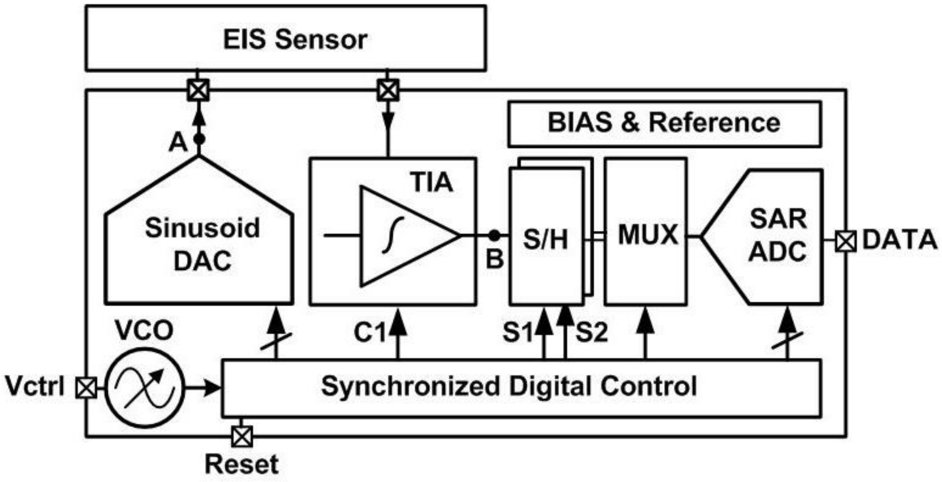


Figure 2.3 Block diagram of the proposed EIS system.

2.5.1 Integration-based TIA

After integration, the sinusoid property is kept with a phase shift of 90 degrees. Assume that a sinusoid current with harmonics is fed into an integrator with an integration capacitor of C_{int}. The input current can be expressed as:

$$\mathrm{I_{in}} = Asin(\omega t) + Bsin(2\omega t) + Csin(3\omega t) + \cdots$$

After integration over the capacitor C_{int}, we can arrive at the ouput as below:

$$V_{out} = \int \frac{I_{in}dt}{C_{int}} = -\frac{1}{\omega C_{int}}\left[Acos(\omega t) + \frac{B}{2}\sin(2\omega t) + \frac{C}{3}\sin(3\omega t) + \dots\right]$$

$$= \frac{1}{\omega C_{in}}\left[Asin(\omega t - 90) + \frac{B}{2}\sin(2\omega t - 90) + \frac{C}{3}\sin(3\omega t - 90) + \cdots\right]$$

The result above indicates that the high frequency components are degraded with a ratio of 1/N (N is the number of harmonics). In terms of a transfer function, a Bode plot of an ideal integration system is shown in Fig. 2.4. The slope is –20 dB/dec, indicating a first-order, low-pass filter at zero. The phase shift is constantly –90, indicating a sinusoidal property after integration in all frequencies. On the whole, the linearity of the system with the switch-capacitor integrator is greatly increased.

From another point of view, it helps relieve the requirements on a sinusoidal generator. In the current design, even if there are harmonic components in the stimulus sinusoid, the output error will not be apparent because of the suppression of the high-frequency component in the TIA.

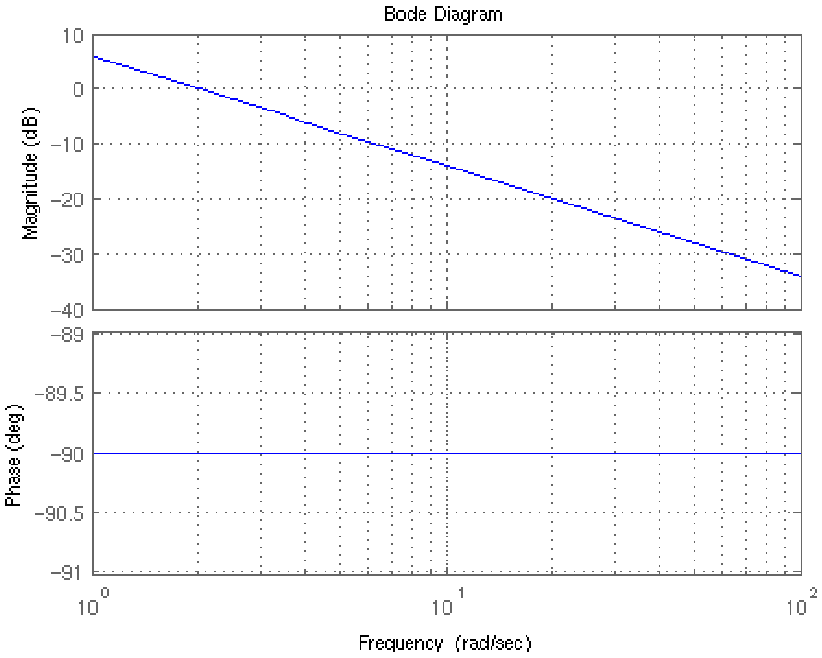


Figure 2.4 Bode plots of an ideal integrator with a gain of 2 in DC.

2.5.2 Time-domain integration detection

Based on the integration method discussed above, a time-domain integration detection method is proposed here. As shown in Fig. 2.3, the system realizes time-domain detection through synchronizing the stimulus sinusoidal signal and integration output.

The output is then sampled at $\frac{\mathrm{T}}{2}$ and $\frac{3\mathrm{T}}{4}$, where T is the period. The two data include the phase and amplitude information. The process can be explained in a real-time plot of signals in different nodes, as in Fig. 2.5.

To explain the impedance characterization function of the proposed system, the time-domain waveforms of key blocks are shown in Fig. 2.3. Assume the generated sinusoid signal at node A in Fig. 2.3 is expressed as:

$$V_A = V_{amp}\sin(2\pi f * t).$$

At the output of the EIS impedance sensor, the response current can be expressed as:

$$I_{in} = I_A \sin(2\pi f t + \emptyset).$$

After integration on capacitor C_{int} in TIA, the output of the TIA at B is:

$$\mathrm{V_{int}} = \frac{I_A}{2\pi f C_{int}}[\cos(2\pi f t + \emptyset) - \cos(\emptyset)].$$

If the voltage is sampled at T/2 and 3T/4we arrive at:

$$\mathrm{V}_{\frac{\mathrm{T}}{2}} = -\frac{I_A}{2\pi f C_{int}} * 2\cos(\emptyset) \;\; ,$$

$$\mathrm{V}_{\frac{\mathrm{T}}{2}} = \frac{I_A}{2\pi f C_{int}} * [\sin(\emptyset) - \cos(\emptyset)] \;\; .$$

The equations above show that the two samples result in two variables: phase and amplitude of the target conductance (impedance). The phase and amplitude information can be extracted with a simple mathematical calculation, as shown below.

$$I_A = \frac{1}{2} * \sqrt{\left(V_{\frac{T}{2}}\right)^2 + \left(V_{\frac{T}{2}} - 2 * V_{\frac{3T}{4}}\right)^2}$$

$$\varphi = artan(\frac{V_{\frac{T}{2}} - 2 * V_{\frac{3T}{4}}}{2V_{\frac{T}{2}}})$$

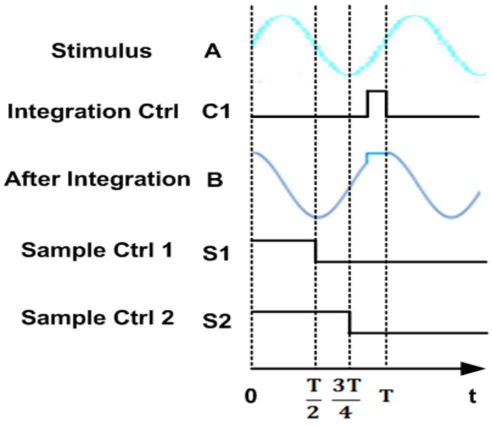


Figure 2.5 Time-domain signals showing system timing.

The effect of harmonics can also be analyzed here. Assume that the input signal is

$$\mathrm{V_{in}} = A_1 \sin(2\pi f * t) + A_3 sin(2\pi * 3f * t) + \cdots$$

After going through the conductance Y(ω), and an ideal integrator with a gain of G_f. For the fundamental tone, the output after a TIA is:

$$V_{out} = -G_f[A_1Y_1(cos(2\pi ft + \emptyset_1) - \cos(\emptyset_1)) + \frac{A_3}{3}Y_3(\cos(3 * 2\pi ft + \emptyset_3) + \cos(\emptyset_3) \ldots]$$

and at $\frac{T}{2}$,

$$\mathrm{V}_{\frac{T}{2}} = 2G_f[A_1Y_1 \cos(\emptyset_1) + \frac{A_3}{3}Y_3\cos(\emptyset_3) \ldots]$$

And at $\frac{3T}{4}$,

$$\mathrm{V}_{\frac{T}{2}} = 2G_f[A_1Y_1 \cos(\emptyset_1) + \frac{A_3}{3}Y_3\cos(\emptyset_3) \ldots]$$

With normalized gain for the fundamental tone, the gain for the 3rd harmonic is 1/3 of the gain in the FFT. Generally, the gain for the Nth harmonic is 1/N of the gain in

FFT method. In conclusion, we can increase the system's immunity to harmonics through the proposed time-domain integration detection method.

The suppression of the high-frequency component of the detection section also eases the requirement for a sinusoidal stimulus generator on-chip. As long as the amplitude of high-frequency components in the sinusoidal stimulus are reasonable, the detection circuit can help absorb the error and result in a reasonable error. Details will be discussed later in the section concerning the sinusoidal generator.

Note here that the current direction needs to be considered at this point. For the integration circuit shown below in Fig. 2.6, the output results should be all opposite as if the input current is defined to be positive when current is flowing in, then the voltage on the capacitor C_{int} is negative (referenced to common DC level).

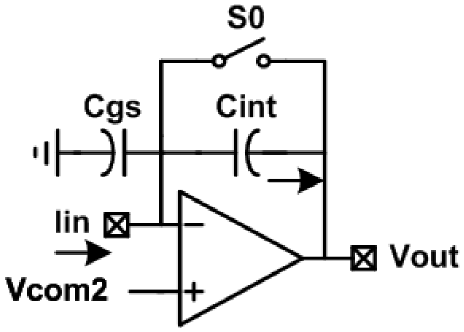


Figure 2.6 Proposed switch-capacitor integrator.

Chapter 3: The Design of EIS system

3.1 Introduction

As described in Chapter 2, a new time-domain integration method has been proposed. The block diagram of the proposed system is shown in Fig. 2.3. In this chapter, the detailed circuit implementations are described. The tradeoffs in design and performance analysis are also discussed.

3.2 Sinusoidal Stimulus

The requirements for the EIS stimulus can be summarized as follows. First, the sinusoidal amplitude added for EIS must be small (~10–30 mV). This ensures the noninvasive process as well as the correctness of the small-signal equivalent model. Second, the amplitude need to be knowable/accurately controlled in order to admit of a calculated impedance later. Third, the sinusoid frequency is a few Hz to kHz.

3.2.1 State of Art

In [10], a quadrature sinusoid is filtered out through the quadrature square wave generated by a divide-by-2 topology. Off-chip low-pass filtering is chosen in [10] considering the low-frequency application.

Disadvantages of this structure are:

a) Inaccurate control of sinusoid;

b) Need for power- and area-hungry filters if the filter is realized on-chip;

c) Need for a good match on quadrature paths.

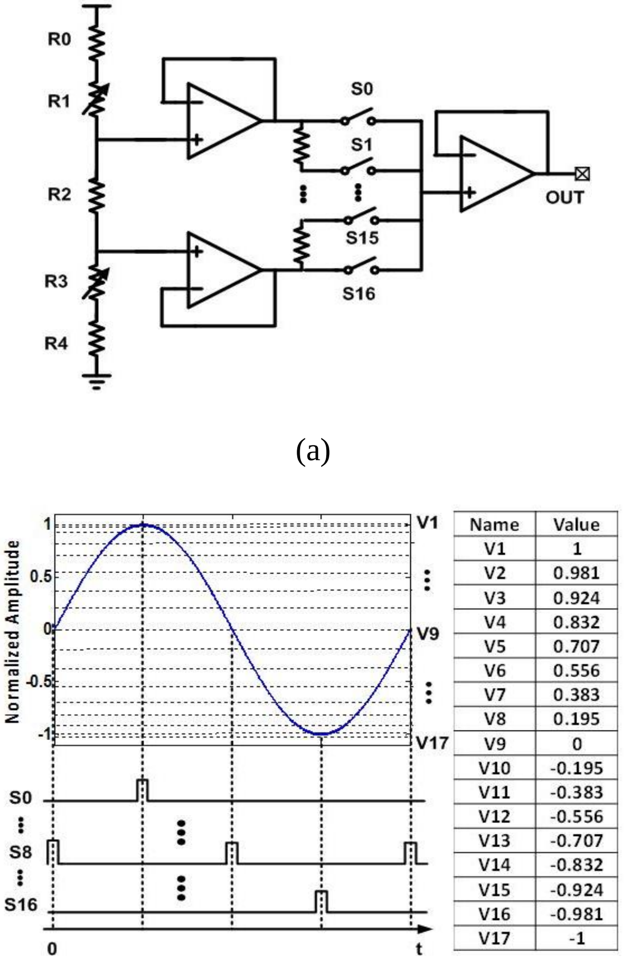
Refs. [12] and [13] both utilize the direct-digital synthesis method. Basically, a reference voltage is generated through a resistor reference [12] or SRAM [13]. However, in [12], a G_m-C filter is used to filter the DAC output, which consumes large power. In [13], no low-frequency harmonic filter is used because the effect of close-in harmonics can be neglected [14]. However, replicas of the DAC output are not considered in the paper. According to the sampling theorem, without any filter, the 2nd main tone at outupt should be the replica generated by sampling. It indicates that the author still used a low-pass filter to filter out the DAC replicas.

3.2.2 The Proposed Sinusoid Stimulus

3.2.2.1 Introduction

This work proposes a direct-digital synthesis sinusoid generator without filter, while controlling the output error at the same time. Based on the proposed method, the error caused by harmonic generation can be suppressed through integration in detection.

Therefore, we propose a low-frequency, low-amplitude sinusoid stimulus, which is realized through a sinusoidal DAC without the need for any analog filtering.



Name	Value
V1	1
V2	0.981
V3	0.924
V4	0.832
V5	0.707
V6	0.556
V7	0.383
V8	0.195
V9	0
V10	-0.195
V11	-0.383
V12	-0.556
V13	-0.707
V14	-0.832
V15	-0.924
V16	-0.981
V17	-1

(a)

(b)

Figure 3.1 The proposed sinusoid DAC: a) basic structure; b) digital control and reference selection.

As shown in Fig. 3.1 (a), a resistor-string DAC is designed. In order to obtain a low-amplitude and mV-accuracy voltage reference, a segmented structure is used. The amplitude is defined by the 1st resistor string. R1 and R3 are used to set the amplitude and output DC value. Buffer stages are used in design to block the load effect by the 2nd stage. The 2nd stage is used to define the 17 voltage references. The 17 voltage references are chosen by sampling the ideal sinusoid with a 32x over-sampling rate, as shown in Fig. 3.1 (b). The reason for choosing a rate of 32 will be related in detail below in sections (2) and (3). Digital control can be generated by a Johnson counter and some simple logic.

The advantages of this topology are [15]:

- Takes full advantage of the availability of almost perfect switches in MOS technologies;
- Simple, fast for < 8 to 10 bits.

The main disadvantages are:

- Long settling time;
- The buffer introduces some mismatch and error.

As the EIS stimulus frequency is not high, the resistor can be large to minimize power consumption. In order to decrease the mismatch of the buffer, a Monte-Carlo simulation was conducted to check the error. According to the Pelgrom model shown as an equation below, the W and L of MOS in buffers are all increased in order to decrease the mismatch. In layout, the two buffers are split into four parts and laid out in the center-symmetric position.

$$\sigma^2(\Delta V_{GS}) \approx \frac{A_{VT0}^2}{WL}$$

3.2.2.2 Analysis of DAC output

The output of an ideal DAC frequency spectrum is shown in Fig. 3.2. The non-ideal DAC may result in 3rd and 5th harmonics at the same time. However, the 2nd highest tone on a DAC output should be the replica caused by sampling rather than the low-frequency harmonics caused by nonlinearity. Therefore, at this point, the replicas should be considered in priority. [15]

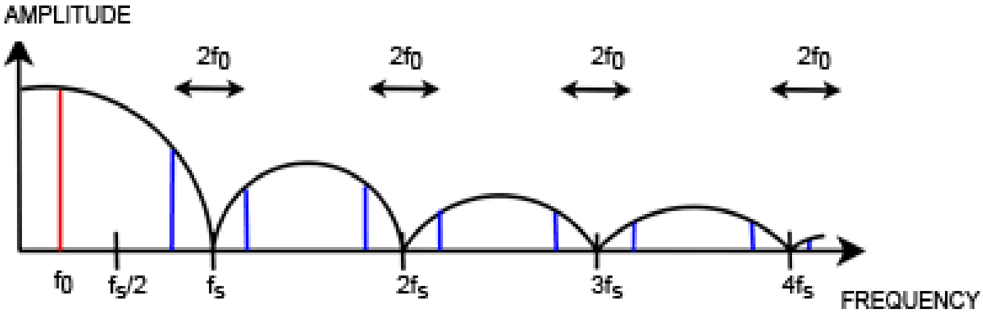


Figure 3.2 Spectrum of DAC output.

To analyze the frequency spectrum of the DAC output, assume unit DAC gain and then the amplitude of main tone can be expressed as:

$$\mathrm{V}_{\mathrm{f}_0} = \mathrm{sinc}(\frac{f_0}{f_s}\pi)$$

Similarly, the 1st replica can be expressed as:

$$\mathrm{V}_{\mathrm{f}_1} = \mathrm{sinc}[\left(1 - \frac{f_0}{f_s}\right)\pi]$$

Therefore, the degradation of replica is:

$$\frac{\mathrm{V}_{\mathrm{f}_1}}{V_{f_0}} = \frac{\mathrm{sinc}[\left(1 - \frac{f_0}{f_s}\right)\pi]}{\mathrm{sinc}\left(\frac{f_0}{f_s}\pi\right)}$$

From the equation above, $\frac{\mathrm{f_0}}{f_s}$ affects the degradation. Moreover, as seen in Fig.3.2, there are multiple replicas. In calculation we can choose the first three main replicas to evaluate the error. To give some example, if $\frac{f_0}{f_s} = \frac{1}{32}$, $\frac{V_{f_1}}{V_{f_0}}$= –32 dB.

3.2.2.1. Analysis of impedance response to stimulus with harmonics

Generally the response current of the impedance is first considered. The impedance can be expressed as:

$$\mathrm{Z(f)} = \mathrm{R_\Omega} + \frac{R_{ct}}{1 + j * 2\pi f * R_{ct} C_d} \approx \frac{R_{ct}}{1 + j * j * 2\pi f * R_{ct} C_d}$$

Therefore, the response current can be expressed as below if the stimulus is $V(f)$.

$$I(f) = V(f) \left[\frac{1}{R_{ct}} + j * 2\pi C_d f \right]$$

We can arrive at the conclusion that the response current increases with the frequency. However, as related in the detection part, there will be a frequency component in the denominator after integration. The output of integration can be expressed as:

$$V_{inte}(f) = V(f) \left[\frac{1}{2\pi f C_{int} R_{ct}} + \frac{j C_d}{C_{int}} \right]$$

Where $\mathrm{C_{int}}$ is the integration capacitor . Therefore, after integration, the output decreases with frequency. And the change of phase and amplitude of the frequency will be different.

3.2.2.3 Analysis of DAC performance considering system error

As related in the parts above, $\frac{f_s}{f_0}$ determines $V(f)$ in the equation for $V_{inte}(f)$. In order to analyze the effect of the sinusoidal DAC, the integration results of an ideal sinusoid and the DAC sinusoid are compared in simulation with the proposed SC integrator. The output error decreases when $\frac{f_s}{f_0}$ increases. The FFT of sinusoid DAC is shown in Fig. 3.3.

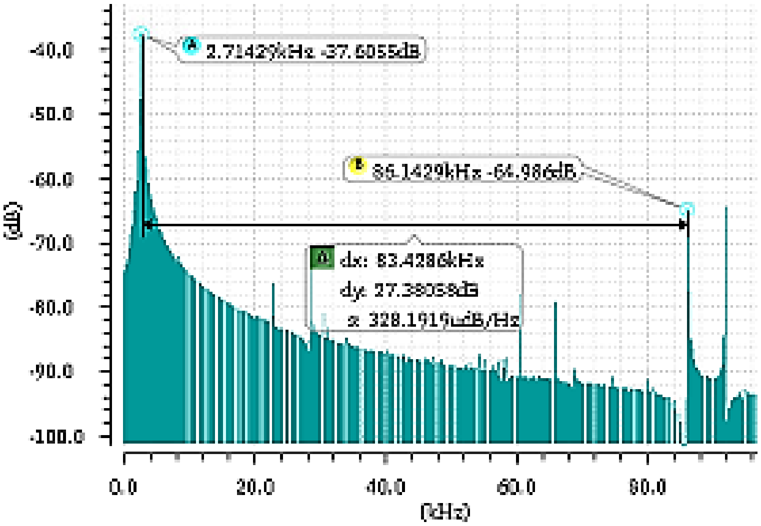


Figure 3.3 FFT of the proposed sinusoid DAC with $f_s/f_0=32$.

With $\frac{f_s}{f_0} = 32$, the output errors are below 5%, which can be seen in Fig. 3.4 and Fig. 3.5. The phase error is more apparent compared with amplitude error. The reason may be due to the calculation method. As we get phase information through the arctan function, a small change of voltage may result in a large phase change.

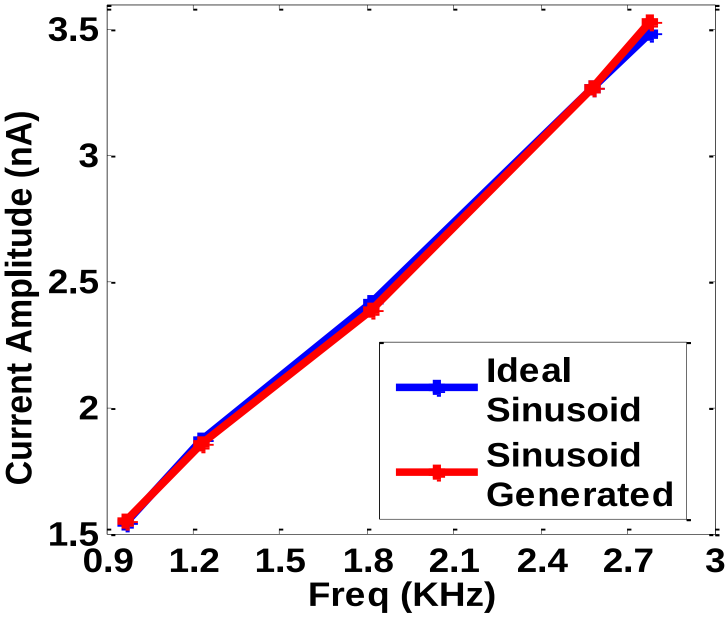


Figure 3.4 Calculated amplitude with ideal sinusoid and sinusoid DAC with fs/f_0=32.

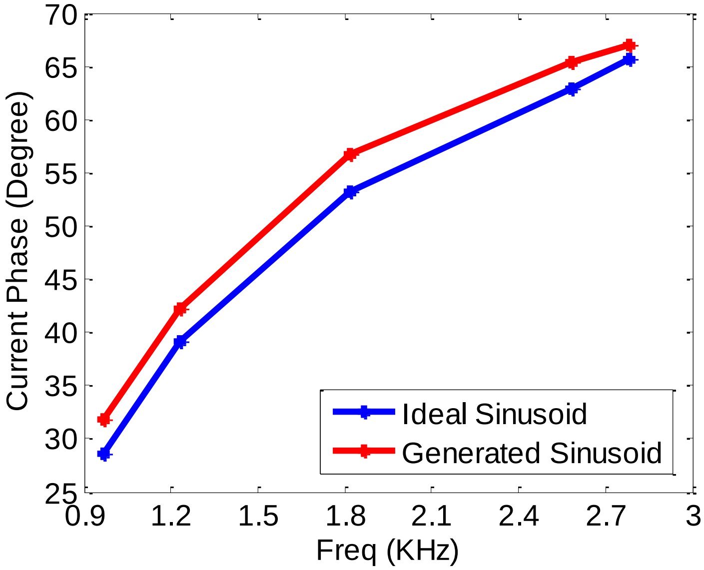


Figure 3.5 Calculated phase with ideal sinusoid and sinusoid DAC with f_s/f_0=32.

3.2.3 Design details

- For the resistor string to define DAC sinusoid references, all the resistor values are unified into a ratio over a unit resistor R_0= 6.16 KΩ, as shown in Table. 3.1.
- The switch in reference selection needs to be designed carefully. The requirement on time constant is not as strict as the application frequency is low. Therefore, the switch size is not large in order to decrease the charge injection effect [16]. Also a small C_{gs} can help decrease the clock feed-trough. As the sampling capacitor is 5 pF, the size of the switch is designed to be within 500 nm x 200 nm.
- For the last buffer, the stability needs to be considered and checked as the load will be large with impedance model. Moreover, as the bandwidth of the last buffer is limited (in design, it is 10 kHz), it has an intrinsic filter effect on the DAC-sinusoid DAC output.

Resistor Name	Number of Unit Resistor
R_1, R_{16}	2
$R_{2,}$ R_{15}	6
$R_{3,}$ R_{14}	9
$R_{4,}$ R_{13}	13
$R_{5,}$ R_{12}	15
$R_{6,}$ R_{11}	17
$R_{7,}$ R_{10}	19
$R_{8,}$ R_9	19

TABLE 1 THE RESISTOR VALUES TO DEFINE 17 VOLTAGE REFERENCES.

- The layout of the DAC sinusoid needs to be carefully designed. The resistor string with switches (Fig. 3.6), the buffers for stage isolation (Fig. 3.7), and the buffer to sensor (Fig. 3.8) are all laid out in symmetric positions.

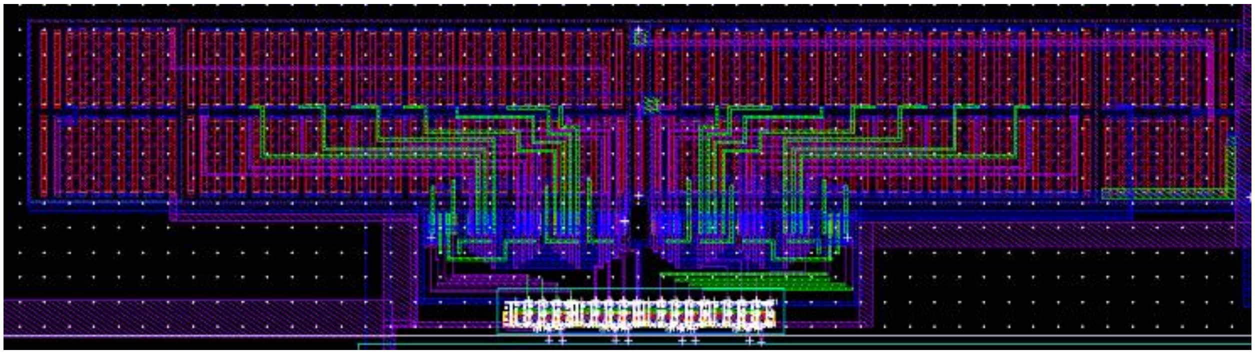


Figure 3.6 The layout of the resistor string with switches.

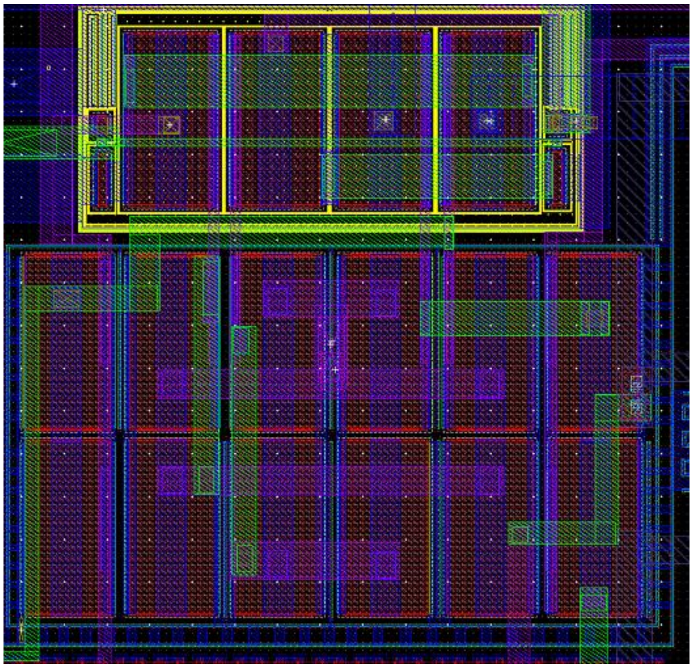


Figure 3.7 The layout of the stage buffers.

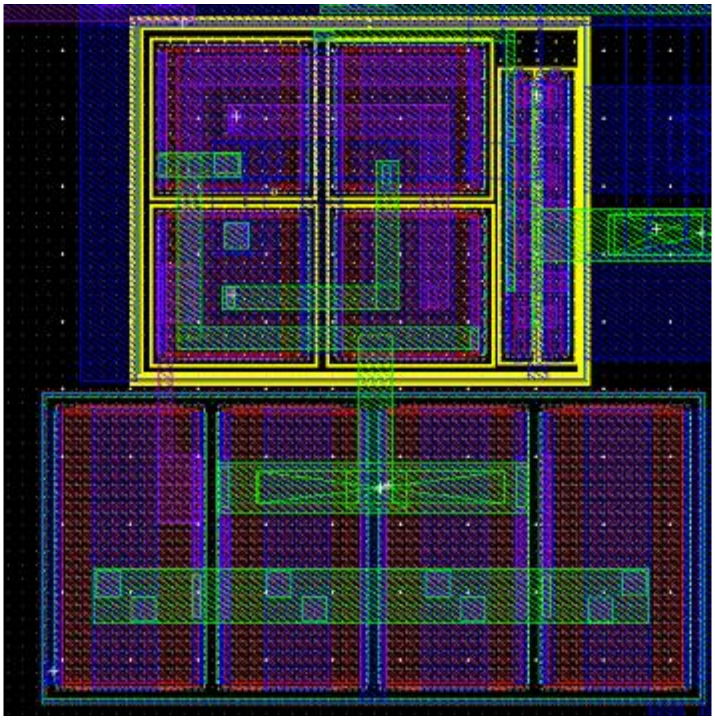


Figure 3.8 The layout of the output buffer.

3.3 Sinusoid Current Detection

3.3.1 Transimpedance Amplifier (TIA)

As related before, the integrator-based transimpedance amplifier has improved harmonic suppression compared with a traditional TIA. A TIA design is shown in Fig. 3.9. The section below describes the detailed design.

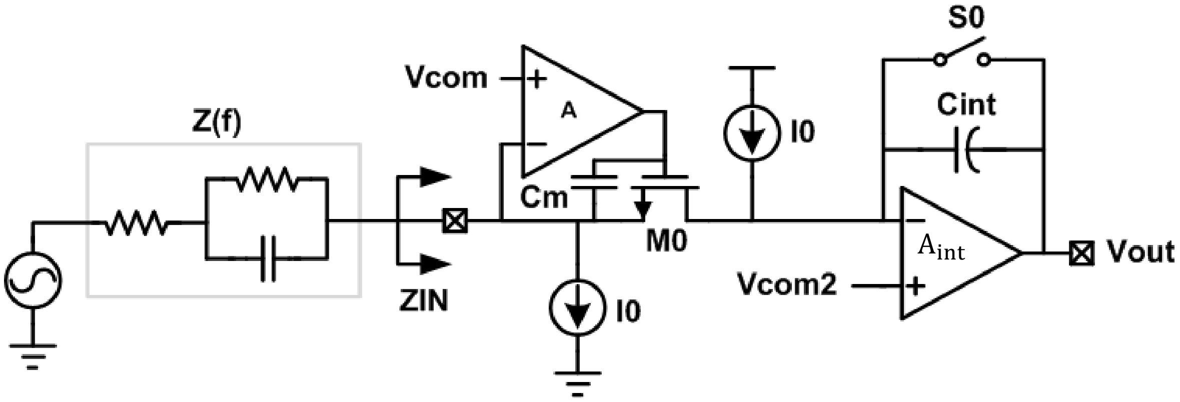


Figure 3.9 The proposed EIS detection circuit.

3.3.1.1 Input Stage

Low input impedance needs to be ensured at the input node in order to keep response current proportional to the target transconductance (impedance). Considering the input of the integrator, the input impedance should be:

$$\mathrm{Z_{in}} = \frac{1}{A_{int} * SC}$$

where $\mathrm{A_{int}}$ is the gain of the amplifier. $\mathrm{A_{int}}$ has been maximized in order to decrease the error introduced by the integration stage. However, the application frequency is low 100 Hz ~ 1 kHz, resulting in ~100 $k\Omega$ input impedance. As the target impedance model changes from 1 MΩ to 10 MΩ, this impedance is not small enough to be ignored.

Therefore, M0 with g_m boosting structure is used here. I0 is mirrored from the current mirror on a chip to bias M0. Through feedback, the input node voltage is also set to V_{com}, which is same as the sinusoid generator. The drain voltage of M0 is set by the bias voltage of the integrator V_{com2}. To ensure that M0 will work in saturation, we make $V_{com2} – V_{com}$ = 200 mV. And, we can know that

$$Z_{in} = \frac{1}{A * gm_{m0}}$$

Assuming that the minimum impedance is around 100 kΩ, to ensure error below 1%, therefore

$$Z_{in} < Z_{im} * 1\% = 1\ k\Omega$$

The noise problem may be brought up here. However, later analysis will demonstrate that the noise of the proposed g_m-boosting structure contributing to the current is negligible.

In order to bias M0, two identical current sources are added here. Cascoded structure is used here to ensure the matching of I_0 Simulation results shows that the mismatch is smaller than 100 pA, which is negligible compared with a nA-scale target current.

A current-biased, active current mirror loaded differential to single-end one-stage OPMAP is used in the design, as shown in Fig. 3.10. The OPAMP together with M0 form a two-stage loop. Stability is ensured through the addition of capacitor Cm.

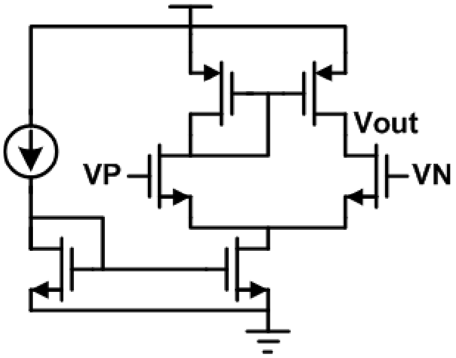


Figure 3.10 The opamp structure for gm boosting.

3.3.1.2 Switched Capacitor (SC) based Integrator

The advantage of using integration-based detection has been explained in the methodology chapter. Here we explain the choice for integration capacitor, switch, and the OPAMP structure.

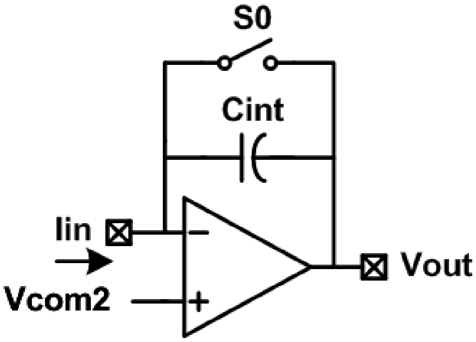


Figure 3.11 The integration stage.

- The choice of integration capacitor:

Considering the gain this integrator, the input stage contributes no gain for current. The whole detection part has gain of

$$\mathrm{G_f} = \frac{1}{2\pi f C_{int}}$$

Considering the input current range ~1–10 nA, with output swing 0.5 V, we set the integration capacitor $\mathrm{C_{int}}$ to be 3.7 pF. $\mathrm{C_{int}}$ is fixed in this system. It can be extended into a capacitor array in order to increase dynamic range.

- Switch

The concern for the switch design here is:

1) Leakage current ($\mathrm{R_{off}}$) in integration mode: considering the integration time 0.1 ms, we need $\frac{1}{\mathrm{R_{off}C}} \ll 0.1ms$.
2) Charge injection during switch on or off: charge injection is relative with size $\mathrm{Q = WLV_{dd}}$

- OPAMP structure

Here a two-stage OPAMP is chosen, as shown in Fig. 3.12, in order to increase gain and decrease the error caused by limited gain. Miller compensation is conducted in the two-stage OPAMP in order to ensure stability of the OPAMP during the reset state. Note that the input MOS size cannot be too large in order to decrease the noise. Detailed analysis will be given later in the section concerning noise.

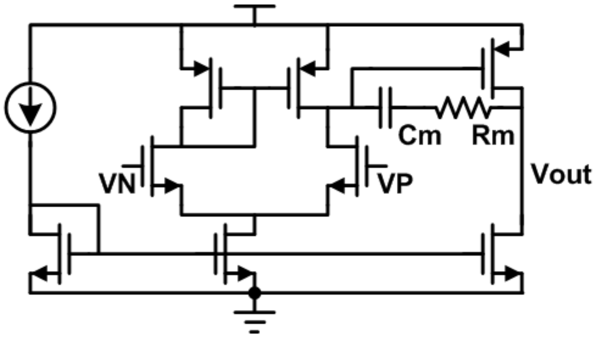


Figure 3.12 The OPAMP structure for integrator.

3.3.2 Noise Analysis for detection circuit

3.3.2.1 Input Stage:

To analyze the noise contribution of the input stage, we first analyze the noise references and then calculate the input referred current noise according to the transfer function.

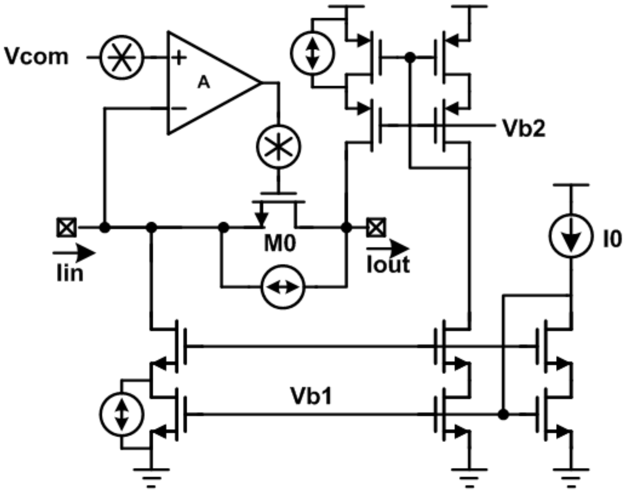


Figure 3.13 The noise source distribution in input stage.

The noise contribution is shown in Fig. 3.13. The main noise sources are thermal and flicker noise because the application frequency is low. Therefore, flicker noise needs to be considered at this point. Detailed analysis is below.

- The Noise of M0：

M0 with current source can be viewed as a cascade structure. As analyzed in [16], when we consider the input referred current, the input node is open, which results in feedback, the current of M0 cancels out its noise current. Therefore the noise of M0 is not contributing to the input referred current.

- The Noise of amplifier A

To simply the analysis, we can see that the input voltage follows Vcom at the input of OPAMP A. Equivalently, the noise of the opamp is added at the input node directly. When we consider the input referred current noise, we need to divide the impedance of the cascoded current source, which is very high. The resulting current noise is also small, because of the large impedance of the cascode current source.

- The Noise of current source I_0

As we open the input node when we calculate the input referred noise, the noise current from current source will add directly to the output current. Therefore, the main noise source for the input stage is the noise from current sources. Noise simulation also demonstrates this conclusion.

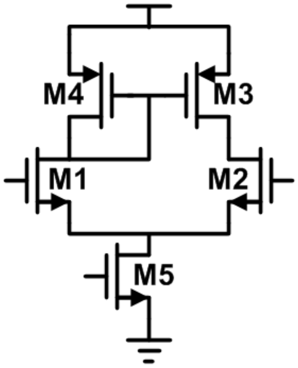


Figure 3.14 The noise source distribution in the two-stage OPAMP.

In order to decrease the noise contribution, two steps are conducted:

1) Push the corner frequency to low frequency by decreasing gm.

   First, because the application frequency is as low as 100 Hz, we push the corner frequency below 100 Hz.

$$\mathrm{As}\ \frac{\mathrm{K_N}}{\mathrm{WLC_{ox}f}} * \mathrm{gm}^2 = \frac{8}{3}\mathrm{KTgm}$$

$$\mathrm{f_c} = \frac{3\mathrm{K_N}}{8\mathrm{WLC_{ox}KT}}\mathrm{gm}$$

So at this point, a large device is chosen and gm is decreased to get low $\mathrm{f_c}$

2) Decrease the thermal noise of the current source by decreasing gm of the top and bottom MOS, as cascoded MOSFETs do not contribute noise at this point.

- Switched-capacitor Integrator

First, consider the noise of the opamp, as the gain of 1st stage is large, the 2nd-stage noise is neglected. The noise source distribution is shown in Fig. 3.14. The input referred noise can be calculated as:

$$\mathrm{V^2_{out_n}} = \frac{2}{3} * 4KT\left(g_{m_3} + g_{m_1}\right) * 2 * \mathrm{R^2_{out}}$$

$$\mathrm{A} = \mathrm{gm_1R_{out}}$$

$$\mathrm{V^2_{n_{in}}} = \frac{V^2_{out_n}}{\mathrm{A}^2} = \frac{16KT}{3g_{m_1}}(1 + \frac{g_{m_3}}{g_{m_1}})$$

Then we need to consider the output noise contributed by the OPAMP. The transfer function needs to be calculated. The equivalent transfer function can be determined from the Fig. 3.15, where C1 stands for the parasitic capacitor

$\mathrm{C_1} = C_{GS_{M1}} + C_{gd_{M0}} + 2 * C_{gd_I}$ and $C_2 = C_{int}$.

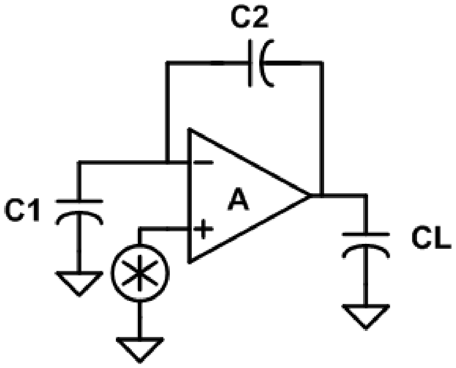


Figure 3.15 The equivalent circuit for the opamp noise-transfer system.

In design, a two-stage OPAMP is designed with Miller compensation, therefore the transfer function of closed loop OTA according to the noise input is:

$$\mathrm{H(s)} = \frac{\mathrm{C_1 + C_2}}{\mathrm{C_2}} * \frac{1}{1+\frac{s}{\omega_0}}$$

where $\omega_0 = \frac{\frac{C_2}{C_1+C_2} g_{m_1}}{C_c}$ and $\mathrm{C_c}$ is the Miller-compensation capacitor.

The noise contributed by the capacitor can be expressed as:

$$\mathrm{V_n^2} = \frac{KT}{C};$$

To compare with the value above, we calculate the integrated noise contributed by the OPAMP as:

$$\mathrm{V_{out}^2} = \int_0^{\infty} V_{n_{in}}^2 H(2\pi f j)^2 \, df$$

$$= \frac{\frac{16\mathrm{KT}}{3\mathrm{g_m}}\left(1+\frac{g_{\mathrm{m_3}}}{g_{m_1}}\right)\omega_0}{4} * \left(\frac{C_1+C_2}{C_2}\right)^2$$

$$= \frac{4\mathrm{KT}}{\frac{3(\mathrm{C_1+C_2})}{\mathrm{C_2}} C_c}\left(1+\frac{g_{\mathrm{m_3}}}{g_{m_1}}\right)$$

From this result, the noise contributed by the OPAMP is determined by $\frac{C_1}{C_2}$ and $\frac{g_{m_3}}{g_{m_1}}$, not g_{m_1}. Therefore, in designing the OPAMP, we should control the size of the input MOS in order to decrease C_1, as well as decrease $\frac{g_{m_3}}{g_{m_1}}$. Note that we still need to decrease the error caused by the finite gain of the OPAMP in integration. Therefore, the tradeoff between input MOSFET size and gain needs to be balanced. Simulation results shows that the main noise contribution of the detection stage is from the current-source bias in the input stage.

Chapter 4: Measurement Results

4.1 Introduction:

This chapter discusses the measured results of the proposed time-domain integration EIS system. Also, the test results are shown and analyzed. Different test methods are discussed and compared.

4.2 Experimental results:

The proposed system was fabricated in a 130nm CMOS process. The die photo is shown in Fig. 4.1. The entire system consumes 10µA with a 1.2V supply. The synchronized digital control signal for the system and the output data are tested with an oscilloscope and the result is shown in Fig. 4.2. DATA_EN is the signal used to flag the start of series data.

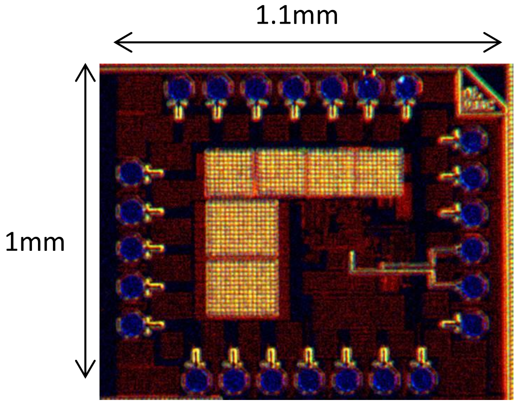


Figure 4.1 Die photo of the EIS chip.

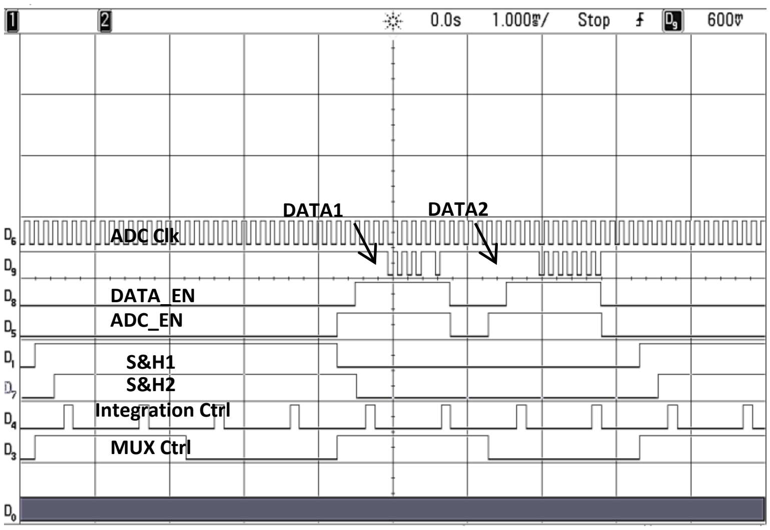
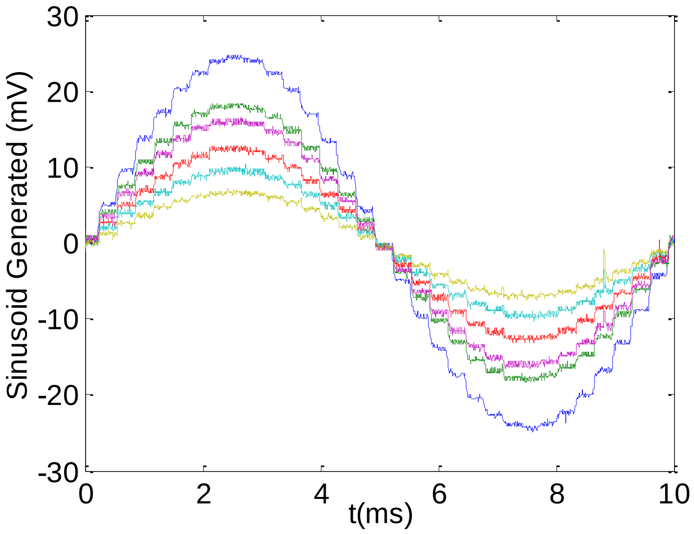


Figure 4.2 The measured clock and timing signal.

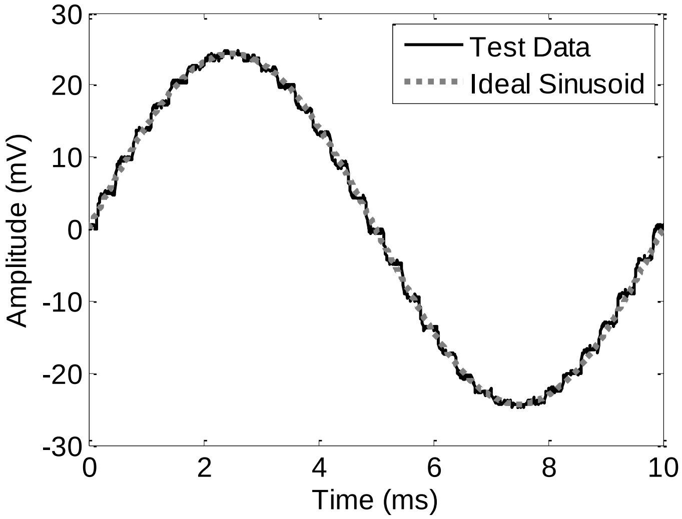
4.2.1 Sinusoid DAC

The sinusoid generated on the chip can be swept from 900Hz to 2.8–kHz. The performance of the sinusoid DAC is shown in Fig. 4.3. Note that the spike at around 7/8 of period in Fig. 4.3 (a) is due to the reset of switch in integrator. The amplitude setting is realized with shift registers which provide test options for the system. The FFT results for the proposed sinusoid DAC are shown in Fig. 4.4. These results are ~~is~~ collected in a time domain span of 500ms. The 500,000 point data file (Fs=1MHz) is processed in MATLAB and the FFT results are obtained. The SFDR for low frequency harmonics is

100 dB. As mentioned in Section III, the omission of a filter in this system, results in replicas of fundamental tones at the output (see Fig. 4.4). The error caused by these replicas can be suppressed by time-domain integration.



(a)



(b)

Figure 4.3 Time domain output of the proposed sinusoid DAC with: (a) output cross amplitude setting; (b) linearity property compared with ideal sinusoid.

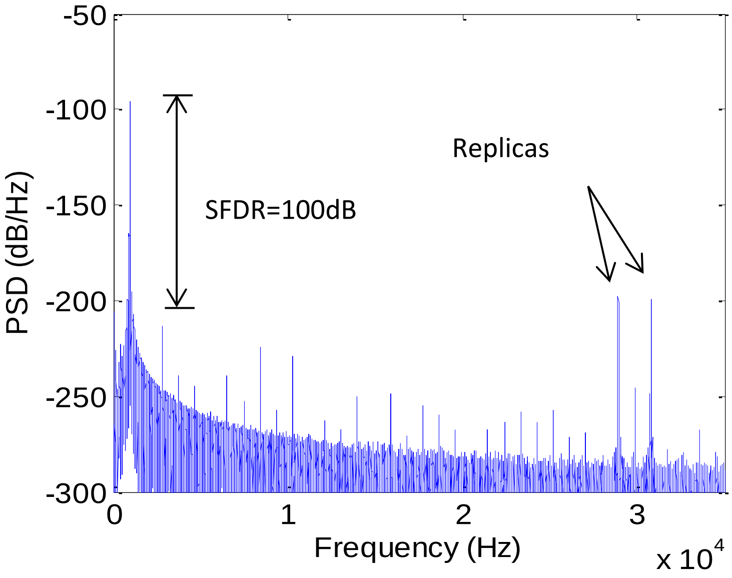


Figure 4.4 FFT of the generated 1KHz sinusoid.

4.2.2 Sinusoid current detection

Before testing the system functionality, both the sinusoid current detector and the integrator need to be validated independently first. In order to check the linearity and gain, a DC current is injected at the inpu using a Keithley current source. Note that to block the large input resistance of the current source, a resistor of 50 KΩ is added between the input node and the Keithley probe.

The test results show~~s~~ that there is a constant leakage current in the sinusoid detection part. By using the Keithley for calibration, the leakage current can be shown to be around 1~2 nA; though this leakage current is not constant from chip to chip. Consequently, leakage current calibration is needed during the test. To achieve this, we can use one of the following two methods:

- Method I: Use the Keithley probe to calibrate the leakage by injecting another DC current to make the integration output flat. This method is easy to conduct. The disadvantage here is that it cannot accurately cancel out the leakage current.
- Method II: This method consists of condunting the experiment twice. The first time including the leakage only and second time including the leakage plus the data. By subtracting the two results, the information with pure data can be obtained. The disadvantage here is that the same test experiment conditioning needs to be verified for both tests.

In the linearity test of TIA, method I is chosen.

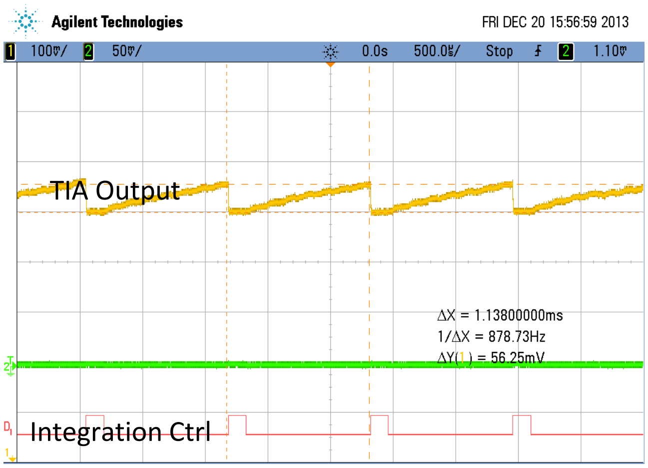


Figure 4.5 The output after TIA.

As discussed here before, the gain of the proposed trans-impedance amplifier is expressed as:

$$G_f = \frac{1}{2\pi f C_{int}}$$

Since the gain is relative with frequency, two test are conducted, one at minimum and one at the maximum frequency of the system. Fig. 4.6 shows the linearity at the target frequency of 2.4 kHz and Fig. 4.7 shows the linearity at the target frequency of 0.8 kHz.

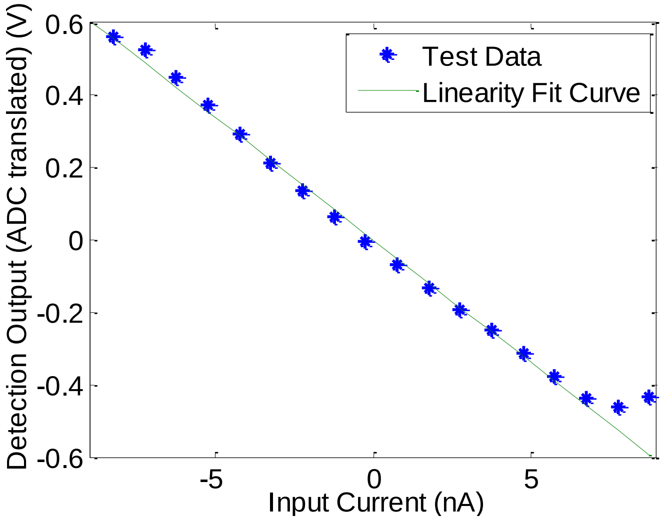


Figure 4.6 The linearity of the proposed TIA working at 2.4 kHz.

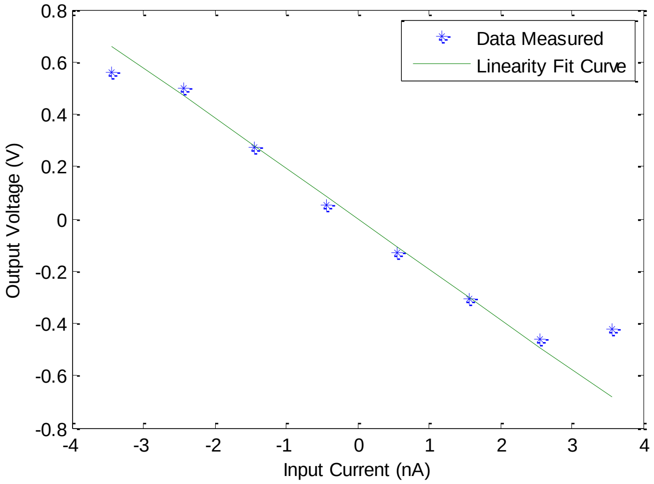


Figure 4.7 The linearity of the proposed TIA working at 0.8 kHz.

4.2.3 Time-domain integration detection with ideal sinusoid stimulus

In order to validate the function of the proposed time-domain detection method, an ideal sinusoid is fed in using a signal generator and synchronized by the on-chip integration control signal, shown in Fig. 4.8.

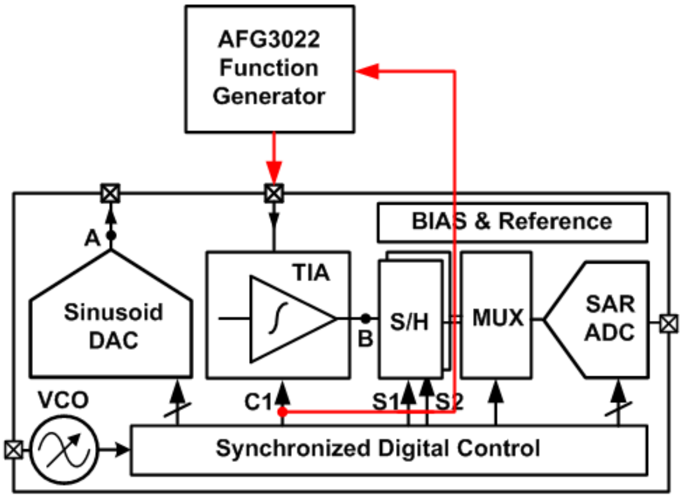
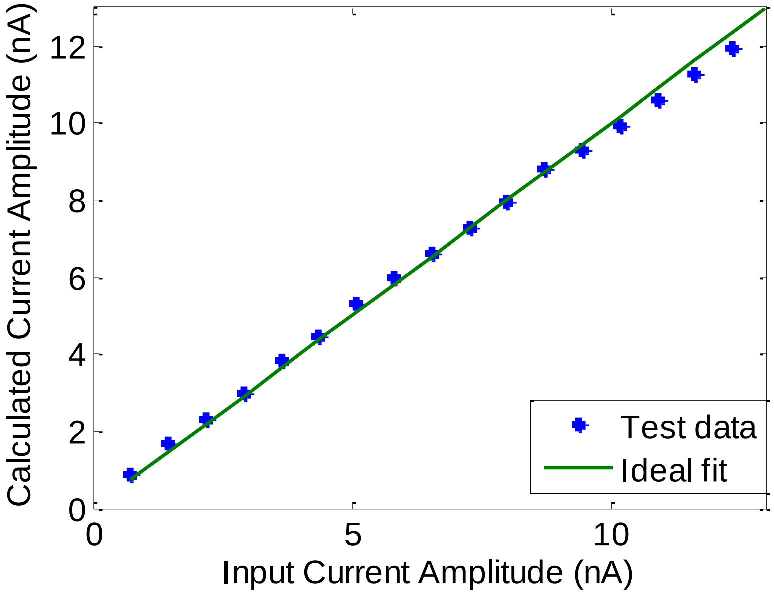
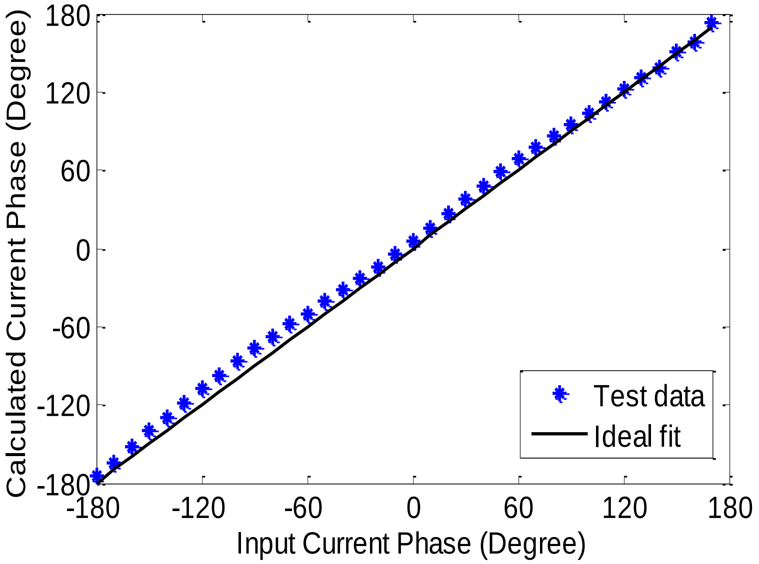


Figure 4.8 The test diagram of the function test.

The system functionality is tested by comparing an ideal input with a recovered phase and amplitude from the test results. Fig. 4.9(a) shows the measured current amplitude with a fixed phase and sweeping the input sinusoid amplitude. Figure 4.9(b) shows the measured phase with a fixed amplitude and sweeping the input sinusoid phase. The test error for both, the amplitude and phase, fall below 3%.



(a)

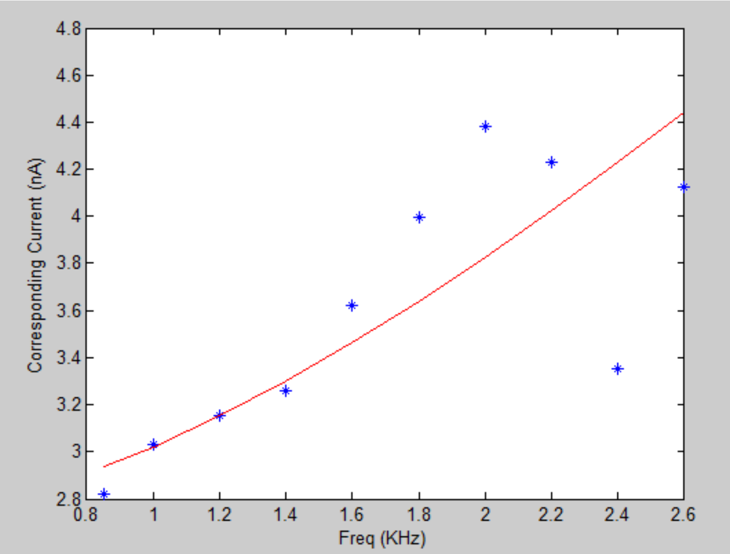


(b)

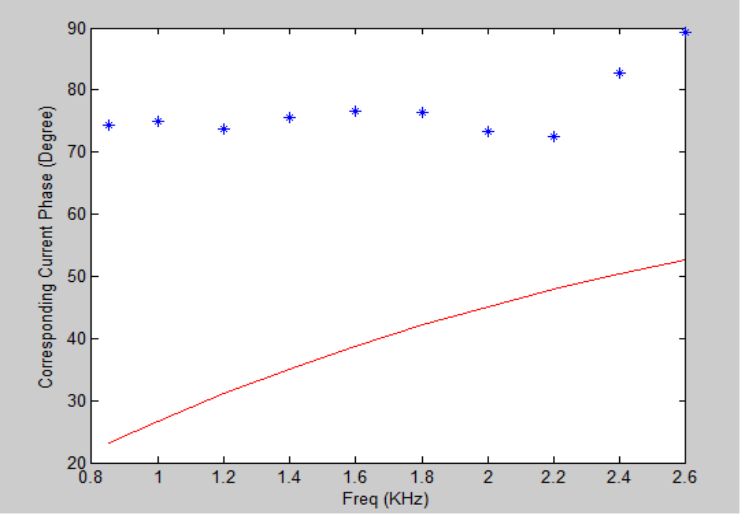
Figure 4.9 Detection test with an ideal sinusoid current and (a) Fixed phase and swept amplitude; and (b) fixed amplitude and swept phase.

4.2.1. System functions with on-chip sinusoid DAC as the stimulus

To realize leakage cancellation, both calibration methods addressed in Part 2) are conducted. System functionality with both, the sinusoid generator and the sinusoid detector, are tested with a sensor model consisting of on-board discrete resistors and capacitor. Data is collected with R=100 Ω, Cd=20 pF and Rd=4 MΩ as the sensor model. With calibration method I, the test data is collected and shown in Fig. 4.10. For this test, it can be seen that the resulting phase error is quite large. With calibration method II, the test data are collected and shown in Fig. 4.11. The amplitude error is below 5% and the phase error is below 8%. These results demonstrate that the error caused by the sinusoid generator's nonlinearity has been mitigated by the proposed method.



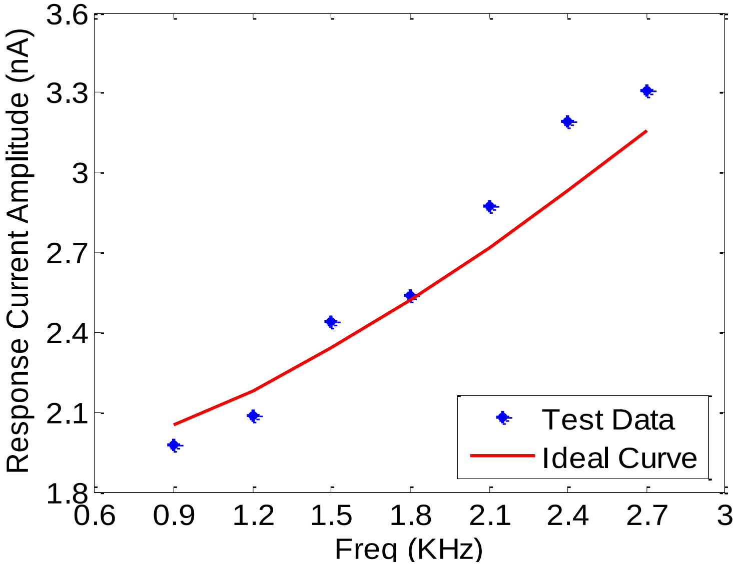
(a)



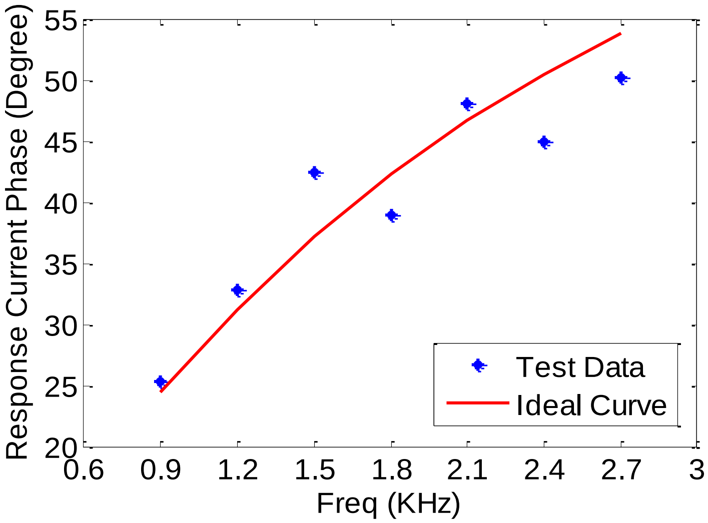
(b)

Figure 4.10 System test data with on-board circuit model of sensor with calibration method I: (a) target conductance (impedance) amplitude change according to frequency sweep; (b) target conductance phase change according to frequency sweep.

Based on Fig. 4.11, the second calibration method exhibits higher accuracy. Moreover, the probe on detection node can also affect the output buffer of sinusoid DAC, resulting in error



(a)



(b)

Figure 4.11 System test data with on-board circuit model of sensor with calibration method II: (a) target conductance (impedance) amplitude change according to frequency sweep; (b) target conductance phase change according to frequency sweep.

3.1 Summary

The performance of the proposed EIS system is summarized in Table I. Table I provides a comparison of the presented design compared to existing impedance spectroscopy systems. The design presented in this work achieves the lowest power and smallest area with a reasonable error.

Table 2: PERFORMANCE COMPARISON OF IMPEDANCE SENSING INTERFACE

System	**This work**	**ISSCC 10** [10]	**JSSCC 09** [11]	**TBCAS 12** [12]
Technology	0.13μm	0.35μm	0.5μm	0.13μm
Power/Channel	12μW	0.85mW	0.3mW	42uW
Area	$0.6mm^2$	$4mm^2$	$2.25mm^2$	$1.68mm^2$
Supply	1.2V	3.3V	3V	1.2V
Resolution	8b	16b	8b	9.3b
Stimulus Generator	Yes	No	No	Yes
Off-chip Auxiliary	No	Yes	Yes	Yes
Error	8%	N.A.	0.3%	8%

Chapter 5: Conclusion

5.1 Summary of Research results

A new EIS test method is proposed in this work. Based on the proposed time-domain integration method, a fully-integrated EIS system is designed, fabricated and tested. The proposed system does not require pure quadrature sinusoid stimulus. Thus, analog filters are omitted while accuracy is ensured, resulting in a lower system complexity and power consumption. The impedance spectroscopy microsystem was fabricated in 130 nm CMOS technology. The entire system consumes 10μA with a 1.2 V supply.

5.2 Future Work

Though the initial goals for this project were generally met, there are areas of future research that would benefit the EIS detection system on contact lenses as a whole. These areas will be introduced in this section.

5.2.1 Noise of the system

The noise of the system can be improved through the technique of Chopper or Correlated Double Sampling. Through the two techniques, 1/f noise can be decreased and the offset of opamp can be eliminated.

5.2.2 Dynamic range of the system

The gain of the detection part now depends on the stimulus frequency in the current system. That is mainly due to the fact that a fixed capacitor is used at the switched capacitor integrator. To increase the dynamic range of the system in the future, the integration capacitor can be extended from the single fixed capacitor to a capacitor array controlled by digital system. Additionally, K_{vco} of the oscillator on the chip can be increased to obtain a larger main clock frequency range.

5.2.3 System Architecture

Currently the system is powered by wired DC. An RF front end can be designed and added to the existing system to realize a wireless-sensing EIS system.

References

[1] Nichols, Jason J., et al "*ANNUAL REPORT: Contact Lenses 2010*". January 2011.

[2] Y. Liao, H. Hao, A. Lingley, B. Parviz, and B. Otis, "*A 3-uW CMOS Glucose Sensor for Wireless Contact-Lens Tear Glucose Monitoring*," IEEE Journal of Solid-State Circuits, Vol. 47, No.1, Jan 2012.

[3] Huanfen Yao, "*Biosensors Embedded in Contact Lenses for Human Health*". PhD Dissertation, University of Washington 2013.

[4] C. R. Mahon and G. Manuselis, *Textbook of diagnostic microbiology*, 2nd ed. Philadelphia: Saunders, 2000.

[5] Zegans, M. E., Becker, H. I., Budzik, J., & O'Toole, G., "*The role of bacterial biofilms in ocular infections*". DNA and Cell Biology, 21(5-6): 415-420 2002.

[6] T. Kim, J. Kang, J. H. Lee, and J. Yoon, "*Influence of attached bacteria and biofilm on double-layer capacitance during biofilm monitoring by electrochemical impedance spectroscopy*," Water Research, vol. 45, pp. 4615-22, Oct 1 2011.

[7] A. J. Bard and L. R. Faulkner, *Electrochemical methods: fundamentals and applications*, 2nd ed. New York: Wiley, 2001.

[8] E. Katz and I. Willner, "*Probing biomolecular interactions at conductive and semiconductive surfaces by impedance spectroscopy: Routes to impedimetric immunosensors, DNA-Sensors, and enzyme business*," *Electroanalysis*, vol. 15, pp. 913-947, Jul 2003.

[9] E. Barsoukov and J. R. Macdonald, *Impedance Spectroscopy: Theory,Experiment, and Applications*, 2nd ed. Hoboken, NJ: Wiley, 2005

[10] A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, and A. Hassibi, "*A CMOS Electrochemical Impedance Spectroscopy Biosensor Array for LAbel-Free Biomolecular Detection*," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International, 2010, vol. 92, pp. 130–131.

[11] C. Yang, S. R. Jadhav, R. M. Worden, and A. J. Mason, "*Compact Low-Power Impedance-to-Digital Converter for Sensor Array Microsystems*," Solid-State Circuits, IEEE Journal of, vol. 44, no. 10, pp. 2844–2855, 2009.

[12] H. Jafari, L. Soleymani, and R. Genov, "*16-Channel CMOS Impedance Spectroscopy DNA Analyzer With Dual-Slope Multiplying ADCs*," IEEE Transactions on Biomedical Circuits and Systems, vol. 6, no. 5, pp. 468–478, Oct. 2012.

[13] Rairigh, D ; Xiaowen Liu ; Chao Yang ; Mason, Andrew J., "*Sinusoid signal generator for on-chip impedance spectroscopy*", 2009 Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on.

[14] M. Min and T. Parve, "*Improvement of lock-in bio-impedance analyzer for implantable medical devices,*" IEEE Trans. Instrum. Meas., vol. 56, pp. 968–974, 2007.

[15] Douglas A. Mercer, "*Digital to Analog Converter Design*", RPI IEEE Student Chapter October 22, 2008.

[16] Razavi, Behzad. *Design of integrated circuits for optical communications*. John Wiley & Sons, 2012.