An Integrated CMOS Passive Transmitter Leakage Suppression Technique for FDD Radios

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Abstract

An Integrated CMOS Passive Transmitter Leakage

Suppression Technique for FDD Radios

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This thesis presents an integrated passive self-interference mitigation (SIM) technique for FDD Radios. A new structure, Four Port Canceller (FPC) serves a dual function as a receiver (RX) input matching network, and provides an auxiliary path from transmitter (TX) to RX, used for leakage cancellation, with minimal penalty on the RX noise figure (NF), power consumption and silicon area.

An example of this technique is applied to the design of WCDMA front-end including the FPC, a low noise amplifier (LNA) and an emulated power amplifier (PA) in a 40nm, 6-metal-layer TSMC CMOS process. A measured TX leakage suppression of more than 20dB is achieved with TX power level from 5 dBm to 30 dBm, over a bandwidth of 5MHz.

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1. Introduction

1.1 Project Overview

The continued demand for higher levels of access and increased data rates for a variety of wireless applications, from mobile smart phone devices to back haul point-to-point communication, continues to drive research towards higher speed, wider bandwidth and lower cost integrated radios. Frequency division duplexing (FDD), rather than time division multiple access (TDMA) standards, provides better network capacity and incurs less cost [1]. However, in a FDD system, since the TX and RX share the same antenna and operate at the same time using a duplexer, a signal with non-negligible power from the TX will "leak" through the duplexer, and appear at the RX front-end. For example, in the WCDMA standard, although a duplexer will significantly suppress the TX leakage signal (up to 50dB), a residual attenuated signal still remains at the receiver input. Thus, the TX leakage is often the largest blocker present at the RX input, making a low-noise and low-power linear receiver design very challenging. This leakage problem is exacerbated by applications such as future cognitive and software-defined radios where the duplex band would ideally be kept to a minimum, to improve spectral efficiency. An off-chip surface acoustic wave (SAW) filter is usually connected between the LNA and down-converter to further suppress the TX leakage. However, these filters are band specific, prohibiting highly programmable solutions. Moreover, additional discrete filters are area inefficient, and increase cost/ power consumption.

1.2 State of Art

Recent efforts have focused on improving RX selectivity in the presence of a self-interfering TX without using any off-chip filters [2-17]. Most of the work has been reported so far using active

methods to do the leakage cancellation including feed-forward filtering [8-9], active two port cancellation [10], LMS adaptive filter [15] and feedback filter [16-17]. All these techniques try to tap the PA output and inject an amplitude adjusted and phase rotated signal into the RX path to cancel the leakage signal. Frequency translational noise cancelling techniques are demonstrated in [2-5] to achieve blocker tolerance, and noise cancelling with a mixer-first topology. Some of the other suppression techniques use a filtering approach[6-7], using either active or passive components.

1.2.1 Frequency Translational Noise Cancelling Technique (FTNC)

The FTNC technique, shown in Fig.1-1, exploits the feature of noise-cancellation with the passive-mixer architecture to simultaneously achieve blocker-tolerance, without degrading the noise performance and providing an input match. Concurrent matching and noise cancelling is achieved using a common-gate device to provide a real 50 Ohm impedance and sense the input as a current signal, while a much larger common-source device, sized for low input-referred noise, sense the input as a voltage signal. After that, the common-gate and common-source devices are combined into balance voltages at RF. However, in this approach, the large voltage gain is present across the wide bandwidth, which may cause the receiver to saturate in the presence of strong blockers. The FTNC, as shown in Fig 1.1, is an advanced topology from the traditional noise cancelling model. Instead of converting a current into a voltage at RF, a passive mixer immediately down-converts the RF current to baseband. Therefore, the out-of-band blockers never experience any voltage gain, which will not saturate the receiver [2-5]. A resulting prototype chip in [2] is functioning from 80MHz to 2.7GHz and achieves a 2dB noise figure, which degrades to 4.1dB in the presence of 0dBm blocker. However, the mixer-first topologies suffer from an inherent LO

leakage issues. Large LO leakage will be reflected back from the antenna and leads to DC offset issues in the direct conversion receiver.

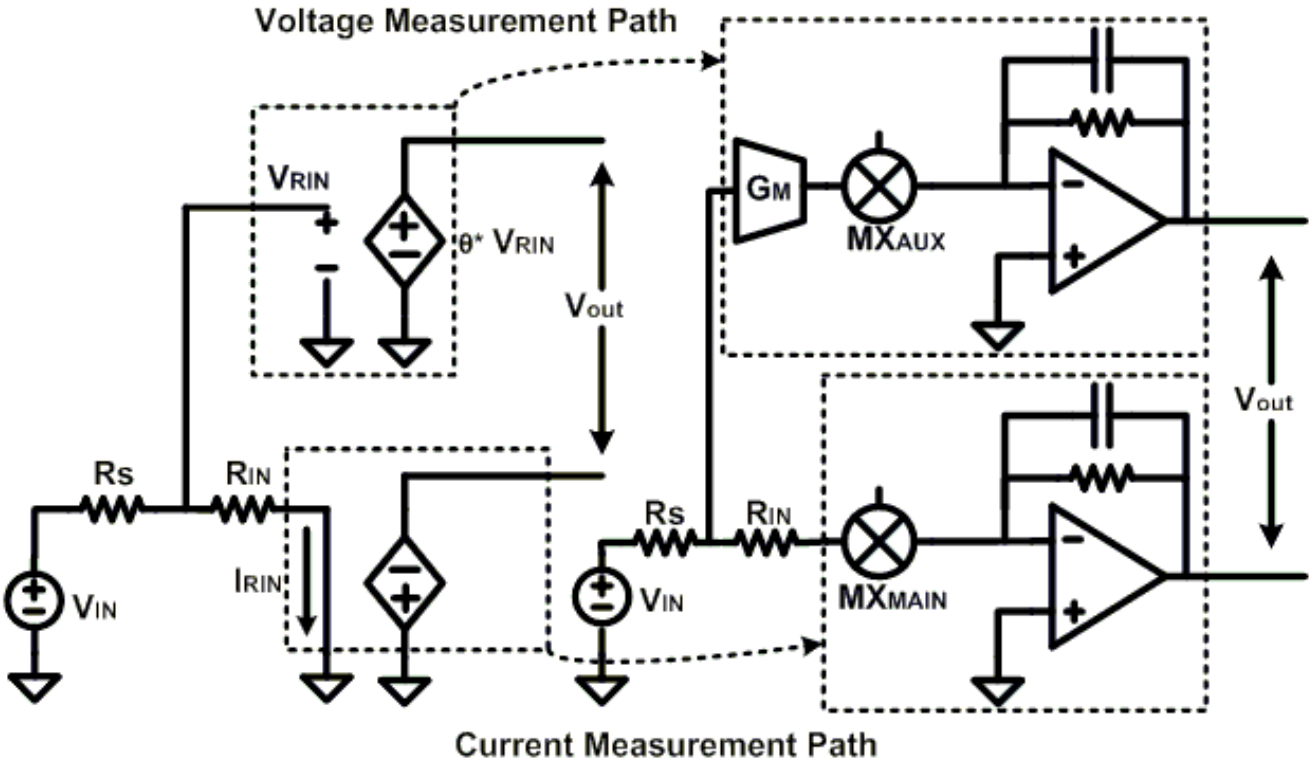

Fig.1-1 Frequency Translational Blocker Tolerant Noise Cancelling Receiver (FTNC-RX)

1.2.2 Active Filtering Technique (AFT)

An active bandpass sink filter, shown in Fig.1-2, was proposed in [6-7] after the down-conversion mixer, filtering out the down-converted TX signal without affecting the desired baseband RF signal. The bandpass sink filter, which is made up of another down-conversion passive mixer with a trans-impedance amplifier, creates a low impedance node at the mixer output at the down-converted TX frequency. In [6], a CDMA-2000 receiver is targeted, operating at 1.96GHz, with the TX leakage offset by 80MHz from the receive band. To improve the receiver

selectivity in the absence of the inter-stage RF filter, a sink filter with an impedance Z_{sink} is desired at the mixer output. Z_{sink} provides a large impedance of around 400-450 Ohm at the down-converted RX frequency and a low impedance of approximately 50 Ohm at the down-converted TX frequency [6]. The resulting system shows a cancellation of 6.5dB with 1.8dB noise figure degradation and additional 48mW. Due to the switch resistance and the other parasitic, it becomes difficult to realize Z_{sink} as an extremely low impedance (close to zero) at the TX down-converted frequency, which reduces the TX-leakage suppression. Moreover, the finite bandwidth of the Opamp limits this approach to a narrowband solution.

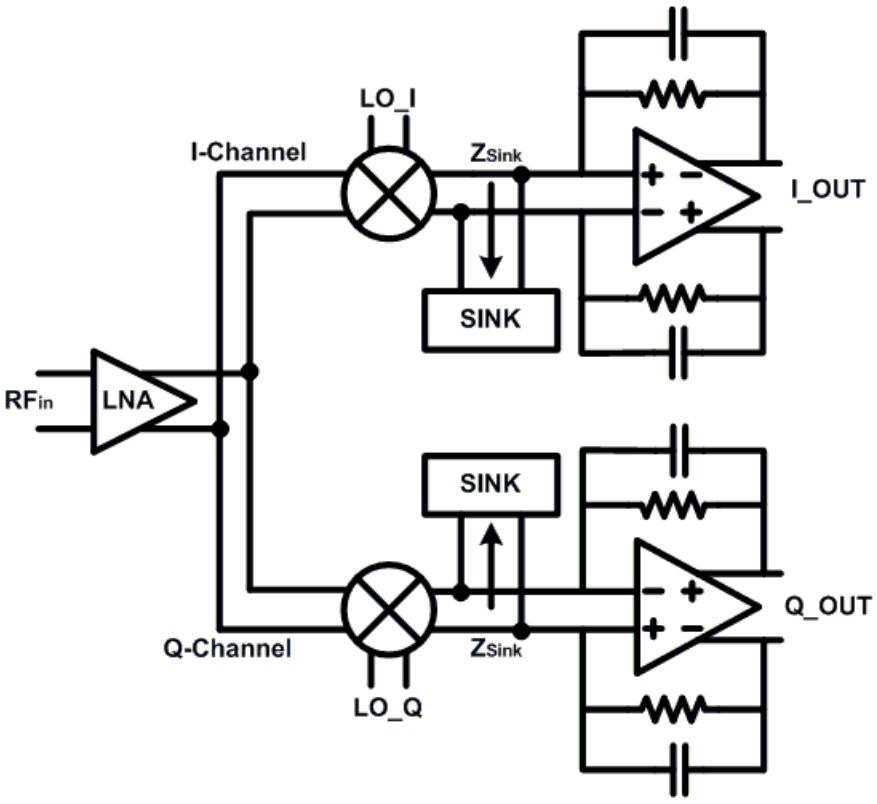

Fig.1-2 An Active Selective Sinking Technique which Filters Out the Down-converted TX signals without Affecting the Desired Baseband RF Signal.

1.2.3 Feed-Forward Filtering Technique

A feed-forward canceller [8-9], shown in Fig.1-3, using a polyphase filter to sample the reference signal from the PA output, then injects an amplitude-adjusted and phase-rotated signal into the LNA output; this was implemented in [8]. This circuit provides a minimum cancellation of 22.5dB over the entire WCDMA TX band with 0.44dB RX noise figure degradation while consuming 18.9mW of power, in the presence of an approximately -25dBm blocker. In the measurement of [8], a 30dB coupler is connected between the vector signal generator and the proposed TX leakage canceller (TXLC), which is mainly made up of an active Gilbert-cell based VGA. However, in a practical system, a PA signal with a high output power (27dBm for cellular PA) will be directly connected to the TXLC. A large voltage swing at the VGA input makes the VGA design very challenging, especially from the perspective of achieving a high the linearity.

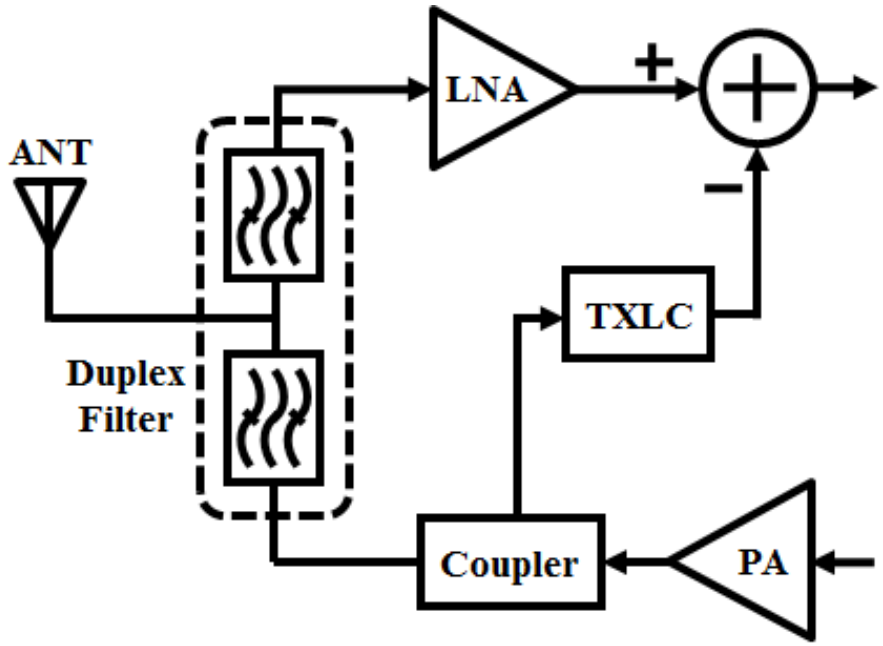

Fig.1-3 Feed-forward Technique which performs TX Leakage Cancellation after LNA

1.2.4 Active Two-Port Cancellation Technique

An active low noise active two-port cancellation technique for TX leakage cancellation, shown in Fig. 1-4, was presented in [10]. In the two-port technique, a current-mode noise cancelling receiver architecture with single-ended common source (CS), common gate (CG) LNA is applied to achieve wideband input matching and low noise. A coupled-TX-signal replica is injected at the gate of the CG device and the drain of CS device of the LNA, which results in a more than 30dB TX leakage cancellation at the RX input and 13dB of TX noise suppression in RX Band with 0.8dB noise figure degradation and additional power consumption of 13-72mW. In [10], the amplitude and phase of the coupled-TX-signal is adjusted by the Cartesian phase rotator. Same as the feed-forward technique discussed above, in a practical system, a TX signal with a high output power will be directly connected to the active phase rotator, leading to a challenged design for the phase rotator.

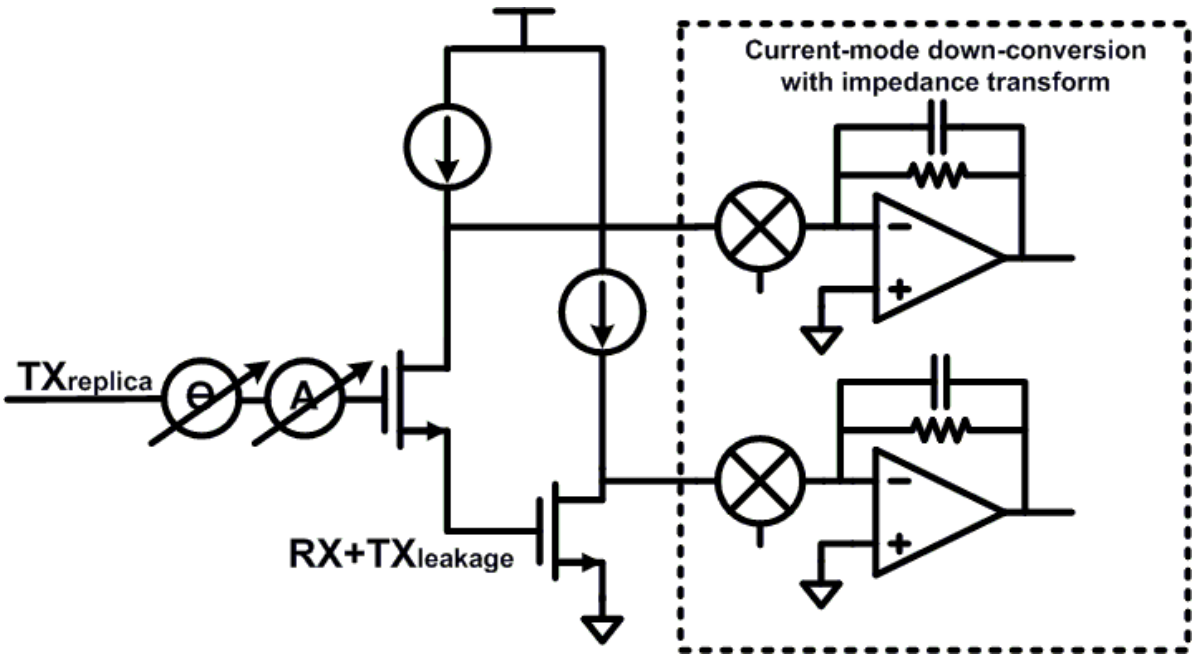

Fig. 1-4 Active Two-Port Cancellation Technique using two path CS-CG LNA

1.2.5 Antenna Cancellation Technique

Another method to perform cancellation is achieved before the signal enters the received signal path. In this approach, the cancellation is achieved through the careful placement of both the TX and RX antennas, such that the TX signal cancels at the RX antenna. This antenna cancellation technique was proposed for self-interference cancellation in [11-13]. The transmitting and receiving antenna are separated by a special distance with respect to the wavelength to demonstrate an electromagnetic cancellation. The idea is shown in Fig.1-5. Perfect cancellation only happens at the center frequency, making it a narrowband solution. Also the cancellation is very sensitive to the on-board EM environment and even the slightest change in the impedance of one antenna relative to the other, will lead to significantly reduction in the amount of leakage cancellation. Moreover, with two or more antennas, the benefits of applying this antenna cancellation technique towards FDD and/or full-duplex systems becomes unclear since similar improvements in spectral efficiency could be achieved through the use of less complicated MIMO antennas in a half-duplex system with less worry about the coupling from the self-interference transmitter.

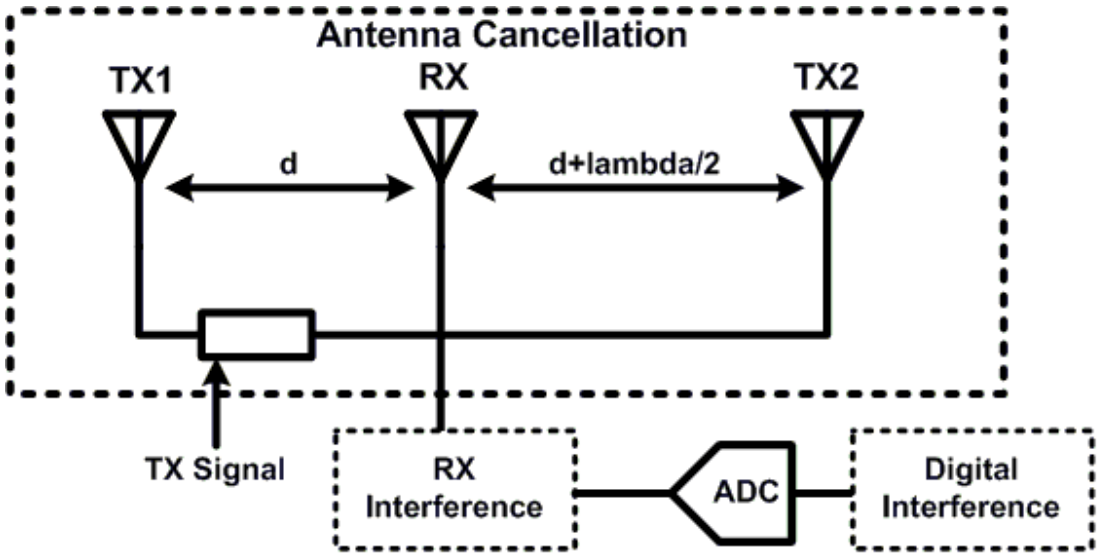

Fig. 1-5 Full Duplex Transceiver with Antenna Cancellation Technique

1.2.6 Other Cancellation Techniques

Other cancellation methods have been proposed which achieve some level of self-interference cancellation. A front-end on-chip high-Q passive-filter using bond wires is presented in [14], see Fig. 1-6. Designing a high-Q on-chip bandpass filter at the RF front-end, to filter the TX leakage is extremely challenging because of the lack of high-Q integrated inductors in the frequency bands up to 5 GHz. In [14], a three-pole differential bandpass filter at 2.14 GHz using bond-wire inductors is presented. Since the TX and RX are usually separated by only a hundred megahertz, even with a third order bandpass filter, the TX leakage suppression is no more than 10dB [14]. Higher order filters will improve the leakage suppression, but results in a higher pass-band insertion loss due to the quality factor of wire-bond inductors and on-chip capacitors.

An integrated LMS adaptive filter was proposed in [15], see Fig. 1-7. The filter functions by injecting a 180^{o} out-of-phase copy of the TX leakage, into the LNA output. The proposed LMS adaptive filter achieves a TX leakage suppression of 28dB with a noise figure penalty of 1.3dB

and an additional 0.5mA power consumption. The suppression is limited by the DC offset in the correlators, the reference signal coupling, and the duplexer group delay.

Feedback techniques provides another set of methods to suppress the TX leakage [16-17]. Two different feedback architectures are shown in Fig. 1-8(a) and Fig.1-8 (b). Fig.1-8 (a) proposes a feedback loop incorporating the receiver's down-conversion path [16] while Fig.1-8 (b) has a separate rejection loop after the LNA, which needs an additional down-converter [17]. Incorporating the down-converter into the feedback loop saves power consumption and silicon area. However, the non-idealities from the RX baseband amplifier reduces the suppression. Overall, the extra feedback circuitry (mixers and amplifiers) adds a non-negligible power consumption (22.32mW in [16]), and results in a relatively poor noise performance (7.25-8.9dB in [16]).

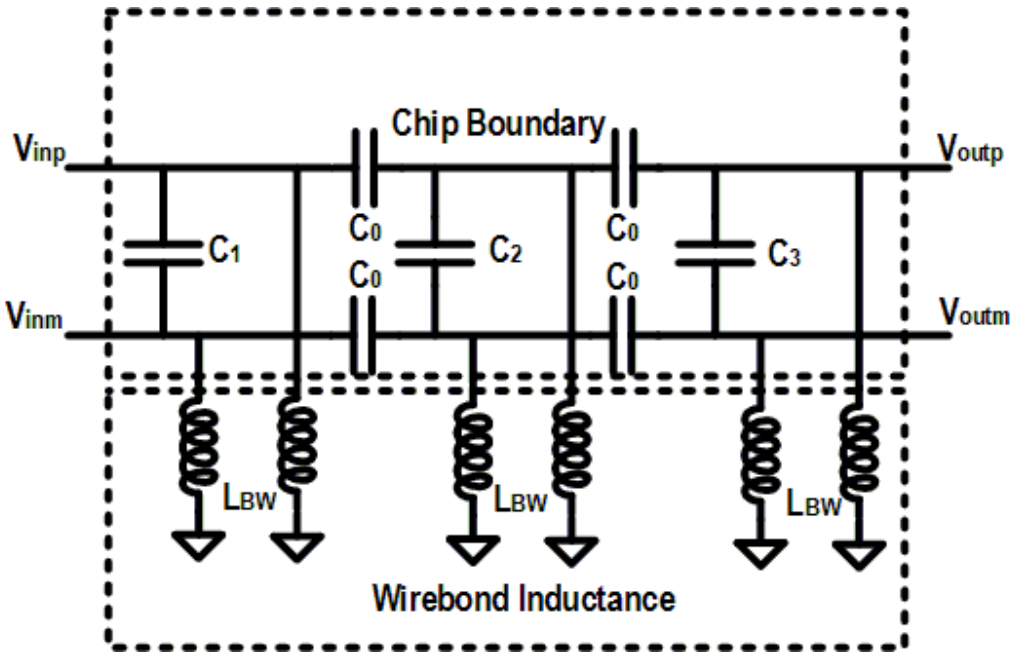

Fig. 1-6 Pseudo filter Technique with equal value bond wires as inductor replacements.

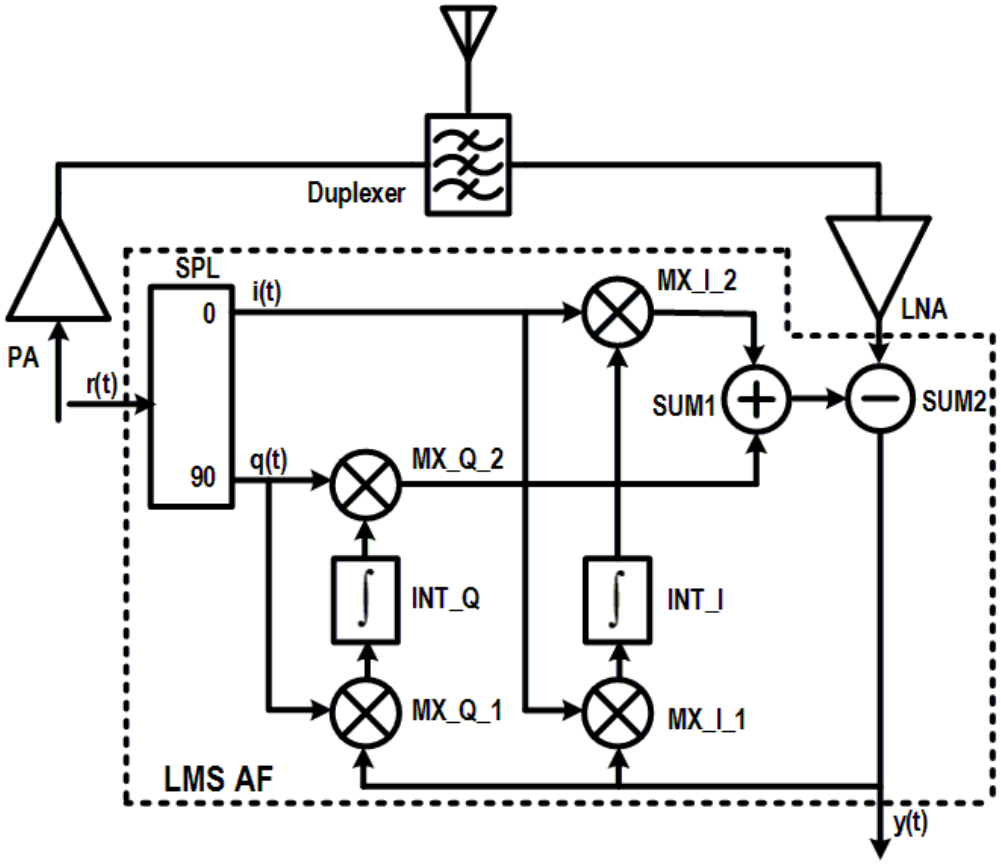

Fig. 1-7 LMS adaptive filter architecture in a CDMA Receiver

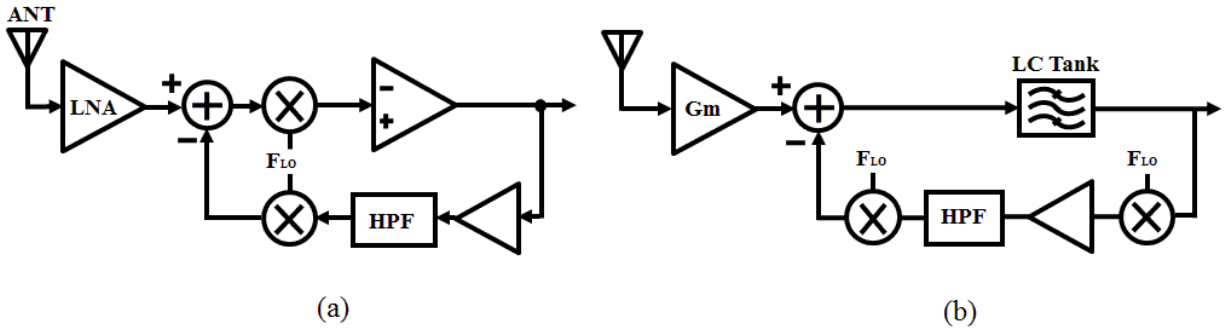

Fig. 1-8 Feedback Filtering Technique in Receiver

1.2.7 Summary

Most of the aforementioned approaches utilize an active cancellation path which is problematic from a noise and power perspective. A trade-off between noise figure, power consumption, stability, area and bandwidth exists, referring to Tab. 1-1.

Table 1-1 Summary of Different TX Leakage Cancellation Techniques

	Extra Power	NF Penalty	Area	BW	Stability	LO Leakage
FTNC	No	No	Small	Wide	No	Yes
AFT	Yes	Moderate	Small	Narrow	No	No
Feed-Forward	Yes	Moderate	Small	Moderate	No	No
Active Two-Port	Yes	Moderate	Small	Narrow	No	No
Antenna Tech.	No	Small	Large	Narrow	No	No
Pseudo-filter using bond-wires	No	Small	Small	Narrow	No	No
LMS Filter	Yes	Moderate	Small	Moderate	No	No
Feed-Back	Yes	Large	Small	Moderate	Yes	No

1.3 Research Objectives

Table 1-1 suggest the existing cancellation techniques leave significant room for improvement and possible exploration of techniques which perform self-interference mitigation without degrading the receiver noise figure. An ideal integrated TX leakage cancellation scheme should have the following characteristics:

- Introduce minimal noise, or additional power, while using minimal silicon area.
- Perform cancellation at the receiver input to relax the required RX selectivity performance.
- Present negligible loading (high impedance) to the TX-PA output.
- Minimize loss in the RX/TX signal chains.
- Minimal possibility of LO-feedthrough impacting the receiver stability.
- Insensitive to packaging and on-board EM environment, such a variation in the antenna impedance.

This thesis proposes to perform TX leakage cancellation at the RX input, using only passive-reactive components with minimal silicon area and negligible extra power.

1.4 Thesis Organization

This thesis is organized as follows:

Chapter 2: A brief introduction of the system considerations is provided. Different coupling mechanisms are described including magnetic coupling and coupling through substrate.

Chapter 3: An integrated passive Four Port Canceller (FPC) is introduced which to suppress the TX leakage. Basic transformer modelling and design will be covered first and the design methodology for a FPC is provided later including the tradeoff between insertion loss, tuning range, noise figure, loading effects and cancellation bandwidth. A comparison between the FPC and the integrated duplexer will be discussed at the end of this chapter.

Chapter 4: Circuit implementation details are discussed in this chapter. An example of the FPC technique was applied to the design of a WCDMA front-end. By performing cancellation at the RX input, the linearity (IP2) performance of the LNA and subsequent blocks are relaxed, leading to a lower power consumption solution.

Chapter 5: Measurement results of the FPC techniques implemented in WCDMA front-end are provided including receiver characteristics (S-Parameter and Noise Figure) and canceller performance.

Chapter 6: A brief summary and conclusion of the thesis and a discussion on the scope for further work and applications.

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2. System Considerations

2.1 TX Leakage Analysis

In a FDD communication systems, data is transmitted and received simultaneously. A three-port duplexer, which is composed of two bandpass filters connected between the antenna, the transmitter and the receiver allows simultaneous transmission of uplink and downlink signals in different frequency bands. One of the dominant sources of interference in FDD systems is caused by insufficient isolation between the transmitter and receiver since the duplex filter only provides an isolation of no more than 55dB. Coupling through the substrate gives another source of TX leakage. In MOS devices, substrate coupling primarily occurs through the bias-dependent source/drain-to-substrate junction capacitance. Since the PA always delivers a high output power (as high as 27dBm in cellular system), the non-linear nature of the junction-capacitance makes the coupling even harder to predict. Other non-negligible coupling includes magnetic coupling, bond-wires coupling and other unexpected on-board coupling.

Using WCDMA as a point of discussion, the TX leakage problem is illustrated in Fig.2-1. Assuming a TX output power of 27dBm and 50dB suppression through the duplexer, a residual -23dBm TX leakage will be present at the LNA input. Assuming an LNA gain at the TX frequency of 15dB, the TX leakage is amplified to -8dBm. In the absence of a SAW filter, the -8dBm TX jammer will appear directly at the LNA output, placing the burden of the IIP2 performance on the mixer; in this example an IIP2 > 45dBm is necessary [1-2]. In addition, any undesired strong blockers close in frequency to the RX band, will create cross-modulation distortion in the presence of a large TX leakage signal. When a strong single-tone jammer with large amplitude is present in the vicinity of the RX band, the leaked TX signal will cross-modulate with the interference tone

due to nonlinearities in the LNA. Although both the TX leakage and jammer are not in the RX band, the spectrum of the cross-modulation products may partially fall into the RX band and desensitize the RX chain.

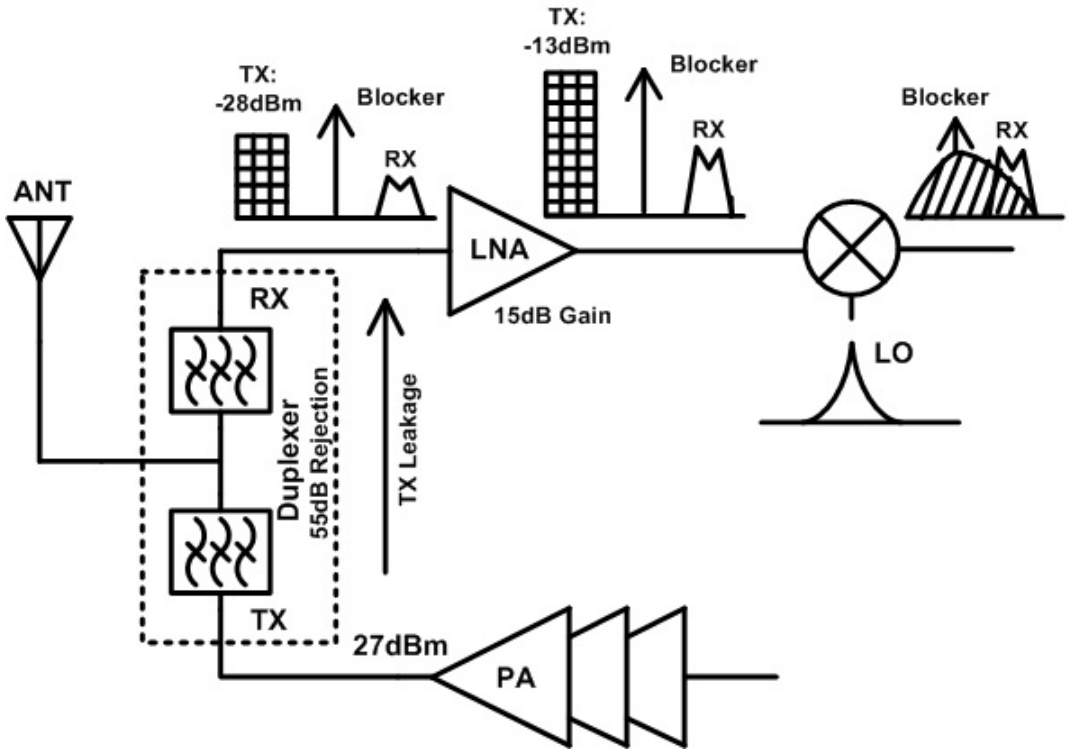

Fig. 2-1 Various mechanisms of TX Leakage signals producing RX interference in full duplex systems for FDD Radios

Reciprocal mixing is another big issue. Reciprocal mixing occurs when a TX leakage mixes with the receiver's local oscillator signal. The local oscillator has finite phase noise, which mixes with the TX leakage and creates an interference component at the baseband. In addition, another effect which degrades the receiver's carrier-to-interference (C/I) radio occurs when a large TX leakage signal begins to modulate the g_m of devices in the signal path, and subsequently frequency translate noise from the bias circuitry to within the signal band of interest. This has the effect of raising the

noise floor in the receive signal path. In addition, a large TX signal present in the receiver will cause gain compression. All of these effects described above will degrade the receiver's carrier-to-interference (C/I) ratio. Thus, it's important to mitigate or cancel self-interference as much as early in the receive chain as possible. .

2.2 Different Coupling Mechanisms

Integration of the PA and the LNA on the same chip causes various coupling paths, as shown in Fig.2-2[3-4]. Except the dominant leakage path through the on-board FBAR duplex filter, additional coupled TX leakage is mainly introduced by the substrate coupling from the PA non-linear junction capacitance, magnetic coupling from the big spirals inside PA/LNA and wire-bond inductance coupling. All these coupling mechanisms will be addressed carefully in the following sections.

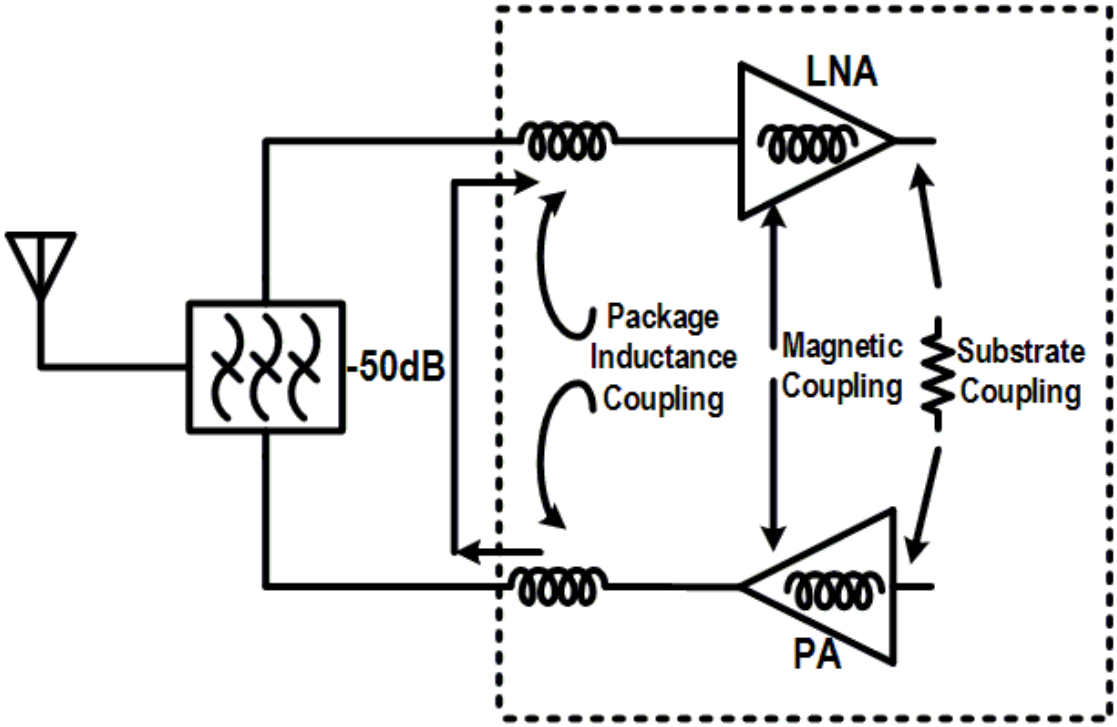

Fig.2-2 Various Leakage Paths from a transmitter to a receiver integrated on the same die.

2.1.1 Substrate Coupling

In MOS devices, substrate coupling primarily occurs through the bias-dependent source/drain-to-substrate junction capacitance. The noise reception of devices such as MOS devices, capacitors, resistors and interconnect lines occur usually through capacitive sensing. The transmission of the substrate noise is a function of the substrate type, geometry and frequency [5].

In general, it is extremely difficult to model the substrate coupling mechanism accurately since it has to include all the noise injector and receptor devices on a substrate and the highly non-linear nature of the junction-capacitance makes the modeling even harder. Equation (2-1) displays the equations for the junction capacitance [6].

$$C_j = \frac{C_{j0}}{\sqrt[3]{1-\frac{V_D}{\varphi_0}}} \tag{2-1}$$

Here, C_j, V_D, φ_0 represents junction capacitance, the bias on the junction and built-in potential, respectively.

2.1.2 Electromagnetic Coupling

On-chip spiral inductors for matching-networks, resonant-loads, oscillators and resonant peaking create another mode of coupling. The on-chip inductors, even with the use of guard rings, result in non-negligible electromagnetic coupling between the TX and RX paths [3-4]. Although isolation could be improved by increasing the distance between TX and RX paths, this solution results in an increase in die size and fabrication cost.

2.1.3 Other Coupling Mechanisms

Other non-negligible coupling mechanisms, which include different paths of coupling through capacitive and wire-bond/package inductance, make the modeling of various TX leakage signal paths even more difficult.

In the proposed system, to account for all the coupling mechanisms described above, TX and RX are fabricated on the same die and are connected together using an on-board FBAR duplexer. Although in the proposed prototype device a PA is not integrated in the chip, the LC matching network for PA and LNA are integrated on the same die to capture the magnetic-coupling. To replicate the effect of substrate leakage from the PA, an nwell-to-psub diode has been added in the primary winding of the PA matching network to emulate the junction capacitance.

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[2] H. Khatri, P. S. Gudem and L. E. Larson, “An Active Transmitter Leakage Suppression Technique for CMOS SAW-Less CDMA Receivers,” IEEE J. Solid-State Circuits, vol. 45, no. 8, Aug. 2010.

[3] R. Minami, J. Y. Hong, K. Okada, A. Matsuzawa, “Measurement of Integrated PA-to-LNA Isolation on Si CMOS Chip,” Proc. of APMC, 2010.

[4] R. Minami, J. Y. Hong, K. Okada, A. Matsuzawa, “Measurement of Integrated PA-to-LNA Isolation on Si CMOS Chip,” IEICE Trans. 94-C(6): 1057-1060, June 2011.

[5] Modeling and Analysis of Substrate Coupling in Silicon Integrated Circuits

[6] P. R. Gray, P. Hurst, S. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed., New York, NY: Wiley, 2001.

3 Four-Port Canceller (FPC) Design

3.1 Transformer Design Basics

In recent years, on-chip transformers have contributed significantly to the enhanced performance of radio frequency integrated circuits. Accordingly, a great amount of research has been focused on the design and characterization of integrated transformers [1-5]. In the following sections, a brief overview of the transformer design will be described first before moving to the four-port canceller design.

3.1.1 Transformer Lumped-Element Model

Fig.3-1 displays the compact model for a transformer with four driven ports [5]. The turns of transformer are modeled by ideal inductors L_p and L_s, and the magnetic flux between the primary and the secondary coils is modeled with a coupling coefficient k. R_p and R_s represents the ohmic losses in the coils and C_{pp}, C_{ss}, C_{dc} model the relevant parasitic capacitances.

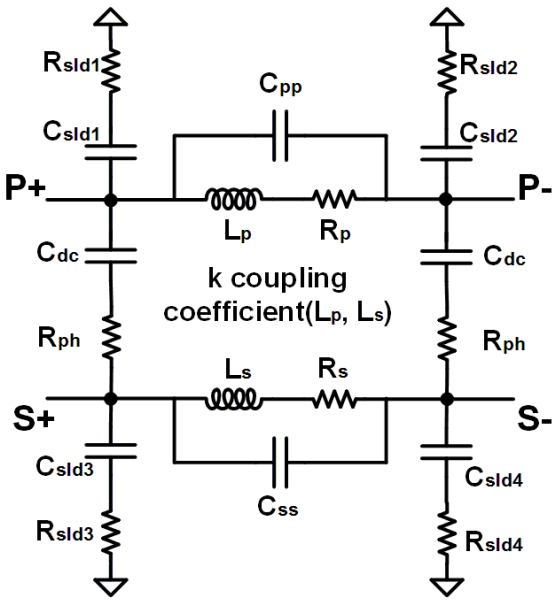

Fig. 3-1 Lumped-Element Circuit Model of the Four-Driven Port Transformer

3.1.2 Transformer S-Parameter Extraction

S-Parameters are used to extract the inductances $\boldsymbol{L_p}$ and $\boldsymbol{L_s}$, quality factors $\boldsymbol{Q_p}$ and $\boldsymbol{Q_s}$ and coupling coefficient $\boldsymbol{k}$ as a function of frequency. These parameters are calculated using the following equations (3-1a) to (3-1e).

$$\mathbf{Q_p} = \frac{\mathbf{Im(Z_{11})}}{\mathbf{Re(Z_{11})}} \tag{3-1a}$$

$$\mathbf{Q_S} = \frac{\mathbf{Im(Z_{22})}}{\mathbf{Re(Z_{22})}} \tag{3-1b}$$

$$\boldsymbol{k} = \sqrt{\frac{\boldsymbol{Im(Z_{12})\cdot Im(Z_{21})}}{\boldsymbol{Im(Z_{11})\cdot Im(Z_{22})}}} \tag{3-1c}$$

$$\mathbf{L}_{\boldsymbol{p}} = \frac{\mathbf{Im(Z_{11})}}{\mathbf{2\cdot\pi\cdot f}} \tag{3-1d}$$

$$\mathbf{L}_{\boldsymbol{s}} = \frac{\mathbf{Im(Z_{22})}}{\mathbf{2\cdot\pi\cdot f}} \tag{3-1e}$$

3.2 Theoretical Analysis of FPC

The FPC, shown in Fig.3-2, is the key component of the TX leakage cancelling technique. This cancelling idea comes from the two-port transformer. In both two-port and four-port schemes, the primary signal, received at the antenna side, travels from port-one to port-two along with any leakage signal from the transmitter. However, in the FPC setup, a portion of the TX output signal is intentionally coupled into the RX path through port-three, so as to cancel the TX leakage component seen at port-two (see Fig.3-2). Accordingly, to achieve such cancellation, the amplitude and phase of the coupled TX signal is tightly controlled by varying the termination reactance on port-three and port-four of the transformer. Also, it is worthy to note that with the FPC

configuration, the entire transformer structure is absorbed in the transformer-based LNA matching network and therefore, consumes minimal additional area.

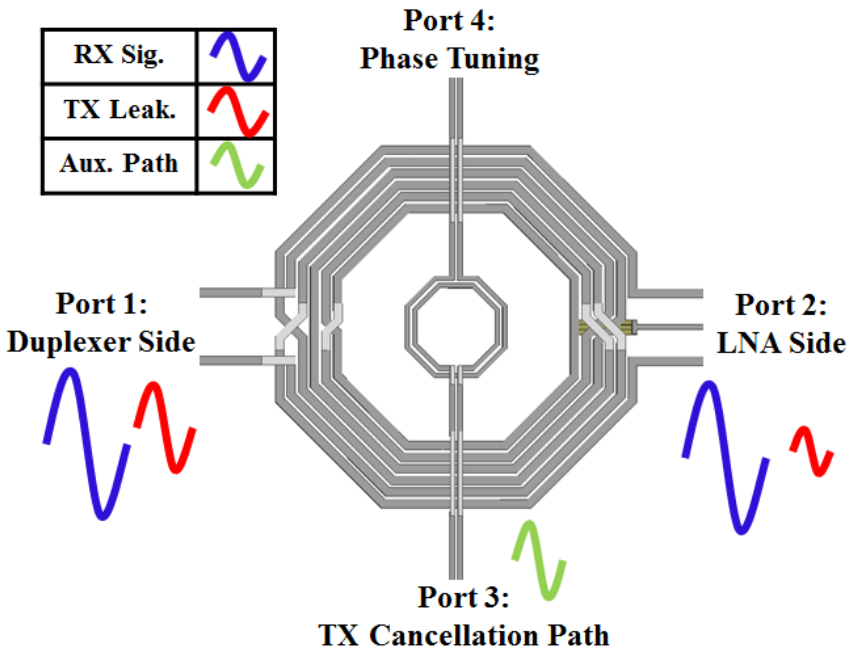

Fig. 3-2 Four-Port Canceller (FPC)

Since the duplexer has a rejection of approximately 50dB at TX frequencies, any practical cancellation technique must be accurately adjusted to match the amplitude and have the opposite phase of the attenuated leakage signal. This is achieved using two techniques. First, ports three and four are weakly coupled with ports one and two. Second, a switched capacitor and varactor bank is placed between the output of the PA matching network and the canceller input, to tune the phase and amplitude of the TX-signal entering the FPC.

The detailed analysis of the FPC will be carried out in the following sections. The design of the three-port canceller is reviewed in Chapter 3.2.1, including discussions on insertion loss, PA

loading and phase tuning range limitations. Chapter 3.2.2 describes the design of the FPC, with an explanation of adding a fourth port to widen the tuning range and get a better cancellation.

3.2.1 Three-Port Canceller (TPC)

The modelling and analysis of the FPC is difficult and presents little intuition due to the many (six in this case) coupling coefficients between each of the primaries. As such, the analysis in this chapter begins with the simplified model of the TPC which a more involved description given in the next chapter. In the TPC design, in order to get some electromagnetic coupling from the PA coil to the RX input for cancellation purposes, a small winding is placed inside the large primary/secondary transformer structure. Fig.3.3 displays the HFSS 3D Structure and equivalent circuit schematic for the TPC.

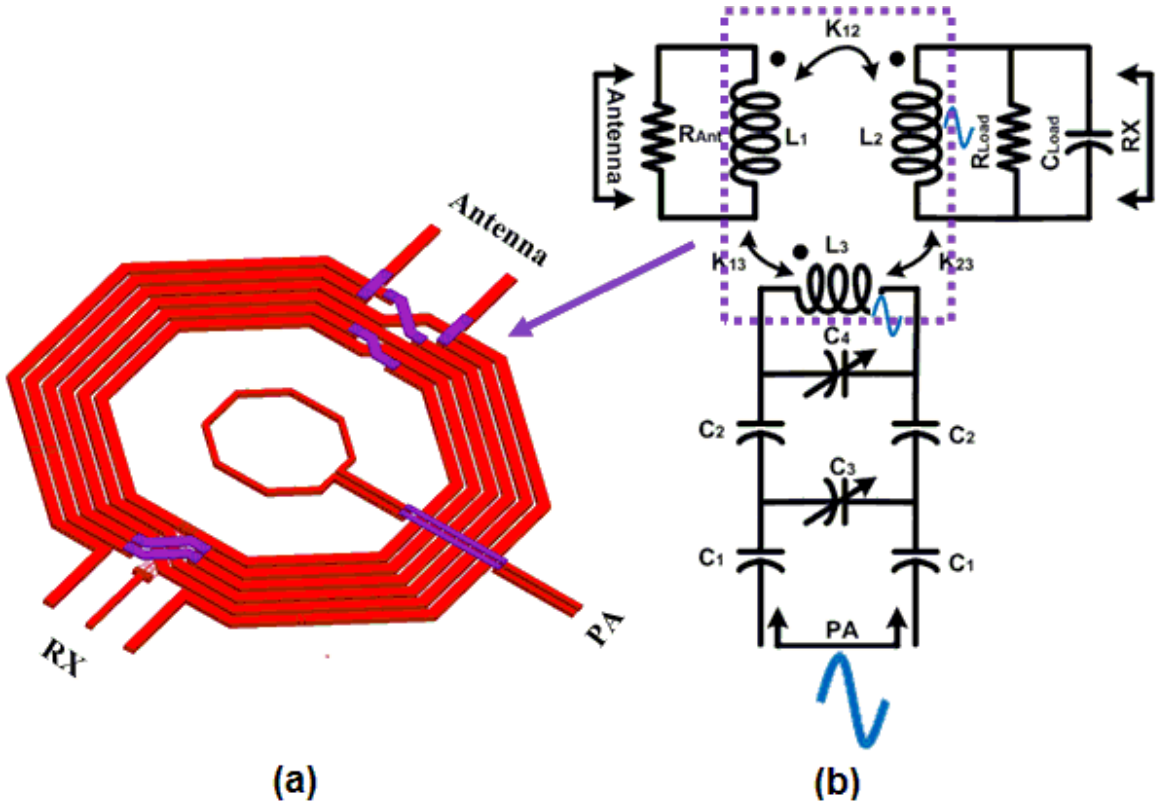

Fig. 3-3 Three-Port Canceller (a) HFSS Model (b) Circuit Equivalent Model with Capacitor Tuning Network

3.2.1.1 Insertion loss of Three Port Canceller

Recent research in integrated duplexers [6-10] indicates that a three-port hybrid transformer suffers from a fundamental 3dB TX/RX insertion loss if port-3 is comparable to the primary and secondary winding. In order to reduce the insertion loss penalty due to the third winding, the coupling must be made small between the third and primary/secondary windings. Since the integrated duplexer looks similar to the proposed TPC or FPC, a detailed comparison between them will be described in Section 3.3.

However, if the third-coil is too small, the coupling coefficients between coil-three and primary/secondary coils reduced, shrinking the available tuning range. Therefore, choosing the coupling coefficient k needs to consider both the leakage signal strength and insertion loss penalty.

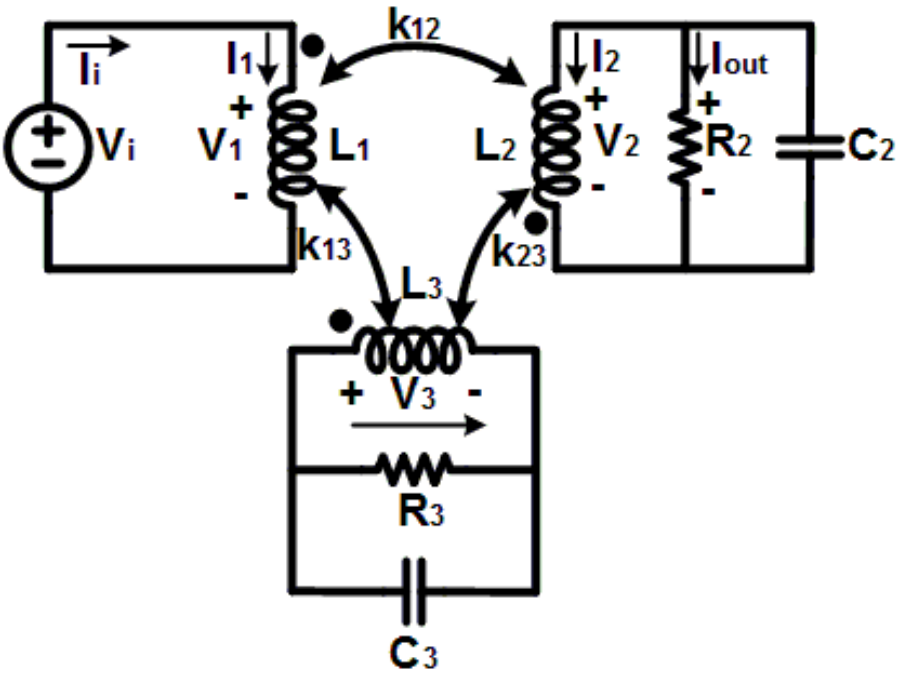

Fig.3-4 Simplified Equivalent Circuit Model for the Three Port Canceller

Using Kirchhoff's voltage and current law, the voltages V_1, V_2 and V_3 , on the primary, the secondary, and the tertiary windings respectively, can be expressed as a function of induced currents I_1, I_2 and I_3.

$$V_1 = L_1 s \cdot I_1 - M_{12} s \cdot I_2 + M_{13} s \cdot I_3 \quad (3\text{-}2a)$$

$$V_2 = L_2 s \cdot I_2 - M_{12} s \cdot I_1 - M_{23} s \cdot I_3 \quad (3\text{-}2b)$$

$$V_3 = L_3 s \cdot I_3 + M_{13} s \cdot I_1 - M_{23} s \cdot I_2 \quad (3\text{-}2c)$$

V_2, I_2 *and* V_3, I_3 are also a function of load impedance

$$V_2 = -I_2 \cdot Z_2 \tag{3-3a}$$

$$V_3 = -I_3 \cdot Z_3 \tag{3-3b}$$

Here, Z_2 and Z_3 represent the parallel combination of R_2, C_2 and R_3, C_3, respectively.

Combining (3-2) and (3-3), and using the definition of the power gain $\mathrm{G} = \frac{\mathrm{P_{out}}}{\mathrm{P_{in}}}$, the power gain G from the antenna to the RX input can be expressed as:

$$G = \frac{P_{out}}{P_{in}} = \frac{V_2 \cdot I_{out}}{V_1 \cdot I_1} = \frac{D^2}{C(AC+BD)R_2} \tag{3-4}$$

Where, $A = L_1 s - \frac{M_{13}^2 S^2}{L_3 s + Z_3}$

$$B = \frac{M_{12} s}{Z_2} - \frac{M_{13} M_{23} s^2}{Z_2 Z_3 (1 + L_3 s / Z_3)}$$

$$C = 1 - \frac{M_{23}^2 s^2}{Z_2 Z_3 \left(1 + \frac{L_3 s}{Z_3}\right)} + \frac{L_2 s}{Z_2}$$

$$D = \frac{M_{13} M_{23} s^2}{L_3 s + Z_3} - M_{12} s$$

Simulation results of the primary to secondary insertion loss versus frequency for varied coupling coefficients are provided in Fig.3-5; specifically k_{13} and k_{23} are fixed to be equal and varied from 0 to 0.2 at 0.05 increments. The simulations were performed from 1.5GHz to 2.5GHz by spectre with Fig.3-4 values $L_1 = 1.2nH$, $L_2 = 6nH$, $L_3 = 0.4nH$, $k_{12} = 0.8$, $R_2 = 300\Omega$, $C_2 = 1pF$, $R_3 = Q_3 \cdot w_0 \cdot L_3$, $Q_3 = 5$, $f_0 = 2$GHz. These values agree well with extracted values from either chip measurements or extracted simulations, which will be discussed later. From Fig.3-

5, coupling coefficients k_{13} and k_{23} should be less than 0.1 to achieve an insertion loss below 0.5dB from the third winding.

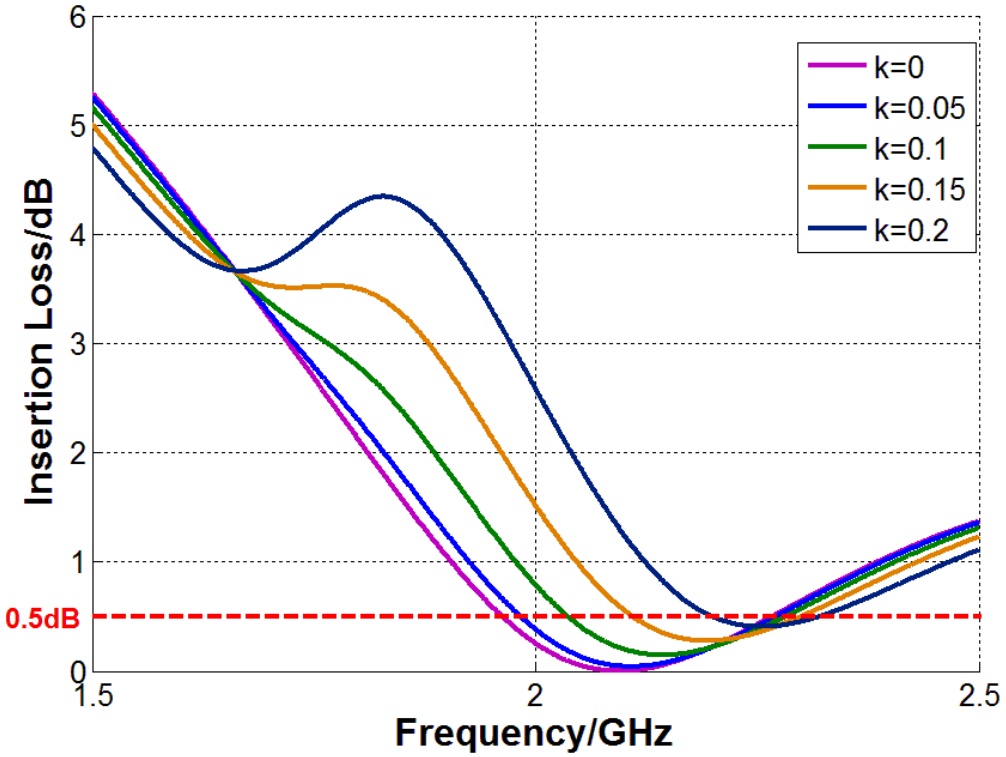

Fig.3-5 Three Port Canceller's Insertion Loss versus frequency and coupling coefficient value: $L_1 = 1.2nH$, $L_2 = 6nH$, $L_3 = 0.4nH$, $k_{12} = 0.8$, $R_2 = 300\Omega$, $C_2 = 1pF$, $R_3 = Q_3 \cdot w_0 \cdot L_3$, $Q_3 = 5$, $f_0 = 2GHz$

3.2.1.2 PA Loading

An ideal integrated canceller should present high input impedance (PA-side), as to mitigate any loading effects on the TX-PA output. Accordingly, accurately characterizing this input impedance is important, such is the topic of this section. Fig.3.6 (b) gives a simplified circuit-model that can be used to describe the TX-PA cancellation path.

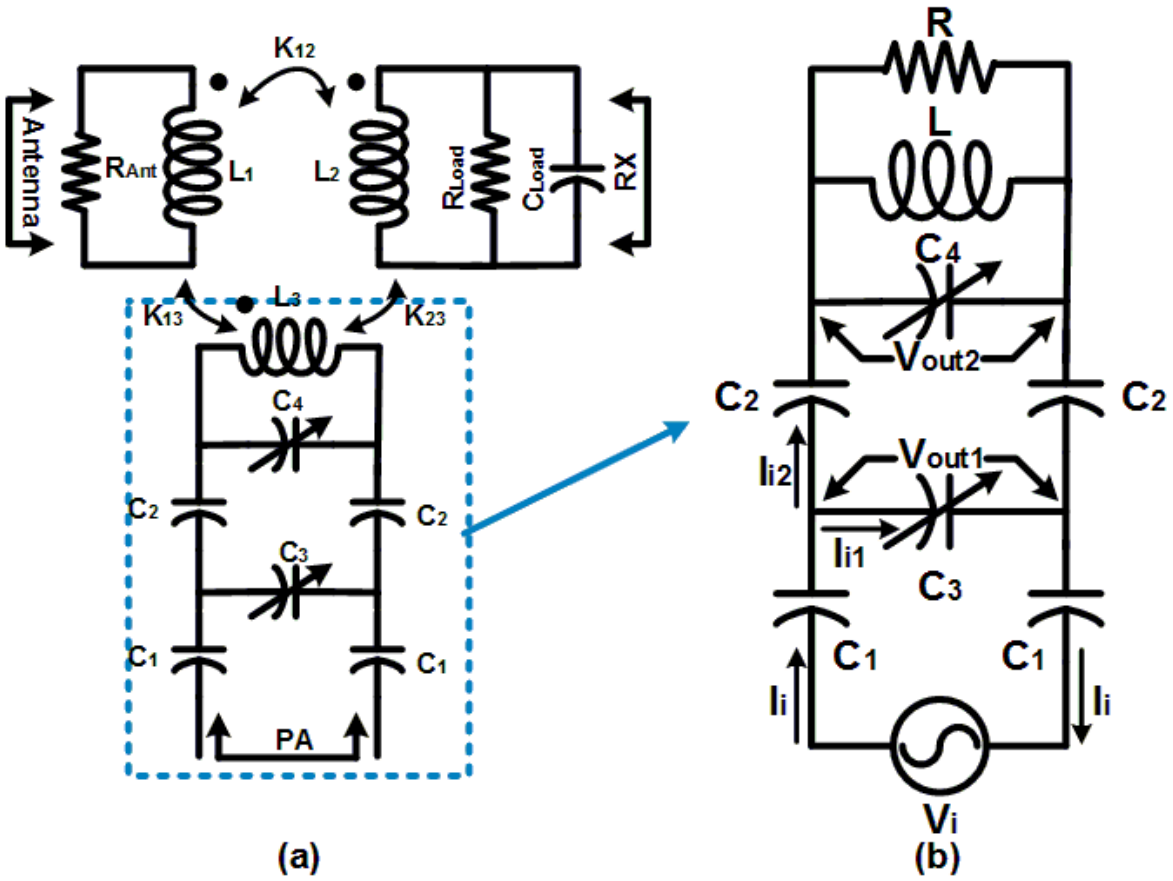

Fig. 3-6 Simplified Models for a Three Port Canceller with Capacitor Tuning Network. (a) Full Circuit Equivalent Model with Three Port Canceller (b) Amplitude/Phase Cancellation Path

The current I_i, I_{i1}, I_{i2} and voltage V_{out1}, V_{out2}, V_i can be described as follows:

$$I_i = I_{i1} + I_{i2} \tag{3-5a}$$

$$V_{out1} = V_{out2} + \frac{2}{sC_2} I_{i2} \tag{3-5b}$$

$$V_{out2} = I_{i2} \cdot (R \parallel sL \parallel 1/sC_4) = I_{i2} \cdot Z \tag{3-5c}$$

$$V_{out1} = I_{i1} \cdot \frac{1}{sC_3} \tag{3-5d}$$

$$V_i = V_{out1} + I_i \frac{2}{sC_1} \tag{3-5e}$$

Where, $Z = R \parallel sL \parallel 1/sC_4$

By combining (3-5a) to (3-5e) and then solving for I_i and V_i, the input admittance seen by the PA can be derived as,

$$Y_i = \frac{I_i}{V_i} = \frac{s\left(1+2\frac{C_3}{C_2}\right)+s^2C_3Z}{2\left(\frac{1}{C_1}+\frac{1}{C_2}+2\cdot\frac{C_3}{C_2}\cdot\frac{1}{C_1}\right)+sZ\left(1+2\frac{C_3}{C_1}\right)} \tag{3-6}$$

In a practical design, since the PA input signal is always large (usually more than 10V voltage swing when PA delivers 30dBm output) and C_3, C_4 is always realized with a switched-capacitor bank or varactors. Due to reliability issues, C_1, C_2 are always realized with a lower value capacitance than C_3 to achieve enough attenuation of the PA signal before it reaches the switches.

Accordingly, Y_i can be simplified to (3-7)

$$Y_i \approx \frac{s\cdot 2\frac{C_3}{C_2}+s^2C_3Z}{4\frac{C_3}{C_1C_2}+sZ\cdot\frac{2C_3}{C_1}} = \frac{C_1 s}{2} \tag{3-7}$$

From (3-7), the input impedance of the canceller from PA side is almost capacitive and could be absorbed into the PA output matching network.

3.2.1.3 Tuning Range Limitations

To suppress the TX leakage at the RX input down to a desired value, the canceller should be tunable over a wide range with enough resolution. Since it is difficult to get the inductor tunable after fabrication, amplitude/phase tuning is performed foremost in the cancellation path, which is shown in Fig.3-6(b). However, before deriving expressions for V_{out2}, let's first look at the level

of amplitude/phase resolution required in the canceller, to achieve 10dB/20dB/30dB/40dB TX suppression, which is defined in (3-8).

$$\text{Leakage Suppression (dB)} = 20 \cdot log_{10} \left| \frac{(A+\Delta A)e^{j\Delta\varphi} - A}{A} \right| \quad (3\text{-}8)$$

Here, $20 \cdot log_{10}(1 + \frac{\Delta A}{A})$ defines amplitude resolution and $\Delta\varphi$ defines the phase resolution.

Table 3-1 TX Leakage Suppression versus Amplitude/Phase Mismatch

Amplitude Resolution/dB	Phase Resolution/Deg	Leakage Suppression/dB
2	5	11.15
2	2	11.63
1	2	17.89
1	1	18.17
0.5	1	24.16
0.5	0.5	24.47
0.2	0.5	-32.02
0.2	0.2	-32.556
0.1	0.2	-38.43
0.1	0.1	-38.62

Table 3-1 shows a TX leakage suppression versus amplitude/phase mismatch on the cancellation path based on (3-8). Better matching is required to get a higher leakage suppression.

The transfer function of V_{out2}/V_i could be expressed in (3-9) according to (3-5).

$$\frac{V_{out2}}{V_i} = \frac{1}{1+\frac{C_3}{C_1}+\frac{2}{sZ}(\frac{1}{C_1}+\frac{1}{C_2}+\frac{2 \cdot C_3}{C_1 \cdot C_2})} \quad (3\text{-}9)$$

Here, C_1 and C_2 are fixed capacitors and the amplitude/phase modulation will mainly be determined by switch capacitor bank C_3, varactor C_4 and the quality factor of the tank.

As discussed in chapter 3.2.1.2, C_1, C_2 is always designed to be smaller than C_3 for reliability reasons, therefore, the transfer function in (3-9) could be simplified to (3-10).

$$\frac{V_{out2}}{V_i} \approx \frac{1}{\frac{C_3}{C_1}+\frac{4}{sZ}\cdot\frac{C_3}{C_1\cdot C_2}} = \frac{1}{\frac{C_3}{C_1}(1+\frac{4}{sZ\cdot C_2})} \tag{3-10}$$

As one observes from (3-10), if C_3 is large enough with respect to C_1 and C_2, amplitude tuning can be performed virtually independent of the system's phase delay. However, it is difficult to get an independent phase modulation.

Substituting the "Z" equivalent impedance into (3-10), the transfer function can be expressed as a function of C_4.

$$\frac{V_{out2}}{V_i} = -\frac{C_1C_2w^2L}{4C_3}\cdot\frac{1}{\frac{j}{Q}+(1-w^2C_4L)} \tag{3-11a}$$

Solving the magnitude and phase of the transfer function, the results are as displayed in (3-11b) and (3-11c). The equation shows that tuning C_4 will get both amplitude and phase modulation.

$$\left|\frac{V_{out2}}{V_i}\right| = \frac{C_1C_2w^2L}{4C_3}\cdot\frac{1}{\sqrt{(1-w^2C_4L)^2+\frac{1}{Q^2}}} \tag{3-11b}$$

$$\measuredangle\left(\frac{V_{out2}}{V_i}\right) = \pi - \operatorname{atan}\left(\frac{1}{Q(1-w^2C_4L)}\right) \tag{3-11c}$$

Therefore, using the three-port transformer, it is intrinsically difficult to maintain the amplitude at a near-constant level while modulating the phase. However, with some calibration methods,

the problem can be resolved. Before discussing the calibration methods, fundamental limitations of the tuning range will be described first.

The quality factor Q of the RLC tank plays a significant role in setting the phase tuning range. Fig. 3-7 displays simulation results of a phase tuning range according to C_4 for different values of Q. If Q is too large (i.e. Q>10), C_4 modulation will become too sensitive, and as a result the linear phase tuning bandwidth will be degraded. On the other side, if Q is too small (i.e. Q<1), the phase-tuning range reduced. Fig. 3-7 shows the simulated phase-tuning range for different values of C_4(varied from 5pF to 40pF) and Q (varied from 1 to 20). Other circuit parameters ($L_1, L_2, L_3, k_{12}, R_2, C_2, Q_3\ and\ f_0$) are kept the same as Fig. 3-5.

$L_1 = 1.2nH, L_2 = 6nH, L_3 = 0.4nH, k_{12} = 0.8, R_2 = 300\Omega, C_2 = 1pF, R_3 = Q_3 \cdot w_0 \cdot L_3,$ $Q_3 = 5, f_0 = 2GHz$

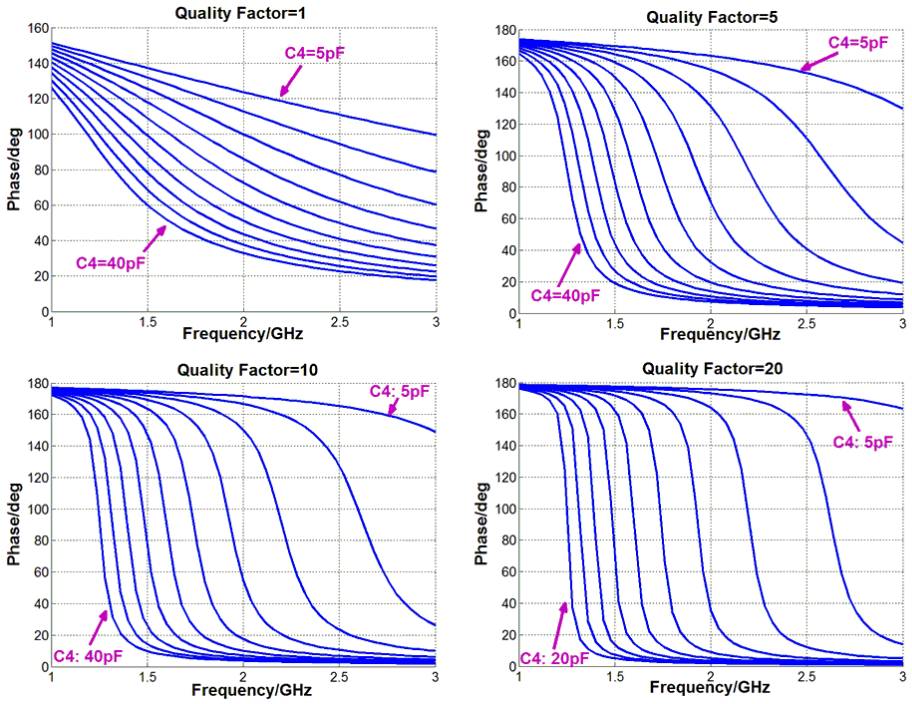

Fig.3-7 Simulation Results of Phase Tuning range as a function of $\mathbf{C_4}$ for Different Values of Q

Fig.3-7 clearly shows that an increase in the tank Q results in an expanded phase turning range. However, for a given C4 size, the linear portion of each phase-tuning curve becomes narrower with an increased Q. Since the phase of the leakage signal is unknown, it is always desired to have a 360 degree phase rotator in the canceller. Due to the fundamental tradeoff between phase tuning range and linear tuning bandwidth, the quality factor of the tank needs to be optimized around 5(see Fig. 3-7).

3.2.1.4 Tunable Tank Impedance:

As discussed in the previous section, a robust canceller design needs to have a 360 degree phase rotator and the phase tuning range which is mostly determined by the tank impedance. Usually, two structures are commonly used to realize tunable capacitors: switch-capacitor banks and varactors. However, getting a large tuning range of capacitors with a reasonable high Q is not possible for the CMOS process. Due to the parasitic capacitance from the switches and the non-linear nature of the varactors, the variable capacitance will likely not exceed 4, if a reasonable Q (i.e. Q>15) is needed. Therefore, the phase tuning range of the canceller becomes narrower with a real tunable capacitors. Accordingly, alternative impedance modulation techniques must be employed in the canceller to achieve wide phase tuning range.

With the exception of switch-capacitor banks and varactors, tunable inductors give another degree of freedom with respect to tuning tank impedance. However, one of the traditional tunable inductor techniques, switch-based tunable inductors suffers from the low Q and low resolution [11]. The inductance value is controlled by switches which are either on or off, however, the series resistance of the switches lowers the Q of the inductor and the limited number of switches reduces the tuning resolution. The resolution could be improved by adding more switches, but the series resistance of the switches lowers the quality factor of the inductor.

What becomes worse is when implementing switch-based inductors in the proposed canceller application since the inductance of the third winding is always small and a little add-on resistance will push the inductor Q to an unacceptable low value. In the next section, a new technique, FPC instead of TPC, will be described to solve this problem.

3.2.2 Four-Port Canceller

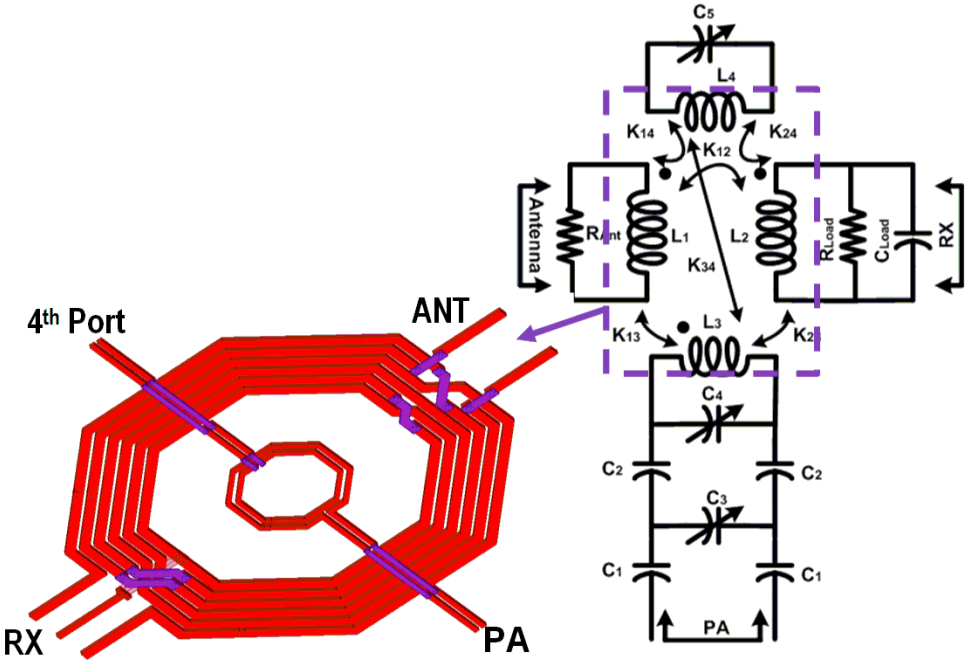

Fig. 3-8 Four Port Canceller (a) HFSS Model (b) Circuit Equivalent Model with Capacitor Tuning Network

In the FPC, a fourth port is added and strongly coupled to the PA port, which is shown in Fig.3-8. The inductance is modulated by tuning the varactors at the fourth port. The resolution is mainly determined by the control voltage of the varactors, which could be improved by adding more control bits in the DAC with minimal effect on the quality factor. Next we try to analyze the transformer-based tunable inductor technique using a simple circuit model, which is shown in Fig. 3-9.

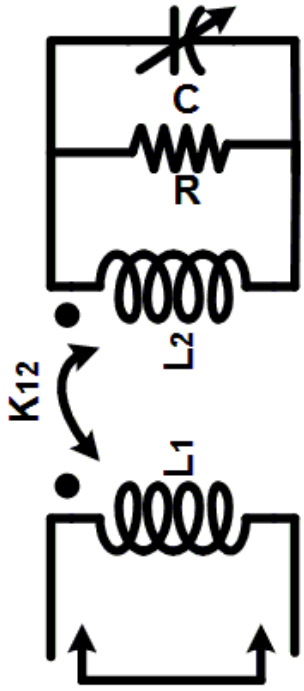

Fig.3-9 Simplified Circuit Model for Tunable Inductor Utilizing Magnetic Coupling to a Varactor Modulated Tank Circuit.

Fig.3-10 presents the simulation results of the input equivalent inductance for different tank quality factors on the fourth port ($Q = 0.5,1,2,10$). For a given varactor value on the fourth port, similar to the discussion given in 3.2.1.3, the linear portion of each inductance curve becomes narrower with an increased Q. The simulations were done from $1.5\sim2.5GHz$ using spectre with model parameters $L_1 = 0.4nH$, $L_2 = 0.4nH$, $k_{12} = 0.4$, $R = Q \cdot w_0 \cdot L_2$, , $f_0 = 2GHz$.

Compared to the TPC, by choosing a reasonable quality factor of the inductance considering the linear portion of the curve and tuning range (Q = 1, see Fig. 3-10), the FPC widens phase tuning range by adding the fourth port.

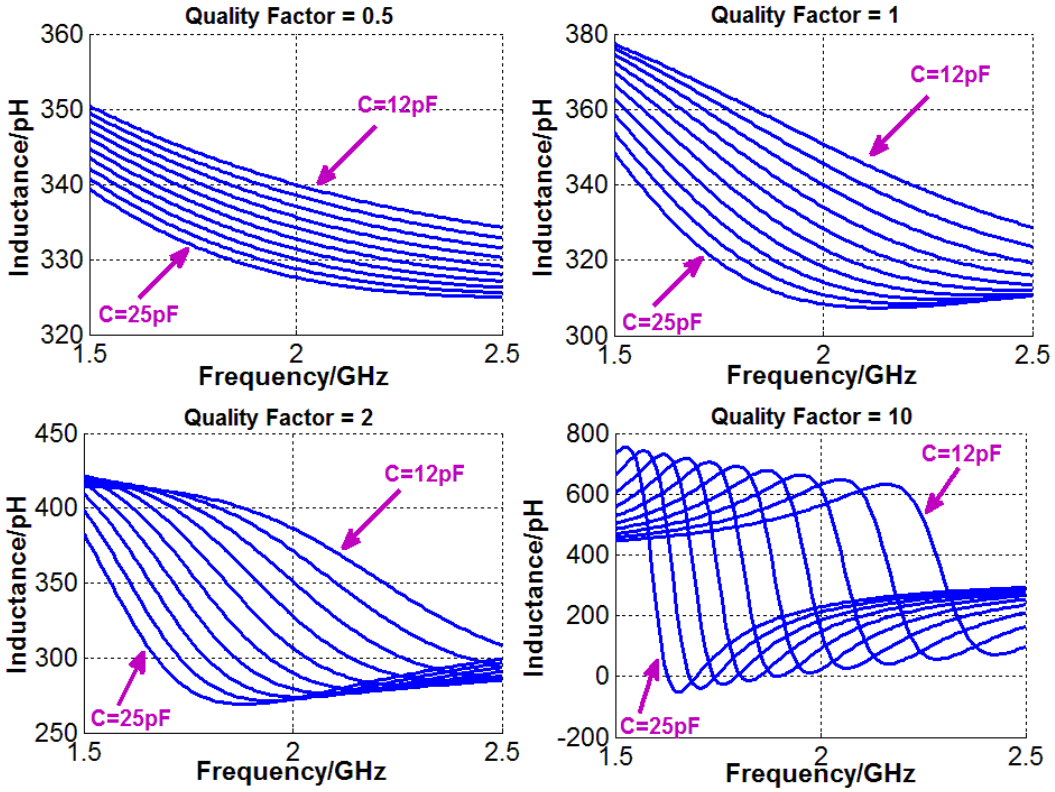

Fig. 3-10 Simulated Input Equivalent Inductance with Varied Capacitance and Tank Q

3.3 Comparison between Integrated Duplexer and FPC

Integrated duplexer [6-10] and FPC both uses multi-port transformers to do full-duplexing or self-interference cancellation. The schematic of these two look quite similar, however, there is a significant difference between these two approaches from the perspective of insertion loss, and the amount of cancellation signal which is coupled to the RX chain. This will be described and analyzed with more detail in the next section.

3.3.1 Integrated Duplexer

The integrated duplexer, shown in Fig. 3-11, has been analyzed in previous work, specifically in [10]. A duplexer is a three-port device which performs concurrent matching for the antenna, transmitter and receiver with the assumption that the duplexer should attenuate the transmitted

signal at the receiver input to avoid saturation problems. Moreover, a large TX output swing allows only passive solutions for an integrated duplexer. However, the passive solutions lead to a reciprocal network, which indicates the S-matrix of the integrated duplexer should satisfy: $S_{ij} = S_{ji}$.

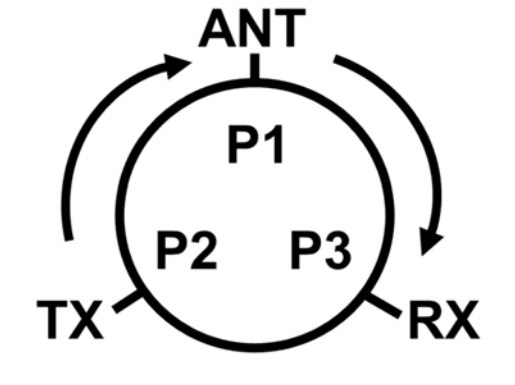

Fig. 3-11 Three Port Integrated Duplexer

Therefore, a matched, reciprocal duplexer should have an S-matrix in the form of:

$$S = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & 0 \\ S_{13} & 0 & 0 \end{bmatrix} \tag{3-12}$$

The S-matrix of any lossless implementation of the duplexer should be a unitary matrix. In other words it should satisfy

$$\sum_{k=1}^{3} S_{ki} S_{ki}^{*} = 1$$

$$\sum_{k=1}^{3} S_{ki} S_{kj}^{*} = 0 \quad for\ i \neq j$$

It has been pointed out that the integrated reciprocal duplexer has to be lossy [10]. Intuitively, if the transmitter directs 100% of its power to the antenna, due to the reciprocal nature of the integrated duplexer, the antenna is forced to deliver 100% power to the transmitter, which conflicts with the 100% power delivery from the antenna to the receiver. The three-port lossy reciprocal network is analyzed as a four-port lossless network with the fourth port terminated using a resistor to represent the loss, see Fig. 3-12.

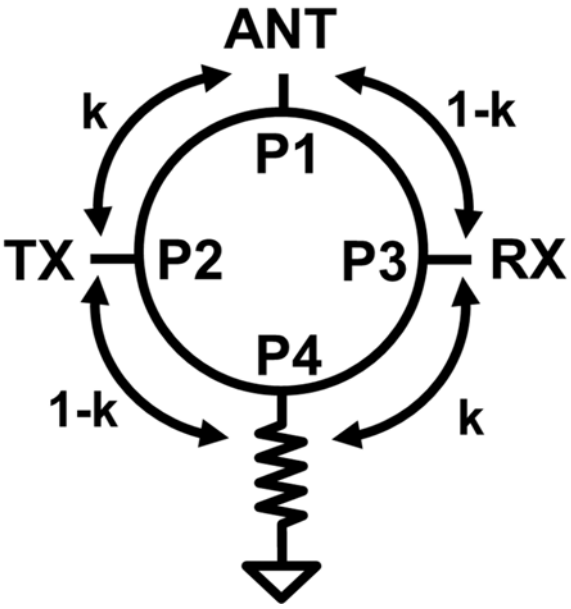

Fig. 3-12 Four-Port Model of the Integrated Duplexer

The S-matrix of the four-port duplexer is given by:

$$S = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & 0 & S_{24} \\ S_{13} & 0 & 0 & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix} \tag{3-13}$$

Applying the condition of lossless network and minimizing the insertion loss and hence maximizing S_{12} and S_{13}, gives,

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{3-14}$$

Equation (3-14) describes the tradeoffs between the transmitter and receiver insertion loss and a graphical interpretation is shown in Fig. 3-13. The power applied at any port is divided between the two adjacent ports. In the balanced case where $k = 1/2$, TX and RX both have an insertion loss of 3dB.

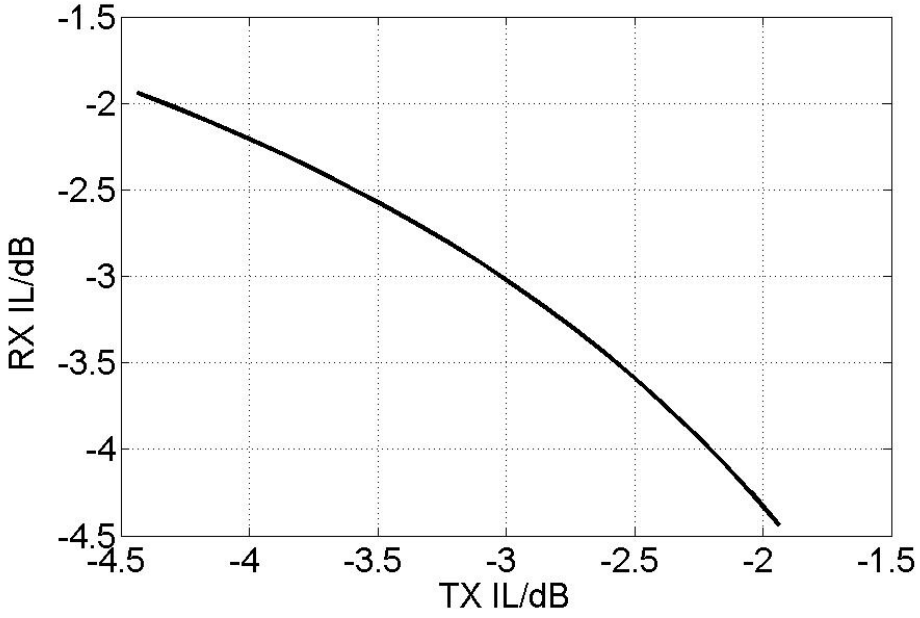

Fig. 3-13 Power Division inside an Integrated Duplexer

From the discussions above, we could conclude that the integrated duplexer has a fundamental 3dB insertion loss and the loss is independent of implementation. Usually, a hybrid four-port transformer [6-10] is used to realize the duplexer function. Next, we will describe how in contrast to the traditional integrated duplexer, the FPC can exhibit a sub-3dB insertion loss.

3.3.2 Proposed FPC

Although the FPC looks similar to the hybrid transformer from a layout perspective, it behaves quite different due to several unique electrical characteristics.

A key difference between the integrated duplexer and the FPC is that a lower coupling is used in the latter between port 3 (Coupled TX) and port 1 (ANT); however, in the integrated duplexer, larger coupling is required to lower the insertion loss, as previously discussed. Another related difference is in the FPC, port 3 from the perspective of transmitter side are designed to be high impedance while in the duplexer the impedance must be matched to 50Ohm load of antenna. Next, the insertion loss of the proposed FPC will be described from the S-matrix analysis.

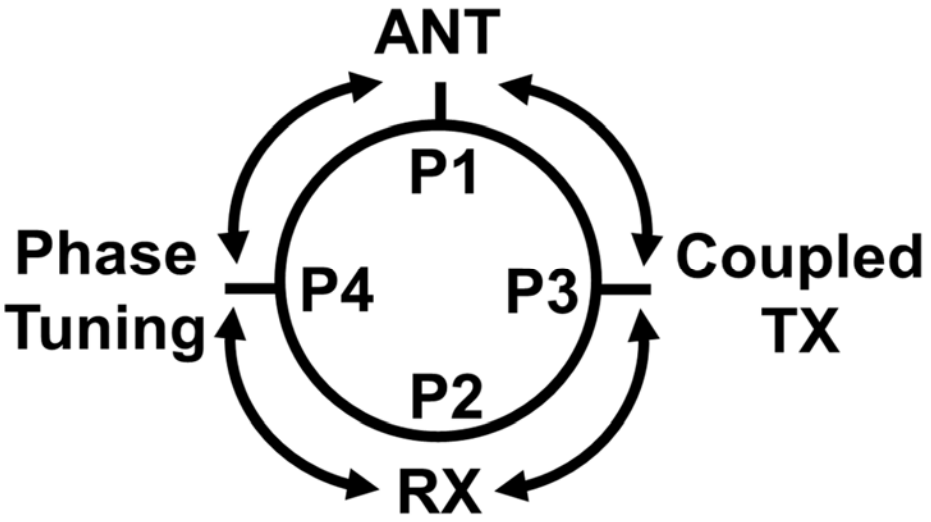

Fig. 3-14 Four-Port Model of the FPC

A Reciprocal S-matrix of the FPC is given by:

$$S = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & S_{23} & S_{24} \\ S_{13} & S_{23} & S_{33} & S_{34} \\ S_{14} & S_{24} & S_{34} & S_{44} \end{bmatrix} \quad (3\text{-}15)$$

Applying the condition of lossless network, one of the solutions to the matrix is the same as equation (3-14). However, since less coupling is required between port 3 and port 1, the insertion loss penalty gets relaxed. Fig.3-15 illustrates the RX insertion loss inside a proposed FPC as a function of coupled TX signal strength. If the coupled TX signal is 20dB lower than the original signal, than the insertion loss in the RX path will be less than 0.1dB.

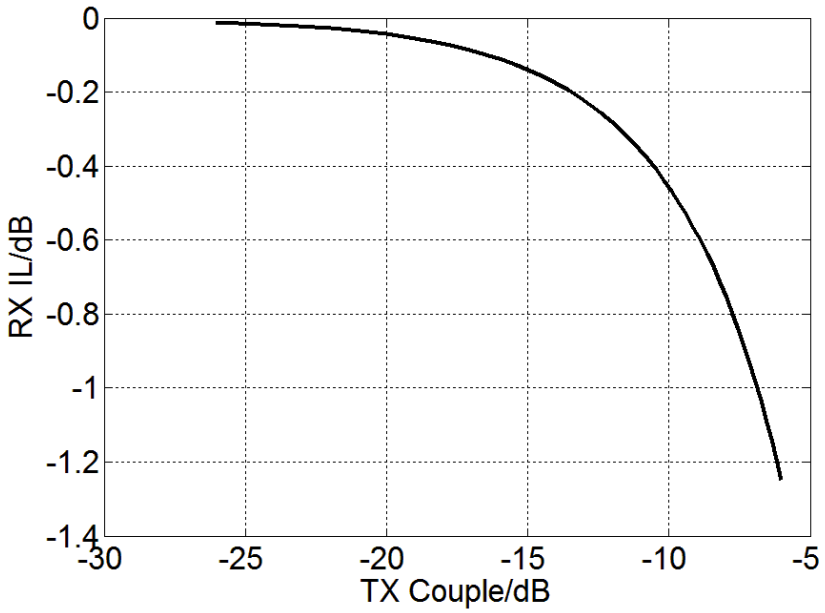

Fig. 3-15 RX Insertion Loss inside a Proposed FPC as a Function of Coupled-TX Strength

3.4 Implementation of FPC

3.4.1 HFSS Model

HFSS is a commercial finite element method solver for electromagnetic structures from Ansys. The FPC is designed and simulated in HFSS and the 3D view is shown in Fig.3-11.

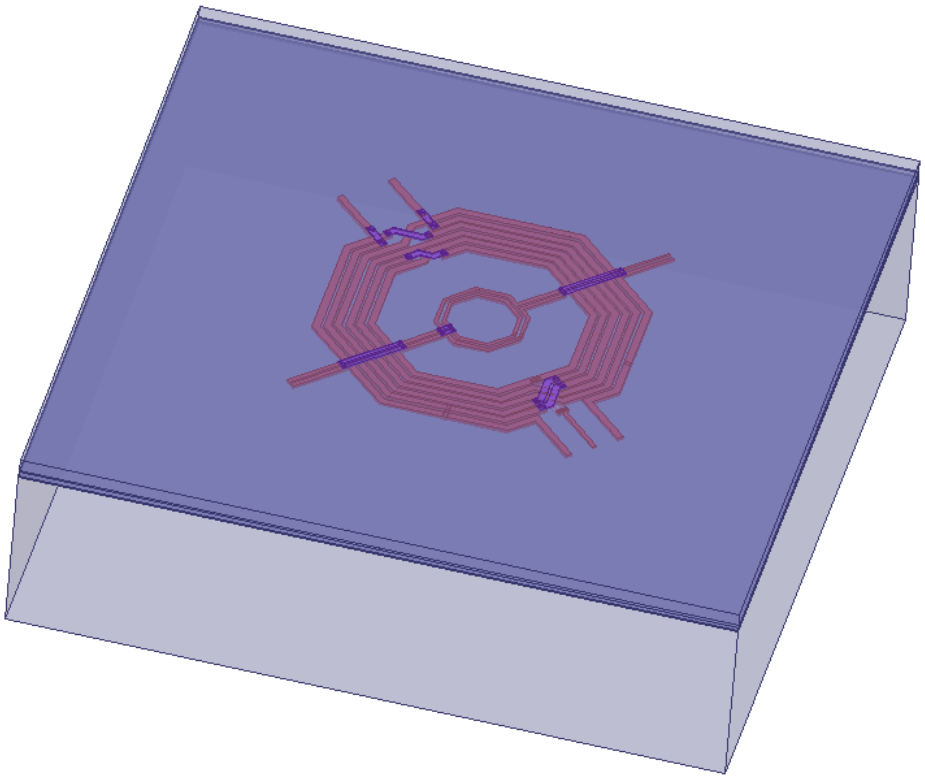

Fig. 3-16 Four Port Canceller Setup in HFSS

3.4.2 FPC Electromagnetic Simulation Results

The simulation results including the FPC characteristics (inductance, coupling coefficients, quality factor and insertion loss) and cancellation bandwidth are shown in Fig. 3-17.

3.4.2.1 S-Parameter

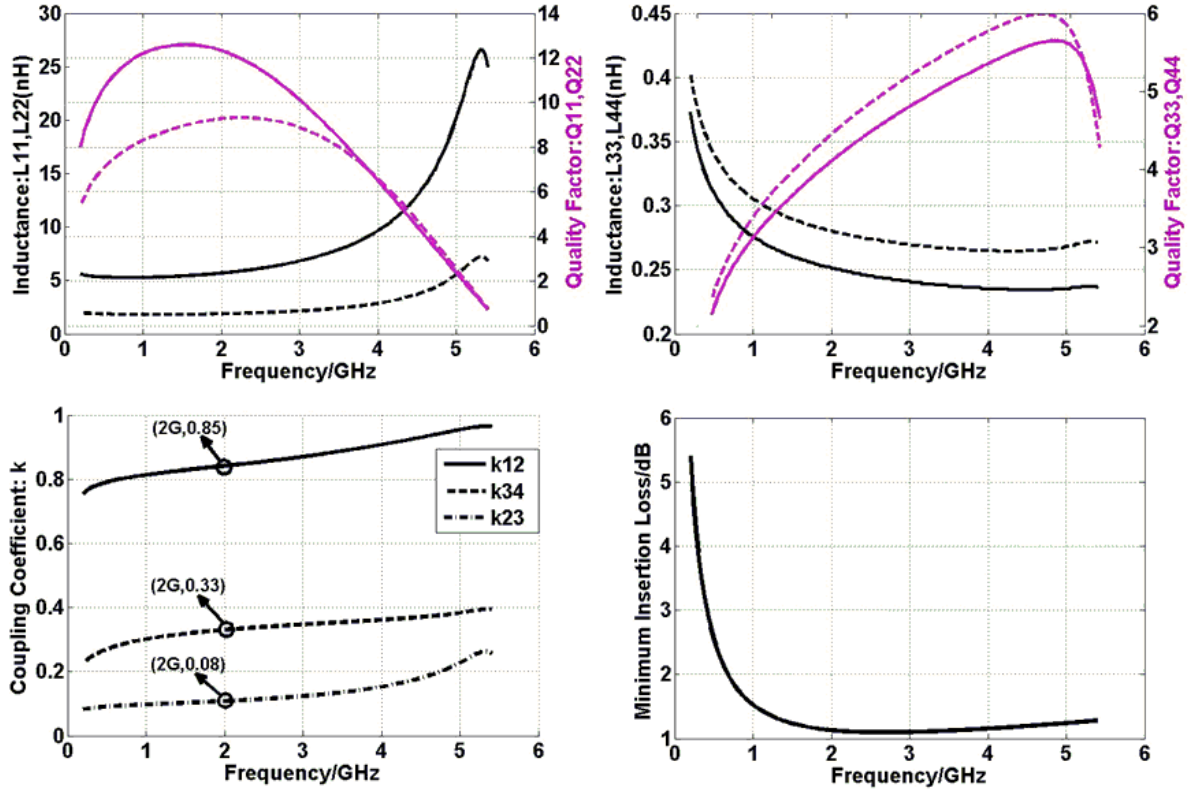

Fig. 3-17 FPC Characteristics

FPC characteristics can be extracted from n-port S-Parameter data using equations (3-1). The primary and secondary windings demonstrate strongly coupling ($k = 0.8 - 0.88$) while maintaining a high quality factor ($Q = 9 - 12$) tominimize the insertion loss ($IL \approx 1dB$). The third and fourth winding show moderate coupling ($k = 0.3 - 0.4$) with an optimized quality factor ($Q = 3 - 5$). The coupling between the primary/secondary and third/fourth windings are relevantly weak ($k < 0.1$), which is optimized for the insertion loss and tuning range.

3.4.2.2 Cancellation Bandwidth

Fig.3-18 demonstrates the cancellation bandwidth of the proposed canceller network. In the simulation, two signals are injected into the FPC, one is at port-one (Ant) and the other is at the input of the canceller network, which is made up of switch-cap bank and connected to port-three (coupled-Tx) after. The signal at port-one is an ideal wideband signal with no phase change across the frequency. However, in the other path, the coupled TX signal at port-three has a second order response from the canceller network and the loading inductors. The mismatch between the two paths reduces the cancellation bandwidth. From the simulation, the 20dB, 30dB and 40dB cancellation bandwidth are 80MHz, 27MHz and 8MHz, respectively.

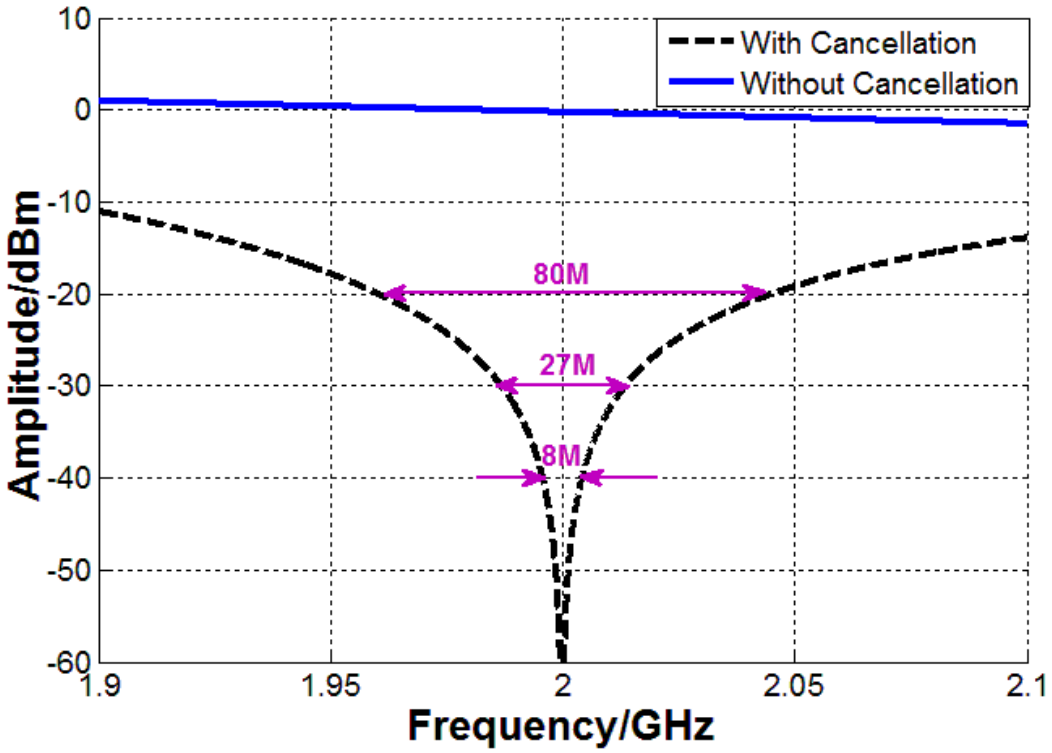

Fig. 3-18 Cancellation bandwidth simulation results of the Proposed Canceller Network.

[1] A. M. Niknejad and R. G. Meyer, “Analysis, design, and optimization of spiral inductors and transformers for Si RFIC’s,” IEEE J. Solid-State Circuits, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.

[2] S. S. Mohan, C. P. Yue, M. Hershenson, S. S. Wong, and T. H. Lee, “Modeling and characterization of on-chip transformers,” in Int. Electron Device Meeting Tech. Dig., Dec. 1998, pp. 531–534.

[3] T. Biondi, A. Scuderi, E. Ragonese, and G. Palmisano, “Analysis and modeling of layout scaling in silicon integrated stacked transformers,” IEEE Trans. Microw. Theory Tech., vol. 54, no. 5, pp. 2203–2210, May 2006.

[4] J. R. Long, “Monolithic transformers for silicon RF IC design,” IEEE J. Solid-State Circuits, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[5] O. El-Gharniti, E. Kerhervé and J. Bégueret, “Modeling and Characterization of On-Chip Transformers for Silicon RFIC”, IEEE Trans. Microwave Theory Tech., Vol 55, No. 4, pp. 607-615, Apr, 2007.

[6] M. Mikhemar, H. Darabi, and A. Abidi, “A tunable integrated duplexer with 50dB isolation in 40nm CMOS,” ISSCC Dig. Tech. Papers, pp. 386-387, Feb. 2009.

[7] M. Mikhemar, H. Darabi, and A. Abidi, “A Multiband RF Antenna Duplexer on CMOS: Design and Performance,” IEEE J. Solid-State Circuits, vol. 48, no. 9, Sep. 2013.

[8] M. Mikhemar, “Interference Cancellation in Software-Defined CMOS Receivers”, Ph.D. Dissertation, University of California, Los Angeles, 2010.

[9] S. Abdelhalem, P. Gudem, and L. Larson, “A tunable differential duplexer in 90nm CMOS,” RFIC Symp., pp. 101–104, Jun. 2012.

[10] S. Abdelhalem, P. Gudem, and L. Larson, “Hybrid transformer-based tunable differential duplexer in a 90-nm CMOS process,” IEEE Trans. Microwave Theory Tech., vol. 61, no. 3, pp. 1316–1326, March 2013.

[11] A. Shirane, Y. Mizuochi, S. Amakawa, N. Ishihara, K. Masu, “Digitally Controllable RF MEMS Inductor,” AMC, Albany Oct. 7th, 2010.

4 Circuit Implementation

4.1 Circuit Block Diagram

The circuit diagram of the integrated WCDMA front-end with passive TX leakage cancellation block is shown in Fig.4-1. In the proposed system, an LNA and an emulated PA are fabricated on the same die, to demonstrate a real scenario with various on-chip coupling schemes. The FPC is connected between an on-chip PA matching network and the LNA. The full cancellation path is shown in Fig. 4-1. To ensure both minimal loading on the PA output matching network and amplitude tuning range, the value of C_{1B} is optimized. In simulation, more than 1.5kΩ of parallel resistance is observed while maintaining a reasonable amplitude tuning range.

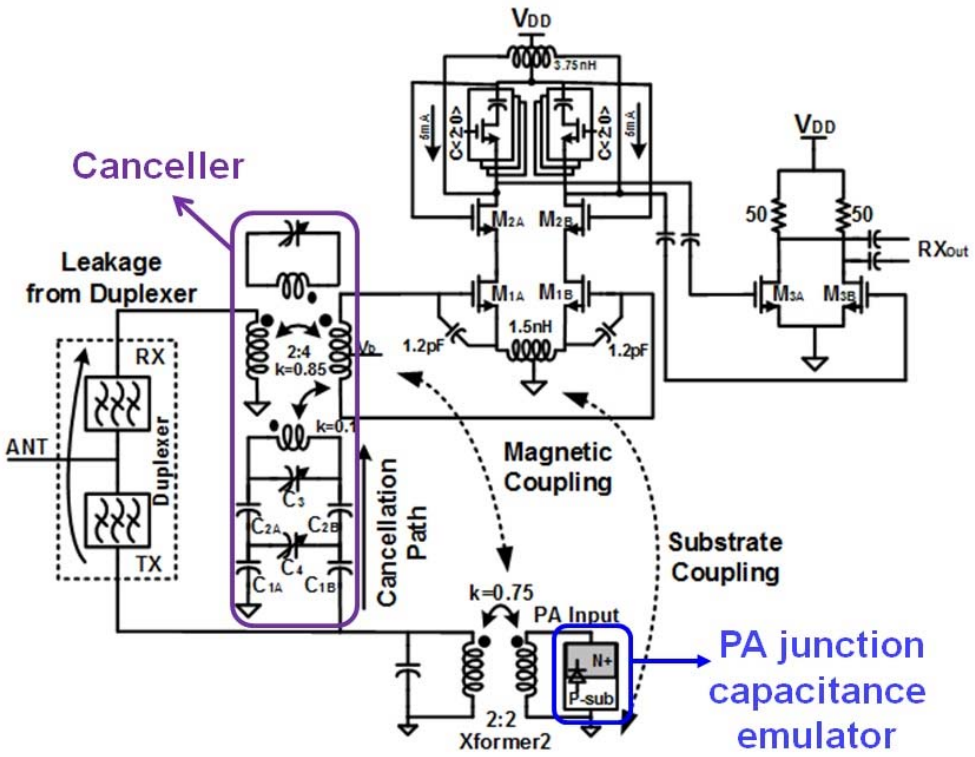

Fig. 4-1 CMOS WCDMA low noise amplifier with TX leakage suppression

The RX portion consists of a differential LNA driving a differential buffer. To achieve a good noise figure, the FPC provides some passive voltage gain (~6dB) by making the transformer turns ratio 2:4.

On the TX side, to capture the magnetic-coupling between transmitter and receiver coils, the PA output matching network was integrated on-chip. The input to the PA matching network can interface either a testboard PA, or an input signal may be applied with a signal generator, both of which deliver a P_{sat} of 30dBm. The matching network consists of a single-ended to single-ended transformer, which is designed to drive an antenna load of 50 Ohm.

Since there is no real PA on chip, in order to replicate the effect of substrate leakage from the PA, an nwell-to-psub diode has been added in-parallel with the primary winding of the PA output matching network. The size of the diode is chosen based on the total active region (NMOS device Area: 22400um^2) in a 2.4GHz 30dBm 90nm CMOS WCDMA PA in [1].

4.2 Simulated Impact on PA Loading

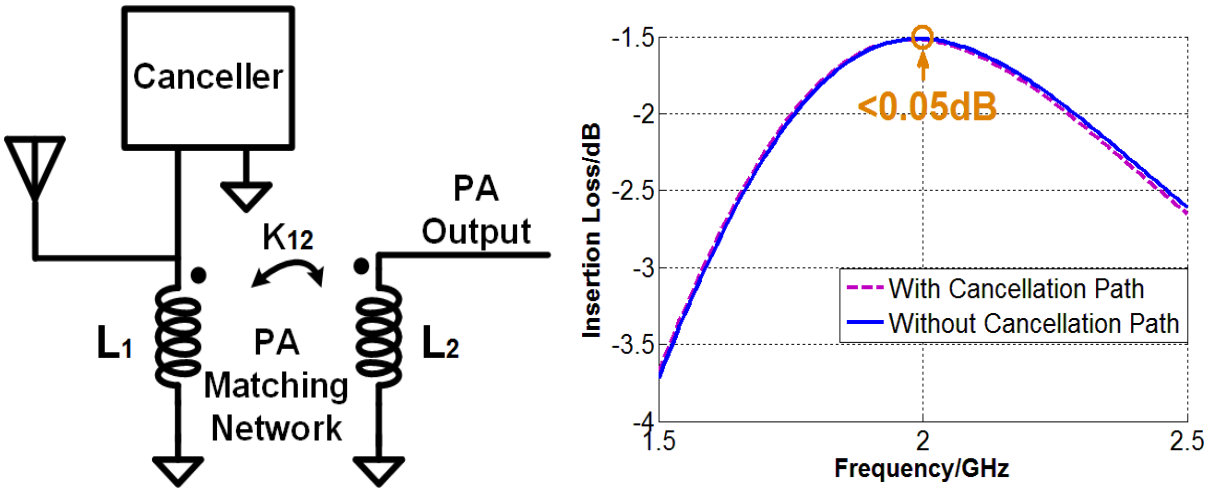

Fig. 4-2 Simulated loading effects of canceller on on PA matching network. Plot shows the TX insertion loss vs. frequency, both with and without cancelling network connected to PA output

Fig.4-2 are extracted simulation results which verify whether the FPC adds any undesired loading effects on the PA output matching network. At 2G, the matching network itself has an insertion loss of 1.5dB. Note that the extracted input impedance of the canceller is more than 1.5k Ohm, which is negligible compared to 50Ohm load of the antenna. From the simulation, the canceller adds a negligible TX signal path loss of 0.05dB.

4.3 Chip Die Photo & Testboard

The chip was fabricated in a 40nm 6-metal stack TSMC CMOS process and occupies 1.6mm x 1.3mm including bond pads, which is shown in Fig. 4-3. The die is wire-bonded and assembled with the testboard using chip-on-board packaging (see Fig. 4-4). The RX input and TX output are connected using a FBAR duplexer on-board. All RF signal lines on board are designed to use co-planar waveguide with ground shield (CPWG) to achieve 50 Ohm impedance matching. To minimize the on-board magnetic coupling between transmission lines, the TX input and RX output

traces are perpendicular to each other. The digital control signals are fed into the chip using opto-isolator to decouple any noise on the digital input lines from the chip. Regulators on board help reduce the supply noise and ferrite beads are connected between the critical RF signals supply/ground and other on-board analog circuits supply/ground to isolate any possible RF signals coupling from the power and ground planes.

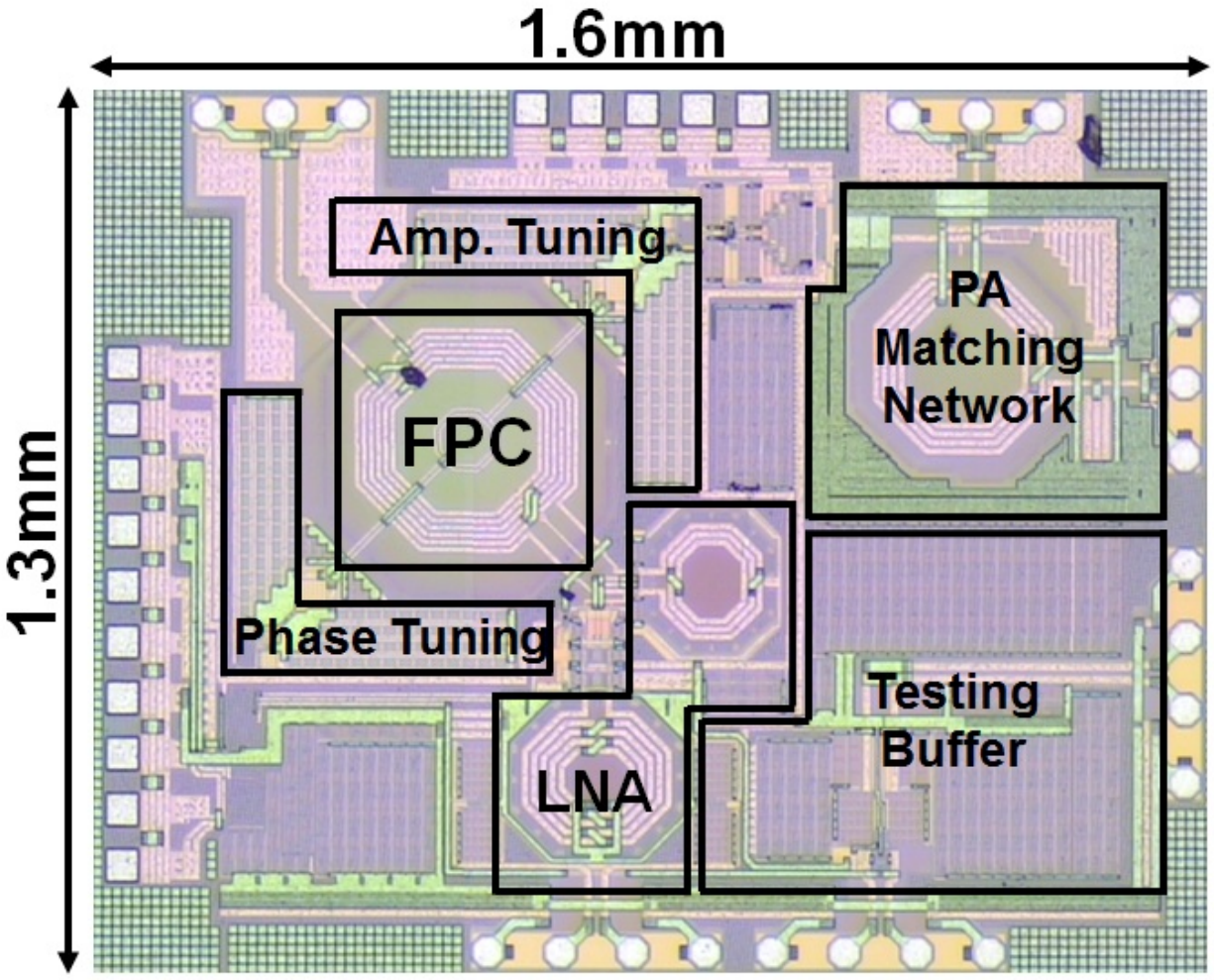

Fig. 4-3 Chip Micrograph

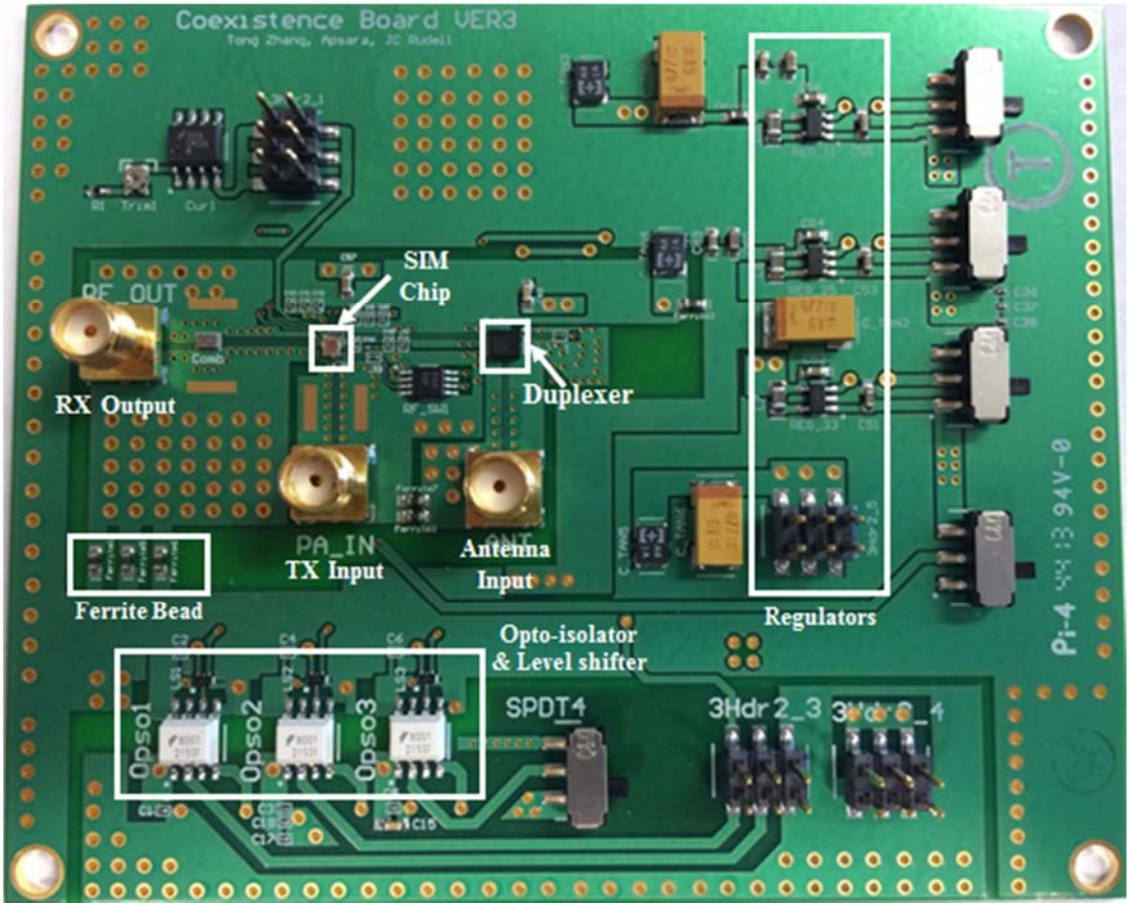

Fig. 4-4 Testboard Photo

[1] D. Chowdhury, C. D. Hull, O. B. Degani, P. Goyal, Y. Wang and A. M. Niknejad, “A Single-Chip Highly Linear 2.4GHz 30dBm Power Amplifier in 90nm CMOS,” ISSCC Dig. Tech. Papers, pp. 378-380, Feb 2009.

5 Simulation/Measurement Results

To test the validity of the canceller design, measurements were taken to characterize the amount of TX suppression, both with and without the duplexer filter. The LNA Noise Figure (NF) was measured with linearity for the in-band third order intercept points. The device is measured using an Agilent Network analyzer (N5247A) to characterize the receiver's S parameter. The LNA gain, input matching network and noise figure are measured with the on-board FBAR duplexer (Avago Technologies: ACMD-7612). For the TX leakage cancellation measurement, an Agilent vector signal generator (E4438C) supplies both a CW and WCDMA modulated signal to a discrete PA (Hittite Microwave Corporation: HMC457QS16G) input which has a capability of delivering 30dBm CW or WCDMA signal to the on-chip PA matching network. A laptop with an Aardvark I2C/SPI host adapter (Total Phase, Inc.) provides digital control bits to the chip via opto-isolators and level shifters. The measurement setup is shown in Fig.5-1.

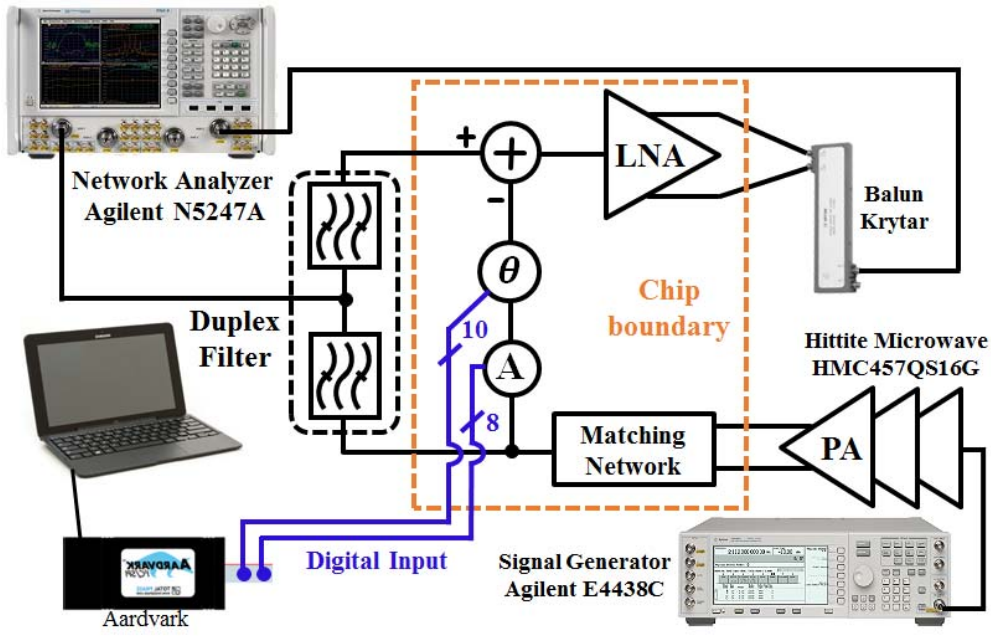

Fig. 5-1 Chip Measurement Setup

5.1 Receiver Measurement Results

5.1.1 S-Parameter Measurement

Since the duplexer has a 1.5dB insertion loss from the antenna side to the RX side, the peak conversion gain of the combiner and LNA is 20.4dB with a gain variation of 1.2dB within 60MHz RX band, see Fig. 5-2.

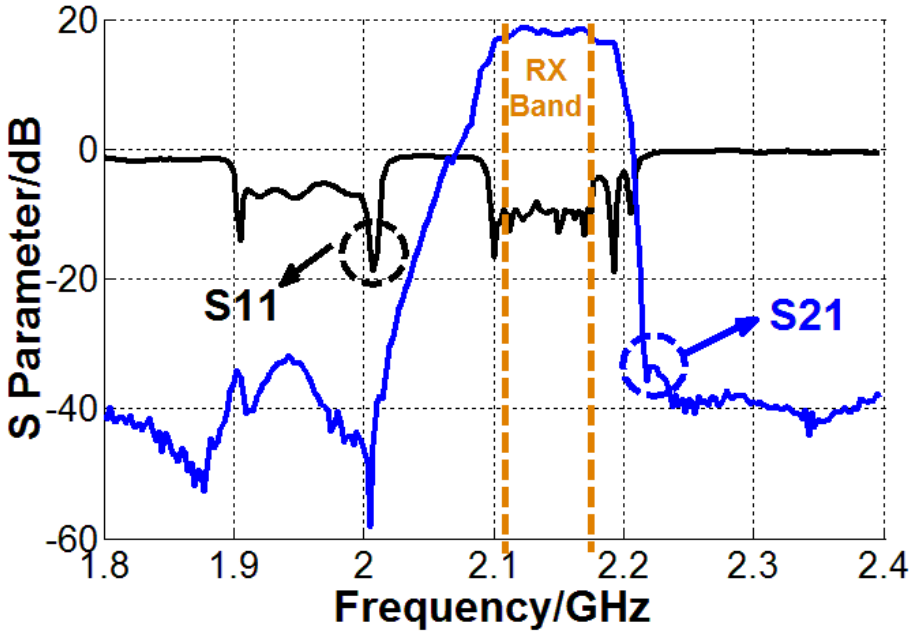

Fig. 5-2 Receiver S-Parameter measurement results. Plotted are the S_{21} from 1.8GHz to 2.4GHz and the S_{11} from the perspective of the antenna side.

5.1.2 Noise Figure Measurement

The RX measured double-sideband NF is 5dB. The estimated contributions to the overall NF are the following: 1.5dB attenuation from the duplexer, an additional loss of 1-1.5dB from the FPC/RX matching network, and 2-2.5dB NF from the LNA, see Fig. 5-3. The passive voltage gain

(~6dB) provided by the FPC, helps to lower the power consumption of LNA while achieving a reasonable gain and noise figure.

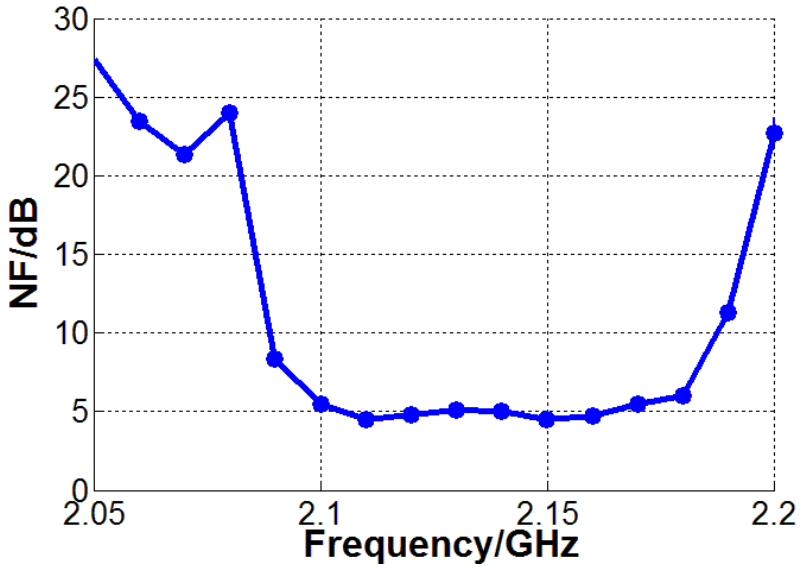

Fig. 5-3 Receiver Noise Figure

5.1.3 Linearity Measurement

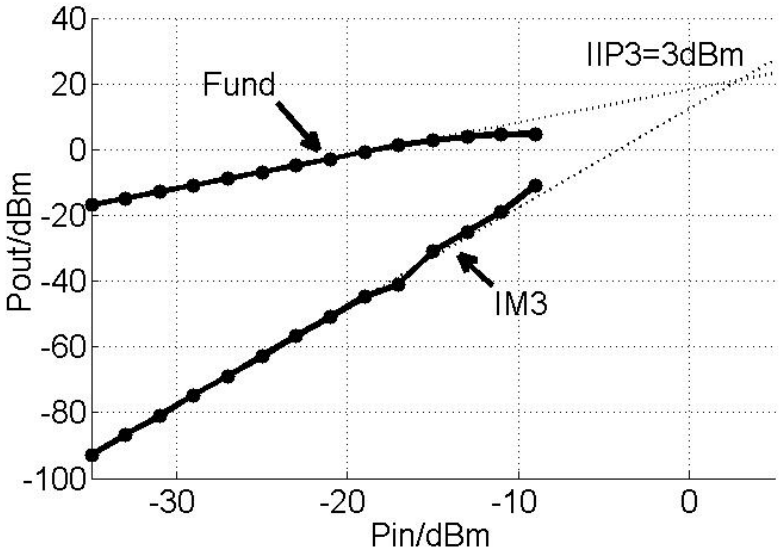

Fig. 5-4 Receiver In-band IIP3 Measurement

The linearity was measured using a two-tone test, with two tones at 10MHz offset from a 2.14GHz center frequency. The in-band IIP3 is 3dBm, see Fig.5-4. This performance is obtained while consuming 10mW from a 1V supply.

5.2 Measurement Results of Canceller

From the extracted simulation, the on chip phase tuning range was expected to be more than 280 degrees, which should be large enough to cover the duplex filter's phase variation over the frequency spectrum of interest. However, due to some unexpected large parasitic inductance in the cancellation path, and other undesired coupling (wire-bond coupling, on-board transmission line coupling and etc) from the PA to LNA, the on-chip phase tuning range was measured to be approximately 50 degrees. Thus, an additional on-board phase shifter was added to perform the actual cancellation measurement in the lab.

5.2.1 TX Leakage Suppression versus Frequency/Input Power

To measure the functionality of the canceller, two signals are injected, one applied to the duplexer while the other is applied to the TX input. By adjusting amplitude and phase inside the cancellation network, an average suppression of 23dB is observed with different input power levels over the entire TX band, see Fig. 5-5 and Fig. 5-6.

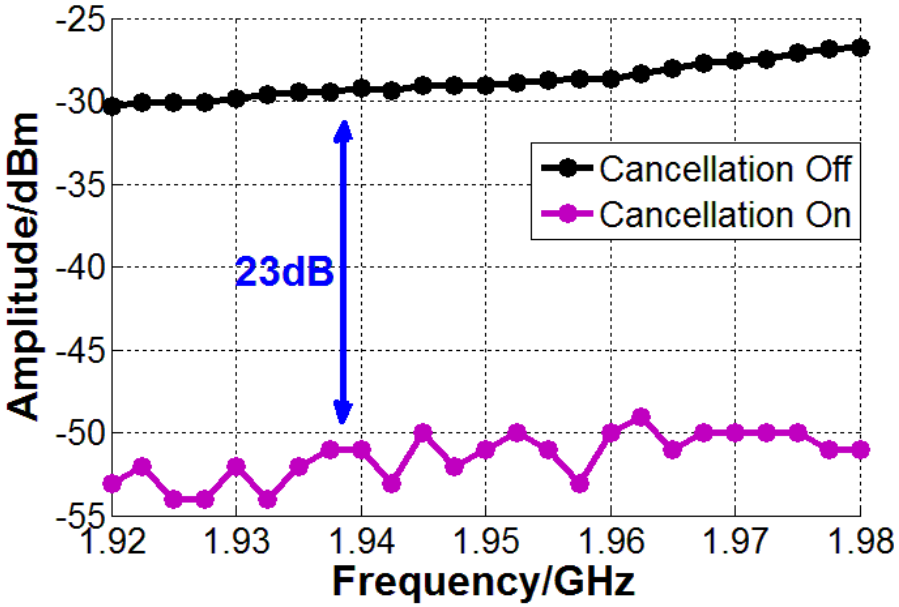

Fig. 5-5 TX Leakage Suppression versus TX Frequency. Measurements performed using a single CW signal.

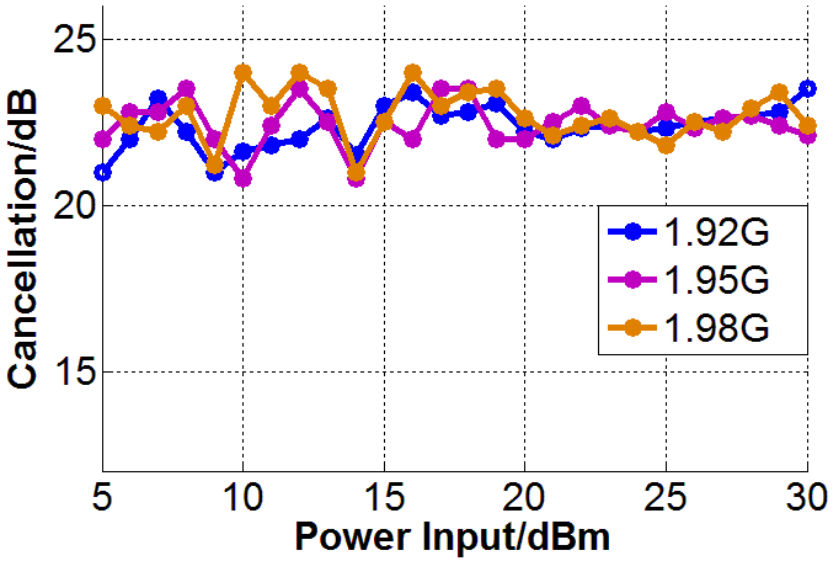

Fig. 5-6 TX Leakage Suppression versus Input Power. Measurements performed using a single CW signal.

5.2.2 Measured TX Suppression over Bandwidth

The cancellation bandwidth is measured in two steps. First, the cancellation is maximized at a center frequency by setting the phase and amplitude bits for maximum suppression. Then, holding this setting and sweeping the applied CW signal while measuring the amount of TX leakage cancellation at the output of the LNA. A minimum 20dB cancellation is achieved with 5MHz bandwidth which is sufficient to accommodate a 3.84 MHz channel bandwidth associated with the WCDMA standard (see Fig.5-7).

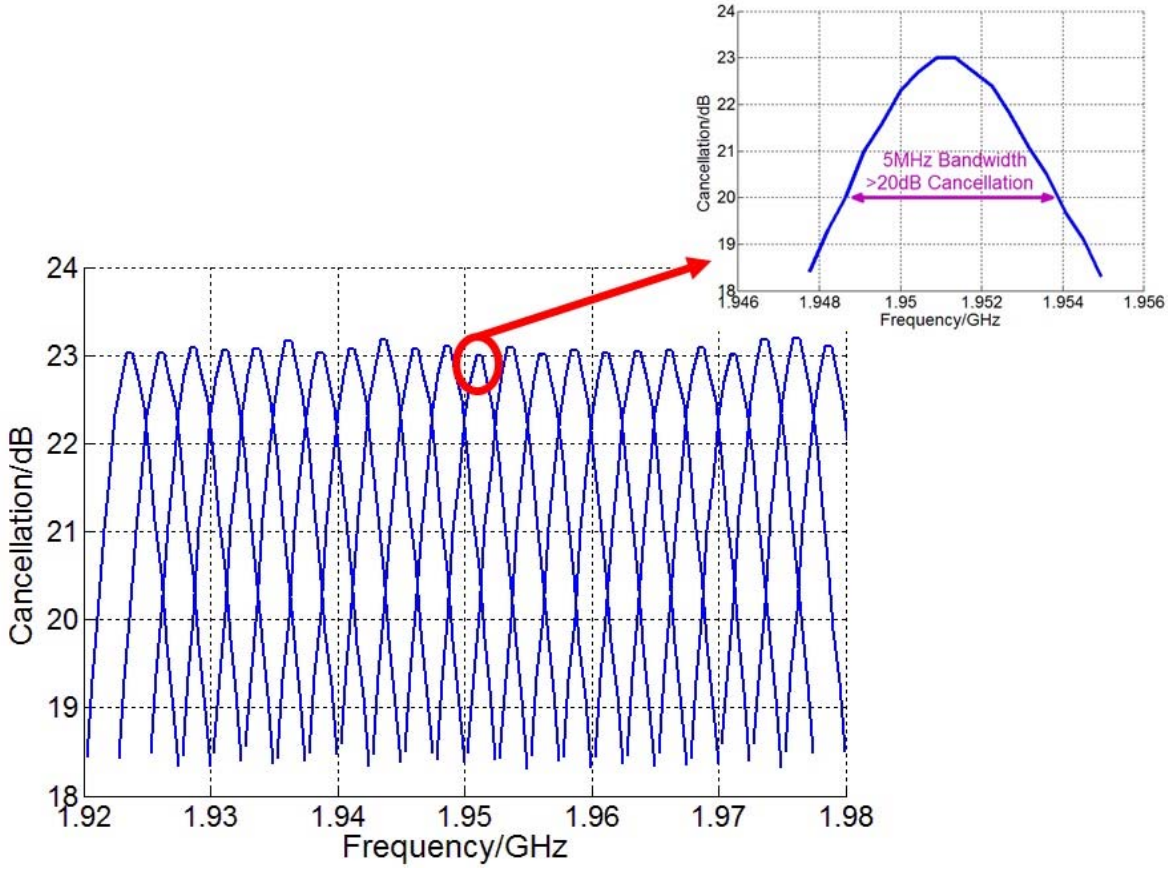

Fig. 5-7 Measured TX Suppression versus Bandwidth

5.2.3 Measured TX Suppression with a Real WCDMA Signal

A real WCDMA modulated signal was applied to the TX input while the LNA output spectrum was measured with both the cancellation network enabled and disabled. A minimum 20dB of cancellation is observed over the signal bandwidth which represents less than 1% of residual leakage power remains post cancellation, see Fig.5-8.

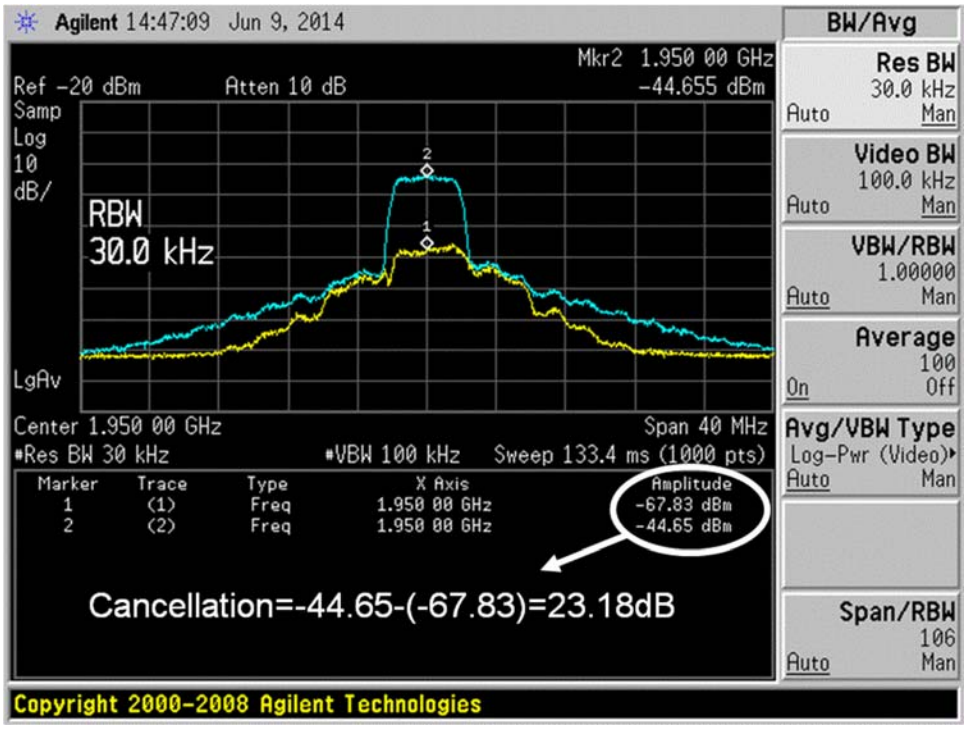

Fig. 5-8 Measured TX Suppression with a real WCDMA Signal

5.2.4 Measured RX Noise Figure with Large TX Interfere

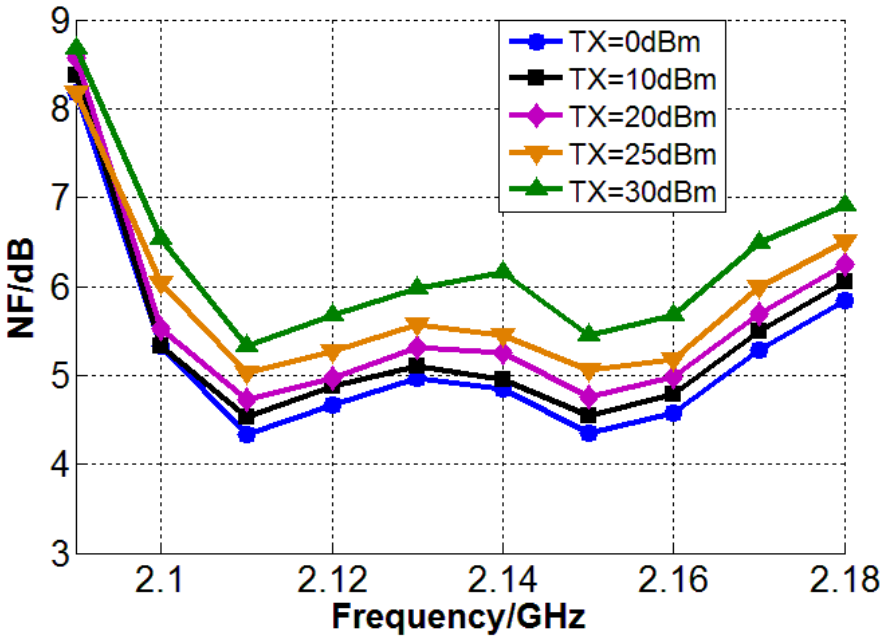

Fig. 5-9 Measured RX Noise Figure with Large TX Interfere which vary in power level from 0 dBm to 30 dBm

Fig.5-9 shows the noise figure degradation due to the TX leakage. The effect of a large TX leakage signal will be to modulate the gm of many devices in the signal path, and subsequently frequency translate noise from the bias circuitry to within the signal band of interest. This has the effect of raising the noise floor in the receive signal path. In addition, a large TX signal present in the receiver will cause gain compression, and potential interference from intermodulation distortion. All of these effects will work to degrade the reeiver's carrier-to-interfernece (C/I) ratio. To test these effects, the TX output power was modulated from 0 dBm to 30 dBm, and the NF was measured across the RX band, see Fig.5-9. From Fig. 5-9, a 30dBm TX output gives 1-1.2dB RX NF degradation when the canceller is off.

5.2.5 Measured RX Noise Figure with/without Large TX Interfere

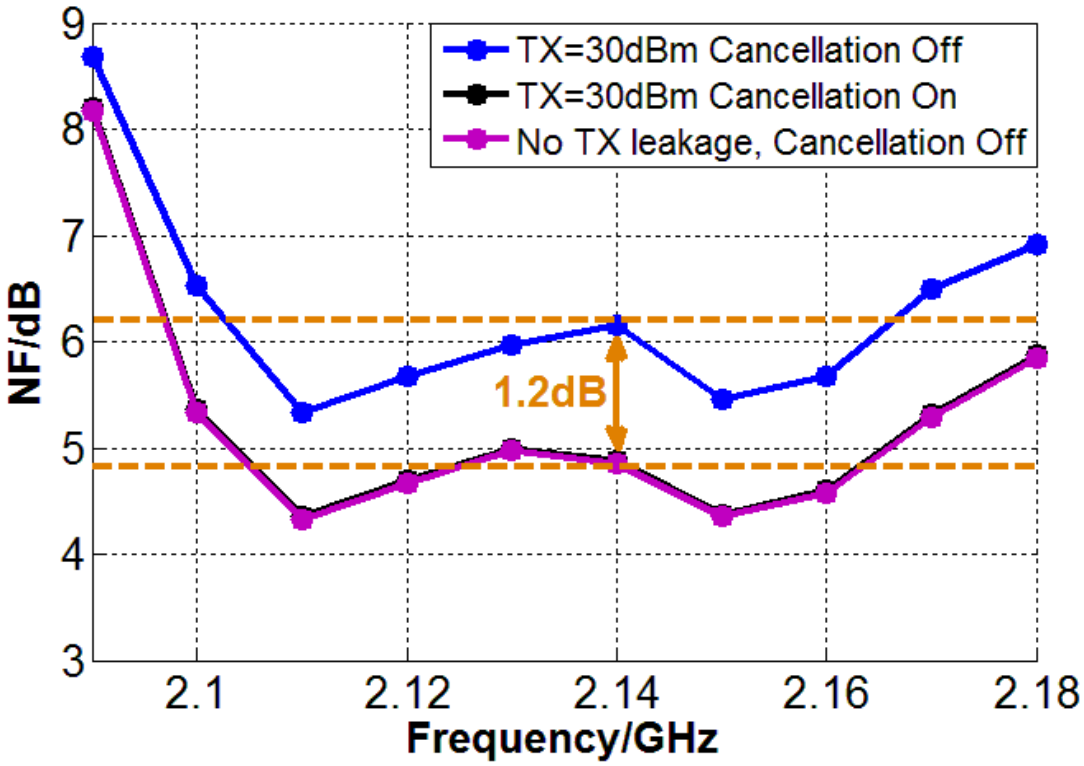

Fig. 5-10 Measured RX Noise Figure with/without large TX Interfere

Fig. 5-10 shows the measurement to test the impact of the canceller on the noise figure performance, a 30dBm CW signal is applied to the transmitter and the noise figure is measured with the canceller enabled and disabled. With the designed canceller on, the RX noise floor goes down and the noise figure improves by 1.2dB, which is nearly identical to the measured noise figure without leakage presented to the receiver (LNA).

5.2.6 Comparison and Performance Summary

The comparison and performance summary for the proposed integrated canceller network is shown in Table 5.1. A canceller structure is proposed showing promise with a measured TX suppression up to 23dB. The proposed leakage suppression technique introduces a negligible

penalty with respect to NF and power consumption, while state-of-art cancellers usually double the power consumption and increase the NF by at least 0.4dB through the introduction of the auxiliary cancellation path.

Table 5-1 Comparison and Performance Summary

	H. Khatri' 2010 JSSC	***H. Kim' 2013 TMTT	J. Zhou' 2014 ISSCC	*** This Work
Architecture	Active Filtering	Feed-forward Filtering	Active Two Port Cancellation	Transformer+ Filtering
Technology/VDC	65nm/2V	180nm/1.8V	65nm/?	40nm/1V
TX Suppression(dB)	6.5	23.4	>30	23
NF(dB)	4.9	2.84	5	*5
NF degradation due to leakage cancellation(dB)	1.8	0.44	0.8	≈0
RX Gain(dB)	45	25.4	19-34	*18
RX Power Consumption(mW)	**44	16.38	75-83	10
Canceller Power Consumption(mW)	***48	18.9	13-72	≈0

*RX Gain/ NF measured with front-end duplexer, which has 1.5-2dB loss.

** Power consumption includes LNA only.

***RX includes only the LNA.

6 Conclusions

The focus of this thesis was the exploration of transmitter leakage mitigation techniques for traditional frequency division duplexing (FDD) radios. In FDD systems, due to the large TX blocker signal leaking to the receiver input, stringent IIP2 and IIP3 specs are posed for the RX design, which usually increases the RX power consumption. Several recent efforts attempt to mitigate the self-interference problems and most of the work reported so far uses active methods to do the leakage cancellation, which is questionable from a power and noise perspective.

An ideal TX leakage canceller should behave as follows:

- Introduce no noise, or additional power, while using minimal silicon area.
- Perform cancellation at the RX input to relax required RX selectivity performance.
- Canceller presents negligible loading (high impedance) to the PA output.
- Minimize loss and LO-feedthrough in the RX/TX signal chain.
- Stable under all conditions.

In this thesis, a passive transmitter leakage suppression technique is proposed for FDD radios. A new structure, Four Port Canceller (FPC), which introduces minimal noise, area and power consumption is described and analyzed. An example of this technique is applied to the design of a WCDMA front-end and is implemented in 40nm CMOS process. A measured cancellation of 20dB is achieved with negligible power consumption and noise penalty over 5MHz signal bandwidth.

Potential applications for this techniques include the current FDD Radios, Wi-Fi Bluetooth coexistence and any radios dealing with a non-negligible self-interference signal from the transmitter.

In the resulting prototype chip, the idea of coupling a small component of TX-replica using transformers is verified successfully, however, due to the unexpected coupling on-board, on-chip and parasitic inductance, the phase tuning range was significantly limited by these effects. One of the most important things we learned from this chip is in order to reduce the un-expected coupling on-board, it's better to have RX down-converter and TX up-converter on chip. Injecting a baseband signal into the chip rather than making inputs/outputs all RF signals have less on-board coupling issues.

Future research in this area will focus on two ideas. The first one is how to make an inductor-less fully passive leakage canceller. Although in the prototype device the canceller is absorbed into the LNA input matching network, which introduces minimal additional area, however, most of the wireless products now use single-ended input LNA to remove the front end matching network (single-ended to differential transformers) to minimize the silicon area due to the cost. Finding a way to design an inductor-less passive leakage canceller becomes a critical issue. The second one is how to improve the cancellation to 60dB or even more than that. In the existing FDD system with approximately a hundred megahertz guard band between TX and RX, the duplex filter already gives 50dB isolation between TX and RX. Therefore, an additional 20-30dB TX leakage suppression is sufficient to avoid gain suppression, noise figure degradation and linearity issues. However, if later we try to remove the duplex band or make full duplex radios to improve the spectrum efficiency, 20-30dB TX leakage suppression may be insufficient. Searching for a way to improve the TX leakage suppression also makes an interesting and meaningful research.