Transcutaneous Induction-Power and IR-Data Linked, Long-Duration, Implantable Neural-Interface System

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Abstract

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Efforts to combat the devastating effects caused by neurological disorders and injuries have been a topic of research for decades. Presently, neuroprosthetics, like cochlear implants, are in common use and effectively restore some degree of biological function. This field, however, is far from mature and the development of neuroprosthetics for other biological systems is extraordinarily challenging.

This dissertation presents a system-level design of an implantable, fully-wireless, neural-interface research platform. The implantable device, designed for implantation into the abdominal region of a rat, can reside in an enclosure cavity measuring 18.0 mm wide, 26.0 mm long and 12.49 mm high. It includes an MSP430 running a custom operating system and 264 Mbit of non-volatile memory to store recorded neural data from an Intan RHS2116. An onboard lithium-ion battery, which is recharged by wireless power, provides over ten minutes of energy for a neurological stimulation and recording experiment. Data transfer and wireless power are accomplished via interaction with a custom-designed base station.

Transdermal wireless communication is achieved with IR communication in the near-infrared region. Downlink data transmission was measured at 115.2 kbps through 5.5 cm of free space, 0.8 mm of sapphire crystal and 4.0 mm of phantom tissue with a packet-loss rate of 0%, given a sample of 10000 transmitted packets. Uplink communication reached 2

Mbps with zero packet errors out of a sample of 10010 transmitted packets at a separation distance of 2.7 cm through a combination of free space, 0.8 mm of sapphire crystal and 3.0 mm of phantom tissue.

Inductively-coupled resonators, operating at 13.56 MHz, provide wireless-power capabilities. 243 mW of power was delivered, post rectifier, to the implant voltage-regulator output at 2.3 cm. End-to-end wireless-power efficiency at this distance was 3.34%, and at a distance of 3.2 cm, 195 mW was successfully transferred.

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Chapter 1
INTRODUCTION

1.1 Towards a Neural Prosthetic Research Platform

1.1.1 Neurological Disorder and Injury Background

Effectively treating the devastation of neurological disorders has remained extraordinarily challenging. Exacerbating the situation, the population of those afflicted by neurological disorders is ever-increasing [21]. While this trend may be attributed to longer life expectancies and increasing population numbers, it is alarming nonetheless. Feigin, et al. revealed in their study that between the years of 1990 to 2015, deaths due to Alzheimer's and other types of dementia increased by 114%. Parkinson's disease, which claimed 117,000 lives globally, jumped by 149.8% over the same 25-year period.

Traumatic spinal-cord injuries (SCI), which have severe life-altering consequences, occur at high-incidence rates. According to Singh, et al. [81], the prevalence of SCI was highest in the United States (906 per million). Given that the leading cause of SCI is due to automobile accidents, it is highly unlikely these rates will recede anytime soon.

Irrespective of cause, disrupted neural communication pathways can severely diminish the quality of life for these patients and place heavy burdens on care givers, family and ultimately, society. Unsurprisingly, repairing and understanding neural pathways has actively been researched for many decades. In the 1950s, electrical activity was studied with wires, followed by patch clamps [12]. The 1980s and 1990s marked significant improvement in multi-electrode arrays, like the Utah arrays. Research related to neuroprosthetics and brain-machine interfaces led to decoding algorithms capable of reading real-time brain activity and translating it to robotic joint motion. Clinical trials in 2004 enabled paralyzed patients to control computer cursors and robotic arms.

Success in these various arenas inevitably generated more complications. Maintaining a high signal-to-noise ratio (SNR) with probes became problematic for long-term implants [39]. The cause was neuronal death and glial scarring, thereby driving additional research into "foreign-body response" or bio-compatibility. On the other hand, the implementation of electronics for biological tasks revealed the importance of low leak-rate packaging and robust electrodes that were not only bio-compatible, but resistant to oxidation. Indeed, the last decade has seen substantial development in this field, but significant challenges remain.

1.1.2 Neuroprosthetic Technology

Despite major challenges in the pursuit of biological function restoration, whether motor or sensory related, neuroprosthetics, in general, have been available and used medically for decades. The cochlear implant is a well-known and relatively mature prosthetic benefiting many thousands of patients worldwide [92]. Present-day cochlear implants benefit from multiple microphones and embedded processors, and they restore some sensory functionality by electrically stimulating the hearing nerve. Yet, the performance of cochlear implants has seen only incremental improvement over the last 30 years.

In contrast to cochlear implants, other sensory prosthetic technology is much less mature. Visual prosthetics, for example, are a major ongoing research field. While these devices restore some vision, full-color images and motion are still problematic [86]. Historically speaking, three different visual prosthetics have been approved for market. However, all three of these devices are no longer available [8].

For most, the concept of restoring motor functionality is immediately associated with walking or moving body parts. Indeed, neuroprosthetics designed to restore such motor functionality form a major branch of ongoing research, which generally speaking, is in its infancy. Although motor functions such as walking are often considered the primary desire of paralyzed patients, returning functionality of seemingly simple and overlooked functions are often more important. For example, urinary and fecal incontinence is a primary concern shared amongst paraplegics and quadriplegics [3]. Research and development into bladder

control devices has been active for decades and today sacral neuromodulation devices are produced by a handful of manufacturers. The most recognizable devices are manufactured by Axonics and Medtronic. Once implanted, the devices are manually controlled by the patient to treat urinary retention, overactive bladder and urge incontinence. Present day research aims at the ultimate goal of a closed-loop neuroprosthesis for bladder control [13].

1.1.3 GSK Innovation Challenge

The work in this dissertation traces back to December of 2013 when GlaxoSmithKline (GSK) launched their Bioelectronics Innovation Challenge (BIC). Stated in their full-criteria document [24], the goal of the challenge was to promote the development of a neural recording and stimulation/blocking device that would "elicit functional changes" for a targeted end organ. Furthermore, the device was to be implanted for 60 days, while maintaining reliable, consistent operation. The urinary bladder was selected as the target organ, and the pelvic nerve was to be neuromodulated to elicit contraction or suppress contraction of the detrusor muscle.

The design of the device was relatively open ended. Therefore, possible stimulation methods included electrical, optical, etc. Irrespective of the technology, the neural data was specified to be recorded with a minimum bandwidth of 12 kHz. The raw, original recorded neural data is then sent to a base station. However, the device must be fully implanted, and have no tethering or backpacks. Therefore, the implantable device must provide a means of wireless communication.

1.1.4 Design Considerations

A device with the aforementioned capabilities requires research and design methodologies from multiple disciplines. From a physiological perspective, interfacing with the peripheral nervous system depends on many factors. For electrical stimulation, interfacing conductive electrodes introduce a unique set of challenges, especially for reliable long-term operation: electrical isolation, biocompatibility, and corrosion-resistance [39]. Furthermore, the material

of the electrodes is extremely important as is the attachment method (e.g., hook, ball-tip, cuff, etc.). A suitable location for recording and stimulation must be identified and verified. Essentially, a model or method is established, often painstakingly [94].

Additionally, the implantable device must be packaged in a durable, biocompatible, low leak-rate, electromagnetic (EM) field compatible material. For example, titanium is a standard material for pacemakers; however, metals inherently present compatibility issues with EM fields, which would be detrimental to wireless power and communication.

Furthermore, the implantable device must remain operational for weeks. Even if reliable wireless power is guaranteed, energy storage reserves are still required. For example, if sufficient power cannot be transferred continuously for a particular operation, energy must be stored until adequate capacity is reached, and then the stored energy will be used to complete the task.

Most importantly, the safety of the animal and users must be taken into consideration. In general, storing energy at high densities comes with some level of risk. A malfunctioning battery, as part of an implant device, would have catastrophic consequences. While energy efficiency is paramount from a performance perspective, heat generated from such processes requires careful management. A conservative goal, one which was applied during the GSK BIC, is to ensure tissue temperature did not deviate by more than $1°C$. The reasoning is based on research of deep-brain stimulation, where an increase of $1°C$ can result in disruption of the blood-brain barrier function [18].

1.1.5 Enabling Technology and Challenges

Effective wireless powering of medical devices has been accomplished both mechanically and electromagnetically. The former leverages acoustic methods, like piezoelectric, while the latter may involve both radiative and non-radiative techniques. Safe and practical inductively-coupled wireless power transfer (WPT) has been demonstrated frequently in literature [44], and therefore is the method investigated in this work. Wireless power via induction is commonly used, and the theoretical concept is modeled by Faraday's and Lenz's

laws, which are coupled in Maxwell's equations. Of course, Nikola Tesla extended this theory into various inventions, but it is only in recent times that it has been accepted as a practicable technology. The research field ballooned following publications presenting the benefits and practical usage of high quality factor (Q), magnetically-coupled resonators (MCR) [43, 49]. Kurs, et al. reported transferring 60W with roughly 40% efficiency at distances larger than 2 meters. In 2011, Bonde, et. al [7] presented a wirelessly-powered ventricular assist device with coil efficiencies over 91%.

Low-power wireless communication is critical to energy-constrained implantable devices. Active radio frequency (RF) transceivers, even the lowest powered variety, consume significant amounts of energy when transmitting: tens to hundreds of mW. On the other end of the power spectrum, radio-frequency identification (RFID) leverages backscatter communication to efficiently communicate with an interrogating RFID reader. The Wireless Identification and Sensing Platform (WISP) [76] expanded on the traditional fixed-function RFID tag by integrating an MSP430 microcontroller to both emulate the standard RFID communication scheme and perform various sensing and computation tasks. However, RF transmission necessitates careful design of an antenna, which becomes even more challenging when confined to a small implant. Of course, in-band load modulation of the wireless power receive (RX) coil is possible, but high bandwidth is inherently at odds with high-Q coupled resonators. Consequently, hybrid or low-power active methods may be the only viable options.

Advancements in integrated circuit technology provide an opportunity to significantly reduce the implant footprint or increase device performance. The ICs used in this research occupy less than 50 mm^2, with many being less than 10 mm^2. Modern microcontrollers, like the MSP430 used for WISP and in this work, have more than adequate performance and available peripherals. Non-volatile memory (NVM) technology, especially flash, enables many Gbit of information storage in tiny form factors, albeit at the expense of considerable power consumption.

While electronics have experienced significant reduction in size due to advanced processes, batteries have not benefited at the same rate. Even state-of-the lithium polymer batteries

occupy significant portions of a device's overall volume. Nonetheless, as is shown in this dissertation, modern-day lithium-based batteries are more than capable of supporting small, implantable devices.

1.1.6 Design Approach

The design of this system covers a relatively wide breadth of topics and investigates the feasibility of a practical, fully-wireless, implantable research platform that can reliably collect neural data following a stimulation event. Thus, the context of this application is critical when considering the work presented in this dissertation. The implant, with strict design constraints, requires that many circuits sacrifice more robust and efficient performance in some cases. This trade off is analogous to that of analog circuit design in nanometer-scale CMOS processes that favor digital circuits. Nonetheless, some of the subsystems presented here achieve respectable performance.

The inherent constraints of the implant device drove the entire design. In general, the design revolves around four fundamental aspects: physical dimensions, biocompatibility, function, and performance. The physical dimension requirement is obviously limited by the size of a rat, more specifically the abdominal region. From an electrical engineering perspective, the physical dimensions and bio-compatibility are largely dependent on desired function. Therefore, final function and physical design were born out of several iterations stemming from the GSK BIC. WPT to an implant device is highly dependent on geometry. Storing energy and neural information requires physical volume. As it turns out, the physical dimensions and performance hinge on the wireless-power RX coil, NVM ICs, but mostly the battery.

The base station development, while critical to the system function, was designed as support equipment for the implant. When commercial off-the-shelf (COTS) equipment was available, it was integrated into the base station. Also, the scope of this thesis does not include an in-depth optimization of certain components, thereby relaxing many of the base-station design constraints. The wireless-power transmit (TX) modules, for example,

integrated into the base station system, were designed from high-power operational amplifiers (op amps). While there was some motivation to compare a linear amplifier's harmonic interference on the sensitive infrared (IR) RX and neural interface (IFC) hardware with that of a much more efficient state-of-the-art Class E power amplifier, the primary consideration was form-factor and convenience.

1.2 Proposed System

While the GSK BIC has long since concluded, the demand for such a research platform still exists. The development of closed-loop neuroprosthetics is extraordinarily challenging. While the ability to decode neural signals to infer human intent is one such challenge, achieving a reliable, long-term sensing interface is likewise difficult [59]. The work presented in this dissertation proposes a system-level design for achieving many of the aforementioned goals.

Although the design rules of the GSK BIC challenge are no longer applicable, many of those design rules were, nonetheless, used as guidelines as development proceeded. Aside from 3-D printed enclosures and custom PCBs, all other components were purchased from familiar vendors. Adhering to this guideline was not an arbitrary decision, as it demonstrates the viability of such a research platform. Of course, many of the designs proposed in this dissertation may be translated and optimized into IC technology. In fact, that is the ultimate goal.

As mentioned above, the complete end device is comprised of two separate but interrelated components: implant and base station. To reiterate, these components do not collectively function as a neuroprosthetic. They are more accurately described as a research tool to accelerate development of future neuroprosthetics. The implant, as discussed above, is designed to reside in the abdominal region of a rat under test (RUT) for extended periods of time. It is responsible for interfacing with the pelvic nerve via a neural IFC, collecting data, and transferring the data to a remote base station. The neural stimulation and recording event must be captured in the absence of wireless power. Therefore, the implant must operate on stored energy for several minutes.

To achieve these design goals, considerable effort was placed in finding the smallest form-factor components that provided adequate functionality with acceptable power dissipation. The Intan RHS2116 "Digital Electrophysiology Stimulator/Amplifier Chip" serves as the neural IFC in this system, while data storage is provided by a NVM bank of four ICs providing 264 Mbit of NOR flash memory. Both of these components are controlled by the MSP430FR5994 microcontroller running a custom operating system (OS). A lithium-ion battery, Murata UMAL small-energy device, provides required energy demands with a nominal voltage and capacity of 2.3 V and 12 mAH, respectively. During bench-top testing, this battery provided 13 minutes of continuous RHS2116 sampling and programming of the onboard flash memory. The unique chemistry of this battery provides long cycle life, high charge/discharge rates and improved safety characteristics relative to other lithium-ion batteries.

As previously mentioned, the implant device acquires energy via wireless power transfer. Collected neural data is transmitted to the base station via an infrared (IR) optical channel. The implant is also controlled by the base station via the same optical channel. Given the ultimate goal of chronic implantation, the RUT would be sedated, but free to move about an enclosure. Of course, this complicated the design for effective wireless power transfer and optical communication. While outside the scope of this dissertation, an array of wireless-power TX coils would line the floor of the enclosure, thereby presenting wireless power over the majority of the usable area. Such a device is presented in [80]. While the integration of IR transceivers with the wireless-power TX array has not been investigated, the research in this paper strongly suggests it is feasible.

While an array of wireless-power TX coils with integrated IR transceivers would provide significant flexibility, it would be impossible to maintain an effective and efficient power and data link with the RUT at all times. Quality inductively coupled wireless-power transfer, and especially IR communication, is highly dependent on separation distance and relative alignment between TX and RX components. Therefore, the scope of the design shall assume a nominal use case where the rat is on all fours with the implant residing about 2.3 cm

away from the enclosure floor. Considering that the implant device RX coil is aligned in a co-planar manner with the TX coil, and if the IR components are mounted co-axially with the coils, then good inductive and optical coupling should be achieved as the RUT moves about the enclosure. In this work, 194 mW of wireless power was delivered to the output of a regulated buck converter at a distance of 3.2 cm. Furthermore, 243 mW was delivered to the implant with an efficiency of 3.34%. For the optical communication, data was transferred from the base station to the implant at a distance of 5.5 cm plus 0.8 mm of sapphire crystal and 4 mm of phantom tissue at 115.2 kbps with a 0% packet-loss rate (PLR) given a sample size of 10000 transmitted frames. During uplink tests, data was transferred off the implant at 2 Mbps with 0% PLR over 10010 transmitted packets through 0.8 mm of sapphire crystal and 3 mm of phantom tissue over a total distance of 2.7 cm.

1.2.1 Similar Work

A brief review of literature reveals the existence of devices with functional overlap to what is proposed in this dissertation. The majority of research focuses on the stimulation and recording front ends for implantable devices. Literature is replete with application-specific ICs (ASICs) targeting this application space. System oriented publications for wirelessly-powered implantable devices are less common. However, very few were identified that propose a complete system solution. A headstage system for a rodent, which is also wirelessly powered, is presented in [50]. In this paper, an ASIC is presented that is compatible with a previously developed system. The system is capable of recharging a super-capacitor or battery; however, being a headstage, the majority of the components are external. A 64-channel recording device, which is fully implantable, is presented in [61]. In this research, the implant leveraged inductive wireless power at 13.56 MHz and was capable transferring up to 100 mW. Non-volatile memory (NVM) was limited to that available on an MSP430 microcontroller. Furthermore, the implant was only operational when it was externally powered. Perhaps the most recent and closest system approach was developed by a team at the University College of London [54]. This platform featured a Qi-standard wirelessly

powered implant, capable of more than 100 mW at 2 cm. Similar to the system presented in this paper, the wireless power is used to recharge a lithium-ion battery for independent, offline stimulation and recording. Similar to above, the available on-board NVM was limited to what was available on the microcontroller: 128 kB. Final enclosure design is unclear, and the device measured 29 mm x 20 mm x 13 mm.

1.3 Data Collection Strategy

A brief commentary on the data collection is warranted. As shown in chapter 2, two different implant devices were used to accelerate the design process and more effectively collect data. To date, the latest functional revision of the true-scale implant is still under construction at the PCB assembly house. Therefore, wireless power and communication data have been collected with the larger version. All attempts were made to ensure that any differences in expected behavior were mitigated. Additionally, some internal implant power numbers, which would have been otherwise impractical to obtain, were collected with the assistance of a custom PCB, which allows the use of bench-top power supplies and multimeters.

1.4 Document Format

This dissertation will present the design details and key findings in the following chapters. Given the complexity of the system, the organization of the chapters will first provide a top-level system overview, which illustrates the interrelation between major subsystem blocks. Then the subsystems will be presented based on their dependence to other subsystem blocks. For example, the Intan RHS2116, which integrates both neural recording and stimulation, is the only known COTS IC with such capabilities that also satisfies the design goals. Likewise, the information storage specifications limit possible NVM solutions. Consequently, the remainder of the system design is a function of the neural IFC and NVM devices. While in-depth testing of the RHS2116 is beyond the scope of this work, baseline device metrics are discussed, as well as a more thorough discussion on the NVM system. Therefore, the implant neural IFC & NVM subsystem is presented first in chapter 3.

The following chapters introduce the remaining subsystem blocks of both implant and base-station devices. Discussion of the implant and base-station system control are presented in chapter 4. Computation and system control hardware, while responsible for coordinating virtually all system functionality, presented some degree of flexibility regarding COTS devices. Several micro-controller solutions exist that are capable of meeting design specifications. Due to previous successful experience with the MSP430 microcontroller, this family was explored for the implant. The PSOC 5LP was used for the base-station, which required a high degree of design flexibility.

Because the communication system involves hardware both external and internal to the micro-controllers, as well as firmware, the IR communication system is presented next in chapter 5. This chapter discusses hardware on both the implant and the base-station, as well as discussion on communication protocol. Power management, therefore, comprises the final two chapters before the conclusion. Power requirements of the implant may be simplified into a dichotomy based on energy flow into the system. When wireless power is present, the source of energy is the base-station unit, and is transferred to the implant lithium-ion battery. In the absence of wireless-power, the battery becomes the source of energy for the implant. Both conditions result in overlapping hardware requirements, but the wireless-power capabilities must satisfy the demands of battery charging. Hence, general implant power management is discussed in combination with energy storage needs in chapter 6, followed by the wireless-power system in chapter 7. Implant wireless-power is completely dependent on energy demands of all aforementioned subsystem blocks. Naturally, the design of this system was the most involved, and several supporting topics are included in this section. Although the base-station wireless power TX system was not the primary focus of this work, complete end-to-end wireless power performance is evaluated.

Lastly, this dissertation will conclude with a brief summary of results and suggested future research: chapter 8. The nature of the work in this dissertation is difficult to limit in scope. Indeed, thorough characterization and optimization of every subsystem could carry on indefinitely. Nonetheless, the suggested future work attempts to provide areas of research

that would yield substantial improvement to the proposed system.

For further reference, complete schematics for all devices used in this system are provided in appendix A.

Chapter 2

SYSTEM OVERVIEW AND PHYSICAL DESIGN

2.1 High-Level Overview

A high-level diagram of system operation is shown in fig. 2.1. There are two main devices that make up the system: the base station and implant. In the diagram, the base station is separated into a base-station main (BS-M) unit and a base-station analog front end (BS-AFE). The BS-M connected via USB cable to a PC for system control. The BS-M connects to the BS-AFE by an RF cable and a USB 3.0 cable. These cables allow for the wireless-power loop-coil, with IR circuitry, to be placed at distance from the BS-M circuitry.

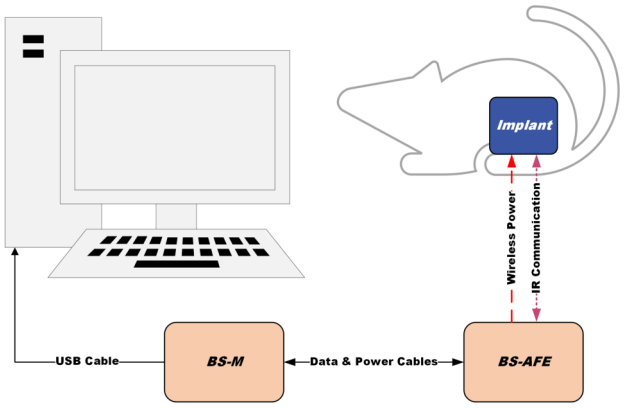


Figure 2.1: High-level diagram illustrating major components of complete system.

The base station delivers wireless power and communicates via an IR link with the implant device. The implant device is intended to be surgically placed into the abdominal region of a rat. A more detailed breakdown of the implant is shown in fig. 2.2. Not including the wireless-power RX coil, the implant device comprises three PCBs. Each PCB subsystem is responsible for critical portions of the entire system design. The implant wireless-power & IR

(IMP-WPIR) PCB, provides front-end IR communication and wireless power management hardware. The implant system control (IMP-SC) PCB is the central computation and control layer, and it hosts the battery and charging circuitry. The final layer is the implant neural IFC & NVM (IMP-NIN) PCB. Note that the voltage rails are labeled XVX and 2VX. This notation emphasizes that these rails are dynamic and are varied depending on the state of operation. Specifics on this operation are covered in chapter 6.

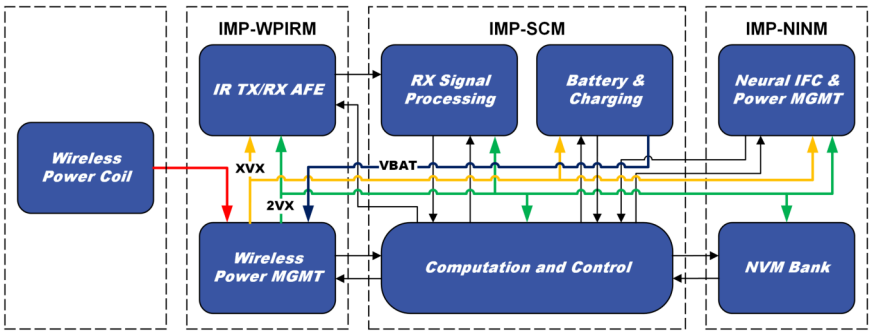


Figure 2.2: Implant subsystem design.

A closer look at the base station is shown in fig. 2.3. The BS-M requires ±15 V external power supplies. While the -15 V supply is only applicable to the BS-M wireless power system, +15 V is also used for powering the BS-SCM and RX signal processing circuitry. The BS-M drives the TX loop-coil at 13.56 MHz. The IR AFE portion uses a USB 3.0 cable for control and signal transmission. It should be noted that the use of a USB 3.0 cable does not imply the remote BS-AFE is USB compliant. Lastly, the BS-M unit connects to a PC by means of a standard USB 2.0 cable. Once connected to the device via a serial terminal, the entire system may be controlled.

As mentioned in the introduction, the physical size of the test animal imposes obvious restrictions on the size of the implant. Consequently, every necessary component comprising the implant device was weighed against its occupation of available volume. Some devices, like the microcontroller, provided satisfactory performance while maintaining a minimal footprint. On the other hand, the energy-storage requirements resulted in very few options

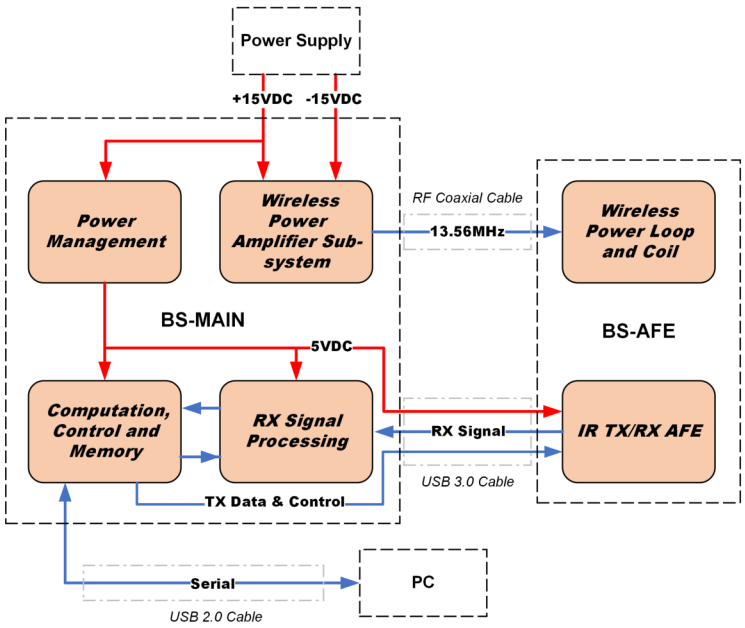


Figure 2.3: Base station subsystem design

that were adequate while placing a major burden on the physical volume budget. In short, some technologies have consistently and rapidly scaled well in terms of functionality and density, like IC technology, while others, like battery technology have improved more slowly.

This application environment necessitates a biocompatible enclosure with low-leak rate to ensure safe and consistent operation of the internal electronics. Ideally the enclosure would be hermetically sealed. Furthermore, the enclosure must be compatible with magnetic fields and optically transparent in near-IR region.

Although the base-station constraints are less imposing, performance, modularity and useability were primary design goals. For the implant to achieve acceptable performance, the base-station components had to meet or exceed the expected functionality of the implant. Because the base-station evolved with implant revisions, hardware flexibility was emphasized. Finally, it was important to produce the base-station unit in an intuitive, user-friendly format. While avoiding an in-depth discussion, which will be reserved for later chapters, this will serve as a foundation to better understand the system-design context.

2.2 Implant Device

The implant device encompasses several fields of study and requires efficient 3-D utilization of available design space. Therefore, the enclosure and PCB design will be briefly discussed before delving into an examination of the general arrangement of the major electronic modules.

Developing an implantable device, especially one that includes embedded processing and analog circuitry, is extremely challenging while debugging and tuning circuitry. The author spent countless hours troubleshooting under a microscope and inadvertently damaging components in the process. As can be seen in some of the following images of the enclosure and PCBs, multiple revisions were required to achieve satisfactory system-level performance. To assist in the process, a so-called "macro-scale" implant was created to verify circuit functionality before it was transferred to the implant design. To distinguish between the two designs, the true-dimension implant shall be referred to as "micro-scale".

2.2.1 LCP Enclosure

As discussed in section 4.3, leak rates of certain materials render them inappropriate for implantation. While devices like pacemakers are hermetically sealed with titanium, a metal case presents serious issues for wireless power and RF communication. During the GSK BIC, the University of Washington (UW) team collaborated with the University College London (UCL) team. The UCL team developed an enclosure made of liquid-crystal polymer (LCP). LCP proved to be a highly-reliable packaging material during the long-term soak tests performed in [52], and is compatible with wireless power and RF communication.

The final iteration of the GSK BIC device is shown in fig. 2.4. In the image, the right-hand half of the implant has a blue supercapacitor "strapped" to the back of the UW PCB and soldered to the front side. The completed UCL PCB with wire-bonded ASICs is shown on the left. After wires or cables for the electrodes are attached to the UCL PCB, the stackup is carefully placed in one half of the LCP package, with the cables passing through

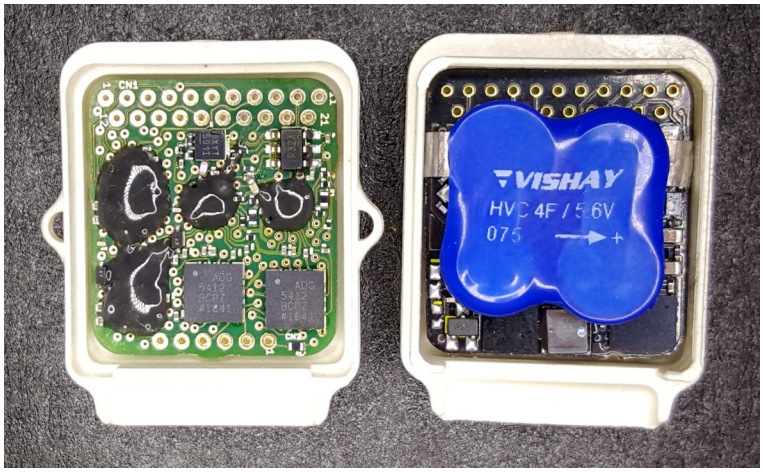


Figure 2.4: LCP enclosure with UCL PCB on the left and the UW PCB on the right. The mating lip area on both halves of the packaging will be sealed with epoxy before implanted.

the extended portion of the LCP package. Medical-grade epoxy mixed with some precision sized glass beads are mixed and carefully applied to one of the enclosure's mating lips. The epoxy mixture also seals the electrode cable penetration. Once the epoxy is applied, the the package is carefully joined together with the other mating half. Following curing of the epoxy, the cables are passed through a strain relief, which is attached to the LCP case with adhesive. The void inside the strain relief is filled with silicone.

2.2.2 Rapid 3-D Printed Enclosure

Due to energy requirements and availability of energy-storage devices (i.e., supercapacitors and batteries), the implantable device dimensions were required to expand lengthwise. To make the implant internals testable, serviceable, and ultimately practical, the thickness of the device was increased to accommodate small connectors interfacing each of the PCBs. Lastly, the choice of IR communication necessitated providing an optical opening in the enclosure, which was accomplished with sapphire-crystal.

In any event, subsequent rapid prototyping of the enclosure leveraged selective-laser sintering (SLS) 3-D printing. The material used for the enclosure (and the BS-M end plates)

are specified in [1]. While this "nylon/polypropylene-like" plastic is inferior to LCP with regards to maintaining a low-humidity environment, it is strong and durable. Additionally prototypes comprised of this plastic are acceptable for medical parts that require USP Class VI compliance or sterilization. That is, this material is certified that there are no deleterious effects due to chemicals leaching out of the plastic enclosure. Ultimately, however, this 3-D printed design should be implemented in LCP for optimal bio-compatibility. The 3-D printed enclosures can be seen below in the implant and base-station sections.

2.2.3 High-Density Interconnect PCBs

High-density interconnect (HDI) PCBs leverage advanced fabrication processes, which allow much smaller features, thereby increasing internal copper and component density. Whereas standard PCB design involves vias that penetrate all-layers, HDI provides blind and buried vias, micro-vias and vias in pad. These features allow for much higher component density. During the development of this system, HDI processes were leveraged from time-to-time. The final GSK BIC UW PCB, shown in fig. 2.5, is an 8-layer PCB with blind vias.

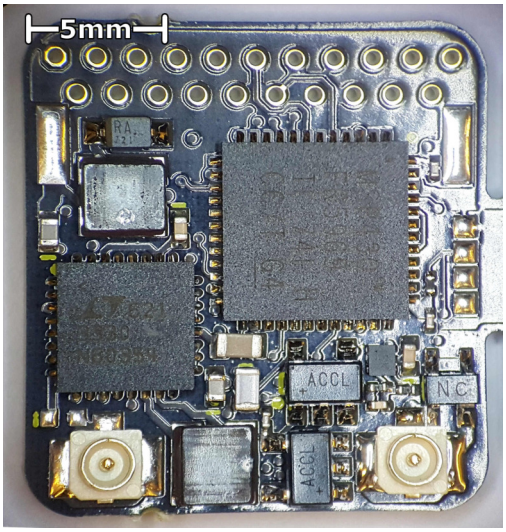


Figure 2.5: Close up of GSK BIC UW PCB.

In traditional PCB design, a via penetrates all layers. Therefore, all unconnected layers must avoid the via. With some HDI processes, an unconnected layer has no such requirement. Additionally, the size of vias and via-in-pad capabilities allow via placement in otherwise restricted areas. A cross-section of the UW PCB is shown in fig. 2.6. The blind via and via-in-pad technology benefits are readily apparent.

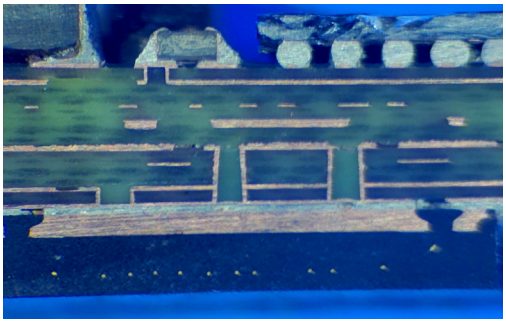


Figure 2.6: GSK BIC UW PCB cross-section showing 8-layers with blind vias.

Ironically, the latest iteration of the micro-scale implant was relatively HDI free. This was partially due to the increased area requirements of the battery. However, as with all technology, standard PCB processes have evolved where the via size and copper trace design rules have improved quite significantly. In other words, yesterday's exotic PCB technology is now commonplace. The latest revision of the micro-scale PCBs are shown in fig. 2.7. The MSP430 microcontroller footprint can be seen at the top of the center, blue PCB panel. This is an 87-pin 0.5 mm pitch BGA footprint, which was accomplished with no via-in-pad nor blind/buried vias. A previous iteration with identical footprint required micro-vias. Regardless, future iterations, especially ones that include more components or reduce the implant physical footprint will most likely require more advanced processes.

2.2.4 PCB Connectorization

In larger designs, standard 2.54 mm pitch headers work well for prototyping. Indeed, these headers were selected for the macro-scale implant. However, the implant PCB stack proved

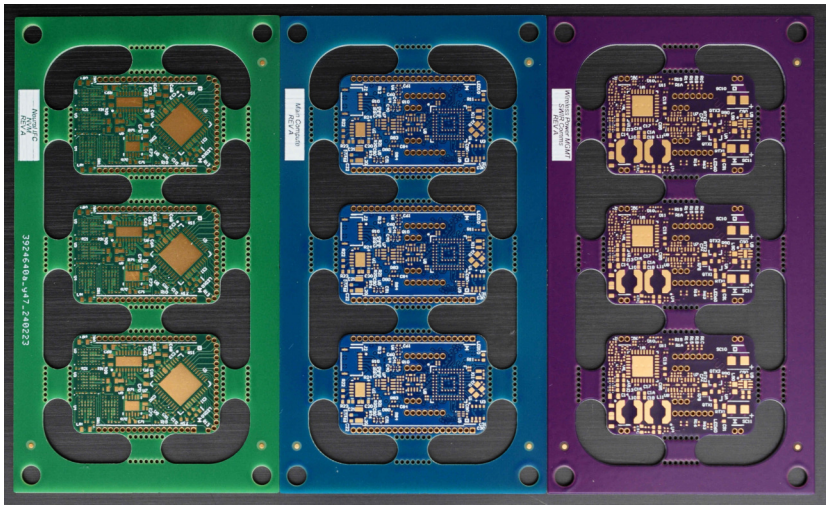


Figure 2.7: Latest micro-scale PCB revision.

quite problematic. While there are many available connectors, all of them either occupied too much area or required the PCBs to be excessively spaced. Ideally, a keyed and locking connector system designed for high-speed data and power with SMD mounting would be implemented to satisfy the space constraints. However, the only commercially available candidates were a series of through-hole 1 mm pitch headers: Sullins SMH and SFM mating connectors. The connectors are shown below. It should be noted that while the connectors perform well, they are extremely difficult to work with. The pins are fragile and the female receptacles easily flood with excessive solder. Additionally, in the absence of a large custom order from the manufacturer, the headers must be cut down to fit, exacerbating the situation.

2.2.5 Micro-Scale Implant

A stack up of a previous revision of the implant PCBs, the micro-scale version, is shown in fig. 2.8. The top PCB is the wireless-power RX coil with a thin ferrite layer placed immediately below it, which is stacked directly on top of the IMP-WPIR PCB. Note that the IR LED and photodiode protrude through a cutout in the wireless-power coil and are roughly aligned in a co-axial manner. The middle, thin PCB is the IMP-SC module. The

red PCB, lowest in the stack, is the IMP-NIN PCB. Between the IMP-NIN PCB and the IMP-SC PCB resides the lithium-ion battery. A thin edge of the battery packaging is visible immediately to the left of the micro-headers connecting the two PCBs.

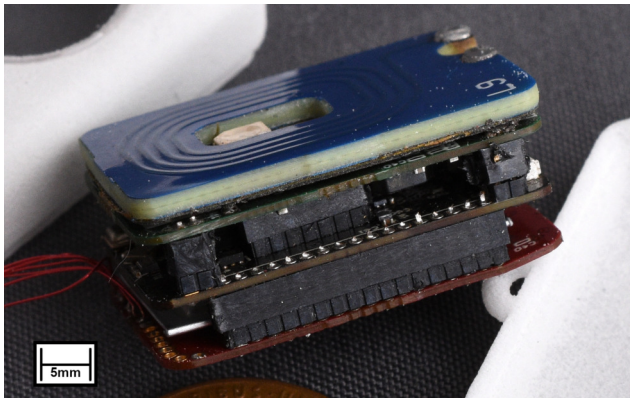
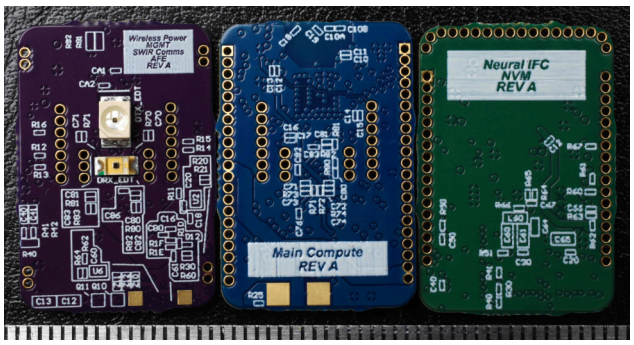


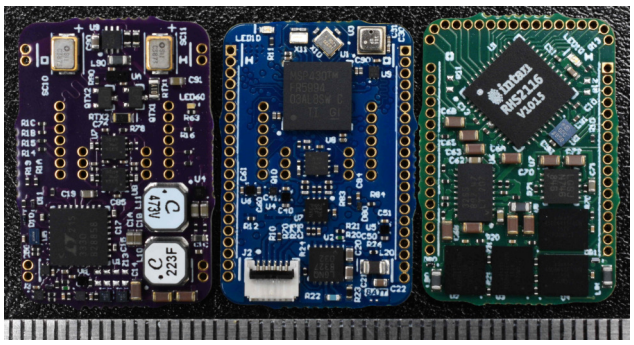
Figure 2.8: Micro-scale implant PCB stack.

Each of the PCBs residing below the wireless power coil, are shown in more detail in fig. 2.9. Note that the reference ruler shown below the PCB is in mm. The "low-density" and "high-density" sides refer only to the the number of components on that particular side. Note that the micro-headers, lithium-ion battery and tuning capacitors have not been installed in the figure. In (a), the purple IMP-WPIR PCB shows the larger IR LED (white package) above the IR photodiode. The blue IMP-SC module shows pads where the lithium-ion battery is soldered into place. The small white connector with black latch is for programming and debugging. It connects to a six-position, 0.5 mm pitch ribbon cable (FFC/FPC), which is attached to implant-developer IFC (IMP-DIFC). No components are on the "low-density" side of the IMP-NIN PCB. The "high-density" side in (b) hosts all other electronic components. The specifics of each system will be discussed throughout this dissertation. However, the schematics for these PCBs may be found in appendix A.

The previously discussed enclosure, 3-D printed with SLS technology, is shown in fig. 2.10 with the micro-scale implant PCB stack inside. Immediately apparent is the the circular cutout on the top half of the enclosure. This allows for a quasi-hermetically sealed biologically



(a) Low-density side



(b) High-density side

Figure 2.9: Micro-scale PCBs: Purple, blue and green PCBs are IMP-WPIR, IMP-SC, IMP-NIN modules, respectively.

compatible optical window for IR communication. The material is sapphire quartz. The sapphire window pictured is 0.8 mm thick and 14.5 mm in diameter and is intended to be epoxied into place. Like the LCP case discussed above, this enclosure allows electrodes to escape via a small cutout between the two halves. The final design would incorporate purpose-built electrodes. To ensure moisture does not enter the enclosure, the electrodes would also pass through another small flexible housing that is sealed to the bill-like structure of the enclosure. The final size of the enclosure is 21.0 mm x 32.0 mm x 15.0 mm. These dimensions do not include the loops, which are intended to surgically secure the implant to the RUT. The internal cavity that holds the micro-scale PCB stack-up is 18.0 mm x 26.0 mm x 12.5 mm.

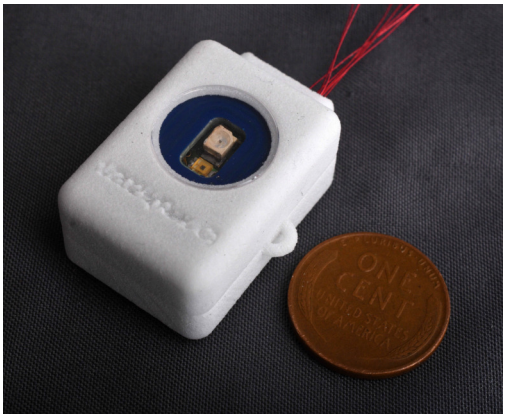
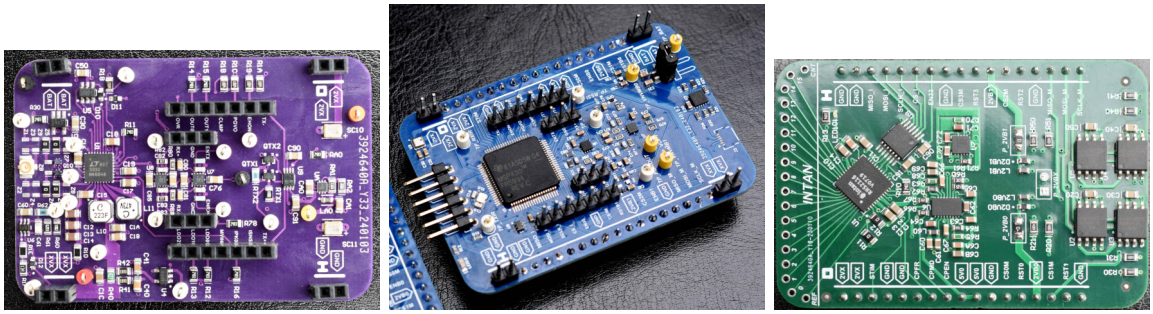


Figure 2.10: Implant device in enclosure.

2.2.6 Macro-Scale Implant

As stated above, the macro-scale PCB is a schematically-equivalent, scaled version of the micro-scale implant. The up-scaling factor, while arguably arbitrary, was designed around the standard 2.54 mm header. The macro-scale PCB dimension ratio is therefore 2.54:1. While every component is not exactly in the same position, each component was placed in the same general region. Whenever possible, the components were chosen in a larger form



(a) IMP-WPIR (b) IMP-SC (c) IMP-NIN

Figure 2.11: Macro-scale PCB modules.

factor to facilitate rapid prototyping and debugging. Some components were not changed if there was any question regarding change in performance. Each of the three PCB modules is shown in fig. 2.11.

A macro-scale prototype is shown next to a micro-scale prototype in fig. 2.12 (a). Note that the micro-scale wireless-power coil was used for the macro-scale device to ensure wireless-power transfer numbers were accurate. Wireless-power performance, discussed in chapter 7, was conducted using the macro-scale version. One difference is that additional ferrite was required on the macro-scale version because the PCB, with internal ground planes, extends beyond the edges of the implant coil. Likewise, the macro-scale enclosures were also 3-D printed. The enclosure dimensions are roughly proportional. The macro and micro-scaled enclosures are shown in fig. 2.12 (b). These enclosures have been dyed black. The sapphire optical window is the same thickness as the one used in the micro-scale version, but the diameter of this window is 32.0 mm. The final dimensions of the macro-scale enclosure are 49.0 mm x 79.0 mm x 36.0 mm. The internal cavity is 44.0 mm x 64.0 mm x 31.5 mm.

2.3 Base Station

The base station comprises a main unit (BS-M) and auxiliary devices. The entire setup with all connections is shown in fig. 2.13. The green box at the top is a simple unit that serially

(a) PCB stack comparison. (b) Enclosure comparison.

Figure 2.12: Micro-scale versus macro-scale devices.

connects voltages from two isolated AC-DC converters, which both supply a regulated 15 V, thereby providing the necessary $\pm 15V$. For monitoring of power performance, two voltage and current meters were installed in the box. The power outputs then connect to the grey box with white end caps. This box is a repurposed power-inverter enclosure made of aluminum. The end caps were 3-D printed to allow custom connections to the BS-M PCB. The black "wand-like" device is the remote wireless-power TX loop and coil with co-axially mounted IR communication hardware (BS-AFE).

2.3.1 Base-Station Main

Shown in fig. 2.14 is the BS-M PCB. The original inverter fan was also used in this design to cool the base-station linear wireless-power module(s) (BS-LWPM), which are identifiable by the yellow PCBs. The current revision only uses one wireless power module. The blue PCB in the lower-right corner is the BS-SCM. This module contains the microcontroller. It interfaces, via a DB-9 connector, to an external module for programming and serial IFC capabilities: the base station developer IFC (BS-DIFC) module. On the upper-left side of the PCB are the SMA connector and power-supply inputs. The IR communication USB 3.0 cable connects in the lower-left corner.

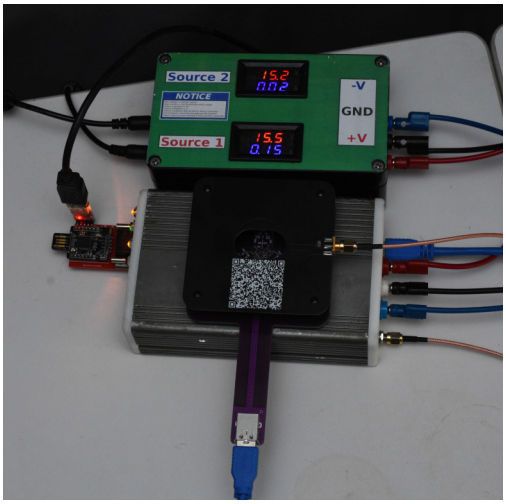


Figure 2.13: Fully-connected base station.

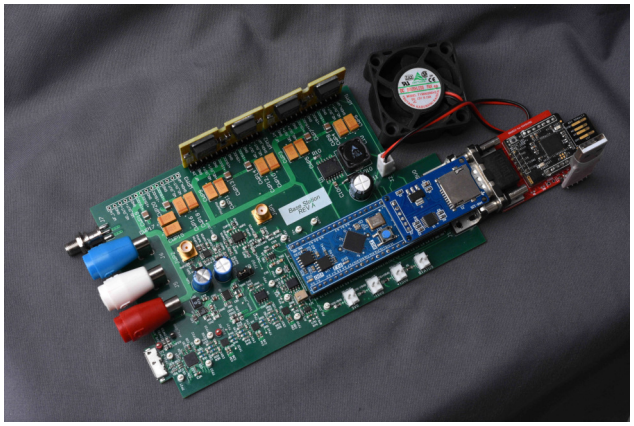
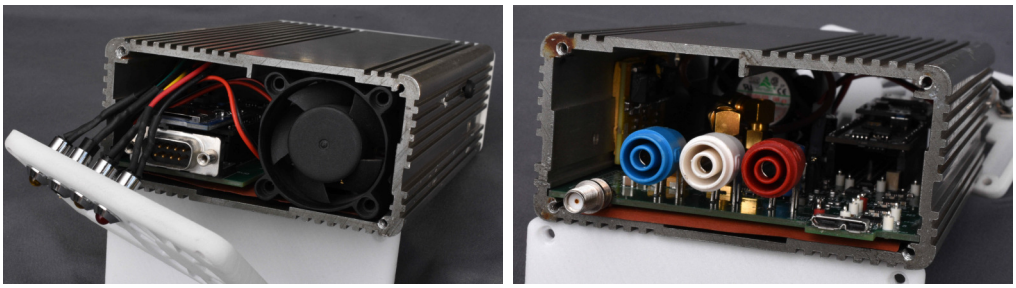


Figure 2.14: BS-M PCB with wireless power modules and fan.



(a) BS-DIFC and BS-LWPM cooling fan. (b) Power supply and BS-AFE connectors.

Figure 2.15: Internal view of BS-M PCB installed in enclosure.

A closer look at the full BS-M unit is shown in fig. 2.15. In (a), the 3-D printed end plate, which houses four indication LEDs, is shown unmounted from the enclosure. The LEDs (arranged from left-to-right) correspond to -15 V, +5 V, +15 V and status, respectively. The red status LED may be configured as the end-user sees fit. Presently, it is illuminated when wireless-power is active. The location of the cooling fan is evident as is the DB-9 connector used for connection to the BS-DIFC. Immediately above the DB-9 connector is a micro-SD card slot for convenient access to recorded neural data. In (b), the RF output, DC input, and USB 3.0 connectors are visible. To the upper left of the blue power input, the yellow BS-LWPM can be seen thermally connected to the aluminum enclosure.

Chapter 3

IMPLANT NEURAL INTERFACE MODULE

3.1 Neural Interface

3.1.1 Background Work

Previous iterations of the neural interface used a combination of different topologies as the GSK BIC progressed. For the first phase, optogenetic stimulation was the selected biological interface. During the second phase, the stimulation method was changed to electrical stimulation. Given the relevant expertise of each lab during the UW and UCL collaboration effort, the system was split into two separate PCBs: UW developed the wireless-power, NVM, and system control circuitry; and UCL designed the neural IFC circuitry.

Optogenetic Stimulation

The optogenetic biological interface comprised two high-powered LEDs from the Cree X-QE series: stimulation at 615 nm and blocking at 465 nm. This line of LEDs was designed to operate at hundreds of mA, with peak drive currents at 1 A. The blue LED had a forward voltage drop of 3.1 V at 350 mA, while the red LED was 2.2 V at 350 mA. The length of time to drive the red LED for stimulation was approximately ten seconds, based on the physiological voiding time for a rat, while the blue LED periodically illuminated for about one second every few seconds to provide blocking.

Even at the most generous WPT rates, the red LED could not be operated continuously for ten seconds. Therefore a 470 mF supercapacitor from the Murata DMF series, designed for high-power discharge, was used to store energy until an optical stimulation pattern was required. Despite the excellent performance of the 470 mF supercapacitor, 470 mF would

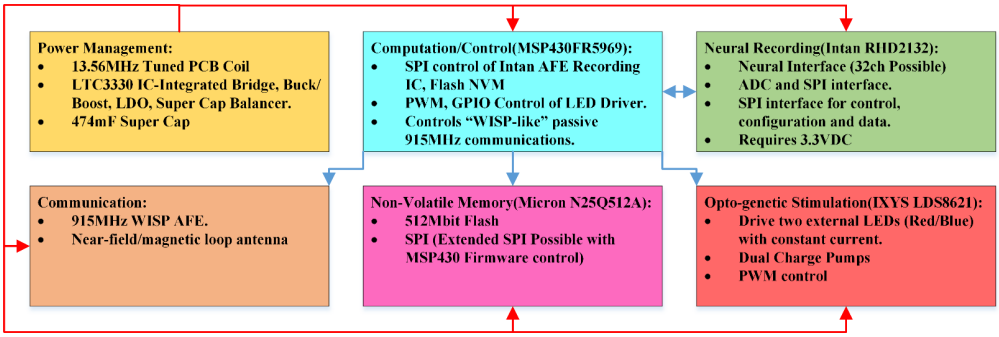


Figure 3.1: Optogenetic-stimulation device block diagram.

limit the stimulation time if driven at 350 mA. While not completely verified, the brightness of the LEDs was thought to be sufficiently bright being driven at approximately 100 mA. The LED driver utilized an IC designed for cell phone camera flash/flashlight LEDs: IXYS LDS8621.

For neural-data acquisition, the Intan RHD2132 was selected. The RHD2132 provides up to 32 channels, and has a fully-integrated 16-bit ADC with an SPI interface. A 512 Mb flash IC provided storage for recorded neural data. System control was accomplished by an MSP430FR5969 microcontroller. A high-level block diagram, fig. 3.1, illustrates the major subsystems required to power the LEDs and the Intan RHD2132.

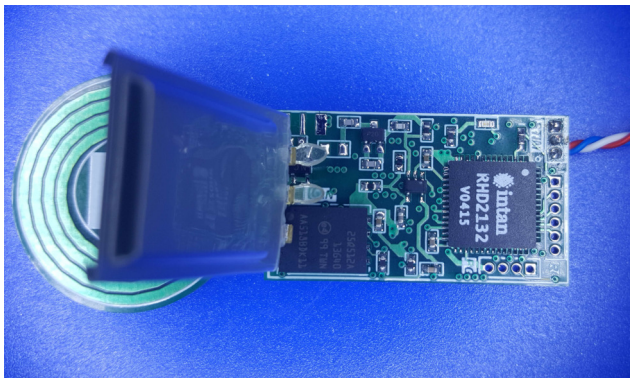


Figure 3.2: The "lollipop" optogenetic stimulation device.

The last revision of the optogenetic stimulation prototype is shown in fig. 3.2. It was referred to as "lollipop" by team members due to the placement of the wireless-power coil, which was integrated into the system PCB. While the optical stimulation portions of this implant device are no longer applicable, all subsequent revisions, including the latest version presented in this dissertation share various aspects.

Electrical Stimulation

For the second stage of the GSK BIC, the UCL neural-IFC PCB included an ultra-low noise amplifier [15] and stimulator [37] ASICs. A simplified block diagram of the UCL PCB module is shown in fig. 3.3. At the biological interface, the UCL PCB has six ports for electrical stimulation and recording. To reduce the electrode count, the amplifier analog inputs and stimulator outputs share the same ports by using analog switches controlled by the UW PCB. There are two channels for stimulation and recording. The remaining two ports are provided for amplifier reference and stimulator common return.

The two stimulator ICs are controlled via SPI. The SPI bus is connected to the "master" ASIC, which controls the "slave" ASIC. The stimulator ASIC is then configured for the appropriate stimulation pattern via SPI and clocked at 1 MHz. The stimulator ASICs require 5 V for all digital input signals, and approximately 14 V to drive the current sources.

The two primary amplifier ICs were ultra-low noise and provided variable gain control with digital inputs. Each amplifier provided two gain setting bits to adjust the amplifier gain to one of the following four voltage gain levels: 1040, 279, 57 and 11.6. The amplifiers were powered at 3.3 V. The input referred noise was measured at 704 $\frac{nV}{\sqrt{Hz}}$ given a bandwidth of approximately 142 Hz to 6.61 kHz. Two additional low noise amplifiers were included to provide an optional gain of ten. All four signals were sampled by the MSP430 ADC. A photo of the completed UCL PCB is shown in fig. 3.4.

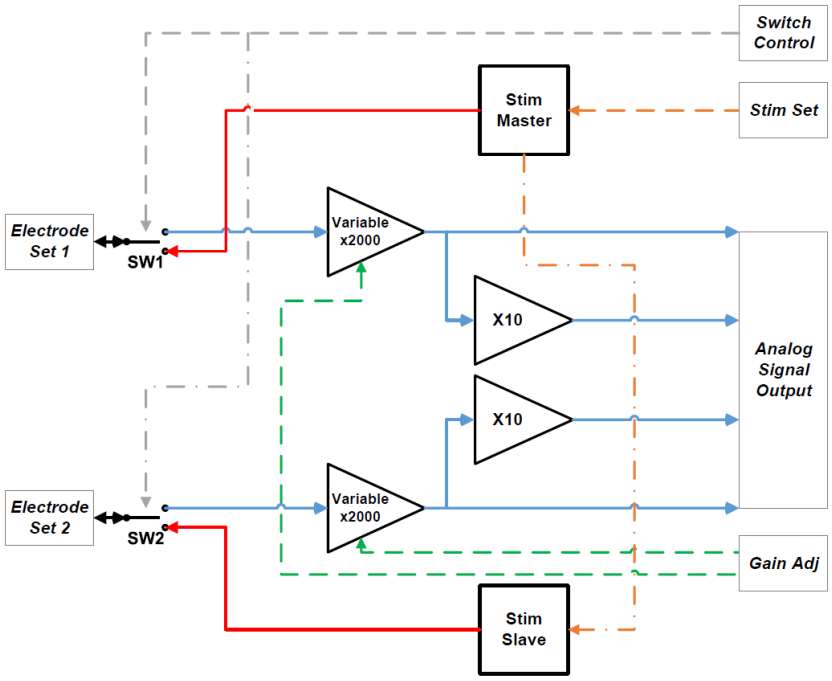


Figure 3.3: A simplified block diagram of the UCL PCB module.

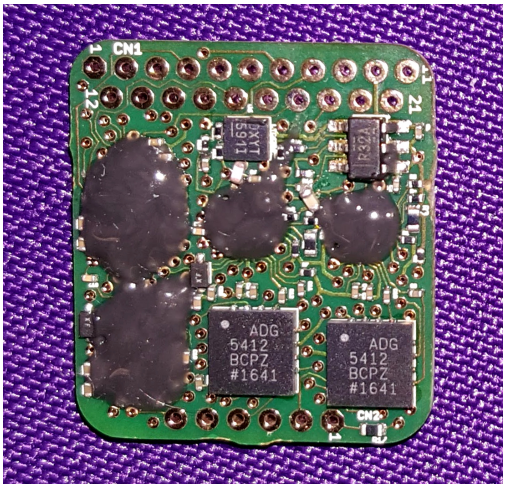


Figure 3.4: The latest revision of UCL PCB includes wire-bonded amplifier and stimulator ASICs with glob-top encapsulation.

3.1.2 Intan RHS2116

Towards the end of GSK BIC, COTS neural-IFC solutions were investigated. Coincidentally, Intan Technologies had recently released the the RHS2116 [34]. Although the market for neural recording and stimulator ASICs is limited, Intan Technologies RHS2116 is state-of-the-art. The RHS2116 has 16 independent multiplexed recording and stimulation channels. The amplifiers have an input referred noise of 2.4 μV_{rms} and the 16-bit ADC can sample each channel up to 40 kHz. The RHS2116 also provides built in filters and electrode impedance measurement. Individual amplifiers and stimulators may be selectively powered to conserve energy. The device is controllable via SPI, further simplifying system integration. The packaged die is provided in a 7 mm x 7 mm leadless package, as shown in fig. 3.5. The RHS2116 level of integration, performance and reliability would be extremely difficult, if not impossible, to outperform with discrete circuitry.

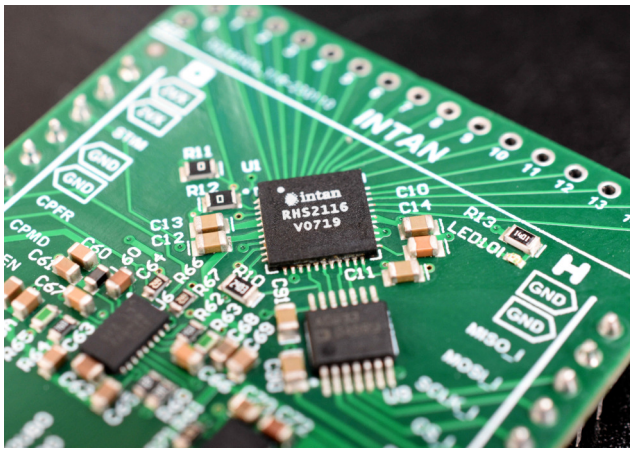


Figure 3.5: Intan RHS2116 ASIC on macro-scale implant PCB.

Although the details of operating the RHS2116 are beyond the scope of this dissertation, control of the device, at least at a high-level is quite simple. The RHS2116 does not contain an integrated processor or clock. Therefore, all timing is derived via the SPI interface: Stimulation and sampling rates are equivalent to the rate of transferred 32-bit SPI commands.

Initialization, configuration, ADC conversion, stimulation, etc. are all accomplished with four commands. To sample neural data, a "CONVERT" command is issued repeatedly. Stimulation is accomplished by cycling through a series of register "WRITE" commands.

3.1.3 Neural Interface Power Management

While the operation of the RHS2116 is relatively straightforward from an SPI perspective, supplying power to the IC presents some challenges in a space-limited environment. The RHS2116 must have 3.3 V supplied for all digital control and analog recording circuitry. The LTC3042 linear regulator was selected, to minimize noise at the 3.3 V supply pin. This regulator boasts "ultralow noise" at 0.8 μV_{rms}, and an "ultra high PSRR" of 79 dB at 1 MHz.

However, the IC must also have a constant positive and negative voltage rail supplied to the IC stimulator voltage inputs. The maximum stimulator supply voltage amplitude is 7 V. Although generating a clean split supply is commonly performed, finding an IC with low-noise, good efficiency, acceptable voltage levels and small form factor is extremely difficult. The LTC3265 is the closest match identified, albeit somewhat over-powered for good efficiency.

The LTC3265 integrates boost and inverting charge pumps, followed by positive and negative low-dropout (LDO) regulators. The minimum supply input is 5 V, and the device may be switched between constant frequency or burst mode. The device is rated at 200 mA. In burst mode, efficiency is satisfactory for the the implant. However, the major concern was charge-pump noise being injected into the neural data. Because the RHS2116 always requires voltage applied to the stimulation power pins, the charge pumps cannot be turned off during recording. The blue trace in fig. 3.6 shows significant spikes in the XVX supply current. This waveform was captured upstream from the charge pump with a current sense amplifier. However, no noise at the stimulator power pins is detectable. The pink trace shows the voltage at the positive stimulation power pin. The negative supply shows similar behavior.

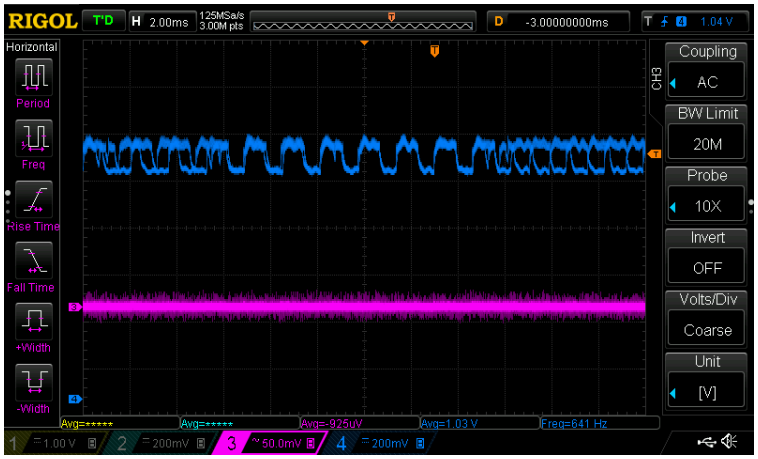


Figure 3.6: XVX supply current pulses, caused by the charge pump, present no detectable noise at the RHS2116.

3.2 Non-Volatile Memory

While non-volatile memory (NVM) is not part of the neural interface, its presence in this design is driven purely by the need to record massive amounts of neural data and store it for later access. Consequently, it becomes one of the primary factors in the design of this device. Indeed, recording times of up to six minutes of raw neural data require intensive engineering trade-off analysis. Per the GSK BIC specifications, two channels with 12 to 16-bits of resolution, sampled at 12 kHz, was the minimum acceptable performance. Furthermore, six minutes of neural data was required. The memory requirements may be calculated using eq. (3.1).

$$NVMSize[bits] = n_{ch} \times f_s \left[\frac{Samp}{s}\right] \times n_{bits} \left[\frac{bits}{Samp}\right] \times t_{rec}\,[s] \times \frac{1}{CR_{data}} \tag{3.1}$$

As specified by the design constraints, any compression algorithm must be lossless. Lossless compression techniques, compatible with the MSP4305994, are currently being explored. Indeed, an increase in compression ratio (CR) would reduce the amount of required NVM. For the work in this dissertation, a CR of 1.0 is assumed. Using anticipated neural

recording metrics, two channels sampled at $30\frac{kS}{s}$, with an ADC resolution of 16 bits, for a duration of 360 s, would require 345.6 Mbit of memory. At 12 bits, 259.2 Mbits would be required.

A quick review of commercially available NVM ICs, with reasonable form factor and power consumption, instantly places restrictions on the technology available to provide the required memory capacity. The great majority of NVM ICs use either flash or EEPROM technologies, both being well-established and proven. Other more exotic NVM technologies, like MRAM and RRAM were explored thoroughly. The NVM IC selected was based not only on memory density and power consumption, but also on control architecture appropriate for a microcontroller like an MSP430FR5969.

3.2.1 Memory Density and Power Consumption

Various technologies were quickly eliminated since their areal density was too low or power consumption too high. EEPROM, for instance, lacked the density to be a viable solution. Magnetoresistive RAM (MRAM) required excessive power during programming operations. Ferroelectric RAM (FRAM) has exceptional durability, speed, and endurance. Additionally, power consumption of FRAM devices is typically very low. Presently there are two vendors of discrete FRAM NVM ICs: Infineon and Fujitsu. The largest capacity FRAM IC on the market is 16 Mbit and is manufactured by Infineon. It is produced in a 6 mm x 8 mm package. Infineon also manufactures the FRAM IC with the largest areal density of bits: It has 8 Mbit of capacity and measures 3.23 mmx 3.28 mm. In either case, the areal density of these FRAM ICs are too low.

A comparison of potential implant NVM ICs, which shows device areal density and power-consumption performance, is shown in fig. 3.7. Please note that manufacturer names have changed since this data was compiled. Cypress is now Infineon, and Adesto is now Renesas. FRAM far outperforms any flash device in terms of power. However, when considering required areal density, FRAM is not a practical solution. On the other hand, flash provides excellent memory density, but power consumption can be excessive.

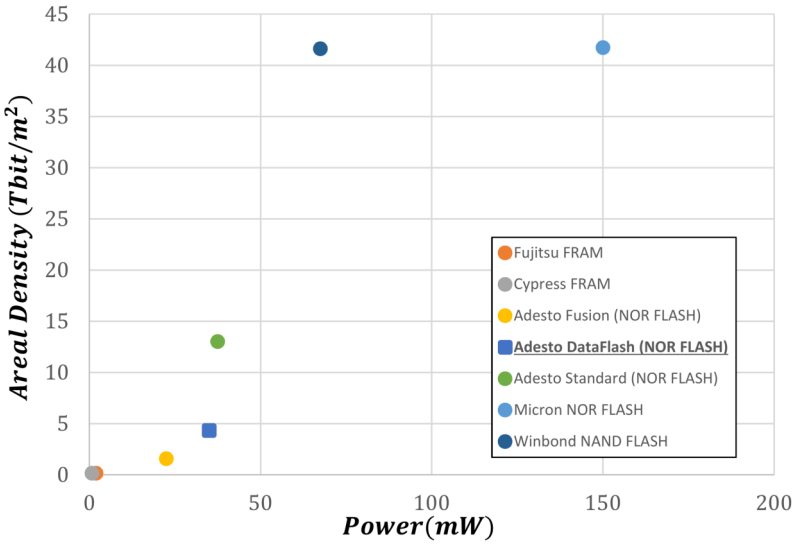


Figure 3.7: Comparison of memory density and power consumption of commercial NVM ICs.

Ultimately, the only NVM technology that would suffice was flash. There are two common types of flash NVM on the market today: NOR and NAND. The low-power programming and areal density of NAND flash are attractive features [27, 62, 73]. While NOR flash read times may be an order of magnitude less than that of NAND flash, both read times are acceptable for this application.

At the time of this work, the choice between NOR and NAND flash technologies was determined not by the performance metrics discussed above, but by compatibility with a low-power microcontroller (i.e., an MSP430FR5994). The great majority of these flash devices are designed for high-performance microcontrollers. For example, single 512 Byte (and larger) SRAM buffers are common on these devices. To be efficient, these SRAM buffers should be filled to capacity, since the hardware will program all contents of the buffer to flash memory, regardless if it is used. Furthermore, the SRAM is unavailable during this procedure. Considering the long program times of NOR flash, the MSP430FR5994 would, therefore, be responsible for buffering any additional incoming neural data.

Adesto Technologies, founded in 2006 with a focus on developing conductive bridging RAM (CBRAM), manufactured NOR flash well-suited for this application. Adesto NOR flash technology is now part of Renesas. Indeed NOR flash typically under performs NAND flash in several critical areas; however, the DataFlash series provides remarkably low power consumption for NOR flash devices, and "ultra-deep power-down" modes drawing only 400 nA [2]. Additionally, the DataFlash NOR flash control circuitry provides an efficient interface for the low-power microcontrollers: user selectable 256 or 264 Byte page address, multiple low power SPI modes and two independent SRAM buffers. The 64 Mbit version in a 3.5 mm x 4.2 mm WLCSP package (AT45DB641E) was selected for this design. An array of four NVM ICs provided a total capacity of 256-264 Mbit, which will meet the specifications given a CR of 1.0 and 12 bits of resolution eq. (3.2). For the full 16 bits of resolution on the Intan RHS2116, neural record time would fall to 275 s.

$$CR_{data} = \frac{2 \times 30\frac{kSamp}{s} \times 12bit \times 360s}{264Mbit} = 0.98 \tag{3.2}$$

The physical layout of the four 64 Mbit NOR flash ICs are shown in fig. 3.8. Aside from maintaining high-speed SPI communication, the location of the NVM ICs is not critical. However, as shown, even in their no-longer-available WLCSP packaging, the bank does occupy a significant amount area on the micro-scale PCB.

3.3 Neural Recording Power Consumption

NOR flash memory can be power intensive. While the variant used in this work is relatively efficient, the power consumption of the DataFlash devices can be significant during certain operations. An erase operation, which is required to reset bits before programming, is especially power intensive. Bench-top tests revealed an erase operation required an additional 13.13 mA of current when operating at 2.5 V. The erase operation is expected to be conducted while wireless power is present to minimize wasted battery energy when the system is awaiting a neural-recording session.

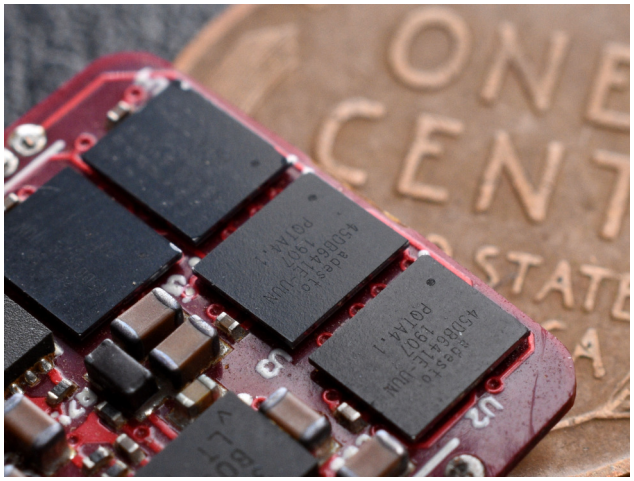


Figure 3.8: Quad 64Mbit SPI Flash array.

A more practical characterization of the power requirements occur during a recording session. While stimulation currents can reach into the mA range momentarily, the sustained neural signal sampling and NVM programming, over a period of several minutes, drive the power consumption. When the NVM ICs are initialized along with the RHS2116, 9.93 mA is required from the XVX rail set at 5 V and 1.40 mA from the 2VX rail set at 2.5 V. Note that these numbers include power consumption of the microcontroller and other idle devices. Furthermore, as will be discussed in chapter 6, the 2VX rail is supplied by the XVX rail through a linear regulator. Therefore, total power consumption is ideally 56.65 mW. During a neural recording session, where one channel is sampled repeatedly at 26 $\frac{ks}{s}$ with NVM programming, the XVX rail current increases to 10.36 mA and the 2VX rail to 6.36 mA, boosting the power dissipation to 83.60 mW.

Chapter 4

COMPUTATION AND CONTROL

4.1 High-Level System Overview

The MSP430FR5994 microcontroller is the heart of the implant computation and control subsystem fig. 4.1. This microcontroller, which is part of the ultra-low power FRAM family, is arguably the most robust. The MSP430FR5994 provides 256 kB of FRAM and 9 kB of SRAM. Eight eUSCI devices offer ample serial channels for external device communication. More than enough ADC and comparator channels are available, as well as numerous timers. Given the complex interconnections of the implant device, almost all 68 GPIOs are used. The MSP430FR5994 is available in a 6 mm x 6 mm BGA package, further making it an ideal candidate for an implant. The macro-scale version uses the 12 mm x 12 mm QFP package.

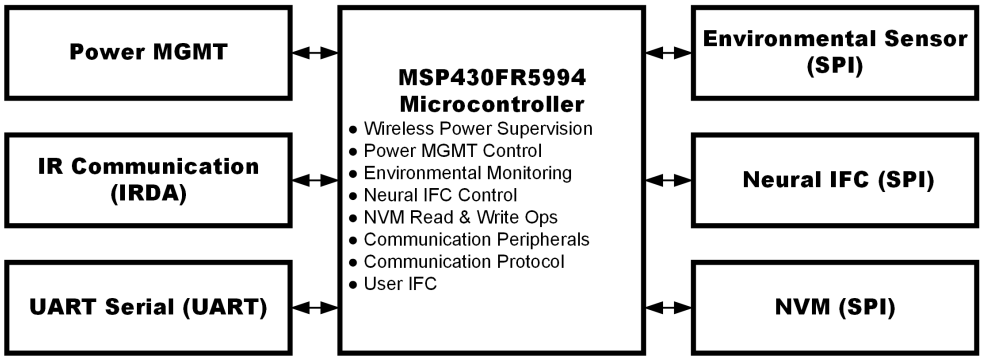


Figure 4.1: The MSP430FR5994 microcontroller provides all system control for the implant.

In a similar manner, the base station is controlled by a PSOC 5LP fig. 4.2. The PSOC 5LP is a sophisticated microcontroller and complex programmable logic device (CPLD) hybrid. Processing is accomplished by an Arm Cortex M3 core capable of running at 80 MHz.

The CY8C5888 version provides 64 kB of RAM, 24 universal-digital blocks (UDB) and an assortment of analog peripherals. The UDBs are highly configurable and are used for onboard digital logic for communication and external component control. Integrated analog devices were also used for communication and wireless power. PSOC schematics may be found in Appendix A.

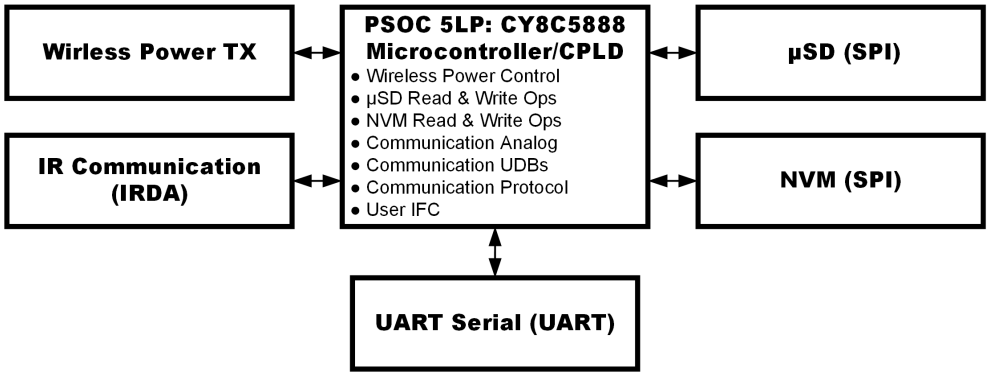


Figure 4.2: The base station leverages a PSOC 5LP for system management.

4.2 Operating System

The complexity of the implant combined with the necessity of scheduling events at particular times require something more involved than a bare-metal approach. The MSP430 must actively monitor wireless-power, battery and communication circuitry while maintaining a calendar for future events. Likewise, the PSOC 5LP must also supervise many operations and external hardware events. However, a true real-time OS (RTOS), while generally a benefit, was not necessarily a requirement for this application. Indeed, any critical events, like an impending system shutdown due to a low battery, needs to be addressed quickly, but for other use cases an OS that provided near real-time functionality would suffice. Additionally, because the device was designed as a research platform, the ability to create custom applications was highly desirable.

Presently there are a few available OSs that are appropriate for this application. The

8 kB RAM of the MSP430FR5994 places a hard limit on some of the more robust OSs, like embedded Linux. In [63], various open-source OSs for IoT were compared. TinyOS, Contiki, RIOT, and FreeRTOS were among the most attractive candidates. Each of them could be configured to a minimal 1.5 kB or less RAM footprint. RIOT and FreeRTOS were the only two viable alternatives that provided full C support with readily available documentation. Both OSs featured an API that was more than capable of supporting this project. After further research, RIOT was pursued given its lower energy demands [11]. Although RIOT has some support for the MSP430, the MSP430 FRAM family is not officially supported. After reaching out to the RIOT community, a member provided partial support for MSP430FR5969, which was the original microcontroller of choice. Still, there was a considerable learning curve to get the OS to function on the MSP430FR5969, and considerable effort was expended developing drivers to support the required peripherals. In short RIOT is a very capable OS in a minimal footprint; however, it is perhaps too capable for this application. After creating some anticipated applications and considering the necessary development time, RIOT was abandoned for a custom kernel.

4.2.1 PSEUDOS

While RIOT is real time and provides multi-tasking, it was ultimately determined that neither of these aspects were required. What was needed was a lightweight OS with near real-time performance that provided an API for scheduling, direct-peripheral control, and application and task creation, all while featuring a simple command-line interface (CLI). The OS would be single-threaded with non-preemptive scheduling: First-come, first-serve (FCFS). The end user would be responsible for memory management and ensuring custom applications do not interfere with other processes.

What started as a convenient method for control and debugging over serial, eventually evolved into a rough OS, thereby resulting in the name PseudOS. While technically an OS, the name PseudOS was originally coined from a tongue-in-cheek slogan: "The sort-of operating system." PseudOS accomplishes all the aforementioned goals with a minimal

resource footprint. Extensive computation analysis has not been conducted on PseudOS, and definition of a "minimal" implementation is highly subjective. While a CLI with "printf" functionality is typically quite resource heavy and purely optional in PseudOS, an example of memory usage without these features initialized is somewhat misleading in this application. Furthermore, memory usage is also highly dependent on how many applications, peripherals, etc. are required in a particular application. However, a simple implementation of PseudOS, with CLI support and a few simple customized programs can be achieved with less than 1 kB of RAM on the MSP430FR5994. This is discussed in more detail below.

Portions of PseudOS were inspired by RIOT. The design of RIOT and configuration revolves around the CPU, microcontroller boards and peripherals [4]. While the CPU and peripherals of a microcontroller are self explanatory, the "boards" aspect refers to commercially available demo or proto boards, like the MSP430 Launchpad and Arduino boards. This portion of RIOT is hardware dependent, while the kernel and drivers are hardware independent. In a similar manner, PseudOS was designed to run on any common microcontroller. Some functionality of PseudOS is peripheral dependent; however, most microcontrollers share a common set of peripherals. A major difference in the design of PseudOS is less emphasis on "board" abstraction. Physical hardware abstraction ends at the microcontroller GPIO. Interfacing with external devices is implemented through common peripheral API. Once initialized and registered in PseudOS, hardware may be controlled via common PseudOS calls. In this regard, there is some level of abstraction. The actual kernel of PseudOS is extremely simple. The user-configured system-timer interrupt-service routine (ISR) calls the PseudOS system timer and sets a flag. Once the flag is set, the main loop services all tasks and one application in the queue. This behavior is illustrated in fig. 4.3 User interaction is provided via a CLI, which is UART interrupt driven and not part of the loop. When a command is provided via the CLI, a shell command will be executed or an application call will be placed on top of the application stack.

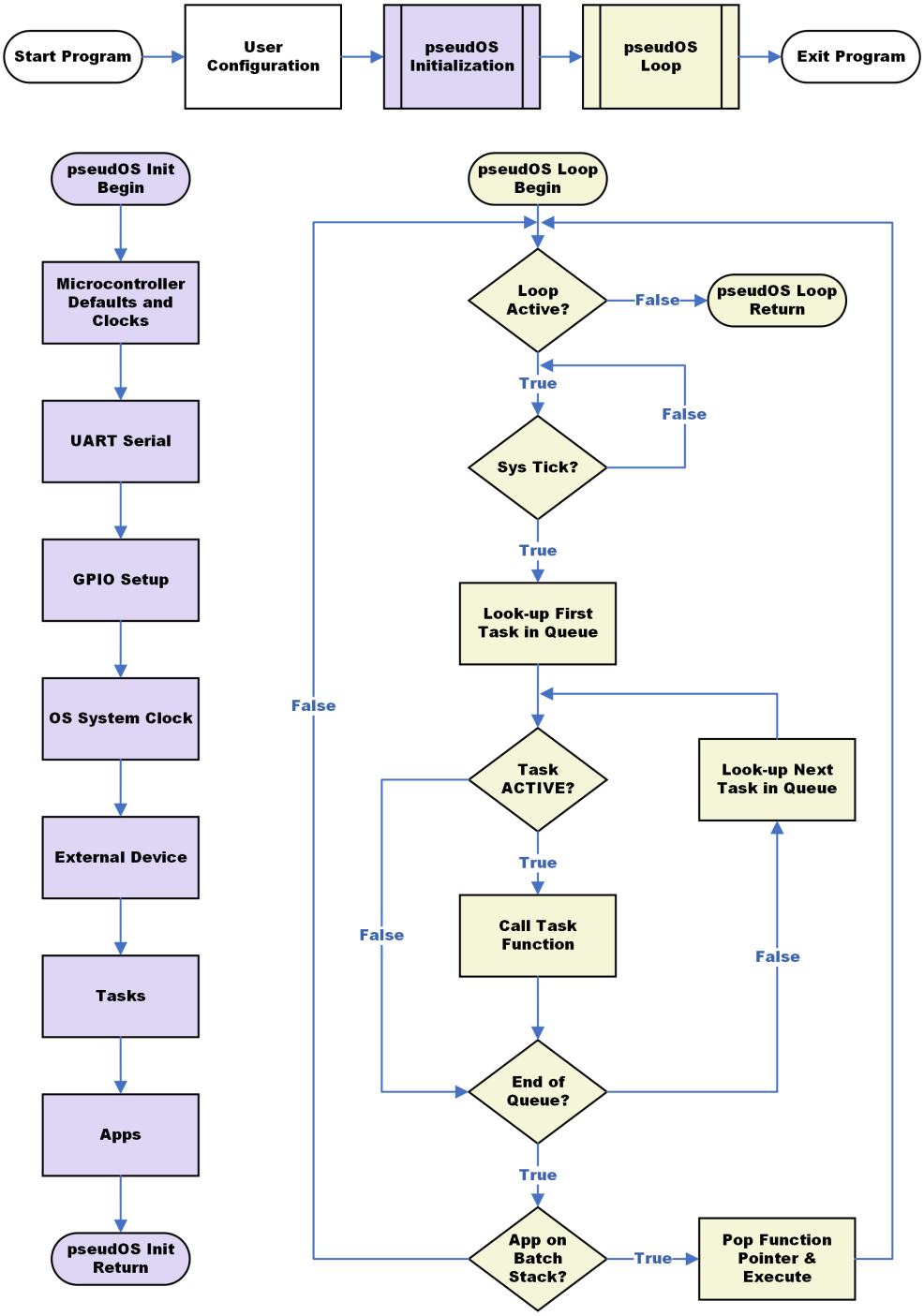


Figure 4.3: Flowchart showing general execution flow of PseudOS.

Tasks and Applications

PseudOS provides two basic methods for custom programming: tasks and applications. The former is intended for fast, lightweight blocks of code that are executed frequently. An example is shown in Program-code 4.1. Initialization of the task requires only a few lines of code and may be initialized in one of three states: active, sleep or dead. "Active" tasks will be immediately executed in the task queue without user intervention. Tasks in "sleep" state, are registered with PseudOS and queued, but skipped over for execution. "Dead" tasks are registered with PseudOS but are not placed in the task queue. Note that it is up to the user to implement some type of delay because PseudOS simply runs through the task queue in a loop and executes the task if it is in the "active" state. In this example, a static variable named "tickDelay" tracks the number of task function executions until the desired code is executed.

```
int main(void)
{
    ...
    const char * sampTask0NameString = "Sample Task 0";
    sampTask0.taskName = sampTask0NameString;
    sampTask0.status = ACTIVE;
    sampTask0.taskPtr = sampTask0_Func;
    ...
    initSys->utaskReg[0] = &sampTask0;
    ...
}

void sampTask0_Func(void * taskDataPtr)
{
    static uint16_t tickDelay = 1500;
    if(tickDelay == 0)
    {
        printf("\nSample Task 0!\n");
```

```
        printf("Executes every 1500 ticks\n");
        tickDelay = 1500;
    }
    else
    {
        tickDelay--;
    }
}
```

Listing 4.1: Sample task in PseudOS

In contrast, applications should be used for more robust portions of code. An example of an application is shown in Program-code 4.2. Similar to task initialization, applications are setup in the main function. Applications may be scheduled for a single execution or a repeated execution, and allows for adjustment of priority in case of scheduling conflicts.

```
int main(void)
{
    ...
    prog_t * sampApp3_Setup = (prog_t*)malloc(sizeof(prog_t));
    progSched_t * sampApp3_Sched = (progSched_t*)malloc(sizeof(
       progSched_t));
    initProgDefault(sampApp3_Setup);
    sampApp3_Setup->info.cmdStr = "sampApp3";
    sampApp3_Setup->info.help = "Help: Samp App 3 Info will go here\n";
    sampApp3_Setup->progReg = &sampApp3;
    sampApp3_Sched->priority = -1;
    sampApp3_Sched->repeat = true;
    sampApp3_Sched->time.csec_u32 = 2000;
    sampApp3_Setup->schedule = sampApp3_Sched;
    ...
    initSys->progReg[0] = sampApp3_Setup;
    ...
```

```
}


int8_t sampApp3(progVars_t * progVars)
{
    (void)progVars;
    printf("Sample Application 3\nSystem Time=\n");
    apiPrintSystemTime(true);
    return PROG_EXIT_OK;
}
```

Listing 4.2: Sample Application in PseudOS

Command-Line Interface

The pseudOS CLI was loosely modeled after familiar CLIs like those found in UNIX-style OSs, and access to it is provided via the UART serial port by default. The CLI allows execution of user applications and access to kernel processes in an intuitive manner. Furthermore, this CLI lends itself to simple integration into a more automated and graphical Python application. The normal PseudOS startup is shown in fig. 4.4, followed by some user commands. Note the execution of the task and the scheduled application.

Although PseudOS was developed for the MSP430FR5994, it was also ported to the PSOC 5LP, which is used for base station control. While the PSOC 5LP is more capable than the MSP430, allowing it to host more robust OSs, a simple serial interface for user control was required as was the ability to create some small applications.

4.3 Implant Environmental Monitoring

Implantable bioelectronic devices require packaging to protect the surrounding biological tissue and the internal, sensitive electronics. Even with state-of-the-art LCP encapsulation methods, the risk of internal humidity increase necessitates monitoring. In [52], while the LCP package significantly outperformed other encapsulation methods during a 300-day soak

```
HW: Serial [OK]
HW: SysClk = 2 cs [OK]
SysTask: App Sched [OK]
SysTask: shell [OK]
SysTask: printf [OK]
HW: RTC [OK]
SysTask: Human Time [OK]
Queue: Sample Task 0 [OK]
Queue: Sample Task 1 [OK]
Reg: sampApp3 [OK]
Sched: sampApp3 [OK]

    ***************
    * pseudOS *
    ***************

$>sysutil -h
Shell Utilities Help
------------------------------
Usage: sysutil [OPT][DATA]
Example: sysutil -a human -x systime
  -x  |  Exec system util.
  -a  |  Util exec parameter. Must precede -x.
  -l  |  List avail system utils.
  -h  |  Help Menu.
$>sysutil -l
Available Util
----------------
 CMD  |  Desc
----------------
showqueue    | Show task queue.
systime      | Show sys time. (-a Human)
showrealtime | Show RTC.
setrealtime  | Set RTC.
showappsched | Show sched. apps.
hwreset      | Reset uC.
$>sysutil -x showqueue
Tasks in Queue:
ID  |   Name    |   Status
--------------------------------------
0        App Scheduler        ACTIVE
1        Shell        ACTIVE
2        Printf        ACTIVE
3        Human Time        ACTIVE
4        Sample Task 0        ACTIVE
5        Sample Task 1        SLEEP
$>sysutil -x showappsched
Scheduled Programs:
Entry | Name  | Time(centi-s)
--------------------------------
0 | sampApp3 | 2000

$>Sample Application 3
System Time=
[00000:0:00:00:20]
$>
Sample Task 0!
Executes every 1500 ticks
```

Figure 4.4: PseudOS Command-Line Interface.

test, evidence of humidity increase was still present. Furthermore, the LCP packages in [52] relied on "welding" of the LCP material to form a hermetic seal. While this project may ultimately utilize this method, the present process of epoxy sealing the LCP package halves is susceptible to leakage. Indeed, the SLS 3-D printed enclosures are even more susceptible to damaging levels of humidity. Irrespective of the process or material, unanticipated moisture could, at a minimum, produce inaccurate or unreliable functionality, or in the worst case, device failure. Additionally, a device fault may result in unexpected temperature and/or pressure increase inside the package, which could damage the device, or worse, the surrounding biological tissue.

In any case, abnormal environmental conditions inside the packaging must be monitored. The environmental sensing need not be at a high sample rate. Given the required form factor and power considerations, the ideal sensing device must have extremely low static or standby power consumption, low dynamic power consumption, and reasonable accuracy given the application.

The Bosch Sensortec BME280 Humidity and Pressure sensor [9] is a near ideal solution for this type of application. It is small, simple, and operates at low voltage and power. The BME280 has three sensing elements—pressure, humidity and temperature—sharing a single multiplexed 16-bit ADC. The dimensions are 2.50 mm x 2.50 mm x 0.93 mm and is shown in fig. 4.5, while being flanked by two 0603 decoupling capacitors. The micro-scale implant uses 0201 decoupling capacitors. The device operates down to 1.71 V for analog and 1.2 V for digital. Although the BME280 is capable of high sample rates, it was optimized for a duty-cycling approach where the temperature, pressure and humidity are measured followed by a long standby state. Current consumption during a sensing interval can reach 714 uA for a pressure reading, at a refresh rate of 1 Hz, it will be as low as 3.6 uA, and it consumes 100 nA (typical) while in sleep mode.

The raw ADC data from the registers must be compensated for accuracy and converted into standard units for analysis. The BME280 is provided with factory-tuned calibration constants, unique to each device. Therefore, on the first startup, these values must be read

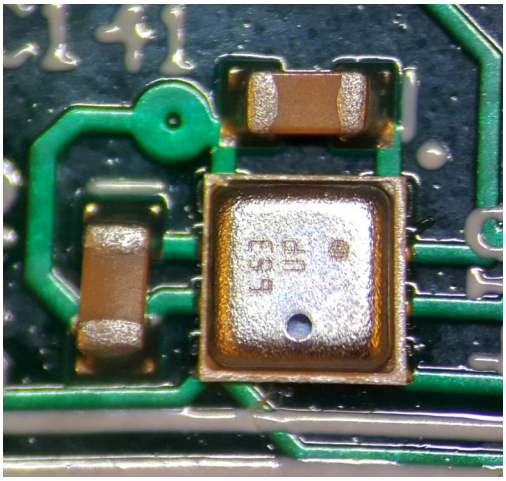


Figure 4.5: Bosch BME280 Humidity and Pressure Sensor.

from read-only registers on the BME280. With these constants, pressure can readily be converted to Pascals, temperature to degrees Celsius and humidity to Relative Humidity. During operation, the raw ADC data is monitored for unsafe operating conditions. The data is also stored and transmitted to the base station on demand.

Chapter 5
COMMUNICATION SYSTEM

To have practical control of the implant device, in the absence of a hard-wired serial link, wireless communication is an obvious requirement. Sufficient data-rate specifications are arguably subjective, perhaps even arbitrary; however, from the beginning of our GSK BIC work, seeking maximum data rates around 2 Mbps was deemed a challenging, yet achievable, goal. Given the initial implant memory of 512 Mbit, and later the 4 x 64 Mbit array, a 2 Mbps uplink placed a complete neural data upload in the range of about five minutes.

Indeed, literature is replete with data rates faster than 2 Mbps, albeit normally without the system constraints imposed on the implant. Often the data rates are achieved only in a limited bench-top setting with little regard to system-level performance. A practical implementation would be confined to a tiny enclosure. Additionally, these data rates are sometimes reported with unrealistically high-power demands or low-transmission distances.

A more practical communication sub-system for an implant would, therefore, need to achieve a reasonably high uplink speed, the previously stated 2 Mbps goal, as well as a responsive downlink speed. By responsive, it is assumed simple commands will be transmitted to the implant for basic configuration, control and scheduling. A standard baud rate of 115.2 kbps was set as the goal for maximum downlink speeds.

5.1 Background

Over the various iterations of communication sub-systems, some preceding the GSK BIC project, low-power RF communication was the natural choice, given our lab experience with backscatter communication. Although the details of backscatter communication can be quite complex, conceptually the hardware is relatively simple. Our early designs, as well as the

GSK BIC version, used circuitry based on the early WISP architectures [77]. In short, the hardware "transmits" data by performing load modulation, thereby reflecting some of the incoming RF signal back to the interrogating device. The receive circuitry expects an amplitude shift-keyed RF signal, which is demodulated via a rectification. The envelope is then compared to a time-averaged version of itself to accommodate changes in signal strength. A low-powered comparator is implemented for this process, which is then fed to the MSP430 for decoding. The result is exceptional data rates at power consumption levels around 100 times lower than even the best active transceivers. A high-level block diagram of the system is shown in fig. 5.1. Note that the so-called "Hummingbird Protocol" was custom firmware for achieving 2 Mbps data rates with the MSP430 eUSCI peripheral. It was designed by Xingyi Shi of the Sensor Systems Lab.

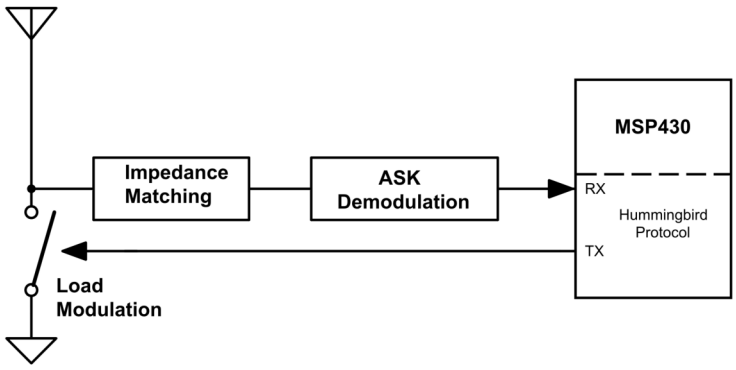


Figure 5.1: Simplified backscatter communication diagram showing a MOSFET for load modulation, an L-match network for matching, a Dickson Charge Pump for rectification and gain, and a comparator to extract data from the envelope.

In [85], we presented a dual-band wireless power and bi-directional data link implemented in 65 nm CMOS fig. 5.2. The author was responsible for designing the RF front-end for the UHF backscatter communication. This CMOS device achieved 25 mW of power conversion at an efficiency of 80%, while a 6 Mbps uplink data rate was demonstrated for the communication, all at 10 mm. Despite the range limitation and power numbers lower

than this project device requires, it demonstrates not only that our 2 Mbps goal is possible, but also suggested that most of the design in this project can be successfully adapted to an integrated circuit.

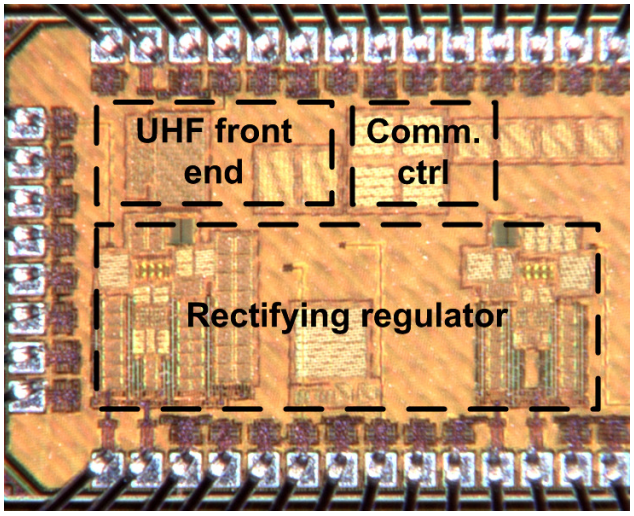


Figure 5.2: A 65 nm CMOS Wireless Power and Bi-Directional Communication IC for implantable neural recording and stimulation applications.

The dual-band antenna structure shown in fig. 5.3 was used for experimental validation. The 13.56 MHz loop and coil for the transmitter side had an overall diameter of 6.5 cm, and the RX wireless power coil was a tightly-wound planar-spiral coil with a diameter of 20 mm. The UHF antenna on the reader side was a segmented-loop structure based on the design presented in [6], while the loop on the RX side was approximately 10 mm in diameter.

One of the drawbacks of a co-axial dual-band antenna structure is the high-degree of coupling between the HF coil and UHF loop [40]. However, as shown in fig. 5.4, simultaneous wireless power and communication via the dual-band antenna was viable on a testbench. The time-domain signals are shown in fig. 5.4(a), while fig. 5.4(b) shows the captured frequency spectrum. In the communication channel, interference of the wireless power at 25 mW is present, but 34.16 dB lower than the average power of the downlink data.

Of course, there are some obvious challenges implementing such a system in the presented

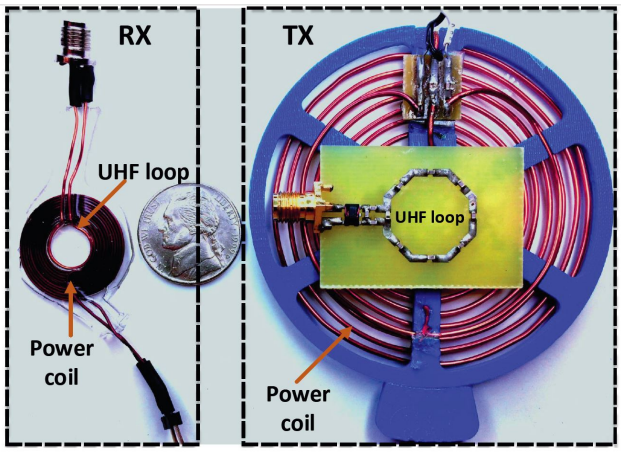
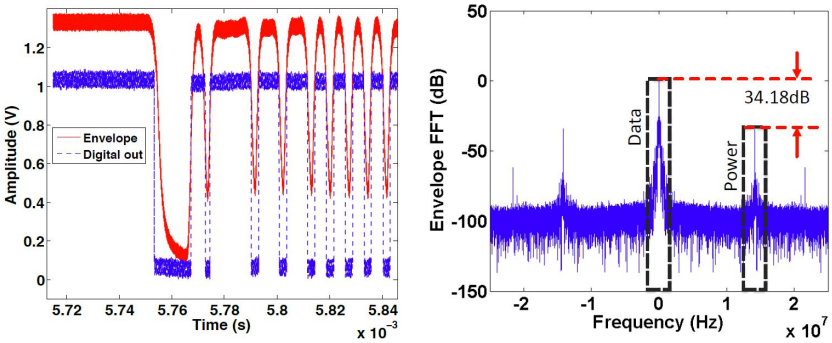


Figure 5.3: Co-axial HF Coil and UHF Loop Antenna Setup. © 2016 IEEE



(a) Time domain signal *(b) Frequency domain*

Figure 5.4: Dual-band communication performance. © 2016 IEEE

implant device. The size of the wireless power coil is too large for the enclosure. Furthermore, the wireless power required to charge the lithium battery is much larger than 25 mW. Consequently, other communication methods were explored.

5.2 IR Optical-Link Solution

During one of our experiments involving the so-called "lollipop" implant, which featured an RX PCB coil and LEDs for optical stimulation, a potential solution presented itself. As shown in fig. 5.5, light in the visible EM spectrum (615 nm) easily penetrates through the abdominal skin of a sedated rat. Both blue and red LEDs were easily observable; however, the longer wavelength red LED was significantly more pronounced.

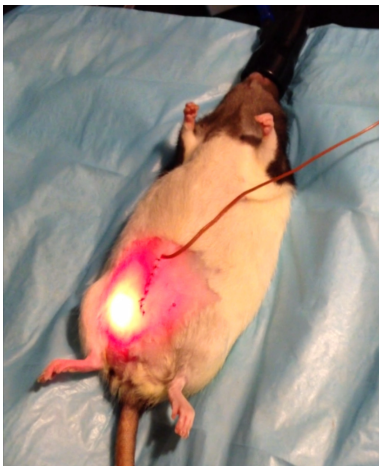


Figure 5.5: LED emission at 615 nm penetrating through abdominal skin of a sedated rat.

Research into optical communication for implantable devices has been conducted for decades [32, 48]. Furthermore, optical properties for transmission across human skin are also well investigated. While other factors could have contributed to the perceived red LED light transmission dominating that of its blue counterpart, transdermal optical transmission favors the longer wavelength side of the spectrum. However, the massive power consumption of the 615 nm LED used for optogenetic stimulation would not be practical for a communication

link. Additionally, the optical properties of the enclosure must be accounted for.

5.2.1 Sapphire Optical Window

Transmission in the near-IR region is possible through both LCP and the nylon-like 3-D printed material, albeit with considerable attenuation. To mitigate optical loss, an IR-window was implemented directly above the IR LED and photodiode in the implant enclosure. The choice of material is not arbitrary. The IR window should not have significant effects on magnetic and electrical performance. Likewise, it should not compromise the integrity of a hermetically-sealed enclosure. Lastly, it must retain acceptable bio-compatibility.

Sapphire is one such material and has been heavily researched. Sapphire has excellent electrical performance, especially considering its insulation and dielectric behavior. In fact, sapphire has been proposed as a substrate material dating back to the 1960's [58]. The optical performance of sapphire shows minimal attenuation in the near-IR region and is considered optically transparent with about 86% optical transmission near a wavelength of 1300nm [17].

Additionally, the biocompatibility of sapphire has also been extensively studied. Sapphire has been specifically examined for implantable devices with generally favorable results. In [36], a vertical-cavity surface-emitting laser (VCSEL) hermetically sealed inside a sapphire enclosure was demonstrated. Some bio-compatibility issues have been encountered with long-term implantation in neural environments [72,87]. It was suggested that surface modification may be required to improve this specific deficit.

5.2.2 Biological Optical Window

The optical properties of skin causing attenuation are complex and highly variable. Biological tissue and fluids interact with penetrating light, which leads to absorption and scattering. The relationship between human-skin attenuation and wavelength has been investigated in a number of studies [5, 14, 23, 28]. In each of these publications, an optical window appears in certain wavelength ranges where the cumulative effect of absorption and scattering create

local minima. The near-IR region, from approximately 1000 nm to 1300 nm, shows the least amount of attenuation.

5.2.3 LED Bandgap Voltage

A convenient coincidence of the near-IR optical window is the general relationship between LED bandgap voltage and wavelength. As shown in equation eq. (5.1), the energy of photo emission from a semi-conductor material is inversely proportion to wavelength. At 1300 nm, for example, the energy is 0.95 eV. Near-IR LEDs, available commercially, present a forward voltage drop of about 1 V when conducting in the tens of mA range. While LEDs vary greatly in terms of efficiency, intensity, etc., this trend suggests the possibility of a considerable reduction in power dissipation by choosing an LED with larger wavelengths.

$$E = \frac{hc}{\lambda} \approx \frac{1240\,[eV \cdot nm]}{\lambda} \tag{5.1}$$

Although a thorough analysis would be required before drawing conclusions, the properties of sapphire, biological tissue and LED bandgap voltage suggest an optimal wavelength in the near-IR region for transdermal communication.

5.3 IR TX Hardware Design

In general, research and commercial design of LED drivers for optical communications is very mature, if not antiquated in some regards. Even before fiber optic communication links, IR remote controls for television sets have been used for decades. For a brief period, free-space optical communication promised to be a method for high-speed wireless communication for consumer devices. In the ‘90s and early ‘00s, the Infrared Data Association (IrDA) specified standardized transmission protocols designed for data rates exceeding 1 Gbps [10]. Given the relatively inexpensive availability of low-power UHF radios, like Bluetooth, the promising high-data rate communication using free-space IR links has been mostly driven into obsolescence. Nonetheless, IR communication for implantable devices with Mbps data

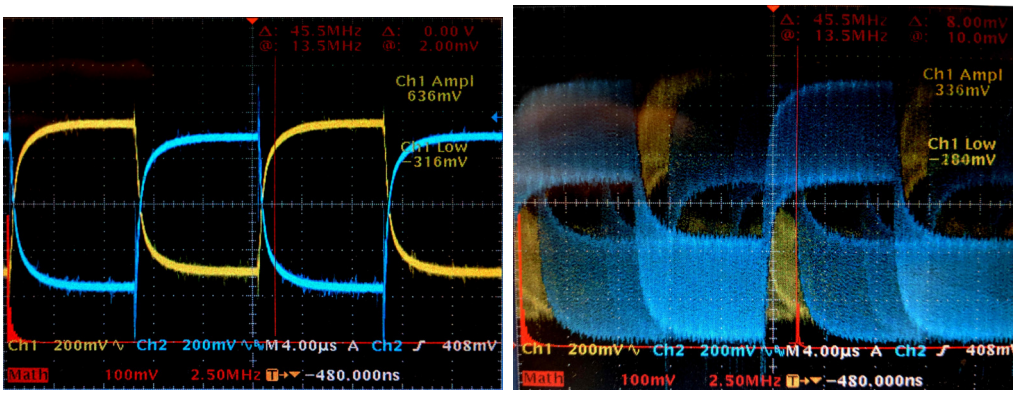
rates has perhaps created a niche design space.

While a naive LED driver for communication may be accomplished with a simple series-connected resistor switched by a transistor, achieving data rates into the Mbps range is not trivial. Of course, diodes have a non-linear I-V relationship; however, the parasitic capacitance when driving LEDs into the MHz range is problematic. When forward biasing a diode, this capacitance must be charged for an LED to be properly illuminated. Conversely, this charge must also be removed for the LED to extinguish. The naive implementation discussed above, therefore, is limited by an RC time constant while being illuminated, but it fails to address the removal of charges while "turning off". It is this latter issue that is generally overlooked.

Many high power, large footprint solutions exist to address this design challenge, but the implantable device cannot employ such techniques. More robust designs often maintain some level of bias current for the LED. While this was investigated, such a design increased the complexity and physical size of the driver. A brief review of literature reveals some relatively simple techniques for rapidly removing charges from the parasitic capacitance.

In [26], a clever topology is introduced whereby the naive implementation provides faster turn-on time by placing a capacitor in parallel with the resistor. The result is some current peeking when the LED is first switched on. To "sweep-out" the charges, an inductor is placed in parallel with the resistor, capacitor, and LED, thereby forcing a free-wheeling like reverse-bias condition that forces the charges back out of the LED. For the implantable LED driver, this technique was avoided due to inductor size, tuning and power consumption. More practical designs are shown in [47] and [46] where MOSFETs are employed to essentially short the LED when switched off. The charge sweeping effect is not as pronounced as that with an inductor, but the MOSFET presents a low-impedance path for capacitance discharge in the off phase of the LED. This general concept was implemented in the design of both implant and base-station IR LED drivers.

A secondary design goal was also investigated. The ability to achieve simultaneous wireless power and communication would provide great benefit to the performance of the



(a) Reference optical signal.

(b) Captured signal in the presence of wireless power.

Figure 5.6: Optical signal interference with wireless power present.

entire system. As discussed above, this ability has been achieved with certain technologies. One of the benefits of optical communications is that the TX LED and RX photodiode will not interact with the wireless power coils in a significant manner. Nonetheless, when working with wireless-power devices, the level of noise present in the adjacent electrical hardware will overwhelm other signals. Digital signaling is usually quite immune, as we have successfully employed microcontrollers into regions of high magnetic field strength. Capturing and amplifying a small IR signal, on the other hand, presents considerable challenges. An early bench test, with a photodiode placed coaxially with the wireless-power RX coil, shows the corrupting nature of wireless power when attempting to receive data fig. 5.6. Consequently, the design approach from early stages was to strategically place IR RX components in areas of lower magnetic flux intensity or provide shielding when possible. Furthermore, placing a heavy emphasis on common-mode rejection within the RX amplifier chain was also pursued.

Implant LED Driver

With limited space and energy resources, a simple, yet effective LED driver was required. The ultimate design is shown in fig. 5.7. Simulation of the RJU003N003 transistors in this arrangement showed effective switching of an LED model up to approximately 10 MHz. The IR LED employed in this application is an infrared emitter by Marktech Optoelectronics (MTE0013-996-IR). It is designed for optical communication and specifies a forward voltage of approximately 1 V when driven at 25 mA. In this design, the TXB0102 level shifter also provides adequate high-side driving of QTX1 given that the variable XVX supply is switched to 5 V. QTX1 and QTX2 are specified with a drain-source voltage [V_{DS}] of less than about 50 mV with 25 mA of drain current while being driven with a gate-source voltage [V_{GS}] larger than 4 V. QTX1, in this design, is responsible for the turn-on phase of the LED, while QTX2 is responsible for draining the parasitic capacitance. RTX1 provides a small amount of resistance to help regulate the current since 1V0 is provided by a voltage regulator and not a more ideal current source. RTX2 helps maintain a small current flow to both accelerate current flow into the LED and alleviate hard switching for the voltage regulator.

The choice of a voltage regulator in this design was driven from a perspective of design space and efficiency. To maximize efficiency, a buck-converter topology was sought. While buck-converters may be configured as current-sources, the added complexity and physical size far outweighed any benefit. However, besides seeking a buck converter that is efficient for the specific load, there are some limiting factors that must be addressed. Firstly, the availability of buck converters that provide a regulated voltage down to 1 V are somewhat limited, more so when seeking one in a compact package. Torex manufactures micro buck converters with an inductor integrated into the package. While general performance was good, the switching frequency and transient response of the buck converter resulted in amplitude modulated IR pulses in the tens of kHz range, thereby distorting the received signal. Consequently, the MIC23030 buck converter from Microchip Technology was used instead. While the MIC23030 isn't as efficient for the required load specifications, it has a switching frequency of 8 MHz

in continuous conduction mode. The high-frequency switching also had the benefit of using a smaller inductor and improved transient response.

Implant Driver

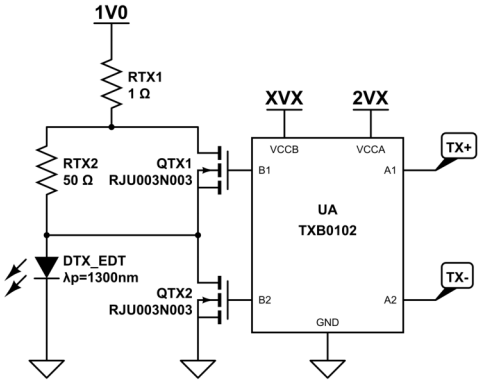


Figure 5.7: Implant IR AFE LED driver.

Base-Station Driver

The base-station TX driver had different design goals. Firstly, since power consumption and physical size were not as constrained as the implant, multiple IR LEDs would be used. Secondly, the downlink data rate was not as critical as the uplink data rate. The target was 115.2 kbps. Thirdly, the base-station implemented an externally connected AFE (BS-AFE) for wireless power and IR Communication to help reduce noise in the IR RX circuitry and provide a practical means of deploying the system in a laboratory setting.

Therefore, either the IR TX driving signal or the IR TX power supply lines would have to be carried through a cable of approximately 1 m in length. The former choice of placing the IR LED driver in the base station proved to be a poor choice. Once the LED was moved to the end of a cable, excessive ringing was observed fig. 5.8, presumably due to cable inductance. Therefore, the latter choice of placing the driver in the BS-AFE was selected.

However, hard switching of an LED with power supplied by the base station still risked the introduction of noise, as was verified in simulation.

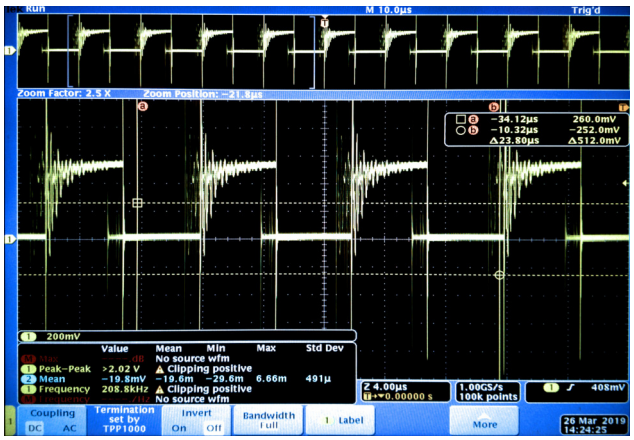


Figure 5.8: Ringing at base-station when driving remote IR LEDs through a cable.

With the first two design goals readily achievable, the reduction in switching noise was the primary concern. Furthermore, placing the drive circuitry in the remote BS-AFE placed a limit on the size and layout of the drive circuitry. The final design is shown in fig. 5.9. D41 through D44 are the same IR LED emitters as used in the implant device. Of course, here they are placed in series to reduce current draw over the USB 3.0 cable. The design is similar to that of the implant with regards to the MOSFET switching: Q40 is responsible for driving the LEDs to the "on" state, while Q41 provides a mechanism to dump some of the charge on the LEDs. With slightly more space available and because of the higher voltage requirements of Q40, a high-side gate driver was selected. The LED supply current is provided by a linear regulator utilized as a current source. The LT3042 is an LDO linear regulator where the regulated output voltage is set by a single resistor, as is the maximum output current. By carefully selecting values for the maximum Vout to that expected by the combined voltage drop of the LEDs and the maximum Iout to that of the drive current, the LT3042 behaves similarly to a current source. The inclusion of the 100 Ω resistor ensures that the LED drive current remains constant regardless of the switching state.

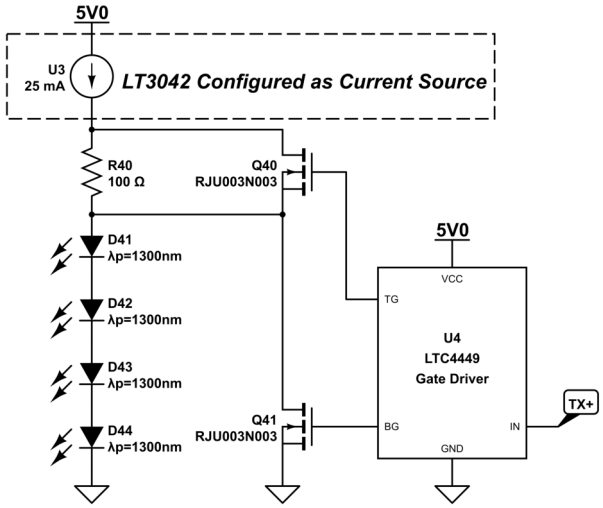


Figure 5.9: BS-AFE IR LED driver.

5.4 RX Hardware Design

While the described functionality of the implant device requires relatively low data rates for successful transmission of simple commands, providing a higher bit rate provides flexibility for future designs that may require large amounts of downlink data. Additionally, a higher data rate provides symmetry between the uplink and downlink, which enhances the overall communication throughput. While the PSoC can seamlessly adjust the IrDA clock, the MSP430FR5994 must be completely reconfigured to achieve a new baud rate. Therefore, a reasonably high, standard serial bit rate was selected for the downlink: 115.2 kbps. Of course, the IR signal must also travel the nominal use case distance in free space and through biological tissue, while minimizing power dissipation.

In both implant and base-station designs, heavy emphasis was placed on noise reduction. The AFEs and subsequent cascaded amplifiers on both units used fully-differential amplifiers (FDAs). Physical routing of traces and placement of components was based on maintaining high-data rates and minimizing noise. The latter goal of minimizing noise was critical due to the high transimpedance gain, especially that of the base station.

Following the AFE stages, both the implant and base station used programmable gain amplifiers (PGAs). Given a practical use case, a RUT would not remain still in an ideal orientation for optimal IR communication. Therefore, an ability to dynamically adjust gain to increase a weak signal or attenuate an overly strong signal was implemented. The PGAs combined with the microcontroller functionality provide automatic gain control (AGC).

5.4.1 Implant

The transimpedance amplifier (TIA) front end for the implant is shown in fig. 5.10. The 1300 nm photodiode is connected differentially with zero-bias voltage to U7 (THS4531), which is an FDA. The TIA configuration shown limits the bandwidth to about 3.2 MHz. U7 connects to U8 (also a THS4531) via a high-pass filter setting the lower bound cutoff to about 1 kHz. The following FDA stage provides a voltage gain of 5.

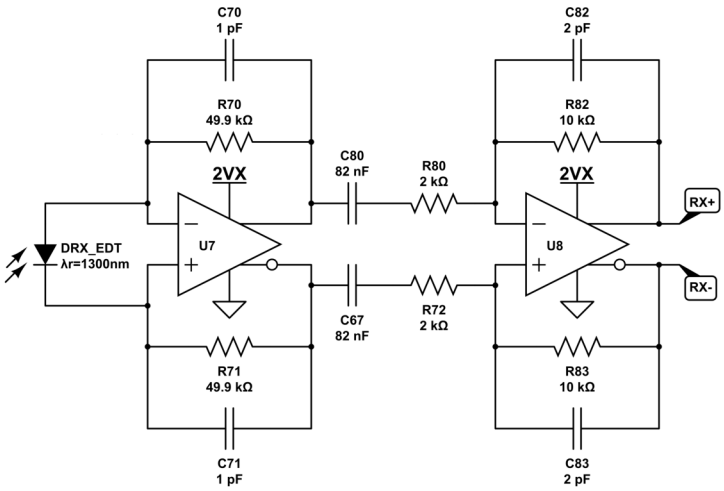


Figure 5.10: Implant fully-differential TIA for IR RX communication.

Following the differential to single-ended signal conversion, a PGA was designed using a standard op amp with integrated resistors and MSP430 GPIO. While PGA ICs are available commercially, none were identified that provided acceptable functionality and low-power

performance while occupying minimal space. The op amp structure implements a T-network for feedback. A similar network is often used in TIAs to boost gain without relying on impractical resistor values. The grounded leg of the T-network here provides an opportunity to manipulate the gain of this stage via a microcontroller.

The schematic in fig. 5.11 shows a group of grounded switches. By toggling microcontroller GPIOs from HI-Z to 0 V, a wide range of gains may be achieved. There are eight possible GPIO combinations, but only six unique gain settings. GPIO settings and corresponding equivalent network resistance R_{adj} are shown in table 5.1. Although there are a discrete number of possible gains, the general behavior is expressed in eq. (5.2).

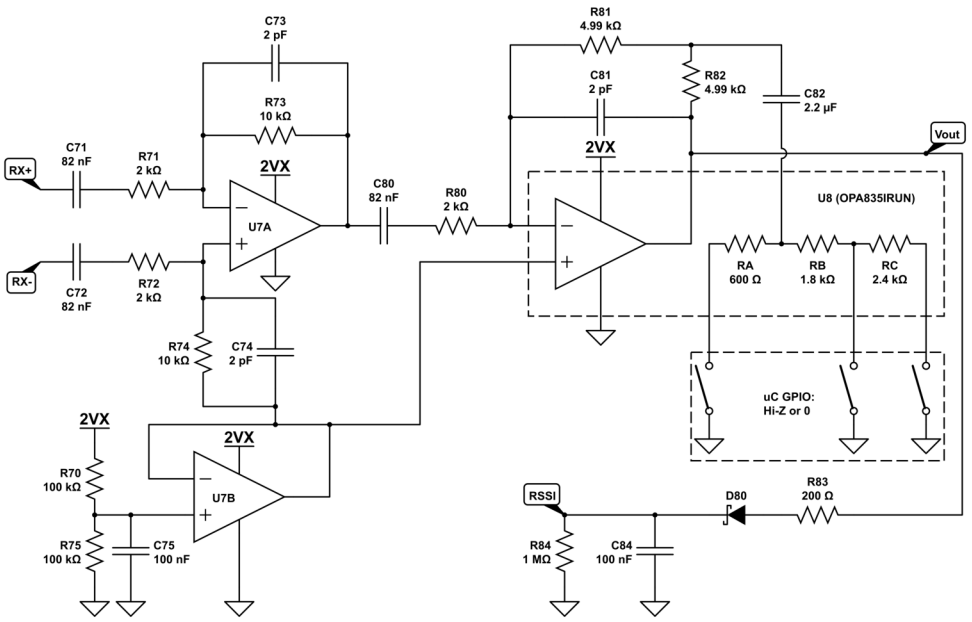


Figure 5.11: Implant RX chain with adjustable gain.

$$V_{out} = -V_{in}\left(\frac{sC_{80}}{1+sC_{80}R_{80}}\right)\left(R_{81}+R_{82}+\frac{sC_{82}R_{81}R_{82}}{1+sC_{82}R_{adj}}\right)+V_{bias} \tag{5.2}$$

The complete implant transimpedance gain, as a function of GPIO states, is shown in fig. 5.12. The legend in the upper left corner shows the state of each GPIO ordered as shown

Table 5.1: PGA GPIO Settings and Equivalent Resistances

$GPIO_A$	$GPIO_A$	$GPIO_A$	R_{adj}
Hi-Z	Hi-Z	Hi-Z	∞
Hi-Z	Hi-Z	0	$R_B + R_C$
Hi-Z	0	Hi-Z	R_B
Hi-Z	0	0	R_B
0	Hi-Z	Hi-Z	R_A
0	Hi-Z	0	$R_A \| \| R_C$
0	0	Hi-Z	$R_A \| \| R_B$
0	0	0	$R_A \| \| R_B$

in fig. 5.11, from left to right. Because of the discrete resistor values in the OPA835, only six unique gains are possible.

5.4.2 Base Station

Connection to the remote base station IR AFE is achieved through a USB 3.0 cable. The design of the USB cable is critical to the IR communication performance. As shown in fig. 5.13, USB 3.0 cables provide dedicated power and data lines. The 3.0 standard provides two additional twisted, shielded differential pairs. One of the pairs is used to transfer the optical signal from the AFE TIA stage to the main base station device. The other lines provide 5 V power, TX signaling and control signals. To ensure signal integrity to the IR hardware mounted coaxially to the wireless power coil, the twisted, shielded pair concept was extended to the PCB. As shown in fig. 5.14, the traces are "twisted" by alternating PCB layers while the ground planes and via-stitching provided shielding.

The RX hardware on the BS-AFE is shown in fig. 5.15. A photodiode receives IR pulses with at a wavelength of 1300 nm. These pulses are then amplified by the differentially-

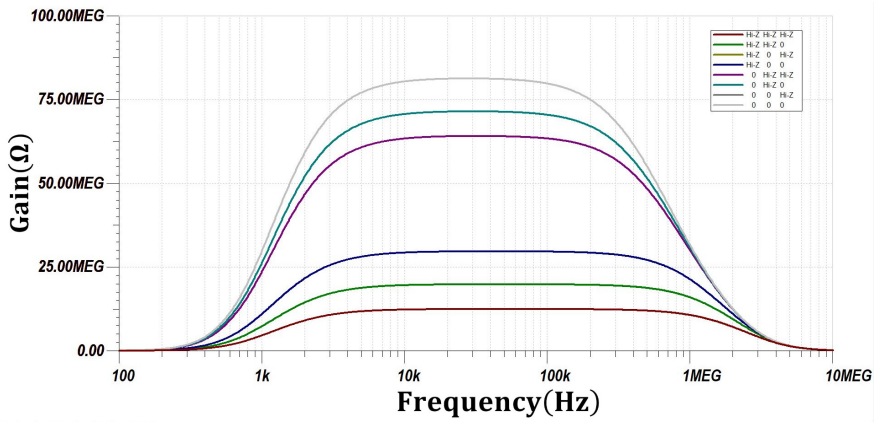


Figure 5.12: Simulated implant IR RX gain varied with GPIO settings.

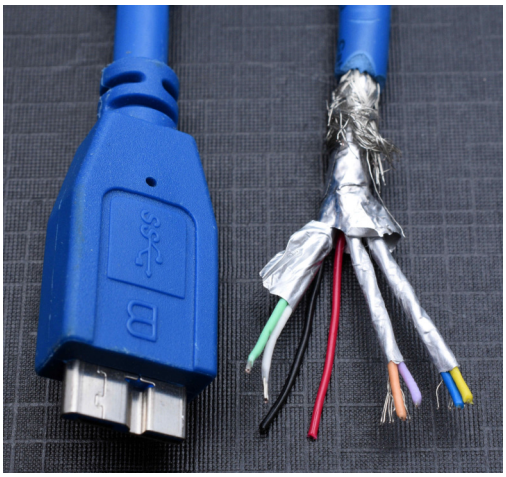
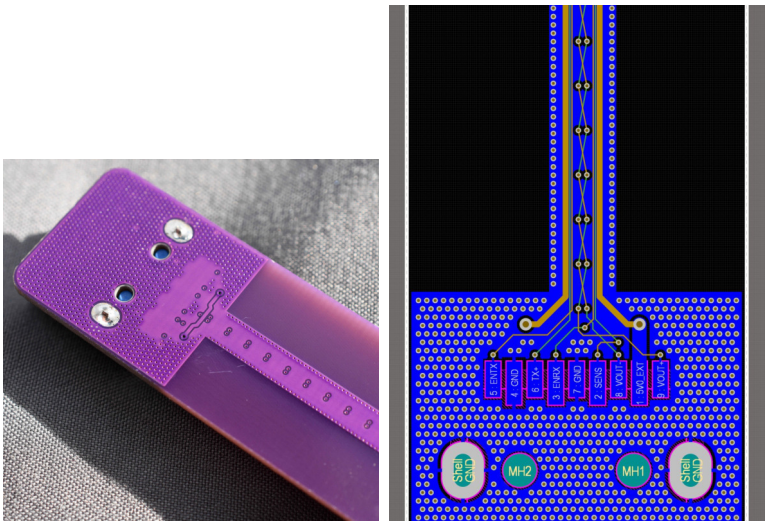


Figure 5.13: A USB 3.0 cable, used for connection to the BS-AFE, comprises power and high-speed data lines.



(a) Cable interface to BS-AFE. (b) PCB twisted-shielded pair.

Figure 5.14: Remote BS-AFE PCB design uses twisted-shielded RX lines with via-stitching.

connected TIA, and additional voltage gain is provided by the second amplifier stage. As shown in the schematic, the circuit was designed to provide user-selectable biasing to the photodiode. By changing the state of a buffer, the photodiode could be biased with 0 V or be reverse biased into the photo-conductive mode with 5 V. Subsequent testing showed no discernible difference in performance with the 5 V of biasing. High-performance FDAs were used in the base-station circuitry as the emphasis was less on power consumption, but more on ensuring the successful reception of IR signals from the implant device. The current design limited bandwidth to less than 13.56 MHz to achieve simultaneous wireless power transfer and communication.

The base-station PGA RX chain, on the other hand, was able to use a purpose-made PGA. The PGA870 is a high-performance PGA that draws nearly 143 mA of quiescent current but provides fine adjustment of gain via a six-bit digital control signal. The 650 MHz bandwidth is more than capable of supporting the uplink reception. The PGA870 output is then amplified by three stages of FDAs configured in multiple-feedback topologies,

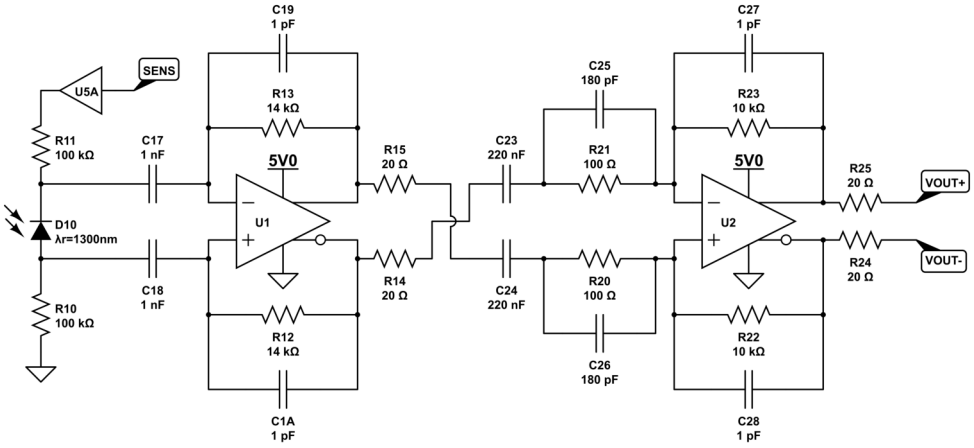


Figure 5.15: Base-station IR AFE.

which terminate into high-speed comparator and received signal strength indicator (RSSI) circuits.

The complete programmable gain of the base station IR RX amplifier system, from TIA to the final FDA, is shown in fig. 5.17. The plot shows simulated results of the circuit performance using manufacturer SPICE models for each of the exact ICs used in the system. With six bits, the PGA has 64 discrete settings. The simulated plot shows seven of those gain settings in increments of 5 dB, from -10 dB to the maximum +20 dB. The passband region was designed to have a flat response between about 10 kHz and 4 MHz. In the passband, the minimum transimpedance gain is $2.84 \times 10^6\,[dB_\Omega]$, while the maximum is $89.7 \times 10^6\,[dB_\Omega]$.

5.4.3 Microcontroller Peripherals

The onboard microcontroller peripherals on both the MSP430FR5994 and the PSOC 5LP form critical portions of the communication hardware. Starting with the implant, the MSP430FR5994 provides decoding of the IrDA signals via its internal eUSCI device. The details are discussed below, but UART data and IrDA data are very similar, which makes this possible. The MSP430FR5994 eUSCI could theoretically achieve slightly higher data rates,

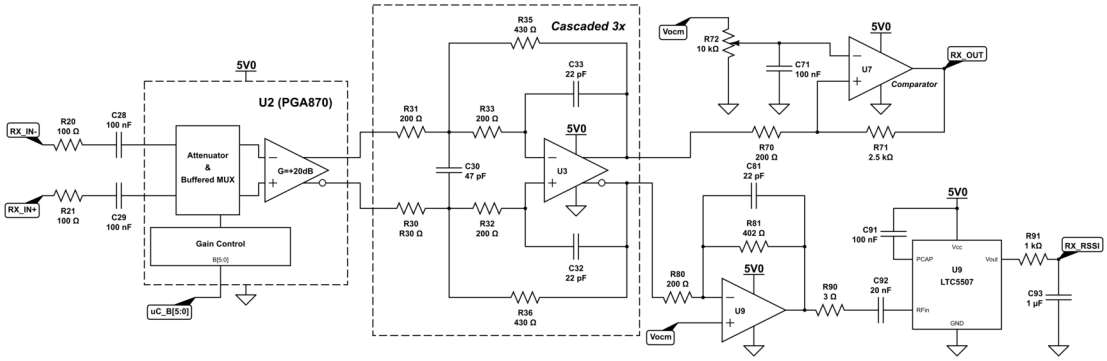


Figure 5.16: Base station high-performance PGA and cascaded FDAs.

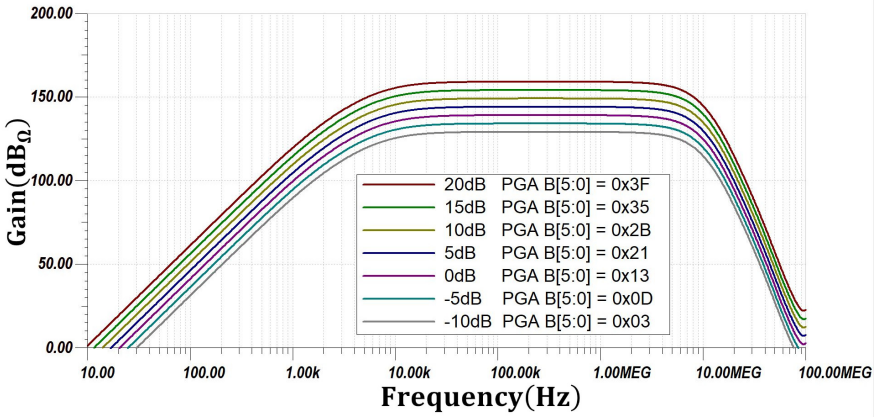


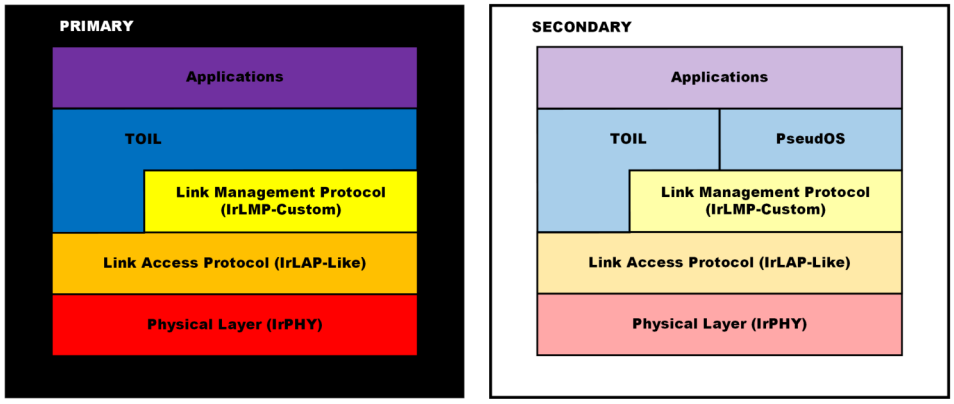
Figure 5.17: Simulated adjustable gain of complete IR RX amplifier chain.

but the limitations of clock speed, IrDA pulse width, and the asynchronous nature of the data frame, limit practical throughput to around 2 Mbps. Before the IR signal enters the eUSCI device, the amplified analog signal is converted to digital via the integrated comparator. The MSP430 comparator easily meets speed requirements but is also highly configurable via C code. The integrated comparator can quickly change hysteresis levels and adjust for changes in bias levels at run time. Also, the ADC was used to monitor the RSSI signal.

The PSOC 5LP provided similar functionality; however, the actual implementation required a slightly different approach. While the PSOC 5LP allows for considerable digital and analog flexibility, an IrDA to UART conversion block is not provided. Consequently, the IrDA decoding was accomplished via PSOC digital blocks in combination with a UART block. The PSOC Creator schematic can be seen in Appendix A. Speed limitations on the integrated analog devices forced external design of communication hardware.

5.5 Custom IrDA-Lite Protocol

To ensure integrity of the IR communication link, a multi-layer stack was implemented in both the MSP430FR5994 and the PSOC 5LP. Given the availability of integrated peripherals on microcontrollers, and existing protocol stacks, a custom implementation of the IrDA protocol was developed. IrDA is an initialism for the Infrared Data Association. The IrDA provides specifications for an existing protocol designed for wireless IR data transfer. While IrDA data transfer is in many cases an archaic protocol for consumer devices, various schemes were implemented to achieve various data rates and a variety of different capabilities regarding interface with end-user applications. While MSP430s can decode IrDA data frames, the higher layers of the protocol are not built into the hardware. Although ready-to-implement IrDA stacks are available, none were identified that would be appropriate for this application. Consequently, an IrDA-like protocol was coded from the ground up on both the MSP430FR5994 and the PSoC 5LP. Some brief research identified that basic IrDA stacks had been implemented on a different version of the MSP430; however, none of that code was available. Nonetheless, details of a lightweight protocol version, "IrDA-



(a) PSOC 5LP primary stack. (b) MSP430 secondary stack.

Figure 5.18: Modified IrDA protocol stacks customized for primary and secondary.

Lite", are well-documented [83]. Furthermore, documentation exists specifically regarding the implementation of IrDA-Lite on an MSP430 [38, 70].

IrDA operates in one of two device modes: primary and secondary. There should only be one primary device, and it is responsible for managing connections to valid secondaries. By design, the primary initiates all transmissions, while the secondary can only respond. Therefore, the first task of the primary device is to "discover" secondary devices and negotiate a link. In this application, it is assumed there is only one secondary, which is the implant device. The primary would therefore be the base station. This distinction does allow a certain degree of simplicity since a primary-only and secondary-only stack must be developed on the PSOC 5LP and MSP430, respectively. A graphical representation of the stack is shown in fig. 5.18. Both stacks are quite similar.

The IrPHY layer in this custom implementation adhered very closely to IrDA specification. This layer is responsible for decoding and validation of the individual transmitted bytes. Moving up through the layers, the standards were relaxed to tailor the stack to the needs of this application. The IrLAP layer processes valid frames, which contain device addresses, commands, and data. Specific frame types are used throughout the process, which enable

the sending of simple commands and the reliable transfer of numbered information frames. In this custom version, all frame types are as specified. A limited set of commands was used, and certain timing specifications were modified. Normally, IrDA stacks use an IrLMP layer for data-flow management and application interfacing, behaving as a multiplexer for different services. This level of capabilities is much more robust than what is required for this use case. Therefore, the IrLMP layer has been significantly simplified. It interfaces directly with PseudOS or through the transdermal optical-inductive link (TOIL) driver.

While the details regarding the stack are beyond the scope of this dissertation, a brief look at the IrDA data packets received by the microcontroller peripheral and the IrLAP frame structure is warranted. A standard asynchronous data packet is shown in fig. 5.19. The structure of common UART data is readily converted to IrDA data. IrDA modulation is a return-to-zero inverted (RZI) scheme. At bitrates up 115.2 kbps, a pulse measuring $\frac{3}{16}$ the bit width is generated when a zero bit is encountered. At higher data rates, this is expanded to $\frac{1}{4}$.

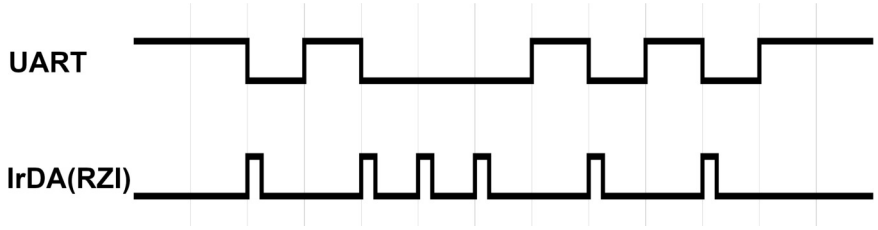


Figure 5.19: UART data versus IrDA data format.

Once a valid frame is received via the IrPHY layer, the IrLAP layer is notified so it can process the frame. The general structure of all frames is shown in fig. 5.20. All frames start with special beginning of frame (BOF) bytes. Extra BOF (XBOF) bytes are optionally added for timing purposes. The actual BOF marker is always 1 byte. Following this byte, the payload data is variable in size, and is only limited by specification and hardware capability. A frame-check sequence (FCS) is provided via a 16-bit cyclic redundancy check (CRC). The final byte is the end of frame (EOF) character. This structure is validated by IrPHY

and then passed onto the IrLAP layer where it processes the payload, which comprises an address (ADDR) byte, control (CTRL) byte, and optional information bytes. A flowchart of the implemented IrPHY process is shown in fig. 5.21.

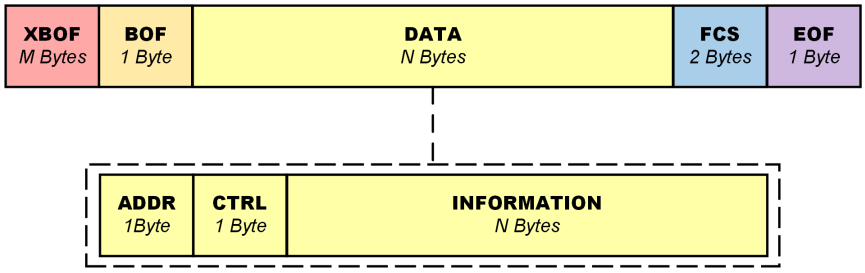


Figure 5.20: IrDA IrLAP frame format.

The IrLAP process on both microcontrollers is completely interrupt driven. While the IrPHY receipt of a valid frame triggers an interrupt, multiple timers are implemented to drive the IrLAP state machine. For a connection to be initiated between a primary and secondary device, information must be exchanged between the two devices. There are three defined states: offline, normal disconnect mode (NDM) and normal response mode (NRM). The uninitialized device is in the offline mode. Once initialized, the device is by default in NDM mode. The state machine is designed to establish a link and advance to NRM mode. This is true of both primary and secondary devices. A diagram showing the behavior of the IrLAP layer is shown in fig. 5.22.

5.6 Results

5.6.1 General Performance

Both uplink and downlink communication goals were achieved. As previously discussed, the power-constrained downlink hardware was designed for 115.2 kbps, while the uplink hardware was intended to reach 2 Mbps. In each case, IrLAP information frames can be sent with high reliability through free space or a phantom. The maximum downlink speeds reached

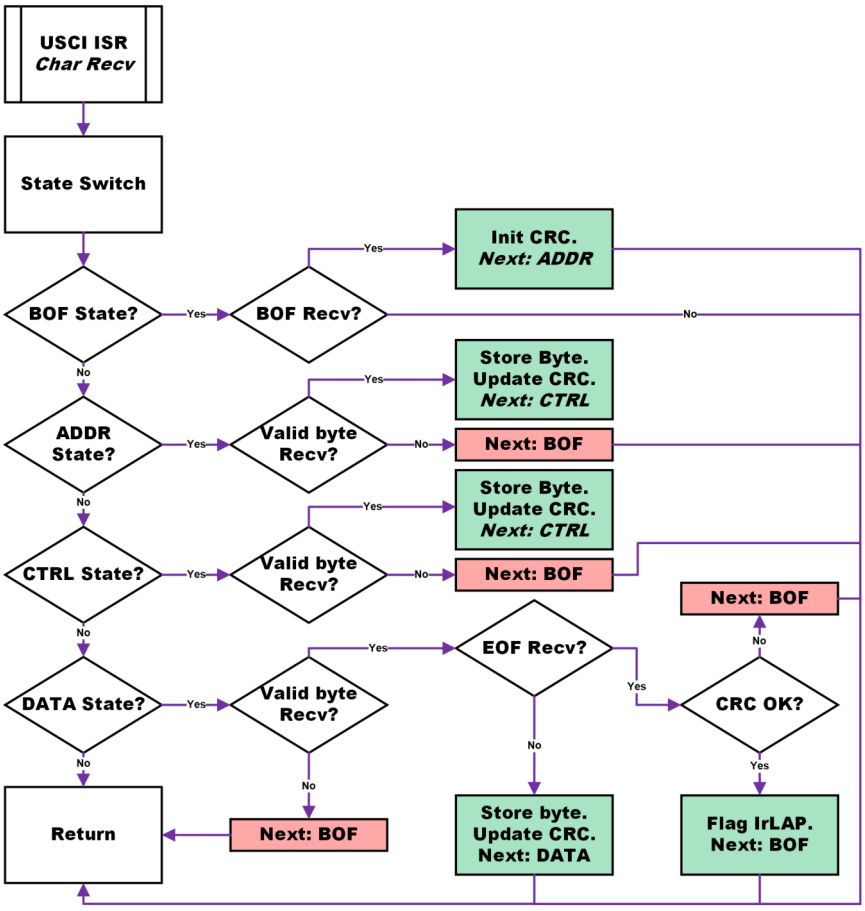


Figure 5.21: IrPHY RX Frame Recovery with CRC

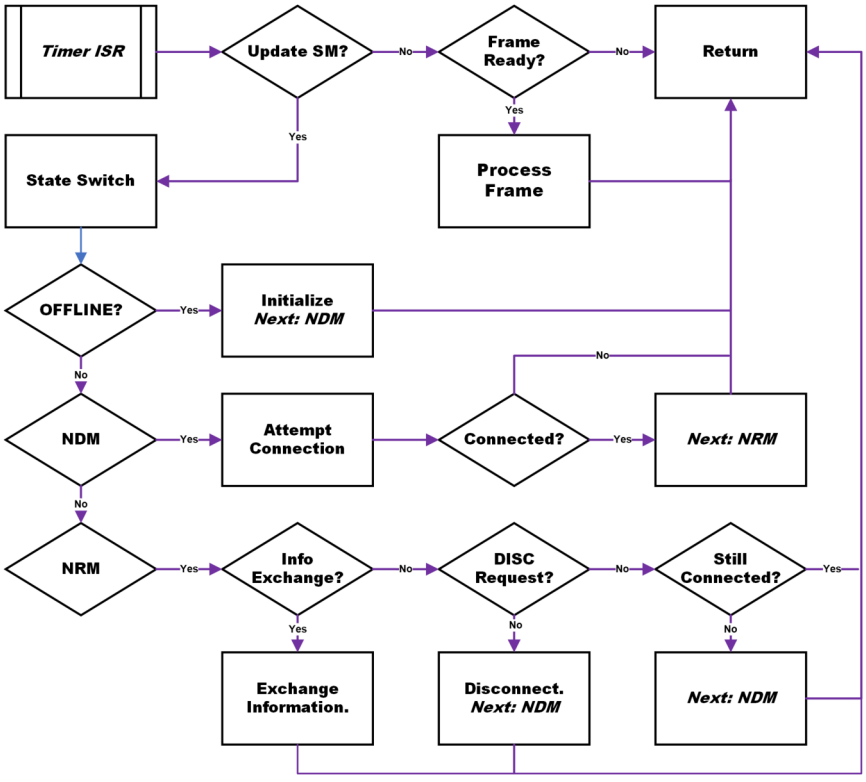


Figure 5.22: IrDA General Operation.

576 kbps through free space separated from a misaligned BS-AFE at about 9 cm. However, the implant RX circuitry dropped nearly 50% of the transmitted packets. In fig. 5.23, the yellow trace is the comparator output, while the blue trace is the PGA voltage output. In this oscilloscope shot, the pulse width is not consistent, most likely causing failed packets.

Figure 5.23: Implant receiving information frames at 576 kbps.

The uplink data rate of 2 Mbps was achieved with reliable performance. Wave forms of an example transmission are shown in fig. 5.24. The top yellow trace is the digital TX signal directly from the implant microcontroller. The middle blue trace is the recovered signal in the BS-M IR chain immediately before the high-speed comparator. The bottom pink trace shows the output from the comparator, which is inverted by the PSoC 5LP before being decoded.

Simultaneous wireless power and IR communication was not possible with this design. Even at low wireless power levels, the received IR signal was corrupted, which is most likely a result of the massive transimpedance gain.

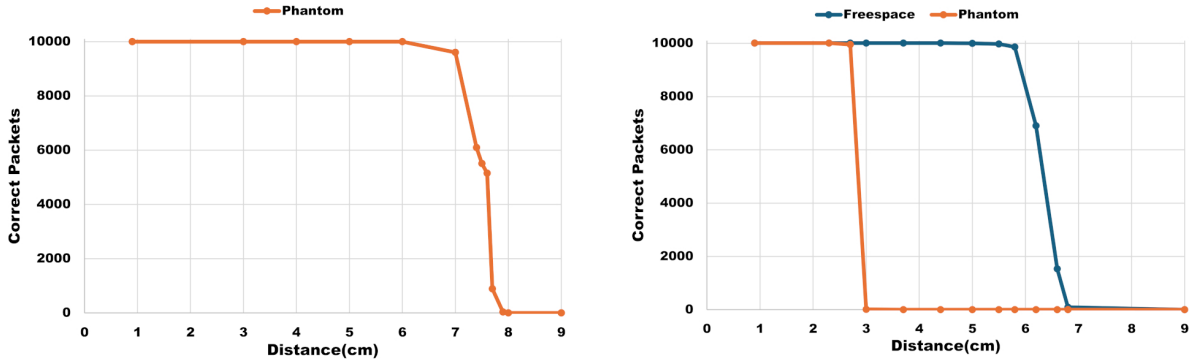
5.6.2 Packet Loss Test

To test the end-to-end performance of the communication link, a fixed 14-byte packet was sent thousands of times at different distances: 0xC0, 0x00, 0x10, 0x10, 0x32, 0x54, 0x76,

Figure 5.24: IrLAP information frame reliably transmitted at 2Mbps.

0x98, 0xBA, 0xDC, 0xFE 0x79, 0xBD, 0xC1. This sequence is an IrLAP I-frame. The first byte is the BOF character. The next two bytes are the address and control bytes, which are then followed by the 8-byte payload: 0x10, 0x32, 0x54, 0x76, 0x98, 0xBA, 0xDC, 0xFE. The final three bytes are the 16-bit CRC and EOF characters. For the downlink and uplink evaluation, the fixed packet was transferred 10000 and 10010 times, respectively. The downlink bitrate was held constant at 115.2 kbps, while the uplink bitrate was set at 2 Mbps. The IrLAP layer of both devices was modified to repeatedly send information frames or count and verify received packets. Because the downlink functioned with separation distances over 10 cm in free space, only a phantom was used to evaluate packet loss. The downlink phantom comprised an IR opaque board with a hole covered by a 0.8 mm thick sapphire crystal and 4 mm of deli sliced ham. The uplink was evaluated through free-space, and through a phantom, defined here as 0.8 mm sapphire and 3 mm of porcine tissue (raw pork chop). The results are shown in fig. 5.25.

Although the abdominal height of a rat is highly variable, the expected distance from the BS-AFE is 2 cm. With the inclusion of skin and the enclosure, the nominal distance from IR LED to IR photodiode is 2.3 cm, assuming the rat is on all four legs. The implant coil and BS-AFE coil were aligned co-axially, thereby orienting the implant LED and BS-AFE



(a) Downlink at 115 kbps.

(b) Uplink at 2 Mbps.

Figure 5.25: Error-free packets received as a function of distance.

photodiode for optimal transmission. As is apparent in subplot (a), the downlink PLR for a sample of 10000 transmitted packets remained at 0% out to a separation distance of 6 cm, far exceeding the nominal use case. For the uplink, shown in subplot (b), the resulting PLR through the phantom was 0% for a sample of 10010 transmitted packets up to 2.3 cm. At 2.7 cm, through the phantom, the uplink PLR was 0.54%.

5.6.3 Implant Power Dissipation

While the base-station power dissipation was not a design priority, the implant device operated on a constrained energy budget. The entire implant RX system, which includes all amplifiers and RSSI circuitry, consumed 1.4 mA while receiving data at 115.2 kbps. Therefore, the dynamic power consumption is 3.5 mW. The TX system, on the other hand, dissipated 46.2 mW of power while transmitting data at 2 Mbps. Given that the MIC23030 operates at nearly 55% efficiency, which is responsible for stepping 5 V down to 1 V, this leaves considerable room for improvement.

Chapter 6

POWER & ENERGY STORAGE MANAGEMENT

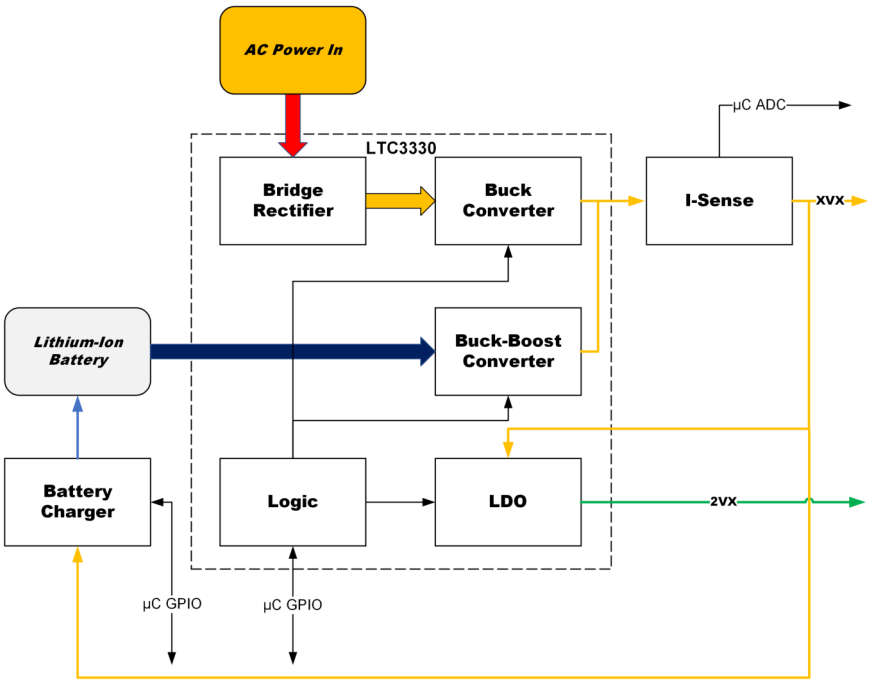


Figure 6.1: Power & battery management overview.

One of the challenges of designing a system with multiple distinctive states of operation, while satisfying the design constraints, is providing appropriate and efficient power to a variety of devices. Charging the lithium-ion battery, for example, requires special charging and discharging management. In chapter 3, a charge pump was required for the RHS2116 IC. The IR communications TX circuitry, discussed in chapter 5, used a buck converter to provide a 1 V supply. Indeed, this design could be simplified by setting the XVX rail to a constant 5 V. However, doing so would result in a considerable amount of wasted energy

while charging the battery.

In short, this section covers the high-level power-distribution and energy-storage circuitry of the implant device, while discussions relating to wireless power will be presented in chapter 7. Of course, there is overlap between the circuitry discussed in this chapter and in chapter 7. In fact, the LTC3330 power-management IC (PMIC) integrates features that span both chapters. However, the details of the wireless-power system require an entire dedicated section.

A block diagram showing the different components of the power and battery management sub-systems is shown in fig. 6.1. The "AC Power In" block represents the flow of wireless power into the system. Thick colored lines represent unregulated power flow, while thin colored lines represent regulated flow. Depending on the availability of wireless power, the LTC3330 will select between the buck and buck-boost converter automatically. When wireless power is present, the buck-converter will supply the XVX rail, which supplies the low-dropout (LDO) linear regulator for the 2VX rail, as well as the battery charger. When wireless power is not available, energy is sourced from the lithium-ion battery. The battery supplies the buck-boost converter, which then supplies XVX and the LDO regulator. The "I-sense" block is a current-sense amplifier, which is monitored by the microcontroller. Similarly, the microcontroller also interfaces with the LTC3330 and the battery charger for supervision purposes.

6.1 Dynamic Voltage Rails

The ability to alter voltage rails during runtime was successfully implemented in our earlier work [75]. Nominal voltage levels for expected states are shown in table 6.1. While the primary energy-harvesting PMIC, the LTC3330, can provide an XVX less than 3.3 V, this system is presently hardwired to limit the minimum voltage to 3.3 V. During IR communication, setting XVX to 5V is based on the IR TX system. At the expense of lower performance, lower XVX values may suffice. An XVX of 5 V is required for the neural IFC PMIC responsible for providing stimulation voltage levels. 2VX levels shown are

Table 6.1: Dynamic Voltage-Rail States

STATE	**XVX(V)**	**2VX(V)**
Default	3.3	2.5
Battery Charge	3.3	2.5
IR Communication	5.0	2.5
Neural Rec/Stim	5.0	2.5
Sleep	3.3	2.0

normally set to 2.5 V. Because 2VX is supplied from XVX via a linear regulator, reduction in voltage may not yield significant reduction in power dissipation. Also, the MSP430FR5994 microcontroller used in the implant is specified down to 1.8 V. While the 2VX may be switched to 1.8 V, a drop below this level could result in the MSP430 entering a brown-out condition and losing RAM memory contents. Therefore, 2.0 V is the suggested minimum.

6.2 Energy Storage Device

Recording neural data for up to six minutes significantly impacted system design. Analysis, based on device datasheets and on bench-top measured performance, placed the energy requirement for six minutes at roughly 20 to 30 J. Two classes of available energy storage devices are immediately apparent: electric double-layer capacitors (supercapacitors) and batteries. To mitigate battery maintenance concerns for long-term implantable devices, primary batteries were eliminated from the candidate list.

However, the availability for COTS energy storage devices with requisite energy density, charge/discharge rates, nominal voltage level, acceptable leakage current and small size are minimal. For example, thin-film lithium batteries boast excellent energy density and are produced in small form factor, but ESR is often too large and max discharge rates are well below what is required. COTS lithium-ion polymer batteries in small-form factor provide

excellent energy densities, well into the 100s of $\frac{Wh}{L}$, and can deliver more than adequate charge and discharge rates. Lithium-ion batteries, while the standard for almost all consumer devices, are known for catastrophic failure due to thermal runaway [31,55]. When a lithium-ion battery is subjected to electrical, mechanical, or thermal abuse, thermal runaway results in combustion and even explosion. While mechanical damage, which is much more likely to occur in vehicles, etc., is unlikely with an implant, an electrical short-circuit is a plausible scenario.

While supercapacitors are plentiful, those that are appropriate for this implantable device are virtually non-existent. Indeed, charge and discharge rates can be quite excellent; however, supercapacitors lack the necessary energy density to meet the demands of this application. Those supercapacitors that do meet the form-factor constraints typically suffer from leakage and high effective series resistance (ESR). The optogenetic stimulation implant, "lollipop", employed the Murata DMF series supercapacitor. The 470 mF, 5.5 V variant was selected for the design. With a low ESR of 45 mΩ (at 1 kHz) this supercapacitor could charge and discharge well above any rate that would ever be required by our device. Leakage current is specified at 5 uA (over 96 h). Charging and discharging of these supercapacitors is flexible and straightforward: No special charging circuitry is required. There is no concern of damage due to complete discharge or incorrect discharge. However, with an energy capacity of 5.9 J, this device, as well as other similar supercapacitors, are clearly incapable of supporting necessary energy demands.

The GSK BIC device used a Vishay 196 HVC ENYCAP series supercapacitor. These supercapacitors are marketed as a type of "hybrid" since charge storage is obtained both electrostatically and electrochemically. The great majority of the capacitors in this series are too large, but a handful are appropriate in size. The best fit with the highest energy capacity was the MAL219691154E3. It is rated at 4 F at 5.6 V and comprises four cells at a size of 14.0 mm x 14.0 mm x 2.5 mm. The design of this supercapacitor limits it lowest discharge voltage to 3.2 V. Given that our main power management IC has a max voltage of 5.0 V, this limits the usable energy to about 29.5 J, which meets initial projected energy demands. However,

the 196 HVC ENYCAPs have relatively high ESR and leakage rates: 10.0 Ω at 1 kHz and 30.0 Ω at DC, with a leakage of 30 uA over 24 hours. Furthermore, the max discharge current is rated at 25 mA and the max charge current at 14 mA. Recommended charging currents are specified from 2 to 8 mA. Furthermore, these capacitors have a minimum discharge voltage of 3.2 V, thereby requiring additional circuitry.

Clearly, the only feasible energy storage device is a lithium-ion battery. While usage of these batteries requires cognizance of potential hazards, lithium-ion batteries for implantable medical devices is a viable strategy. In fact, lithium-based batteries have been used in medical devices for decades, and rechargeable lithium-ion batteries may be found in ingestible and implantable medical devices [90]. There are various mechanisms for improving lithium-ion battery safety. In 2016 Murata released so-called "Small Energy Devices", which comprised the UMAC and UMAL series. These devices are a type of lithium-ion battery; however, their performance incorporates some supercapacitor characteristics, making them more robust and safer than traditional lithium-ion batteries but with superior energy density compared to supercapacitors. These batteries mitigate thermal runaway, and although not recommended, can survive a complete discharge. The technology is based on the new manufacturing trend of using alternate materials for the electrodes: lithium titanate for the cathode and lithium cobalt oxide for the anode. The trade-off, compared to traditional lithium-ion batteries, like those used in cells phones, is a lower energy density.

The UMAC (UMAC040130A003TA01) is provided in a cylindrical can, like electrolytic capacitors. The UMAC is presently available in one configuration: 4 mm diameter by 12 mm length, with a capacity of 3 mAh at a nominal voltage of 2.3 V. This is equivalent to approximately 10 F or 20.3 J. The energy density is therefore 37.3 $\frac{Wh}{L}$. The ESR is rated at 800 mΩ.

The UMAL (UMAL361421B024TA01), on the other hand, is produced in a form factor almost identical to the Murata DMF and DMT series supercapacitors with a size of 21 mm x 14 mm x 3.6 mm. It has an ESR of 100 mΩ, capacity of 24 mAh at a nominal 2.3 V and a max charge/discharge current of 240 mA. For this battery, 24 mAh is equivalent

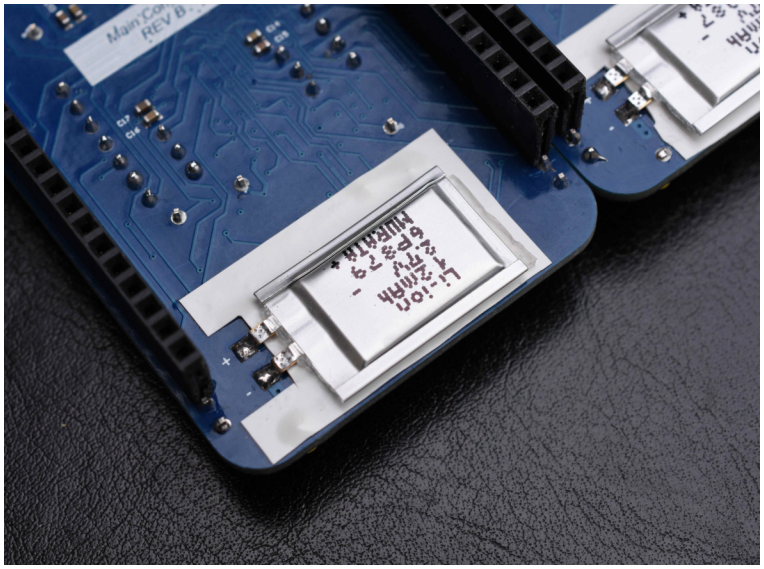


Figure 6.2: UMAL lithium-ion battery installed on macro-scale PCB.

to a supercapacitor of approximately 100 F. Indeed, analysis of the discharge curves, per the datasheet, show that for a constant discharge of 24 mA, the UMAL can run for over 60 minutes before reaching its minimum voltage of 1.8 V. Integrating this curve showed a usable energy capacity of 213.8 J. Equating this to a capacitor produces 105.6 F, with an energy density of 56.1 $\frac{Wh}{L}$, which is 32 times higher than the 474 mF supercapacitor and 25 times higher than the 4 F supercapacitor.

Murata also produced the UMAL201421A012TA01 and UMAL201421A012TA02, which is the previous generation of the UMAL device discussed above. It has an ESR of 200 mΩ, a capacity of 12 mAh, and a maximum charge/discharge rate of 120 mA. Dimensionally, it is thinner than the 24 mAh version at 21.0 mm x 14.0 mm x 2.0 mm. However, its thinner dimensions result in a 56% reduction in volume, which is critical for device miniaturization. Derived from multiple datasheets [65–67], fig. 6.3 shows energy discharge of all three devices at different current levels.

While both UMAL devices could be used for this design, the 12 mAh version was selected since it was thinner and provides sufficient power for expected operation. The battery is

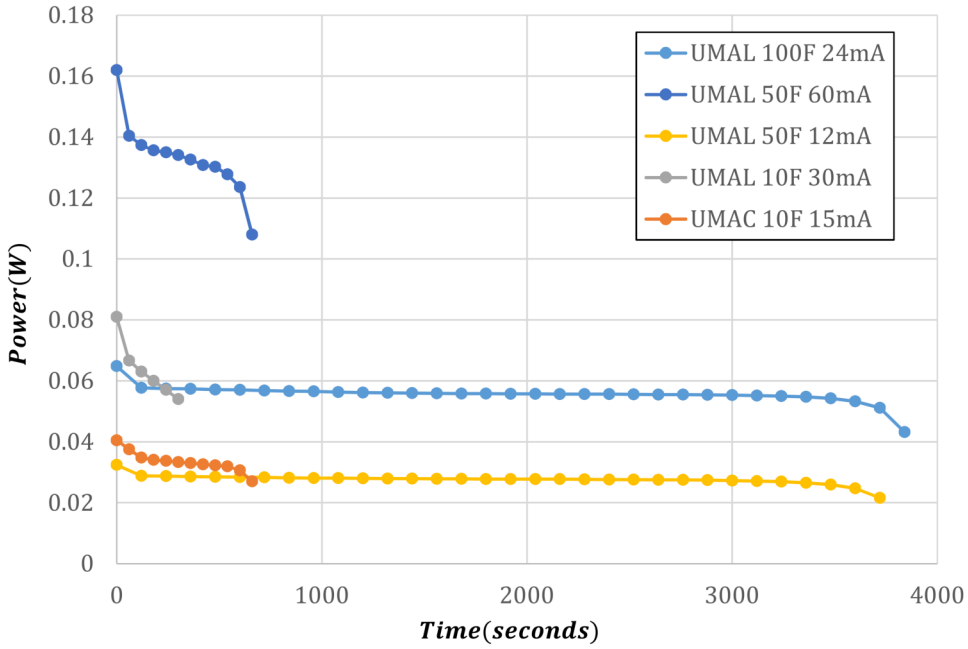


Figure 6.3: UMAL Small-energy device discharge curves.

shown in fig. 6.2 where it is installed on the macro-scale IMP-SC PCB. At this time, Murata no longer manufactures this battery, and no direct substitutes have been identified.

6.3 Battery Charge Management

While the LTC3330 is responsible for discharging the lithium-ion battery into the integrated buck-boost converter, battery charging must be handled by external circuitry. Indeed, there are numerous options available for charging lithium-ion batteries; however, the unique battery chemistry of the UMAL devices makes them incompatible with most battery charging ICs. Ideally, a high-efficiency buck-converter style battery charger could be incorporated into this design. However, none were identified that were appropriate for this application.

The only IC that met the design specifications was a multi-chemistry linear charger: LTC4079. This battery charger IC can operate down to an input voltage of 2.7 V, and charge a battery with a nominal voltage of 1.2 V. One benefit of this IC is that the charging

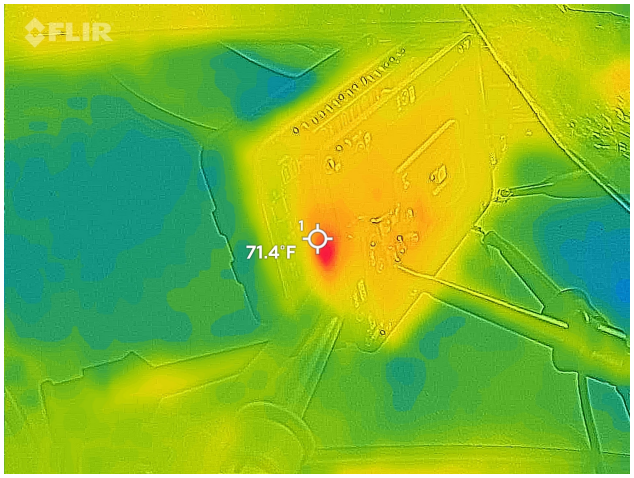


Figure 6.4: During battery charging, heating was minimal at the 47.4 mA rate.

maximum current can be set by a single resistor. To support different states of wireless power transfer, MSP430 GPIOs are used to switch between two charge levels: 12.28 mA and 47.4 mA. During battery charging the LTC3330 XVX rail is switched down to 3.3 V to maximize efficiency, thereby requiring about 41 mW of delivered wireless power. At 47.4 mA, the power jumps to 156 mW. As shown in fig. 6.4, no significant heating was observed on the linear charger IC at the 47.4 mA charge rate. With the maximum current set at 47.4 mA, a full recharge takes approximately 15 minutes. By adjusting associated resistors, the charge levels can be changed to any arbitrary level.

6.4 Battery Discharge Management

The LTC3330, by design, manages battery discharge. One of the primary functions of the LTC3330 is to power a buck-boost converter from a battery when energy harvesting is not available. Given that the battery voltage is always less than that provided to the XVX rail, the buck-boost converter is always in the boost state. When battery voltage drops below 1.8 V, the internal logic of the LTC3330 terminates the buck-boost converter operation, thereby preventing over-discharge damage.

Because wireless power is not the expected energy source during a neural-recording operation, the battery must provide sufficient power for the Intan RHS2116 circuitry, NVM bank, and microcontroller unit. As stated in chapter 3, the ideal power consumption is 83.60 mW, which was measured directly with 5.0 V and 2.5 V power supplies. Because the buck-boost converter must step-up the constantly depleting battery voltage, battery output current is not constant, nor is the efficiency. Per the datasheet, the LTC3330 will experience a reduction in efficiency of about 15% as the battery reduces from 2.3 V to 1.8 V.

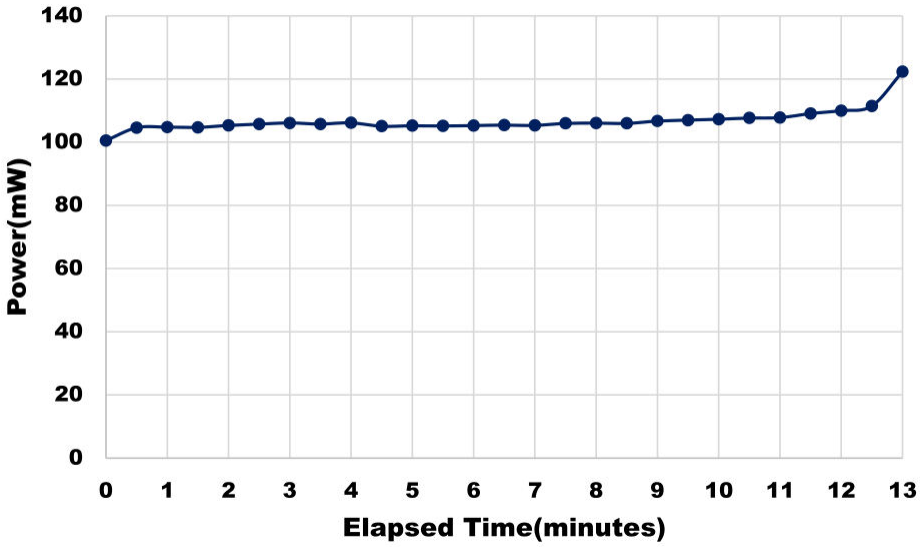


Figure 6.5: Battery power delivery while neural recording operation in progress.

To characterize the behavior of the power system during a neural-recording experiment, the Intan RHS2116 sampled continuously as the data was programmed into the NVM flash memory. Beginning with a fully-charged battery, the neural recording continued until the battery voltage reduced below the LTC3330 1.8 V threshold. As was discussed in chapter 3, one channel was sampled at 26 $\frac{ks}{s}$. All NVM ICs were initialized and idle, not in any sleep mode. The results are summarized in fig. 6.5. The implant was able to sustain this recording operation for 13 minutes before the LTC3330 cut out the buck-boost converter, causing a

system reset. The characteristic lithium-ion discharge curve is evident in the plot. With a fully-charged battery, the power delivered was approximately 100 mW. Near the nominal voltage, power remained relatively constant at around 105 mW for about eight minutes, before peaking at 122 mW, which occurred immediately before the buck-boost converter cut out. Clearly, sustaining neural recording for six minutes is achievable. During the 13-minute experiment, 83 J of energy was transferred to the LTC3330.

On the other end of the power-dissipation spectrum, the implant device was set to its lowest power state. All unused circuitry was switched off, put into sleep mode, etc. The XVX rail was set to 3.3 V. Finally, the MSP430FR5994 was placed into sleep mode with RAM retention (LPM 3). Beginning with a fully charged battery, the system remained in this state for approximately 17 hours before the battery was depleted. These results demonstrate that the implant system may be charged and retain sufficient energy for a neural recording session while placed into the low power sleep mode.

Chapter 7

WIRELESS POWER SYSTEM

The wireless power system, arguably the most critical component, must be designed around all other aspects of the system. The TX and RX inductors are the starting point for adaptation to any practical design. Because this device is a medical implant, the RX coil is obviously the most constrained in the system given the dimensions of the enclosure internal cavity: a rounded rectangle with a width of 17.2 mm and a length of 25.2 mm. Scaling down wireless-power coils degrades Q due to the physical consequences of the coil geometry. Also, the nature of power electronics engineering, in general, places heavy focus on the tradeoffs of footprint reduction versus efficiency. Furthermore, the RX coil in this design resides inside the enclosure in close proximity to all other circuitry.

Previous research and experience suggested that a 3-coil wireless-power system should be used instead of the more familiar 4-coil system that we have used in various applications. While 4-coil systems have been demonstrated to provide excellent performance, the design becomes significantly more complicated when building a loop-coil system in such a confined space. Furthermore, 3-coil systems can attain the high-efficiencies of 4-coil systems but are better equipped to deliver more load power at longer distances [45]. Also, 3-coil systems tested in [30] tended to provide a flatter efficiency response as the coupling k_{23} was swept from tightly to loosely coupled at a constant frequency.

Earlier work referenced in this dissertation leveraged a well-proven and reliable hardware solution for the TX part of the system. The TX system comprises a single-ended class-E power amplifier (PA), which utilizes a direct digital synthesizer for signal generation. This system has experienced several revisions and is available commercially from WiBotic. Furthermore, the Sensor System Lab has many previously designed and reliable coils spanning

a relatively large range of geometries.

The latter work includes a compact linear wireless-power TX module (BS-LWPM) that resides within the BS-M enclosure. While an extensive analysis of PA design is outside the scope of this work, a simple PA was integrated to not only test form-factor feasibility but investigate inter-device interference.

7.1 Coil Design

Miniaturization of the wireless-power RX coil is extremely challenging, given the diminished operating range and Q of coils as they scale down. Additionally, the range of practical, efficient wireless-power transfer via magnetic near-field coupling is roughly 1.5x to about 2.5x the diameter of the coils. In [91], for example, an RX coil was integrated into the upper metal layers of an IC that measured approximately 2 mm x 2 mm, and at a separation distance of 10 mm in air, an efficiency of 1.8% was achieved. Complicating matters, these small form-factor coils become difficult to model using traditional methods, which are normally suitable for larger coils.

Mostly due to the "mass-production" emphasis of the GSK BIC, hand-wound coils for this implantable device seemed impractical, not to mention inconsistent. Therefore, researching and designing with PCB coils quickly became a viable alternative. PCB coil design, especially small coils, parallels many of the same design methods utilized by IC designers. While experience exists in this field of study, the available literature for PCB coil design is less than desirable. Available information provides general design concepts and often provides rough approximations or empirically derived results, relevant to a particular form factor. Literature on 20 mm or less diameter coils for wireless power are limited, and even scarcer for multi-layer PCB coils.

The first PCB coil for the GSK Challenge project, designed for the optogenetic stimulation platform, utilized an online PCB coil design tool for inductive sensing [33]. Given time constraints, a coil was optimized via general coil design guidelines. Given that the outside diameter of the coil was set at roughly 20 mm and a "quick-turn" four-layer PCB was to be

fabricated, other parameters were adjusted intuitively until the estimated Q was maximized and the calculated self-resonant frequency (SRF) was as high as possible. Naturally, the adjustments were a tradeoff between inductor turns, trace width and trace spacing. The final coil had an outside diameter of 21 mm with four turns. The trace width was approximately 40 mil while the trace spacing was 10 mil. The fabricated PCB coil performed remarkably well, but lacked the solid theoretical modeling required for optimization.

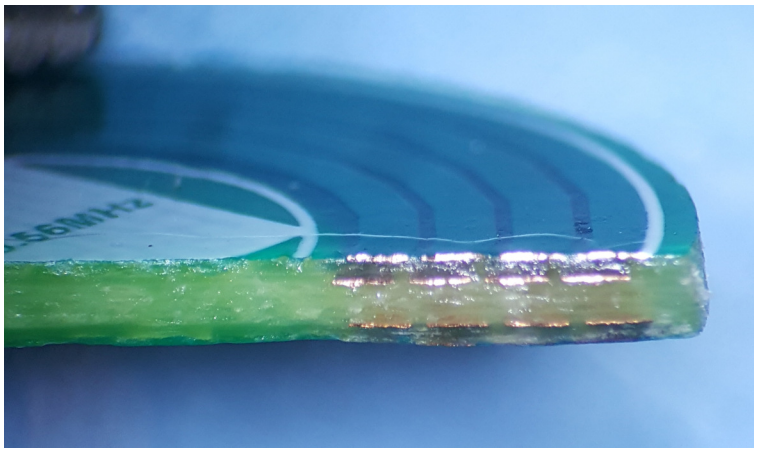


Figure 7.1: A cross-section of the "lollipop" PCB multi-layer coil. Copper layers show significant overlap, which contributes to the parasitic capacitances.

A cross-section of the designed coil is shown in fig. 7.1. Of particular importance is the non-uniform distance between copper layers. The FR-4 core is much thicker than the prepreg layers. Due to the limitations of the online software, copper layers 1 and 2 have significant overlap, which increases parasitic capacitances and lowers SRF.

To further investigate and develop a theoretical model for sub 20 mm diameter coils, a PCB containing 20 coils with varying turns and trace spacing was designed via the online creator tool, completed in Altium, and fabricated by Sunstone Circuits.

As before, the PCB used standard FR-4 with four 1 oz copper layers. Core thickness was 28.0 mil and prepreg layer thickness was 11.9 mil. Each of the 20 coils was designed to maintain an outer diameter as close to 20 mm as possible with 40 mil trace widths, while

varying the number of turns and trace spacing. Five groups of coils were designed with 2, 3, 4, 5 and 6 turns. Each group stepped through trace spacing of 6, 8, 10 and 12 mil. The PCB was v-scored and provided a pad on each coil for a tuning capacitor and a standard SMA connector. The PCB is shown in fig. 7.2.

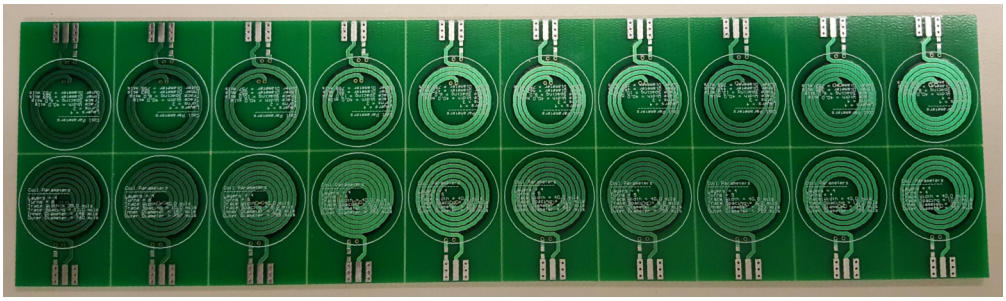


Figure 7.2: A v-scored PCB with 20 multi-layer PCB coils. Each has an outer diameter of approximately 20 mm with variable turns and trace spacing.

Each of the 20 coils was populated with a 0Ω resistor and characterized on a VNA. A 1600-point frequency sweep was conducted from 500 kHz to 50 MHz. S-parameters were converted to impedances and analyzed for resistance, reactance, Q and SRF.

Not surprisingly, the 6-turn PCB coils with 6 mil spacing exhibited the worst performance. The SRF was 23.1 MHz with a Q of 19.1 at 13.52 MHz. All of the 2-turn coils performed well with Q values ranging from 74.2 to 78.3. The SRF for each of the coils was larger than 50 MHz. Interestingly, the coil with the highest Q had the smallest trace spacing of the group at 6 mil. The results are summarized in fig. 7.3.

While later work incorporated custom PCB inductors for the TX and RX systems, all referenced early work was conducted with hand-wound loop-coils. Early work on implantable devices in the Sensor Systems Lab focused almost exclusively on the RX coil given the maturity of our TX systems. The TX loop and coil were well-characterized and performed exceptionally well in similar applications. The TX loop-coil used throughout the initial work is described in [84], and the parameters of the coil are reprinted here for convenience in 7.1.

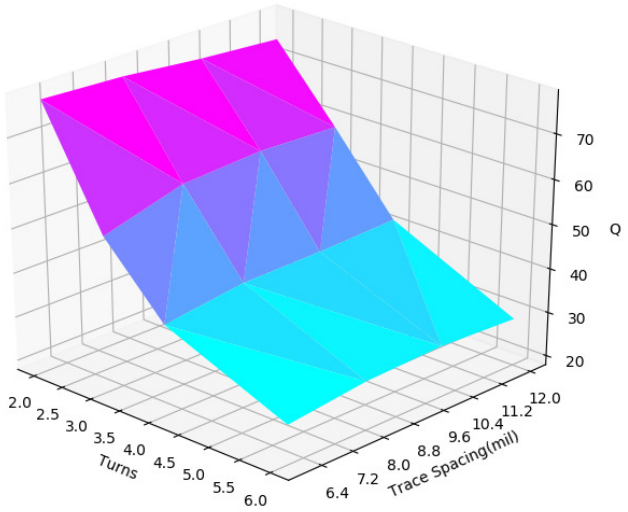


Figure 7.3: PCB Coil Q derived from VNA measurements: This plot reveals the effect of parasitic capacitance and SRF on coil Q.

Table 7.1: TX Coil Parameters

Parameter	**Value**
Outer Diameter (cm)	6.5
Wire Material	Copper
Wire Size (AWG)	18
$L_{loop}\,(\mu H)$	0.3
$L_{coil}\,(\mu H)$	4.86
$C_{loop}\,(pF)$	423.8
$C_{Coil}\,(pF)$	42.6
Q_{loop}	16.5
Q_{coil}	308.3

7.1.1 PCB Coil Modeling and Appliqué

Accurate modeling of PCB-based coils, especially those used in this project, is not a trivial process. Following coil characterization, an accurate theoretical model was sought to verify the experimental findings. First, the measured parameters of each coil were compared to the estimated values given in the online coil designer. Given that this design was outside the scope of this design tool, the results in general were not accurate. For the coil with 2 turns and 6 mil spacing, the online tool calculated the inductance at 0.57 μH and a Q of 159.3. As stated above, the actual Q was approximately 78.3 and the extracted inductance, measured at 500 kHz, was about 1.6 μH, nearly 3 times larger! The extracted inductance of each of the coils deviated with a percent difference of about 30 to 60%.

Other methods were also explored, such as modeling the inductances as layers of concentric loops. Formulas such as those in [89], [64] and [25] were applied and modified where necessary for the particular geometry of the small PCB coils. None of these methods provided accurate results.

[93] provided a thorough and practical discussion, with empirically derived formulas, specifically for multi-layer PCB coils in the range of a few μH. Unfortunately, these results also showed unacceptable inaccuracy, which may be the result of the number of turns ranging from 5 to 20 in [93].

Literature was also surveyed for accurate theoretical modeling for multi-layer PCBs. On first glance, the work presented in [35] appeared to provide insight into modeling small multi-layer PCB coils for wireless power. The paper was well-written and insightful, and attempted to generalize multi-layer PCB coils into a simple π model. Although a generalized equation was presented, there was no information on how to calculate the coupling coefficient $k = \frac{M}{\sqrt{L_1 L2}}$, which renders the equation useless for my application.

Because of the lack of relative literature, research was directed at not only developing an accurate model, but also determining why other methods had failed. Returning to the source, Maxwell's equations, and basic electromagnetic theory, revealed the problem. In most cases,

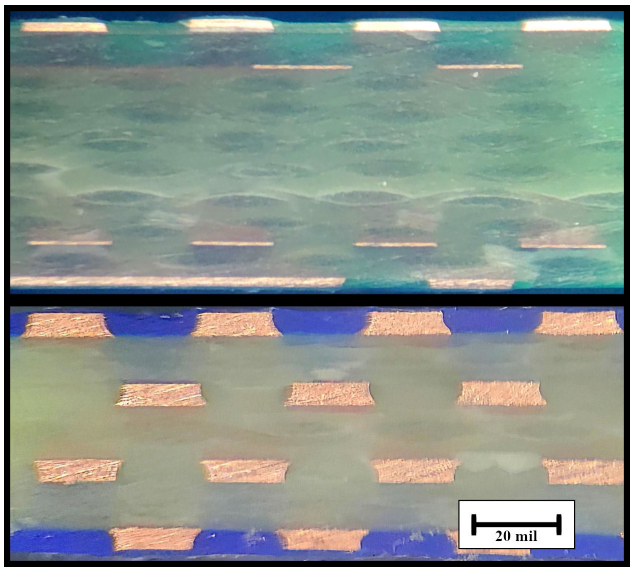
the inaccuracies can be attributed to user error. In other words, the majority of available equations for inductance are based on simple and large geometries where the radius of the conductor can be reasonably approximated as a theoretical current filament. Therefore, these formulas are not necessarily inaccurate, but they are often used without consideration of how the formula was derived. Even the Neumann formula, shown in eq. (7.1) for convenience, will produce inaccurate results when the conductor cannot be approximated as a filament. Obviously, in the case of small multi-layer PCB coils, it cannot be accurately modeled by a single current filament.

$$M_{12} = \frac{\mu_0}{4\pi} \oint_{C2} \oint_{C1} \frac{d\mathbf{l_1} \cdot d\mathbf{l_2}}{\mathbf{r}} \tag{7.1}$$

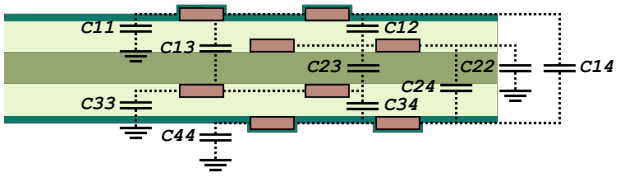
Indeed, the obvious solution is a full 3-D EM simulation tool. It is undoubtedly the most accurate and complete tool for correctly analyzing multi-layer printed inductors. However, a more intuitive lumped-element modeling process was desired, especially one that was free. Additionally, the ability to export models directly to PCB CAD software like Altium Designer or Ki-CAD was also important. The quest ultimately led to the creation of an entire printed inductor modeling methodology automated in a Python-based graphical user interface (GUI): Appliqué [57]. Appliqué is an acronym for "Automated Planar Printed Layered Inductor Quasi-static Unified Evaluator". Appliqué is more accurately described as a GUI wrapper in that it interfaces with other applications to develop an accurate model for printed inductors. As shown below, the lumped-element model is able to predict printed inductor behavior in SPICE simulation given accurate inductance and capacitance extraction.

For example, consider four-layer PCB inductors, which could be used in a wireless power transfer system, like those shown in fig. 7.4 (a). While the traces of the PCB form the desired inductance, significant capacitance is formed between the traces, resulting in self-resonance. If the self-resonant frequency (SRF) is near the operating frequency of the wireless power coil, the performance is severely degraded. Additional factors that further degrade the coil Q include parasitic DC and AC resistances.

The proposed lumped-element model for a printed inductor is most readily conveyed in

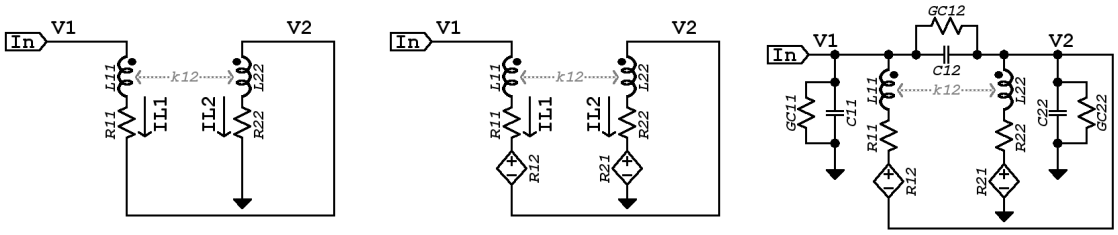


(a) Four-layer PCB spiral inductor for wireless power.



(b) A graphical representation showing parasitic capacitance.

Figure 7.4: Modeling of the parasitic capacitances in a four-layer printed inductor.



(a) Inductance (b) AC Resistance (c) Parasitic Capacitance

Figure 7.5: Modeling a 2-layer PCB inductor.

a visual manner. First, consider a two-layer printed inductor. A basic schematic diagram is shown at the left-hand side of fig. 7.5 in part (a). However, tightly-wound inductors must also consider proximity effect, and those operating at higher frequencies must include skin effect. The middle schematic models these AC resistances as dependent voltage sources. The final figure shows the inclusion of parasitic capacitance forming a more accurate representation of the printed inductor behavior.

Extending the model to four layers would, therefore, take the form of that shown in fig. 7.6. It is apparent that the four-layer model is far more complex than the two-layer version, thereby making hand-analysis intractable. Extending the model to an n-layer PCB follows the pattern of a complete graph where n is the number of nodes or vertices. The model is shown schematically in fig. 7.7. Using nodal analysis the resulting equations are eq. (7.2) and eq. (7.3).

$$\begin{aligned} I_n = V_n \left[\sum_{i=1}^{n} \left(Y_{Cn,i} \right) + Y_{Ln,i} \right] \\ - \sum_{\substack{i=1 \\ i \neq n}}^{n} \left[V_i \left(Y_{Cn,i} \right) + Y_{Ln,i} \left(I_{Li} \cdot Z_{n,i} \right) \right] \end{aligned} \tag{7.2}$$

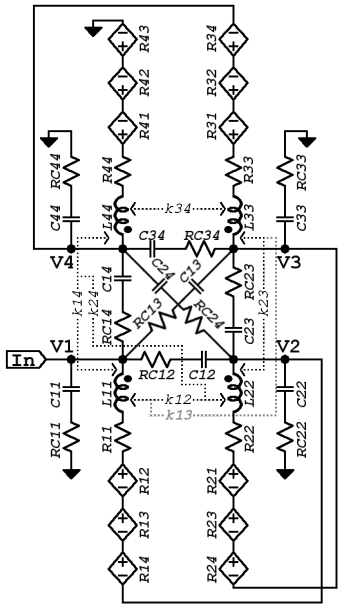


Figure 7.6: Schematic model of a four-layer PCB printed inductor.

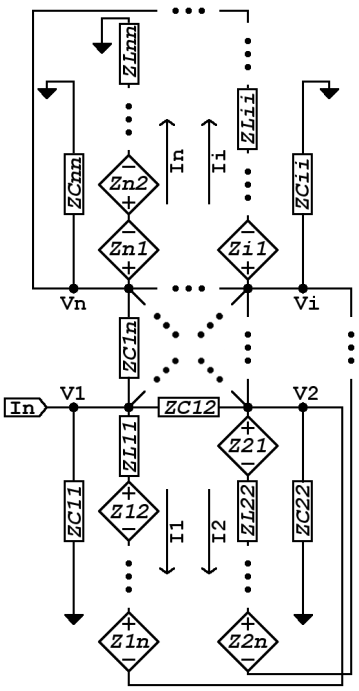


Figure 7.7: Generalized n-layer PCB inductor model.

$$
\begin{aligned}
Z_{n,i} &= R_{n,i} + s \cdot L_{n,i} \\
Y_{Ln,i} &= \frac{1}{s \cdot L_n + R_n} \\
Y_{Cn,i} &= G_{Cn,i} + s \cdot C_{n,i}
\end{aligned}
\tag{7.3}
$$

While not a complete model, it is interesting to note that when capacitance may be considered negligible, the Z-parameter matrix simply collapses to the sum of all Z-parameter elements. Therefore, the total inductance is eq. (7.4) and the total resistance is eq. (7.5).

$$
L_{total} = \frac{\mathbb{I}\mathrm{m}\left[\sum_{i=1}^{n}\sum_{j=1}^{n} Z_{i,j}\right]}{\omega} = \sum_{i=1}^{n}\sum_{j=1}^{n} L_{i,j} \tag{7.4}
$$

$$
R_{total} = \mathbb{R}\mathrm{e}\left[\sum_{i=1}^{n}\sum_{j=1}^{n} Z_{i,j}\right] = \sum_{i=1}^{n}\sum_{j=1}^{n} R_{i,j} \tag{7.5}
$$

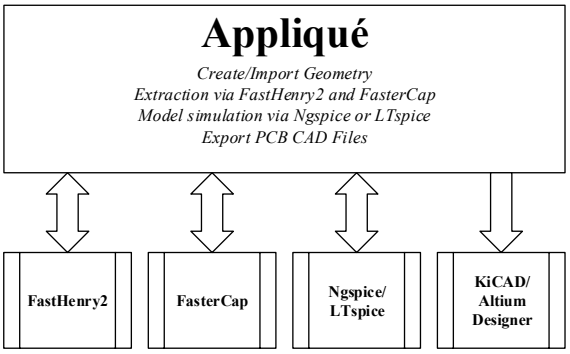


Figure 7.8: High-level diagram of Appliqué functionality.

With an underlying lumped-element model defined, the basic functionality of Appliqué is introduced in fig. 7.8. Like SPICE GUI front ends, Appliqué interfaces with multiple programs using text-based input and output files. In short, a PCB inductor is designed in a GUI, which can then be modeled using extracted lumped-element parameters simulated in

SPICE, and finally exported to PCB CAD software. A screen shot of the GUI is shown in fig. 7.9. The python-based graphics are powered by Mayavi [74]. While SPICE is more familiar, two underlying applications provide the extracted inductance and capacitance parameters.

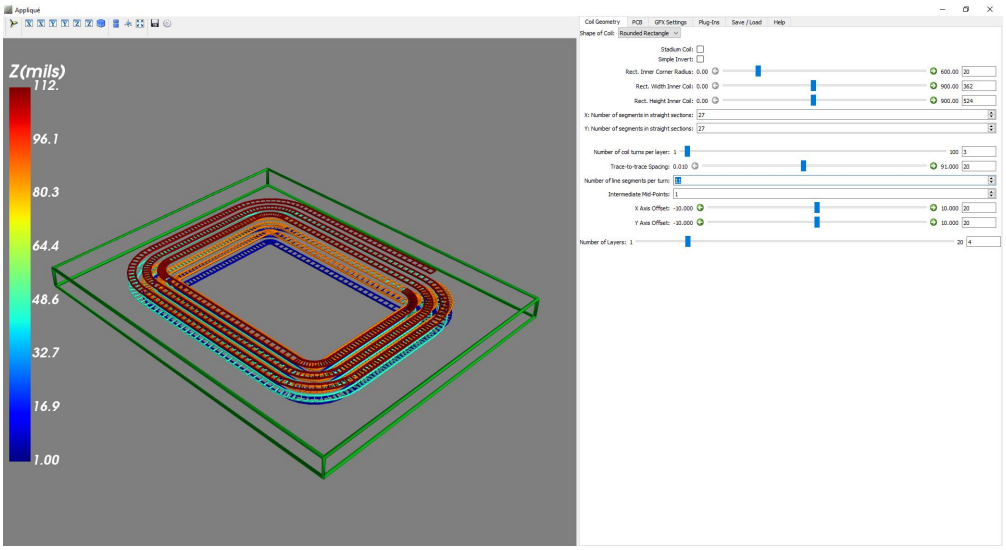


Figure 7.9: Appliqué GUI: Intuitive design environment for PCB coils.

In the 1990s, software was created that leverages a multi-filament solution for inductance modeling given quasi-magnetostatic conditions: FastHenry [41]. FastHenry is still available as open source for Linux distributions; however, it has since been ported to Windows. Both versions have been used; however, Appliqué builds upon the more recent FastHenry2 Windows port [20]. FastHenry is simple to use but requires 3-D geometries to be constructed as a series of parallelepipeds or "bricks". To operate FastHenry, a user generates a text-based description of the brick segments. The data is simply a series of connected line segments with a specified width and height. To improve accuracy for high-frequency effects, such as skin-effect, the brick segments can be further discretized to ensure a representative placement of current filaments, at the expense of longer computation times. After FastHenry analyzes the input file, z-parameters are returned in matrix format for each specified frequency. The

impedances contain the reactances due to self and mutual inductances and the resistances due to various parasitics. Since conductance and frequency are both specified, FastHenry calculates DC resistances as well as AC effects including skin and proximity effects.

Similar to FastHenry, FastCap is a capacitance extraction tool also developed in the 1990s [68]. The input files to run FastCap simulations are considerably different, and more complicated than the FastHenry version. Where FastHenry uses line-segments, FastCap uses panels to define the structure. Furthermore, all bounding dielectrics must also be specified. Because of this, FastCap files can be much more complex than the FastHenry file for the same geometry. FastCap allows the usage of a "LST" file where common geometry files (QUI) can be referenced and translated to generate complex structures. Like FastHenry, FastCap is still available as open-source for Linux, and has been ported to Windows. A more recent version, called FasterCap [19] is reportedly more efficient and accurate in particular configurations. Appliqué interfaces with the more recent FasterCap for capacitance extraction. The FasterCap output is somewhat similar in that it returns a matrix, but instead of a z-parameter impedance matrix, FasterCap returns a Maxwell Capacitance matrix [16], shown in eq. (7.6).

$$\mathbf{Q} = \mathbf{CV}$$

$$\mathbf{C} = \begin{bmatrix} C_{11} + C_{12} + \cdots + C_{1n} & -C_{12} & \dots & -C_{1n} \\ -C_{21} & C_{21} + C_{22} + \cdots + C_{2n} & \dots & -C_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{n1} & -C_{n2} & \dots & C_{n1} + C_{n2} + \cdots + C_{nn} \end{bmatrix} \quad (7.6)$$

$$\mathbf{V} = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix}$$

As is apparent in eq. (7.6), the matrix $\mathbf{C}$ is the ratio of the charge on a set of conductors

to the voltage between them. In the case of a multi-layer PCB coil, considering each layer as an isolated conductor, mutual capacitances would exist between each layer. Additionally, each conductor would also have self or auto capacitance to "ground". It is important to note that the capacitances are returned in a complex format if electrical permittivity is known. The complex format includes a frequency-dependent dielectric loss, modeled as a shunt conductance in parallel with a parasitic capacitance. The resulting complex elements of the matrix are, therefore, more accurately expressed as an admittance, as shown in eq. (7.7).

$$\frac{Y}{j\omega} = C - j\frac{G}{\omega} \tag{7.7}$$

Although many variations of SPICE have existed for decades, the theme of providing these tools using common free and open-source software helped limit the choices down to LTSPICE and ngSPICE. The former is not open source but is a well-known SPICE platform that may be downloaded at zero cost. On the other hand, ngSPICE is less known, but it is completely open source. Theoretically, any SPICE software could be used, but it is worth noting that although most of the basic functionality is common between the two variants in the form of netlists, the modeling of frequency dependent elements required the computation of two different netlists. Modeling circuits with a frequency dependent coupling factor is not supported by SPICE. Therefore, the commonly used k statement cannot be used. For LTSPICE, the B-source, an arbitrary behavioral source, was used to model frequency-dependent effects and coupling. Frequency dependent characteristics leverage the Laplace function. In ngSPICE, a different approach was required because the XSPICE s_xfer function cannot handle fractional-order transfer functions. Therefore, the netlist must be implemented with a special "hertz" variable.

Per the FastHenry User's Manual [42], a good rule of thumb is to ensure that the outer most discretized sections are approximately equal to the skin depth. This can be accomplished by either creating more discretizations, which increases computation time, or correctly adjusting the ratio of adjacent sections. The formula shown in eq. (7.8) is implemented in Appliqué, which automatically calculated the optimal number of discretations

D_{total}.

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \approx \frac{D_{total}}{\left[2 + 2\sum_{i=2}^{\frac{n-1}{2}} r^{i-1} + r^{\frac{n-1}{2}}\right]} \tag{7.8}$$

Increased accuracy in the printed inductor model is also achieved by including the effects of skin and proximity effects, which is supported in Appliqué. For the most precise printed inductor modeling, Appliqué can run FastHenry2 at each frequency of interest. For a large bandwidth with fine resolution, the simulation could comprise thousands of FastHenry2 executions. Of course, this is extraordinarily time-consuming. To reduce computation time, Appliqué can run so-called single, double or triple-point analyses. For the single-point simulation, only one frequency is run. The double-point and triple-point simulations run FastHenry2 at two and three different frequencies, respectively. The double-point includes frequency-dependent resistance, while the triple-point also considers frequency-dependent inductance. While analytical expressions for frequency-dependent resistance and inductance is highly complex, an accurate approximation may be achieved using data points near DC, the frequency of operation, and some arbitrary very high frequency. The concept is based on solving two simultaneous equations, eq. (7.9). The results of these approximations are shown in table 7.2, which was published in [57]. These results are based upon the coils discussed above. As shown, Appliqué is very accurate with predicting SRF, within a few percent. It should be noted that the triple-point scheme provides little benefit in accuracy. Therefore, the double-point is the recommended default approach.

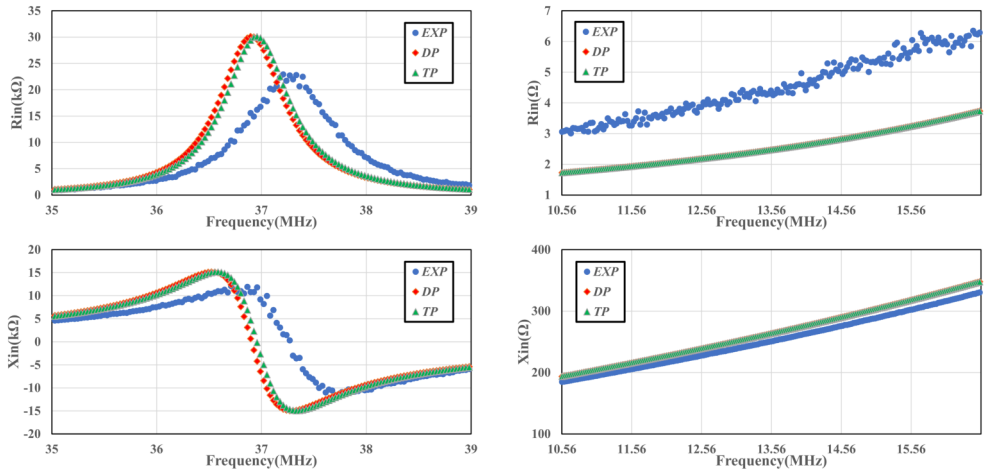
$$\begin{aligned} R_{total} &= R_{DC} + c_1\sqrt{f} \\ L_{total} &= L_{HF} + c_2\frac{\sqrt{f}}{f} \end{aligned} \tag{7.9}$$

Presently, Appliqué models inductance and capacitance well. However, there are some inaccuracies with the prediction of resistance. As shown in fig. 7.10, the SRF, which is a function of inductance and capacitance, is quite accurate. However, the resistance is consistently an ohm or two underestimated.

Table 7.2: Appliqué SRF Modeling Accuracy

ID	**n**	**TW (mil)**	**TS (mil)**	**App. SRF (MHz)**	**Exp. SRF (MHz)**	**Err. (%)**
1	3	40.0	8.0	36.93	37.30	0.988
2	3	40.0	10.0	37.35	37.61	0.685
3	3	40.0	12.0	37.62	38.11	1.296
4	4	40.0	6.0	28.64	28.77	0.466
5	4	40.0	8.0	29.02	29.04	0.056
6	4	40.0	10.0	29.56	29.47	0.330
7	4	40.0	12.0	29.89	30.25	1.209
8	5	40.0	6.0	24.68	24.73	0.188
9	5	40.0	8.0	25.08	25.47	1.540
10	5	40.0	10.0	25.58	26.08	1.928
11	5	40.0	12.0	26.14	26.83	2.602
12	6	40.0	6.0	22.44	23.09	2.819
13	6	40.0	8.0	23.02	23.81	3.341
14	6	40.0	10.0	23.72	24.64	3.729
15	6	39.0	12.0	24.02	24.87	3.296

Note: (App.) = Appliqué and (Exp.) = experimental.



(a) SRF modeling. (b) Impedance in the 13.56 MHz region.

Figure 7.10: Appliqué post analysis of coil #1.

RX Coil Design

Although the coils analyzed above performed well, the new implant enclosure with an 18.0 mm x 26.0 mm internal cavity required modification. To maximize magnetic field coupling, a rounded-rectangle geometry was selected. Due to manufacturing variation, the coil was designed with a width of 17.0 mm and a height of 25.0 mm. It is important to note that the entire area was not available for the printed coil since the coil required a practical means to attach to the lower wireless power PCB.

To minimize DC and AC resistances an array of potential RX coils was manufactured using 4 oz. copper. The updated RX coils, blue, are shown in fig. 7.11. The green coils are those characterized above in the Appliqué section and shown for comparison. The new RX coils have a finished thickness of 56.5 mil. Each copper layer is separated equally at 17 mil. A cross-section of one of the coils is shown in fig. 7.4.

Following thorough analysis, coil L6 was selected, which was based on measured inductance, Q and SRF. The design parameters, as well as measured characteristics, are shown in

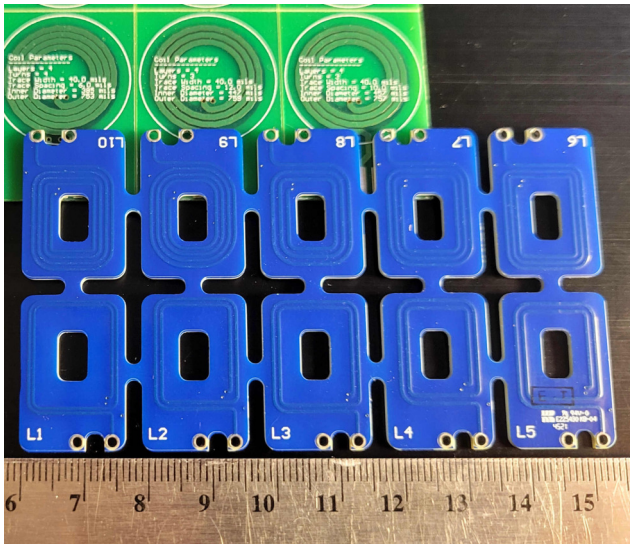


Figure 7.11: 4oz. PCB RX coil array.

table 7.3. Because these coils are of the rounded rectangle variety, some new parameters are introduced in the table. The inner width and inner heights of the copper traces are listed as W_{inner} and H_{inner}, respectively. Likewise, the inner corner radius is R_{inner}. In an effort to minimize layer-to-layer capacitance, each layer is offset in the X-Y plane: $Off_x(mil)$ and $Off_y(mil)$. The SRF is that calculated in Appliqué.

Loop-Coil Design

The design of the TX loop-coil system was optimized using an iterative process with customized scripts similar to that used in Appliqué. Given that various implementations of the RX coil were already designed, those relevant parameters were considered set. Likewise, the expected separation of about 2-3 cm was considered constant as this was the defined nominal use case. It's important to note that the loop-coil system used for the latest implant, was originally optimized for a slightly larger spiral RX coil. Using much of the underlying Appliqué software, TX loop and coil parameters were swept to firstly maximize Q, and secondly to identify a region of compatibility with the RX coil. In short, thousands of

Table 7.3: RX Coil Parameters

Parameter	**Value**
$Turns$	3
$T_w(mil)$	20.0
$T_s(mil)$	20.0
$R_{inner}(mil)$	20.0
$W_{inner}(mil)$	362
$H_{inner}(mil)$	524
$Off_x(mil)$	20.0
$Off_y(mil)$	20.0
$L(\mu H)$	3.40
$C(pF)$	28.0
Q	37.4
$SRF(MHz)$	33.9

simulations were run to identify TX loop and coil parameters. Following some baseline loop and coil designs, which reduced the large number of possible combinations, three possible coil designs were identified. Using the methodology discussed in [78], k_{12} and L_1 were swept in an effort to match the original transmitter source resistance to the empirically derived load resistance: $R_s = 50\Omega$ and $R_{load} \approx 200\Omega$. In [78], an approximation for a three-coil system input impedance was presented, which is shown in eq. (7.10).

$$Z_{in} = Z_1 + \frac{\omega^2 M_{12}^2}{Z_2 + \frac{\omega^2 M_{23}^2}{Z_3}} \tag{7.10}$$

As discussed, all parameters were set for three different TX-coil designs except that involving the loop dimensions and coupling to the TX coil. However, the more general $(M_{12})^2 = k_{12}^2 L_1$ was known, as its value was set in order to satisfy the input impedance equation. The modified software, which could sweep all parameters of a three-coil system and model the behavior through FastHenry2, was set to adjust loop outer diameter, loop trace width and loop-coil separation. Using the compiled simulation data, loop Q was maximized while filtering out simulations that did not satisfy the desired $k_{12}^2 L_1$. Upon fabricating the optimized loop and coil, the simulated data was verified. The best performing design is shown in table 7.4. The simulated optimal loop-coil separation distance was calculated at approximately 909 mil (23.1 mm), with 899 mil (22.6 mm) used due to available PCB standoffs.

However, the loop-coil separation distance was later modified for the current RX coil. Adjusting the distance by hand revealed the best performance to be at about 10 mm, which corresponded to an available nylon standoff spacer.

7.2 Linear Power Amplifier Module

As previously mentioned, the PA used for wireless power transmission for the most recent implant device was a relatively simple, linear configuration integrated as a module into the BS-M unit: the BS-LWPM. The simplified schematic for the BS-LWPM is shown in fig. 7.13.

Table 7.4: Printed TX Loop-Coil Parameters

Parameter	**Loop**	**Coil**
$D_o(mil)$	1466	2500
$T_w(mil)$	100	100
$T_s(mil)$	NA	40
$Turns$	1	7
$L(\mu H)$	0.145	1.95
$C(pF)$	948	73.2
$SRF(MHz)$	240.8	51.5
Q	116.5	49.15

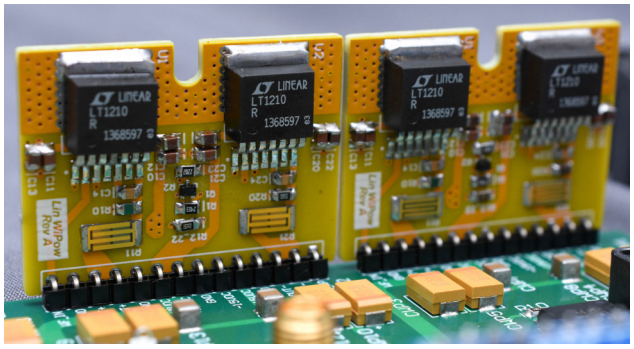


Figure 7.12: Linear wireless power amplifier modules in base station.

Compared to state-of-the-art switching PAs, this unit is far inferior in terms of efficiency. The goal, however, was to integrate a small form-factor module into the BS-M unit for both proof of concept and convenience. Secondly, an analysis of the wireless power interference on the sensitive IR RX circuitry was desired. The gain of this op amp configuration is shown in eq. (7.11). If $\frac{R_{20}-R_{10}}{R_{12\_22}} = 1$, then the gain reduces to that of eq. (7.12). Given the values here, the gain is set at approximately 6.

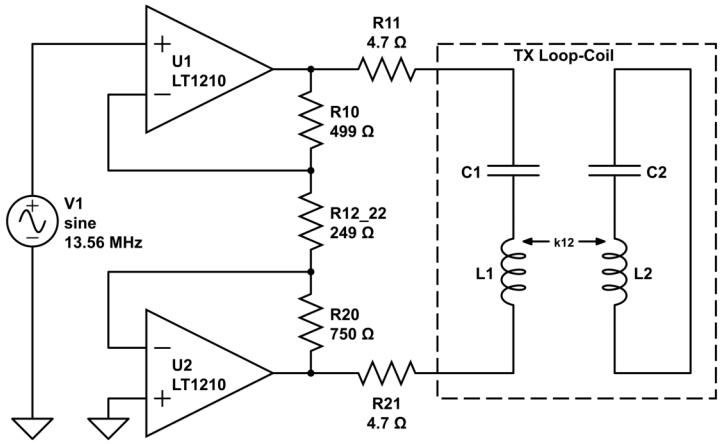


Figure 7.13: High-power bridge-amplifier TX loop-coil driver.

Despite being a relatively familiar op amp configuration, there are some key aspects that are critical for proper functionality. The LT1210 is a high-power current-feedback amplifier (CFA) rated at 35 MHz. It can operate from $\pm 15V$ rails and deliver well over 1 A into a load. Given the capabilities of this CFA, careful attention must be paid to the external component selection. While a CFA places importance on resistor values, the output current necessitates proper power ratings for R11 and R21, which are both rated at 6 W. Also, R11 and R21 have been included to help "buffer" the amplifier when driving the resonant load at the expense of additional power dissipation. To maintain a predictable voltage swing, the gain-setting resistors should be of the precision variety. As a side note, since both op amps share R12_R22, this provides one less component subject to tolerance variation. However,

that also places more emphasis on the selection of R10 and R20.

$$\frac{V_{drv}}{V_1} = \left(\frac{R_{10} + R_{20}}{R_{12\_22}} + 1 \right) \tag{7.11}$$

$$\frac{V_{drv}}{V_1} = 2 \left(\frac{R_{20}}{R_{12\_22}} \right) \tag{7.12}$$

7.3 Wireless Power Conversion

A high-level overview of the implant wireless power system and its relation to the general power system is shown in fig. 7.14. Naturally, the wireless-power coil is the primary energy source for the entire implant. The thick red arrows represent unregulated 13.56 MHz AC voltage. Downstream from the wireless power coil, resides the over-voltage protection (OVP) clamp and the bridge rectifier of the LTC3330. The unregulated rectified DC voltage is represented as a thick yellow arrow, which feeds into the buck converter. The output is a thin yellow line, which represents the regulated XVX voltage rail. As discussed above, a current-sense amplifier measures the output current and the LDO steps down XVX to a default 2.5 V. The buck-boost converter is not in operation during wireless-power operations. Therefore, there is no power flow from the battery to the converter, and that block is grayed out in the figure.

Given that the buck-converter is responsible for efficient rectified wireless power voltage, bench-top tests were conducted to evaluate its performance. These tests supplied a constant 8 V to the input of the LTC3330 bridge rectifier. The input voltage to the LTC3330 is highly variable, but approximately 8 to 10 V is common while under load. Therefore, these power tests were focused on end-to-end performance as opposed to evaluation of an isolated buck converter. In fig. 7.15, the resulting power-conversion efficiencies are shown with the output set to 5 V. The end-to-end efficiency is approximately 70% from about 5 mA to 35 mA. However, taking into consideration the voltage drop of the bridge rectifier the buck converter efficiency spanned from about 95% to about 87%.

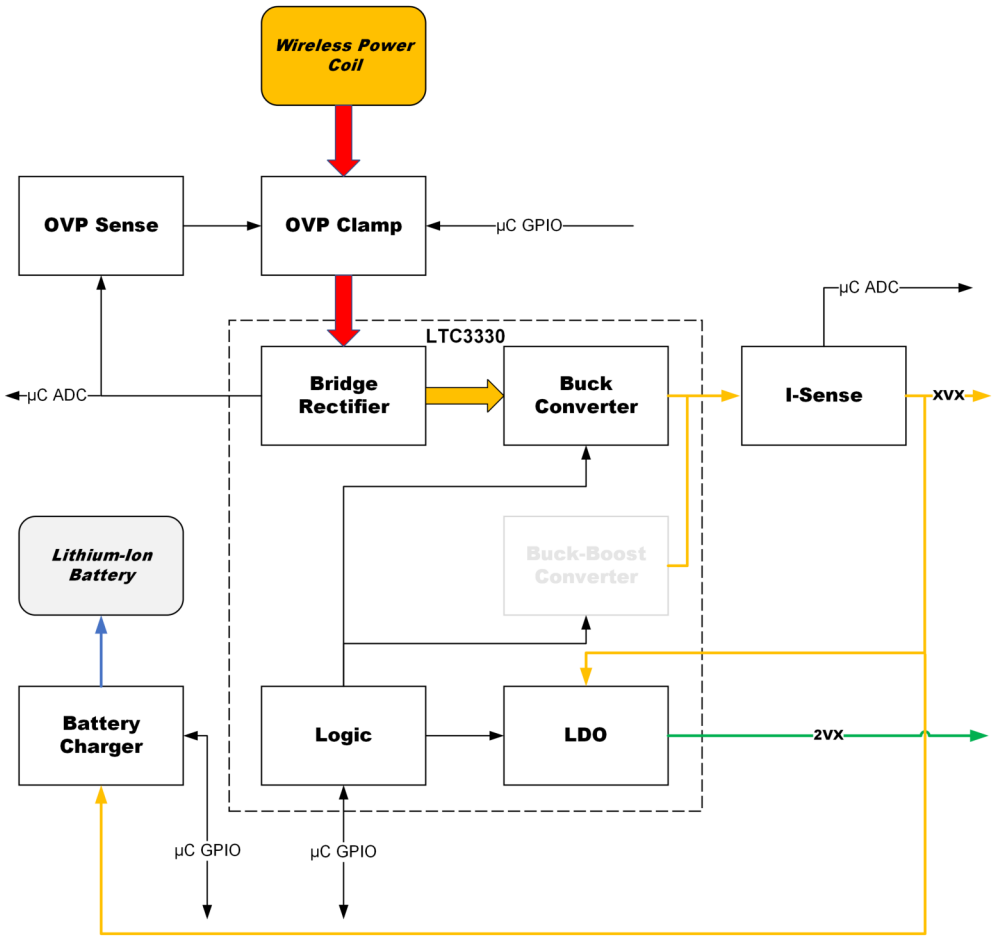


Figure 7.14: Implant wireless-power management overview.

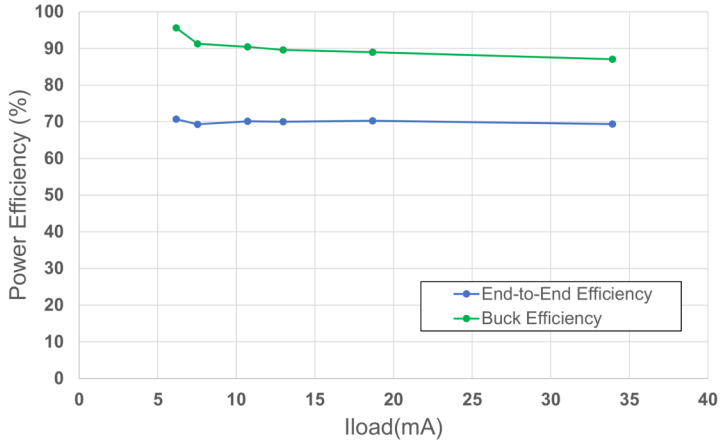


Figure 7.15: LTC3330 wireless-power conversion efficiency is consistently efficient over range of currents.

7.3.1 Over-Voltage Protection

Due to the highly variable nature of wireless power delivery, over-voltage protection is often required for device protection. The LTC3330 integrated bridge rectifier has an absolute maximum voltage rating of 19 V. While the implant device is charging the battery, for example, the heavy load on the system maintains the rectifier voltage well under the maximum rating. However, when a heavy load transitions to a light load, or the implant inadvertently is positioned too close to the TX coil, the maximum voltage can often be exceeded. For protection, the LTC3330 provides an integrated Zener diode with a breakdown voltage of approximately 20 V. Our experience with wireless-power RX systems has shown that Zener diodes are very problematic when used as a shunt protection device for a rectifier input. The exact mode of failure has not been thoroughly investigated, but the result is usually the Zener diode failing into a short-circuit condition. A similar effect happens with LTC3330 when the maximum voltage is exceeded for sustained periods of time, thus destroying the energy harvesting capability of the entire IC.

Because the integrated rectifier output and buck converter input of the LTC3330 are externally connected to a pin, a simple shunt clamp is a possible and relatively easy remedy.

However, the current handling capabilities of the integrated diodes have a maximum rating of 50 mA. Therefore, shunting the rectified voltage in an attempt regulate the rectifier input voltage is also potentially destructive.

Limited by space, an active clamp at the input of the LTC3330 rectifier was the only practicable option. The final design is shown in fig. 7.16. Conceptually, the operation is quite simple. The rectified voltage is compared against a reference. If that reference is exceeded, the op amp begins to apply voltage to the gates of the MOSFETs, thereby shunting current in a controllable fashion. It is important to consider the transient response of the clamp. Previous iterations implemented a comparator-based clamp to minimize response time. However, these comparator-based circuits resulted in oscillation. Additionally, a slower, linear response enabled the LTC3330 to still harvest energy if the rectified voltage approaches destructive levels. The output voltage of the op amp circuit, V_{clamp}, is shown in eq. (7.13). Note that V_{in} refers to the rectified output voltage seen across the LTC3330 Zener diode. This circuit was designed specifically to ensure that no clamping voltage was applied to the MOSFET gates up to a particular voltage, at which point the circuit would begin to slowly apply voltage. Furthermore, the components were selected to ensure the op amp provided maximum voltage to the MOSFET gates before the Zener diode reached breakdown voltages. The final values implemented were intended to begin clamping action at approximately $V_{in} = 13.8$ V and provide 3.3 V at $V_{in} = 16.9$ V. If XVX is set to 5.0 V, a V_{clamp} of approximately 5 V is achieved at $V_{in} = 18.5$ V.

An additional feature of this clamping circuit allows the microcontroller to clamp the input. U3 is an open-drain inverter. When a logic high is provided, the output of U3 swings to 0 V, ensuring that U6 swings to XVX. There are two reasons for this behavior. Firstly, the microcontroller actively monitors the wireless-power rectified voltage. Secondly, the clamping action may be used for a low data rate load modulation scheme. However, analysis of the second design intent has not been verified.

The configuration of the MOSFETs here are similar to those employed in AC-AC power switching schemes. As shown in [69], multiple configurations are possible, each with their

inherent tradeoffs. In this design, with the sources of each MOSFET tied to ground and the gates connected, applying an adequate gate-source voltage (V_{gs}) is much more practical with the constrained DC-powered circuitry since the source is always 0 V. This design also relies on the intrinsic body diodes of the MOSFET in that when one of the transistors is switched on, the other must conduct current through this parasitic diode.

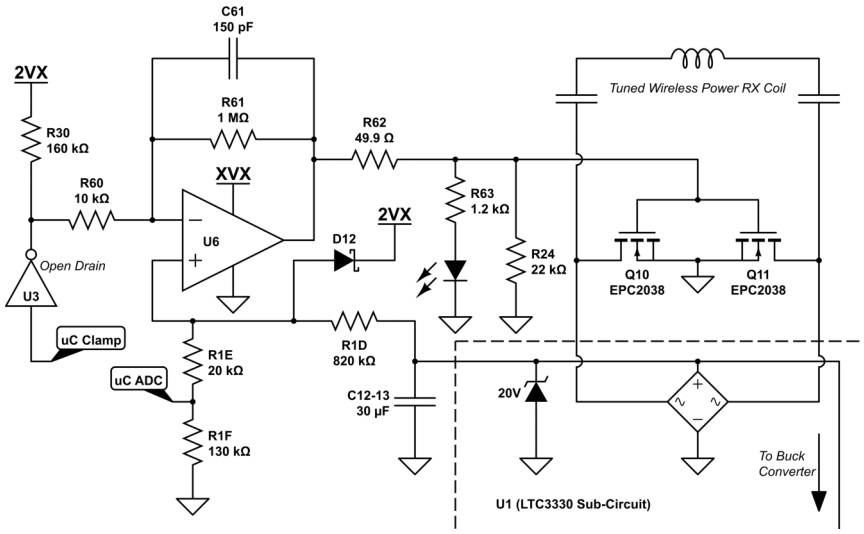


Figure 7.16: Over-voltage protection for LTC3330 rectifier.

When designing an over-voltage protection, designed to clamp the rectifier input, the selection of MOSFETs is not an arbitrary decision. Of course, the MOSFETs must be able to handle the voltage and current when shunting current away from the rectifier. Additionally, the MOSFETs must be physically small. Just as important is the parasitic capacitance introduced by the clamping transistors. The tuning capacitance required for an inductor of $3.3\mu H$, places the capacitance in the tens of pF, which is in the range of parasitic capacitance introduced by transistors. Given the above criteria, enhancement mode gallium-nitride (eGaN) MOSFETs were selected. The eGaN MOSFETs provide superb power handling characteristics in a tiny form factor and are designed for high-frequency applications. In this design the EPC2038 eGAN MOSFET was selected. The EPC2038 can handle up to 100 V

for V_{DS} and 500 mA of drain current. The on resistance, $R_{DS(on)}$, is specified at a nominal 2.1 $m\Omega$ with V_{GS}=5 V. Each transistor occupies only 0.9 mm x 0.9 mm. While parasitic capacitances of interest vary with applied voltage, the total shunt capacitance introduced to the RX coil network is estimated to be 1.84 pF.

During bench-top experimentation, the clamp behaved as expected limiting the rectified input voltage below harmful levels. Because of the destructive nature of verifying the operation of this circuit, a thorough analysis comparing the unprotected input voltages versus the clamped voltages has not been conducted. DC power supply tests to LTC3330 rectifier clamping circuit revealed triggering at the expected voltage. When the trigger voltage was exceeded, the DC power supply source current began approaching 100 mA before the experiment was terminated. No deleterious effects to the clamping circuit, nor excessive heating, were observed. During wireless power tests, the "warning LED", D12, activated numerous times while the LTC3330 buck converter was changing states. Presently, the normally sensitive LTC3330 bridge rectifier has yet to show any signs of damage.

$$\begin{aligned} V_{clamp} &= V_{div} + (V_{div} - 2VX)\,\frac{R_{61}}{R_{60} + R_{30}} \\ V_{div} &= V_{in}\frac{R_{1E} + R_{1F}}{R_{1D} + R_{1E} + R_{1F}} \end{aligned} \tag{7.13}$$

7.4 Results

7.4.1 Previous Power-Delivery Experiments

Phantom

The original optogenetic "lollipop" PCB also used the LTC3330. It was similarly set at an output voltage of 5.0 V, with the LDO at 3.3 V. Power transfer tests were conducted on the test-bench, in a phantom and later in-vivo. A cut of pig muscle was used as the phantom. Simulating expected implant depths, a pocket was cut into the pig muscle and the "lollipop" PCB was inserted. Wireless power transfer tests were performed from about 2 to 6 cm. The

results of the test are shown in fig. 7.17. The TX output power spanned from about 1 W to just over 5 W. The load attached to the LTC3330 was set to ensure about 300 mW of power could be delivered, which was done out to about 5 cm. At 6 cm with a significantly increased TX output power of over 5 W, about 230 mW could be delivered to the load. 300 mW was successfully delivered to the phantom, spanning from contact to the 5 cm maximum target distance.

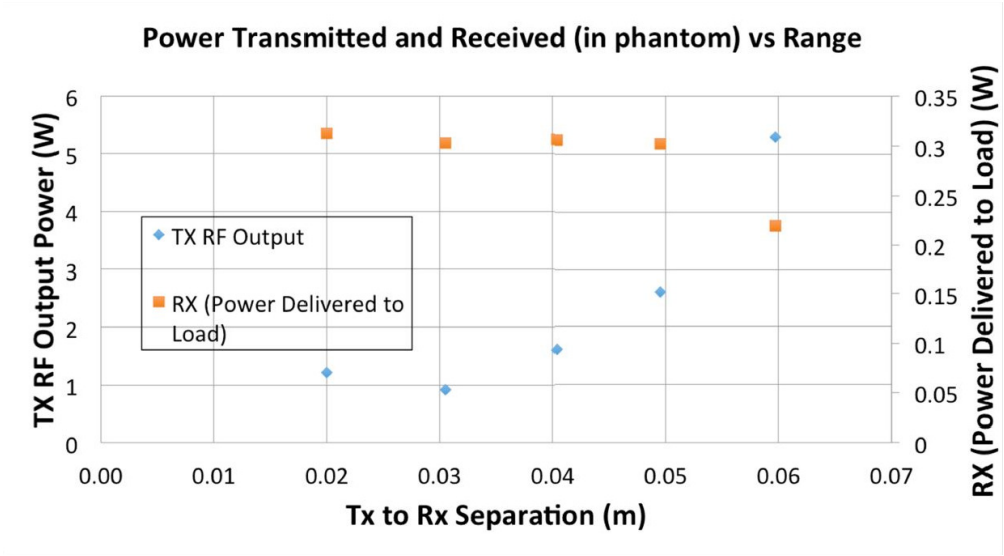


Figure 7.17: "Lollipop" power delivery while in phantom.

In-Vivo

Following successful phantom tests, the "lollipop" system was implanted in the abdomen of a rat with a thermocouple probe for measuring temperature in the cavity. The incision was sutured, and the device was powered at distances of about 2 to 5 cm. The prototype was designed to allow the 470 mF super capacitor to charge to 5.0 V and release the energy to the red and blue LEDs, discussed in chapter 3, which was successfully demonstrated over all of the distances. More importantly, temperature increase within the cavity remained under $1°C$.

7.4.2 Final Power-Delivery Results

Since the latest revision of the implant device features a coil significantly smaller than what was used in the "lollipop" design, performance is expected to be lower than what was demonstrated above. Furthermore, the linear op amp based wireless-power modules are expected to be highly inefficient in comparison to Class D or E power amplifiers. Nonetheless, as is shown below, more than adequate power delivery is possible at use-case distances.

Given that the LTC3330 integrates the bridge rectifier and the buck converter, the buck converter cannot be isolated for testing. Therefore, the buck converter output was selected as the final DC output for power measurements. Furthermore, output power was not recorded if the LTC3330 buck converter could not achieve regulation. Because the device is regulated to a default 3.3 V, the buck converter was fixed at four near-constant power levels by adjusting the load resistance: approximately 240 mW, 195 mW and 148 mW and 100 mW. While 240 mW and 195 mW are larger than any expected power-dissipation levels, 148 mW and lower are realistic power levels encountered during expected operation. As discussed in chapter 6, with XVX set to 3.3 V, it must supply over 41 mW and 156 mW when the maximum charge rate is set to 12.28 mA and 47.4 mA, respectively.

Bench-top experiments were conducted using the macro-scale implant device without a phantom or enclosure. Some brief tests revealed that the presence of the enclosure and phantom tissue, used in the optical communications tests, showed little degradation in performance to the wireless power. The RX wireless-power coil was positioned in a co-planar, approximately co-axial, orientation relative to the TX loop-coil during all performance evaluations. The separation distance was swept from approximately 3 mm to 32 mm. Additional DC power, relative to the zero amplitude quiescent state, is shown in fig. 7.18, while the resulting efficiency is shown in fig. 7.19.

In chapter 5, the nominal separation distance between the implant coil and the BS-AFE was specified at 23 mm. At each of the four power-levels, optimal power efficiency occurred just under 20 mm, with some reduction when reaching 23 mm. As shown in fig. 7.18 and

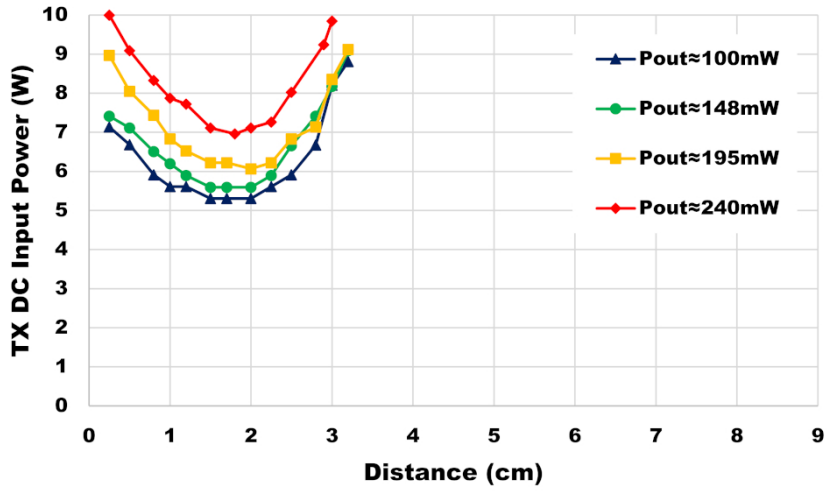


Figure 7.18: TX DC-input power required for wireless transmission to implant at various distances and output powers (Pout).

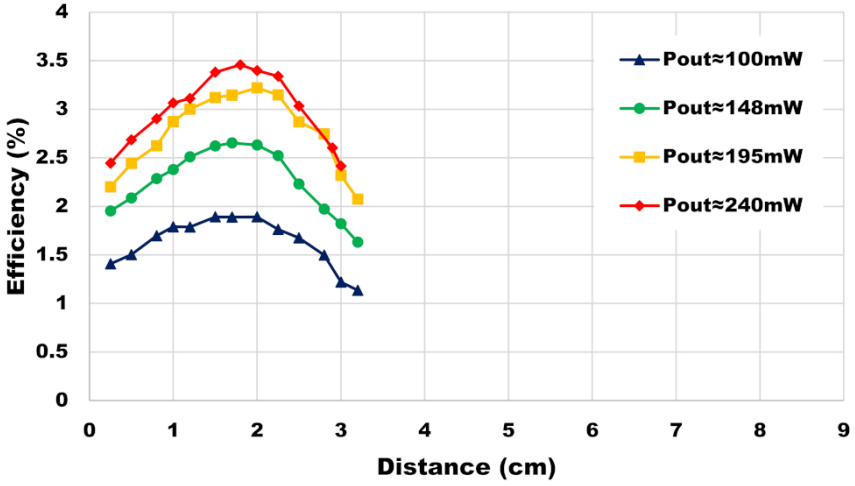


Figure 7.19: Full end-to-end DC-DC power efficiency.

fig. 7.19 243 mW was delivered at 23 mm with an efficiency of 3.34%. At the same distance, 3.15%, 2.52% and 1.76% efficiencies were achieved at 196 mW, 149 mW and 98.9 mW, respectively. The required input DC power was 7.26 W, 6.22 W, 5.90 W and 5.61 W at each of the respective output power levels. Additionally, this system provided 238 mW at 2.42% efficiency at 3.0 cm. At the three lower power levels, 3.2 cm was achieved before the LTC3330 fell out of regulation. Therefore, a power dissipation at more than 148 mW, required for the high-rate battery charging, is completely feasible.

Although not shown in the plots, higher power levels were achieved: 270 mW was observed. However, in-depth tests at these power levels were not conducted in order to avoid damage to the wireless-power circuitry. As shown with the "lolli-pop" device, which also used the LTC3330, over 300 mW is possible. However, several devices were damaged while trying to obtain maximum power delivery during these tests.

Chapter 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusion

In this dissertation, a fully-wireless, implantable research platform has been presented. The implantable portion of this system, designed for operation in the abdominal region of a rat, is housed in a SLS 3-D printed enclosure modeled after a quasi-hermetically sealed enclosure of similar proportions. The latest revision of the device, which comprises four vertically stacked PCBs, occupies a volume measured 18.0 mm x 26.0 mm x 12.5 mm. The enclosure dimensions are 21.0 mm x 32.0 mm x 15.0 mm. To assist in debugging and performance characterization, a so-called "macro-scale" version was developed. The macro-scale version is an electrically equivalent device but scaled up at a ratio of 2.54:1. The macro-scale version resides in an enclosure cavity measuring 44.0 mm x 64.0 mm x 31.5 mm. Similarly, a macro-scale enclosure was also built, which measured 49.0 mm x 79.0 mm x 36.0 mm.

Each of the implant PCBs provides a portion of the implant system functionality. The bottom PCB (IMP-NIN), or that which is facing inward, comprises the Intan RHS2116 neural-IFC ASIC as well as supporting power-management circuitry. Furthermore, this PCB also contains a bank of four NVM NOR-flash ICs, each providing 264 Mbit of memory for neural data storage. Moving outward, the next PCB (IMP-SC) is responsible for computation and system control. The MSP430FR5994, running a custom OS, provides all necessary computation, communication, and supervisory functions. Some IR communication circuitry is also present at this level. Near the microcontroller, a BME280 environmental sensor allows monitoring of internal temperature and humidity. Because of space constraints, a multi-chemistry battery charging IC, as well as the lithium-ion battery, also reside on this PCB.

The next PCB in the stack (IMP-WPIR) contains all wireless power management circuitry as well as IR communication hardware. The LTC3330 forms the heart of the wireless power conversion circuitry and is responsible for the main dynamic voltage rails used throughout the entire implant. The LTC3330 also extracts charge from the lithium-ion battery to power the system in the absence of wireless power. IR communication circuitry, on this level, includes the IR photodiode and TIA stages, as well as, the IR LED and related driver circuitry. The outermost PCB, which is separated from the others via thin layer of ferrite, is the wireless power RX coil.

In parallel, a base station was developed to interface with the implant by means of wireless data communication and power transfer. The core base-station circuitry, powered by external $\pm$ 15 V supplies, resides in an aluminum enclosure. Inside the enclosure are the main PCB (BS-M), a computation and control module (BS-SCM), and a wireless-power module (BS-LWPM). IR communication hardware, within the main device, resides on the main PCB, as well as power management and some wireless-power circuitry. The computation and control module features the PSOC 5LP. The wireless power module is a simple, op amp based, linear amplifier. The enclosure thermally connects to the wireless power module, which is cooled by a fan. A remote wireless-power coil with co-axially positioned IR communication circuitry (BS-AFE) is connected to the base station by RF and USB 3.0 cables. Control of the system is accomplished via a serial link.

The IR communication and wireless power systems required significant design effort as well as numerous revisions to achieve the aforementioned goals. The IR channel, which operated at a wavelength of 1300 nm, was designed to be transmitted through free space, a sapphire quartz window embedded in the enclosure, and about 1-2 mm of biological tissue. Likewise, the wireless power system would need to achieve effective inductive coupling through a similar set of mediums. Given that the IR photodiode and LED, as well as supporting circuitry, are aligned co-axially and approximately reside in the same plane, the TX and RX separation distance for both communication and wireless power is considered the same. While at any given time, the implanted device could be separated from the BS-AFE

by an unknown distance, a separation distance of 2.3 cm was considered the nominal use case when a RUT would be on all fours inside of a designated area.

IR communication performance was evaluated using a PLR test over a variable separation distance between transmitter and receiver. Both downlink and uplink performance were characterized. The downlink flow of data, from the BS-AFE to the implant, met stated bitrate goals with excellent reliability. While aligning the IR LED and photodiode in the most favorable orientation, a phantom comprising 4 mm of deli ham and a sapphire crystal 0.8 mm thick were placed near the implant photodiode to simulate a real-use case. Downlink data transmission was measured at 115.2 kbps with 0% PLR in a sample of 10000 transmitted packets at a separation distance of 6 cm. Freespace tests showed that up to 576 kbps was possible, albeit with nearly 50% PLR. The uplink test was conducted in the same manner, except it was performed with both a phantom and in free space. The phantom in this case was very similar: 0.8 mm of sapphire and 3 mm of raw pork. Uplink communication reached 2 Mbps with 0% packet loss in 10010 transmitted packets at 2.7 cm. In free space, the same reliability was achieved to a distance just under 5 cm.

The wireless-power link, in its current form, was shown to achieve acceptable overall performance. Similar to the communication evaluation tests, the wireless power system was aligned co-axially for optimal coupling. The wireless-power data presented in this dissertation was conducted through free space. However, subsequent tests through the enclosure material and 3 mm of raw pork at a few test distances showed little difference in performance. Nonetheless, wireless-power was transferred 2.3 cm to the implant buck-converter output resulting in 243 mW of load power. The end-to-end efficiency at this distance was 3.34%. Also at 2.3 cm separation distance, transmission of 196 mW, 149 mW and 98.9 mW, resulted in efficiencies of 3.15%, 2.52% and 1.76%, respectively. Furthermore, 195 mW was transferred to the implant at a distance of 3.2 cm.

While developing the wireless power system, software was designed in Python that leveraged several underlying open-source applications and provided the ability to export directly into common PCB CAD software. The software, entitled Appliqué, provided an

intuitive graphical front end. Printed inductor designs could then be modeled by FastHenry2, FasterCap and SPICE. Comparing simulated and experimental results showed a relatively high degree of accuracy when predicting inductance as well as parasitic resistance and capacitance. SRF was predicted in a range of about 0.056% to 3.73% error.

8.2 Future Work

Because this dissertation focused on the feasibility of a system design, many aspects remained unoptimized and unexplored. In general, further iterations of the designs are suggested with a primary focus on improving the robustness of the system, minimizing energy consumption, reducing implant size, etc. Similarly further research and testing will unveil new opportunities for system improvement. While discussing every possible topic for improvement is outside the scope of this dissertation, the following sub-sections highlight some of the most important aspects.

8.2.1 Lossless Data Compression

The recorded data from the Intan RHS2116 necessitates substantial NVM in this application. As discussed, the required NVM occupies considerable space and consumes significant energy. Although outside the scope of this investigation, the implementation of lossless compression algorithms promises a non-negligible reduction in memory requirements. Some exceptional CRs were reported for lossless compression techniques: [71] reported a CR of 5.35 and 10.54 for local-field potentials (LFPs) and spikes, respectively, with a custom 180-nm CMOS analog front end. Another paper [56], also in custom 180-nm silicon, reported CR of 8 and 16 using compressive sensing. Presently, the applicability of either compression technique remains unclear.

The goal, therefore, would be to implement a practical compression algorithm with minimal computational resources. While many examples exist with impressive compression ratios, implementing such a scheme on an MSP430 that is also compatible with the design constraints will be challenging. Although the signal bandwidth of only 1 kHz was used,

Foerster, et al. [22], implemented a lossless data-compression scheme using previously-recorded primate ECoG data. In the publication, compression was accomplished by combining Huffman encoding with a linear prediction method and principal component analysis. Moreover, the compression scheme was implemented on an MSP430. Using only Huffman encoding, the authors report a CR of 2.0, while the best tradeoff between complexity and performance was the application of first-order linear-prediction, and then Huffman encoding, which achieved a CR of 4.1. While this work will have to be analyzed as it applies to the type of neural signals expected in our application, the results are extremely promising.

8.2.2 Communication

IR Hardware and Physical Layer

The IR TX and RX hardware in both the implant and base station circuitry presents various opportunities for improvements. While the implant side is much more limited in terms of space and power, further refinements regarding power dissipation and gain-bandwidth tradeoffs are warranted. As discussed in chapter 5, the implant IR TX sub-system is potentially capable of providing the same bitrate performance at about half the required power. Presently, 5 V is stepped down to 1 V to drive the IR LED. The buck converter is about 55% efficient for this particular load. A simple revision that extracts energy directly from the lithium-ion battery could minimize losses. Furthermore, to reduce voltage spiking, the IR LED driver sinks constant current when the IR LED is in the off state. The current design allows modification by changing R_{TX2} from 50 Ω to a larger value, thereby reducing the off-state current and minimizing wasted energy. Further improvements should focus on the IR LED TIA stage biasing and improving the AGC.

Of course, the base station provides ample opportunity for improvements given its relatively loose design constraints. The IR TX circuitry traded speed for driving four IR LEDs, while minimizing inductive ringing. As shown in the IR downlink evaluation, the base station remote AFE is able to reliably deliver data at 6 cm. While gain on the implant could be

reduced, this could also provide an opportunity for better performance by reducing the total number of IR LEDs.

While the encoding scheme in this research was limited to the asynchronous form specified by IrDA, various other methods exist. The synchronous 4 PPM encoding, also specified by IrDA, when transmitting at 4 Mbps was considered for this project. However, the MSP430, while providing the asynchronous modulation hardware, does not have a 4 PPM capable peripheral. Although it is possible to create a workable solution in C code, 4 PPM is something that is practical when implemented on an FPGA. During the development, some basic 4 PPM functionality was implemented on the PSOC5LP; however, further development has not been pursued.

Upper Protocol Layers

During development, the strict adherence to the IrDA Lite specifications was somewhat relaxed and customized as implementation ascended upward through the layers. The IrPHY layer was designed to be within specification. The IrLAP layer was also relatively consistent. However, the IrLMP layer provided some of the specified functionality, but was also highly customized for the application. Indeed, the IrDA Lite implementation is not a requirement. Ultimately a custom protocol like IrDA, but with application specific commands, would be desirable in future revisions.

8.2.3 Wireless Power

Coil Design and Modelling

While the implant coils in this project have relied on multi-layer printed inductors with tuning capacitors placed in series, a thorough examination of printed-coil topologies and tuning methods should also be conducted: for example, a comparison of different PCB layer counts combined with series and/or parallel tuning. As previously discussed, the SRF of the small-scale PCB coils is a function of parasitic capacitance, which severely degrades

the coil Q. Related, the dissipation factor of the PCB laminate also negatively impacts the performance of the coil. Investigation in this dissertation was limited to that of FR-4 laminates, which is regarded as inexpensive and merely adequate for some RF designs. Therefore, thorough research into more advanced laminates, such as those offered by Rogers is warranted.

To further assist in the design, more extensive modeling techniques and simulation will be required. While Appliqué provides a platform to quickly model and design PCB coils, it has various limitations. While revisions to improve the user-experience and eliminate bugs are always necessary, Applique is inherently limited by its reliance of FastHenry2 and FasterCap. FastHenry2 does not consider magnetic materials: Thus, relative permeability is always assumed to be one. This presents a serious challenge for modeling the effects of ferrite shielding. Since this software is open source, the possibility to implement this feature is always possible. In addition to the quasi-magnetostatic and quasi-electrostatic analysis, full-3D EM simulation using software like CST, which was utilized in [79], should be investigated.

TX Power Amplifier

Considerable improvement opportunity for the base station wireless power module also exists. The scope of this work did not entail thorough research and design into this subsystem. The goal was to integrate a convenient, practicable solution into the base station. With tuning for improved impedance matching, some end-to-end improvements should be achievable. However, a switching power supply, like Class D or Class E is most likely the best option. A linear amplifier system, while inefficient, may provide benefits with regards to device interference, more specifically communication. While that issue remains unsettled, the conservative approach of time-interleaving wireless power with communication demands that switching power amplifier topologies specifically designed for this application be integrated.

Adaptive Impedance Matching

The OVP shunt protection circuit would ideally "mistune" the resonant receiver circuit when lightly loaded, or more generally, adaptively adjust the tuning for optimal impedance matching at all loads. Initial designs explored placing large-valued capacitors in series with each eGaN MOSFET. The intent was to shift the resonant frequency as the rectified voltage increased beyond the desired threshold. Results were mixed. Some mistuning was observed, but the effects were not adequate to protect the LTC3330. In some cases, it seemed to be counterproductive.

While this method was abandoned for the implant design, the observed results in combination with the many concepts explored in literature and industry suggest this is a worthwhile pursuit. For example, Waters, et al [88] demonstrated a tunable π network for an adaptive impedance matching algorithm, while Lee, et al [51] demonstrated a reconfigurable resonant coil method where the impedance was varied by manipulating the coupling coefficient by switching in different loops, relative to the high-Q coil. A tapped-inductor topology for optimal super-capacitor charging was investigated in [60]. It is important to note that [88], [51] and [60] demonstrated these designs at HF. Linear Technologies leverages so-called "Dynamic Harmonization Control" (DHC), which was patented by the University of Auckland spinout Power By Proxy [29], in their LTC4120 PMIC. The DHC approach dynamically adds a shunt impedance (capacitive) to the tuning capacitor. As power levels become too large, the resonant frequency is shifted away from that of the transmitter, and as power levels become too small, the resonant frequency is shifted towards that of the transmitter. It is important to consider that the LTC4120 was designed with a nominal frequency of 130 kHz in mind. While it is unclear how well this system would perform at 13.56 MHz, the concept is sound, at least theoretically.

8.2.4 Custom Devices

ASICs

This design was largely at the mercy of available ICs and device packaging. Throughout the process, every component was minimized when possible. The reality, however, is that this application stretched the scope of many components beyond their intended design. Hence, many devices had marginally adequate performance and, oftentimes, unnecessary features. The latter, of course, is a waste of precious resources.

The high-level of integration of the LTC3330 was enabling in many aspects; however, it was also debilitating in others. The integrated bridge rectifier and buck-converter caused the premature failure of countless chips. The bridge is limited to an absolute maximum of 50 mA and the input voltage to about 19 V. The LTC3330 has integrated a Zener diode with a breakdown voltage of 20 V. Experience has shown that Zener diodes are very problematic in wireless power systems when used as OVP. The LTC3330 likewise is extremely sensitive to over voltage, as discussed in chapter 7. The buck-converter input is also susceptible to damage from excessive current. During the process of this research, it was also discovered that in-rush current into the bridge and buck converter was the culprit for many device failures that weren't caused by obvious misuse. These shortcomings are not criticisms of the LTC3330. It was designed to be a "nanopower" energy harvester with the intent of extending primary-cell battery life. For this application, a more robust wireless power system would greatly benefit from a custom-IC tailored to the power requirements of the implant.

Similarly, there are various other portions of the implant that would yield substantial returns from ASICs. The RHS2116 is designed to be a front-end for various devices, hence the usage of SPI for data transfer and clocking. However, for the purpose of a wireless implant device, a more suitable design would integrate a processor (e.g; Arm Cortex M).

Energy Storage

Until we see dramatic improvements in supercapacitor and battery technology, lithium batteries appear to be the only practicable energy storage solution for a system in this application space. The so-called UMAL devices were the most appropriate devices available but were only produced in two capacities: 12 mAh and 24 mAh. Both had a width of 14 mm and length of 21 mm, thereby setting limits on implant size and dimensions. To make matters worse, these devices have been discontinued by Murata. No known substitutes are available. Nonetheless, it is conceivable that a similar chemistry battery could be developed with slightly less capacity and reduced dimensions.

IC Packaging

Given the power and communication requirements of this design, current IC processes make a complete SoC highly unlikely for the foreseeable future. Regardless, multiple opportunities exist for improved packaging. Many of the ICs used in this project can be realized by COTS devices. Previous versions of the implant included Torex's "micro DC/DC" converters, which included an integrated inductor. Per conversation with Marktech Optoelectronics custom packaging is also available for the LEDs and photodiodes.

8.2.5 Inductor Elimination and Reduction

In general, inductors consume significant area, which of course is detrimental to the size of an implantable device. Indeed, significant area savings are achieved, at the expense of efficiency, by increasing the switching frequency. GaN transistors can achieve efficient DC-DC power conversion at frequencies well above a few MHz [53], but further reductions in area can be achieved by so-called single-inductor-multiple output [SIMO] converters. This power conversion topology uses one inductor as the energy storage element, and time-multiplexes the energy delivery to multiple outputs. Power efficiencies have been shown at 87% at 330mW [82]. The tradeoff, of course, is increased complexity, decreased efficiency, and

increased voltage ripple at the outputs. Given that this system will require additional discrete components, and more switching transistors, its implementation may simply consume too much space, thereby negating its benefit.

8.2.6 Biomedical Simulations & Experiments

Additionally, simulated tissue effects should be conducted, even though less than $1°C$ was measured during an in-vivo experiment. A higher level of confidence will be achieved if specific absorption rate (SAR) values are within accepted standards.

Similarly, in-vivo experiments will further enhance the robustness of the proposed implant. Long-term implantation, which will confirm complete package reliability, device performance and biocompatibility is, perhaps, the ultimate validation.

8.2.7 Full GUI Application

As was mentioned in the [24], the GSK BIC required a centralized "base station". While the specifications were open-ended, the base station was to maintain system time and provide an interface for scientists to perform experiments. Presently the Sensor Systems Lab has various GUI applications for wireless power and backscatter devices written in Python. Both the WISP and wireless-power applications have seen many years of refinement, so they are quite reliable and robust.

Similarly, the design of this system was completed with the goal of being controlled by a custom GUI application. The CLI used via serial terminal can be conveniently integrated into an environment like Python. With a GUI, the configuration and control of the implant can be much more intuitive and automated.

8.2.8 Extension to Other Applications

Although the current system was targeted toward recording neural data from a RUT, this system could be adapted to many applications. In the current configuration, the Intan

RHS2116 may be used as a general-purpose neural IFC. The modular design of both the implant and base-station devices opens this system up to countless sensing opportunities. For example, the IMP-NIN PCB could be exchanged for a sensing module designed for recording conditions within a hazardous environment.

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Appendix A

SCHEMATICS

This appendix includes all base station and implant schematics, as well as custom programmer and serial IFCs used during development. All PCBs were designed in Altium Designer. Some of the simpler PCBs use only a single schematic page, while the more complex PCBs comprise several sub-schematics with an associated "top-level" schematic detailing interconnections. The schematics are organized as follows:

BS-M Base Station Main.

BS-LWPM Base Station Linear Wireless-Power Module.

BS-SCM Base Station System-Control Module.

BS-AFE Base Station Analog Front End.

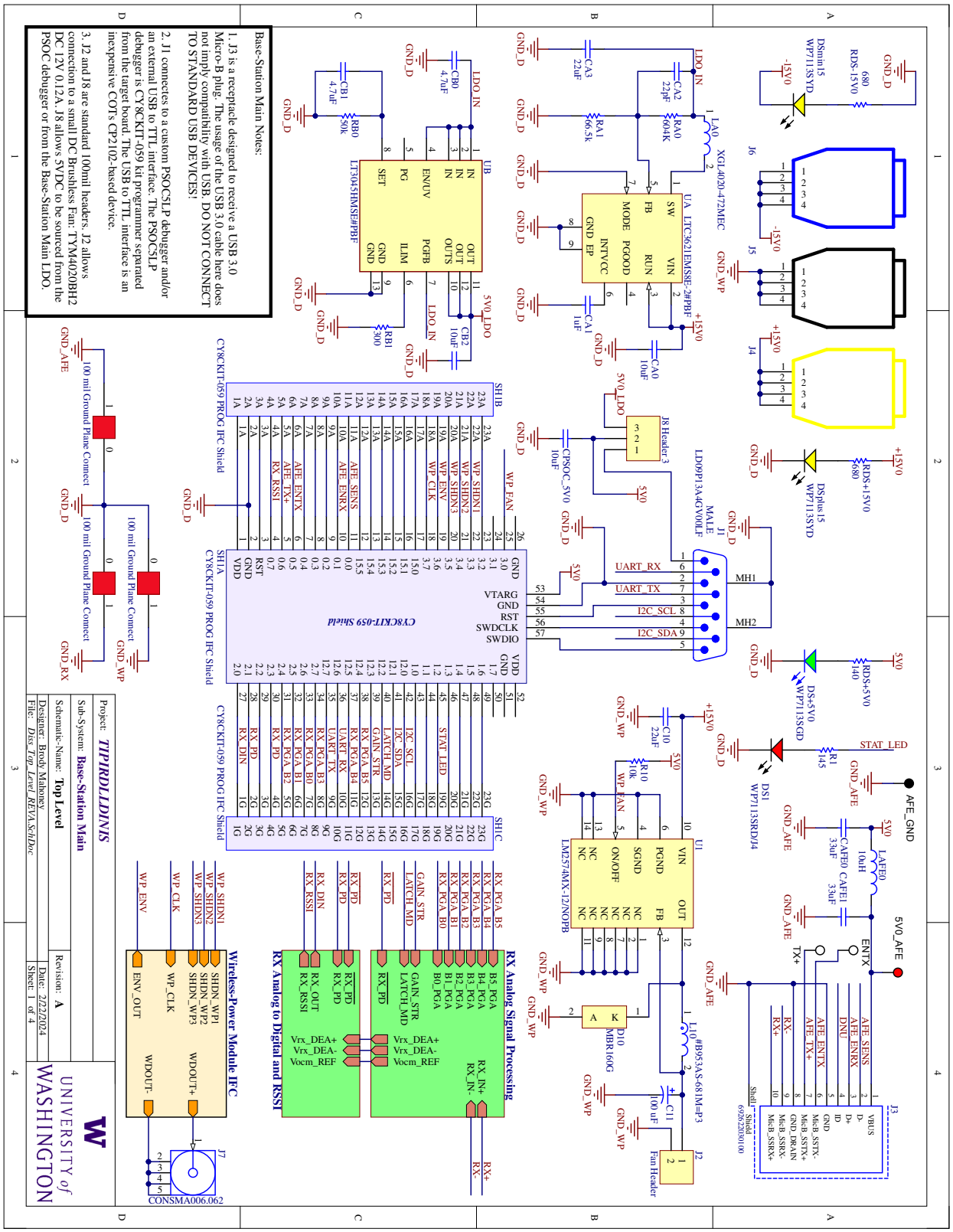
BS-DIFC Base Station Developer IFC.

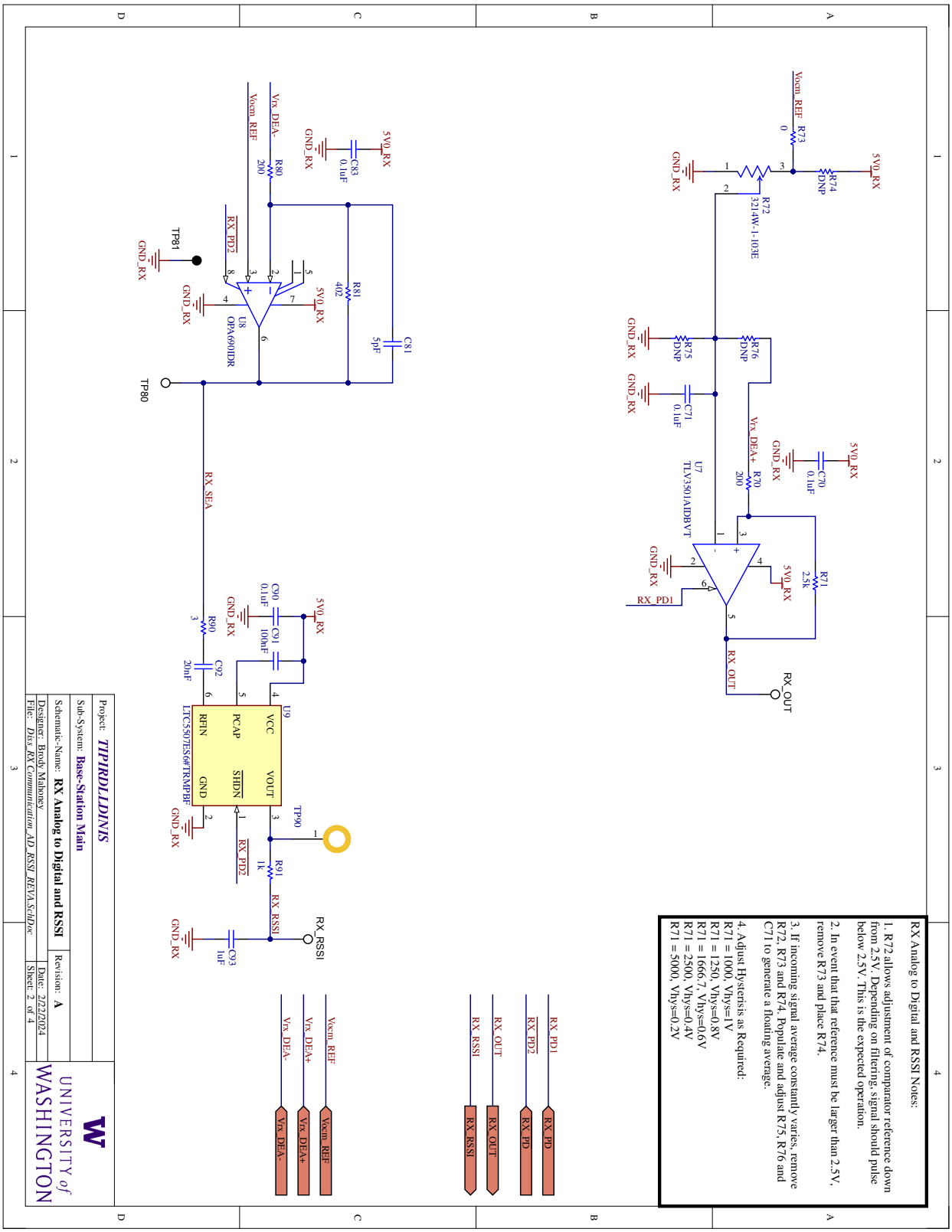
IMP-NIN Implant Neural Interface & NVM.

IMP-SC Implant System Control.

IMP-WPIR Implant Wireless Power.

IMP-DIFC Implant Developer IFC.


Base-Station Main Notes:
1. J3 is a receptacle designed to receive a USB 3.0 Micro-B plug. The usage of the USB 3.0 cable here does not imply compatibility with USB. DO NOT CONNECT TO STANDARD USB DEVICES!
2. J1 connectes to a custom PSOC5LP debugger and/or an external USB to TTL interface. The PSOC5LP debugger is CY8CKIT-059 kit programmer separated from the target board. The USB to TTL interface is an inexpensive COTs CP2102-based device.
3. J2 and J8 are standard 100mil headers. J2 allows connection to a small DC Brushless Fan: TYM4020BH2 DC 12V 0.12A. J8 allows 5VDC to be sourced from the PSOC debugger or from the Base-Station Main LDO.
CY8CKIT-059 Shield
RX Analog Signal Processing
RX Analog to Digital and RSSI
Wireless-Power Module IFC
Project: TIPIRDLLDINS
Sub-System: Base-Station Main
Schematic-Name: Top Level
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Dss_Top_Level_REVA.SchDoc
Sheet: 1 of 4
UNIVERSITY of WASHINGTON


RX Analog to Digital and RSSI Notes:
1. R72 allows adjustment of comparator reference down from 2.5V. Depending on filtering, signal should pulse below 2.5V. This is the expected operation.
2. In event that that reference must be larger than 2.5V, remove R73 and place R74.
3. If incoming signal average constantly varies, remove R72, R73 and R74. Populate and adjust R75, R76 and C71 to generate a floating average.
4. Adjust Hysterisis as Required:
R71 = 1000, Vhys=1V
R71 = 1250, Vhys=0.8V
R71 = 1666.7, Vhys=0.6V
R71 = 2500, Vhys=0.4V
R71 = 5000, Vhys=0.2V
5V0_RX
Vocm_REF
R73
0
R74
DNP
GND_RX
R72
3214W-1-103E
R75
DNP
R76
DNP
C71
0.1uF
Vrx_DEA+
R70
200
C70
0.1uF
U7
TLV3501AIDBVT
RX_PD1
R71
2.5k
RX_OUT
RX_OUT
C83
0.1uF
Vrx_DEA-
R80
200
R81
402
C81
5pF
RX_PD2
U8
OPA690IDR
TP81
TP80
RX_SEA
C90
0.1uF
C91
100nF
R90
20nF
C92
U9
LTC5507ES6#TRMPBF
VCC
PCAP
RFIN
GND
VOUT
SHDN
TP90
R91
1k
C93
1uF
RX_RSSI
RX_PD
RX_PD2
RX_OUT
RX_RSSI
Vocm_REF
Vrx_DEA+
Vrx_DEA-
Project: TIPIRDLLDINS
Sub-System: Base-Station Main
Schematic-Name: RX Analog to Digital and RSSI
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Dins_RX Communication_AD_RSSI_REVA.SchDoc
Sheet 2 of 4
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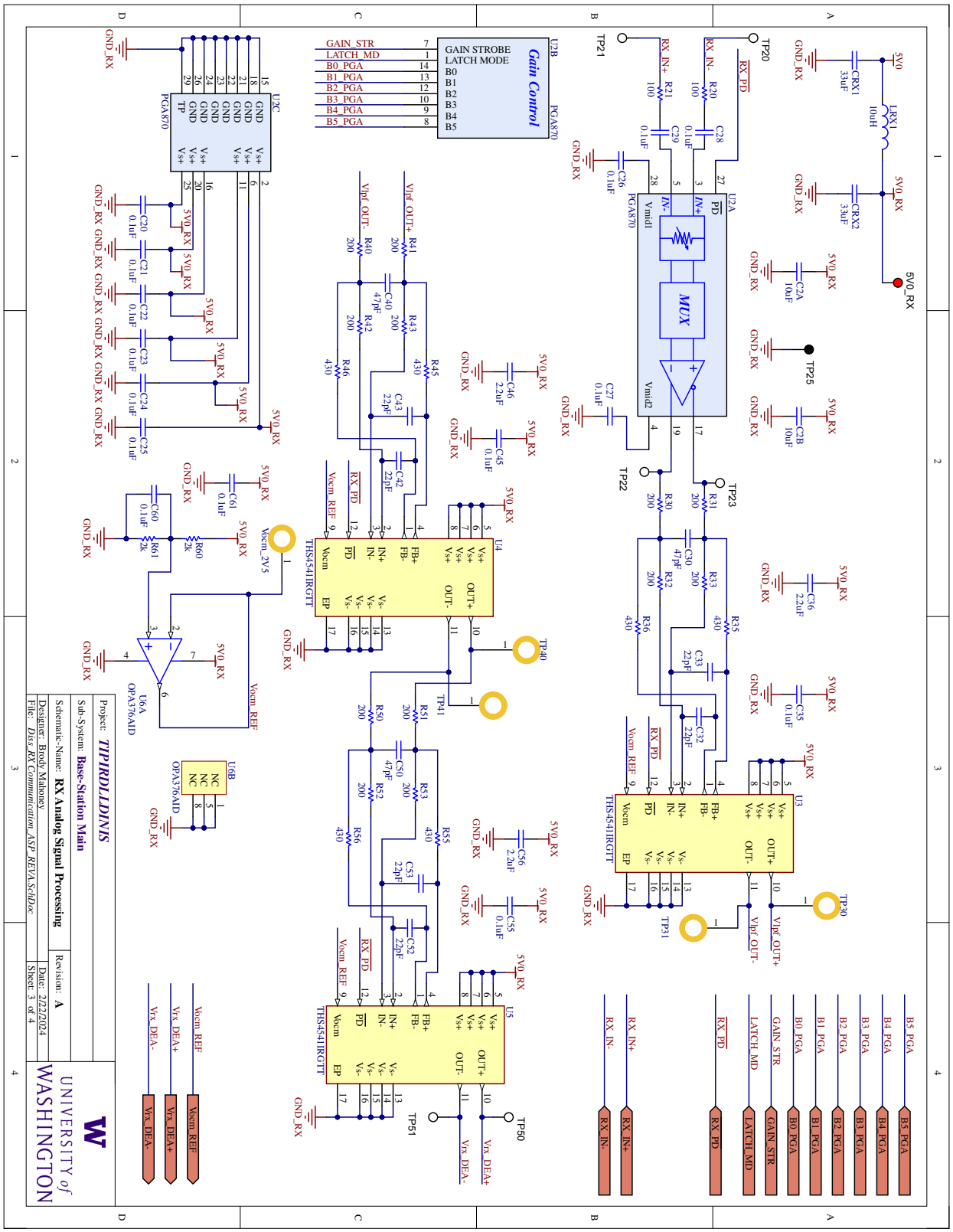
5V0
5V0_RX
LRX1
10uH
CRX1
33uF
CRX2
33uF
GND_RX
TP20
RX_PD
RX_IN-
RX_IN+
R20
100
R21
100
C28
0.1uF
C29
0.1uF
C26
0.1uF
U2A
PGA870
PD
IN+
IN-
Vmid1
Vmid2
MUX
TP21
TP22
TP23
TP25
C27
0.1uF
C2A
10uF
C2B
10uF
R30
200
R31
200
R32
200
R33
200
R35
430
R36
430
C30
47pF
C32
22pF
C33
22pF
C35
0.1uF
C36
2.2uF
U3
THS4541IRGTT
Vocm_REF
RX_PD
Vinf_OUT+
Vinf_OUT-
TP30
TP31
B5_PGA
B4_PGA
B3_PGA
B2_PGA
B1_PGA
B0_PGA
GAIN_STR
LATCH_MD
RX_PD
RX_IN+
RX_IN-
U2B
Gain Control
GAIN STROBE
LATCH MODE
B0
B1
B2
B3
B4
B5
GAIN_STR
LATCH_MD
B0_PGA
B1_PGA
B2_PGA
B3_PGA
B4_PGA
B5_PGA
U2C
TP
GND
Vs+
Vocm_2V5
R60
2k
R61
2k
C60
0.1uF
C61
0.1uF
U6A
OPA376AID
U6B
NC
C20
C21
C22
C23
C24
C25
0.1uF
R40
200
R41
200
R42
200
R43
200
R45
430
R46
430
C40
47pF
C42
22pF
C43
22pF
C45
0.1uF
C46
2.2uF
U4
R50
200
R51
200
R52
200
R53
200
R55
430
R56
430
C50
47pF
C52
22pF
C53
22pF
C55
0.1uF
C56
2.2uF
U5
TP40
TP41
TP50
TP51
Vrx_DEA+
Vrx_DEA-
Vocm_REF
Project: TIPIRDLLDINIS
Sub-System: Base-Station Main
Schematic-Name: RX Analog Signal Processing
Designer: Brody Mahoney
File: Dinx_RX Communication_ASP_REVA.SchDoc
Revision: A
Date: 2/22/2024
Sheet 3 of 4
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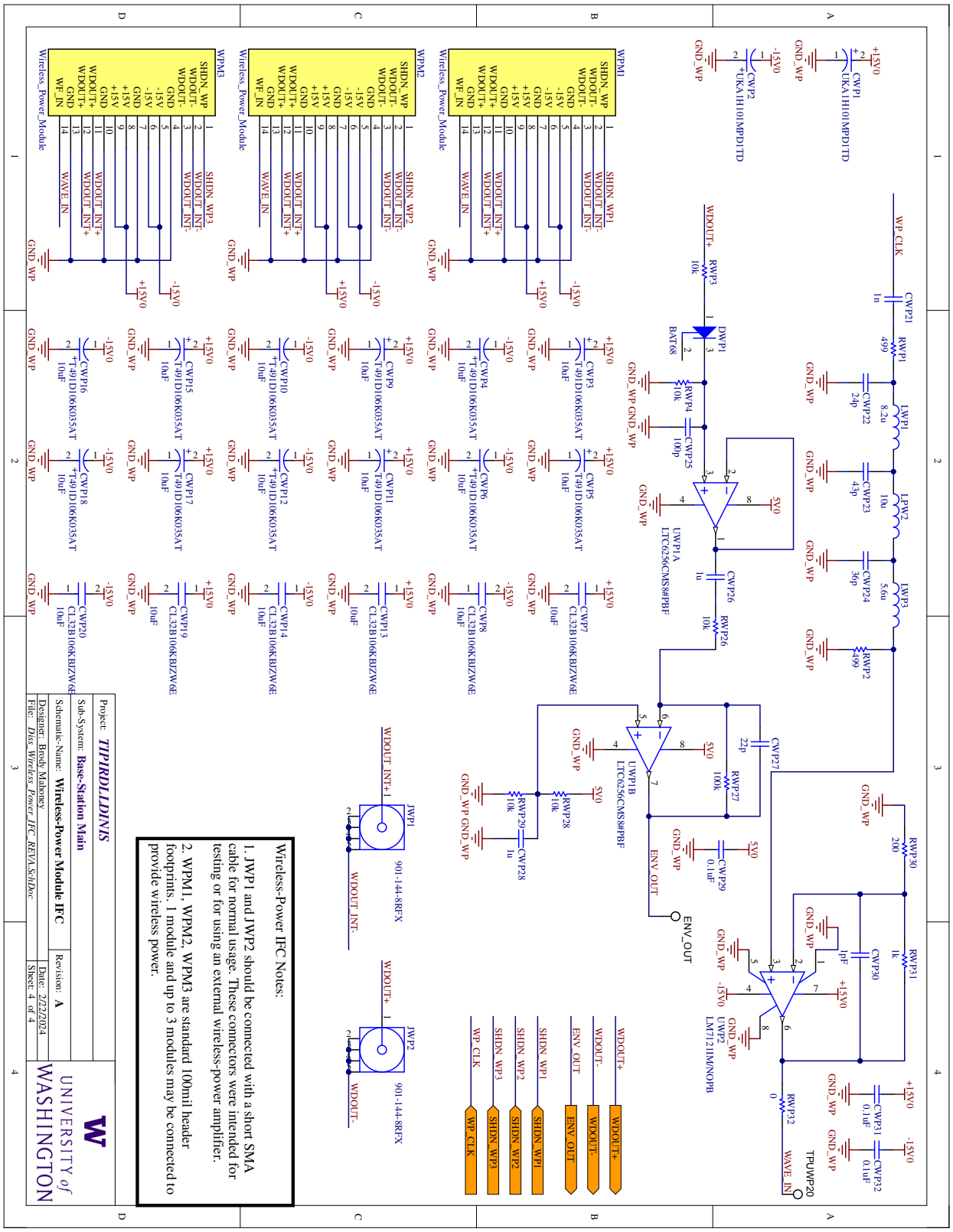
Wireless-Power IFC Notes:
1. JWP1 and JWP2 should be connected with a short SMA cable for normal usage. These connectors were intended for testing or for using an external wireless-power amplifier.
2. WPM1, WPM2, WPM3 are standard 100mil header footprints. 1 module and up to 3 modules may be connected to provide wireless power.
Project: TIPIRDLLDINS
Sub-System: Base-Station Main
Schematic-Name: Wireless-Power Module IFC
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Diss_Wireless_Power_IFC_REVA.SchDoc
Sheet: 4 of 4
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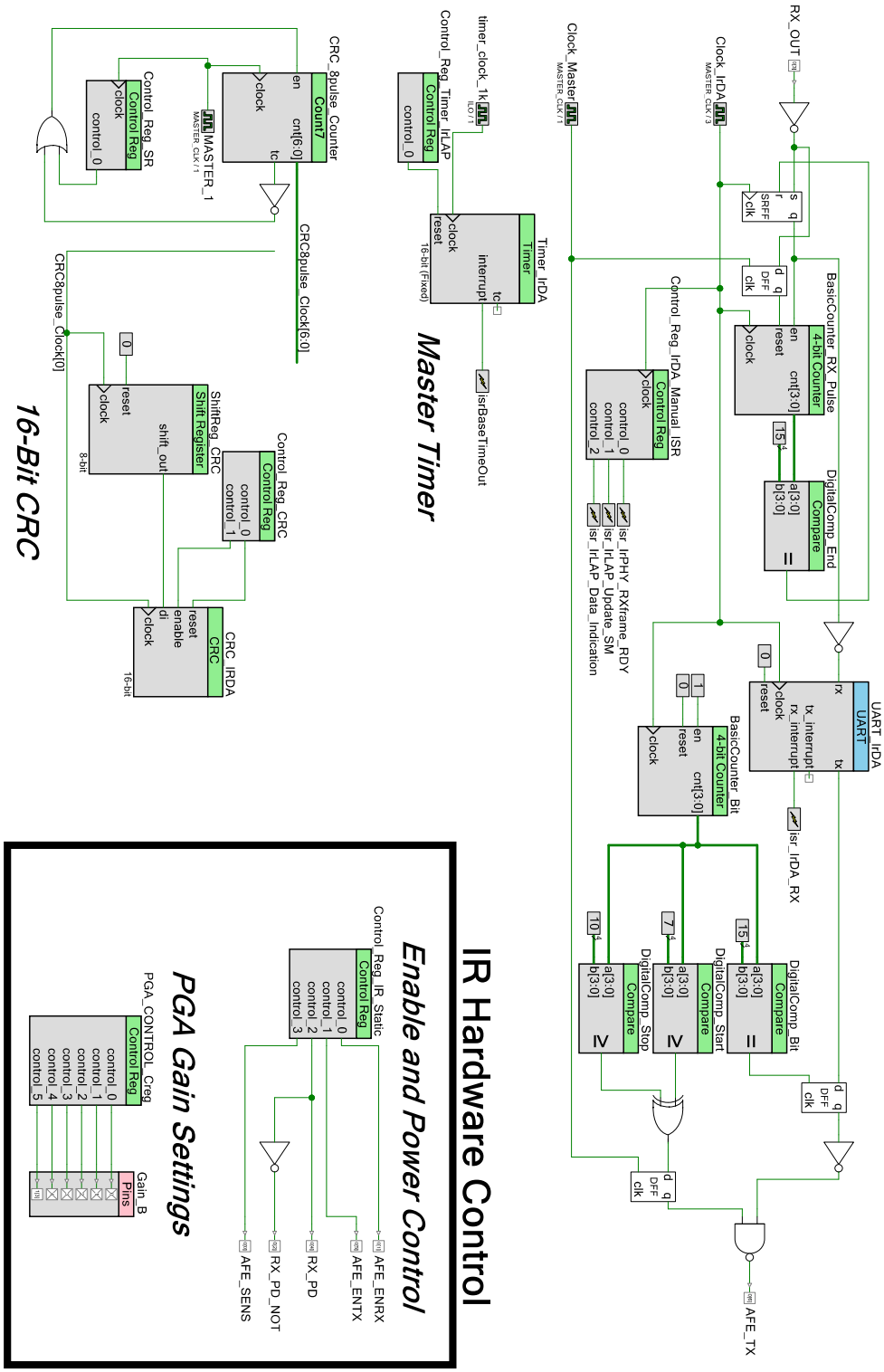
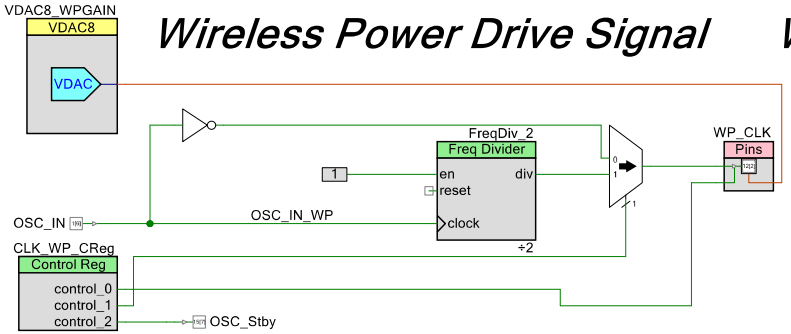
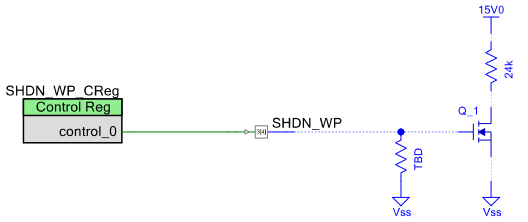

IrDA Async Machine
RX_OUT
Clock_IrDA_1M
Clock_Master_1M
UART_IrDA
UART
BasicCounter_RX_Pulse
4-bit Counter
DigitalComp_End
Compare
Control_Reg_IrDA_Manual_ISR
Control Reg
isr_IrPHY_RXframe_RDY
isr_IrLAP_Update_SM
isr_IrLAP_Data_Indication
isr_IrDA_RX
BasicCounter_Bit
DigitalComp_Bit
DigitalComp_Start
DigitalComp_Stop
AFE_TX
Timer_IrDA
Timer
timer_clock_1k
Control_Reg_Timer_IrLAP
isrBaseTimeOut
Master Timer
CRC_8pulse_Counter
Count7
MASTER_1
Control_Reg_SR
CRC8pulse_Clock[6:0]
CRC8pulse_Clock[0]
ShiftReg_CRC
Shift Register
Control_Reg_CRC
CRC_IRDA
CRC
16-Bit CRC
IR Hardware Control
Enable and Power Control
Control_Reg_IR_Static
AFE_ENRX
AFE_ENTX
RX_PD
RX_PD_NOT
AFE_SENS
PGA Gain Settings
PGA_CONTROL_Creg
Gain_B
Pins

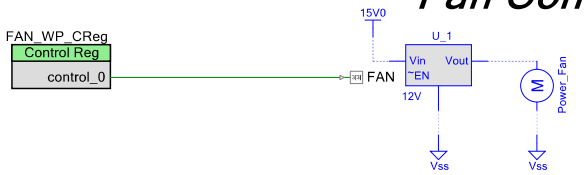
Wireless Power Drive Signal



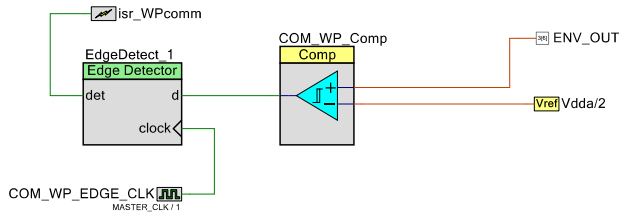
Wireless Power Module Shutdown

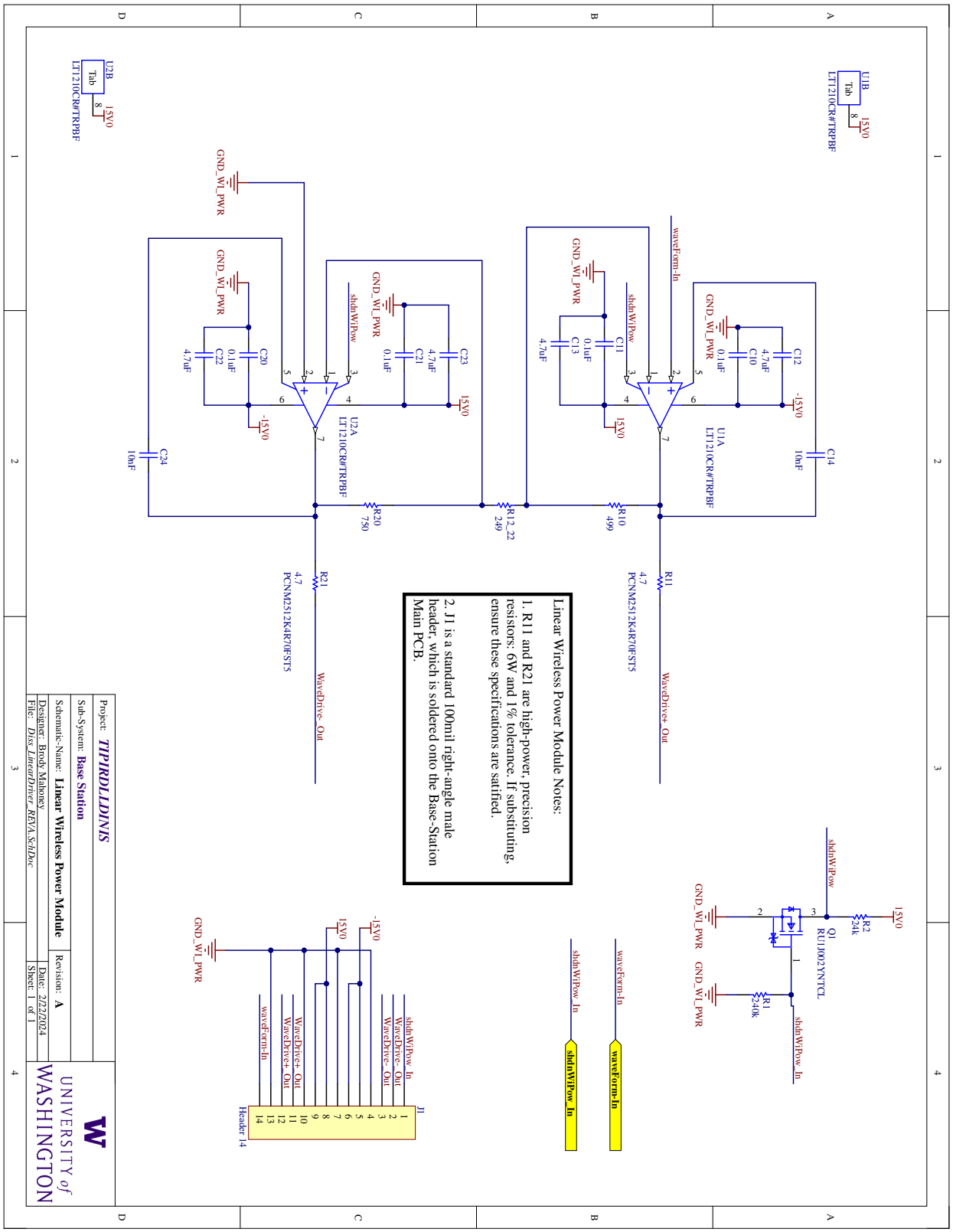


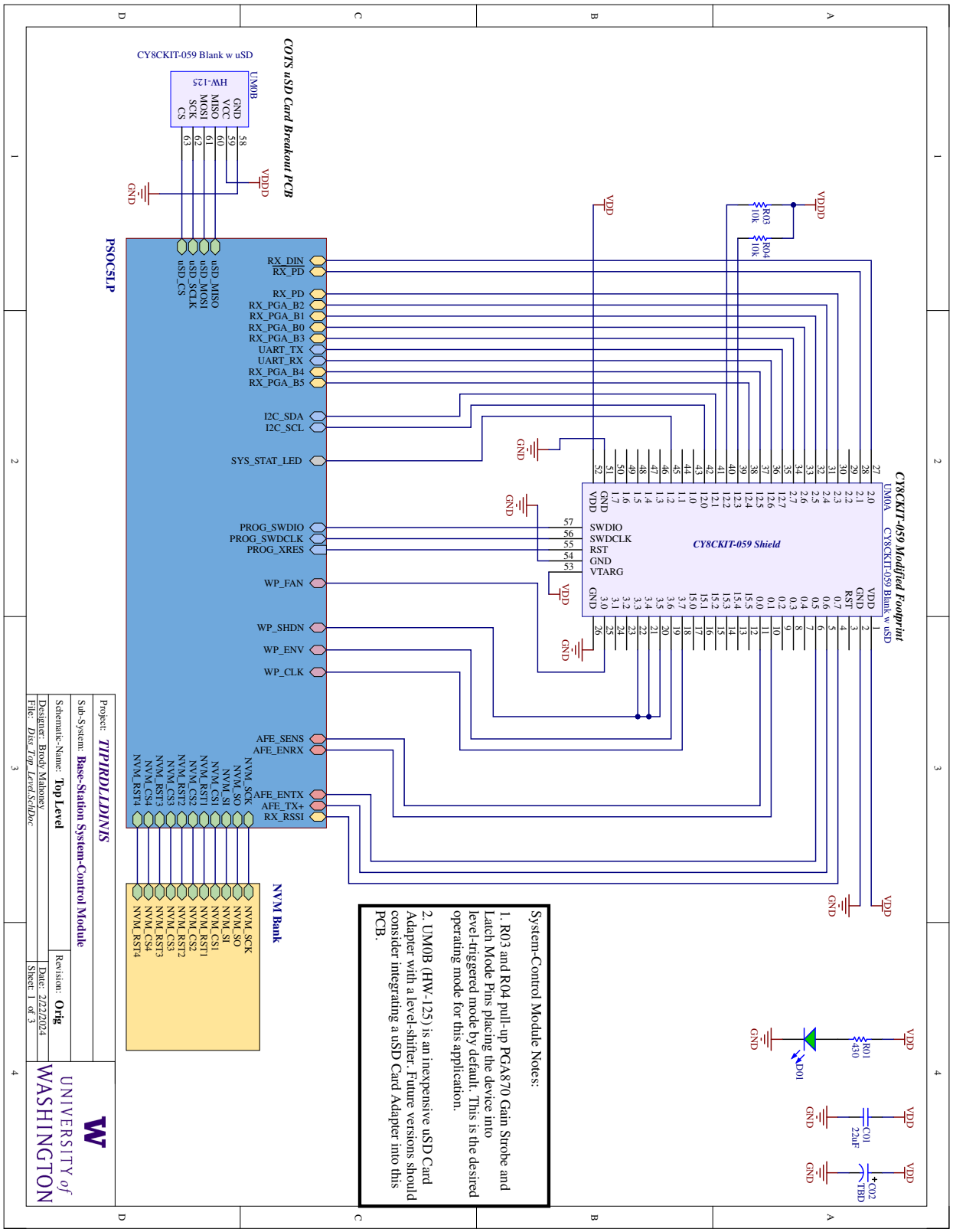
Fan Control



Wireless Power Envelope Detector




Linear Wireless Power Module Notes:
1. R11 and R21 are high-power, precision resistors: 6W and 1% tolerance. If substituting, ensure these specifications are satified.
2. J1 is a standard 100mil right-angle male header, which is soldered onto the Base-Station Main PCB.
Project: TIPIRDLLDINS
Sub-System: Base Station
Schematic-Name: Linear Wireless Power Module
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Diss_LinearDriver_REVA.SchDoc
Sheet 1 of 1
UNIVERSITY of WASHINGTON
U1A
LT1210CR#TRPBF
U1B
LT1210CR#TRPBF
U2A
LT1210CR#TRPBF
U2B
LT1210CR#TRPBF
Q1
RUJ1002YNTCL
J1
Header 14
waveForm-In
shdnWiPow
shdnWiPow_In
WaveDrive+ Out
WaveDrive- Out
GND_WI_PWR
15V0
-15V0


CY8CKIT-059 Blank w uSD
UM0B
HW-125
GND
VCC
MISO
MOSI
SCK
CS
COTS uSD Card Breakout PCB
PSOC5LP
RX_DIN
RX_PD
RX_PGA_B2
RX_PGA_B1
RX_PGA_B0
RX_PGA_B3
UART_TX
UART_RX
RX_PGA_B4
RX_PGA_B5
I2C_SDA
I2C_SCL
SYS_STAT_LED
PROG_SWDIO
PROG_SWDCLK
PROG_XRES
WP_FAN
WP_SHDN
WP_ENV
WP_CLK
AFE_SENS
AFE_ENRX
AFE_ENTX
AFE_TX+
RX_RSSI
uSD_MISO
uSD_MOSI
uSD_SCLK
uSD_CS
NVM_SCK
NVM_SO
NVM_SI
NVM_CS1
NVM_RST1
NVM_CS2
NVM_RST2
NVM_CS3
NVM_RST3
NVM_CS4
NVM_RST4
NVM Bank
CY8CKIT-059 Modified Footprint
UM0A
CY8CKIT-059 Blank w uSD
CY8CKIT-059 Shield
SWDIO
SWDCLK
RST
GND
VTARG
VDDD
VDD
R03
10k
R04
10k
R01
430
D01
C01
22uF
C02
TBD
System-Control Module Notes:
1. R03 and R04 pull-up PGA870 Gain Strobe and Latch Mode Pins placing the device into level-triggered mode by default. This is the desired operating mode for this application.
2. UM0B (HW-125) is an inexpensive uSD Card Adapter with a level-shifter. Future versions should consider integrating a uSD Card Adapter into this PCB.
Project: TIPIRDLLDINS
Sub-System: Base-Station System-Control Module
Schematic-Name: Top Level
Revision: Orig
Designer: Brody Mahoney
Date: 2/22/2024
File: Diss_Top_Level.SchDoc
Sheet 1 of 3
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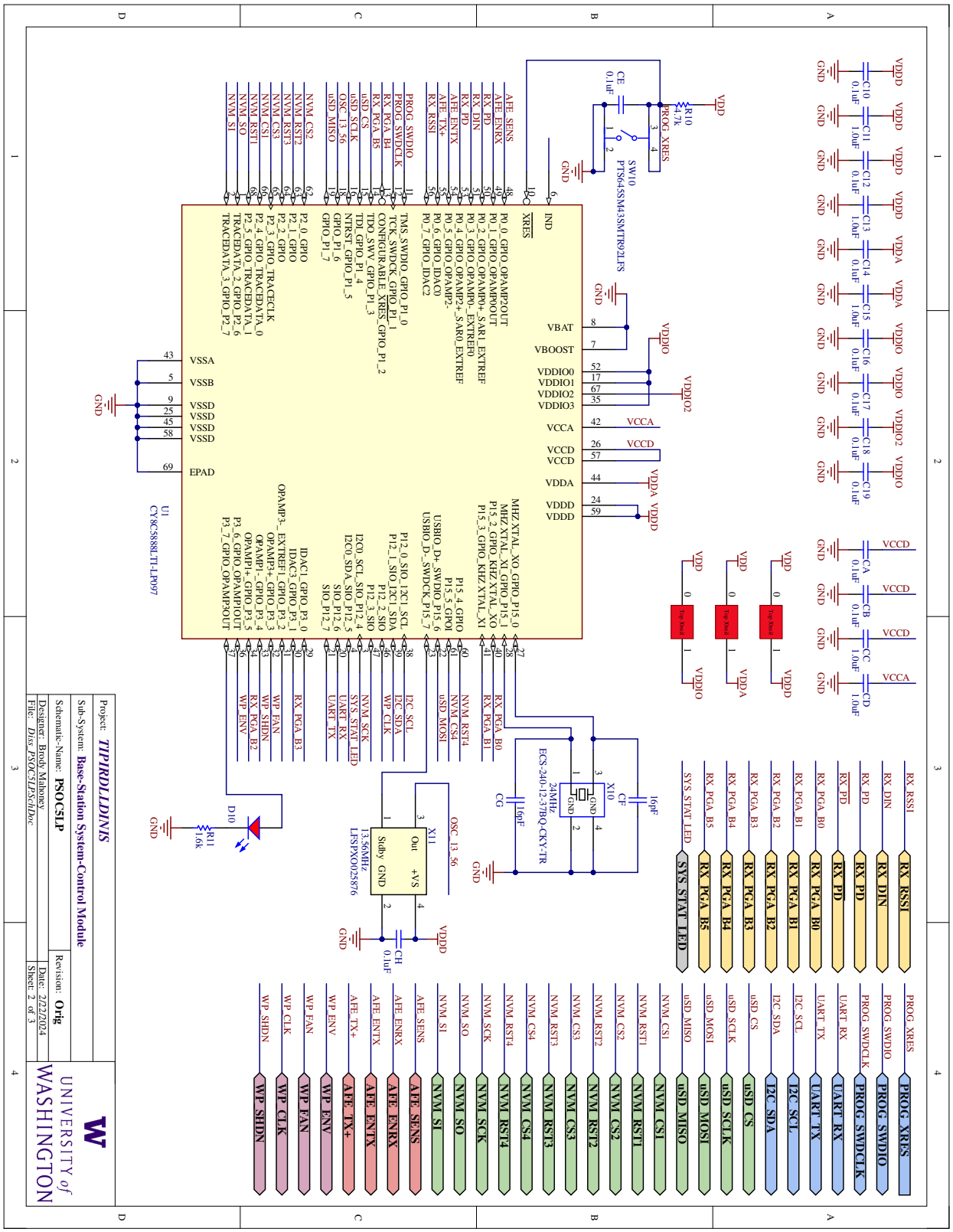
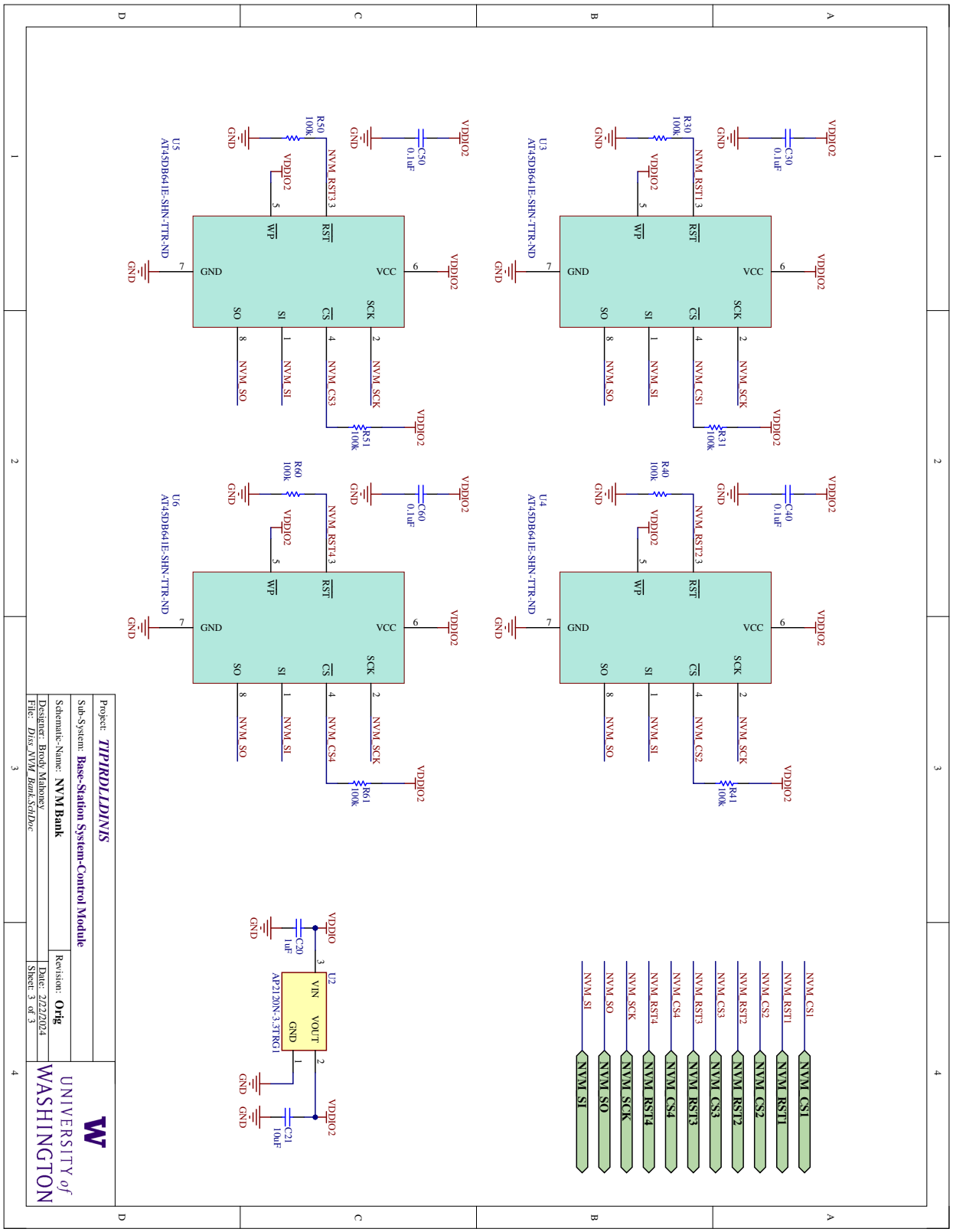
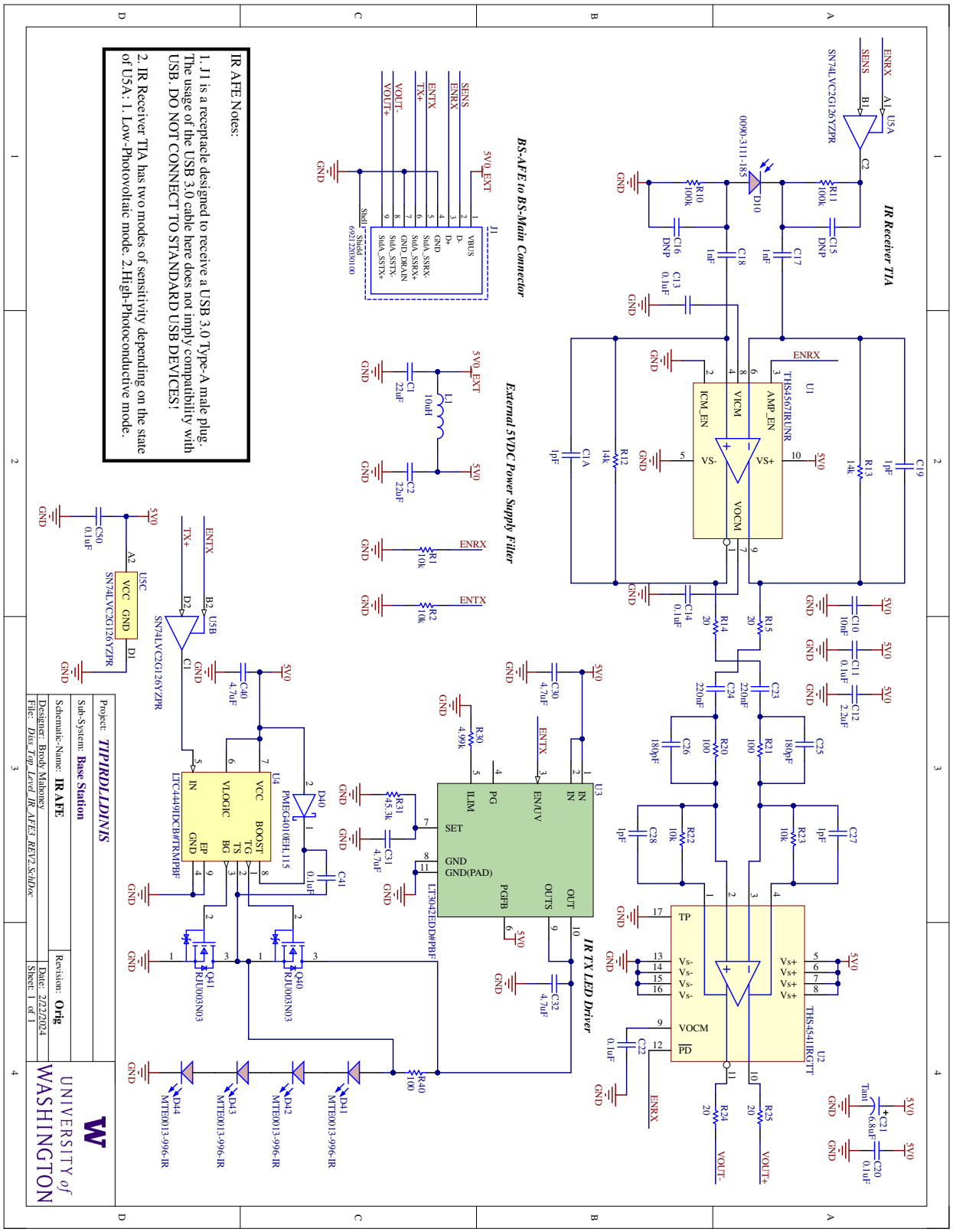
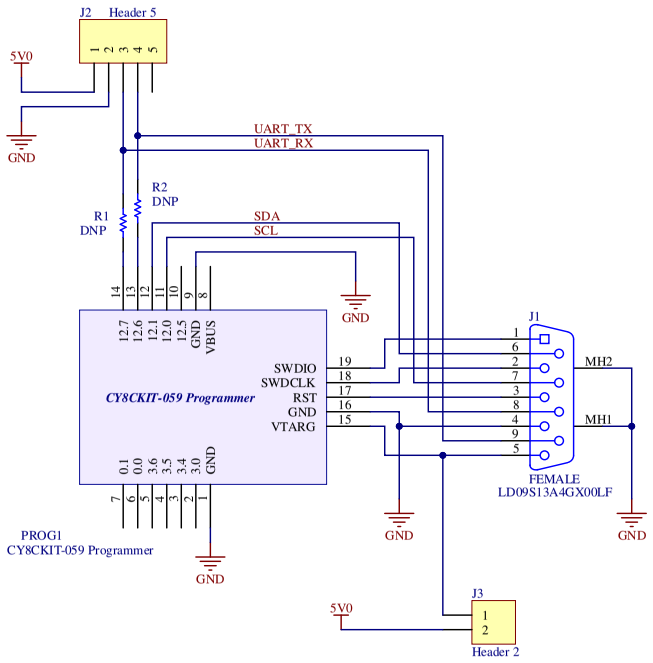

PROG_XRES
PROG_SWDIO
PROG_SWDCLK
UART_RX
UART_TX
I2C_SCL
I2C_SDA
uSD_CS
uSD_SCLK
uSD_MOSI
uSD_MISO
NVM_CS1
NVM_RST1
NVM_CS2
NVM_RST2
NVM_CS3
NVM_RST3
NVM_CS4
NVM_RST4
NVM_SCK
NVM_SO
NVM_SI
AFE_SENS
AFE_ENRX
AFE_ENTX
AFE_TX+
WP_ENV
WP_FAN
WP_CLK
WP_SHDN
RX_RSSI
RX_DIN
RX_PD
RX_PGA_B0
RX_PGA_B1
RX_PGA_B2
RX_PGA_B3
RX_PGA_B4
RX_PGA_B5
SYS_STAT_LED
U1
CY8C5888LTI-LP097
X10
24MHz
ECS-240-12-37BQ-CKY-TR
X11
13.56MHz
LFSPXO025876
D10
R11
1.6k
R10
4.7k
SW10
PTS645SM43SMTR92LFS
CE
0.1uF
CF
16pF
CG
16pF
CH
0.1uF
VDDD
VDDA
VDDIO
VDDIO2
VCCA
VCCD
GND
Project: TIPIRDLLDINS
Sub-System: Base-Station System-Control Module
Schematic-Name: PSOC5LP
Revision: Orig
Designer: Brody Mahoney
Date: 2/22/2024
File: Disc PSOC5LPSchDoc
Sheet 2 of 3
UNIVERSITY of WASHINGTON


U3
AT45DB641E-SHN-TTR-ND
U4
AT45DB641E-SHN-TTR-ND
U5
AT45DB641E-SHN-TTR-ND
U6
AT45DB641E-SHN-TTR-ND
U2
AP2120N-3.3TRG1
VDDIO2
VDDIO
GND
VCC
WP
RST
SCK
CS
SI
SO
VIN
VOUT
NVM_CS1
NVM_RST1
NVM_CS2
NVM_RST2
NVM_CS3
NVM_RST3
NVM_CS4
NVM_RST4
NVM_SCK
NVM_SO
NVM_SI
Project: TIPIRDLLDINS
Sub-System: Base-Station System-Control Module
Schematic-Name: NVM Bank
Designer: Brody Mahoney
File: Diss_NVM_Bank.SchDoc
Revision: Orig
Date: 2/22/2024
Sheet 3 of 3
UNIVERSITY of WASHINGTON


IR AFE Notes:
1. J1 is a receptacle designed to receive a USB 3.0 Type-A male plug. The usage of the USB 3.0 cable here does not imply compatibility with USB. DO NOT CONNECT TO STANDARD USB DEVICES!
2. IR Receiver TIA has two modes of sensitivity depending on the state of U5A: 1. Low-Photovoltaic mode. 2.High-Photoconductive mode.
IR Receiver TIA
BS-AFE to BS-Main Connector
External 5VDC Power Supply Filter
IR TX LED Driver
SN74LVC2G126YZPR
0090-3111-185
THS4567IRUNR
THS4541IRGTT
LTC4449IDCB#TRMPBF
LT3042EDD#PBF
PMEG4010EH,115
RJU003N03
MTE0013-996-IR
J1
Project: TIPIRDLLDINIS
Sub-System: Base Station
Schematic-Name: IR AFE
Revision: Orig
Designer: Brody Mahoney
Date: 2/22/2024
File: Dss Top Level IR AFE3 REV2.SchDoc
Sheet: 1 of 1
UNIVERSITY of WASHINGTON



PSOC5LP Program and Serial Notes:

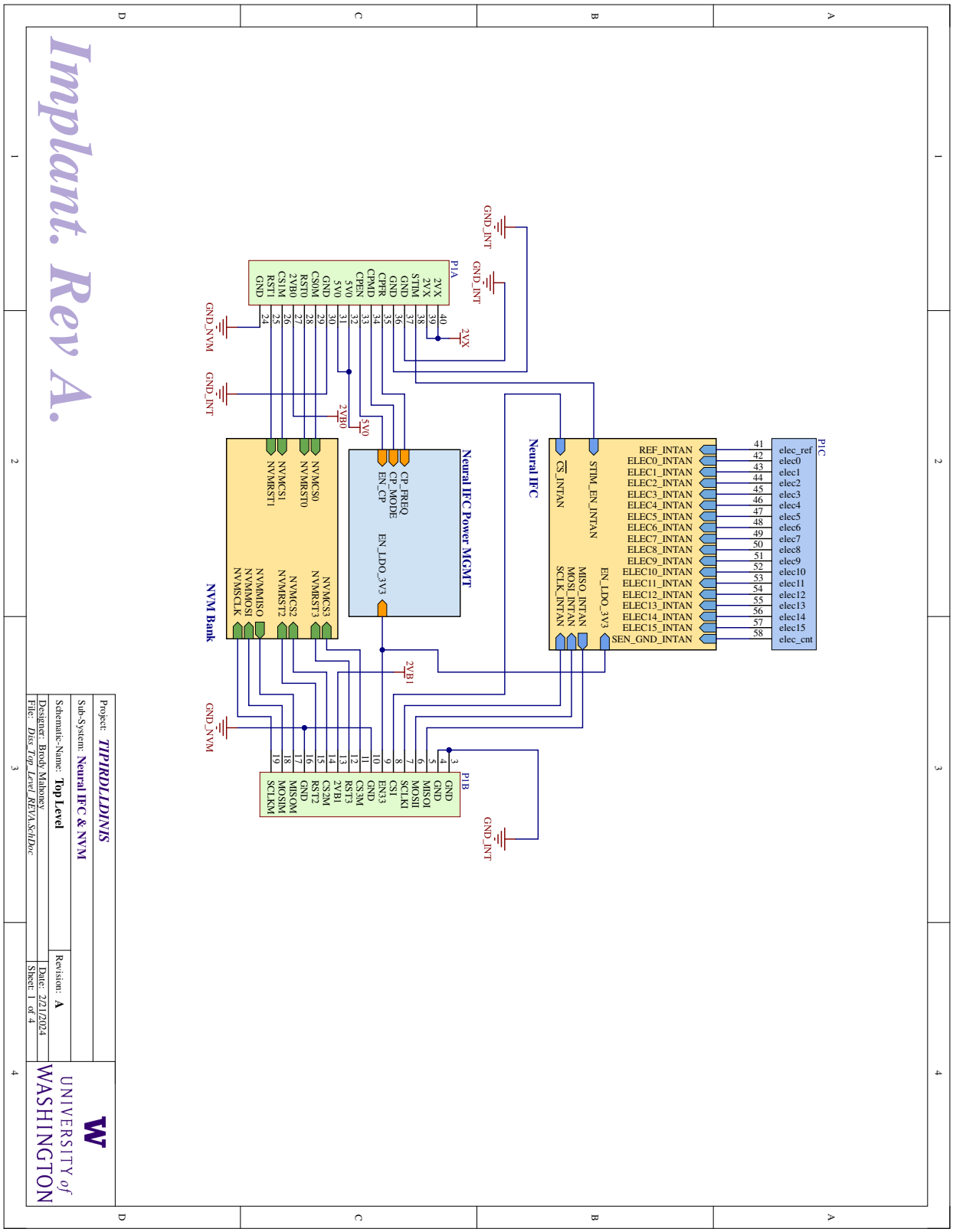
1. PROG1 footprint uses standard 100mil headers. The footprint is designed so that the separated CY8CKIT-Programmer portion can be soldered to this PCB.

2. J2 is a standard 100mil header. J2 allows connection of an inexpensive USB to Serial device: HiLetgo CP2102 USB 2.0 to TTL Module.

3. R1 and R2 may be populated with 0 ohm resistors in the event the user wants to use the CY8CKIT-059 built-in UART-Serial device. However this connection has been highly unreliable in this application.

Project: *TIPIRDLLDINIS*		
Sub-System: **Base-Station Developer IFC**		
Schematic-Name: **PSOC5LP Program and Serial**	Revision: **Orig**	
Designer: Brody Mahoney	Date: 2/22/2024	
File: *Diss_PSOC5LP_Programmer.SchDoc*	Sheet: 1 of 1	

UNIVERSITY of WASHINGTON


Implant. Rev A.
P1A
2VX
2VX
STIM
GND
GND
CPFR
CPMD
CPEN
5V0
5V0
GND
CS0M
RST0
2VB0
CS1M
RST1
GND
P1C
REF_INTAN
ELEC0_INTAN
ELEC1_INTAN
ELEC2_INTAN
ELEC3_INTAN
ELEC4_INTAN
ELEC5_INTAN
ELEC6_INTAN
ELEC7_INTAN
ELEC8_INTAN
ELEC9_INTAN
ELEC10_INTAN
ELEC11_INTAN
ELEC12_INTAN
ELEC13_INTAN
ELEC14_INTAN
ELEC15_INTAN
SEN_GND_INTAN
elec_ref
elec0
elec1
elec2
elec3
elec4
elec5
elec6
elec7
elec8
elec9
elec10
elec11
elec12
elec13
elec14
elec15
elec_cnt
Neural IFC
STIM_EN_INTAN
CS_INTAN
EN_LDO_3V3
MISO_INTAN
MOSI_INTAN
SCLK_INTAN
Neural IFC Power MGMT
CP_FREQ
CP_MODE
EN_CP
EN_LDO_3V3
NVM Bank
NVMCS0
NVMRST0
NVMCS1
NVMRST1
NVMCS3
NVMRST3
NVMCS2
NVMRST2
NVMMISO
NVMMOSI
NVMSCLK
P1B
GND
GND
MISOI
MOSII
SCLKI
CSI
EN33
GND
CS3M
RST3
2VB1
CS2M
RST2
GND
MISOM
MOSIM
SCLKM
GND_INT
GND_NVM
2VX
2VB0
5V0
2VB1
Project: TIPIRDLLDINS
Sub-System: Neural IFC & NVM
Schematic-Name: Top Level
Revision: A
Designer: Brody Mahoney
Date: 2/21/2024
File: Diss_Top_Level_REVA.SchDoc
Sheet 1 of 4
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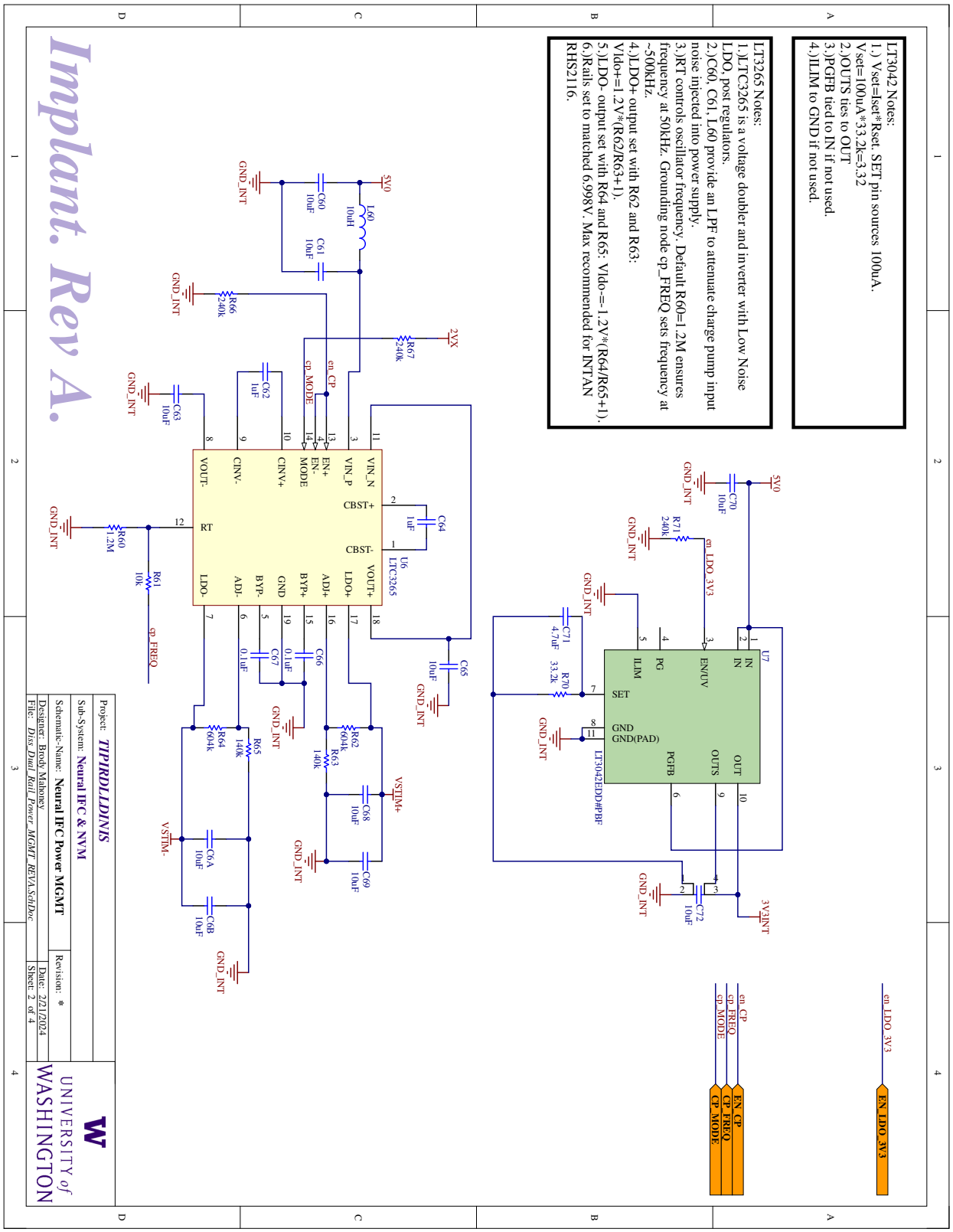
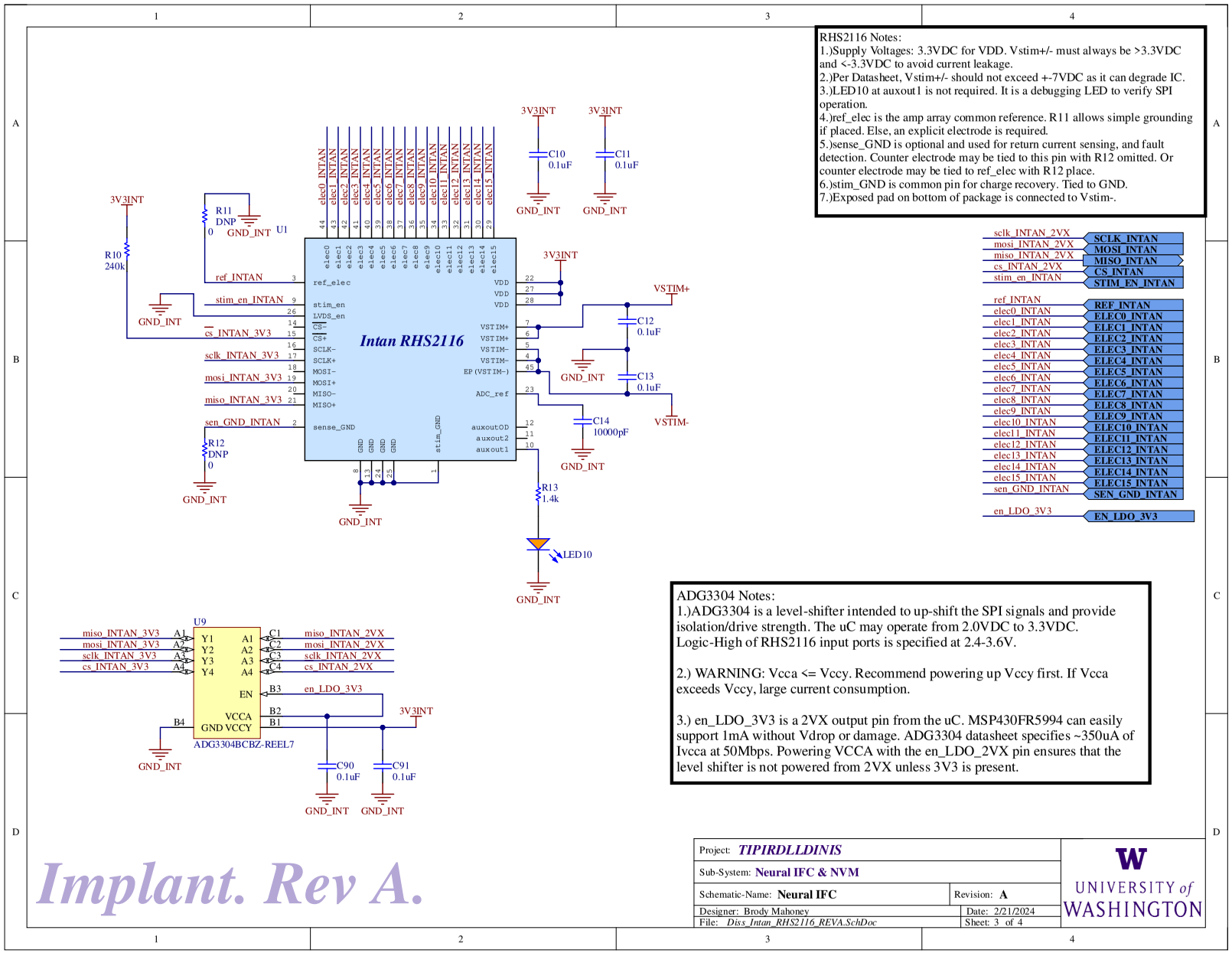

LT3042 Notes:
1.) Vset=Iset*Rset. SET pin sources 100uA.
Vset=100uA*33.2k=3.32
2.)OUTS ties to OUT
3.)PGFB tied to IN if not used.
4.)ILIM to GND if not used.
LT3265 Notes:
1.)LTC3265 is a voltage doubler and inverter with Low Noise LDO, post regulators.
2.)C60, C61, L60 provide an LPF to attenuate charge pump input noise injected into power supply.
3.)RT controls oscillator frequency. Default R60=1.2M ensures frequency at 50kHz. Grounding node cp_FREQ sets frequency at ~500kHz.
4.)LDO+ output set with R62 and R63:
Vldo+=1.2V*(R62/R63+1).
5.)LDO- output set with R64 and R65: Vldo=-1.2V*(R64/R65+1).
6.)Rails set to matched 6.998V. Max recommended for INTAN RHS2116.
Implant. Rev A.
EN_LDO_3V3
EN_CP
CP_FREQ
CP_MODE
U7
LT3042EDD#PBF
LTC3265
5V0
2VX
3V3INT
GND_INT
VSTIM+
VSTIM-
Project: TIPIRDLLDINS
Sub-System: Neural IFC & NVM
Schematic-Name: Neural IFC Power MGMT
Designer: Brody Mahoney
File: Diss_Dual_Rail_Power_MGMT_REVA.SchDoc
Revision: *
Date: 2/21/2024
Sheet 2 of 4
UNIVERSITY of WASHINGTON


RHS2116 Notes:
1.)Supply Voltages: 3.3VDC for VDD. Vstim+/- must always be >3.3VDC and <-3.3VDC to avoid current leakage.
2.)Per Datasheet, Vstim+/- should not exceed +-7VDC as it can degrade IC.
3.)LED10 at auxout1 is not required. It is a debugging LED to verify SPI operation.
4.)ref_elec is the amp array common reference. R11 allows simple grounding if placed. Else, an explicit electrode is required.
5.)sense_GND is optional and used for return current sensing, and fault detection. Counter electrode may be tied to this pin with R12 omitted. Or counter electrode may be tied to ref_elec with R12 place.
6.)stim_GND is common pin for charge recovery. Tied to GND.
7.)Exposed pad on bottom of package is connected to Vstim-.
Intan RHS2116
U1
3V3INT
GND_INT
R10 240k
R11 DNP 0
R12 DNP 0
C10 0.1uF
C11 0.1uF
C12 0.1uF
C13 0.1uF
C14 10000pF
R13 1.4k
LED10
VSTIM+
VSTIM-
ref_INTAN
stim_en_INTAN
cs_INTAN_3V3
sclk_INTAN_3V3
mosi_INTAN_3V3
miso_INTAN_3V3
sen_GND_INTAN
sclk_INTAN_2VX
mosi_INTAN_2VX
miso_INTAN_2VX
cs_INTAN_2VX
stim_en_INTAN
SCLK_INTAN
MOSI_INTAN
MISO_INTAN
CS_INTAN
STIM_EN_INTAN
REF_INTAN
ELEC0_INTAN
ELEC1_INTAN
ELEC2_INTAN
ELEC3_INTAN
ELEC4_INTAN
ELEC5_INTAN
ELEC6_INTAN
ELEC7_INTAN
ELEC8_INTAN
ELEC9_INTAN
ELEC10_INTAN
ELEC11_INTAN
ELEC12_INTAN
ELEC13_INTAN
ELEC14_INTAN
ELEC15_INTAN
SEN_GND_INTAN
en_LDO_3V3
EN_LDO_3V3
ADG3304 Notes:
1.)ADG3304 is a level-shifter intended to up-shift the SPI signals and provide isolation/drive strength. The uC may operate from 2.0VDC to 3.3VDC. Logic-High of RHS2116 input ports is specified at 2.4-3.6V.
2.) WARNING: Vcca <= Vccy. Recommend powering up Vccy first. If Vcca exceeds Vccy, large current consumption.
3.) en_LDO_3V3 is a 2VX output pin from the uC. MSP430FR5994 can easily support 1mA without Vdrop or damage. ADG3304 datasheet specifies ~350uA of Ivcca at 50Mbps. Powering VCCA with the en_LDO_2VX pin ensures that the level shifter is not powered from 2VX unless 3V3 is present.
U9
ADG3304BCBZ-REEL7
C90 0.1uF
C91 0.1uF
Implant. Rev A.
Project: TIPIRDLLDINIS
Sub-System: Neural IFC & NVM
Schematic-Name: Neural IFC
Revision: A
Designer: Brody Mahoney
Date: 2/21/2024
File: Diss_Intan_RHS2116_REVA.SchDoc
Sheet: 3 of 4
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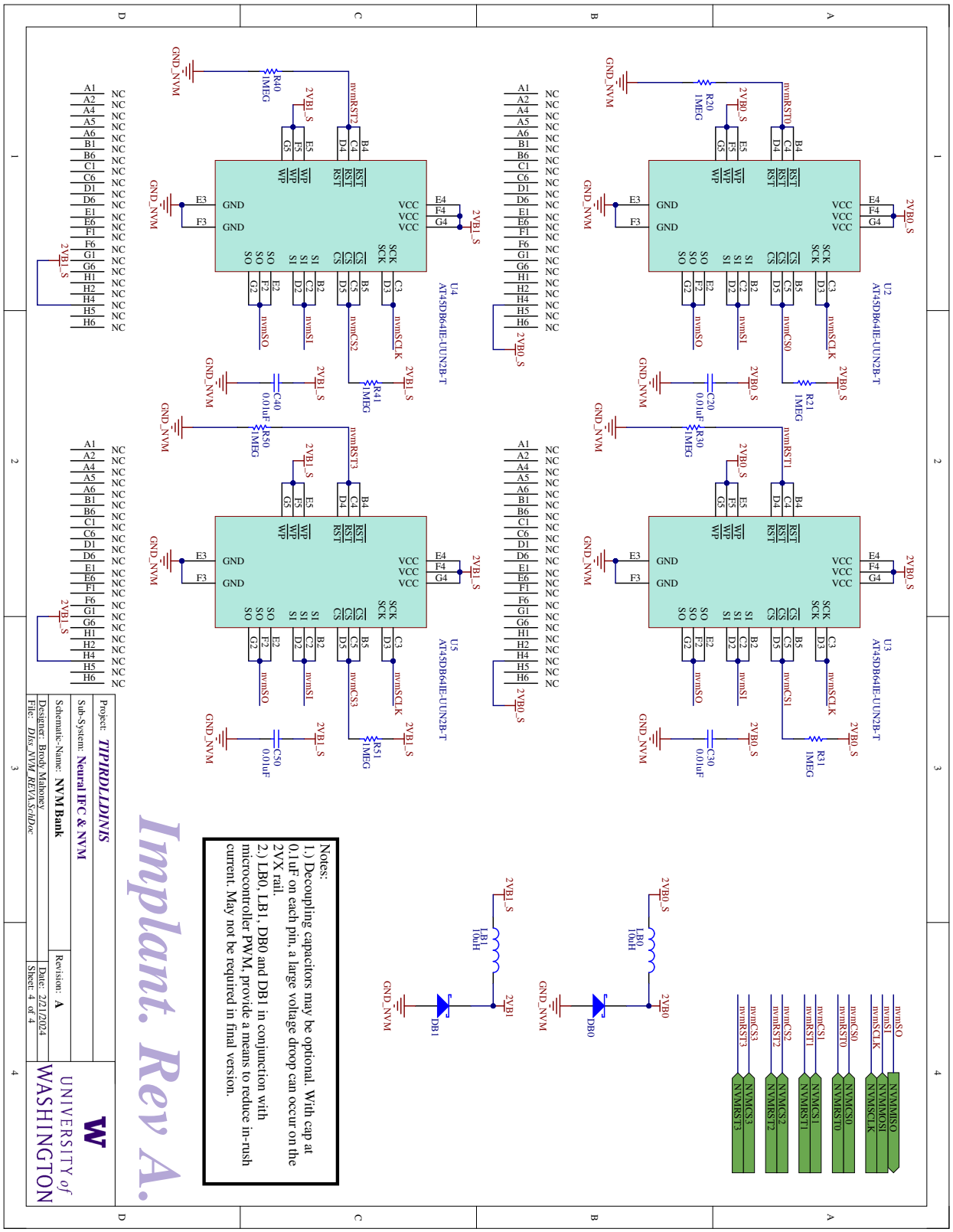
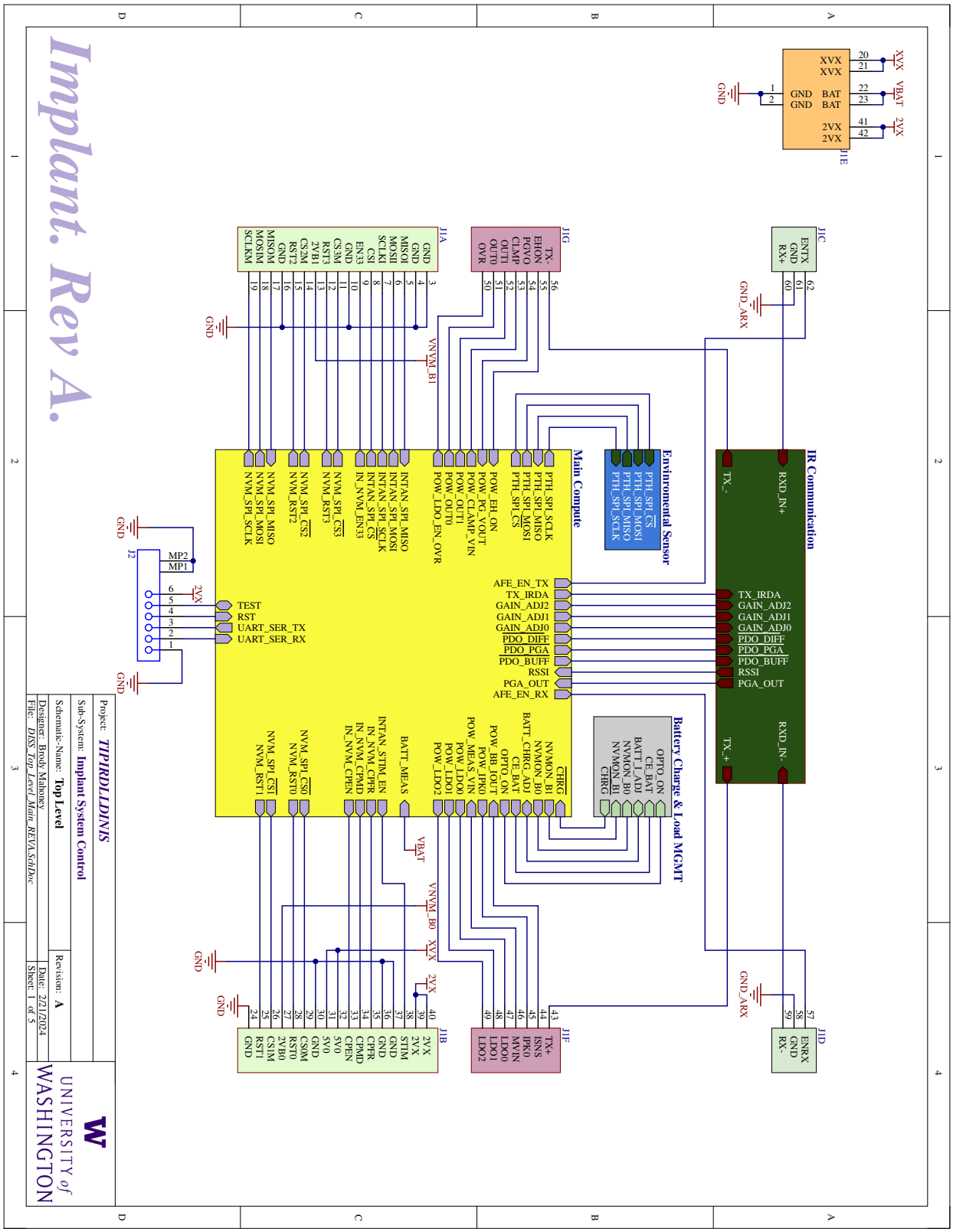

Implant. Rev A.
Notes:
1.) Decoupling capacitors may be optional. With cap at 0.1uF on each pin, a large voltage droop can occur on the 2VX rail.
2.) LB0, LB1, DB0 and DB1 in conjunction with microcontroller PWM, provide a means to reduce in-rush current. May not be required in final version.
Project: TIPIRDLLDINS
Sub-System: Neural IFC & NVM
Schematic-Name: NVM Bank
Revision: A
Designer: Brody Mahoney
Date: 2/21/2024
File: Dlss_NVM_REVA.SchDoc
Sheet 4 of 4
UNIVERSITY of WASHINGTON
U2 AT45DB641E-UUN2B-T
U3 AT45DB641E-UUN2B-T
U4 AT45DB641E-UUN2B-T
U5 AT45DB641E-UUN2B-T
2VB0_S
2VB1_S
GND_NVM
nvmSO
nvmSI
nvmSCLK
nvmRST0
nvmCS0
nvmRST1
nvmCS1
nvmRST2
nvmCS2
nvmRST3
nvmCS3
NVMMISO
NVMMOSI
NVMSCLK
NVMCS0
NVMRST0
NVMCS1
NVMRST1
NVMCS2
NVMRST2
NVMCS3
NVMRST3
R20 1MEG
R21 1MEG
R30 1MEG
R31 1MEG
R40 1MEG
R41 1MEG
R50 1MEG
R51 1MEG
C20 0.01uF
C30 0.01uF
C40 0.01uF
C50 0.01uF
LB0 10uH
LB1 10uH
DB0
DB1
2VB0
2VB1


Implant. Rev A.
Main Compute
IR Communication
Environmental Sensor
Battery Charge & Load MGMT
J1E
J1C
J1D
J1F
J1G
J1A
J1B
J2
XVX
VBAT
2VX
GND
GND_ARX
VNVM_B1
VNVM_B0
TEST
RST
UART_SER_TX
UART_SER_RX
TX_IRDA
GAIN_ADJ2
GAIN_ADJ1
GAIN_ADJ0
PDO_DIFF
PDO_PGA
PDO_BUFF
RSSI
PGA_OUT
AFE_EN_TX
AFE_EN_RX
PTH_SPI_SCLK
PTH_SPI_MISO
PTH_SPI_MOSI
PTH_SPI_CS
POW_EH_ON
POW_PG_VOUT
POW_CLAMP_VIN
POW_OUT1
POW_OUT0
POW_LDO_EN_OVR
INTAN_SPI_MISO
INTAN_SPI_MOSI
INTAN_SPI_SCLK
INTAN_SPI_CS
IN_NVM_EN33
NVM_SPI_CS3
NVM_SPI_CS2
NVM_SPI_MISO
NVM_SPI_MOSI
NVM_SPI_SCLK
NVM_SPI_CS0
NVM_RST0
NVM_SPI_CS1
NVM_RST1
INTAN_STIM_EN
IN_NVM_CPFR
IN_NVM_CPMD
IN_NVM_CPEN
BATT_MEAS
CHRG
NVMON_B1
NVMON_B0
BATT_CHRG_ADJ
CE_BAT
OPTO_ON
POW_BB_IOUT
POW_IPK0
POW_MEAS_VIN
POW_LDO1
POW_LDO0
POW_LDO2
Project: TIPIRDLLDINS
Sub-System: Implant System Control
Schematic-Name: Top Level
Revision: A
Designer: Brody Mahoney
Date: 2/21/2024
File: DINS_Top_Level_Main_REVA.SchDoc
Sheet 1 of 5
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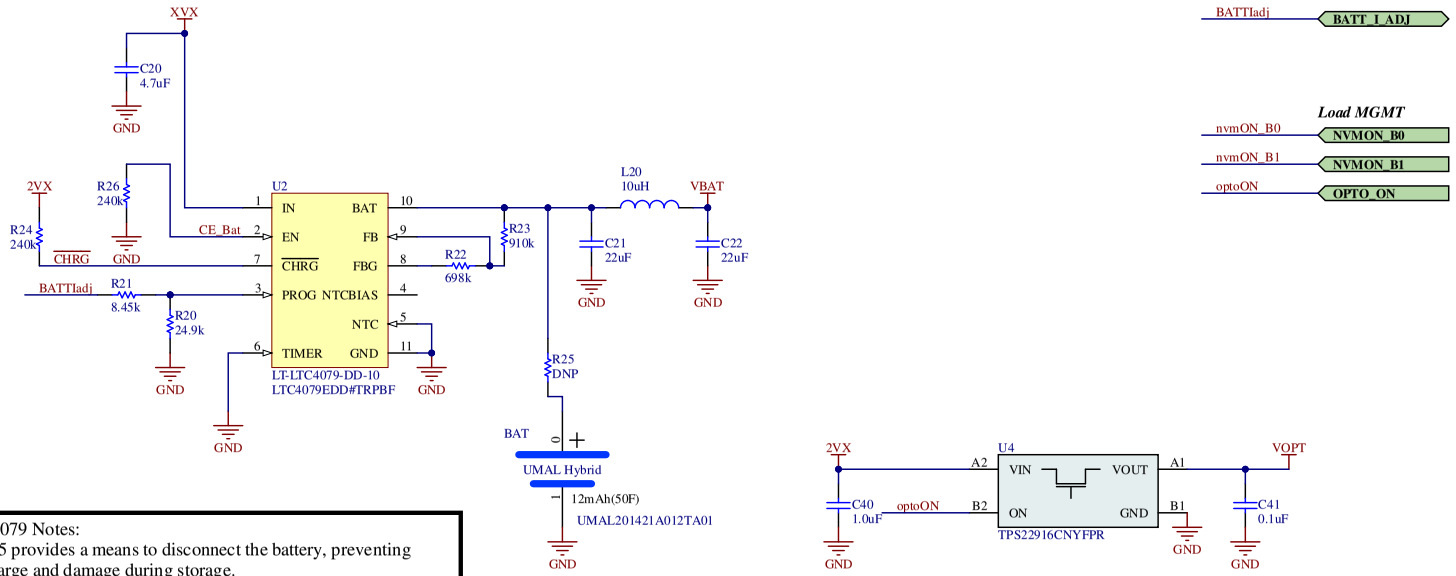

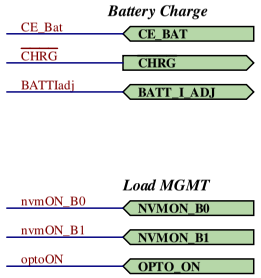

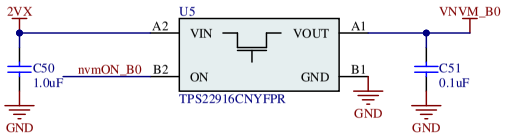

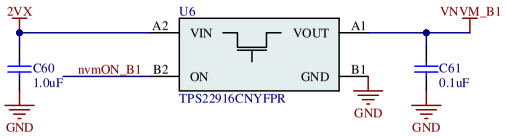

LTC4079 Notes:
1. R25 provides a means to disconnect the battery, preventing discharge and damage during storage.
2. Battery charge current set by pull-down resistor at Pin 3 of U2. Rprog=297.5/Ichrg. R20 = Rprog = 25k. Default Ichrg=~12mA(1C).
3. R21 allows Ichrg to be adjusted by using a GPIO and switching from Hi-Z to Digitial output 0. Thus Rprog = R20||R21. With R21=8.4k, Ichrg may be increased to ~60mA(5C).
4. Battery charge current may be measured at Pin 3 of U2 if GPIO interfacing with R21 is set as Hi-Z input. Ibat=250*Vprog/Rprog.
5. Battery voltage set by R22 and R23. Vchg=1.170V(1+R23/(R22+160))=~2.7V.
6. C21, C22, L20 form a LPF to protect the battery from high frequency current draws. The LTC3330 Boost converter, inherently pulses current from the battery. L20 selection is important for cutoff frequency and power dissipation. Footprint is set as 0805 limiting practical values to about 10-20uH.

Implant. Rev A.

Project: ***TIPIRDLLDINIS***	
Sub-System: **Implant System Control**	
Schematic-Name: **Battery Charge & Load MGMT**	Revision: **A**
Designer: Brody Mahoney	Date: 2/21/2024
File: *DISS_Battery_Power_MGMT_REVA.SchDoc*	Sheet: 2 of 5

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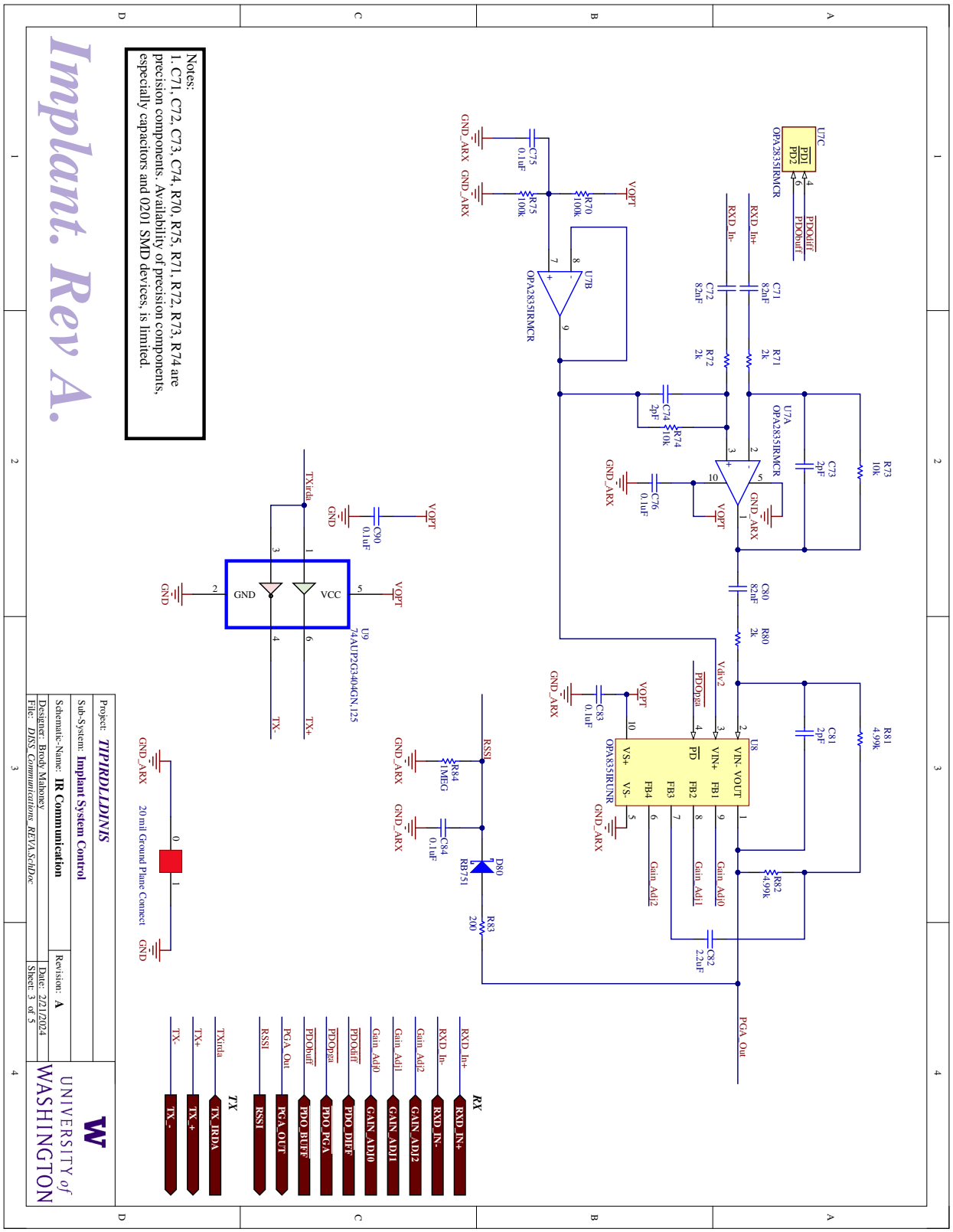
Implant. Rev A.
Notes:
1. C71, C72, C73, C74, R70, R75, R71, R72, R73, R74 are precision components. Availability of precision components, especially capacitors and 0201 SMD devices, is limited.
U7C
OPA2835IRMCR
PDOdiff
RXD_In+
RXD_In-
C71 82nF
C72 82nF
R71 2k
R72 2k
U7A
OPA2835IRMCR
C73 2pF
C74 2pF
R74 10k
R73 10k
C75 0.1uF
R75 100k
R70 100k
U7B
OPA2835IRMCR
VQPT
GND_ARX
C76 0.1uF
C80 82nF
R80 2k
Vdiv2
PDOpga
U8
OPA835IRUNR
VIN- VOUT
VIN+
PD
VS+
VS-
FB1
FB2
FB3
FB4
C83 0.1uF
C81 2pF
R81 4.99k
R82 4.99k
Gain_Adj0
Gain_Adj1
Gain_Adj2
C82 2.2uF
PGA_Out
RSSI
R84 1MEG
C84 0.1uF
D80 RB751
R83 200
TXirda
C90 0.1uF
U9
74AUP2G3404GN,125
GND
VCC
TX+
TX-
RXD_In+
RXD_In-
Gain_Adj2
Gain_Adj1
Gain_Adj0
PDOdiff
PDOpga
PGA_Out
RSSI
RX
RXD_IN+
RXD_IN-
GAIN_ADJ2
GAIN_ADJ1
GAIN_ADJ0
PDO_DIFF
PDO_PGA
PDO_RUFF
PGA_OUT
RSSI
TX
TX_IRDA
TX+
TX-
20 mil Ground Plane Connect
Project: TIPIRDLLDINS
Sub-System: Implant System Control
Schematic-Name: IR Communication
Designer: Brody Mahoney
File: DDS Communications REVA.SchDoc
Revision: A
Date: 2/21/2024
Sheet 3 of 5
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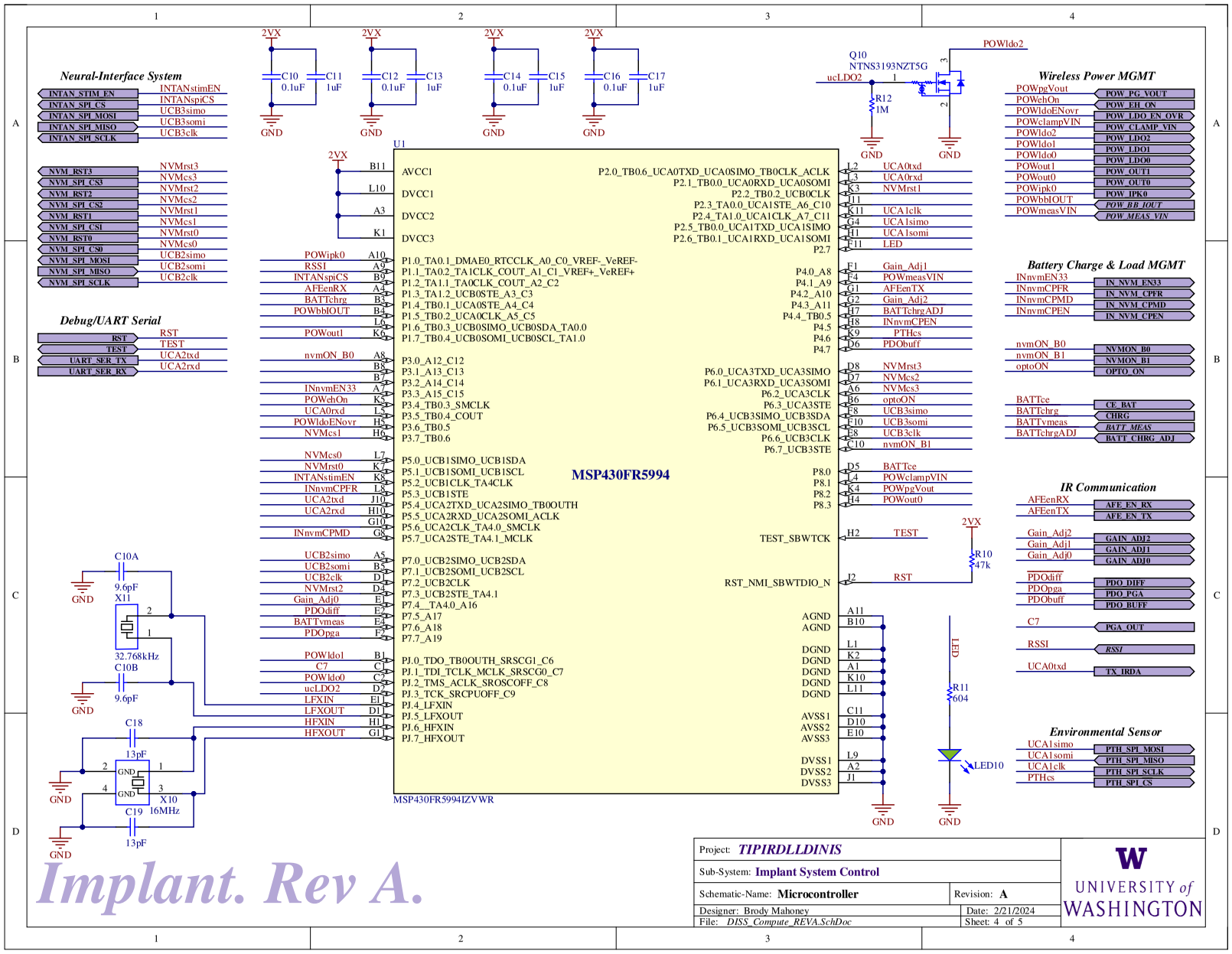
Neural-Interface System
INTAN_STIM_EN
INTAN_SPI_CS
INTAN_SPI_MOSI
INTAN_SPI_MISO
INTAN_SPI_SCLK
INTANstimEN
INTANspiCS
UCB3simo
UCB3somi
UCB3clk
NVM_RST3
NVM_SPI_CS3
NVM_RST2
NVM_SPI_CS2
NVM_RST1
NVM_SPI_CS1
NVM_RST0
NVM_SPI_CS0
NVM_SPI_MOSI
NVM_SPI_MISO
NVM_SPI_SCLK
NVMrst3
NVMcs3
NVMrst2
NVMcs2
NVMrst1
NVMcs1
NVMrst0
NVMcs0
UCB2simo
UCB2somi
UCB2clk
Debug/UART Serial
RST
TEST
UART_SER_TX
UART_SER_RX
RST
TEST
UCA2txd
UCA2rxd
2VX
C10 0.1uF
C11 1uF
C12 0.1uF
C13 1uF
C14 0.1uF
C15 1uF
C16 0.1uF
C17 1uF
GND
U1
MSP430FR5994
MSP430FR5994IZVWR
AVCC1
DVCC1
DVCC2
DVCC3
P1.0_TA0.1_DMAE0_RTCCLK_A0_C0_VREF-_VeREF-
P1.1_TA0.2_TA1CLK_COUT_A1_C1_VREF+_VeREF+
P1.2_TA1.1_TA0CLK_COUT_A2_C2
P1.3_TA1.2_UCB0STE_A3_C3
P1.4_TB0.1_UCA0STE_A4_C4
P1.5_TB0.2_UCA0CLK_A5_C5
P1.6_TB0.3_UCB0SIMO_UCB0SDA_TA0.0
P1.7_TB0.4_UCB0SOMI_UCB0SCL_TA1.0
P3.0_A12_C12
P3.1_A13_C13
P3.2_A14_C14
P3.3_A15_C15
P3.4_TB0.3_SMCLK
P3.5_TB0.4_COUT
P3.6_TB0.5
P3.7_TB0.6
P5.0_UCB1SIMO_UCB1SDA
P5.1_UCB1SOMI_UCB1SCL
P5.2_UCB1CLK_TA4CLK
P5.3_UCB1STE
P5.4_UCA2TXD_UCA2SIMO_TB0OUTH
P5.5_UCA2RXD_UCA2SOMI_ACLK
P5.6_UCA2CLK_TA4.0_SMCLK
P5.7_UCA2STE_TA4.1_MCLK
P7.0_UCB2SIMO_UCB2SDA
P7.1_UCB2SOMI_UCB2SCL
P7.2_UCB2CLK
P7.3_UCB2STE_TA4.1
P7.4__TA4.0_A16
P7.5_A17
P7.6_A18
P7.7_A19
PJ.0_TDO_TB0OUTH_SRSCG1_C6
PJ.1_TDI_TCLK_MCLK_SRSCG0_C7
PJ.2_TMS_ACLK_SROSCOFF_C8
PJ.3_TCK_SRCPUOFF_C9
PJ.4_LFXIN
PJ.5_LFXOUT
PJ.6_HFXIN
PJ.7_HFXOUT
P2.0_TB0.6_UCA0TXD_UCA0SIMO_TB0CLK_ACLK
P2.1_TB0.0_UCA0RXD_UCA0SOMI
P2.2_TB0.2_UCB0CLK
P2.3_TA0.0_UCA1STE_A6_C10
P2.4_TA1.0_UCA1CLK_A7_C11
P2.5_TB0.0_UCA1TXD_UCA1SIMO
P2.6_TB0.1_UCA1RXD_UCA1SOMI
P2.7
P4.0_A8
P4.1_A9
P4.2_A10
P4.3_A11
P4.4_TB0.5
P4.5
P4.6
P4.7
P6.0_UCA3TXD_UCA3SIMO
P6.1_UCA3RXD_UCA3SOMI
P6.2_UCA3CLK
P6.3_UCA3STE
P6.4_UCB3SIMO_UCB3SDA
P6.5_UCB3SOMI_UCB3SCL
P6.6_UCB3CLK
P6.7_UCB3STE
P8.0
P8.1
P8.2
P8.3
TEST_SBWTCK
RST_NMI_SBWTDIO_N
AGND
DGND
AVSS1
AVSS2
AVSS3
DVSS1
DVSS2
DVSS3
POWipk0
RSSI
INTANspiCS
AFEenRX
BATTchrg
POWbblOUT
POWout1
nvmON_B0
INnvmEN33
POWehOn
UCA0rxd
POWldoENovr
NVMcs1
NVMcs0
NVMrst0
INTANstimEN
INnvmCPFR
UCA2txd
UCA2rxd
INnvmCPMD
UCB2simo
UCB2somi
UCB2clk
NVMrst2
Gain_Adj0
PDOdiff
BATTvmeas
PDOpga
POWldo1
C7
POWldo0
ucLDO2
LFXIN
LFXOUT
HFXIN
HFXOUT
UCA0txd
UCA0rxd
NVMrst1
LED
Gain_Adj1
POWmeasVIN
AFEenTX
Gain_Adj2
BATTchrgADJ
INnvmCPEN
PTHcs
PDObuff
NVMrst3
NVMcs2
NVMcs3
optoON
UCB3simo
UCB3somi
UCB3clk
nvmON_B1
BATTce
POWclampVIN
POWpgVout
POWout0
TEST
RST
Q10
NTNS3193NZT5G
ucLDO2
R12
1M
POWldo2
R10
47k
C10A
9.6pF
X11
32.768kHz
C10B
9.6pF
C18
13pF
X10
16MHz
C19
13pF
R11
604
LED10
GET
Wireless Power MGMT
POWpgVout
POWehOn
POWldoENovr
POWclampVIN
POWldo2
POWldo1
POWldo0
POWout1
POWout0
POWipk0
POWbblOUT
POWmeasVIN
POW_PG_VOUT
POW_EH_ON
POW_LDO_EN_OVR
POW_CLAMP_VIN
POW_LDO2
POW_LDO1
POW_LDO0
POW_OUT1
POW_OUT0
POW_IPK0
POW_BB_IOUT
POW_MEAS_VIN
Battery Charge & Load MGMT
INnvmEN33
INnvmCPFR
INnvmCPMD
INnvmCPEN
IN_NVM_EN33
IN_NVM_CPFR
IN_NVM_CPMD
IN_NVM_CPEN
nvmON_B0
nvmON_B1
optoON
NVMON_B0
NVMON_B1
OPTO_ON
BATTce
BATTchrg
BATTvmeas
BATTchrgADJ
CE_BAT
CHRG
BATT_MEAS
BATT_CHRG_ADJ
IR Communication
AFEenRX
AFEenTX
AFE_EN_RX
AFE_EN_TX
Gain_Adj2
Gain_Adj1
Gain_Adj0
GAIN_ADJ2
GAIN_ADJ1
GAIN_ADJ0
PDOdiff
PDOpga
PDObuff
PDO_DIFF
PDO_PGA
PDO_BUFF
C7
PGA_OUT
RSSI
RSSI
UCA0txd
TX_IRDA
Environmental Sensor
UCA1simo
UCA1somi
UCA1clk
PTHcs
PTH_SPI_MOSI
PTH_SPI_MISO
PTH_SPI_SCLK
PTH_SPI_CS
Implant. Rev A.
Project: TIPIRDLLDINIS
Sub-System: Implant System Control
Schematic-Name: Microcontroller
Revision: A
Designer: Brody Mahoney
Date: 2/21/2024
File: DISS_Compute_REVA.SchDoc
Sheet: 4 of 5
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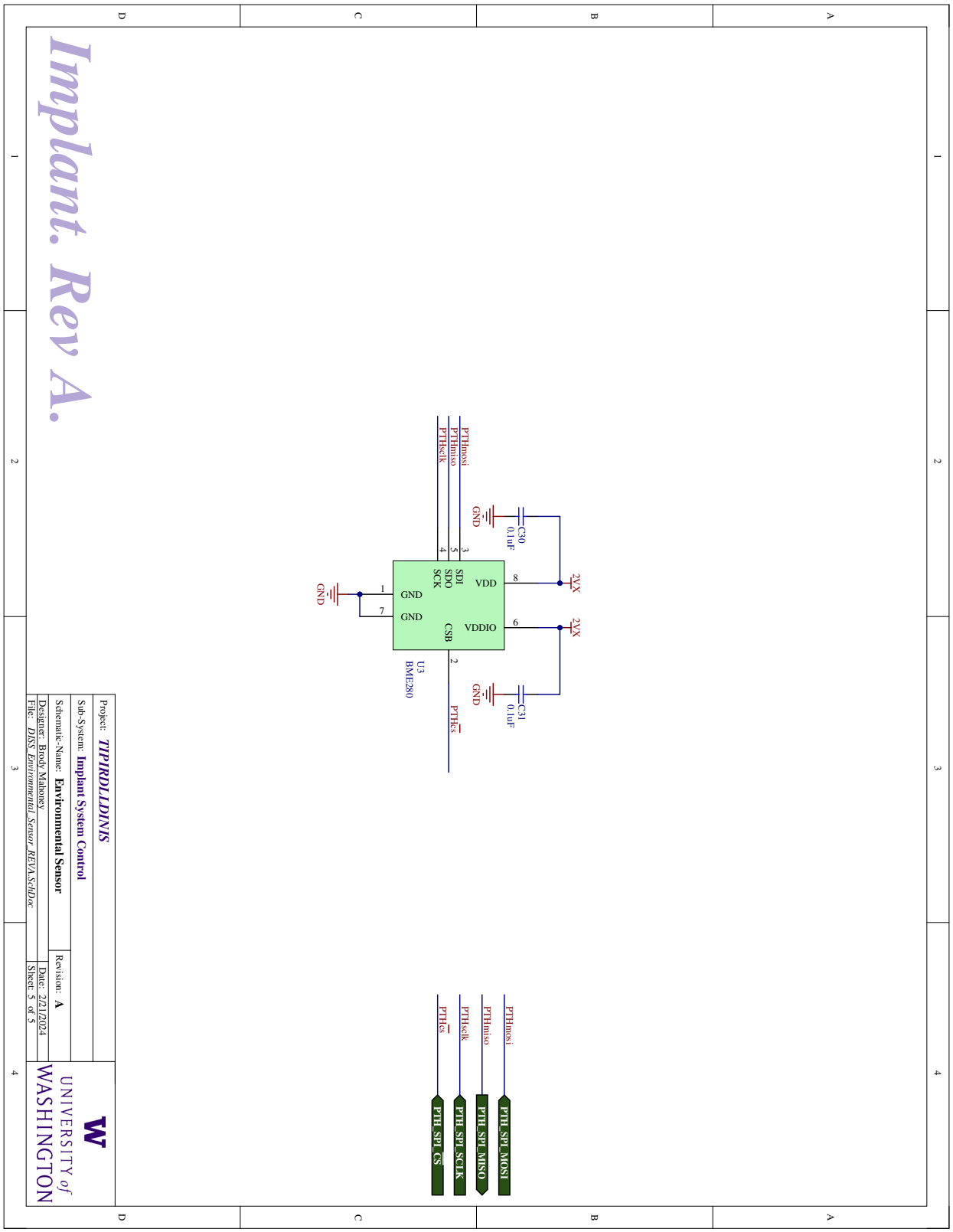
Implant. Rev A.
PTHmosi
PTHmiso
PTHsclk
PTHcs
PTH_SPI_MOSI
PTH_SPI_MISO
PTH_SPI_SCLK
PTH_SPI_CS
GND
C30
0.1uF
C31
0.1uF
2VX
U3
BME280
SDI
SDO
SCK
CSB
VDD
VDDIO
Project: TIPIRDLLDINIS
Sub-System: Implant System Control
Schematic-Name: Environmental Sensor
Revision: A
Designer: Brody Mahoney
Date: 2/21/2024
File: DISS_Environmental_Sensor_REVA.SchDoc
Sheet 5 of 5
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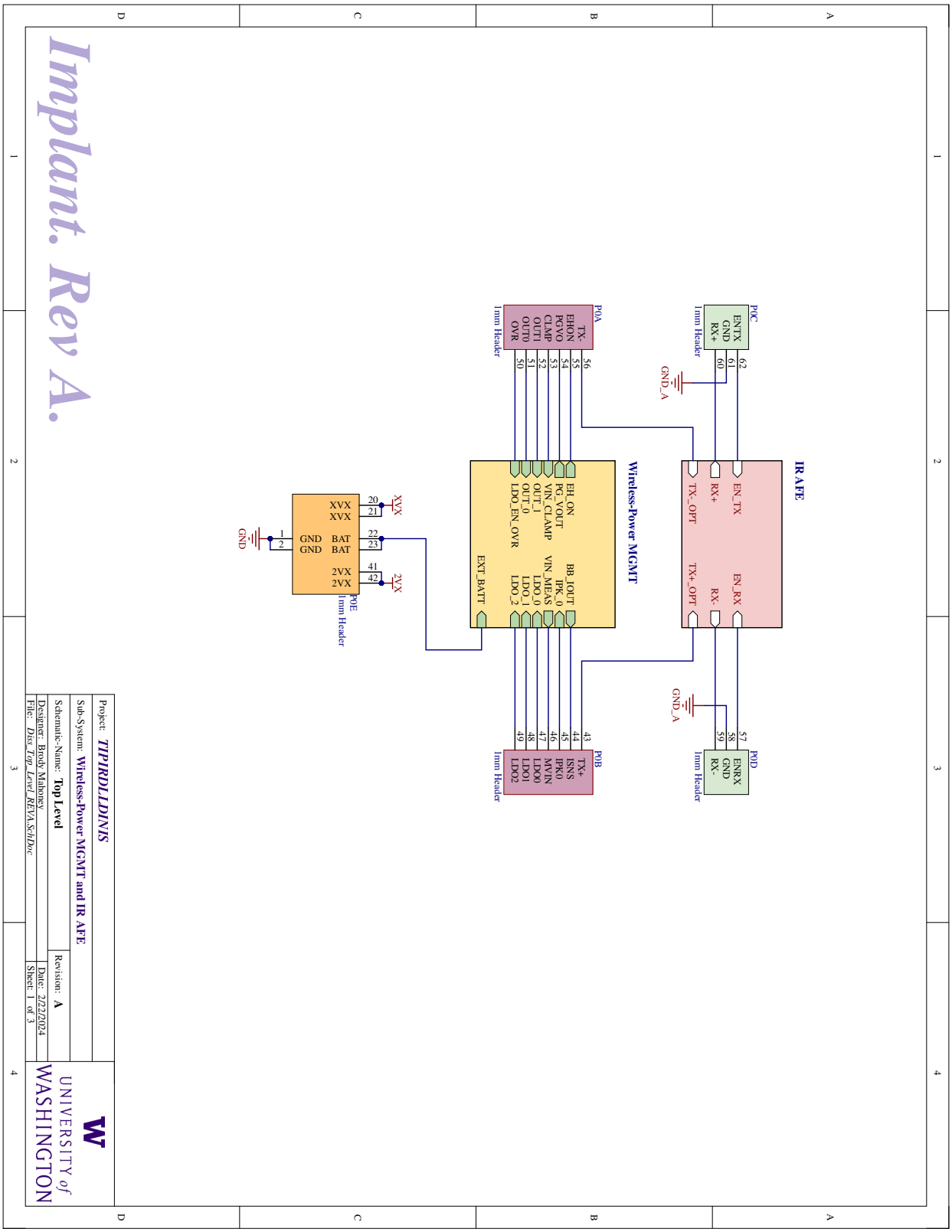
Implant. Rev A.
IR AFE
EN_TX
RX+
TX-_OPT
EN_RX
RX-
TX+_OPT
Wireless-Power MGMT
EH_ON
PG_VOUT
VIN_CLAMP
OUT_1
OUT_0
LDO_EN_OVR
EXT_BATT
BB_IOUT
IPK_0
VIN_MEAS
LDO_0
LDO_1
LDO_2
P0A
TX-
EHON
PGVO
CLAMP
OUT1
OUT0
OVR
P0B
TX+
ISNS
IPK0
MVIN
LDO0
LDO1
LDO2
P0C
ENTX
GND
RX+
P0D
ENRX
GND
RX-
P0E
XVX
XVX
GND
BAT
GND
BAT
2VX
2VX
1mm Header
GND_A
GND
XVX
2VX
Project: TIPIRDLLDINS
Sub-System: Wireless-Power MGMT and IR AFE
Schematic-Name: Top Level
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Dss_Top_Level_REVA.SchDoc
Sheet 1 of 3
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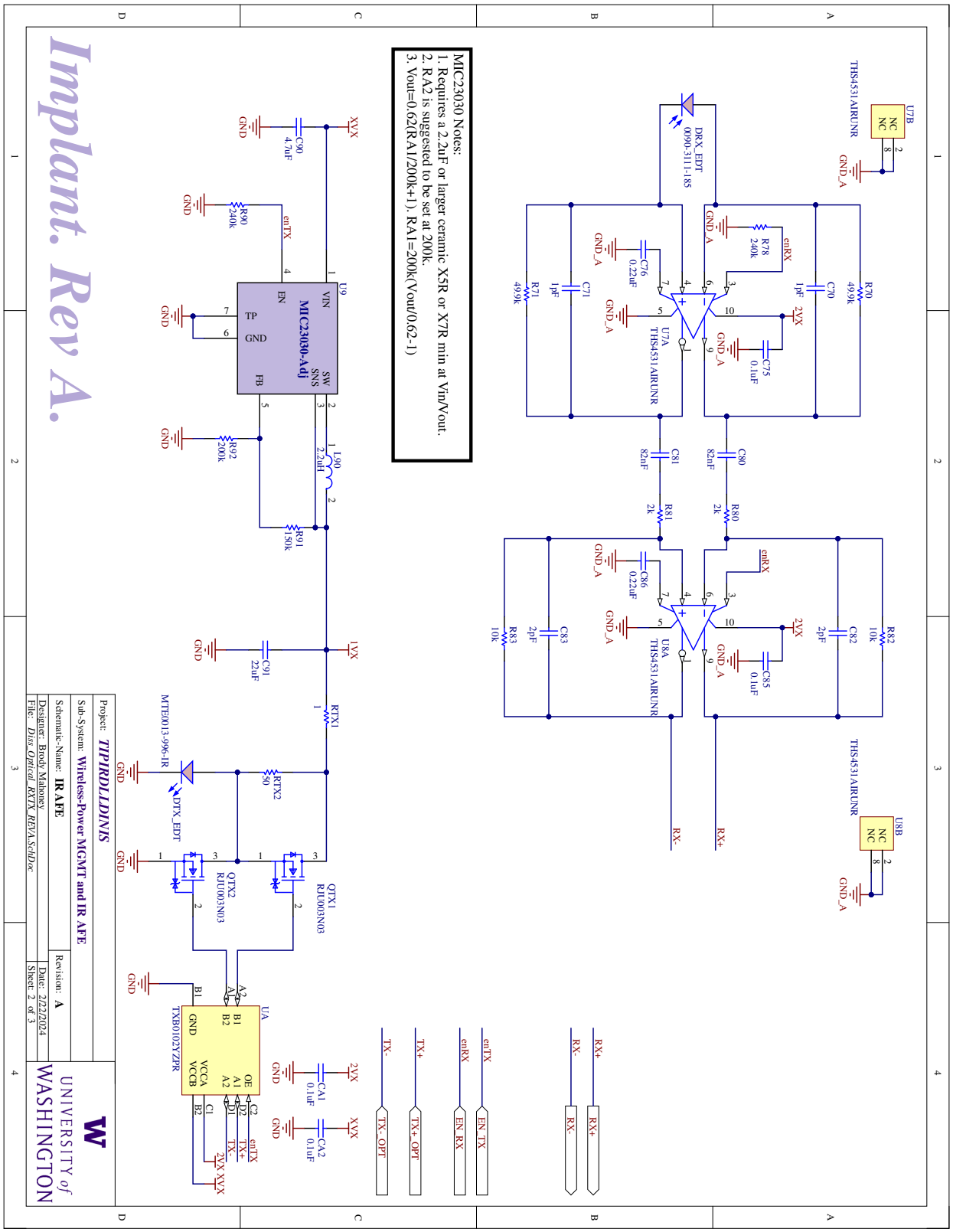
MIC23030 Notes:
1. Requires a 2.2uF or larger ceramic X5R or X7R min at Vin/Vout.
2. RA2 is suggested to be set at 200k.
3. Vout=0.62(RA1/200k+1). RA1=200k(Vout/0.62-1)
Implant. Rev A.
Project: TIPIRDLLDINS
Sub-System: Wireless-Power MGMT and IR AFE
Schematic-Name: IR AFE
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Diss_Optical_RXTX_REVA.SchDoc
Sheet 2 of 3
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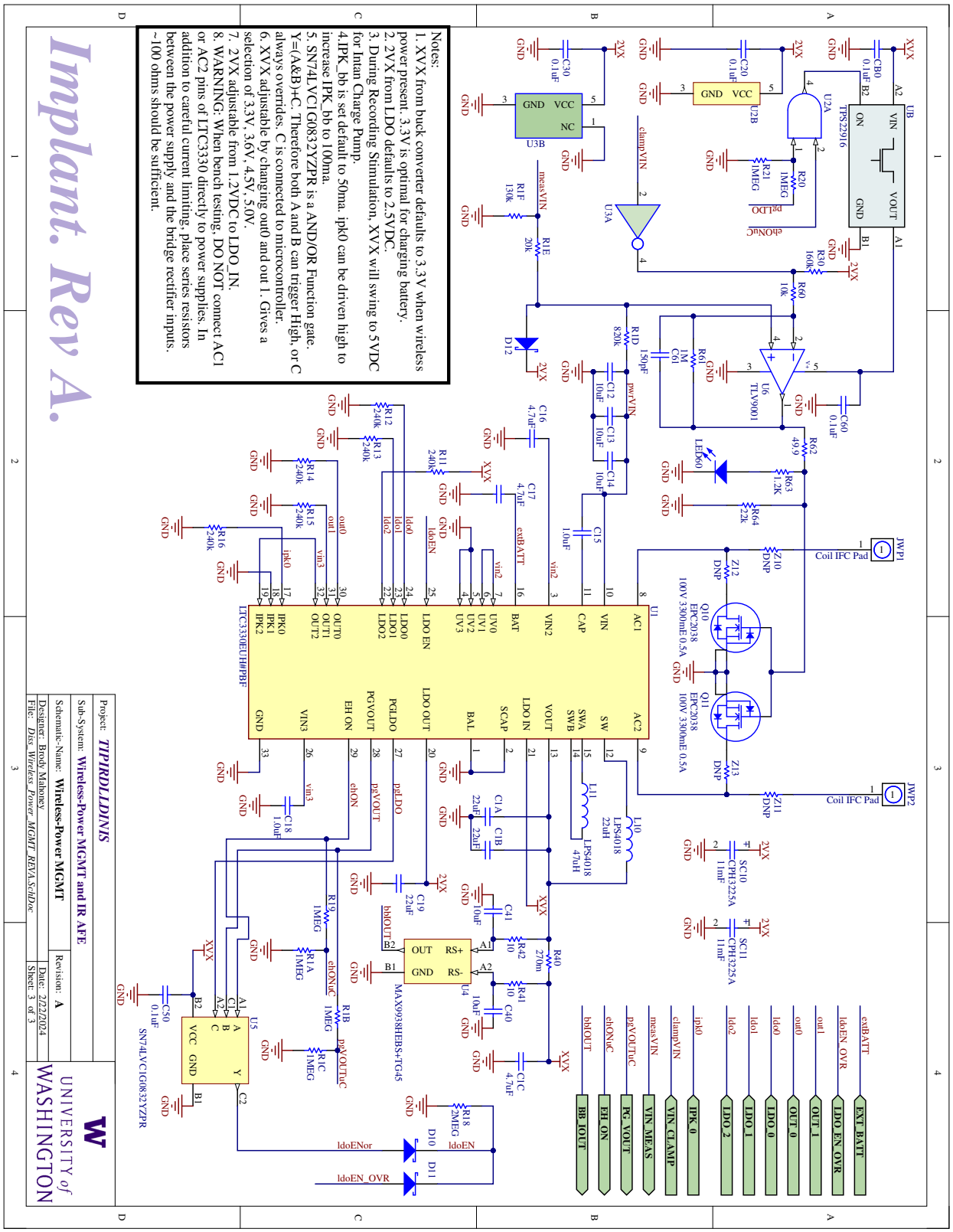
MIC23030-Adj
THS4531AIRUNR
TXB0102YZPR
RJU003N03
MTE0013-996-IR
DRX_EDT
DTX_EDT
RX+
RX-
TX+
TX-
EN_TX
EN_RX
TX+_OPT
TX-_OPT


Implant. Rev A.
Notes:
1. XVX from buck converter defaults to 3.3V when wireless power present. 3.3V is optimal for charging battery.
2. 2VX from LDO defaults to 2.5VDC.
3. During Recording Stimulation, XVX will swing to 5VDC for Intan Charge Pump.
4.IPK_bb is set default to 50ma. ipk0 can be driven high to increase IPK_bb to 100ma.
5. SN74LVC1G0832YZPR is a AND/OR Function gate. Y=(A&B)+C. Therefore both A and B can trigger High, or C always overrides. C is connected to microcontroller.
6. XVX adjustable by changing out0 and out 1. Gives a selection of 3.3V, 3.6V, 4.5V, 5.0V.
7. 2VX adjustable from 1.2VDC to LDO_IN.
8. WARNING: When bench testing, DO NOT connect AC1 or AC2 pins of LTC3330 directly to power supplies. In addition to careful current limiting, place series resistors between the power supply and the bridge rectifier inputs. ~100 ohms should be sufficient.
LTC3330EUH#PBF
SN74LVC1G0832YZPR
MAX9938HEBS+TG45
TPS22916
TLV9001
Coil IFC Pad
Project: TIPIRDLLDINS
Sub-System: Wireless-Power MGMT and IR AFE
Schematic-Name: Wireless-Power MGMT
Revision: A
Designer: Brody Mahoney
Date: 2/22/2024
File: Diss_Wireless_Power_MGMT_REVA.SchDoc
Sheet: 3 of 3
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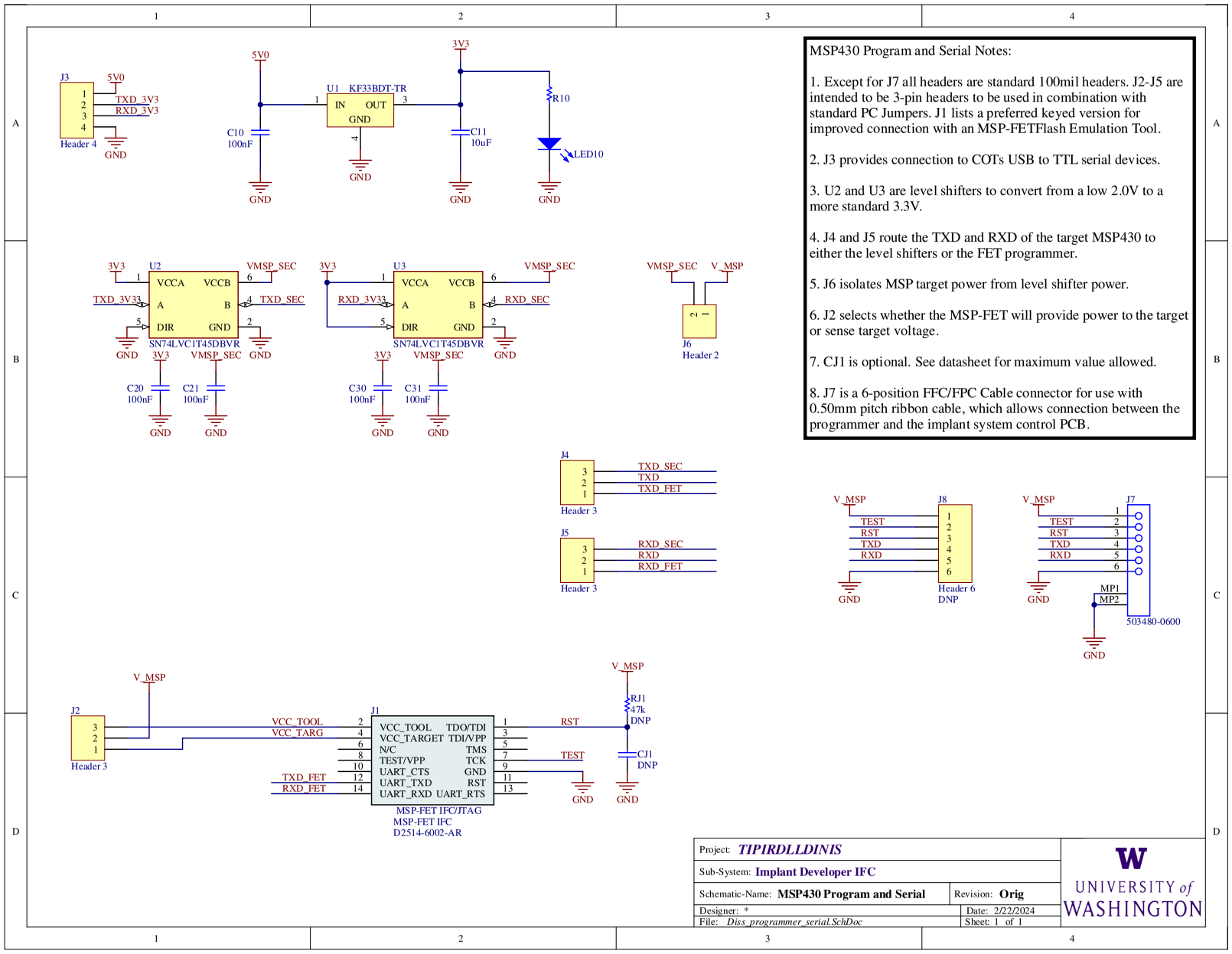
MSP430 Program and Serial Notes:
1. Except for J7 all headers are standard 100mil headers. J2-J5 are intended to be 3-pin headers to be used in combination with standard PC Jumpers. J1 lists a preferred keyed version for improved connection with an MSP-FETFlash Emulation Tool.
2. J3 provides connection to COTs USB to TTL serial devices.
3. U2 and U3 are level shifters to convert from a low 2.0V to a more standard 3.3V.
4. J4 and J5 route the TXD and RXD of the target MSP430 to either the level shifters or the FET programmer.
5. J6 isolates MSP target power from level shifter power.
6. J2 selects whether the MSP-FET will provide power to the target or sense target voltage.
7. CJ1 is optional. See datasheet for maximum value allowed.
8. J7 is a 6-position FFC/FPC Cable connector for use with 0.50mm pitch ribbon cable, which allows connection between the programmer and the implant system control PCB.
J3
Header 4
5V0
TXD_3V3
RXD_3V3
GND
U1 KF33BDT-TR
IN
OUT
C10 100nF
C11 10uF
R10
LED10
3V3
U2
U3
VCCA
VCCB
DIR
SN74LVC1T45DBVR
VMSP_SEC
TXD_SEC
RXD_SEC
C20 100nF
C21 100nF
C30 100nF
C31 100nF
J6
Header 2
V_MSP
J4
Header 3
TXD_SEC
TXD
TXD_FET
J5
RXD_SEC
RXD
RXD_FET
J8
Header 6
DNP
TEST
RST
J7
503480-0600
MP1
MP2
J2
J1
MSP-FET IFC/JTAG
MSP-FET IFC
D2514-6002-AR
VCC_TOOL
VCC_TARG
TXD_FET
RXD_FET
TDO/TDI
TDI/VPP
TMS
TCK
UART_CTS
UART_TXD
UART_RXD
UART_RTS
RJ1
47k
CJ1
Project: TIPIRDLLDINIS
Sub-System: Implant Developer IFC
Schematic-Name: MSP430 Program and Serial
Revision: Orig
Designer: *
Date: 2/22/2024
File: Diss_programmer_serial.SchDoc
Sheet: 1 of 1
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