A Toolbox of Optimized Silicon Photonics Devices

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Abstract

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Silicon photonics has emerged as a disruptive technology to address the exponentially growing demand for bandwidth in optical interconnects and data communications. The silicon material system supports large wafers, high device yield and performance uniformity, leveraging the half-century of investment by the electronics industry. Silicon is transparent in the 1.3 – 1.6 μm wavelength range, and has higher refractive index than its oxide, enabling submicron waveguides. On the other hand, the high index contrast between silicon and oxide, 3.4 to 1.4, making silicon photonic devices very sensitive to geometry variations commonly seen in complementary metal-oxide-semiconductor (CMOS) fabrication. I demonstrate a design approach using coupled particle swarm optimization (PSO) and finite difference time domain (FDTD) method that produces highly compact, efficient and robust passive devices. Silicon also has a high thermo-optic coefficient, 1.8×10^{-4} K^{-1}, making resonant devices, which are critical for wavelength

filtering and multiplexing, sensitive to temperature perturbations that are common in practical environments. A universal stabilization approach based on bandgap temperature sensor and active feedback control is presented.

In addition to passive devices, active device such as modulators, photodetectors, and lasers are needed for practical photonics integrated circuits (PICs). Electro-optic modulation in silicon can be achieved by free carrier plasma effect, typically implemented as reverse biased p-n junction overlapping with the waveguide mode. However lasing or photo detection is inherently not available in silicon, and is only possible by integrating other optically active materials. Germanium is the preferred absorber because of its CMOS compatibility, but germanium processing has received far less attention than silicon so far, with active ongoing research trying to understand its implantation, dopant diffusion, and metal contact alloying properties. Hence a photodetector that does not require doping or metallization of germanium is highly desirable. I propose and demonstrate a germanium-on-silicon photodetector using only intrinsic germanium and no metal-germanium contact, which significantly simplify the process flow. The detector shows 1.14 A/W responsivity, over 40 GHz 3 dB bandwidth, and less than 1 μA dark current. I also demonstrate a hybrid-integrated laser based on Sagnac loop mirror and micro-ring wavelength filter with 44 dB side mode suppression ratio, 1.2 MHz line-width, and 4.8 mW on-chip output power. Compared to distributed Bragg grating based cavity, which require ultra-fine feature size, the Sagnac loop mirror is simple to fabricate, and provides accurately controlled transmittance (and reflectivity) with negligible excess loss.

The toolbox of devices presented in this thesis includes, in summary:

i. Highly efficient, compact, and robust Y-junctions and waveguide crossings, as well as an universal PSO-FDTD design methodology;

ii. A floating germanium photodetector that is free from doping in Ge and direct Ge-metal contact, with high responsivity, high bandwidth and low dark current;

iii. A Sagnac loop mirror and micro-ring based on-chip cavity configuration for laser integration;

iv. A bandgap temperature sensor for resonance thermal stabilization.

These address the unique challenges of building integrated photonics devices using CMOS-compatible material system, and, bring the vision of large-scale photonic integration on silicon an important step forward to practical application.

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GLOSSARY OF ACRONYMS

APD Avalanche Photodetector

BER Bit Error Rate

BOX Buried Oxide

CMOS Complementary Metal-Oxide-Semiconductor

DBR Distributed Bragg Reflector

DCA Digital Communication Analyzer

DRC Design Rule Checking

DUT Device Under Test

FDTD Finite Difference Time Domain

FOM Figure of Merit

FSR Free Spectral Range

FWHM Full Width at Half Maximum

GaAs Gallium Arsenide

InP Indium Phosphide

$LiNO_3$ Lithium Niobate

MFD Mode Field Diameter

MPW Multi Project Wafer

NRZ Non-Return to Zero

PIC Photonic Integrated Circuits

PSO Particle Swarm Optimization

QD Quantum Dot

RSOA Reflective Semiconductor Optical Amplifier

SOI Silicon on Insulator

SEM Scanning Electron Microscope

TEC Thermal Electric Cooler

WDM Wavelength Division Multiplexing

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I would like to thank my wife Shuyu for her unwavering love and care, and my entire family for their help and support over the years.

DEDICATION

To my wife Shuyu and my parents

CHAPTER 1. INTRODUCTION

The exponential growth in Internet traffic generates unprecedented demand for communication bandwidth on optical transport networks and local interconnects. Photonic integration is the only viable solution to address this challenge. Silicon photonics is emerging as a promising platform for building high-speed, low energy consumption, and low cost photonics integrated circuits (PICs). Several unique challenges for building integrated photonics devices in CMOS material systems are explained, including fabrication tolerance and thermal sensitivity of passive devices due to high refractive index contrast and thermo-optic effect of silicon. Other challenges, including the weak electro-optic effect for modulation, as well as the effect of the large and indirect bandgap, which prohibits lasing and creates challenges for photo detection at telecom wavelengths. My graduate research on passive device design and optimization, floating germanium on silicon photodetector, hybrid laser integration, and resonance thermal stabilization to address such challenges are outlined.

1.1 Internet traffic growth

We now live in a connected world, with way more information exchange day in and day out than ever before. Fixed and mobile devices, such as personal computers, TV, tablets, smart phones, and laptop, become essential tools of life. People communicate learn, work, entertain, and transact more and more via the Internet. Such shifts of lifestyle generates an enormous amount of data traffic on the core and access networks. The global Internet traffic has grown from 1.2 Mb/s in the early 1990s, to 100 Gb/s in early 2000s, and 28 Tb/s in 2013. Strong Internet traffic growth is expected to continue, according to Cisco visual network index [1]. The projections covering the 5-year period

from 2013 to 2018 are summarized in Fig. 1. Fixed Internet traffic doubles and is mainly driven by high definition video services. Mobile Internet accounts for a smaller percentage, but is predicted for a 5-fold growth.

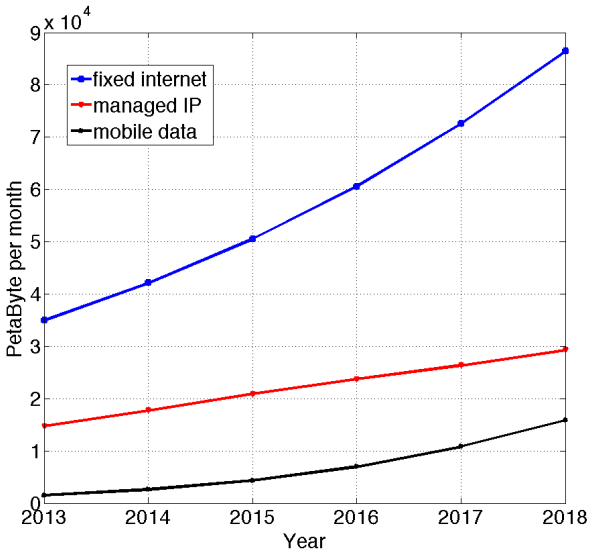

Fig. 1.1 Internet traffic growth projections between 2013 and 2018 [1]

Since the adoption of optical communications in the 1980s, fiber transmission capacity has been increasing by a factor of ten over every four years, driven by a constant stream of new technologies, as shown in Fig. 2 [2]. In the very beginning, work focused on reducing fiber propagation loss, and then erbium doped fiber amplifier (EDFA) was introduced in around 1990s. It is well understood that new fiber deployment was extremely capital intensive; hence capacity improvement was achieved by upgrading the terminal equipment whenever possible. Wavelength division multiplexing (WDM), and advanced modulation formats and coherent detection helped keeping the capacity growth by pumping more data though the same existing fibers.

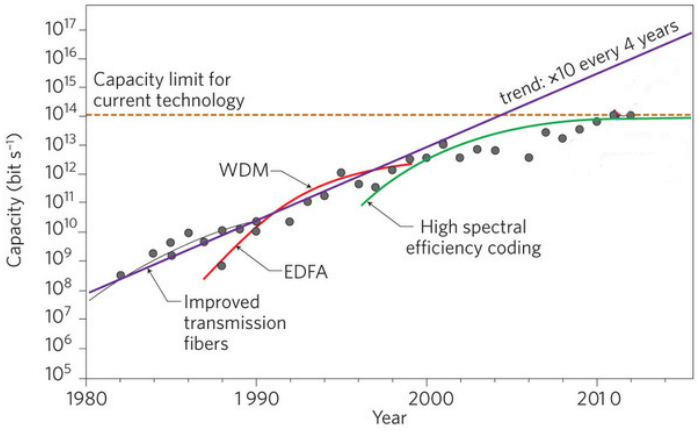

Fig. 1.2 Optical fiber transmission capacity growth [2]

1.2 Photonic integration

Optical transceivers are critical parts of data transmission equipment. Current state-of-the-art optical transceivers are mainly based on discrete components made in different materials, usually Indium Phosphide (InP) lasers, Lithium Niobate ($LiNO_3$) modulators, glass-on-silicon wavelength filters and multiplexers, and Indium Gallium Arsenide (InGaAs) photodetectors. In high-end applications, each device is commonly fabricated from a material that has optimal properties for the corresponding functionality, then aligned to submicron precision, and finally hermetically sealed in a "gold box". Then the optical devices, together with their driver IC, biasing and temperature controlling system, are assembled into an optical module. These packaging process are expensive and difficult to scale into volume. The path to address the challenges associated with this complex packaging, as seen by both academia and industry, is in creating complex photonic integrated circuits. Photonic integration was first proposed in late 1960s [3], not far behind electronic IC's, but has made much less progress. The electronic IC followed Moore's law nicely in the past-half century, i.e. device density was doubled by every 12 to 18 months, and achieved tremendous success. The number of transistors per chip has

rocketed up from 4 in the very beginning to over 10^9 nowadays. The first commercial "large-scale" InP PIC didn't appear on the market until 2005, with 10^2 devices integrated on a single chip [4]. The unique challenge of photonic integration is its requirements for a diversity of functionalities, including wave guiding, splitting, filtering, multiplexing, lasing, amplification, modulation, and detection. PICs that integrate such functions are traditionally built on InP, and more recently also on silicon.

InP is the only viable single material that can integrate most of the functions above. State-of-the-art InP PICs can transmit and receive 10-wavelength, polarization-multiplexed, quadrature phase shift keying (PM-QPSK) signals at 112 Gb/s, corresponding to an aggregated bandwidth of 1.12 Tb/s [5]. However, an active InP PIC requires many layers of epitaxy, in certain cases over 90 layers, and multiple etches. Consecutive etches depends on PIC functionality and may reach 6-7 steps [6]. Complicated epitaxial growth and etch tend to reduce device yield. InP platform is also limited by the wafer size, typically 3 inch, compared to silicon (12 inch or larger).

1.3 Silicon photonics

Silicon is transparent in the telecom wavelength, 1.3 μm to 1.6 μm, making it possible as a platform to build photonic devices. Moreover, the high refractive index contrast between silicon and silicon dioxide, 3.4 to 1.4, supports tight mode confinement and allows submicron waveguide cross-section and micron scale low-loss waveguide bends, enabling very dense integration. Sate-of-the-art complementary metal-oxide-semiconductor (CMOS) silicon processing technology developed by the IC industry can be leveraged for large volume manufacture with high yield and uniformity. However, silicon has its Achilles heel as a photonic material, for the following reasons: a) Due to

silicon large refractive index and high thermo-optic coefficient, silicon photonics device tends to be sensitive to geometry variations and temperature perturbations; b) Because of the center symmetry of silicon lattice, there is no direct electrooptical effect, hence efficient modulator is challenging; and c) Most critically, silicon is an indirect band gap material, making it prohibitively difficult to build lasers and photodetectors at telecom wavelengths. Note that silicon is not the best material for electronics in terms of absolute device performance either. The first transistor was demonstrated on germanium, and compound material such as Gallium Arsenide (GaAs) has much higher carrier mobility. Silicon became the dominating IC substrate material because of its manufacturability, which is valid for electronics as well as optics. To conquer these disadvantages and make efficient electrooptical devices, while maintaining the CMOS compatibility, is the fundamental topic of silicon photonics research.

Thanks to the foundational work by R. Soref, electrooptical modulation could be achieved utilizing by free carrier plasma dispersion effect [7]. It could be implemented either in the format of a *pn* junction or MOS capacitor overlapping with the waveguide mode [8]. The *pn* junction depletion region width or MOS capacitor accumulation carrier density are modulated respectively, creating a waveguide refractive index perturbation in response to the electrical driving signal. The refractive index perturbation leads to a phase change of the propagating optical signal, which can then be converted into intensity modulation by forming a micro-ring resonator or Mach-Zehnder interferometer (MZI). Micro-rings are more compact and energy efficient, while MZIs are advantageous in terms of thermal and processing tolerance. The work described in this thesis was

organized into three primary efforts, i.e. efficient and robust passive design, high-responsivity photodetector, hybrid laser integration, and thermal stabilization.

As transistors demonstrate various secondary effects that used to be negligible as they shrink, sub-micron silicon waveguides are more sensitive to fabrication errors than their counter parts on glass-on-silicon substrate. For example, a 10 nm core size variation is negligible for waveguides on the order of a few microns, but noticeably change the refractive index of submicron silicon waveguide. As simple as a waveguide mode doesn't have an analytic solution, the wave propagation in complex structures, such as a y-shape power splitter or waveguide crossing, is only manageable numerically. Relying on manual trial-and-error approaches to come up with high performance and robust device design is prohibitively inefficient. To conquer this challenge, particle swarm optimization (PSO) is implemented in silicon photonics design for the first time. Finite difference time domain (FDTD) method is used to model the optical mode evolution. PSO is coupled with FDTD to respond to the effect of geometry change on device performance and render the optimal design. Efficient Y-junctions, functioning as 3 dB power splitters, and waveguide crossing are demonstrated using this design methodology, as detailed in Chapter 2.

Germanium is the preferred light absorber for photodetectors in silicon photonics, because it is a CMOS compatible material and can be directly grown on silicon. However, germanium processing received much less research attention than silicon. Its ion implantation, dopant diffusion, and contact metal alloying properties are less understood and characterized. In Chapter 3, a novel germanium on silicon photodetector is proposed and demonstrated. Compared to conventional detectors, there is neither

doping in germanium and nor germanium metal direct contact. As a matter of fact, the only requirement to fabricate the device in addition to a silicon modulator flow is germanium epitaxy. It significantly reduces the fabrication complexity and ultimately the cost to build silicon PICs. Despite the simplified fabrication, device performance is significantly improved compared to the baseline photodetector, with high responsivity of 1.14 A/W, reduced low dark current of 0.12 μA, and enhanced 3 dB bandwidth of 40 GHz.

Laser integration on silicon is tackled in Chapter 4. An external cavity laser was built by butt coupling a reflective semiconductor optical amplifier (RSOA) with a silicon on insulator chip. Compared to bonding of III/V wafers, this approach is non-invasive and allows silicon and RSOA to be independently. We propose and demonstrate laser cavities on silicon using a Sagnac loop mirror and a micro-ring wavelength filter for the first time. The Sagnac loop mirror provided broadband reflection, which is simple to fabricate and robust compared to Bragg gratings. It also provides accurately controlled reflectivity, and negligible excess loss. Single mode operation is achieved by inserting a micro-ring wavelength filter into the cavity. I report a device lasing at 1551.7 nm, with 44 dB side mode suppression ratio, 1.2 MHz linewidth, and 4.8 mW on-chip output power. I also demonstrate QD RSOA based O-Band laser, and high speed transmission at 10 Gb/s and 40 Gb/s.

In Chapter 4, it is shown that the resonant wavelength of micro-rings can be lithographically controlled to a standard deviation of 3.6 nm, which then could be fine adjusted by thermal tuning. On the other hand, the large thermo-optic coefficient of silicon also leads the devices vulnerable to thermal perturbations in practical applications.

In Chapter 5, wavelength stabilization based on bandgap temperature sensor and active feedback control is demonstrated. It is a universal approach that doesn't rely on specific device functionality, and can be applied to micro-ring modulators, wavelength filters, and Echelle grating wavelength multiplexers.

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CHAPTER 2. PASSIVE DEVICE DESIGN AND OPTIMIZATION

Silicon has a high refractive index contrast over its oxide, 3.4 to 1.4, which allows optical field to be tightly confined in a submicron waveguide, with core sizes usually around 500 nm × 220 nm. The high confinement factor enables dense integration, but makes silicon photonics devices very sensitive to geometry variations normally seen in micro fabrication at the same time. Designing high performance and efficient passive devices has been a great challenge. I propose and demonstrate a design and optimization methodology based on finite difference time domain (FDTD) method and particle swarm optimization (PSO), which produces highly efficient, compact, and robust passive silicon photonics devices. Two device examples, a Y-junction 3 dB power splitter with insertion loss as low as 0.28 ±0.02 dB, and a waveguide crossing with insertion loss 0.017±0.005 dB and cross talk lower than -40 dB, both with high cross-wafer uniformity, are presented.

2.1 Silicon waveguides

Since J. Kilby made the first integrated circuit chip consisting of four transistors in 1954, it was not obviously a good idea to integrate multiple devices in a monolithic circuit, since initial yield of even single transistors was poor. ICs keep getting more powerful and energy efficient, and their application has penetrated into every corner of modern society. Today even phones have billions of transistors monolithically integrated. Having witnessed the enormous success of monolithic integration for electronics, it would be natural for optical engineers to think about putting multiple optical devices onto one substrate. The first proposal of photonic circuit integration was published on the Bell

System Technical Journal in 1969 [1], but the first commercial application didn't occur until 2005, with about 10^2 devices on an indium phosphide chip [2].

At the same time, silicon was extended to more other fields other than just ICs. One good example is micro-electromechanical systems (MEMS). In 1987, R. Soref published the pioneering work on free carrier plasma effect, which became the foundation for electro-optic modulation in silicon. But the first modulator with plausible bandwidth wasn't demonstrated until 2004 [4]. The first product occurred as a transceiver in an active optical cable in 2007 [5] and the first silicon PIC for coherent metro and long haul transceivers was demonstrated in 2014 [6].

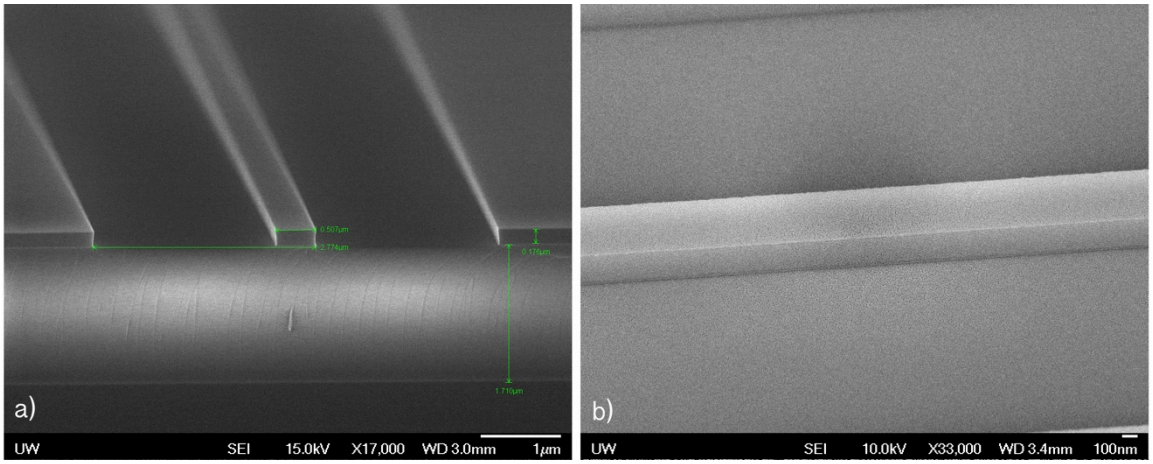

Fig. 2.1 SEM image of submicron silicon waveguides: a) cross-section and b) perspective view. Both the silicon device layer and buried oxide is clearly visible in a). The waveguides are patterned using JBX-6300FS electron beam lithography system and etched using Inductively coupled plasma reactive ion etcher.

One roadblock, among others, had been fabricating low loss silicon waveguides. Silicon waveguide loss was reduced from 32 dB/cm to 0.026 dB/cm [7, 8], enabling efficient on-chip routing and other devices. Similar effort was also seen in fiber optics, where fiber loss decreased from 20 dB/km to 0.2 dB/km. The reason for high waveguide loss is its submicron core cross-section and tight confinement, as shown in Fig. 2.1 and

2.2. Such capability to concentrate optical power sparked considerable research on nonlinear optics [9]. One significant drawback is that modal field is still intense at the silicon waveguide core and oxide cladding interface, where it is usually rough due to the nature of dry etching. The waveguide sidewall roughness causes scattering and results in waveguide loss. The journey to reduce waveguide loss has been a combined effort of waveguide design and fabrication, i.e. to decrease optical mode intensity near the sidewall by engineering waveguide geometry and also smooth out the interface using silicon processing techniques, such as oxidation.

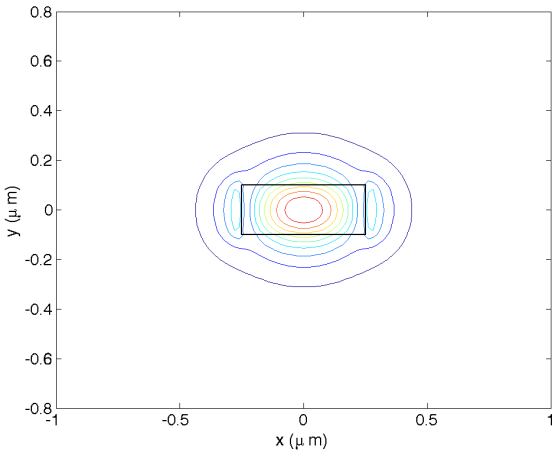

Fig. 2.2 Contour plot of silicon waveguide mode. Oxide cladding is assume both under and on top of the silicon core, illustrated by the black rectangle.

2.2 Passive device design challenge

One of the other shortcomings in silicon photonics devices is the high sensitivity to geometry variation, also a natural outcome of extremely compact device size. This is similar to what has been seen in electronics, secondary effects, such as sub-threshold conduction, become non-negligible as transistor shrinks. I use a simple Y-shape branch 3 dB power splitter, or Y-junction, as an example. A Y-junction is theoretically lossless, while this is not the case due to finite resolution of micro fabrication. Sharp corners in

layout usually get rounded out on silicon. Sharp tips violate the minimum feature size rule of a lithographic process and can be easily detected by design rule checking (DRC) routines. The possible detrimental effects of this violation in fabrication includes peeling off of photoresists, shallower etch in the narrow gap, and voids in subsequent oxide cladding deposition. All of the above degrade device performance and lower yield. To avoid the DRC violation, we used to put a butt waveguide at the splitting position, as shown in Fig. 2.3. The butt waveguide is an abrupt discontinuity, which causes light scattering and back reflection. It does satisfy the design rules, but sacrifices device performance.

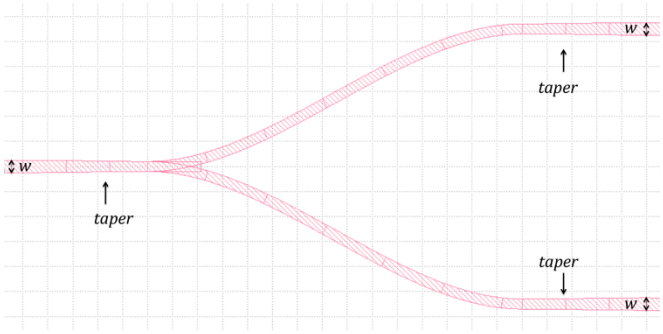

Fig. 2.3 Layout of a conventional Y-junction. A butt waveguide is inserted to comply with design rules

The insertion loss of this device can be measured using the test structure shown in Fig. 2.4. Grating couplers are used for on and off chip light coupling to a single mode fiber. Light from a test laser is launched into the left port, and detected from either the center or right port. If there is no excess loss, detected power will be 3 dB lower than that of a control grating coupler loop without the device under test. The measured spectra are plotted in Fig. 2.5. The parabolic line shape is determined by the grating coupler spectral response. Ripples on the spectrum are from the reflection of the gratings, which forms an implicit Fabry-Perot cavity. The offset in vertical direction between the green and blue curve shows the insertion loss caused by the Y-junction, which is 4.2 dB. Taking out 3

dB from intrinsic power splitting, the excess loss of this device is 1.2 dB, which is too high for practical applications. For example, a Mach-Zehnder modulator with two such Y-junctions will cause 2.4 dB insertion loss, let alone the loss from fiber coupling

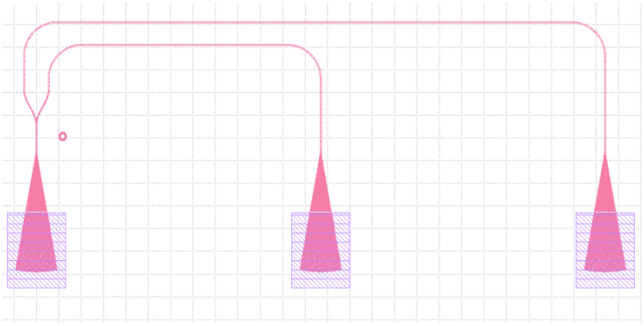

Fig. 2.4 Y-junction insertion loss test structure

and free carrier absorption, making the silicon modulator less competitive to the commercial Lithium Niobate ($LiNO_3$) modulators, which usually have about 4 dB fiber to fiber loss.

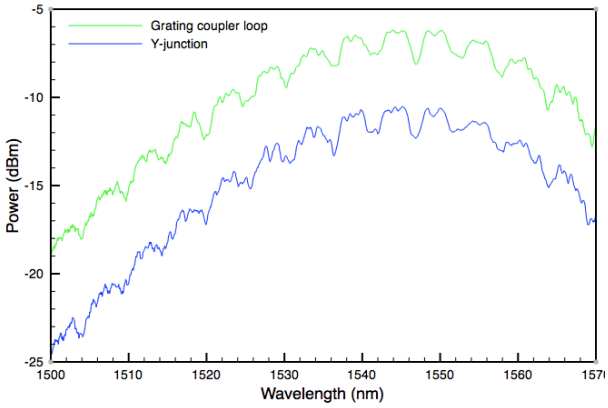

Fig. 2.5 Spectra of the Y-junction test structure and a control grating coupler loop

2.3 FDTD simulation

Since there is no analytic solution even for a silicon waveguide mode, designers have to rely extensively on numerical simulations. When the device size is comparable to the operating wavelength, its electromagnetic properties are usually simulated by finite different time domain (FDTD) method. In the differential form of Maxwell's equations

2.1 – 2.2, it can be seen that the time derivative of H-field is dependent on the curl of E-field, and vice versa.

$$\nabla \times E = -\mu \frac{\partial H}{\partial t} \tag{2.1}$$

$$\nabla \times H = \varepsilon \frac{\partial E}{\partial t} - J \tag{2.2}$$

In Cartesian coordinate system, Eq. 2.1-2.2 is equivalent to the following scalar Eq. 2.3-2.5,

$$-\mu \frac{\partial H_x}{\partial t} = \frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z} \tag{2.3}$$

$$-\mu \frac{\partial H_y}{\partial t} = \frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x} \tag{2.4}$$

$$\mu \frac{\partial H_z}{\partial t} = \frac{\partial E_x}{\partial y} - \frac{\partial E_y}{\partial x} \tag{2.5}$$

To solve the equations numerically, the electromagnetic fields are discretized in a style proposed by Yee [10], in which the field components are discretized at slightly different special positions as shown in Fig. 2.6.

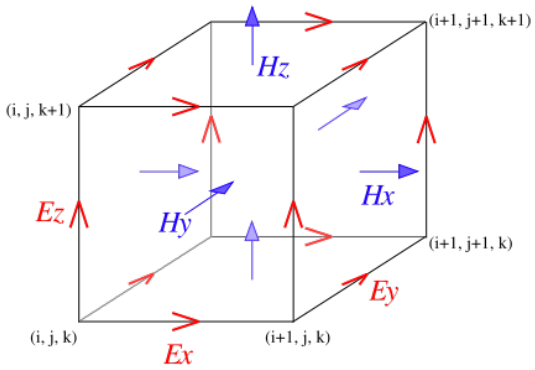

Fig. 2.6 Yee cell used in FDTD simulation

After discretization, the H-field at any point can be updated in time using the stored H-field value and curl of E-field at the same spatial volume, for example, discrete form of Eq. 2.3 is shown below.

$$\mu \frac{H_x^{n+\frac{1}{2}}\left(i,j+\frac{1}{2},k+\frac{1}{2}\right) - H_x^{n-\frac{1}{2}}\left(i,j+\frac{1}{2},k+\frac{1}{2}\right)}{\Delta t} = \frac{E_y^n\left(i,j+\frac{1}{2},k+1\right) - E_y^n\left(i,j+\frac{1}{2},k\right)}{\Delta z} - \frac{E_z^n\left(i,j+1,k+\frac{1}{2}\right) - E_z^n\left(i,j,k+\frac{1}{2}\right)}{\Delta y} \tag{2.6}$$

Other field components can be updated next in the same way. This process is repeated until the desired transient or steady state electromagnetic field behavior is fully solved.

An example of FDTD simulation on the aforementioned Y-junction is shown in Fig. 2.7. Light in the waveguide fundamental mode is launched from the left with unit E-field value. Then the field pattern can be recorded at either branch. Note that the ratio of captured power to launched power is not necessarily the device insertion loss, because high order mode might be excited at the splitting point. Since the waveguide is short, although high order modes are leaking out, they may still be captured by the field monitor. Making the waveguide much longer will help, but at the price of significantly longer simulation time. The power in the fundamental mode can be extracted by the mode overlap integral, as defined by Eq. 2.7.

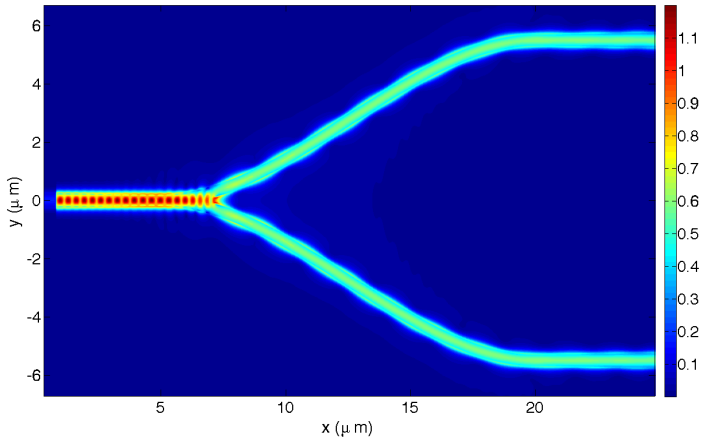

Fig. 2.7 E-field pattern of Y-junction simulated by FDTD

$$P = \langle \varphi_0 | A | \Psi \rangle = \int dA \begin{pmatrix} E_{x0}^* & E_{y0}^* & E_{z0}^* & H_{x0}^* & H_{y0}^* & H_{z0}^* \end{pmatrix} \begin{pmatrix} 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} Ex \\ Ey \\ Ez \\ Hx \\ Hy \\ Hz \end{pmatrix} \tag{2.7}$$

2.4 Particle swarm optimization

With the FDTD simulation, we can model the electromagnetic response of an arbitrary geometry. However, the device design challenge hasn't been addressed yet. We only know how to evaluate the insertion loss of a given device design. It's not clear how to modify the device geometry to reduce the Y-junction insertion loss. In particular, since FDTD is a computing and memory intensive simulation, the manual trial and error approach is prohibitively inefficient. If we can generate a number of designs, chances are one will have better performance than the rest. If we can further pick up the best one and keep improving on it, a satisfactory design might emerge. This approach leads me to the idea of coupling FDTD with some optimization algorithm.

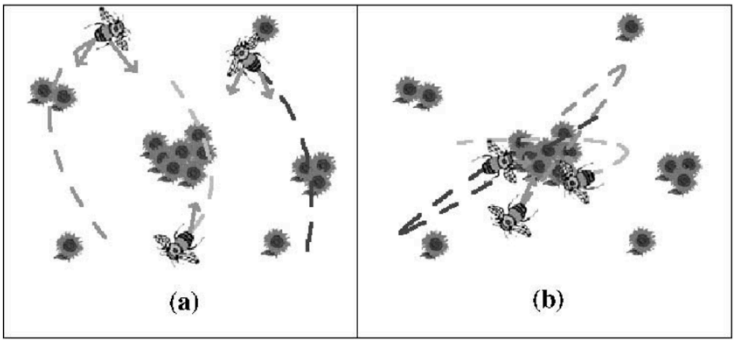

Fig. 2.8 (a) Like bees searching for a spot with the highest flower density, particles in PSO are attracted both to the best position found by the entire swarm and the best location individually encountered by the particle. (b) Eventually, after being attracted to areas of high flower concentration, all the bees swarm around the best location over-flying it only to be pulled back in after failing to find a higher concentration of flowers elsewhere [12].

Particle swarm optimization (PSO) was originally inspired by the social behavior of flocks of birds or schools of fishes [11], and has been successfully applied to electromagnetic optimization problems [12]. I decided to use it for silicon photonics device design and optimization, for the first time, to the best of my knowledge. In PSO,

the potential solutions, called particles or agents, are initialized at random positions with random velocities in the parameter space. A figure of merit function is defined to evaluate the particle position according to the optimization goal. The best position for each individual particle is recorded, as well as a global best position ever achieved by any particle in the swarm. The position of a particle is updated by the following equation,

$$x_n = x_n + \Delta t * v_n \tag{2.8}$$

$$v_n = \omega * v_n + c_1 * rand() * (p_{best,n} - x_n) + c_2 * rand() * (g_{best,n} - x_n) \tag{2.9}$$

where v_n and x_n are particle's velocity and position in the n^{th} dimension of the parameter space, and $p_{best,n}$ and $g_{best,n}$ are individual and global best positions, respectively. Apparent from Eq. 2.8, the new velocity is the old velocity scaled by ω and increased in the direction of $p_{best,n}$ and $g_{best,n}$. ω, known as the inertial weight, is a measurement of how much a particle would like to stay at the old velocity. c_1 determines how much a particle is influenced by the memory of its best position, thus sometimes called cognitive rate. And c_2 is a factor determining how much the particle is affected by the global best position of the whole swarm, hence called social rate. The two random numbers *rand*(), uniformly distributed between 0 and 1, are used to simulate the unpredictable behavior of natural swarm. It can be seen that the particle velocity is large when it is far from $p_{best,n}$ and $g_{best,n}$, becomes smaller as it is closer to the best position and gets pulled back after flying over. The optimization is stopped when the figure of merit is good enough or a large number of iterations is reached.

2.5 Y-junction

I. Y-junction design

Our goal was to design a compact, low loss and wavelength insensitive Y-junction for submicron silicon waveguide, compatible with typical CMOS photonic processes, where 193 nm or 248 nm steppers are commonly used. A minimum feature size of 200 nm was assumed during the design, which would not break the designs rules, thus ensuring optimal yield. Silicon waveguide geometry is 500 nm wide and 220 nm high and the taper width is 0.5 µm at the input and 1.2 µm at the output, as shown in Fig. 2.9(a). The length of the taper connecting input and output waveguides was set to 2 µm to keep the device compact. The size of Ge-on-Si photodetectors and absorption modulators are usually on the order of 10 µm, and *pn* junction modulator with phase shifter length of 50 µm has been demonstrated [13]. A simple passive component like a Y-junction should be compact enough to be part of a more complicated active device or an integrated optical circuit. The Y-junction is symmetric in the propagation direction to ensure balanced output at the two branches.

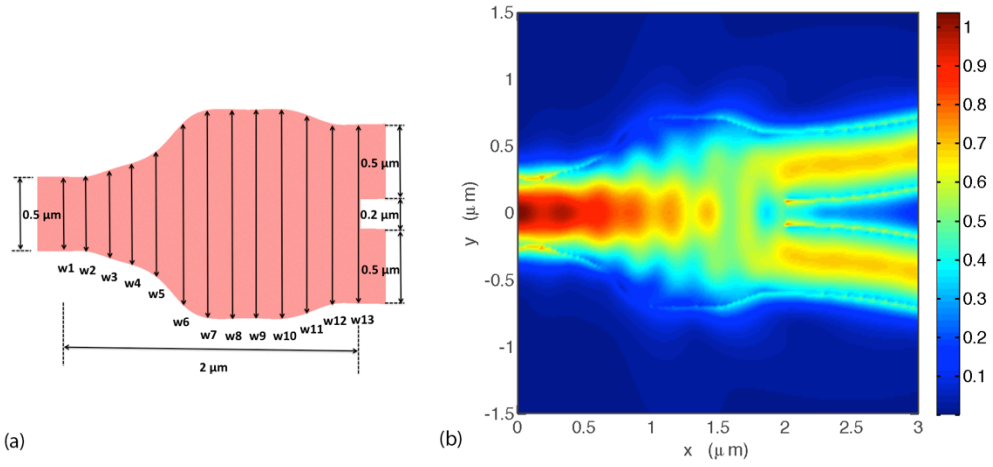

Fig. 2.9 a) Schematic of device layout. The taper geometry is defined by spline interpolation of w1 to w13. b) Contour plot of simulated E-field distribution at 1550 nm wavelength.

In this design, the taper was first digitalized into 13 segments of equal length. The width of each segment, labeled as w1 to w13 in Fig. 2.9(a), was optimized to achieve low loss coupling. Taper geometry is defined by spline interpolation of these 13 points. The optimization figure of merit (FOM) was the power in the TE_0 mode at either branch. It was calculated by the overlap integral of the TE_0 mode of a 500 nm × 220 nm waveguide with the detected field at the output branch at wavelength 1550 nm. Note that it is not proper to set the total detected power to be FOM, since higher order modes will leak out of the waveguide along the way. Maximizing the power effectively reduces the scattering and back-reflection. The swarm population was set to 30. 2D FDTD was used as an approximation of 3D FDTD for computing efficiency during optimization. A commercially available code was used [14]. Within 50 iterations, one solution with sub-0.2 dB insertion loss emerged, as shown in Table 2.1. Then 3D FDTD was run on this solution to double check the result with a mesh equal to 1/34 of the free space wavelength. The insertion loss was determined to be 0.13 dB. Scattering is negligible, as shown in the contour plot of electric field in Fig. 2.9(b). There is an interference pattern at the input end, indicating existence of very weak back-reflection. The normalized transmission and reflection power as a function of wavelength is plotted in Fig. 2.10. It can be seen that both the transmission and reflection are virtually wavelength insensitive, with variation below 1% and 0.5% over the wavelength range from 1500 nm to 1580 nm.

Table 2.1. Taper width in μm

w1	**w2**	**w3**	**w4**	**w5**	**w6**	**w7**	**w8**	**w9**	**w10**	**w11**	**w12**	**w13**
0.5	0.5	0.6	0.7	0.9	1.26	1.4	1.4	1.4	1.4	1.31	1.2	1.2

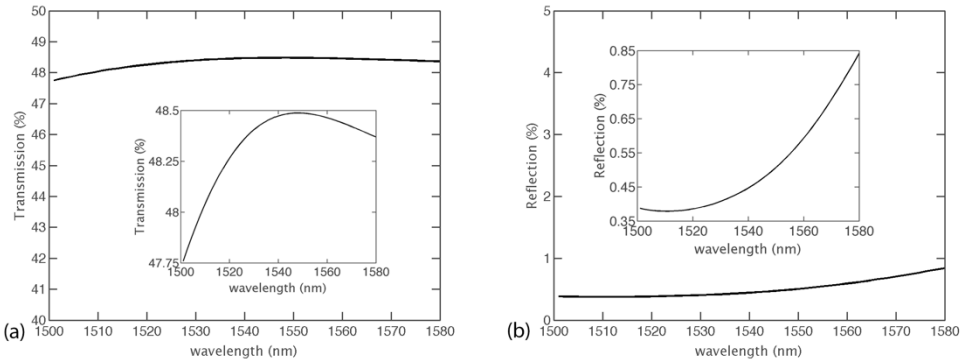

Fig. 2.10 Simulated (a) power transmission and (b) reflection as a function of wavelength, with zoomed-in view in the insets.

II. Device fabrication

The optimized device was prototyped by participating in a multi-project wafer (MPW) run offered by *OpSIS foundry*. Starting substrate was an 8-inch SOI wafer, with 220 nm, 10 ohm-cm p-type top silicon film, 2 μm buried oxide on top of a silicon handle. Photo mask was fabricated in a commercial mask shop with grid resolution much finer than the device minimum feature size. Waveguides were patterned using 248 nm UV lithography followed by dry etching. Then 2.3 μm of oxide was deposited as top cladding. Light coupling on and off the chip was achieved by grating couplers (GC). Two kinds of characterization structures were laid out, as shown in Fig. 2.13. A cascade of Mach-Zehnder structures formed by butt coupled Y-junctions was used to measure the insertion loss. The other structure has the three terminals of the Y-junction connected to three grating couplers to measure the two outputs directly. In both cases, the bend radius of the connecting waveguides is 5 μm, large enough to introduce negligible bending loss. The grating coupler pitch is 127 μm, determined by the pitch of our fiber array. Simple GC loops, i.e. two GCs connected by a U-turn waveguide, were used as a reference structure. A photo of the fabricated chip is shown in Fig. 2.11. Tiles used around the

devices to achieve a certain filling ratio are visible in the photo. A SEM image of the optimized Y-junction is also shown in Fig. 2.12.

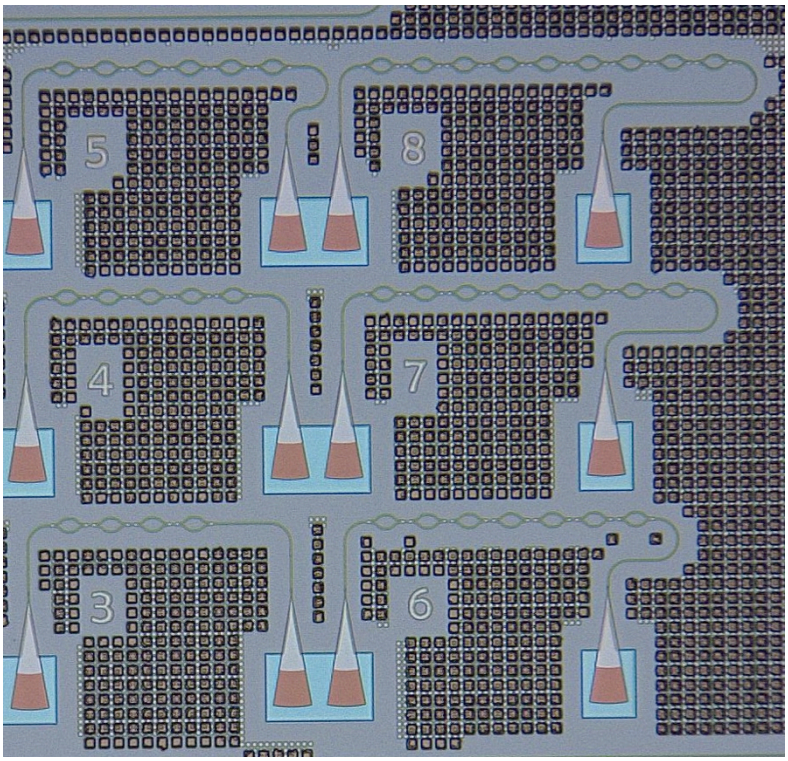

Fig. 2.11 Chip photo of cascaded Y-junction characterization structures

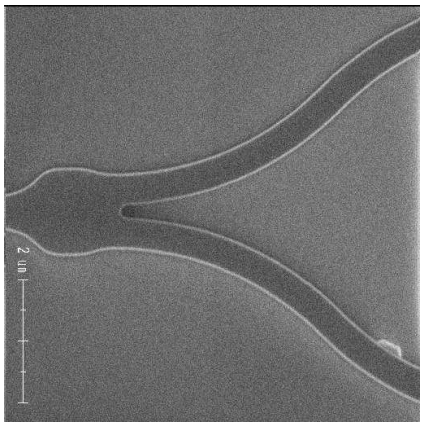

Fig. 2.12 SEM image of the fabricated optimized Y-junction

III. Y-junction characterization

Devices were measured on a wafer scale setup that can map the wafer coordinate to the stage coordinate, so that any device can be easily probed after initial alignment. Light from a tunable laser was coupled into the device under test (DUT) via a polarization maintaining (PM) fiber and grating coupler, then to a photodetector through another grating coupler and PM fiber. Chuck temperature was set to 35 °C, slightly higher than room temperature, where it is most stable. The device performance reported in this paper is not expected to vary strongly as a function of temperature. Reticle size on the wafer is 2.5 cm × 3.2 cm. Excluding incomplete dies on the edge, Y-junctions in 26 dies were tested to characterize the cross-wafer performance.

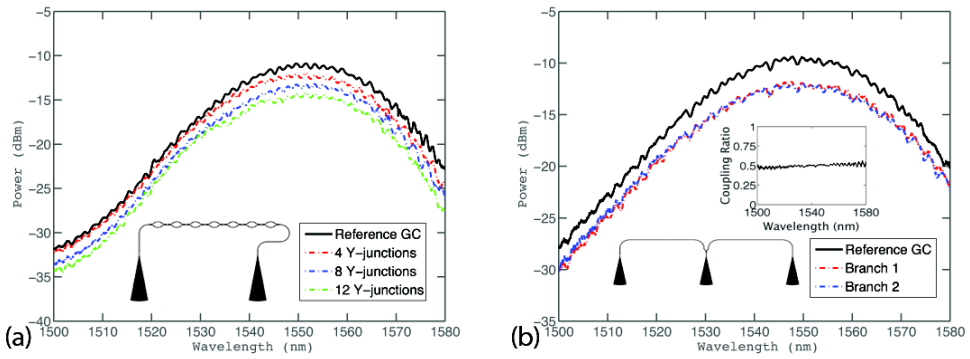

Fig. 2.13 Typical measured spectra and corresponding test structure. The inset in (b) gives coupling ratio as a function of wavelength. Parabolic line shape and ripples are determined by grating coupler spectral response and imperfect linear polarization, respectively, as discussed in the main text. Offset in y-axis is from Y-junction insertion loss.

Typical measured spectra and corresponding test structure are shown in Fig. 2.13. The parabolic-like shape is determined by the grating coupler spectral response. The grating coupler design used here works for TE mode only, which has over 20 dB selectivity over TM mode at the fiber array angle we used for testing. If non-perfectly linear polarization light is fed into the grating coupler from a fiber, both *s* and *p* polarization, which are not in phase, partially overlap with the TE mode of grating

coupler and couple into the waveguide. They interfere and create ripples on the spectrum. The ripple magnitude scales with the amount of fiber polarization mixture. With a simple fiber birefringence based polarization controller, we typically manage to control the fringes within 0.5 dB peak to peak. It is possible to reduce the fringe even further with more dedicated polarization adjustment.

It is difficult to measure sub-0.5 dB insertion loss from a single device. Therefore, test structures with different numbers of Y-junctions in the loop were used to extract the insertion loss. For each transmission spectrum, a 30 nm wavelength span near the peak was fitted by a parabolic curve, and the maximum of the parabolic fit was used as the peak power in insertion loss calculation to minimize the effect of ripples. The measured peak power as a function of number of Y-junctions is plotted in Fig. 2.14(a). Blue dots are test data, and red line is a linear fit. The slope of the line gives the insertion loss in dB per Y-junction, 0.27 ± 0.01 dB in the case of the DUT. Loop baseline losses – about 11 dB, mainly due to grating coupler insertion loss – are the same for all structures, thus won't affect the slope of the fitting line.

Photonic devices performances are sensitive to geometry variations, which can be from either the SOI wafer itself, exhibiting typically ± 20 nm thickness variation for an 8 inch SOI wafer with 220 nm top silicon, or the fabrication process flow. Resonant wavelengths variation on the order of 10 nm is observed in devices fabricated by CMOS high-volume tools [15-17]. As a basic building block, high cross-wafer uniformity is as important as other metrics such as compact footprint and low insertion loss. For this Y-junction design, a major contribution to performance non-uniformity is the silicon film thickness variation. Our 3D-FDTD simulation indicates excess loss is 0.2 dB at thickness

of 200 nm and increases to 0.3 dB at 240 nm. A contour plot of insertion loss is shown in Fig. 2.14(b). From the histogram in Fig. 2.14(c), we can see that the insertion loss is bounded between 0.23 and 0.32 dB, with a cross-wafer average of 0.28 dB and a standard deviation of 0.02 dB. Low cross-wafer variation confirms that our device is not fabrication sensitive, and fully addresses the DRC violation issue of conventional Y-junctions. Thus it can be a reliable component of an integrated photonic system.

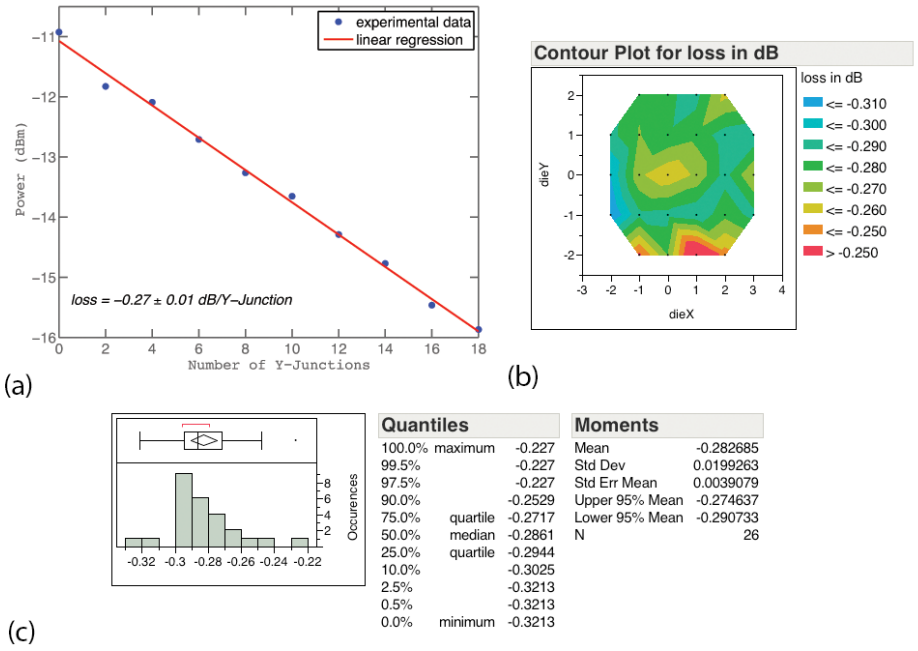

Fig. 2.14 (a) Measured power as a function of the number of Y-junctions in the GC loop. Blue dots are measured peak optical power. Red line is linear fit; (b) Contour plot of measured Y-junction insertion loss across the wafer; and (c) Histogram of 26-reticle test data of measured insertion loss, showing mean value of 0.28 dB and standard deviation of 0.02 dB.

It is shown in [18] that etch residues or air voids in the gap defined by sharp corners in the layout will lead to non-uniform output at two branches of the Y-junction. In Fig. 2.13(b), the spectra of two branches overlap over the whole testing wavelength range, indicating balanced output power and wavelength insensitive coupling ratio. From the simulation, we note that the coupling efficiency does roll off at shorter wavelength, as the

mode confinement gets tighter. For example, calculated excess loss is about 0.6 dB at wavelength 1310 nm. So for data communication wavelength of 1310 nm, the Y-junction geometry has to be redesigned or scaled properly.

2.6 Waveguide crossing

To further prove the viability of the FDTD + PSO design approach, I show another device example – an ultra low-loss silicon waveguide crossing working at O-Band. As the number of devices per chip increases, the complexity for device interconnects scales up quickly. The electronics industry addresses this problem by adding multiple metal layers. In a modern CMOS process, over ten layers of metal are common for local and global signal routing. However, a similar approach doesn't serve PICs well. Electronic connection between different layers is compact and efficient using metal plug vias, while evanescent or grating coupling of waveguides on different layers is bulky and lossy.

However, photons are bosons and electrons are fermions, which have distinctly different properties. In free space, two optical beams don't interfere even if they directly intersect. This is still true on chip, where to waveguides can cross and still maintain their optical signal. But at the same time, due to the lack of guiding at the intersection, the mode diverges, which causes over 1 dB insertion loss and -10 dB cross talk. In principle, it is possible to reduce insertion loss and cross talk by reducing the divergence using multi-mode interference. A dedicated number of modes with specific amplitude ratio and phase relationship needs to be created, which is challenging, if possible at all, using analytic approach or only FDTD. I show how FDTD and PSO work together to guide us to a right solution. The waveguide crossing is decomposed into four identical tapers.

Then the taper is digitalized into 13 sections, similar to what we do for the Y-junction, as shown in Fig. 2.15.

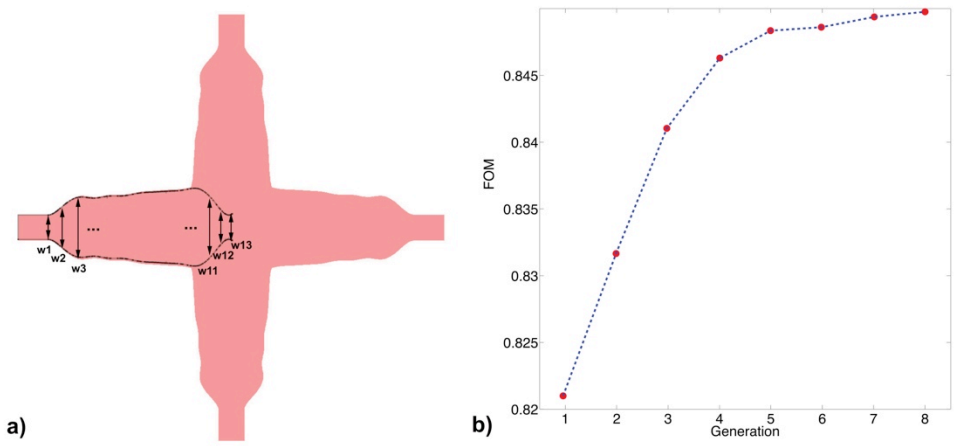

Fig. 2.15 a) Schematic device layout. The waveguide crossing consists of four identical tapers defined by w1 to w13; b) Evolution of FOM in the first 8 generations.

The optimization figure of merit (FOM) was transmission minus back reflection and crosstalk, as described in Eq. 2.10,

$$FOM = T - R - Xtalk \tag{2.10}$$

In the FOM calculation, the average value at 10 wavelength points sampling the entire O-band was used to minimize wavelength dependence of the device. The swarm population was set to 20. 2D FDTD was used as an approximation of 3D FDTD for computing efficiency during optimization. *w1* and *w13* were set to a fixed value of 0.42 μm as the I/O interface waveguide width. Initial values of *w2*-*w13* were those from the C-band waveguide crossing scaled by 1.31/1.55 [19]. Improvement of FOM in the first few generations was plotted in Fig. 2.15(b). Interaction from designers was sometimes needed, mainly to reset the range of optimization variables if best solution converged at the boundary. Taper length was set at a fixed value to reduce optimization time.

Optimized device geometry based on the methodology above is not unique. We chose two taper length values, 3 μm and 4.5 μm, and got one optimized solution for each case, as summarized in Table 2.2. The FOM for Device A and Device B are similar. Device B was designed for minimal device footprint, 6 μm × 6 μm. Device A is slightly larger, 9 μm × 9 μm, and has higher fabrication tolerance.

Table 2.2 Optimized waveguide crossing geometry. *L* and *w1*-*w13* are in μm

Dev.	*FOM*	*L*	*w1*	*w2*	*w3*	*w4*	*w5*	*w6*	*w7*	*w8*	*w9*	*w10*	*w11*	*w12*	*w13*
A	0.971	4.5	0.42	0.78	1.2	1.312	1.316	1.338	1.423	1.466	1.585	1.726	1.99	2.0	0.42
B	0.987	3	0.42	0.74	1.03	1.00	1.07	1.08	1.17	1.21	1.24	1.28	1.32	0.9	0.42

The field pattern of Device A, as well as the simulated transmittance, reflectivity, and crosstalk as a function of wavelength are plotted in Fig. 2.16. The mode evolution from TE_0 to higher order modes inside the taper is clearly illustrated. At the intersection, despite lacking a guiding structure, the field doesn't diverge when passing through it due to carefully engineered multimode interference. Some very weak scattering is also visible, corresponding to reflection and crosstalk lower than -30 dB. Note that most of the transmitted power stays in the TE_0 mode, while only a small portion of scattered power is in the TE_0 mode. Because the I/O waveguide supports only the TE_0 mode, high order modes will leak out along the way, which further reduces crosstalk. As we calculated FOM based on an average of multiple wavelengths, the optimized device doesn't have strong wavelength dependence. Transmittance, reflectivity, and crosstalk are all relatively flat over the entire O-band.

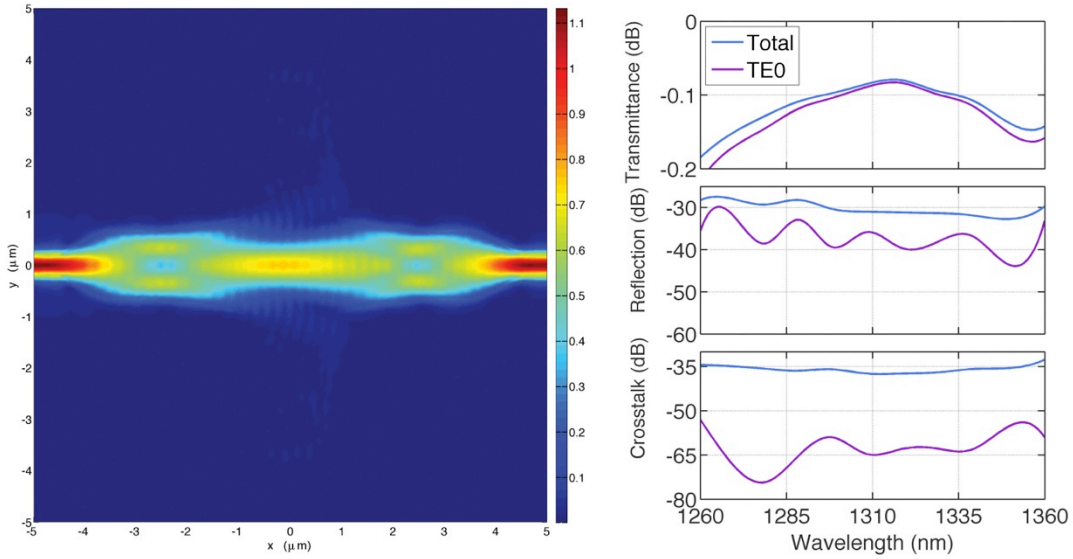

Fig. 2.16 Electric field profile and simulated transmittance, reflection, and crosstalk of waveguide crossing design A

Since each waveguide crossing was expected to have extremely low loss, we cascaded different numbers of devices in a waveguide loop, as shown in Fig. 2.17(a). Note that the parabolic spectrum was determined by GCs. A reduction in power indicates extra losses added by a larger number of crossings. The slope of transmission power as a function waveguide crossing count in the loop gives insertion loss in dB per crossing. A second group of characterization structures was utilized to measure the crosstalk, as shown in Fig. 2.17(b). Device B was measured to have an average insertion loss of 0.19±0.02 dB and crosstalk better than -35 dB, with 6 μm × 6 μm footprint, roughly consistent with our projected value. Due to lithography proximity effect, insertion loss of Device A is lower than 0.02 dB, specifically 0.017 dB in Fig. 2.17(c), which is better than the simulated result.

We add a brief comment on the measurement of crosstalk, as determined by the data shown in Fig. 2.17(b). Crosstalk was measured by aligning to the outer two grating couplers of the bottom device layout (with three couplers) shown in Fig. 2.17(a). The intermediate grating coupler was then already aligned to the intermediate port in our 127 μm pitch fiber array. An optical transmission spectrum from the leftmost coupler to the central coupler was then measured, which should indicate no optical transmission in the ideal case of no crosstalk. In fact, a spectrum with more than 35 dB excess loss as compared to the leftmost to rightmost coupler spectrum was seen. One may note that the spectrum shown for crosstalk in Fig. 2.17(b) is near the optical noise floor and has a high-frequency set of fringes. This may indicate that in fact, coupling from an alternative optical path is occurring via the silicon substrate, thus implying that the true crosstalk is even better than what we report. However, we adopt the most conservative stance and assume all coupled light for this experiment is due to non-idealities in our device. We also noted that insertion loss is insensitive to wavelength over the entire O-Band, Fig. 2.17(d), matching our simulation in Fig. 2.16.

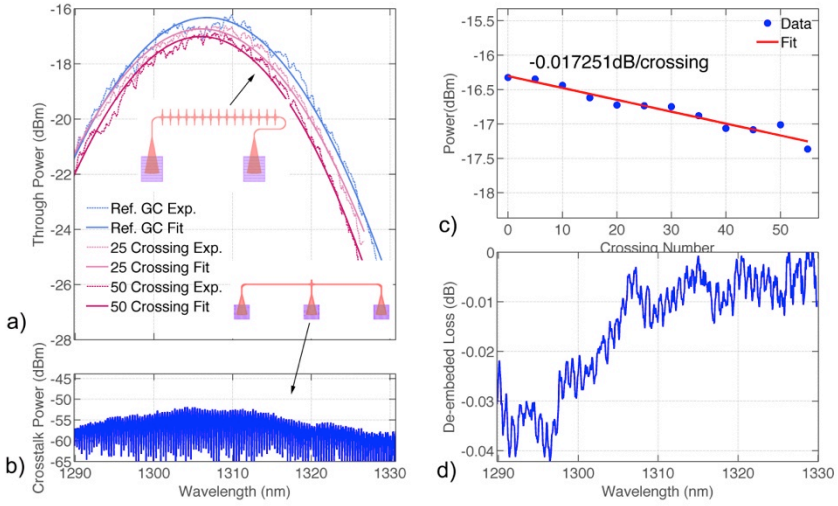

Fig. 2.17 Measured insertion loss and crosstalk of Device A. a) Insertion loss characterization structure and corresponding measured spectrum. Parabolic line shape and ripples on the spectrum are determined by GCs, and reduction in power shows additional loss added by a larger number of waveguide crossings; b) Crosstalk characterization structure and measured spectrum from the outer two GCs; c) The slope of peak power in a) as a function of waveguide crossing count gives insertion loss in dB/Crossing; d) De-embeded wavelength dependence of crossing insertion loss.

To serve as a reliable building block of complex photonics integrated circuits (PICs), device yield and uniformity are as important as the absolute performance of a single device itself. With reticle size equal to 2.5 cm × 3.2 cm, the 8-inch wafer was divided into 30 dies, excluding incomplete dies at the edge. I performed cross-wafer test on the device to study possible local and global effects on the device. Insertion loss distribution contour and statistics of Device A are illustrated in Fig. 2.18. As this device has a larger footprint, and a smoother geometry determined by spline interpolation, it is not sensitive to non-idealities such as SOI epi-thickness variation and processing non-uniformities. Cross-wafer insertion loss mean is 0.0168 dB, with standard deviation of 0.0047 dB. The uniformity confirms this device can be readily used for building PICs on chip.

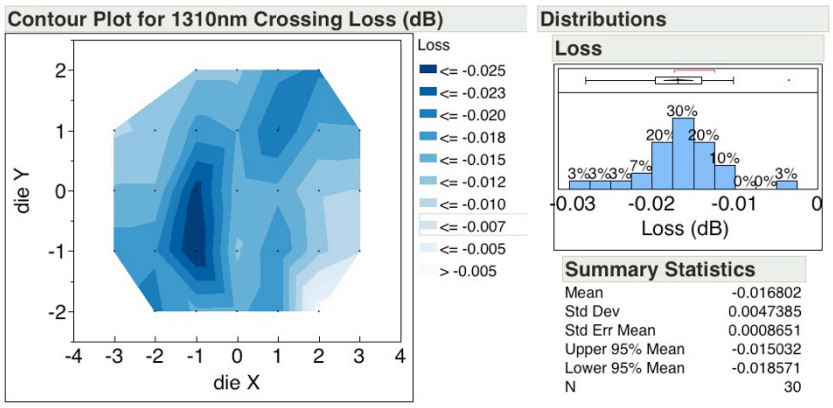

Fig. 2.18 Waveguide crossing cross-wafer insertion loss distribution

2.7 Summary

In this chapter, fabrication sensitivity of submicron silicon photonics devices is illustrated. A design methodology based on FDTD and PSO was developed to address this challenge. Two example devices, a Y-junction and a waveguide crossing, designed using this methodology are described in detail, both of which are compact and extremely low-loss. These two devices can be readily used to serve as building blocks of more complicated PICs. The design methodology is universal and can be used for other devices as well.

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CHAPTER 3. FLOATING GERMANIUM PHOTODETECTOR

Lower power consumption is a critical requirement for optical transceivers, especially in data center and metro applications, which is sensitive to volume and cost. A typical link power budget is around 9 dB. For example the IEEE 802.3 40GBASE-LR4 has 6.7 dB allocated for channel insertion loss and 2.3 dB for penalties [1]. Due to the large mode mismatch between glass fibers and submicron silicon waveguides, on-and-off chip coupling loss is usually quite high, over 1 dB in a mature commercial process [2]. In some cases, device insertion loss could be significantly reduced by design optimization as described in Chapter 2. However, in other cases, insertion loss and device efficiency are orthogonal. For instance, in silicon electro-optic modulators, higher doping results in higher modulation efficiency, but also increases insertion loss at the same time. Insertion losses of state of the art silicon modulators reported in both [3, 4] are over 5 dB. Link power budget often emerges as a tight constraint during design of silicon based data links. A photodetector with high responsivity could compensate for some of the channel insertion loss, and help satisfy the required link power budget. Based on thin device layer of SOI wafers used in silicon photonics and self-faceting of epitaxy germanium, I propose a photodetector that eliminates the needs for doping Ge and direct Ge-Metal contact. The device is measured to have 1.14 A/W responsivity at 1550 nm wavelength, 40 GHz 3-dB bandwidth, and less than 1 μA dark current.

3.1 Germanium hetero-epitaxy on silicon

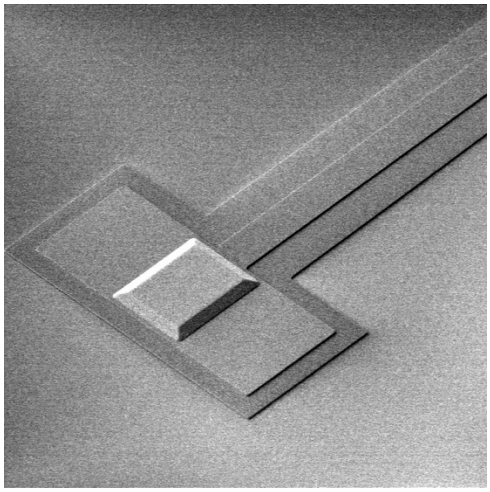

Fig. 3.1 An SEM image of germanium directly grown on silicon. The germanium base width is 8 μm × 11 μm

Due to the 4% lattice mismatch, hetero-epitaxy of germanium on silicon used to problematic, because of high surface roughness from island growth and high threading dislocation density in the germanium epi layers. Colace et al showed a two step-step ultrahigh vacuum / chemical vapor deposition (UHV/CVD) could be used to grow flat Germanium epilayers with 0.5 nm room-mean-square surface roughness [5]. Then Luan et al reported post epitaxy cyclic thermal annealing could reduce the threading dislocation density to 2.3×10^{6} cm^{-2} because of thermal stress induced dislocation glide and annihilation [6]. For selectively grown germanium, because mesa sidewalls are effective dislocation sinks, dislocation defect free small mesas were observed. A typical Germanium growth thus is first depositing a buffer layer of a few tens of nanometers at low temperature around 300 °C, then fast growth higher temperature, above 500 °C, to 500 nm to 1 μm, and finally annealing 800 – 900 °C for a few minutes to reduce dislocation density. Such procedure produces device quality germanium that has been widely reported [7-13]. An SEM image of a rectangle germanium mesa of 8 μm × 11 μm

base width is shown in Fig. 3.1. Similar to the anisotropic wet etch of silicon, which naturally stops at the (111) surface due to a much slower etch rate, crystal germanium growth rate is different in different directions. The germanium geometry also depends on the trench angle of the oxide hard mask, and can be projected by the Wulff construction model [14]. In Fig. 3.1, the germanium sidewall is 25° from the wafer surface, determined the angle between <311> and <100> crystal orientations.

3.2 Conventional p-i-n detectors

Waveguide-coupled *p-i-n* Ge-on-Si detectors have attracted extensive attention due to their high bandwidth, good responsivity and low dark current. Ge-on-Si detectors with lateral and vertical *p-i-n* junction configuration are illustrated in Fig. 3.2. Attractive Ge-on-Si detector performances have been reported, with typical responsivity around 0.8 A/W and bandwidth high enough for 40 Gb/s operation [7-13].

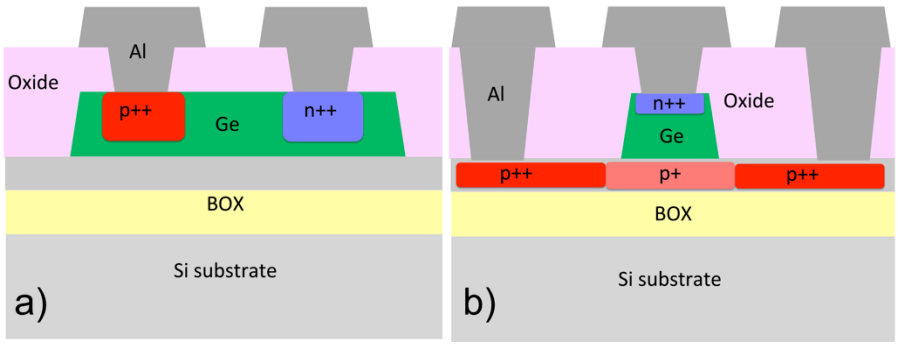

Fig. 3.2. Lateral and vertical *p-i-n* Ge-on-Si photodetectors.

As shown in Fig. 3.2, both types of devices require heavily-doped germanium to form the junction, as well as the direct contact of germanium with metal via plugs. Germanium processing received far less research attention than silicon, and is therefore much less well understood and characterized. While silicon modulators have been optimized for efficiency [15], similar TCAD models remain elusive for germanium detectors. Hence a

photodetector that does not require doping or metallization of germanium is highly desirable.

3.3 Floating Ge detector design

I report a Ge-on-Si photodetector without doped Ge or Ge-metal contacts. We gave it a short name, floating germanium photodetector, mimicking the floating gate devices in circuits. It is just for convenience, and not perfectly accurate, since the germanium is the source for photocurrent. The device was measured to have a responsivity of 1.14 A/W at -4V reverse bias, at 1550 nm wavelength. I also show that responsivity can be increased to 1.44 A/W with -12V reverse bias. The detector dark current remains below 1 μA for both bias conditions. 40Gb/s operation is demonstrated.

A schematic illustration of the floating germanium photodetector is shown in Fig. 3.3(a). Compared to the conventional detector configurations shown in Fig. 3.2, the germanium is free of defects caused by ion implantation damage and metallization. Furthermore, we note that creating metal via-plugs is a complicated multi-step process in CMOS, requiring implantation, annealing, contact hole opening, silicide formation, diffusion barrier deposition, metal deposition, patterning, and planarization [16]. The proposed floating germanium detector configuration significantly simplifies the silicon photonic process flow and will ultimately reduce the cost of building silicon-based photonic integrated circuits (PICs). Since this diode design shares exactly the same doping levels and metallization procedures of a silicon modulator, the only extra step needed to build the device is germanium epitaxy. Incidentally, a similar device, independently designed from this work at approximately the same time, was presented at the *Optical Fiber Communications Conference* (OFC) recently by Liow et al [17]. The

device in [17] was designed as an avalanche photodetector (APD) with low electric field strength in germanium, separated absorption and multiplication region, and was characterized at 1.3 µm wavelength, while our device is an enhanced *p-i-n* detector with relatively high electric field strength in germanium to effectively sweep out photo generated carriers at high speed, and we report device performance at 1.55 µm wavelength.

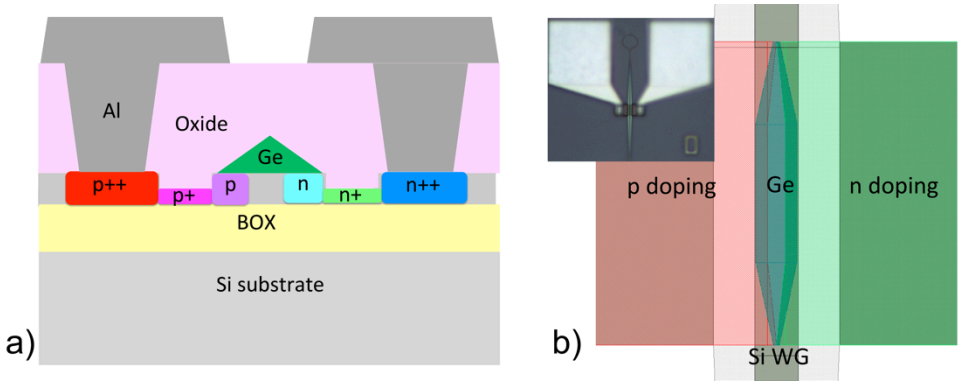

Fig. 3.3. (a) Schematic cross-section, (b) layout and a photo of the floating germanium detector. Only silicon, germanium, p and n doping layers are shown.

Despite the simplified fabrication, the floating germanium detector is expected to have higher responsivity than the conventional ones shown in Fig. 3.2, because metal absorption from the electrodes and free carrier absorption from heavy contact doping are eliminated. The dark current is expected to be lower too because of the preserved crystal quality after epitaxy. To achieve high responsivity, photons should be confined in the intrinsic germanium absorber, and scattering needs to be minimized. The fundamental mode of this germanium silicon hybrid waveguide structure is plotted in Fig. 3.4(a). The optical mode is well confined to the germanium, with a confinement factor of 88%, ensuring efficient absorption and minimizing detector length, and thus capacitance. A 3

μm long germanium taper from 0.22 μm to 1.5 μm in width was used to adiabatically transfer light from the input silicon waveguide to the hybrid waveguide. A 50 μm long taper used to connect the standard 0.5 μm wide strip routing waveguide and the 1.5 μm rib waveguide detector input, as shown in Fig. 3.3(b).

Without a *p-i-n* junction formed in germanium, the device relies on the fringe field of the silicon junction to sweep out photo-generated carriers. It has been reported that the fringe field and its corresponding capacitance is a non-negligible part of the 220 nm-thick silicon *pn* junction and must to be accounted for in modulator design [18]. As germanium has a much higher permittivity than typical CMOS dielectrics, such as silicon nitride or silicon dioxide, the portion of fringe field in the germanium and the capacitance will be even higher for the same silicon junction. We numerically solved Poisson's equation and plotted the electric field distribution in Fig. 3.4(b). The junction's intrinsic region width in Fig. 3.4(b) is set to match the mode field diameter in Fig. 3.4(a). The electric field in most of the germanium is stronger than 10^4 V/cm at -4V reverse bias, high enough for the carriers to drift at the saturation velocity [19]. Slightly higher bias might be needed to drive all photo-generated carriers, due to the non-uniformity of electric field. Note that the *p-i-n* junction extends to the tapered part of the hybrid silicon germanium waveguide to collect photo-generated carriers in the germanium taper, as shown in the layout in Fig. 3.3(b).

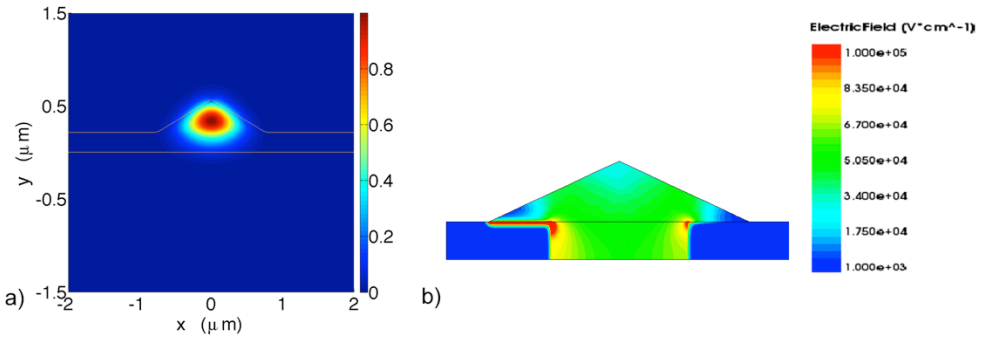

Fig. 3.4. (a) Optical mode profile and (b) electrical field at -4V reverse bias.

3.4 Floating Ge detector characterization

The aforementioned device was prototyped by participating in a multi-project wafer (MPW) run offered by the *OpSIS foundry*. Fabrication occurred at *Institute of Microelectronics* in Singapore. The floating germanium detector was fabricated using the standard process to create our baseline vertical *p-i-n* detectors with a 0.5 µm thick germanium slab, and no additional process split was needed thanks to the anisotropic epitaxial growth of germanium. The starting substrate was an 8-inch silicon on insulator (SOI) wafer, with 220 nm, 10 ohm-cm p-type top silicon film, and 2 µm buried oxide on top of a high resistivity silicon handle. Waveguides and grating couplers were patterned using 248 nm UV lithography followed by dry etching. Boron and phosphorus ions were implanted into silicon, and activated by rapid thermal annealing. Germanium epitaxy followed and then two layers of aluminum metal interconnect were added to complete the fabrication flow.

I. Optical spectrum

Two sets of characterization structures corresponding to the device cross-section in Fig. 3.3(a) were designed. Grating couplers were used as optical I/O to a fiber array in both cases. In Set A, transmitted light after the germanium absorber was guided to

another grating coupler, which was used to characterize the germanium absorption efficiency and determine the required device length. In Set B, the through port was connected to a y-junction with its two branches tied together, which effectively functioned as a broadband mirror, as shown in the device photo in Fig. 3.3(b). A fiber array was first aligned to the grating couplers in Set A, and the devices were measured using a tunable laser that can sweep from 1500 nm to 1570 nm. The spectra of two devices with different germanium length, as well as a reference grating coupler, are plotted in Fig. 3.5. The overall parabolic shape is due to the spectral response of the grating coupler. A reduction in power level indicates extra loss added by the germanium strip. No interference fringes were observed on the spectrum, confirming that light stayed in its fundamental mode throughout the structure. Single mode operation prevented a waste of photons from scattering or divergence, and also improved absorption per unit length since the light was tightly confined in the germanium absorber. The capability to couple light upward into germanium and back down into silicon is useful for constructing germanium absorption modulators as well. The lengths of the two detectors in Fig. 3.5 are 11 μm and 16 μm respectively, including 6 μm for tapers. Stronger absorption at shorter wavelengths is clearly illustrated, because shorter wavelengths are further from the band edge of germanium. At 1550 nm, the 16 μm long germanium had 26 dB of attenuation. With the y-junction loop mirror to reflect the transmitted photons back for reabsorption, the 16 μm long detector in device Set B will be able to achieve almost 100% internal quantum efficiency.

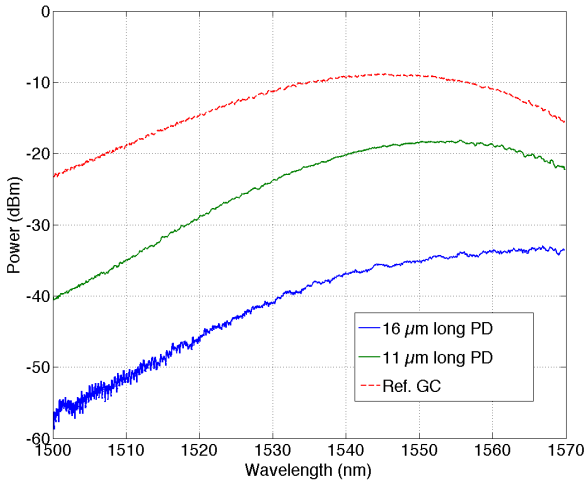

Fig. 3.5. Transmission spectra of floating germanium detectors and a reference grating coupler loop.

II. IV characterization

In addition to the optical properties, device performance also depends on the *p-i-n* junction shown in Fig. 3.4(b). I probed the device and characterized the IV curve using a semiconductor device analyzer, both for dark operation and with incident light, shown in Fig. 3.6(a). The dashed line shows a typical diode IV curve. The dark current is only 0.12 μA at -4V, which is an order of magnitude smaller than the dark current of conventional vertical *p-i-n* detectors fabricated in the same process. I attribute this improvement to the smaller junction area and preserved germanium crystal quality from and after the epitaxy. The dark current increases to 0.29μA, 0.9μA, and 26μA at -8V, -12V, and -16V respectively. Similar traces were observed when light was incident. Photocurrent was extracted by subtracting dark current from the total current. Photocurrent increases with reverse bias voltage and saturates at about -2 V. With less than -2 V, the fringe field is not strong enough to sweep out photo-generated carriers before they recombine. With more than -2 V, essentially all photo-generated carriers are swept out within their lifetime and are collected by the electrodes. Hence the photocurrent in Fig. 3.6(a) saturates and

stays relatively flat until beyond -5 V, where it slowly tails up due to the turn-on of avalanche gain. Different from a typical avalanche photodetector, photocurrent reaches a maximum at -17V and drops when reverse bias is further increased. This is most likely due to the silicon junction beneath the germanium entering its avalanche regime and beginning to conduct a significant amount of current.

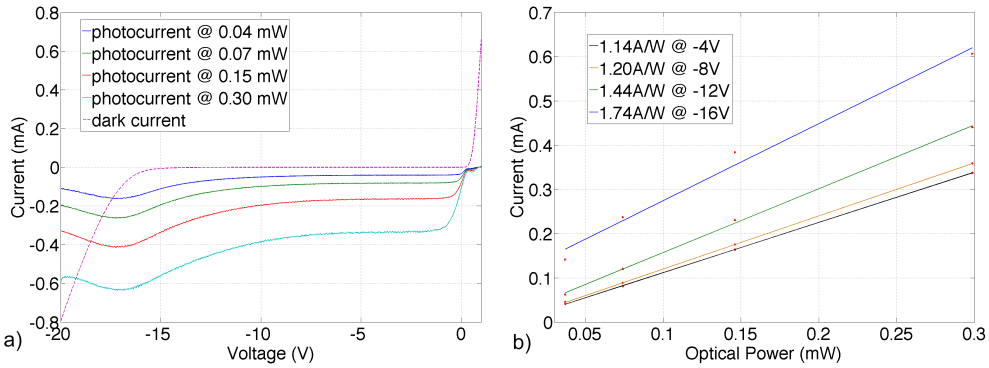

Fig. 3.6. (a) Device IV curves in darkness and with various incident optical powers; (b) Photocurrent as a function of input optical power at different bias voltages. The slope of the linear fit gives the responsivity for each bias.

From Fig. 3.6(a), the photocurrent as a function of optical power impinging on the device at each bias voltage can be plotted, as shown in Fig. 3.6(b). Red dots are measured data points, and colored straight lines are linear fits. The slope of the fitting line gives the responsivity value at the corresponding bias. At -4V, the device works as a normal *p-i-n* detector, the responsivity is 1.14 A/W, comparable to the best state-of-the-art devices [9, 11, 12]. Responsivity further improves as reverse bias increases due to avalanche multiplication. At -12V, responsivity goes up to 1.44 A/W, while the dark current remains below 1 μA. Further increasing bias continues to increase the responsivity, but at the price of higher dark current.

For receivers with *p-i-n* detectors, the noise is typically limited by thermal noise generated from the load resistor. In this case the signal to noise ratio and receiver sensitivity is determined by photocurrent amplitude, which is proportional to detector responsivity. Compared to our baseline detector with 0.75A/W responsivity, receiver sensitivity, and hence link budget, is improved by 1.82 dB if the floating germanium detector is biased at -4V. At -12V, thermal noise still dominates due to the minimal avalanche multiplication factor, receiver sensitivity benefits from the enhanced responsivity and increases to 2.83 dB better than the baseline PD.

III. Bandwidth

Photocurrent roll-off was characterized by measuring the *s*-parameters using a vector network analyzer (VNA) and a $LiNO_3$ modulator. S21 traces at different bias voltages are plotted in Fig. 3.7. At -4V, the 3 dB bandwidth is around 20 GHz, sufficient for detecting 25 Gb/s on-off keying (OOK) signals. The response at -2V matches that of -4V at low frequencies, indicating all photo-generated carriers have been swept out within their lifetime, matching the IV curves in Fig. 3.6(a), but frequency roll-off is fast due to transit time limitation. At -8V and -12V, the 3 dB bandwidth increases to over 40 GHz, which indicates that carrier transit time limits the device bandwidth at lower bias. At -16 V, bandwidth drops slightly to 30 GHz as the avalanche gain increases.

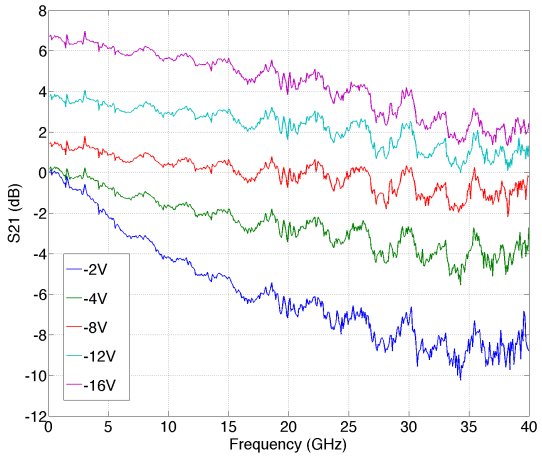

Fig. 3.7. Device S21 at different reverse bias voltages.

Generally the bandwidth of a photodetector is determined either by carrier transit time or device RC time constant. Taking the saturation velocity to be 6.5×10^6 cm/s [19], and mode field diameter 0.85 μm, the transit time limited bandwidth is estimated to be

$$f_t = \frac{0.44 v_{sat}}{L} = 33.6GHz$$

which is close to the measured bandwidth. The transit-time-limited bandwidth could be improved by using a narrower germanium strip, which won't degrade the detector efficiency given the strong absorption of germanium, as shown in Fig. 3.5.

The device capacitance was determined to be 8 fF, calculated from the phase information of the *s*-parameters. Low capacitance is critical for the device to be used in optical interconnects [20]. Assuming a 50 Ω load impedance, the major contributor of series resistance are the p+ and n+ doped 90 nm silicon slabs connecting the silicon under the germanium to the metal via. Sheet resistance at this intermediate doping level is 3750 Ω/□ and 1490 Ω/□ for p+ and n+ silicon slab respectively. They are 1.5 μm wide and

16 μm long, leading to around 490 Ω series resistance. Thus the RC time limited bandwidth is

$$f_{RC} = \frac{1}{2\pi C_{pd}(R_{pd} + R_L)} = 36.8GHz$$

Since the light is tightly confined in the germanium, it is safe to use higher doping on these connecting slabs without introducing noticeable optical loss from free carrier absorption. Sheet resistance for p++ and n++ dope slab is 137 Ω/□ and 60 Ω/□, which is an order of magnitude smaller than those of p+ and n+ slab, and will totally remove RC time limit on device operating bandwidth.

I further performed data transmission experiments to verify the detector performance. Light modulated with a 40Gb/s non-return to zero (NRZ) pseudo random bit sequence (PRBS) was launched into the photodetector. The detector RF output was displayed on a digital communication analyzer (DCA). Eye patterns obtained at -4V, -8V, -12V, and -16V bias are shown in Fig. 3.8. The eye opening at -4V is not as good as those at higher bias voltages due to the bandwidth limitation. Because of the low dark current and small gain factor, the detector noise remains low, confirmed by open eye diagrams, even at -16V. As a compromise between low noise, high responsivity and high bandwidth, -12V is an optimal operating bias voltage, which is a factor of 2 to 3 lower than that required by conventional APDs. At this bias level, a 1.44 A/W responsivity can be obtained, with a dark current of 0.9 μA, which is orders of magnitude smaller than that of Ge/Si APDs [21-23].

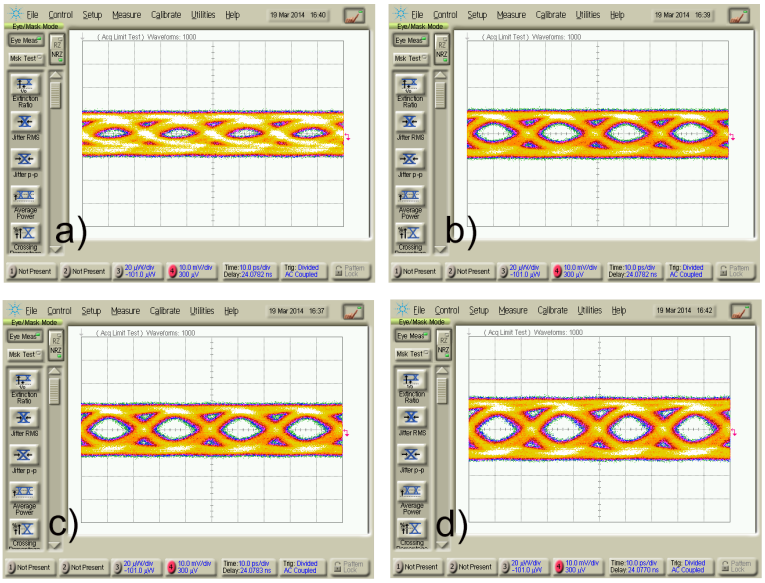

Fig. 3.8. 40 Gb/s eye diagrams at (a) -4V, (b) -8V, (c) -12 V and (d) -16V bias.

3.5 Summary

In this chapter, requirement for an easy to fabricate, high responsivity, and high speed photodetector is discussed. Germanium on silicon hetero-epitaxy process is reviewed next. Then a novel floating germanium photodetector is proposed and demonstrated. The floating detector doesn't require doping in germanium and metal germanium direct contact, which significantly simplified the silicon photonics fabrication process flow. The device was measured to have a responsivity of 1.14 A/W at -4V reverse bias, at 1550 nm wavelength. I also show that responsivity can be increased to 1.44 A/W with -12V reverse bias. The detector dark current remains below 1 μA for both bias conditions. 40Gb/s operation is demonstrated.

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CHAPTER 4. HYBRID LASER INTEGRATION

A high quality laser is critical to the performance of any optical data links. Because silicon doesn't lase at telecom wavelengths, external gain material has to be integrated in a CMOS compatible manner. Silicon waveguide distributed Bragg gratings require sub-50 nm feature size and are challenging to manufacture. A reliable cavity is also needed to provide feedback for lasing operation. Monolithic and hybrid gain integration approaches are reviewed. A novel laser cavity configuration utilizing Sagnac loop mirror and micro-ring resonator is proposed. Hybrid lasers based on such cavity are demonstrated with 1.2 MHz linewidth, 4.8 mW on-chip output power, and over 40 dB side mode suppression ratio.

4.1 Gain integration

Semiconductor lasers and optical amplifiers are preferred in transceivers because they are efficiently electrically pumped and die size is small. Lasing is a radiative recombination process in semiconductors, where an electron in the conduction band recombines with a hole in the valence band and a photon is emitted. Its reverse process is electron hole pair generation through optical absorption. Conservation of both energy and momentum are required in this process. Because the photon's energy is equal to the bandgap of the semiconductor, energy conservation is satisfied. But a photon's momentum is negligible compared to that of an electron or a hole. To meet momentum conservation requirement, the top of the valence band and bottom of the conduction band need to be aligned. In other words, the semiconductor needs to be a direct bandgap material. This is true for a number of III-V compound materials such as gallium arsenide (GaAs) and indium phosphide (InP), but unfortunately not the case for silicon.

The Raman silicon laser was also demonstrated [1], but making an electrically pumped silicon laser is prohibitively difficult. Other gain materials have to be introduced into silicon material system. Various gain integration approaches have been reported, including monolithic epitaxy, wafer bonding, and SOA edge coupling.

A monolithic laser is most preferable because its high integration density, which makes the chip compact and mechanically reliable. Moreover, the connection between the laser and the rest of the system, either a modulator in a transmitter or a 90-degree optical hybrid in a coherent receiver, is lithographically defined, thus no alignment is needed and no coupling loss is introduced, which saves substantial packaging cost and system power consumption. Germanium is a CMOS compatible material and is widely used for photodetectors in silicon photonics. It's also a Group IV element in periodic table, the same as silicon, and an indirect bandgap material as well. But the direct bandgap of Germanium, between valence band top and Γ valley, is 0.80 eV, and its indirect bandgap between valence band top and L valley is 0.664 eV, with only 0.136 eV difference. During the epitaxy step, the germanium lattice is relaxed at elevated growth temperature of over 600 C. Because germanium has a larger thermal expansion coefficient than silicon, it gets 0.2-0.3% tensile strain upon cooling down to room temperature, which shrinks the difference between direct and indirect bandgap to around 0.1 eV. If the germanium is n-doped, electrons on the conduction band will first fill empty states in L valley. Because the energy states below the direct Γ valley are fully occupied by extrinsic electrons from heavy n-doping, electrons injected by the pump current have to fill the Γ valley and direct bandgap emission occurs [2]. Alloying with Tin (Sn) also helps to convert germanium into a direct bandgap material [3]. Electrically

pumped germanium lasers at room temperature were first reported recently [4]. But the device has an extremely high threshold current density of 300 kA/cm^2. Germanium lasers remain to be a very promising approach, but device efficiency needs to be improved significantly for practical applications.

Gain could also be monolithically integrated by epitaxy of III/V material on silicon. Historically IIIV quantum well lasers directly grown on silicon have suffered from poor performance due to high dislocation density due to lattice mismatch. This could be mitigated by switching to quantum dot (QD) lasers, where strong carrier confinement and localization within a single quantum dot can effectively shield carriers from dislocations. Also due to the strong confinement, carrier recombination rate is much less sensitive to temperature. Silicon QD lasers have been demonstrated by multiple groups [5, 6] and they operate up to over 100 °C. QD laser is another promising approach, but it still requires complicated buffer layers for hetero-epitaxy, and the compatibility with the rest of device library needs to be addressed.

Since both germanium and QD laser are in their infancy, integrating relatively simple InP structures is more plausible for near and mid-future applications. One approach is to bond an InP wafer on the SOI wafer after the waveguides are defined, which act as the top cladding. The optical mode penetrates in to InP, thus the propagating optical signal experiences gain [7,8]. Another approach is to place an InP block into an engineered pit and metal bond it to the silicon wafer, then pattern the InP waveguide and use deposited poly silicon to fill the gap and reduce coupling loss [9]. Because the buried oxide layer is removed in the pit and, the InP gain block in direct contact with the silicon handle wafer, which helps thermal dissipation. Both approaches maintain the advantage of a monolithic

laser, where optical alignment is not needed. But they require III–V processing, which is a big hurdle to implement in a commercial CMOS fab.

A third approach is to make an external cavity laser by butt coupling a reflective semiconductor optical amplifier (RSOA) and a SOI chip [10-12]. This approach does require accurate alignment of the RSOA and SOI chip, but state-of-the-art packaging process developed by the optoelectronics industry can be leveraged. A flip chip bonder can place the gain chip within 0.1 μm, [11]. With a carefully designed edge coupler, the coupling loss variation is controlled to with in 1 dB, satisfying production requirement in terms of both performance and packaging cost. The distinctive advantage of this hybrid approach is that both silicon and RSOA can be independently optimized without compromising each other. And high CMOS compatibility is preserved. Commercial off-the-shelf RSOA can be used. Silicon chips can be obtained from foundry services, such as OpSIS and ePIXfab. So we chose this hybrid integration approach for our light source solution.

4.2 On-chip laser cavity

To the first order, a laser is a device that consists of some gain medium between two mirrors. One mirror is highly reflective and the other is partially reflective, which serves as the output. For discrete laser diodes, the cleaved facets of semiconductor are natural mirrors, and are usually covered with coatings to further optimize the reflectivity. Broadband mirror form Fabry-Perot lasers. To build a single mode laser, reflectivity of at least one of the mirrors needs to be wavelength selective, or a wavelength filter needs to be inserted into a Fabry-Perot cavity. In the hybrid integration approach, the SOA is coated with high-reflective coating on one end and anti-reflective coating on the other

end. So the wavelength selective partial reflective mirror function has to be implemented on silicon. Distributed Bragg reflector (DBR) is an intuitive choice an optical device designer may have. This is indeed reported in silicon photonics platforms with 3 μm or 1.5 μm silicon film thickness [9,10]. However, for the mainstream submicron SOI substrate, a narrow band grating requires sub-50 nm feature size, which is beyond the lithography resolution of typical silicon photonics processes. For example, a DBR with 40 nm square gratings in layout on waveguide sidewall is measured to have 0.4 nm 3 dB bandwidth, but the fabricated device turned out to be wavy or sinusoidal, as shown in Fig. 4.1 [13].

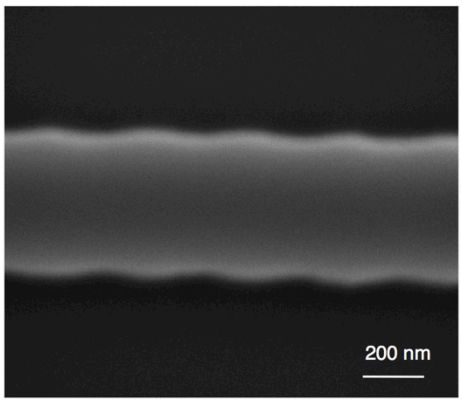

Fig. 4.1 SEM image of silicon waveguide DBR. Grating is square corrugations of size 40 nm in layout [13].

I explain briefly why SOIs with various silicon layer thickness are used, and why sub-50 nm features cannot be fabricated in typical photonics processes (even though people often read that PC or smart phone chips are made 14 nm, 20 nm, or 28 nm node in technology news). The silicon photonics research and development is a concurrent effort of industrial labs from prominent corporations, startups, academic groups, and foundry services [14-20]. The silicon device layer thickness is chosen based on the need to merge into existing CMOS process flows, differing polarization management techniques, ease of

packaging, and considerations of device performance. Generally, thicker SOI gives better passive device performance, in particular low polarization dependent loss (PDL) and uniform wavelength filter and multiplexers such as Echelle gratings, since the percentage of thickness variation is small. However, a large waveguide core is less tolerant to waveguide bending loss and can't be used to build efficient *pn* junction phase shifters. As a result, submicron SOI, usually 220 nm, gained more and more popularity and became common choice of many parties [14, 16-20].

248 nm lithography is typically used for silicon photonics for both economical and technical reasons. Transistors perform better when their size gets smaller. Speed is higher and power consumption is lower. However, size of photonics devices is determined by the structure of waveguide and cannot be easily shrunk. If the silicon wire becomes thinner, it is not a guiding structure any more. For the same reason, photonics devices are orders of magnitude larger than transistors, ranging from micron to millimeter scale. Mask manufacture and fabrication cost increase significantly when moving to a new node. Building photonics chips using most advanced technology nodes is prohibitively expensive. For this reason, instead of monolithic integration of both electronics and photonics, hybrid integration of PIC and electrical drivers is preferred.

Coming back to the topic of on-chip cavity, since DBR is not an option, a partial reflective mirror is still elusive. Note that micro-ring resonators can be used as wavelength filters. They are compact, thanks again to the tight mode confinement of submicron silicon waveguides, and the Lorentzian shape provide strong side mode suppression, which helps laser line width reduction if used in a cavity [21]. They are also thermally tunable, due to the temperature dependence of silicon refractive index, 1.8×10^{-4}

K^{-1}, which could be used for laser wavelength tuning, as well as wavelength locking with an etalon reference and some controlling circuitry. So the problem reduces to just make a broadband partial reflective mirror. This mirror needs to be manufacturable and of low excess loss.

My first generation design that is shown in Fig. 4.2. It consists a low loss Y-junction, as described in Chapter 2. Two branches of the Y-junction are tied together, which forms a broad band mirror. The optical beam splits into two with equal power and same phase. Then the two beams travel across exactly the same path in reverse direction, and combines coherently again at the Y-junction. So the net effect is that the beam direction is reversed. The excess loss of this mirror is twice of that of the Y-junction.

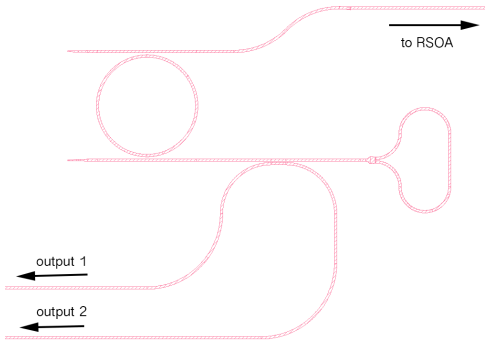

Fig. 4.2 Y-junction loop mirror

A directional coupler is used to tap the cavity waveguide to extract output power. A directional coupler, also known as evanescent coupler, is just two straight waveguides in parallel, with very narrow gap. The coupling strength can be adjusted by changing the gap width or coupling length, so arbitrary coupling ratio between 0 and 100% can be achieved. Directional couplers are generally not used in InP since it requires etching a narrow gap between two waveguides that are microns thick. However, as the waveguide thickness is only 220 nm for SOI and anisotropic dry etching of silicon is mature,

directional coupler is a flexible and yet reliable power coupler in the silicon photonics platform. The drawback with this cavity design is that there are two outputs of equal power at the same wavelength. It would be useful to power a dual channel parallel transmitter, or a coherent transceiver, where one output is used for transmitter and the other as local oscillator (LO). However, without a known phase relationship, combining the two outputs is not trivial and adds additional power consumption, which makes it not a good general solution.

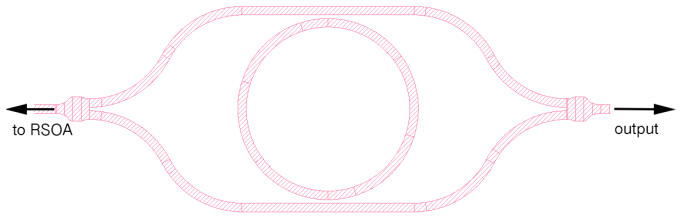

Fig. 4.3 Eye-shape reflector

To solve the problem in the first generation design, I come up with the eye-shape reflector as shown in Fig. 4.3. This device does have a single output, and is wavelength selective at the same time due to the embedded ring in the Mach-Zehnder structure. To illustrate the principle this device, let's first assume that the ring is critically coupled. The optical beam injected from the left side is first split at the Y-junction, then coupled to the ring and gets dropped on the other side. So for light at the ring resonant wavelengths, it is a 100% reflection mirror. Light off the ring resonant wavelengths completely passes this structure with low excess loss. To get some power coming out of the output port on the right side, the coupling strength is tuned slight off critical coupling. But ring resonance is very sensitive to the coupling strength, hence the mirror reflectivity is hard to control. So this is not a perfectly satisfactory solution either.

Then I come up with the Sagnac loop mirror based cavity configuration, as shown in Fig. 4.4. The micro-ring is fixed at critical coupling condition just for wavelength filtering, and the Sagnac loop mirror is used for broadband reflection. There is only one output, and the reflectivity can be accurate controlled by adjusting coupling length. The micro-filter and Sagnac loop mirror are independent and can be optimized separately. At the same time, it is a robust device, with low excess loss. We described the characterization of this device in detail in the next section.

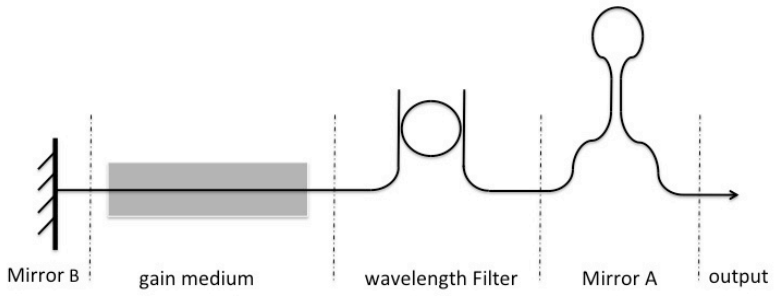

Fig. 4.4 Diagram of Sagnac loop mirror based laser cavity configuration

4.3 Sagnac loop and micro-ring ECL

I. Proof-of-concept device

The proposed device was prototyped via participating in a multi-project-wafer (MPW) run offered by *OpSIS foundry*. Fabrication occurred at *Institute of Microelectronics* in Singapore. The Sagnac loop mirror transmittance and reflectivity can be predicted analytically as it contains only a DC other than routing waveguide. Measured data match well with theory, as summarized in Fig. 4.5. Waveguide confinement decreases as the working wavelength is red shifted, hence evanescent coupling, and as a result the reflectivity of Sagnac loop mirror, is stronger in longer wavelength, as shown in the inset of Fig. 4.5(a).

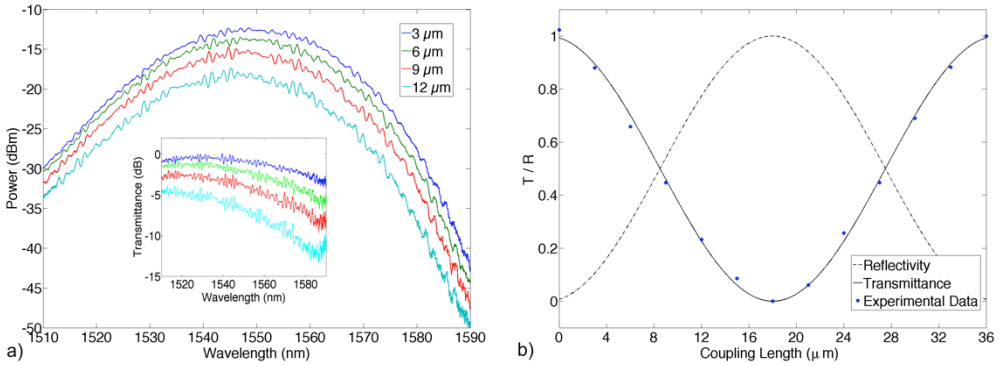

Fig. 4.5 (a) Sagnac loop mirror transmission spectrum measured using a tunable laser and grating couplers; Normalized transmittance spectrum is shown in the inset; (b) Transmittance and reflectivity of Sagnac loop mirror as a function of DC coupling length at 1550 nm wavelength.

A racetrack ring resonator was used as the wavelength filter in this device. The ring has 10 μm radius, and a 1.5 μm long straight DC to maintain critical coupling. The ring FSR is 8.7 nm, and FWHM 0.075 nm, corresponding to Q of 20 000. Because the ring resonator is a comb filter and has multiple pass bands, the device is expected to lase at a resonant wavelength near the top of the SOA gain spectrum, labeled by a red pentagram in Fig. 4.6.

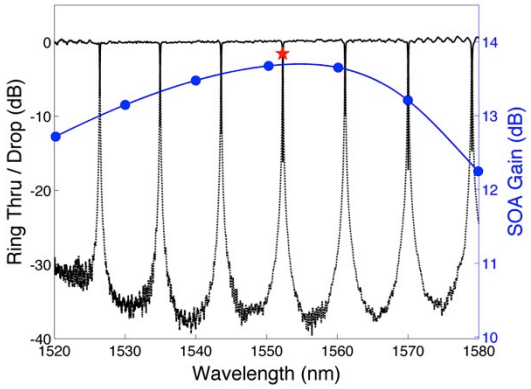

Fig. 4.6 Ring filter drop (solid) and through (dashed) spectrum, and SOA gain spectrum at 150 mA (blue). The expected lasing wavelength (1552.3 nm) is labeled by a red pentagram.

The diced silicon chip was first polished to create a flat and smooth sidewall for edge coupling. An ultra-thin edge coupler was used trying to match the SOA mode for low

coupling loss, as detailed in [22]. A half-cavity on silicon chip was aligned to the SOA using a six-axis stage. An image of the testing setup is shown in Fig. 4.7(a). The measured spectrum at 170 mA pump current using an optical spectrum analyzer with 0.1 nm resolution is plotted in Fig. 4.7(b). Fingerprints of the ring filter spectral response are clearly seen in the laser spectrum, with mode spacing equal to the ring FSR. The lasing peak appeared at 1552.3 nm, as expected from Fig. 4.6. The SMSR was 40 dB. On-chip power was 1.05 mW after normalizing the grating coupler insertion loss. Mirror transmittance, 90% at the Sagnac loop on silicon chip and 10% at the SOA far-end facet, as well as the coupling loss, estimated to be over 4 dB, were the major contributors of cavity loss. Note that angled waveguides were used on both silicon chip and SOA to avoid reflection into the cavity at the chip interface.

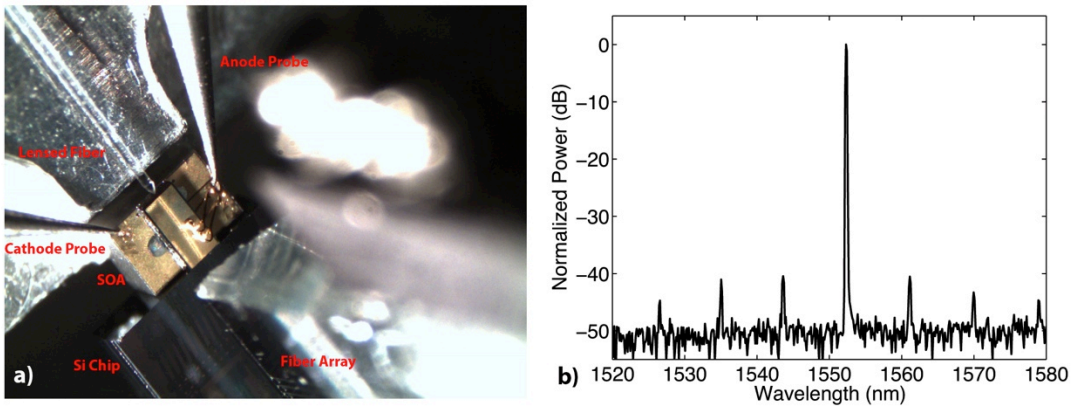

Fig. 4.7 a) Image of the testing setup and b) Laser spectrum measured using a fiber array shows clear fingerprints of the ring filter and 40 dB SMSR.

We performed heterodyne experiment to measure the laser linewidth. Our laser output from the fiber array was combined with the output of a narrow linewidth laser (Agilent 81600B, linewidth about 100 kHz) by a 2×2 fiber coupler. The combined signal was converted into electrical domain by a photodetector, whose photocurrent was fed into a RF spectrum analyzer. The heterodyne spectrum is plotted in Fig. 4.8, together with a

Lorentzian fit. The fitted curve shows that the FWHM of our laser is approximately 13.17 MHz.

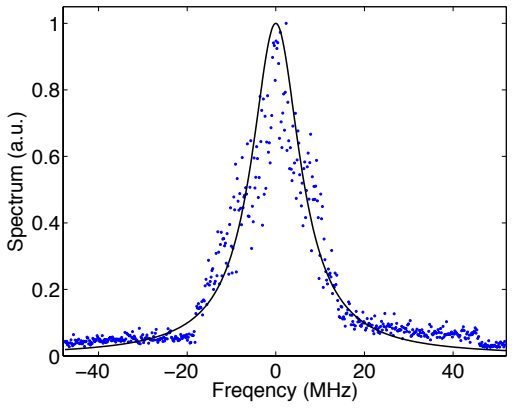

Fig. 4.8 Heterodyne spectrum (blue dot) and a Lorentzian fit curve with 13.27 MHz FWHM.

II. Lithographic Micro-ring resonant wavelength control

As shown in Fig. 4.7, although with a high SMSR of 40 dB, a number of longitudinal modes are available, up to 10 dB over the ASE noise floor. This is because the micro-ring is a comb filter, and the SOA gain spectrum is relatively wide and flat. The laser is vulnerable to perturbations and the lasing wavelength may hop to the next cavity longitudinal mode. It can be addressed by increasing the ring free spectral range (FSR). If the FSR is wider than the flat gain spectrum, all other cavity modes will be suppressed.

A second drawback of micro-rings is their sensitivity to fabrication variations. For wafers processed in a commercial CMOS fab, it has been reported that the cross-wafer spread in resonant wavelength is as large as its FSR [23]. If the micro-ring is used as a WDM modulator, the ring resonance can be thermally tuned to the nearest grid channel, thus mitigating the fabrication sensitivity to a certain extent. However, if the micro-ring is used inside a laser cavity, the non-predictability of lasing wavelength greatly impedes the practical application of such device.

The effect of waveguide geometry variation on micro-ring resonance wavelength can be modeled as a perturbation to the waveguide effective index. The FSR depends on the group index of the waveguide, which is immune to fabrication errors and can be accurately controlled among wafers and lots [23]. If the FSR is increased to be significantly larger than the random spread of wavelengths, that spread determines the range of possible lasing wavelengths. The spread depends on ring waveguide design, the SOI wafer, and silicon processing. We chose an adiabatically widened micro-ring (AMR), which has a large FSR [24] and is more robust against fabrication variations [25]. In an AMR, waveguide is narrow near the coupling region to ensure single mode operation, and then gradually widened to support tight bend and possible need to form metal contact. For an AMR of 2 μm radius, the FSR is as large as 54 nm. As shown in Fig. 4.9(a), there is only one resonance peak in our testing laser's sweepable range,1500 nm to 1580 nm. Resonance FWHM is 1.38 nm, corresponding to a finesse of 39 or Q-factor of 1100. We measured the same device design on all 31 complete 2.5 cm × 3.2 cm reticles across an 8-inch wafer. Wafer chuck temperature was set to 30 °C, where it is most stable. The resonant wavelength distribution contours and statistics are shown in Figs. 9(b)-9(c). The mean is 1528.76 nm and standard deviation is 3.32 nm.

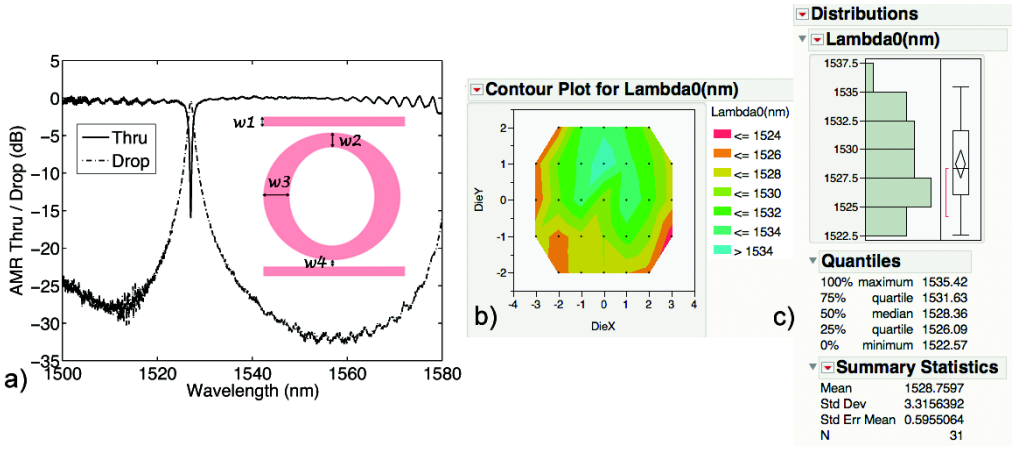

Fig. 4.9. (a) Spectrum of AMR drop (solid) and through (dashed) ports. Inset is schematic of AMR layout, where w1 = 0.3 μm, w2 = 0.46 μm, w3 = 0.76 μm, and w4 = 0.2 μm; (b) Contour plot for resonant wavelength distribution across an 8-inch wafer; (c) Statistics of the resonant wavelength distribution.

To further validate the predictability of resonant wavelength, AMRs with slightly different radii on the same wafer were also measured, and summarized in Fig. 4.10 and Table 4.1. The wavelength range, maximum minus minimum, falls between 12.30 nm and 16.30 nm. Standard deviation is between 3.32 nm and 3.78 nm, with an average of 3.6 nm. Note that the device is patterned using 248 nm lithography on SOI wafers with 20 nm 3σ thickness variations. Significant device uniformity improvement was observed by switching to 193 nm [26], 193 nm immersion lithography, and more uniform wafers [27]. For WDM applications, the target wavelength can be set as the lower bound of the wavelength spread, and then locally and thermally tuned to the grid wavelength and stabilized with active feedback control [28]. Since the tuning range is a very small fraction of the FSR, thermal tuning power is minimal [29].

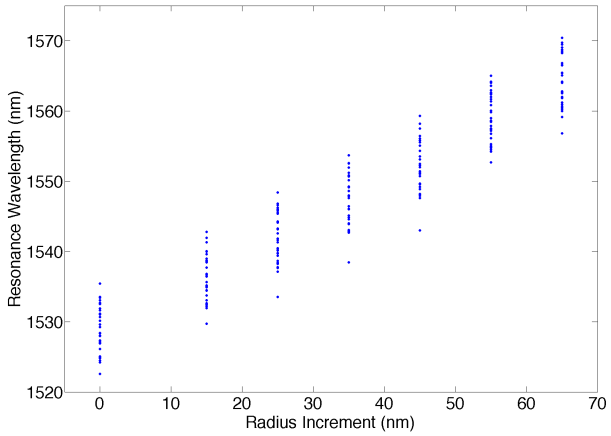

Fig. 4.10 AMR resonance increase as ring radius increases, measured on 31 reticles across an 8-inch wafer.

Table 4.1. Resonant wavelength distribution of AMR with slightly different radius.

ΔR (nm)	0	15	25	35	45	55	65
Min	1522.57	1529.71	1533.52	1538.47	1543.00	1552.70	1556.80
Max	1535.42	1542.8	1548.42	1553.70	1559.30	1565.00	1570.41

Range	12.85	13.09	14.90	15.23	16.30	12.30	13.61
Std Dev.	3.32	3.38	3.59	3.75	3.78	3.47	3.62

III. Si_3N_4 edge coupler

One other shoring coming of the proof-of-concept device is the low output power from the coupling loss at the chip interface due to mode mismatch between the silicon waveguide and RSOA waveguide. Cross-section of a typical silicon waveguide and its mode profile is shown in Fig. 1.1 and Fig. 1.2. The near field mode profile of the RSOA waveguide is not precisely known, but typical single mode lasers have mode field diameters (MFD) around 3 μm × 1 μm. To better match the RSOA mode and reduce coupling loss, I utilized a silicon nitride waveguide edge coupler. Silicon nitride is a CMOS compatible material, and commonly used as hard-mask, backend of the line (BEOL) dielectric, and wafer passivation layer. After the silicon waveguide is defined, 350 nm of oxide is deposited and then planarized to 100 nm above silicon waveguide top surface using chemical mechanical planarization (CMP). Then 200 nm silicon nitride is deposited and patterned by lithography and dry etching. Light is coupled from silicon waveguide to nitride waveguide using a push-pull coupler, as shown in Fig. 4.11. The silicon waveguide width is tapered down from 0.5 μm to 0.18 μm, while silicon nitride waveguide width increases gradually from 0.25 μm to 1.0 μm. The insertion loss of this coupler is characterized to be 0.3 dB. Then the silicon nitride waveguide width is adiabatically tapered to 4.25 μm. Refractive index of silicon nitride is 1.95 – 2.0, with a 0.2 μm thickness, it is guiding, but the confinement factor is low. In the vertical direction, a large portion of the mode is in the oxide cladding, as shown in Fig. 4.12. The MFD of this silicon nitride waveguide is 3.5 μm × 0.7 μm, better matching a typical SOA mode.

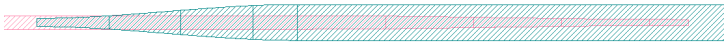

Fig. 4.11 Layout of silicon waveguide to silicon nitride waveguide coupler. Pink is silicon, and green is silicon nitride.

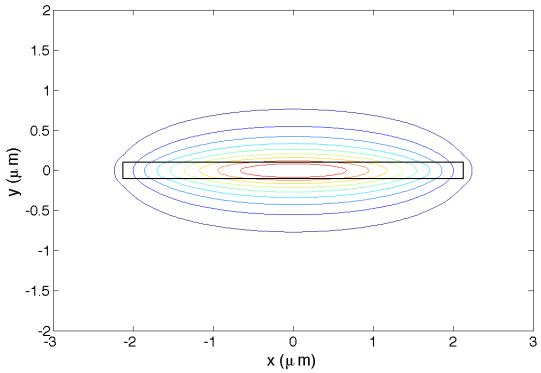

Fig. 4.12 Mode profile of a silicon nitride waveguide of size 4.25 μm × 0.2 μm

With the AMR and improved edge coupler, I repeated the alignment and measurement procedure described before. After the SOI chip, the RSOA chip and the fiber array were properly aligned, the RSOA pump current was turned on. A sharp threshold behavior near 60 mA was observed when cranking up the pump current. At 170 mA, about 3× threshold current, optical power measured from the power meter is -5 dBm, which corresponds to on-chip power 6.8 dBm or 4.8 mW after normalizing the 8.5 dB grating coupler insertion loss and 3.3 dB Y-junction insertion loss. The optical and heterodyne spectrum are plotted in Fig. 4.13(b). The Lorentzian fit of the heterodyne spectrum has a full width half maximum (FWHM) of 1.28 MHz, indicating the hybrid laser linewidth is about 1.2 MHz.

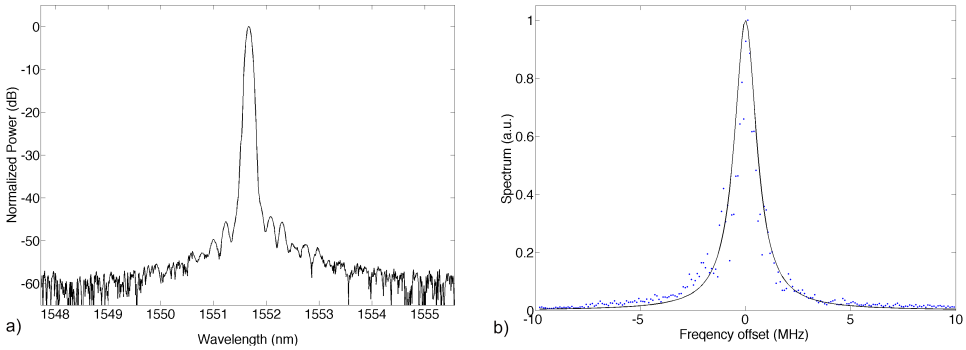

Fig. 4.13. (a) Optical spectrum with 0.1 nm resolution; (b) Heterodyne spectrum (blue dot) and a Lorentzian fit curve with 1.28 MHz FWHM.

IV. QD O-Band Laser

One major application of silicon photonics is high-speed data communications, such as optical interconnect in data centers. Short reach systems have standardized in the O-Band, the lowest dispersion wavelength window of standard single mode fibers. Thus O-Band silicon photonics devices are of great interest. However, almost all devices demonstrated up to date operate at C-Band, the fiber low loss window, because of the wider availability of lasers, amplifiers, and other testing apparatus at this wavelength range. Fortunately the knowledge of C-Band devices can be well leveraged. To the first order, passive device geometry scales with wavelength, free carrier plasma effect used for modulation is not wavelength sensitive, and germanium in photodetectors has stronger absorption at O-Band. Gain spectrum of typical materials cannot cover both wavelengths, so a different gain medium needs to be considered. Conventional quantum well lasers can be used, but QD lasers have better performance in terms of low threshold current and low thermal sensitivity [30,31]. Hence we selected a QD based RSOA. It is based on indium arsenide quantum dots in gallium arsenide with aluminum gallium arsenide barriers and commercially off-the-shelf available [32]. Facet reflectivity is >99% for the high reflective end and <1% for the anti-reflective end. The silicon chip layout and alignment

procedure is similar to the previous device. It inherits the unique advantages of QD lasers, and maintains the maturity of a commercial RSOA, and the CMOS compatibility of the silicon photonics chip. The LIV curve and spectrum are plotted in Fig. 4.14. Threshold is at 90 mA. Some kinks due to mode hopping when current is swept are also available, which is common to hybrid silicon photonics lasers. The kink near 250 mA is irregular and most likely due to mechanically or thermally induced alignment perturbations. Lasing peak appears at 1302 nm and over 50 dB SMSR is obtained.

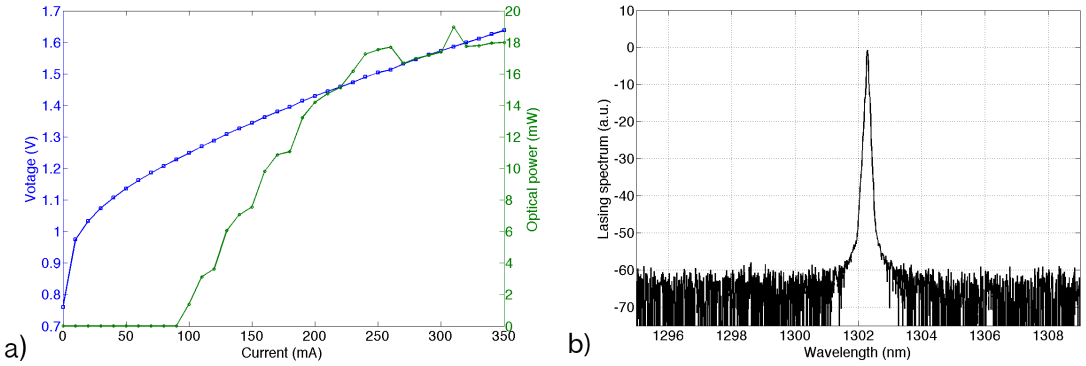

Fig. 4.14 a) Laser bias voltage and output power as a function of pump current; b) Optical spectrum of the QD O-Band laser.

I performed data transmission experiments to further verify the viability of our hybrid external cavity laser. The Laser output is non-return to zero (NRZ) modulated using a Lithium Niobate ($LiNO_3$) Mach-Zehnder modulator, and detected using InGaAs photodetector. The photocurrent is amplified and displayed on a digital communication analyzer (DCA). Clearly open eye diagram is observed at 10 Gb/s, as shown in Fig. 4.15, which is an overall testament of the laser quality, including linewidth, relative intensity noise, stability etc.

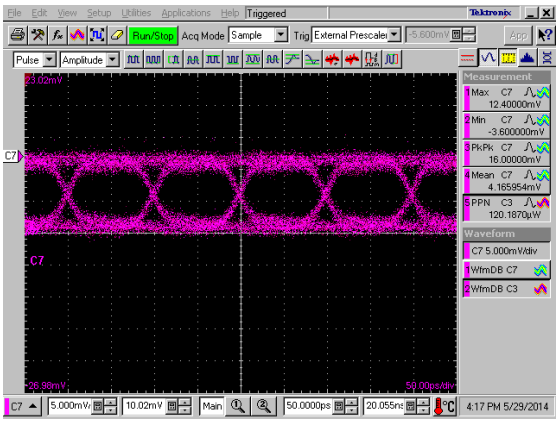

Fig. 4.15 Eye diagrams of laser output externally modulated at 10 Gb/s

The data rate was then cranked up to 40 Gb/s. A commercial DFB laser (Agere Systems A1611A/B) was used as control experiment. Due to system bandwidth limitation, longer rise and fall time is observed. I then switched to our hybrid silicon external cavity laser, and repeat the same level of eye-openness, which confirms the device under test is viable to be used in high speed data application systems.

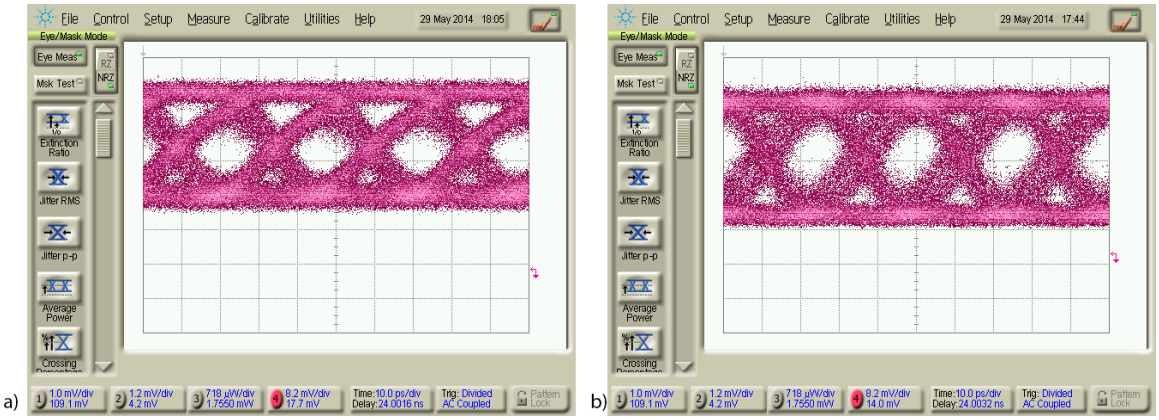

Fig. 4.16 Eye diagrams at 40 Gb/s: a) control experiment using a commercial DFB laser; b) hybrid silicon external cavity laser

4.4 Summary

Different gain integration approaches are reviewed, including heavily n-doped germanium, III-V QD, wafer bonding and RSOA butt coupling. A novel Sagnac loop and micro-ring based laser cavity is proposed, which is simple and reliable, with accurately controlled reflectivity and negligible excess loss. Resonant wavelength of a 2 μm radius

micro-ring is shown to be lithographically controlled to a standard deviation of 3.6 nm. Both C- and O-Band lasers based on Sagnac loop mirror and micro-ring cavity are demonstrated. The laser is shown to be able to be modulated at 40 Gb/s.

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CHAPTER 5. MICRO-RING THERMAL STABILIZATION

Resonant devices are critical for efficient modulation, wavelength filtering, and multiplexing. Determined by the thermo-optic coefficient of silicon, resonant wavelength drifts by 80 pm per degree temperature change, making these devices extremely vulnerable to thermal perturbations. I demonstrate resonance thermal stabilization with bandgap reference sensor and active control, which enables resonant devices to operate in practical environments. Compared to feedback using monitoring the optical power in a ring resonator, the bandgap reference senor doesn't rely on specific device functionality and operating condition and applies universally to different type of devices.

5.1 Micro-ring temperature sensitivity

Fabrication sensitivity of silicon photonics devices has been discussed in Chapter 2 and Chapter 4. Micro-ring is the most sensitive device because light passes the same path many times. It is presented in Chapter 4 that a micro-ring with radius as small as 2 μm is more robust again fabrication non-uniformities and its resonant wavelength can be lithographically controlled to with in a standard deviation of 3.6 nm. But this is still too large a range for many practical applications.

In addition to fabrication non-uniformities, silicon photonics device, same to almost all semiconductor devices, are sensitive to temperature changes. Silicon has a thermo-optic coefficient of $1.8\times10^{-4}\ K^{-1}$, determined by material property. Micro-ring resonant wavelength drift as a function of temperature change can be derived from first principles. The accumulated phase after light travels some distance l is $\varphi = \frac{2\pi}{\lambda} n_{eff}(\lambda,T) l$, where n_{eff} is expressed both as a function of wavelength and temperature. A resonant wavelength

drift means both due to the change of wavelength and temperature, the resonance condition is maintained, i.e. the phase accumulation per circumference doesn't change. Hence

$$d\varphi = \frac{\partial \varphi}{\partial \lambda} d\lambda + \frac{\partial \varphi}{\partial T} dT = 0 \tag{5.1}$$

Plug in the expression for φ, we get,

$$\frac{d\lambda}{dT} = \frac{\partial n_{eff}}{\partial T} \frac{\lambda}{n_g} \tag{5.2}$$

where n_g is the group index. Since the optical mode is tightly confined in silicon, as shown in Fig. 1.2, and also because the thermo-optic coefficient of silicon oxide is 1×10^{-5} K^{-1}, an order of magnitude smaller than that of silicon, the contribution from oxide cladding can be neglected, and Eq. 5.2 can be approximate by

$$\frac{d\lambda}{dT} = \frac{\partial n_{Si}}{\partial T} \frac{\lambda}{n_g} = 1.8\times10^{-4} \frac{\lambda}{n_g} \tag{5.3}$$

For typical single mode submicron silicon waveguide of size 500 nm × 220 nm, the group index near 1550 nm wavelength is about 4. So for per degree temperature change, the resonant wavelength will drift by about 0.07 nm, which is comparable to the FWHM the 10 μm radium ring in Chapter 4. Typical operating temperature range for optical devices is -5 °C to 75 °C. Resonant wavelength can change by 0.6 nm or 70 GHz over 80 °C. So silicon micro-ring resonators are extremely sensitive to temperature changes. Such property could be used to build temperature sensors (together with an optical spectrum analyzer) [1], or very efficient thermally tunable filters [2,3], or to compensate

off-target resonant wavelength due to fabrication errors [4,5]. One the other hand, this also leads to the serious vulnerability in practical environments.

5.2 Resonant wavelength stabilization

I. Athermal

One way to mitigate the thermal sensitivity is to use a cladding material, usually some kind of polymer, that has negative thermo-optic coefficient to balance the positive the positive thermo-optic coefficient of silicon, so the total waveguide effective index is athermal [6]. Because of the strong mode confinement, this is usually difficult to achieve without modifying the silicon core geometry. Even if one succeeds to find such material, it is likely not CMOS compatible.

II. Active feedback control

A second approach is to use active feedback control to stabilize the ring resonance again temperature variations. A resistive heater can be easily integrated on the ring as the actuator, so the problems deduce to finding a proper sensing signal to feed into the control circuitry. Different approaches have been reported, including monitoring the circulation power using a tap [7,8], or the bit error rate (BER) [9]. Monitoring BER is only applicable to a ring modulator, not other devices such as the wavelength filter used inside the laser cavity in Chapter 4. The circulating power can vary in different applications, or different operating condition of the same device, for example, an intra-cavity filter in a laser at different pump current, or a ring modulator at different bias condition or running different modulation formats. A more universal approach is to directly monitor temperature.

Almost any device on-chip has some temperature dependence. Generally there is no "fancy" electronics device like metal-oxide-semiconductor field-effect transistor (MOSFET) or bipolar junction transistor (BJT) in typical silicon photonics processes. But *pn* junction is common, which is used in both modulators and photodetectors. The current density of a *pn* junction is

$$J = J_0(e^{\frac{qV}{nkT}} - 1) \tag{5.4}$$

where J_0 is the magnitude of the saturation current density, q is fundamental charge, V is applied voltage, k is Boltzmann constant, n is the junction ideality factor, and T is temperature. The junction current does depend on temperature, but it also depends on many other factors such as junction size, doping concentration, generation and recombination rate etc. However, the bias voltage difference of two matched junctions biased at different current density, or two junctions of different sizes biased at the same current density, depends only on temperature [10]. Making two matched junctions is easy in micro-fabrication, especially when they are placed physically close.

$$\Delta V = \frac{kT}{q}\ln(\frac{I_1}{I_2}) \tag{5.5}$$

Note that ΔV is proportional to absolute temperature (PTAT). This technique is widely used in electronics, and is usually called bandgap temperature sensor. I designed a ring modulator with both bandgap sensor and integrated heater for thermal stabilization. The device layout and a photo of the chip is shown in Fig. 5.1. The pn junction phase shifter sensor accounts for the top semi ring, resistive heater is in the bottom left, and bandgap temperature sensor is in bottom right of the ring. Two pn junctions in the

bandgap temperature sensor are identical and share the same ground pin. Characterization of individual components is presented, followed by demonstration of resonance stabilization.

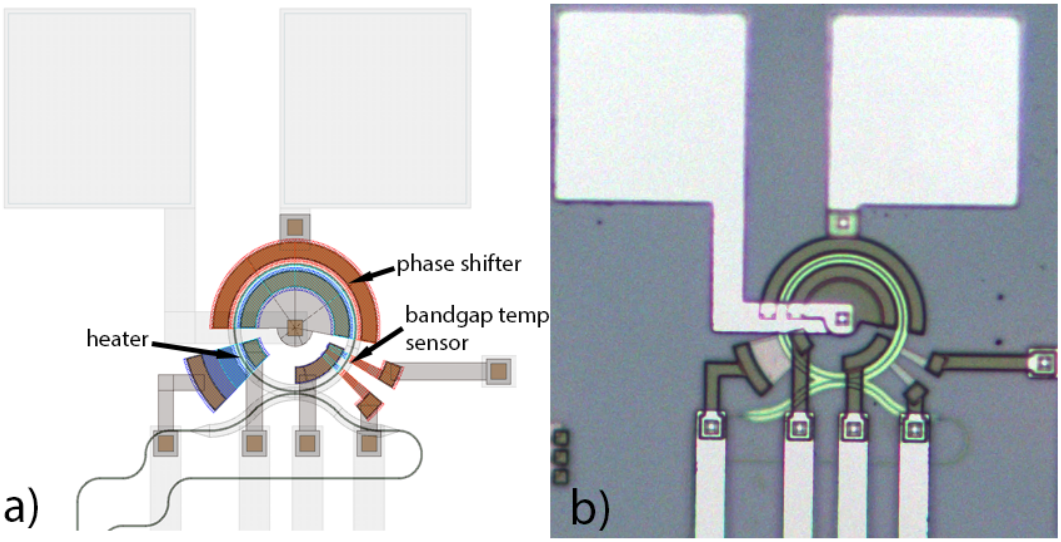

Fig. 5.1. Ring modulator with bandgap temperature sensor. Device layout (a) and device photo (b)

5.3 Device component characterization

I. Micro-ring resonator

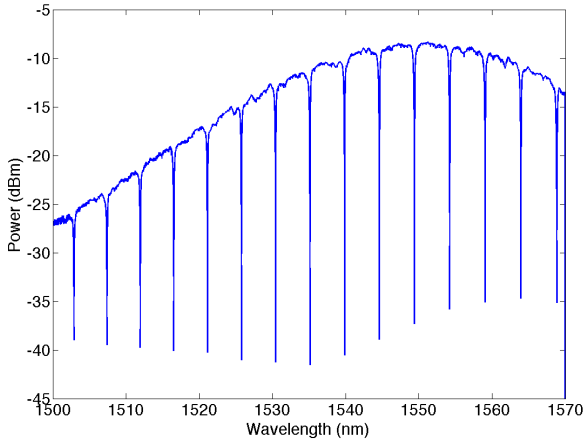

Fig. 5.2 Ring modulator spectrum at 25 °C

The ring radius is 20 µm, with a 300 nm edge-to-edge gap between the bus waveguide and ring waveguide and 2 µm straight coupling length. The circumference

leads to a FSR of 4.75 nm. Measured extinction ratio is greater than 30 dB, indicating that critical coupling is achieved. Note that some of the characterization data shown below are done on device variants with slightly lower extinction ratio, or to avoid over probing one device.

II. Resistive heater

To verify the thermal sensitivity discussed above, the wafer temperature was varied from 25 °C to 80 °C. Spectra at different temperature were record and plotted in the Fig. 5.3(a). The resonance peak was shifted by 4.38 nm, from 1548.203 nm to 1552. 592 nm over the 55 °C temperature range. So the resonance wavelength sensitivity is 0.08 nm/K, which is close to the estimated value 0.07 nm/K.

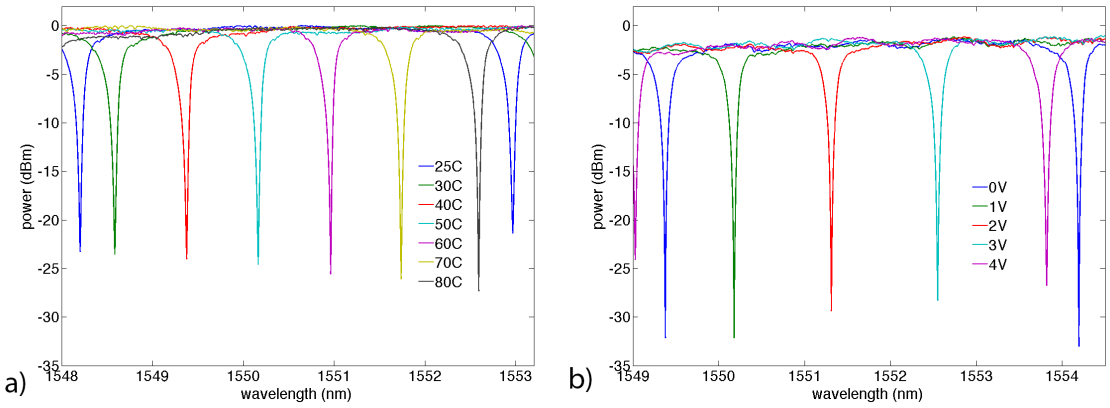

Fig. 5.3 Ring thermal tenability: a) spectra versus wafer chuck temperature, and b) spectra versus heater voltage

Next the wafer was held at 25 C, and different voltages were applied onto the heater. Heater resistance is measured to be 290 ohm by an IV sweep. As shown in Fig. 5.3(b), 4V on the heater shift the resonant wavelength by 4.44 nm, similar to the effect of increasing the wafer chuck temperature from 25 °C to 80 °C. Because temperature

change perturbs the coupling strength between the ring and bus waveguide, the extinction ratio drifted slightly as temperature was changed as well.

III. Bandgap temperature sensor

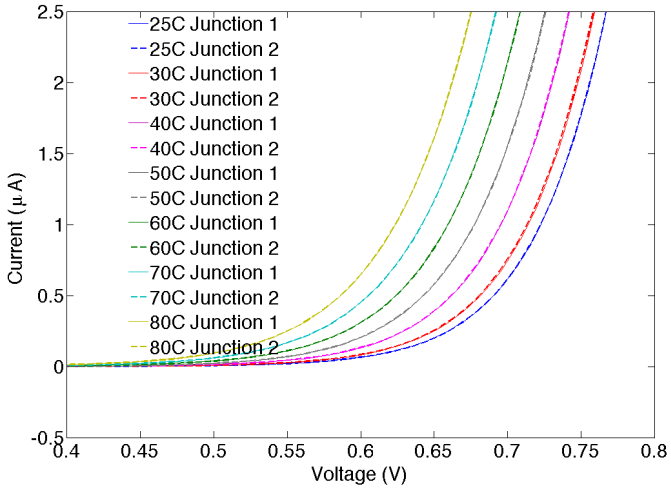

Fig. 5.4 Temperature sensing junction IV curve at different temperatures

The IV curves of two sensing junctions were recorded during the thermal cycle from 25 °C to 80 °C too, as shown in Fig. 4. IV curves of one junction are plotted using solid lines and the other with dashed lines. Data taken at the same temperature share the same color. IV curves of two junctions overlap at any temperature, showing that two junctions are perfectly matched. The response of the junction IV characteristic to temperature change is also clearly illustrated. If one sensing junction is connected to a current source of 1 μA and the other 100 nA, their bias voltages as a function of temperature are plotted in Fig. 5. The dashed line and blue line clearly shows the differential voltage increases as temperature is increased.

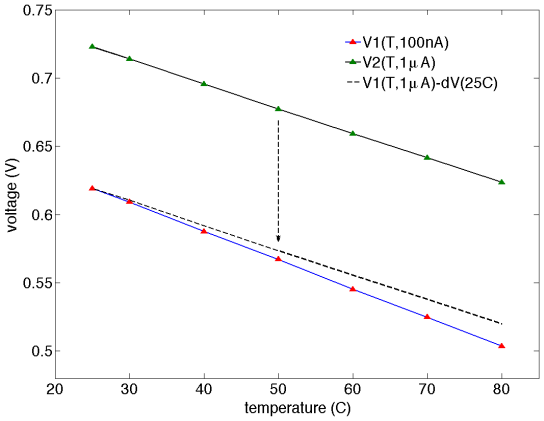

Fig. 5.5 Sensing junction bias voltage as a function of temperature. The dashed line is V1(T,1μA) minus the difference between V1(25C,1μA) and V2(25C,100nA) to show the differential voltage increase as temperature is increased

IV. PN junction phase shifter

The device also integrates a high-speed pn junction phase shifter, as shown in Fig. 5.1. The pn junction is reverse biased, and the depletion region width is modulated by the driving signal. Device transmission spectra at different bias are shown in Fig. 5.6. The phase shifter efficiency is evaluated by the resonant wavelength shift per applied drive voltage. In Fig. 5.6, resonant wavelength is shifted by 20 pm from 0 V to -1 V, corresponding to tuning efficiency of 20 pm/V.

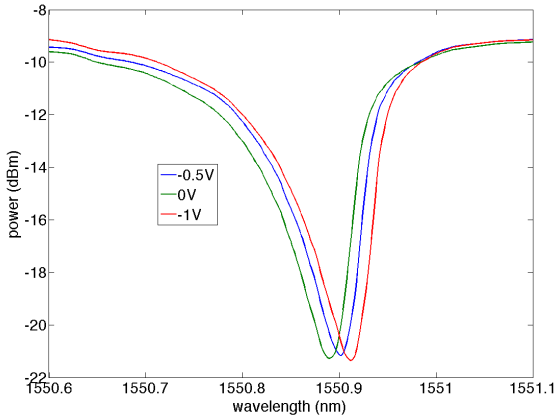

Fig. 5.6 Ring resonance shift as a function of reverse bias of the phase shifter *pn* junction

Modulation bandwidth is also characterized by measuring the s-parameters, with laser set at the 3dB point and 0 V applied bias. Analog bandwidth is around 30 GHz, as shown in Fig. 5.7, which enough for passing OOK data at 40 Gb/s.

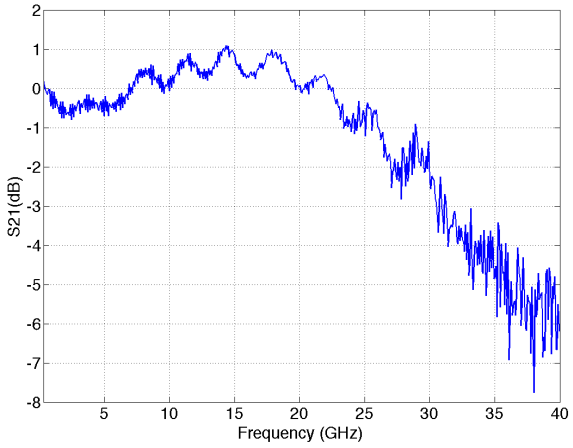

Fig. 5.7 RF S21 of the ring modulator

5.4 Resonance stabilization

The diagram for ring resonance stabilization is shown in Fig. 5.8. The differential output voltage of the bandgap temperature sensor is amplified. Then a control circuit adjusts the drive current of the resistive heater based on the amplifier output.

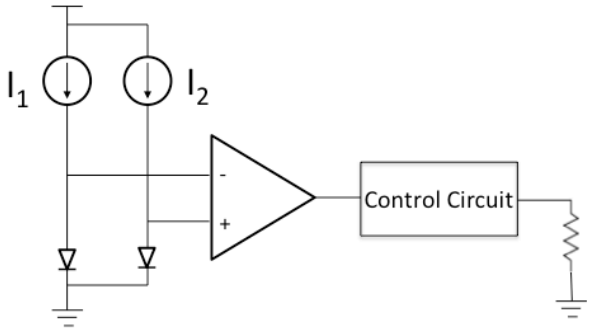

Fig. 5.8 Ring resonance stabilization schematic

The chip was mounted on a TEC to provide temperature perturbation for debugging and testing. A triangle signal was applied to the TEC input, as shown by the red curve in Fig. 5.9. With resistive heater kept open, the corresponding bandgap temperature sensor

reading was plotted in blue. It was noticed that there is some delay between the blue and read traces, because it takes some time for the TEC to respond and for the heat to propagate to the device. The feedback control system output is plotted in green. Then the control system output signal is applied to drive the resistive heater. The sensor reading with feedback control enabled is plotted in black, which is a flat line, indicating the local temperature near the ring resonator is stabilized.

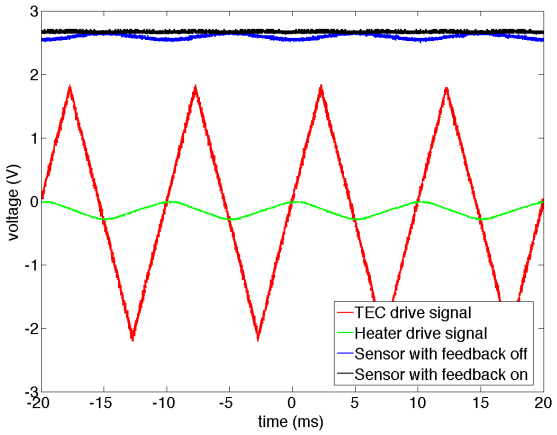

Fig. 5.9 Ring stabilization signals: TEC input voltage, bandgap temperature sensor output, and feedback control output for driving resistive heater

The ring resonator spectrum with varying temperature was recorded, as shown in Fig. 5.10. (a) shows the thermal drift of resonant wavelength, while (b) shows the stabilized resonant wavelength with active feedback control. Compared to the control system that relies on monitoring cavity circulation power or modulator BER, this device directly senses the local device temperature, making it a general and universal solution, independent of specific device function. This stabilization approach applies to a ring filter or modulator, or other type of devices, such as arrayed waveguide grating (AWG) or Echelle grating.

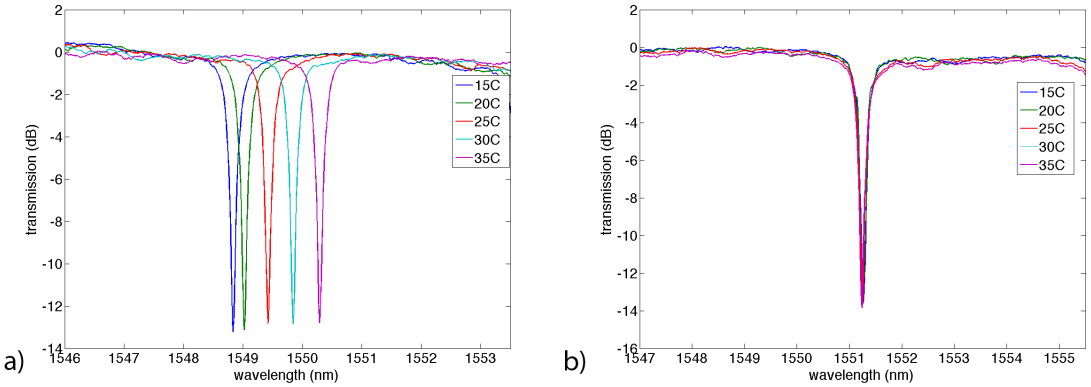

Fig. 5.10 Micro-ring resonator spectra at different temperatures: (a) feedback control system off and (b) feedback control system on

5.5 Summary

Thermal sensitivity of passive silicon photonics devices is presented and analyzed, which could be used to compensate fabrication non-uniformities. But high thermal sensitivity makes the device vulnerable to any thermal perturbation from the environment. A universal thermal stabilization approach based on bandgap temperature sensors is demonstrated. The stabilized ring resonator could be used for modulation and wavelength filtering in practical applications. The stabilization scheme can also be applied to other type of devices.

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