

Organic Semiconducting Thin Films: Device Applications and Beyond

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Abstract

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Materials Science and Engineering

Organic semiconductors show great promise for device applications, particularly as organic thin film transistors (OTFTs) and organic photovoltaics (OPVs), due to their potential for low cost, high volume fabrication when compared to traditional inorganic semiconductors. While the performance of organic devices generally lags behind the more established inorganic devices, significant growth in the field of organic semiconductors has led to rapid improvements. In this thesis, device operation and characterization of OTFT and OPV systems are explained, the dramatic effects of fabrication procedures on the charge transport performance of OTFTs are demonstrated, and the reproducibility issues inherent to OPVs are explored. The potential for self-healing behavior in organic semiconductors is also investigated.

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Chapter 1. Introduction and Background

1.1 Background on Organic Semiconductors

Organic semiconductors are a class of materials composed of a conjugated carbon backbone that exhibit semiconducting properties (Figure 1). The field of organic semiconductors began with the discovery by Shirakawa, Heeger, and MacDiarmid that halogen-doped polyacetylene could exhibit metallic like conductivity; up to 10^5 S/m.^[1] This doping removed an electron from the π conjugated structure of the polyacetylene resulting in a mobile polaron, which led to radically increased conductivity in the polymer.

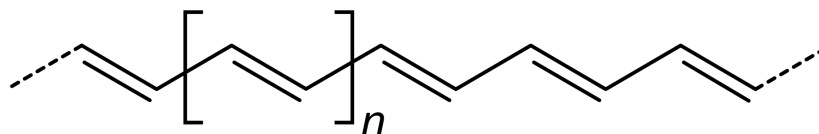


Figure 1. Polyacetylene, the first widely studied semiconducting polymer.

While doped polyacetylene exhibited conducting properties similar to metals, undoped π conjugated systems were observed to exhibit semiconducting behavior more similar to silicon or germanium. The basis of this semiconducting behavior lies in the π conjugation of the organic system. Conjugated π bonds in polymers, oligomers, and small molecules allow for electron delocalization along the molecule, giving rise to increased conductivity and electronic behavior when compared to non-conjugated organic molecules. This π conjugation explains why polyacetylene is a semiconductor that can be doped into the conducting region, while the non-conjugated polyethylene is an insulator. Since this discovery, the field has rapidly grown, with

organic semiconductors finding application in such areas as organic photovoltaics (OPV), organic thin film transistors (OTFT), organic light emitting diodes (OLED), and even more niche areas such as electronic “paper” displays and memory units. [2-6]

Organic semiconductors are currently very promising materials for device applications, however they require significant research and improvement if they are to overtake inorganic semiconductors from any sort of performance perspective. Current single crystal silicon based solar cells are routinely reported at 25% efficient, while OPV technology lags behind, with champion devices just reaching over 11% in the past few years. Multijunction inorganic cells have even been reported at efficiencies of over 44%, further exemplifying this gap in performance.^[7] A primary cause for this large difference in recorded efficiencies lies in the excitonic nature of organic semiconductors. In an inorganic semiconductor, an electron may be excited from the top of the valence band to the bottom of the conduction band via absorption of a photon with energy greater than the band gap of the material. Due to their relatively low dielectric constants, strong coulombic interactions take place between an excited electron and its resultant hole in organic semiconductors (Figure 2). The excitons that form in organic semiconductors generally have binding energies on the order of 0.2-0.5 eV, and must be dissociated in order to obtain free charge carriers. This excitonic behavior is a large consideration in the design of organic semiconductor based devices, especially in OPV.

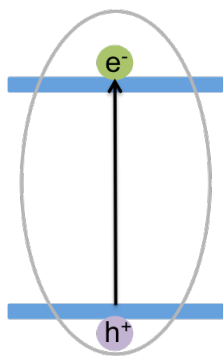


Figure 2. An exciton in a semiconducting polymer. The electron and hole are coulombically bound together and must be dissociated in order to do useful work.

Despite this gap in device performance, organic semiconductors are interesting from an economic standpoint due to their lower costs of production and processing. Organic semiconductors are an attractive alternative to the more established inorganic semiconductors such as silicon and germanium due to their solubility in common and inexpensive organic solvents. While inorganic semiconductors must be carefully grown or deposited in high temperature or vacuum conditions, deposition of organic semiconductors can be performed using much simpler techniques, including spin coating, drop casting, and doctor blading, among others. This ease of processibility results in much lower associated costs with the fabrication of organic semiconductor based devices. This cost difference can be quantified by considering the energy pay back time (EPBT) in the case of an OPV.

$$EPBT = \frac{\text{Total energy to produce, install, and decommission device per unit time}}{\text{Energy produced per unit time}} \quad (1)$$

Recent review articles have estimated the EPBT for an OPV to be on the order of days to weeks, while the EPBT of inorganic photovoltaics is more commonly accepted to be on the order of years.^[8-10] This large difference in EPBT assumes an average lifetime of 15 years for OPV, and around twice that for inorganic photovoltaic.

Organic semiconducting materials may be easily be compared through a variety of benchmark properties, including absorption spectrum, quantum efficiency, and charge carrier mobility. Charge carrier mobility is a particularly important property for organic semiconductors for applications in OPV and OTFT, since it is a measure of the ease of charge transport through the material, and thereby the material's conductivity. Charge carrier mobility is typically

reported in units of $\text{cm}^2/(\text{V}\cdot\text{s})$. A large charge carrier mobility is highly desirable in almost any application, since it identifies the material as an effective charge transport pathway. In OPVs, high charge carrier mobility is necessary for high-density charge extraction from a device. In organic transistors, a high charge carrier mobility allows for more current to flow through the transistor when it is turned on, thereby increasing the efficacy and selectivity of the transistor. A few popular methods for extracting charge carrier mobilities for organic semiconducting materials will be exploring in the following sections.

1.2 Device Operating Principles

Organic semiconductors are a promising class of materials for device applications. In particular, the ease of processing of these materials makes them ideal candidates for low cost, thin film based devices. Two of the most prevalent of these devices are OPVs and OTFTs.

1.2.1 Organic Thin Film Transistor

OTFTs function in much the same way as traditional silicon transistors, with a gate, a dielectric, a transport layer, and source and drain contacts. Two of the most common OTFT device architectures utilize a bottom gate, with either top or bottom contacts (Figure 3).

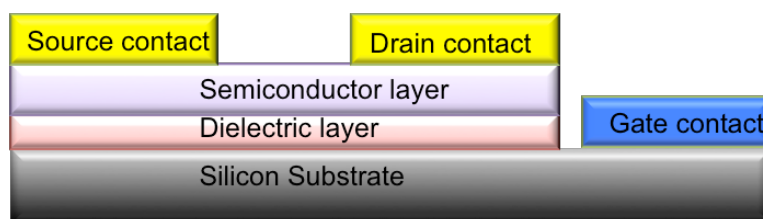


Figure 3. Typical top-contact, bottom-gate OTFT device architecture.

OTFTs may be either p-type or n-type. In a p-type OTFT, the semiconducting material conducts holes under a negative gate bias. In an n-type OTFT, electrons are conducted under a positive gate bias instead. In this research, p-type OTFTs were predominantly studied with a top contact device architecture, so the focus will be on this specific system throughout the following explanations.

In a p-type OTFT, a negative gate voltage (V_G) causes capacitive coupling across the dielectric layer, resulting in an increased positive charge carrier concentration near the bottom of the organic semiconducting film. The resulting charge carriers can be collected if a second bias is applied between the source and drain electrodes. The current that can be extracted from a transistor is dependent on the drain voltage (V_D), the threshold voltage (V_T), and V_G . V_T can be described as the applied gate voltage necessary to induce mobile charge carriers in the semiconducting thin film. An OTFT that is conducting current may either be in the linear or saturation regime. For a p-type OTFT with all negative biases, the device is said to be in the linear regime if $|V_D| < |V_G - V_T|$. In the linear regime, the drain current (I_D) is linearly proportional to V_G and proportional to V_D^2 . The following relation describes the current in the linear regime.

$$I_{D,lin} = \frac{W}{L} C_{ox} \mu_{lin} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right] \quad (2)$$

Where W is the width of the transistor channel as defined by the contacts, L is the length of the transistor, C_{ox} is the capacitance of the dielectric per unit area, and μ_{lin} is the charge carrier mobility within the linear regime. If $|V_D| > |V_G - V_T|$, the device is in the saturation regime. I_D in the saturation region is largely independent of V_D , due to the formation of a depletion region near the drain electrode causing a “pinch off” of the charge carrier concentration across the transistor (Figure 4). Further increases in V_D in the depletion regime will change the width of the depletion

region, but the device will continue to function as normal as long as the L is much greater than the width of the depletion region.^[11]

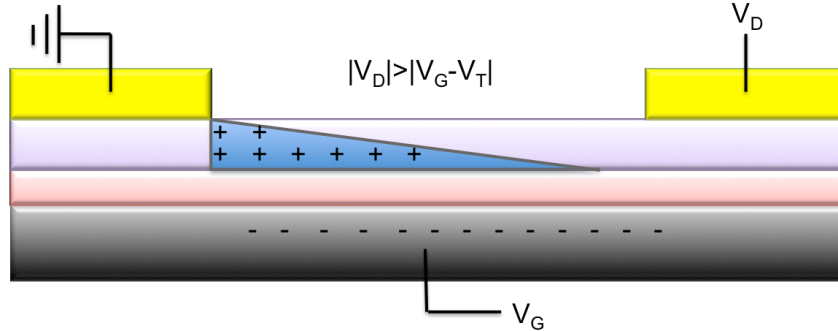


Figure 4. Carrier concentration (dashed area) pinch off in the saturation regime of the device. The blue region represents positive charge distribution. Notice that the channel no longer reaches all the way between contacts.

The current within the saturation region is given by:

$$I_{D,sat} = \frac{W}{2L} C_{ox} \mu_{sat} (V_G - V_T)^2 \quad (3)$$

This equation can be rearranged to allow for calculation of the expected charge carrier mobility in the saturation region from an I_D - V_G curve.

$$\mu_{sat}^{calculated} = \frac{1}{C_{ox} W / 2L} \left(\frac{d\sqrt{|I_{D,sat}|}}{dV_G} \right)^2 \quad (4)$$

From this equation we can see that the saturation charge carrier mobility of the semiconducting material in the OTFT can be obtained by calculating the slope of the linear region of a plot of $I_{D,sat}^{1/2}$ vs. V_G .^[12] A similar sort of rearrangement may be performed with equation 2 to calculate the linear charge carrier mobility, however the saturation mobility is much more widely reported and compared, so future references to charge carrier mobility may be assumed to refer specifically the saturation charge carrier mobility.

Threshold voltage and charge carrier mobility are two very important parameters to consider when choosing materials for transistor applications. Another prominent parameter that is worth mentioning is the on-off ratio, which is a measure of the current ratio between the on

state and the off. Whether in the linear or saturation regime, a transistor is considered on if $V_G > V_T$, and off if $V_G < V_T$.

1.2.2 Organic Photovoltaics

OTFTs are a popular application for organic semiconducting thin films that can be used to calculate valuable material properties, but the most prominent application of organic semiconductors is within the area of OPVs. As mentioned in the previous section, organic semiconductors are an attractive choice for photovoltaic applications due to their relatively low production costs and high throughput potential. OPVs may be fabricated using many different device architectures; standard, inverted, and tandem devices are all frequently reported.^[2,13,14] Additionally, differences in fabrication may have large influences on the performance of OPV. Changing annealing time and temperature, and including solvent additives and interfacial layers are all popular methods for tuning device performance.

Standard OPVs are generally formed by spin coating a conductive interfacial layer on top of an indium doped tin oxide (ITO) substrate (Figure 5). Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) is a common interfacial layer due to its high conductivity and ductility, which allow for fabrication of flexible devices. Recent research has seen an increase in the use of transition metal oxide as a bottom interfacial layer in order to avoid stability problems that are known to arise due to the acidity of PEDOT:PSS.^[2] On top of this interfacial layer, an active layer is deposited from a solution of electron donating and electron accepting materials *via* spin coating. Contacts are then deposited, frequently *via* thermal evaporation through a shadow mask. Thermal annealing may be done before or after the evaporation step, and the preferred order generally depends on the composition of the active layer.

Single junction cells with such an architecture may be further improved through incorporation of charge carrier highways in the active layer, or through use of solvent additives to optimize the microstructure of the active layer.^[14-16]

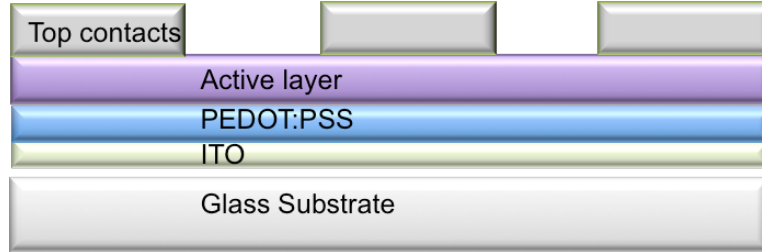


Figure 5. Standard OPV device architecture.

Some of the most prominent factors of interest when considering an OPV system are the short circuit current density (J_{sc}), the open circuit voltage (V_{oc}), the fill factor (FF), and the power conversion efficiency (PCE). J_{sc} is a measure of the amount of current produced when the applied voltage on the solar cell is 0. J_{sc} is generally reported preferentially over short circuit current as it standardizes short circuit current values by device area, though devices with smaller areas are often acknowledged to yield higher J_{sc} values than a similar system with a larger area due to the relatively high sheet resistance of ITO.^[17] V_{oc} is the maximum voltage that a specific solar cell can produce. The FF is a measure of the maximum power that can be obtained from a solar cell. The PCE of a device is arguably the most important parameter, taking into account the previous three parameters and representing the efficiency and potential applicability of the device. The PCE is given by the following relation:

$$PCE = \frac{V_{oc}J_{sc}FF}{P_i} \quad (5)$$

Where P_i is the power incident on the solar cell.

The operation of an OPV can be split into four primary steps, light absorption, exciton diffusion, exciton dissociation, and charge collection. The process begins when an incident

photon is absorbed in the active layer of the OPV, promoting an electron from the highest occupied molecular orbital (HOMO) to the lowest unoccupied molecular orbital (LUMO) in the donor material. Due to the relatively low dielectric constants of organic semiconductors, excited electrons are not sufficiently screened from their holes, and the coulombic attraction between the electron and hole results in the generation of an exciton. Excitons in organic semiconductors typically have diffusion lengths of 5-10 nm wherein they must be dissociated in order to avoid recombination of the electron and hole.^[2,18] Dissociation occurs at the donor-acceptor material interface, with the electron moving into the acceptor material and the hole remaining in the donor. Due to the limited diffusion length of excitons, and the necessity for each exciton to reach a donor-acceptor material interface, a unique active layer morphology known as the bulk heterojunction (BHJ) is almost exclusively used in OPV fabrication (Figure 6). The ideal bulk BHJ ensures that an exciton is always within 5-10 nm of a dissociation interface in order to harvest the maximum amount of charges from each device.

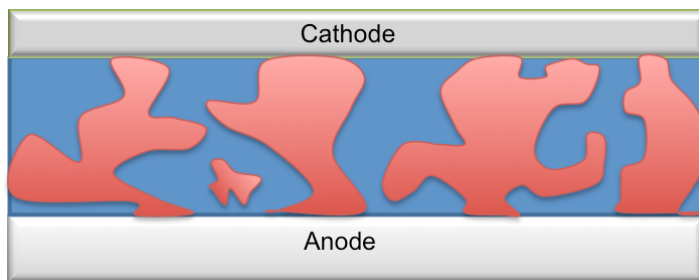


Figure 6. Simplified BHJ. Donor and acceptor regions would ideally be no more than 20 nm in width to ensure maximum exciton dissociation. Note that only the domains that contact the correct electrode contribute to the device's performance. Isolated regions trap charge.

In order for exciton dissociation to occur at the material interface, the energy difference between the LUMO of the donor material and the LUMO of the acceptor material must be at least 0.3 eV. Upon exciton dissociation, the free charge carriers may be transported to their corresponding electrodes and collected to do useful work (Figure 6). It is during the charge

collection step of OPV operation that the importance of charge carrier mobility becomes apparent once again. A material with high charge carrier mobility for its respective charge carrier will improve the performance of the entire system, increasing the rate of charge extraction and minimizing losses within charge trap sites. Additionally, balanced charge carrier mobilities for both the electron and the hole are known to reduce recombination losses in an OPV system and thereby further increase efficiency.^[19]

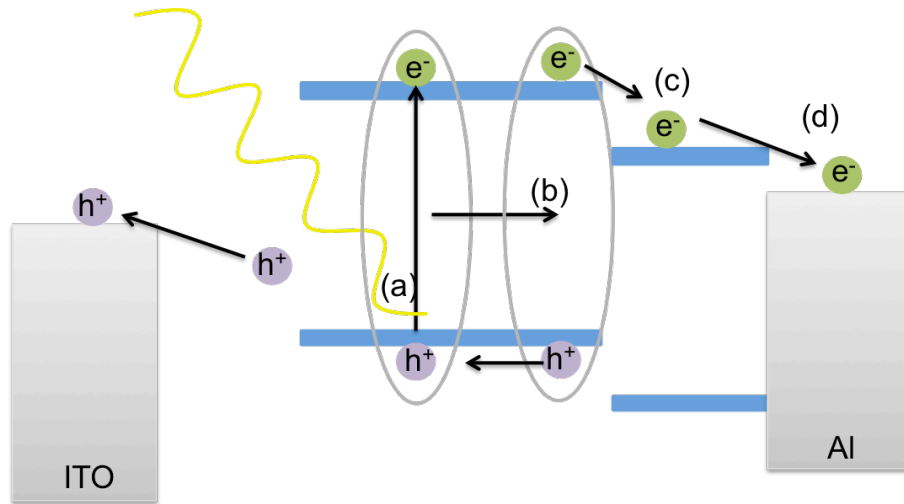


Figure 7. Schematic detailing OPV operation. Light absorption (a), exciton diffusion (b), exciton dissociation (c), and charge collection (d), are all vital steps that require optimization.

OPV architectures may also be used to obtain charge carrier mobilities *via* the use of the space charge limited current (SCLC) technique. Device architectures for SCLC devices are almost identical to OPVs except for the electrode material choice. In SCLC devices, the electrode materials are deliberately chosen to block extraction of a single type of charge carrier, thereby only investigating the transport properties of either the electron or hole. When a voltage is applied across this diode, unipolar charge is injected from one of the electrodes into the semiconducting film. This charge injection results in a build up of space charge, which opposes further charge injection. The space charge quickly increases and limits the charge injection rate

to the point where charges are only injected to replace charges extracted at the opposite electrode. The current density in this space charge limited regime is given by the Mott-Gurney law:

$$J_{sclc} = \frac{9}{8} \mu_{sclc} \varepsilon \frac{V^2}{d^3} \quad (6)$$

Where μ_{sclc} is the charge carrier mobility, ε is the permittivity of the film, V is the applied voltage, and d is the film thickness. Charge carrier mobility is known to vary with applied electric field, so the Mott-Gurney law is typically modified to account for this field dependence.

$$J_{sclc} = \frac{9}{8} \varepsilon \frac{V^2}{d^3} \mu_0 * \exp\left(0.89\gamma \sqrt{\frac{V}{d}}\right) \quad (7)$$

Where μ_0 is the zero-field charge carrier mobility, and γ is a measure of the strength of the field dependence of μ_{sclc} .

Chapter 2. DFBT System

2.1 Introduction

The polymers investigated in this section were prepared by Colleen Scott's group at Mississippi State University, and were based around the electron withdrawing difluorobenzothiadiazole (DFBT) unit, and its selenium variant (Figure 8).

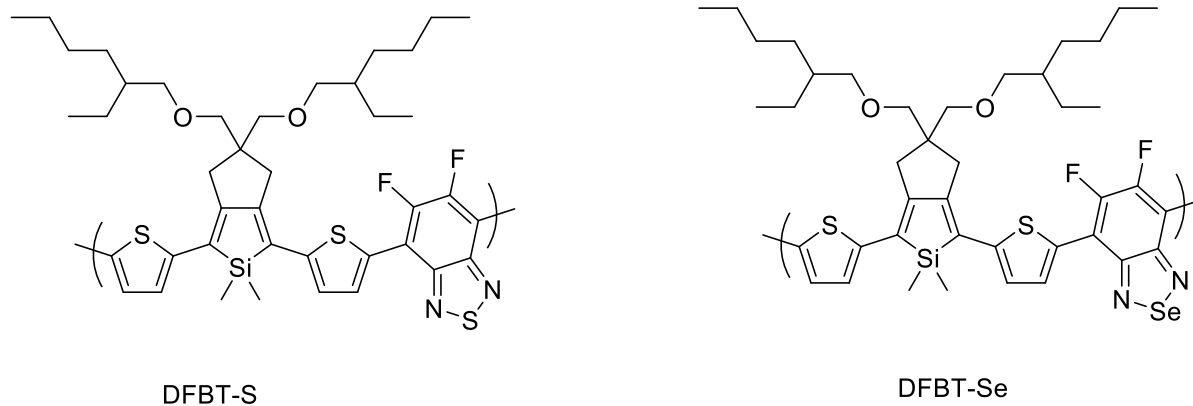


Figure 8. DFBT polymers synthesized by Colleen Scott's group at Mississippi State University.

DFBT based polymers show great promise as a donor molecules for OPV applications, with recent publications showing single junction DFBT OPVs at greater than 7.5% PCE.^[14] In order to investigate the charge transport properties of these polymers, transistors were fabricated using the top contact transistor architectures outlined in section 1.2.1. Devices were fabricated under various conditions in order to identify the fabrication conditions that would produce the highest performing devices.

2.2 Methods

2.2.1 Substrate Preparation

All devices were fabricated on silicon substrates with thermal oxide grown on top, which were cleaned with detergent and deionized (DI) water before sequential 15 min ultrasonication in DI water, acetone, and isopropyl alcohol (IPA) Substrates were then cleaned by oxygen plasma for an additional 15 min in order to remove any residual organic contaminants. Various surface treatments were attempted prior to spin coating, in order to attempt to improve the morphology and charge transport properties of the polymer layer.

2.2.2 General Device Fabrication

Solutions were prepared at least 12 h before spin coating, using different solvents, and were allowed to stir at 550 rpm and 60 °C until immediately before spin coating. Solution concentrations were all held constant at 5 mg/mL. Spin coating was performed in an inert glovebox environment, with various spin speeds, using 60 μL of solution per substrate. Gold contacts were then deposited *via* thermal evaporation through a shadow mask at a rate of 1 $\text{\AA}/\text{s}$ and were 100 nm thick. The mask used for evaporation resulted in devices with a channel width of 1000 μm and a channel length of 100 μm . Devices were annealed at various temperatures and times. Different solvents, surface treatments, spin speeds, and annealing conditions were all utilized in order to identify the fabrication procedure that resulted in devices with the highest hole mobilities.

2.2.3 Device Testing Procedures

All devices were tested using a Signatone Probe Station in combination with a Hewlett Packard 4145B Semiconductor Parameter Analyzer system. Negative gate voltages were applied in order to induce positive charge carriers in the transistor channel. As a donor molecule, the hole mobility of DFBT is of primary interest. I_D - V_G curves were obtained by sweeping from gate voltages of 0 V to -100 V with a constant V_D of -100 V. I_D - V_D curves were obtained for gate voltages of 0 V, 20 V, 40 V, 60 V, 80 V, and 100 V and were used to confirm that V_D of -100 V was sufficient to drive all charge carriers through the device channel.

2.2.4 Surface Treatment

Surface treatments are commonly employed in OTFT systems in order to lower the surface energy between the gate dielectric and the semiconducting layer, allowing for better adhesion, smoother surfaces, and higher performing devices.^[20] In this work, two primary surface treatments were investigated for the DFBT system. The first surface modification utilized a vapor deposited octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM). This OTS SAM was deposited *via* a custom vapor deposition process based on established methods.^[21] The process involved the use of a small volume of OTS in an open vial, covered with a crystallization dish inside of a vacuum over. Clean substrates were placed inside of the crystallization dish as well, and a rough vacuum was pulled over the entire system. Temperature was increased to roughly 60 °C for 2 h to ensure that the OTS completely transformed into the vapor phase. After 2 h of vacuum heating, the vacuum line was closed, leaving a local OTS vapor phase inside of the crystallization dish. The substrates were left under this local OTS vapor overnight, allowing the SAMs to form *via* spontaneous adsorption and rearrangement of OTS molecules (Figure 9). Benzocyclobutene (BCB) was also used as a surface treatment, in an effort to passivate the silicon dioxide layer and improve uniformity of the semiconducting layer. BCB layers were spin coated at 4000 rpm for 60 s, using 100 μ L of 1 wt% BCB in toluene solution per substrate.

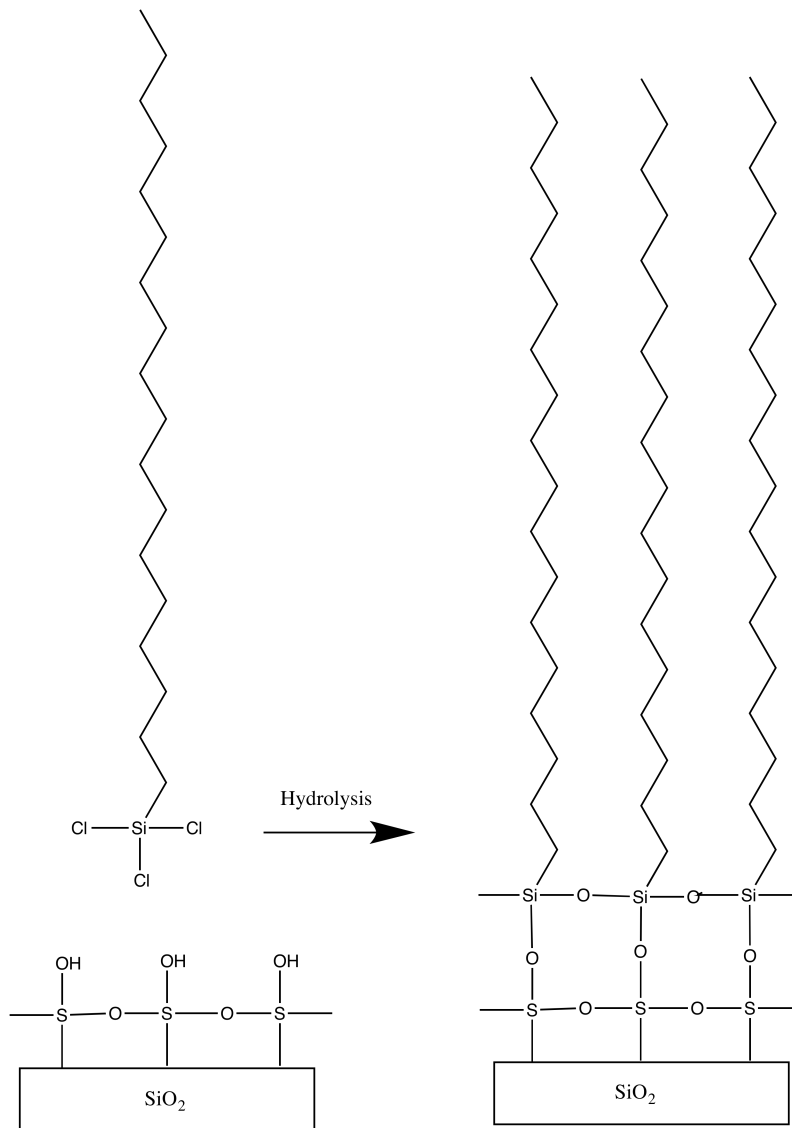


Figure 9. Schematic illustrating OTS adsorption to a SiO₂ substrate *via* hydrolysis. Covalent bonding between the molecules and the substrate results in a highly ordered layer.

2.3

Results and Discussion

Device mobilities are recorded and discussed for all factors investigated. All mobility values are for saturation hole mobility and are reported in cm²/(V.s). All device efficiencies were obtained through the use of equation 4 and fitting to the saturation regime in a curve of

$$\sqrt{|I_{D,sat}|} \text{ vs. } V_G.$$

2.3.1 Solvent Choice

Devices were fabricated from both DFBT-S and DFBT-Se polymers using both anhydrous chloroform and anhydrous tetrahydrofuran (THF) as solvents. Solutions were spin coated onto clean, untreated SiO₂ substrates at 1500 rpm for 60 s and annealed at 150 °C for 10 min after contact evaporation. From the hole mobility values collected, chloroform was identified as the superior solvent for DFBT-S and THF the superior solvent for DFBT-Se, though the distinction for DFBT-Se was not as significant (Table 1).

Table 1. Hole mobility values for devices fabricated from polymer solutions using different solvents.

<i>Polymer</i>	DFBT-S		DFBT-Se	
<i>Solvent</i>	THF	CHCl₃	THF	CHCl₃
<i>Average Mobility (cm²/(V.s))</i>	4×10 ⁻⁴	9×10 ⁻⁴	1.0×10 ⁻⁴	9×10 ⁻⁵
<i>St. dev.</i>	2×10 ⁻⁴	3×10 ⁻⁴	0.6×10 ⁻⁴	4×10 ⁻⁵

2.3.2 Surface Treatment

Surface treatment procedures were conducted as outlined in section 2.2.4. Solutions were spin coated onto cleaned and treated substrates and fabricated using the same conditions as in section 2.3.1, with chloroform used for DFBT-S and THF used for DFBT-S. OTS and BCB treated surfaces were compared against devices fabricated on clean, bare SiO₂ surfaces. Surface treatment resulted in the most dramatic increase in device performance of any factors investigated, with OTS clearly producing the highest performing devices for both polymers (Table 2). This increase in recorded mobilities may be due to preferential polymer arrangement due to interactions between the polymer and the OTS layer resulting in a more ordered and crystalline film, thereby increasing the ease of charge transport through the layer, however

further studies would be necessary to confirm this. BCB was found to actually drastically reduce device mobility when compared to bare SiO₂, possibly due to the BCB film acting as an insulating layer between the semiconductor and dielectric layer.

Table 2. Hole mobility values for devices fabricated from both polymers using different surface treatments.

<i>Polymer</i>	DFBT-S			DFBT-Se		
<i>Treatment</i>	OTS	BCB	Clean	OTS	BCB	Clean
<i>Average Mobility (cm²/(V.s))</i>	1.1×10 ⁻²	2.2×10 ⁻⁸	1.17×10 ⁻⁵	6×10 ⁻⁴	3×10 ⁻⁸	2.5×10 ⁻⁶
<i>St. dev.</i>	0.9×10 ⁻²	0.7×10 ⁻⁸	0.03×10 ⁻⁵	6×10 ⁻⁴	2×10 ⁻⁸	0.2×10 ⁻⁶

2.3.3 Spin Speed

Devices were fabricated using optimal solvents, on clean SiO₂. Spin speeds of 1000 rpm, 1500 rpm, and 2000 rpm were investigated for both polymers. Slower spin speeds resulted in higher charge carrier mobilities for both polymer variants (Table 3). Slight variations in performance are noticeable between devices batches, likely due to differences in wait time between device annealing and testing. Due to this, mobilities of devices were only compared within the same batch when deciding on optimal fabrication conditions.

Table 3. Hole mobility values for devices fabricated using various spin speeds during semiconductor layer deposition.

<i>Polymer</i>	DFBT-S			DFBT-Se		
<i>Spin speed</i>	1000 rpm	1500 rpm	2000 rpm	1000 rpm	1500 rpm	2000 rpm
<i>Average Mobility (cm²/(V.s))</i>	3.0×10 ⁻⁵	2.0×10 ⁻⁵	2.1×10 ⁻⁵	3.9×10 ⁻⁶	2.9×10 ⁻⁶	3.2×10 ⁻⁶
<i>St. dev.</i>	0.7×10 ⁻⁵	0.3×10 ⁻⁵	0.2×10 ⁻⁵	0.4×10 ⁻⁶	0.2×10 ⁻⁶	0.4×10 ⁻⁶

2.3.4 Annealing Temperature

Annealing temperatures of 125 °C, 150 °C, and 175 °C were investigated for each polymer. Devices were fabricated using chloroform and THF for DFBT-S and DFBT-Se, respectively. OTS surface treated substrates were spin coated at 1000 rpm for 60 s prior to evaporation and annealing. All annealing was done for 10 min. 175 °C annealing for 10 min resulted in the devices with the highest mobility for both polymers (Table 4). In order to determine if higher temperature annealing would produce higher mobility, devices were fabricated with 200 °C annealing temperature during annealing time testing, and results were compared.

Table 4. Hole mobility values for devices annealed at different temperatures.

<i>Polymer</i>	DFBT-S			DFBT-Se		
<i>Annealing T.</i>	125 °C	150 °C	175 °C	125 °C	150 °C	175 °C
<i>Average Mobility (cm²/(V.s))</i>	2.2×10^{-3}	2.7×10^{-2}	3.5×10^{-2}	9×10^{-5}	2.1×10^{-4}	5×10^{-4}
<i>St. dev.</i>	0.1×10^{-3}	0.7×10^{-2}	0.2×10^{-2}	5×10^{-5}	0.3×10^{-4}	3×10^{-4}

2.3.5 Annealing Time

In order to determine the effects of annealing time on device mobility, devices made of both polymers were annealed at 175 °C for 5 min, 10 min, and 15 min. Additionally, some devices were annealed at 200 °C for 10 min and compared to the 175 °C annealed devices to decide if even higher temperature annealing would further benefit mobility. Unfortunately, due to mechanical difficulties with the Signatone Probe Station, mobility values were only recorded for the DFBT-S polymer. However, based on past trends, it is likely that the ideal fabrication conditions for the DFBT-S polymer would also be the ideal conditions for the DFBT-Se

polymer. Annealing at 175 °C for 10 min was determined to have produced the best films due to the significantly smaller standard deviation or the results for that group, though the difference between the 10 and 15 min annealing times is not dramatic (Table 5). Annealing at 200 °C for 10 min resulted in the worst devices. It is possible that 200 °C annealing causes degradation in the polymer, though additional studies would have to be conducted to confirm this.

Table 5. Hole mobility values for DFBT-S devices annealed for different time periods. 200 °C is compared to 175 °C annealing.

<i>Polymer</i>	DFBT-S			
<i>Annealing T.</i>	175 °C	175 °C	175 °C	200 °C
<i>Annealing time</i>	5 min	10 min	15 min	10 min
<i>Average Mobility (cm²/(V.s))</i>	6.2×10 ⁻³	1.1×10 ⁻²	1.2×10 ⁻²	2×10 ⁻³
<i>St. dev.</i>	0.4×10 ⁻³	0.3×10 ⁻²	0.8×10 ⁻²	1×10 ⁻³

2.4 Conclusions

The device optimization conducted in this chapter demonstrates that device fabrication conditions play a substantial role in determining the recorded mobility values of an organic semiconductor in an OTFT architecture (Table 6). Comparing initial mobilities obtained during section 2.3.1 to the highest mobility values, obtained during section 2.3.4, dramatic mobility increases are evident for both polymers.

Table 6. Total improvement in recorded hole mobility values over the course of DFBT device optimization.

	DFBT-S	DFBT-Se
Initial Mobility (cm ² /(V.s))	9×10 ⁻⁴	1×10 ⁻⁴
Final Mobility (cm ² /(V.s))	3.5×10 ⁻²	5×10 ⁻⁴
Improvement (%)	4000	500

Of this improvement, surface modification was found to play the largest role and was responsible for the significant orders of magnitude increases between the two fabrication schemes. Solvent choice, spin speed, annealing temperature, and annealing time all influenced

recorded mobility values as well, albeit to a lesser extent, with differences between devices due to those factors generally limited to a single order of magnitude at most. The final, optimized device fabrication scheme is shown below (Table 7).

Table 7. Optimized fabrication scheme for both DFBT polymers.

<i>Polymer</i>	DFBT-S	DFBT-Se
<i>Solvent</i>	CHCl ₃	THF
<i>Surface Treatment</i>	OTS	OTS
<i>Spin Speed</i>	1000 rpm	1000 rpm
<i>Annealing Temp.</i>	175 °C	175 °C
<i>Annealing Time</i>	10 min	10 min

The curves used to obtain the mobility value of a DFBT-S device from section 2.3.1 and a DFBT-S device after optimization are plotted below for comparison (Figure 10).

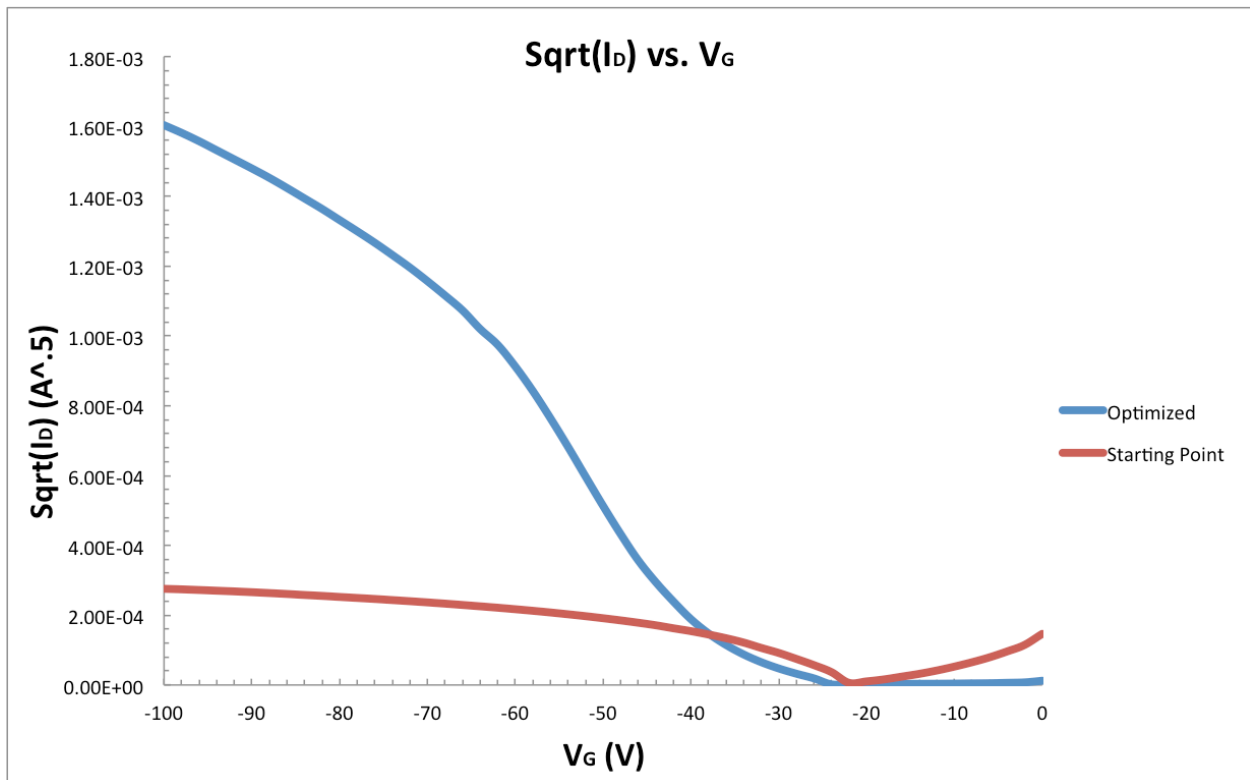


Figure 10. Plots of $\text{Sqrt}(I_D)$ vs. V_G for both a non optimized and an optimized DFBT-S device. The mobility is taken to be the slope of the linear region of each plot, multiplied by system constants, according to eqn. 4. The dramatic difference in mobility value is apparent.

2.5 DFBT Summary

The charge transport properties of DFBT polymers in an OTFT architecture were investigated. Fabrication choices were found to play a massive role in the recorded hole mobility values of these polymers. Solvent choice, substrate surface treatment, spin speed, and annealing conditions were all investigated and found to have a significant impact on the charge transport performance of DFBT thin films, with surface treatment having the most impact. Fabrication optimization led to an improvement of roughly 4000% in the hole mobility values exhibited by DFBT-S, while the same optimization led to an order of magnitude smaller improvement of 500% in the DFBT-Se polymer.

Chapter 3. P3HT:PCBM System

3.1 Introduction

The OPV system composed of a poly(3-hexylthiophene-2,5-diyl) (P3HT) donor and a phenyl-C₆₁-butyric acid methyl ester (PCBM) acceptor is one of the most studied, and is often considered a benchmark of the OPV field (Figure 11).^[2,10,14] This system is particularly useful as an initial test system to compare device efficiencies to literature values and ensure that fabrication and testing conditions allow for devices with reproducible behavior. In this work, the P3HT:PCBM system was used primarily as a first fabrication system used with the intent of moving on to other systems that included less studied materials synthesized by collaborating groups.

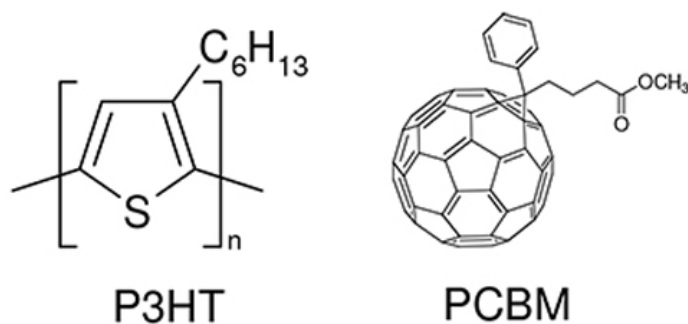


Figure 11. P3HT and PCBM are two of the most common molecules used in OPV systems.

3.2 Methods

3.2.1 Substrate Preparation

All substrates were cleaned in an identical manner to those used in OTFTs, with the only difference being that the substrates used for OPVs are ITO coated glass instead of diced silicon wafers with thermal oxide grown on top. Refer to section 2.2.1 for cleaning procedures. Surface treatments and SAMs were not utilized for this system.

3.2.2 General Device Fabrication

All devices were fabricated using the typical OPV BHJ architecture described in section 1.2.2. A 40 nm thick film of PEDOT:PSS was deposited onto a clean substrate *via* spin coating 0.45 μm filtered PEDOT:PSS solution in air at 2500 rpm for 60 s, using 60 μL of solution per substrate. The substrates were then annealed at 150 $^{\circ}\text{C}$ for 10 min before being transferred into a glovebox for active layer deposition. Active layer solutions were prepared using anhydrous chloroform, and all solutions used for the P3HT:PCBM system were held at a concentration of 40 mg/mL, using a donor:acceptor mass ratio of 1:0.6. Solutions were left to stir in a glovebox at

550 rpm and 60 °C for at least 12 h prior to filtering and spin coating and were timed so that spin coating of active layer was performed as soon as possible after annealing the PEDOT:PSS layer. Solutions were filtered using a 0.2 µm filter, and then spin coated at 3000 rpm for 60 s also using 60 µL of solution per substrate. Active layer film thickness was measured at 120 nm using profilometry. Aluminum contacts were deposited *via* thermal evaporation at a rate of 2 Å/s for a contact thickness of 100 nm. Devices were then annealed at 140 °C for 10 min prior to testing.

3.2.3 Device Testing Procedures

All efficiency values and other device parameters were calculated from devices under 100 mW/cm² air mass (AM) 1.5 simulated solar spectrum illumination, generated by a xenon source lamp. Current-voltage curves for each device were obtained *via* the use of Keithley 2400 source meter. Of the 16 devices present on each substrate, the characteristics of the highest performing 6-8 devices were recorded and averaged across substrates. P3HT:PCBM systems are typically reported as having device PCE of 3-4%, but this value may vary dramatically depending on exact fabrication conditions.^[22] Recorded device parameters obtained from an average of 15 devices are listed in the table below.

3.3 Results and Discussion

3.3.1 “S” Shaped J-V Curve

Initial P3HT:PCBM devices had poor performance, exhibiting PCE values of under 1%. The devices displayed average V_{oc} values of 0.58 V and J_{sc} values of 63.1 A/m², which are lower than those reported in the literature.^[13] The largest factor influencing this poor performance was the excessively low fill factor of the devices, recorded at 0.199, roughly one third or what was

expected. By looking at a J-V curve of one of these earlier devices, we immediately see that the shape of the J-V curve is atypical and is resulting in the low fill factor of the devices (Figure 13).

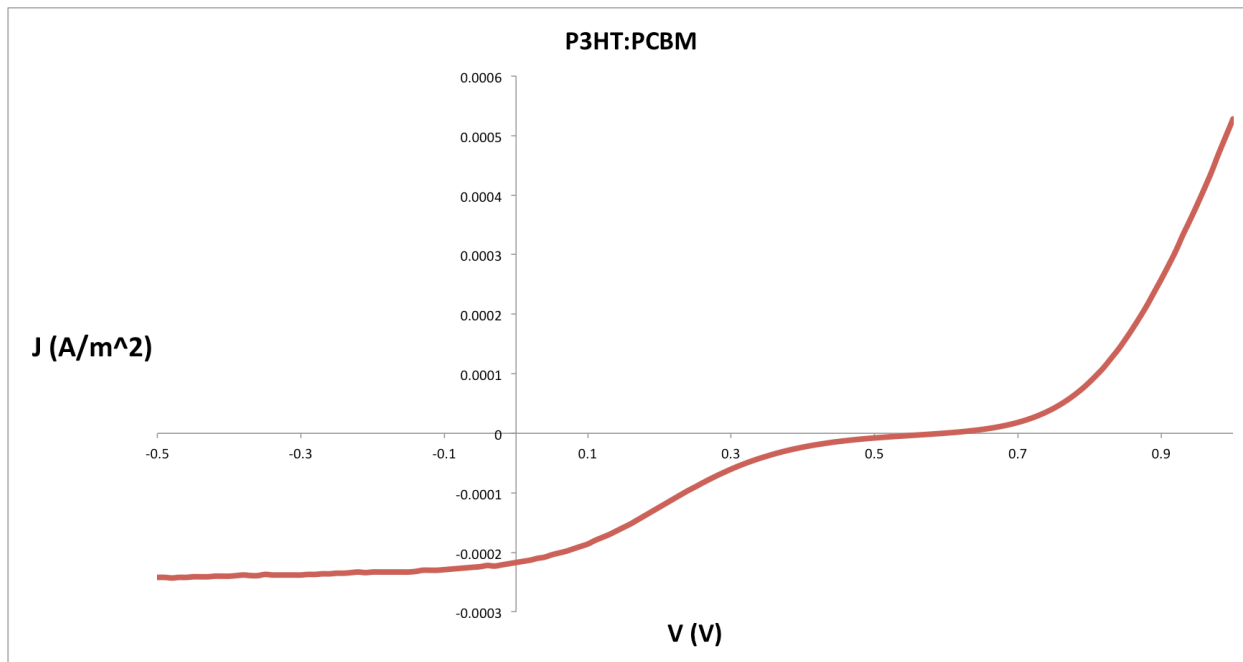


Figure 12. “S” shaped curve resulting in devices with unexpectedly low fill factor.

The S-shaped curve has been shown to result from uneven charge extraction in the device. One cause for this uneven charge extraction may be PCBM phase segregation during solvent evaporation, specifically during the annealing step. This segregation of PCBM results in poor contact between the PCBM component of the BHJ and the cathode, thereby reducing electron extraction rate and creating an imbalance in charge extraction behavior.^[15] Uneven charge extraction may also occur as a result of poor matching of the work functions of the electrodes to the active layer. Specifically, the work function of ITO is vulnerable to modification *via* extended plasma treatment.^[23]

3.3.2 Fullerene Comparison

Devices had previously been fabricated using the same fabrication scheme as the P3HT:PCBM system, but with fullerene molecules used as the acceptor component instead of PCBM molecules. While these P3HT:fullerene devices did not perform exceptionally well due to their low V_{oc} and J_{sc} values, they exhibited much higher fill factors than the initial P3HT:PCBM devices (Figure 13). This comparison suggested that the root of the problem might lie in the

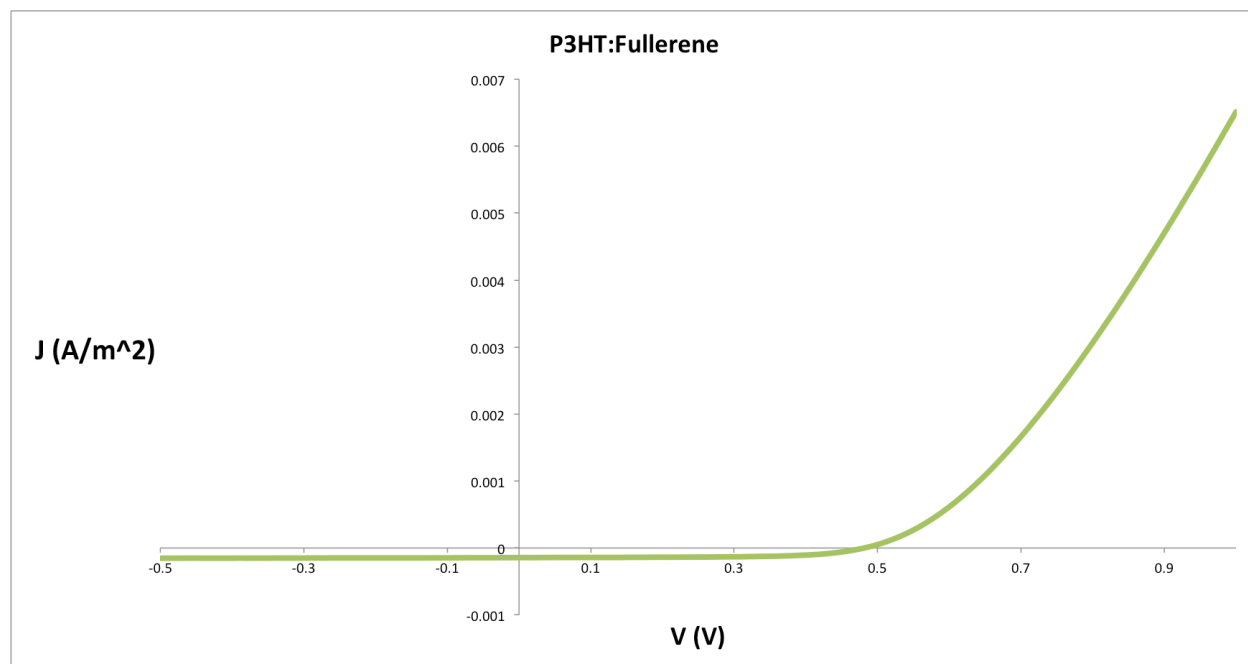


Figure 13. Fullerene based devices did not exhibit an “S” shaped curve, and as a result had much higher FF.

PCBM component of the OPV. In order to determine whether this was simply a materials issue, PCBM was borrowed from the Jen group at the University of Washington and devices were fabricated as before.

3.3.3 Role of PCBM in J-V Curve Shape

Devices fabricated using the borrowed PCBM exhibited an increased FF of 0.54. The V_{oc} of these devices were near literature values, and the J_{sc} were improved from before. The comparison between different sets of PCBM may be seen below (Figure 14). Both sets of devices were fabricated identically.

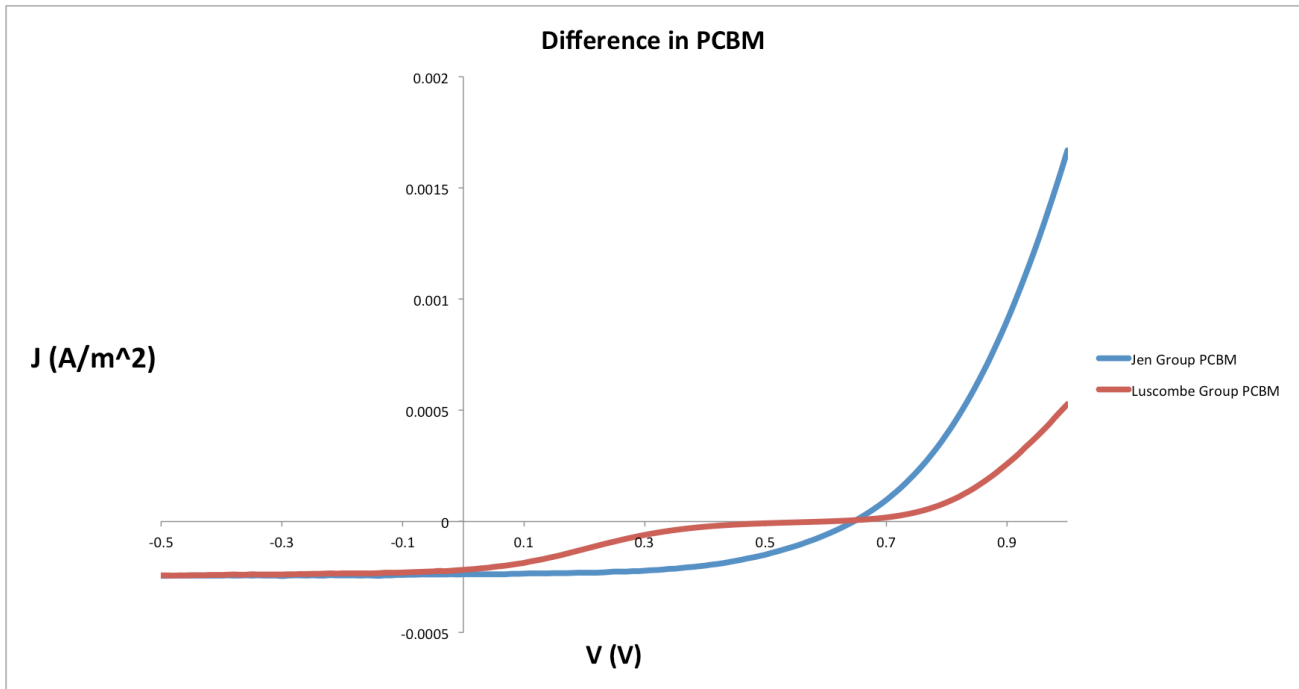


Figure 14. New PCBM did not exhibit “S” shaped curve.

3.4 Conclusion

Device parameters for each of the sets of devices described in 3.3 reveal that the PCBM used in the initial set of devices may have played a role in the poor initial performance of the OPVs.

Table 8. OPV device parameters for all sets of device. Note the low FF in the first set of devices. FF is much improved for both the second and third set of devices, leading to improved PCE.

	V_{oc} (V)	J_{sc} (A/m^2)	FF	PCE (%)	
Average	0.58	63	0.20	0.72	Luscombe Group PCBM
St. dev.	0.05	5	0.03	0.08	
Average	0.476	39	0.62	1.2	Fullerene
St. dev.	0.005	4	0.02	0.1	
Average	0.645	70	0.54	2.4	Jen Group PCBM
St. dev.	0.003	4	0.01	0.1	

While a PCE of 2.4% is not quite in the range of expected values, previous work done by Laura Corcoles, a visiting researcher from the Institut de Ciencia de Materials de Barcelona, showed that the age of the PEDOT:PSS solution used in device fabrication may play a large role in recorded device efficiencies. PEDOT:PSS is generally accepted to have a shelf life of around 6 months, and the material used in this device fabrication was 8 months old, potentially explaining the gap the deviation from expected efficiency. At this stage, the next step is to fabricate devices using new PCBM and PEDOT:PSS to determine whether the low PCE values are an inherent material problem or if there is a problem at some stage in the fabrication flow. Once the fabrication process has been confirmed to be reproducible, it will be time to move on to testing different material systems that have been synthesized by our collaborating groups. SCLC will then be used to determine mobility values of those systems in an OPV architecture.

3.5 P3HT:PCBM Summary

The performance of P3HT:PCBM OPVs was investigated in order to ensure that reproducible OPV fabrication was being conducted, as a preliminary step before moving onto other material systems. Initial devices were found to have very poor performance, largely due to a low fill factor caused by an “S” shaped J-V curve. This “S” shaped curve was thought to be caused by uneven charge extraction in the film, either due to PCBM segregation during solvent evaporation or due to modification of ITO work function by extended plasma treatment. By switching the PCBM used in the first set of devices with a fullerene acceptor, the “S” shape was eliminated, greatly increasing the FF of the devices. This observation suggested that the initial batch of PCBM may have played a role in the “S” shaped curve, so a different set of PCBM was borrowed from a collaborating group and used in a new set of P3HT:PCBM devices. These new devices exhibited performance parameters much closer to literature values, but still slightly lower than expected. This difference in performance was attributed to the age of the PEDOT:PSS solution used in fabrication due to previous work done by a collaborating group member suggesting this to be the case. In order to test this theory, new PEDOT:PSS has been purchased, and devices should be fabricated using it and compared to literature values. If the efficiency issue is identified as being rooted in the materials used, the fabrication procedure will be labeled as reproducible, and fabrication of new OPVs using materials sent by collaborating groups may begin. SCLC measurements will then be conducted on these new OPVs in order to gain valuable information regarding the charge transport characteristics of the devices, which will hopefully give greater insight into the charge transport imbalance origin of the “S” shaped curve as well.

Chapter 4. Self-healing Semiconductors

4.1 Introduction

While the bulk of this work has focused on strict device applications of organic semiconductors, and how to characterize those devices, previous research into potential self-healing capabilities of organic semiconductors is worth mentioning. Unlike their inorganic counterparts, organic semiconductors have the unique capability to exhibit self-healing behavior through thiol-disulfide bond exchange, restoring thin film integrity after mechanical damage or breakdown due to excessive photo irradiation. This potential could spur organic semiconductor based devices, such as solar cells, towards increased longevity, durability, and applicability in a wider range of conditions. P3HT is an excellent choice to investigate this behavior, as it is a well-understood organic semiconductor and can be easily thiol end group functionalized.^[24]

It is well understood that thiol-disulfide exchange reactions may take place in the presence of oxidizing or reducing environments (Figure 15). This reversible cross-linking has

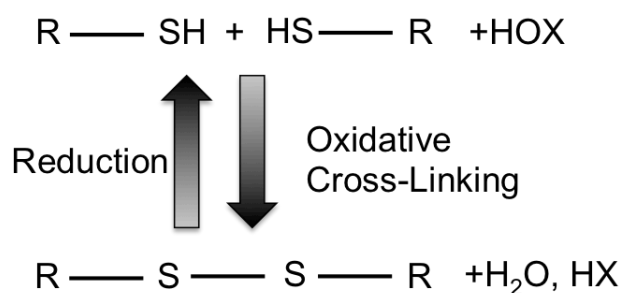


Figure 15. Thiol-disulfide redox reaction scheme.

been used in dynamically reversible systems in order to increase stability and rigidity of polymer systems, and can be used for self-healing as well if the polymer is in an oxidative environment.^[25,26] The thiol-disulfide exchange has also been shown to be able to occur *via* a

radical thiyl pathway in the absence of catalysis in ambient conditions, allowing for more practical applications of self healing (Figure 16).^[27]

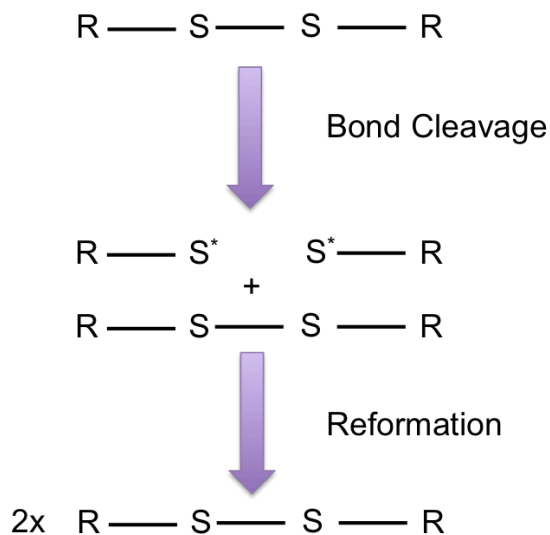


Figure 16. Disulfide bond reformation via a radical thiyl pathway following disulfide bond cleavage.

4.2 Methods

4.2.1 Film Preparation

Thiol terminated P3HT was synthesized according to literature procedures^[24]. Films were spin coated onto cleaned silicon substrates at 1500 rpm for 60 s using a solution concentration of 5 mg/mL of P3HT in chloroform. Prior to spin coating, solutions were exposed to UV light for 30 min in order to encourage oxidation and formation of disulfide bonds between molecules.^[28] Gold contacts were deposited through a transistor shadow mask with the same deposition conditions as listed in section 2.2.2.

4.2.2 Film Testing

Devices were tested and mobility values recorded prior to inducing mechanical damage, using a Signatone Probe Station in combination with a Hewlett Packard 4145B Semiconductor Parameter Analyzer. Devices were then scratched through the transistor channel using the tip of one of the probes, and tested again. Devices were then allowed to remain in ambient conditions for 24 h before follow up testing.

4.3 Results and Discussion

Initial device mobilities were recorded in the range of $2.0\text{-}2.5 \times 10^{-5} \text{ cm}^2/(\text{V}\cdot\text{s})$. These values were noted to be much lower than literature values, likely due to the lack of fabrication optimization, and were recorded only as a comparison against mobilities to be obtained after mechanical damage and attempted healing. Upon scratching, devices did not exhibit transistor characteristics, and I_D did not increase with increasing V_D or V_G . The devices were then tested again after 24 h inside of the glovebox, and were still found to be non-operational. Scratching was still evident optically, and so healing was noted not to have occurred.

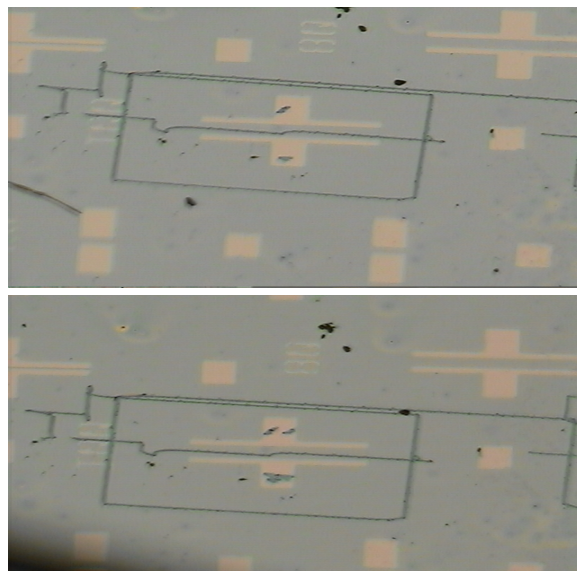


Figure 17. Image of initial scratch (top) and scratch after 24 h in glovebox environment (bottom). No healing was observed.

There are multiple reasons that this film may not have exhibited self-healing. In order for a scratch to heal, the molecules on each side of the scratch must be able to traverse the scratch and contact one another. The width of a scratch that can be filled is determined in part by the viscosity and flow behavior of the polymer. A rigid polymer will not be able to flow to fill the scratch, and therefore the film will not be able to heal.^[27] Additionally, the self healing reaction is based on the interaction between thiyl radicals resulting from disulfide cleavage. In the oxidized thiol terminated version of the linear polymer P3HT, it is not likely that there are sufficient disulfide linkages to induce any significant healing. This problem may be overcome by functionalizing the alkyl side chains of the P3HT to increase the thiol count of the polymer and thereby the self healing capability as well.^[25]

4.4 Conclusions

Self-healing behavior was not identified in the thiol functionalized P3HT thin films investigated. Further optimization of the P3HT variant to be used in this study is likely to be necessary before a film will be expected to recover from large scale mechanical damage.

4.5 Self-Healing Semiconductor Summary

Thiol terminated P3HT was synthesized and oxidized to form disulfide bonds between molecules. Thin films of the material were deposited in OTFT architectures, and charge transport properties of the material were recorded before and after mechanical damage, and then once more after a 24 h healing period. Devices did not function after mechanical damage, and showed no improvement after 24 h. Incomplete oxidation, lack of sufficient thiol end groups, and the large size of the scratch investigated are all suspected to have played a part in this lack of self-

healing. In order to find the root of the problem, functionalization of P3HT alkyl side chains should be performed, followed by oxidation and characterization of the oxidized product to ensure a high degree of disulfide bond formation. Initial scratching should start on a very small scale, ideally coming from an AFM tip in contact mode, in order to determine the size scale of mechanical damage that this system is capable of healing.

Chapter 5. Concluding Remarks

Organic semiconductors have great potential for use in low cost, high performance devices such as OPVs and OTFTs. This work demonstrates the dramatic increase in recorded charge carrier mobilities that can result from device fabrication process optimization, revealing the importance of optimizing each material system of interest. The reproducibility of OPVs are investigated, and the importance of balanced charge extraction is apparent in the P3HT:PCBM system analyzed. Charge carrier imbalance may result from phase segregation during device annealing and solvent evaporation, and may also be influenced by ITO substrate preparation methods. Self-healing behavior of organic semiconductors is also discussed, with further work being necessary to fully determine the viability of this self-healing behavior in devices and to quantify the efficacy of self-healing behavior at recovering electrical and mechanical properties of organic semiconducting thin films after damage.

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